Allwinner H5 Datasheet

Quad-Core OTT Box Processor

Revision 1.0

May.20,2016

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Revision History

Revision	Date	Description
1.0	May. 20,2016	Initial Release Version

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About This Documentation

The documentation describes features of each module, pin/signal characteristics, current consumption, PLL electrical characteristics, the interface timing, thermal and package of H5 processor. The documentation is intended to provide guidance to the hardware designers for electronics or sales personnel for electronic components. This documentation assumes that the reader has a background in electronic components.

1. Overview

The Allwinner H5 is a highly cost-efficient quad-core OTT Box processor, which is a part of growing home entertainment products that offer high-performance processing with a high degree of functional integration.

The H5 processor has some very exciting features, for example:

- **CPU**: Quad-core ARM Cortex™-A53 Processor, a power-efficient ARM v8 architecture, it has 64 and 32bit execution states for scalable high performance ,which includes a NEON multimedia processing engine.
- **Graphics**: The hexa-core ARM Mali450 GPU including dual Geometry Processors(GP) and quad Pixel Processors(PP), provides users with superior experience in video playback and mainstream game; OpenGL ES2.0 and OpenVG1.1 standards are supported.
- **Video Engine**: H5 provides multi-format high-definition video encoder/decoder with dedicated hardware, including H.265 decoder by 4K@30fps , H.264 decoder by 4K@30fps, MPEG1/2/4 decoder by 1080p@60fps, VP8/AVS jizhun decoder by 1080p@60fps, VC1 decoder by 1080p@30fps, H.264 encoder by 1080p@60fps.
- **Display Subsystem**: Supports DE2.0 for excellent display experience, and two display interfaces for HDMI1.4 and CVBS display.
- **Memory Controller**: The processor supports many types of external memory devices, including DDR3/DDR3L, NAND Flash(MLC,SLC,TLC,EF),Nor Flash, SD/SDIO/MMC including eMMC up to rev5.1.
- **Security System**: The processor delivers hardware security features that enable trustzone security system, Digital Rights Management(DRM) , information encryption/decryption, secure boot, secure JTAG and secure efuse.
- **Interfaces**: The processor has a broad range of hardware interfaces such as parallel CMOS sensor interface, 10/100/1000Mbps EMAC with FE PHY, USB OTG v2.0 operating at high speed(480Mbps) with PHY, USB Host with PHY and a variety of other popular interfaces(SPI,UART,CIR,TSC,TWI,SCR).

2. Features

2.1. Processor Features

2.1.1. CPU Architecture

- Quad-core ARM Cortex™-A53 MPCore™ Processor
- Thumb-2 Technology
- Supports NEON Advanced SIMD(Single Instruction Multiple Data)instruction for acceleration of media and signal processing functions
- Supports Large Physical Address Extensions(LPAE)
- VFPv4 Floating Point Unit
- Independent 32KB L1 Instruction cache and 32KB L1 Data cache
- Shared 512KB L2-cache

2.1.2. GPU Architecture

- Hexa-core ARM Mali450 GPU
- Dual Geometry Processors with 32KB L2 cache
- Quad Pixel Processors with 128KB L2 cache
- Concurrent multi-core processing
- 3000Mpix/sec and 163Mtri/sec
- Full scene over-sampled 4X anti-aliasing engine with no additional bandwidth usage
- OpenGL ES 1.1/2.0 and OpenVG 1.1 support

2.1.3. Memory Subsystem

2.1.3.1. Boot ROM

- On chip ROM
- Supports secure and non-secure access boot
- Supports system boot from the following devices:
  - NAND Flash
  - SD/TF card
  - eMMC
  - Nor Flash

- Supports system code download through USB OTG

2.1.3.2. SDRAM

- Compatible with JEDEC standard DDR3/DDR3L SDRAM
- Supports clock frequency up to 667MHz(DDR3-1333)
- 32-bit bus width
- Up to 3GB address space
- Supports 2 chip selects
- 16 address signal lines and 3 bank signal lines
- Supports Memory Dynamic Frequency Scale(MDFS)
- Random read or write operation is supported

2.1.3.3. NAND Flash

- Compliant with ONFI 2.3 and Toggle 1.0
- Up to 2 flash chips
- 8-bit data bus width
- Up to 64-bit ECC per 1024 bytes
- Supports 1024, 2048, 4096, 8192, 16K bytes size per page
- Supports SLC/MLC/TLC flash and EF-NAND memory
- Supports SDR, ONFI DDR and Toggle DDR NAND
- Embedded DMA to do data transfer
- Supports data transfer together with normal DMA

2.1.3.4. SMHC

- Up to 3 SD/MMC host controller(SMHC) interfaces
- Complies with eMMC standard specification V5.1, SD physical layer specification V3.0, SDIO card specification V3.0
- 1-bit or 4-bit data bus transfer mode for SD/TF cards up to 50MHz in SDR mode
- 1-bit or 4-bit data bus transfer mode for connecting to an external Wi-Fi module up to 150MHz in SDR mode and 50MHz in DDR mode
- 1-bit ,4-bit or 8-bit data bus transfer mode for MMC cards up to 150MHz in SDR mode or 100MHz in DDR mode
- Supports block size of 1 to 65535 bytes
- Embedded special DMA to do data transfer
- Supports hardware CRC generation and error detection

2.1.4. System Peripherals

2.1.4.1. Timer

- 2 on-chip Timers with interrupt-based operation
- 1 watchdog to generate reset signal or interrupt
- Two 33-bit Audio/Video Sync(AVS) Counter to synchronize video and audio in the player

2.1.4.2. High Speed Timer

- 1 High Speed Timer with 56-bit counter
- 56-bit counter that can be separated to 24-bit high register and 32-bit low register
- Clock source is synchronized with AHB clock, much more accurate than other timers

2.1.4.3. RTC

- Time,calendar
- Counters second,minutes,hours,day,week,month and year with leap year generator
- Alarm:general alarm and weekly alarm
- One 32KHz fanout

2.1.4.4. GIC

- Supports 16 Software Generated Interrupts(SGIs), 16 Private Peripheral Interrupts(PPIs) and 125 Shared Peripheral Interrupts(SPIs)

2.1.4.5. DMA

- Up to 12-channel DMA
- Interrupt generated for each DMA channel
- Transfers data width of 8/16/32/64-bit
- Supports linear and IO address modes
- Programs the DMA burst size
- Supports data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory

2.1.4.6. CCU

- 9 PLLs
- Supports an external 24MHz crystal oscillator and an on-chip 16MHz RC oscillator
- Supports clock configuration and clock generated for corresponding modules

- Supports software-controlled clock gating and software-controlled reset for corresponding modules

2.1.4.7. PWM

- Supports outputting two kinds of waveform: continuous waveform and pulse waveform
- 0% to 100% adjustable duty cycle
- Up to 24MHz output frequency

2.1.4.8. Thermal Sensor

- Temperature Accuracy : ±3℃ from 0℃ to +100℃, ±5℃ from -20℃ to +125℃
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Averaging filter for thermal sensor reading
- 2 temperature-sensing cell embedded :sensor0 for CPU,sensor1 for GPU

2.1.4.9. KEYADC

- Analog to digital converter with 6-bit resolution for key application
- Maximum sampling frequency up to 250 Hz
- Supports general key, hold key and already hold key
- Supports single , normal and continuous work mode

2.1.4.10. Message Box

- Two users for Message Box instance
- Eight Message Queues for the MSGBox instance
- Each of Queues could be configured as transmitter or receiver for user
- Two interrupts for the MSGBox instance
- Register polling for the MSGBox instance
- 32-bit message width
- Four-message FIFO depth for each message queue

2.1.4.11. Spinlock

- 32 spinlocks
- Two kinds of status of lock register: TAKEN and NOT TAKEN

2.1.4.12. Crypto Engine(CE)

- Supports symmetrical algorithm: AES, DES, TDES

- Supports hash algorithm:SHA-1/SHA-224/SHA-256,MD5,HMAC
- Supports 160-bit hardware PRNG with 175-bit seed
- Supports 256-bit TRNG
- Supports ECB,CBC, CTR, CTS modes for AES
- Supports ECB, CBC, CTR modes for DES
- Supports ECB, CBC, CTR modes for TDES
- 128-bit, 192-bit and 256-bit key size for AES
- Embedded special DMA to do data transfer

2.1.4.13. Security ID(SID)

- Supports 2K-bit EFUSE for chip ID and security application

2.1.4.14. CPU Configuration

- Configure related CPU parameters, including power on, reset, cache, debug, and check the status of CPU
- One 64-bit common counter

2.1.5. Display Subsystem

2.1.5.1. DE2.0

- Output size up to 4096x4096
- Supports four alpha blending channel for main display, two channel for aux display
- Supports four overlay layers in each channel, and has a independent scaler
- Supports potter-duff compatible blending operation
- Supports input format YUV422/YUV420/YUV411/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555 and RGB565
- Supports Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports SmartColor 2.0 for excellent display experience
  - Adaptive edge sharping
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify
- Supports writeback for high efficient dual display

2.1.5.2. Display Output

- Supports HDMI V1.4 output up to 4K@30fps
  - Compatible with HDMI 1.4 specification
  - Compatible with HDCP 1.2 for HDMI
  - Supports EDID block read by DDC

- Supports HPD
- Integrated CEC hardware
- Supports TMDS clock from 27MHz to 297MHz
- Supports RGB888,YUV444 video formats with only 8bit color depth
  4K@30Hz
  1920 x 1080p@50/60Hz
  1920 x 1080p@24Hz
  1920 x 1080i@50/60Hz
  1280 x 720p@50/60Hz
  720 x 480p@60Hz
  720 x 576p@50Hz
  3D Frame Packing 1920 x 1080p@24Hz
- Supports L-PCM audio format
  Up to 192KHz IEC-60958 audio sampling rate
  Maximum 24bit, 8 channel
- Supports IEC-61937 compressed audio format

• Supports TV CVBS output
  - Standard NTSC-M and PAL-B,D,G,H,I output
  - Plug status auto detecting

2.1.6. Video Engine

2.1.6.1. Video Decoder

• Supports multi-format video playback, including:
  - H.265 MP/L5.0: 4K@30fps
  - H.264 BP/MP/HP Level4.2: 4K@30fps
  - H.263 BP: 1080p@60fps
  - MPEG1 MP/HL: 1080p@60fps
  - MPEG2 MP/HL: 1080p@60fps
  - MPEG4 SP/ASP L5: 1080p@60fps
  - Sorenson Spark: 1080p@60fps
  - VP8 N/A: 1080p@60fps
  - VC1 SP/MP/AP: 1080p@30fps
  - AVS/AVS+ jizhun: 1080p@60fps
  - xvid N/A: 1080p@60fps
  - MJPEG: 1080p@30fps
• Supports 1080p blu-ray 3D
• Supports 3D size:3840x1080,1920x2160
• Supports decoding output format:YV12

2.1.6.2. Video Encoder

- Supports H.264 video encoder up to 1080p@60fps
- Supports input picture size up to 4800x4800
- Supports input format: tiled (128x32)/YU12/YV12/NU12/NV12/ARGB/YUYV
- Supports Alpha blending
- Supports thumb generation
- Supports 4x2 scaling ratio: from 1/16 to 64 arbitrary non-integer ratio
- Supports rotated input

2.1.7. Image Subsystem

2.1.7.1. CSI

- Supports 8-bit YUV422 CMOS sensor interface
- Supports CCIR656 protocol for NTSC and PAL
- Up to 5M pixel camera sensor
- Supports video capture resolution up to 1080p@30fps

2.1.8. Audio Subsystem

2.1.8.1. Audio Codec

- Two audio digital-to-analog(DAC) channels
  - 100 ± 3 dB SNR@A-weight
  - Supports ADC sample rate from 8 KHz to 192 KHz
- Two audio analog-to-digital(ADC) channels
  - 93 ± 3 dB SNR@A-weight
  - Supports ADC sample rate from 8 KHz to 48 KHz
- Supports analog/ digital volume control
- Supports Dynamic Range Controller(DRC) adjusting the DAC playback output
- Supports Dynamic Range Control(DRC) adjusting the ADC recording input
- Three audio inputs:
  - Two differential microphone inputs
  - One stereo Line-in L/R channel input
- One audio output: Stereo line-out L/R channel output

2.1.8.2. I2S/PCM

- 2 I2S/PCM controllers
- Compliant with standard Inter-IC sound(I2S) bus specification

- Compliant with left-justified, right-justified, PCM mode, and TDM(Time Division Multiplexing) format
- Supports 8-channel in TDM mode
- Full-duplex synchronous work mode
- Mater and slave mode configured
- Clock up to 100 MHz
- Adjustable audio sample resolution from 8-bit to 32-bit
- Sample rate from 8 KHz to 192 KHz
- Supports 8-bit u-law and 8-bit A-law companded sample
- Supports programmable PCM frame width:1 BCLK width(short frame) and 2 BCLKs width(long frame)
- One 128 depth x 32-bit width FIFO for data transmit, one 64 depth x 32-bit width FIFO for data receive
- Programmable FIFO thresholds

2.1.8.3. One Wire Audio(OWA)

- IEC-60958 transmitter functionality
- Compliance with S/PDIF Interface
- Supports channel status insertion for the transmitter
- Hardware parity generation on the transmitter
- One 32×24 bits FIFO (TX) for audio data transfer
- Programmable FIFO thresholds

2.1.9. External Peripherals

2.1.9.1. USB

- One USB 2.0 OTG,with integrated USB PHY
  - Complies with USB2.0 Specification
  - Supports High-Speed (HS,480Mbps),Full-Speed(FS,12Mbps) and Low-Speed(LS,1.5Mbps) in host mode
  - Complies with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface(OHCI) Specification, Version 1.0a for host mode
  - Up to 8 User-Configurable Endpoints in device mode
  - Supports point-to-point and point-to-multipoint transfer in both host and peripheral mode
- Three USB Host, with integrated USB PHY
  - Complies with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface(OHCI) Specification, Version 1.0a.

2.1.9.2. Ethernet

- Integrated an internal 10/100M PHY
- Supports 10/100/1000Mbps data transfer rate
- Supports MII/RGMII/RMII interface
- Supports full-duplex and half-duplex operation

- Programmable frame length
- Automatic CRC and pad generation controllable on a per-frame basis
- Options for Automatic Pad/CRC Stripping on receive frames
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Programmable Inter Frame Gap (40-96 bit times in steps of 8)
- Supports a variety of flexible address filtering modes

2.1.9.3. CIR

- A flexible receiver for IR remote
- Programmable FIFO threshold

2.1.9.4. UART

- Up to 5 UART controllers, one UART for CPUx debug, one UART for CPUs debug, others for UART applications
- UART0: 2-wire; UART1/2/3: 4-wire; S_UART: 2-wire
- Compliant with industry-standard 16450 and 16550 UARTs
- Supports word length from 5 to 8 bits, an optional parity bit and 1,1.5 or 2 stop bits
- Programmable parity(even, odd and no parity)
- 64-byte Transmit and receive data FIFOs for all UART

2.1.9.5. SPI

- Up to 2 SPI controllers
- Full-duplex synchronous serial interface
- Master/Slave configurable
- Mode0~3 are supported for both transmit and receive operations
- Two 64-byte FIFO for SPI-TX and SPI-RX operation
- DMA-based or interrupt-based operation supported
- Polarity and phase of the chip select(SPI_SS) and SPI_Clock(SPI_SCLK) are configurable
- The maximum frequency is 100MHz
- Supports single and dual read mode

2.1.9.6. TWI

- Up to 4 TWI(Two Wire Interface) controllers
- Supports Standard mode(up to 100K bps) and Fast mode(up to 400K bps)
- Master/Slave configurable
- Allows 10-bit addressing transactions
- Perform arbitration and clock synchronization
- Allows operation from a wide range of input clock frequencies

2.1.9.7. TSC

- Up to 4 TSC(Transport Stream Controller)
- Compliant with the industry-standard AMBA Host Bus(AHB) Specification, Revision 2.0.Supports 32-bit Little Endian bus
- Supports DVB-CSA V1.1 Descrambler
- One external Synchronous Parallel Interface(SPI) or one external Synchronous Serial Interface(SSI)
- Configurable SPI and SSI timing parameters
- Hardware packet synchronous byte error detecting
- Hardware PCR packet detecting

2.1.9.8. SCR

- Up to 2 SCR(Smart Card Reader) controllers
- Supports APB slave interface for easy integration with AMBA-based host systems
- Supports the ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) Specifications
- Supports adjustable clock rate and bit rate
- Configurable automatic byte repetition
- Supports asynchronous half-duplex character transmission and block transmission
- Supports synchronous and any other non-ISO 7816 and non-EMV cards
- Performs functions needed for complete smart card sessions, including:
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card

2.1.10. Package

- FBGA 347 balls, 0.65mm ball pitch, 14mm x 14mm

3. Block Diagram

Figure 3-1 shows the block diagram of H5 processor.

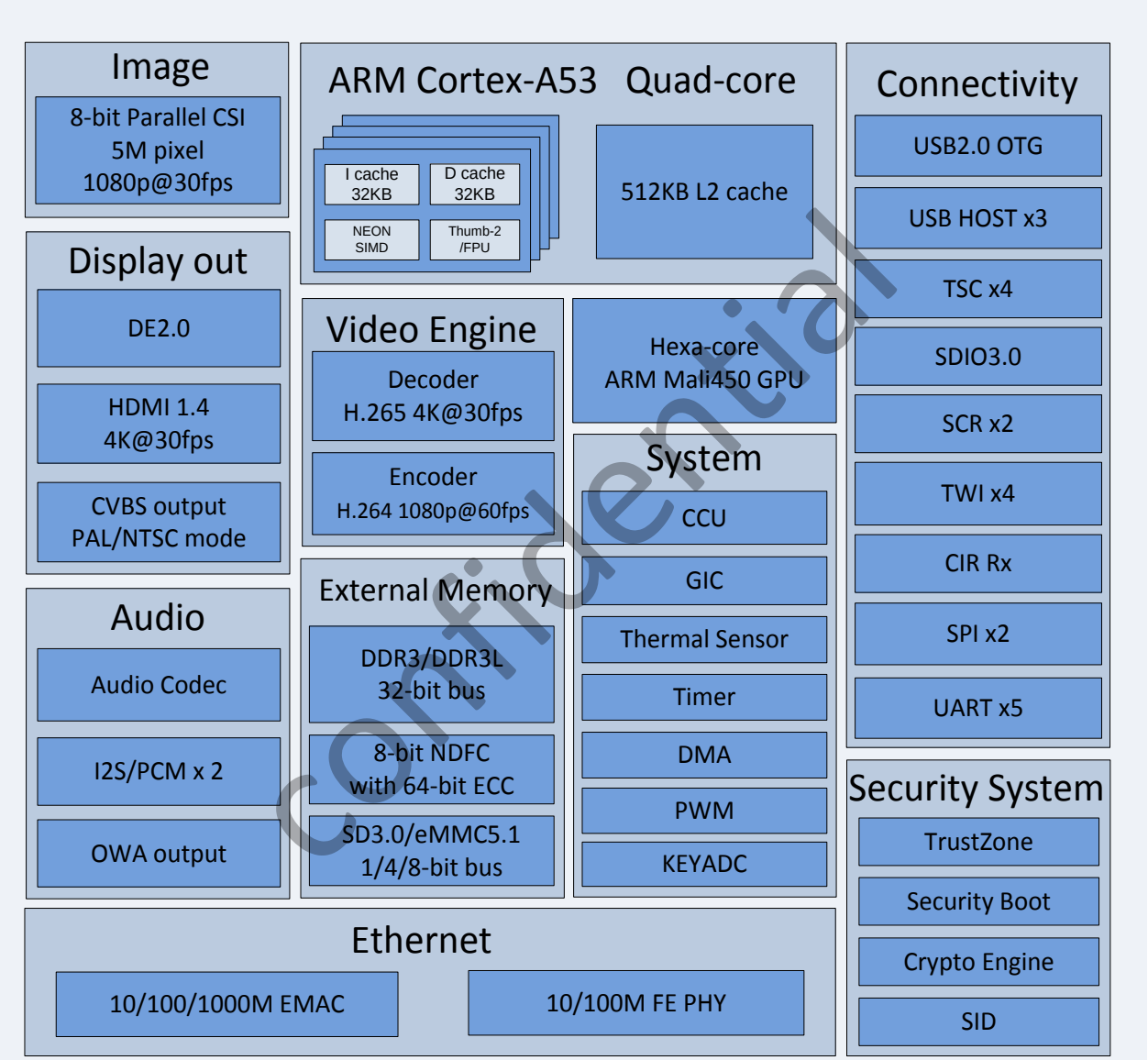


Figure 3-1. H5 Block Diagram

4. Pin Description

4.1. Pin Characteristics

Table 4-1 lists the characteristics of H5 Pins from seven aspects: BALL#, Pin Name, Default Function, Type, Reset State, Default Pull Up/Down, and Buffer Strength.

(1).**Ball#** : Package ball numbers associated with each signals.
(2).**Pin Name** : The name of the package pin.
(3).**Signal Name** : The signal name for that pin in the mode being used.
(4).**Function** : Multiplexing function number.
(5).**Ball Reset Rel. Function** : The function is automatically configured after RESET from low to high.
(6).**Type** : Denotes the signal direction
I (Input),
O (Output),
I/O(Input / Output),
OD(Open-Drain),
A (Analog),
AI(Analog Input),
AO(Analog Output),
A I/O(Analog Input/Output),
P (Power),
G (Ground)
(7).**Ball Reset State** : The state of the terminal at reset.
Z(High-impedance)
(8).**Pull Up/Down** : Denotes the presence of an internal pull-up or pull-down resistor. Pull-up(PU) and Pull-down(PD) resistors can be enabled or disabled via software.
(9).**Buffer Strength** : Defines drive strength of the associated output buffer.
(10).**Power Supply** : The voltage supply for the terminal's IO buffers.

Table 4-1. Pin Characteristics

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
DRAM									
T17	SA0	SA0	NA	NA	O	Z	NA	NA	VCC-DRAM
U18	SA1	SA1	NA	NA	O	Z	NA	NA	VCC-DRAM
V19	SA2	SA2	NA	NA	O	Z	NA	NA	VCC-DRAM
V20	SA3	SA3	NA	NA	O	Z	NA	NA	VCC-DRAM
V21	SA4	SA4	NA	NA	O	Z	NA	NA	VCC-DRAM
Y19	SA5	SA5	NA	NA	O	Z	NA	NA	VCC-DRAM
Y20	SA6	SA6	NA	NA	O	Z	NA	NA	VCC-DRAM
V15	SA7	SA7	NA	NA	O	Z	NA	NA	VCC-DRAM
W18	SA8	SA8	NA	NA	O	Z	NA	NA	VCC-DRAM
Y18	SA9	SA9	NA	NA	O	Z	NA	NA	VCC-DRAM
P19	SA10	SA10	NA	NA	O	Z	NA	NA	VCC-DRAM
N19	SA11	SA11	NA	NA	O	Z	NA	NA	VCC-DRAM
R18	SA12	SA12	NA	NA	O	Z	NA	NA	VCC-DRAM
V12	SA13	SA13	NA	NA	O	Z	NA	NA	VCC-DRAM
N17	SA14	SA14	NA	NA	O	Z	NA	NA	VCC-DRAM
R17	SA15	SA15	NA	NA	O	Z	NA	NA	VCC-DRAM
W17	SBA0	SBA0	NA	NA	O	Z	NA	NA	VCC-DRAM
T18	SBA1	SBA1	NA	NA	O	Z	NA	NA	VCC-DRAM
V17	SBA2	SBA2	NA	NA	O	Z	NA	NA	VCC-DRAM
U15	SCAS	SCAS	NA	NA	O	Z	NA	NA	VCC-DRAM
AA19	SCK	SCK	NA	NA	O	Z	NA	NA	VCC-DRAM
AA20	SCKB	SCKB	NA	NA	O	Z	NA	NA	VCC-DRAM
AA21	SCKE0	SCKE0	NA	NA	O	Z	NA	NA	VCC-DRAM
Y21	SCKE1	SCKE1	NA	NA	O	Z	NA	NA	VCC-DRAM
W20	SCS0	SCS0	NA	NA	O	Z	NA	NA	VCC-DRAM
W21	SCS1	SCS1	NA	NA	O	Z	NA	NA	VCC-DRAM
W11	SODT0	SODT0	NA	NA	O	Z	NA	NA	VCC-DRAM
V11	SODT1	SODT1	NA	NA	O	Z	NA	NA	VCC-DRAM
N20	SDQ0	SDQ0	NA	NA	I/O	Z	NA	NA	VCC-DRAM
P21	SDQ1	SDQ1	NA	NA	I/O	Z	NA	NA	VCC-DRAM
P20	SDQ2	SDQ2	NA	NA	I/O	Z	NA	NA	VCC-DRAM
U21	SDQ3	SDQ3	NA	NA	I/O	Z	NA	NA	VCC-DRAM
R19	SDQ4	SDQ4	NA	NA	I/O	Z	NA	NA	VCC-DRAM
T20	SDQ5	SDQ5	NA	NA	I/O	Z	NA	NA	VCC-DRAM
U19	SDQ6	SDQ6	NA	NA	I/O	Z	NA	NA	VCC-DRAM
U20	SDQ7	SDQ7	NA	NA	I/O	Z	NA	NA	VCC-DRAM
J19	SDQ8	SDQ8	NA	NA	I/O	Z	NA	NA	VCC-DRAM
H20	SDQ9	SDQ9	NA	NA	I/O	Z	NA	NA	VCC-DRAM
H21	SDQ10	SDQ10	NA	NA	I/O	Z	NA	NA	VCC-DRAM
J21	SDQ11	SDQ11	NA	NA	I/O	Z	NA	NA	VCC-DRAM
L20	SDQ12	SDQ12	NA	NA	I/O	Z	NA	NA	VCC-DRAM
L21	SDQ13	SDQ13	NA	NA	I/O	Z	NA	NA	VCC-DRAM
M21	SDQ14	SDQ14	NA	NA	I/O	Z	NA	NA	VCC-DRAM
M19	SDQ15	SDQ15	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y17	SDQ16	SDQ16	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA17	SDQ17	SDQ17	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y16	SDQ18	SDQ18	NA	NA	I/O	Z	NA	NA	VCC-DRAM
W15	SDQ19	SDQ19	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y14	SDQ20	SDQ20	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA14	SDQ21	SDQ21	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y13	SDQ22	SDQ22	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y12	SDQ23	SDQ23	NA	NA	I/O	Z	NA	NA	VCC-DRAM
W12	SDQ24	SDQ24	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA11	SDQ25	SDQ25	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y11	SDQ26	SDQ26	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y10	SDQ27	SDQ27	NA	NA	I/O	Z	NA	NA	VCC-DRAM
W9	SDQ28	SDQ28	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA8	SDQ29	SDQ29	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y8	SDQ30	SDQ30	NA	NA	I/O	Z	NA	NA	VCC-DRAM

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
Y7	SDQ31	SDQ31	NA	NA	I/O	Z	NA	NA	VCC-DRAM
M20	SDQM0	SDQM0	NA	NA	O	Z	NA	NA	VCC-DRAM
G20	SDQM1	SDQM1	NA	NA	O	Z	NA	NA	VCC-DRAM
AA18	SDQM2	SDQM2	NA	NA	O	Z	NA	NA	VCC-DRAM
AA12	SDQM3	SDQM3	NA	NA	O	Z	NA	NA	VCC-DRAM
R20	SDQS0	SDQS0	NA	NA	I/O	Z	NA	NA	VCC-DRAM
R21	SDQS0B	SDQS0B	NA	NA	I/O	Z	NA	NA	VCC-DRAM
K20	SDQS1	SDQS1	NA	NA	I/O	Z	NA	NA	VCC-DRAM
J20	SDQS1B	SDQS1B	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA15	SDQS2	SDQS2	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y15	SDQS2B	SDQS2B	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA9	SDQS3	SDQS3	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y9	SDQS3B	SDQS3B	NA	NA	I/O	Z	NA	NA	VCC-DRAM
V13	SRAS	SRAS	NA	NA	O	Z	NA	NA	VCC-DRAM
U16	SRST	SRST	NA	NA	O	Z	NA	NA	VCC-DRAM
T16	SVREF	SVREF	NA	NA	P	NA	NA	NA	VCC-DRAM
W13	SWE	SWE	NA	NA	O	Z	NA	NA	VCC-DRAM
V10	SZQ	SZQ	NA	NA	AI	Z	NA	NA	VCC-DRAM
L16,M16,N16,P16,P17,R16,T12,T13,T14,T15,U11	VCC-DRAM	VCC-DRAM	NA	NA	P	NA	NA	NA	NA
GPIOA									
D11	PA0	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		UART2_TX	2		O				
		JTAG_MS	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT0	6		I				
		IO Disable	7		OFF				
D5	PA1	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		UART2_RX	2		I				
		JTAG_CK	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT1	6		I				
		IO Disable	7		OFF				
D6	PA2	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		UART2_RTS	2		O				
		JTAG_DO	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT2	6		I				
		IO Disable	7		OFF				
E13	PA3	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		UART2_CTS	2		I				
		JTAG_DI	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT3	6		I				
		IO Disable	7		OFF				
F5	PA4	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		UART0_TX	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT4	6		I				
		IO Disable	7		OFF				
H6	PA5	Input	0	Function7	I	Z	PU/PD	20	VCC-IO

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		Output	1		O				
		UART0_RX	2		I				
		PWM0	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT5	6		I				
		IO Disable	7		OFF				
E14	PA6	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SIM0_PWREN	2		O				
		PCM0_MCLK	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT6	6		I				
		IO Disable	7		OFF				
D8	PA7	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SIM0_CLK	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT7	6		I				
		IO Disable	7		OFF				
F13	PA8	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SIM0_DATA	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT8	6		I				
		IO Disable	7		OFF				
D13	PA9	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SIM0_RST	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT9	6		I				
		IO Disable	7		OFF				
E11	PA10	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SIM0_DET	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT10	6		I				
		IO Disable	7		OFF				
F11	PA11	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		TWI0_SCK	2		I/O				
		DI_TX	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT11	6		I				
		IO Disable	7		OFF				
C13	PA12	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		TWI0_SDA	2		I/O				
		DI_RX	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT12	6		I				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		IO Disable	7		OFF				
E15	PA13	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SPI1_CS	2		I/O				
		UART3_TX	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT13	6		I				
		IO Disable	7		OFF				
G12	PA14	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SPI1_CLK	2		I/O				
		UART3_RX	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT14	6		I				
		IO Disable	7		OFF				
F14	PA15	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SPI1_MOSI	2		I/O				
		UART3_RTS	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT15	6		I				
		IO Disable	7		OFF				
D15	PA16	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SPI1_MISO	2		I/O				
		UART3_CTS	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT16	6		I				
		IO Disable	7		OFF				
C14	PA17	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		OWA_OUT	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT17	6		I				
		IO Disable	7		OFF				
B13	PA18	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		PCM0_SYNC	2		I/O				
		TWI1_SCK	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT18	6		I				
		IO Disable	7		OFF				
B14	PA19	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		PCM0_CLK	2		I/O				
		TWI1_SDA	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT19	6		I				
		IO Disable	7		OFF				
A13	PA20	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		PCM0_DOUT	2		O				
		SIM0_VPPEN	3		O				
		Reserved	4		NA				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		Reserved	5		NA				
		PA_EINT20	6		I				
		IO Disable	7		OFF				
A14	PA21	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		PCM0_DIN	2		I				
		SIM0_VPPPP	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT21	6		I				
		IO Disable	7		OFF				
GPIOC									
C15	PC0	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_WE	2		O				
		SPI0_MOSI	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C16	PC1	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_ALE	2		O				
		SPI0_MISO	3		I/O				
		SDC2_DS	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
B16	PC2	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_CLE	2		O				
		SPI0_CLK	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
B15	PC3	Input	0	Function7	I	PU	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_CE1	2		O				
		SPI0_CS	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
F16	PC4	Input	0	Function7	I	PU	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_CE0	2		O				
		Reserved	3		NA				
		SPI0_MISO	4		I/O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
A17	PC5	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_RE	2		O				
		SDC2_CLK	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
E16	PC6	Input	0	Function7	I	PU	PU/PD	20	VCC-PC
		Output	1		O				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		NAND_RB0	2		I				
		SDC2_CMD	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
A16	PC7	Input	0	Function7	I	PU	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_RB1	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
B18	PC8	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ0	2		I/O				
		SDC2_D0	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C17	PC9	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ1	2		I/O				
		SDC2_D1	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
D17	PC10	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ2	2		I/O				
		SDC2_D2	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C18	PC11	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ3	2		I/O				
		SDC2_D3	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
B17	PC12	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ4	2		I/O				
		SDC2_D4	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
B19	PC13	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ5	2		I/O				
		SDC2_D5	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
F17	PC14	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ6	2		I/O				
		SDC2_D6	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C19	PC15	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ7	2		I/O				
		SDC2_D7	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
H16	PC16	Input	0	Function7	I	PD	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQS	2		O				
		SDC2_RST	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
G15	VCC-PC	VCC-PC	NA	NA	P	NA	NA	NA	NA
GPIOD									
C21	PD0	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_RXD3/ MII_RXD3/ RMII_NULL	2		I				
		DI_TX	3		O				
		TS2_CLK	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
H17	PD1	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_RXD2/ MII_RXD2/ RMII_NULL	2		I				
		DI_RX	3		I				
		TS2_ERR	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
B20	PD2	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_RXD1/ MII_RXD1/ RMII_RXD1	2		I				
		Reserved	3		NA				
		TS2_SYNC	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
H18	PD3	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_RXD0/ MII_RXD0/ RMII_RXD0	2		I				
		Reserved	3		NA				
		TS2_DVLD	4		I				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
A20	PD4	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_RXCK/ MII_RXCK/ RMII_NULL	2		I				
		Reserved	3		NA				
		TS2_D0	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
F19	PD5	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_RXCTL/ MII_RXDV/ RMII_CRS_DV	2		I				
		Reserved	3		NA				
		TS2_D1	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
B21	PD6	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_NULL/ MII_RXERR/ RMII_RXER	2		I				
		Reserved	3		NA				
		TS2_D2	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
E18	PD7	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_TXD3/ MII_TXD3/ RMII_NULL	2		O				
		Reserved	3		NA				
		TS2_D3	4		I				
		TS3_CLK	5		I				
		Reserved	6		NA				
		IO Disable	7		OFF				
E20	PD8	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_TXD2/ MII_TXD2/ RMII_NULL	2		O				
		Reserved	3		NA				
		TS2_D4	4		I				
		TS3_ERR	5		I				
		Reserved	6		NA				
		IO Disable	7		OFF				
F21	PD9	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_TXD1/ MII_TXD1/ RMII_TXD1	2		O				
		Reserved	3		NA				
		TS2_D5	4		I				
		TS3_SYNC	5		i				
		Reserved	6		NA				
		IO Disable	7		OFF				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
H19	PD10	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_TXD0/ MII_TXD0/ RMII_TXD0	2		O				
		Reserved	3		NA				
		TS2_D6	4		I				
		TS3_DVLD	5		I				
		Reserved	6		NA				
		IO Disable	7		OFF				
F20	PD11	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_NULL/ MII_CRS/ RMII_NULL	2		I				
		Reserved	3		NA				
		TS2_D7	4		I				
		TS3_D0	5		I				
		Reserved	6		NA				
		IO Disable	7		OFF				
E19	PD12	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_TXCK/ MII_TXCK/ RMII_TXCK	2		I/O				
		Reserved	3		NA				
		SIM1_PWREN	4		O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
K17	PD13	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_TXCTL/ MII_TXEN/ RMII_TXEN	2		I/O				
		Reserved	3		NA				
		SIM1_CLK	4		O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
L17	PD14	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_NULL/ MII_TXERR/ RMII_NULL	2		O				
		Reserved	3		NA				
		SIM1_DATA	4		I/O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
K18	PD15	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_CLKIN/ MII_COL/ RMII_NULL	2		I				
		Reserved	3		NA				
		SIM1_RST	4		O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
L18	PD16	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		MDC	2		O				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		Reserved	3		NA				
		SIM1_DET	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
L19	PD17	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		MDIO	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
J15	VCC-PD	VCC-PD	NA	NA	P	NA	NA	NA	NA
GPIOE									
B10	PE0	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_PCLK	2		I				
		TS0_CLK	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
A10	PE1	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_MCLK	2		O				
		TS0_ERR	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
B11	PE2	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_HSYNC	2		I				
		TS0_SYNC	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C10	PE3	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_VSYNC	2		I				
		TS0_DVLD	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C9	PE4	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_D0	2		I				
		TS0_D0	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
E10	PE5	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_D1	2		I				
		TS0_D1	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		IO Disable	7		OFF				
D10	PE6	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_D2	2		I				
		TS0_D2	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C8	PE7	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_D3	2		I				
		TS0_D3	3		I				
		TS1_CLK	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C11	PE8	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_D4	2		I				
		TS0_D4	3		I				
		TS1_ERR	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C12	PE9	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_D5	2		I				
		TS0_D5	3		I				
		TS1_SYNC	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
E8	PE10	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_D6	2		I				
		TS0_D6	3		I				
		TS1_DVLD	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
A11	PE11	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_D7	2		I				
		TS0_D7	3		I				
		TS1_D0	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
B12	PE12	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_SCK	2		I/O				
		TWI2_SCK	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C7	PE13	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_SDA	2		I/O				
		TWI2_SDA	3		I/O				
		Reserved	4		NA				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C6	PE14	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		Reserved	2		NA				
		SIM1_VPPEN	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C5	PE15	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		Reserved	2		NA				
		SIM1_VPPPP	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
GPIOF									
D19	PF0	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SDC0_D1	2		I/O				
		JTAG_MS	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT0	6		I				
		IO Disable	7		OFF				
A19	PF1	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SDC0_D0	2		I/O				
		JTAG_DI	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT1	6		I				
		IO Disable	7		OFF				
D20	PF2	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SDC0_CLK	2		O				
		UART0_TX	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT2	6		I				
		IO Disable	7		OFF				
F18	PF3	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SDC0_CMD	2		I/O				
		JTAG_DO	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT3	6		I				
		IO Disable	7		OFF				
E21	PF4	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SDC0_D3	2		I/O				
		UART0_RX	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT4	6		I				
		IO Disable	7		OFF				
C20	PF5	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		SDC0_D2	2		I/O				
		JTAG_CK	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT5	6		I				
		IO Disable	7		OFF				
G18	PF6	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT6	6		I				
		IO Disable	7		OFF				
GPIOG									
J3	PG0	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_CLK	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT0	6		I				
		IO Disable	7		OFF				
L2	PG1	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_CMD	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT1	6		I				
		IO Disable	7		OFF				
H4	PG2	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_D0	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT2	6		I				
		IO Disable	7		OFF				
F3	PG3	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_D1	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT3	6		I				
		IO Disable	7		OFF				
C2	PG4	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_D2	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT4	6		I				
		IO Disable	7		OFF				
C1	PG5	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_D3	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT5	6		I				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		IO Disable	7		OFF				
G4	PG6	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		UART1_TX	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT6	6		I				
		IO Disable	7		OFF				
D3	PG7	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		UART1_RX	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT7	6		I				
		IO Disable	7		OFF				
C3	PG8	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		UART1_RTS	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT8	6		I				
		IO Disable	7		OFF				
E3	PG9	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		UART1_CTS	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT9	6		I				
		IO Disable	7		OFF				
M3	PG10	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		PCM1_SYNC	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT10	6		I				
		IO Disable	7		OFF				
D2	PG11	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		PCM1_CLK	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT11	6		I				
		IO Disable	7		OFF				
D1	PG12	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		PCM1_DOUT	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT12	6		I				
		IO Disable	7		OFF				
B1	PG13	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		PCM1_DIN	2		I				
		Reserved	3		NA				
		Reserved	4		NA				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		Reserved	5		NA				
		PG_EINT13	6		I				
		IO Disable	7		OFF				
H7	VCC-PG	VCC-PG	NA	NA	P	NA	NA	NA	NA
GPIO L									
N1	PL0	Input	0	Function7	I	PU	PU/PD	20	VCC-RTC
		Output	1		O				
		S_TWI_SCK	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT0	6		I				
		IO Disable	7		OFF				
M1	PL1	Input	0	Function7	I	PU	PU/PD	20	VCC-RTC
		Output	1		O				
		S_TWI_SDA	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT1	6		I				
		IO Disable	7		OFF				
P2	PL2	Input	0	Function7	I	Z	PU/PD	20	VCC-RTC
		Output	1		O				
		S_UART_TX	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT2	6		I				
		IO Disable	7		OFF				
R1	PL3	Input	0	Function7	I	Z	PU/PD	20	VCC-RTC
		Output	1		O				
		S_UART_RX	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT3	6		I				
		IO Disable	7		OFF				
N2	PL4	Input	0	Function7	I	Z	PU/PD	20	VCC-RTC
		Output	1		O				
		S_JTAG_MS	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT4	6		I				
		IO Disable	7		OFF				
R2	PL5	Input	0	Function7	I	Z	PU/PD	20	VCC-RTC
		Output	1		O				
		S_JTAG_CK	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT5	6		I				
		IO Disable	7		OFF				
T4	PL6	Input	0	Function7	I	Z	PU/PD	20	VCC-RTC
		Output	1		O				
		S_JTAG_DO	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT6	6		I				
		IO Disable	7		OFF				
T3	PL7	Input	0	Function7	I	Z	PU/PD	20	VCC-RTC

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		Output	1		O				
		S_JTAG_DI	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT7	6		I				
		IO Disable	7		OFF				
T2	PL8	Input	0	Function7	I	Z	PU/PD	20	VCC-RTC
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT8	6		I				
		IO Disable	7		OFF				
M6	PL9	Input	0	Function7	I	Z	PU/PD	20	VCC-RTC
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT9	6		I				
		IO Disable	7		OFF				
V2	PL10	Input	0	Function7	I	Z	PU/PD	20	VCC-RTC
		Output	1		O				
		S_PWM	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT10	6		I				
		IO Disable	7		OFF				
U2	PL11	Input	0	Function7	I	Z	PU/PD	20	VCC-RTC
		Output	1		O				
		S_CIR_RX	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT11	6		I				
		IO Disable	7		OFF				
System									
AA6	NMI	NMI	NA	NA	I	Z	PU/PD	NA	VCC-RTC
V6	RESET	RESET	NA	NA	I/O	Z	PU/PD	NA	VCC-RTC
T5	TEST	TEST	NA	NA	I	PD	PU/PD	NA	VCC-RTC
W6	UBOOT	UBOOT	NA	NA	I	PU	PU/PD	NA	VCC-RTC
A1	JTAG-SEL0	JTAG-SEL0	NA	NA	I	PU	PU/PD	NA	VCC-IO
B2	JTAG-SEL1	JTAG-SEL1	NA	NA	I	PU	PU/PD	NA	VCC-IO
ADC									
AA5	KEYADC	KEYADC	NA	NA	AI	NA	NA	NA	AVCC
TV-OUT									
F10	TVOUT	TVOUT	NA	NA	AO	NA	NA	NA	V33-TV
G9	V33-TV	V33-TV	NA	NA	P	NA	NA	NA	NA
EPHY									
A2	EPHY-LINK-LED	EPHY-LINK-LED	NA	NA	O	NA	NA	NA	EPHY-VCC
F7	EPHY-SPD-LED	EPHY-SPD-LED	NA	NA	O	NA	NA	NA	EPHY-VCC
F6	EPHY-RTX	EPHY-RTX	NA	NA	AI	NA	NA	NA	EPHY-VCC
A4	EPHY-RXN	EPHY-RXN	NA	NA	A I/O	NA	NA	NA	EPHY-VCC
B4	EPHY-RXP	EPHY-RXP	NA	NA	A I/O	NA	NA	NA	EPHY-VCC
A3	EPHY-TXN	EPHY-TXN	NA	NA	A I/O	NA	NA	NA	EPHY-VCC
B3	EPHY-TXP	EPHY-TXP	NA	NA	A I/O	NA	NA	NA	EPHY-VCC
G7	EPHY-VCC	EPHY-VCC	NA	NA	P	NA	NA	NA	NA
F8	EPHY-VDD	EPHY-VDD	NA	NA	P	NA	NA	NA	NA
HDMI									

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
G5	HCEC	HCEC	NA	NA	I/O	NA	NA	NA	VCC-HDMI
M2	HHPD	HHPD	NA	NA	I/O	NA	NA	NA	VCC-HDMI
H3	HSCL	HSCL	NA	NA	O	NA	NA	NA	VCC-HDMI
K3	HSDA	HSDA	NA	NA	I/O	NA	NA	NA	VCC-HDMI
G1	HTX0P	HTX0P	NA	NA	AO	NA	NA	NA	VCC-HDMI
F1	HTX0N	HTX0N	NA	NA	AO	NA	NA	NA	VCC-HDMI
H2	HTXIP	HTXIP	NA	NA	AO	NA	NA	NA	VCC-HDMI
G2	HTX1N	HTX1N	NA	NA	AO	NA	NA	NA	VCC-HDMI
J1	HTX2P	HTX2P	NA	NA	AO	NA	NA	NA	VCC-HDMI
J2	HTX2N	HTX2N	NA	NA	AO	NA	NA	NA	VCC-HDMI
F2	HTXCP	HTXCP	NA	NA	AO	NA	NA	NA	VCC-HDMI
E2	HTXCN	HTXCN	NA	NA	AO	NA	NA	NA	VCC-HDMI
J6	HVCC	VCC-HDMI	NA	NA	P	NA	NA	NA	NA
USB									
B5	USB-DM0	USB-DM0	NA	NA	A I/O	NA	NA	NA	VCC-USB
A5	USB-DP0	USB-DP0	NA	NA	A I/O	NA	NA	NA	VCC-USB
B7	USB-DM1	USB-DM1	NA	NA	A I/O	NA	NA	NA	VCC-USB
B6	USB-DP1	USB-DP1	NA	NA	A I/O	NA	NA	NA	VCC-USB
A8	USB-DM2	USB-DM2	NA	NA	A I/O	NA	NA	NA	VCC-USB
A7	USB-DP2	USB-DP2	NA	NA	A I/O	NA	NA	NA	VCC-USB
B9	USB-DM3	USB-DM3	NA	NA	A I/O	NA	NA	NA	VCC-USB
B8	USB-DP3	USB-DP3	NA	NA	A I/O	NA	NA	NA	VCC-USB
G11	VCC-USB	VCC-USB	NA	NA	P	NA	NA	NA	NA
Audio Codec									
U3	AGND	AGND	NA	NA	G	NA	NA	NA	NA
V3	AVCC	AVCC	NA	NA	P	NA	NA	NA	NA
W1	LINEINR	LINEINR	NA	NA	AI	NA	NA	NA	AVCC
V1	LINEINL	LINEINL	NA	NA	AI	NA	NA	NA	AVCC
Y3	LINEOUTR	LINEOUTR	NA	NA	AO	NA	NA	NA	AVCC
AA3	LINEOUTL	LINEOUTL	NA	NA	AO	NA	NA	NA	AVCC
W3	MBIAS	MBIAS	NA	NA	AO	NA	NA	NA	AVCC
Y1	MICIN1N	MICIN1N	NA	NA	AI	NA	NA	NA	AVCC
W2	MICIN1P	MICIN1P	NA	NA	AI	NA	NA	NA	AVCC
AA2	MICIN2N	MICIN2N	NA	NA	AI	NA	NA	NA	AVCC
Y2	MICIN2P	MICIN2P	NA	NA	AI	NA	NA	NA	AVCC
Y4	VRA1	VRA1	NA	NA	AO	NA	NA	NA	AVCC
W5	VRA2	VRA2	NA	NA	AO	NA	NA	NA	AVCC
V4	VRP	VRP	NA	NA	AO	NA	NA	NA	AVCC
Clock									
V5	X32KIN	X32KIN	NA	NA	AI	NA	NA	NA	VCC-RTC
U4	X32KOUT	X32KOUT	NA	NA	AO	NA	NA	NA	VCC-RTC
P3	X32KFOUT	X32KFOUT	NA	NA	AOD	NA	NA	NA	VCC-RTC
M4	RTC-VIO	RTC-VIO	NA	NA	AO	NA	NA	NA	VCC-RTC
K6	VCC-RTC	VCC-RTC	NA	NA	P	NA	NA	NA	NA
K2	X24MIN	X24MIN	NA	NA	AI	NA	NA	NA	VCC-PLL
K1	X24MOUT	X24MOUT	NA	NA	AO	NA	NA	NA	VCC-PLL
K4	X24MFOUT	X24MFOUT	NA	NA	AOD	NA	NA	NA	VCC-RTC
L5	PLLTEST	PLLTEST	NA	NA	AOD	NA	NA	NA	VCC-PLL
N3	VCC-PLL	VCC-PLL	NA	NA	P	NA	NA	NA	NA
Efuse									
G10	VDD-EFUSE	VDD-EFUSE	NA	NA	P	NA	NA	NA	NA
H11	VDD-EFUSEBP	VDD-EFUSEBP	NA	NA	O	NA	NA	NA	NA
Power									
J12	VDD-GPUFB	VDD-GPUFB	NA	NA	O	NA	NA	NA	NA
N8,P6,P7,P8,P9, R6,R7,R8,T6,T7, T8,U6,U9	VDD-CPUX	VDD-CPU	NA	NA	P	NA	NA	NA	NA
J7,J8	VDD-CPUS	VDD-CPU	NA	NA	P	NA	NA	NA	NA
H10,J10,J11,K10, K11,K12,L10,L11, L12,L13,L14	VDD-SYS	VDD-SYS	NA	NA	P	NA	NA	NA	NA
G13,G14,H13, H14,J14	VCC-IO	VCC-IO	NA	NA	P	NA	NA	NA	NA

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
Ground									
A21,AA1,G8,H12,H15,H8,J13,J16,J9,K13,K14,K15,K16,K7,K8,K9,L15,L8,L9,M10,M11,M12,M13,M14,M15,M5,M7,M8,M9,N10,N11,N12,N13,N14,N15,N7,N9,P10,P11,P12,P13,P14,P15,R10,R11,R12,R13,R14,R9,T11,T9	GND	GND	NA	NA	G	NA	NA	NA	NA

4.2. Signal Descriptions

H5 contains many peripheral interfaces. Many of the interfaces can multiplex up to eight functions. Pin-multiplexing configuration can refer to Table 4-1. Table 4-2 shows the detailed function description of every signal based on the different interface.

(1).**Signal Name**: The name of every signal.
(2).**Description**: The detailed function description of every signal.
(3).**Type**: Denotes the signal direction:
I (Input),
O (Output),
I/O(Input/Output),
OD(Open-Drain),
A (Analog),
AI(Analog Input),
AO(Analog Output),
A I/O(Analog Input/Output),
P (Power),
G (Ground)

Table 4-2. Signal Descriptions

Signal Name[1]	Description[2]	Type[3]
DRAM		
SDQ[31:0]	DRAM Bidirectional Data Line to the Memory Device	I/O
SDQS[3:0]	DRAM Active-High Bidirectional Data Strobes to the Memory Device	I/O
SDQSB[3:0]	DRAM Active-Low Bidirectional Data Strobes to the Memory Device	I/O
SDQM[3:0]	DRAM Data Mask Signal to the Memory Device	O
SCK	DRAM Active-High Clock Signal to the Memory Device	O
SCKB	DRAM Active-Low Clock Signal to the Memory Device	O
SCKE[1:0]	DRAM Clock Enable Signal to the Memory Device for Two Chip Select	O
SA[15:0]	DRAM Address Signal to the Memory Device	O
SWE	DRAM Write Enable Strobe to the Memory Device	O
SCAS	DRAM Column Address Strobe to the Memory Device	O
SRAS	DRAM Row Address Strobe to the Memory Device	O
SCS[1:0]	DRAM Chip Select Signal to the Memory Device	O
SBA[2:0]	DRAM Bank Address Signal to the Memory Device	O
SODT[1:0]	DRAM On-Die Termination Output Signal for Two Chip Select	O
SRST	DRAM Reset Signal to the Memory Device	O
SZQ	DRAM ZQ Calibration	AI
SVREF	DRAM Reference Input	P
VCC-DRAM	DRAM Power Supply	P

Signal Name[1]	Description[2]	Type[3]
System		
UBOOT	UBOOT Mode Select	I
TEST	TEST Signal	I
NMI	Non-Maskable Interrupt	I
RESET	Reset Signal	I/O
JTAG-SEL0	JTAG Mode Select 0	I
JTAG-SEL1	JTAG Mode Select 1	I
PLL&Clock		
X32KFOUT	32KHz Clock Fanout	AOD
X32KIN	Clock Input Of 32KHz Crystal	AI
X32KOUT	Clock Output Of 32KHz Crystal	AO
VCC-RTC	RTC Power Supply	P
RTC-VIO	Internal LDO Output Bypass	AO
X24MFOUT	24MHz Clock Fanout	AOD
X24MIN	Clock Input Of 24MHz Crystal	AI
X24MOUT	Clock Output Of 24MHz Crystal	AO
PLLTEST	PLL Test	AOD
VCC-PLL	PLL Power Supply	P
HDMI		
HTX0P	HDMI Positive TMDS Differential Line Driver Data0 Output	AO
HTX0N	HDMI Negative TMDS Differential Line Driver Data0 Output	AO
HTX1P	HDMI Positive TMDS Differential Line Driver Data1 Output	AO
HTX1N	HDMI Negative TMDS Differential Line Driver Data1 Output	AO
HTX2P	HDMI Positive TMDS Differential Line Driver Data2 Output	AO
HTX2N	HDMI Negative TMDS Differential Line Driver Data2 Output	AO
HTXCP	HDMI Positive TMDS Differential Line Driver Clock Output	AO
HTXCN	HDMI Negative TMDS Differential Line Driver Clock Output	AO
HHPD	HDMI Hot Plug Detection Signal	I/O
HCEC	HDMI Consumer Electronics Control	I/O
HSCL	HDMI Serial Clock	O
HSDA	HDMI Serial Data	I/O
HVCC	HDMI Power Supply	P
USB		
USB-DM0	USB DM Signal	A I/O
USB-DP0	USB DP Signal	A I/O
USB-DM1	USBDM Signal	A I/O
USB-DP1	USB DP Signal	A I/O
USB-DM2	USB DM Signal	A I/O
USB-DP2	USB DP Signal	A I/O
USB-DM3	USB DM Signal	A I/O
USB-DP3	USB DP Signal	A I/O
VCC-USB	USB Power Supply	P

Signal Name[1]	Description[2]	Type[3]
ADC		
KEYADC	ADC Input for KEY Application	AI
EPHY		
EPHY-RXP	Transceiver Positive Output/Input	A I/O
EPHY-RXN	Transceiver Negative Output/Input	A I/O
EPHY-TXP	Transceiver Positive Output/Input	A I/O
EPHY-TXN	Transceiver Negative Output/Input	A I/O
EPHY-RTX	EPHY External Resistance to Ground	AI
EPHY-LINK-LED	EPHY LINK Up/Down Indicator LED	O
EPHY-SPD-LED	EPHY 10M/100M Indicator LED	O
EPHY-VDD	3.3V Analog Power Supply for EPHY	P
EPHY-VCC	1.1V Analog Power Supply for EPHY	P
TV		
TV-OUT	TV Output	AO
V33-TV	TV Out Power Supply	P
Audio Codec		
LINEINL	LINE-IN Left Channel Input	AI
LINEINR	LINE-IN Right Channel Input	AI
LINEOUTL	LINE-OUT Left Channel Output	AO
LINEOUTR	LINE-OUT Right Channel Output	AO
MBIAS	Master Analog Microphone Bias	AO
MICIN1N	Microphone Negative Input 1	AI
MICIN1P	Microphone Positive Input 1	AI
MICIN2N	Microphone Negative Input 2	AI
MICIN2P	Microphone Positive Input 2	AI
VRA1	Reference Voltage Output	AO
VRA2	Reference Voltage Output	AO
VRP	Reference Voltage Output	AO
AVCC	Analog Power	P
AGND	Analog GND	G
I2S/PCM		
PCM0_SYNC	PCM0 Sync/I2S0 Left and Right Channel Select Clock	I/O
PCM0_CLK	PCM0 Sample Rate Clock/I2S0 Bit Clock	I/O
PCM0_DOUT	I2S0/PCM0 Serial Data Output	O
PCM0_DIN	I2S0/PCM0 Serial Data Input	I
PCM0_MCLK	I2S0/PCM0 Master Clock	O
PCM1_SYNC	PCM1 Sync/I2S1 Left and Right Channel Select Clock	I/O
PCM1_CLK	PCM1 Sample Rate Clock/I2S1 Bit Clock	I/O
PCM1_DOUT	I2S1/PCM1 Serial Data Output	O
PCM1_DIN	I2S1/PCM1 Serial Data Input	I
OWA		
OWA_OUT	One Wire Audio Output	O

Signal Name[1]	Description[2]	Type[3]
SD/MMC		
SDC0_CMD	Command Signal for SD/TF Card	I/O
SDC0_CLK	Clock for SD/TF Card	O
SDC0_D[3:0]	Data Input and Output for SD/TF Card	I/O
SDC1_CMD	Command Signal for SDIO Wi-Fi	I/O
SDC1_CLK	Clock for SDIO Wi-Fi	O
SDC1_D[3:0]	Data Input and Output for SDIO Wi-Fi	I/O
SDC2_CMD	Command Signal for MMC	I/O
SDC2_CLK	Clock for MMC	O
SDC2_D[7:0]	Data Input and Output for MMC	I/O
SDC2_RST	Reset Signal for MMC	O
SDC2_DS	Data Strobe for MMC	I
NAND FLASH		
NAND_DQ[7:0]	NAND Flash0 Data Bit [7:0]	I/O
NAND_DQS	NADN Flash Data Strobe	I/O
NAND_WE	NAND Flash Write Enable	O
NAND_RE	NAND Flash chip Read Enable	O
NAND_ALE	NAND Flash Address Latch Enable	O
NAND_CLE	NAND Command Latch Enable	O
NAND_CE[1:0]	NAND Flash Chip Select [1:0]	O
NAND_RB[1:0]	NAND Flash Ready/Busy Bit	I
Interrupt		
PA_EINT[21:0]	GPIO A Interrupt	I
PF_EINT[6:0]	GPIO F Interrupt	I
PG_EINT[13:0]	GPIO G Interrupt	I
S_PL_EINT[11:0]	GPIO L Interrupt	I
PWM		
S_PWM	Pulse Width Modulation Output	O
PWM0	Pulse Width Modulation Output	O
IR		
S_CIR_RX	Consumer IR Data Receive	I
CSI		
CSI_PCLK	CSI Pixel Clock	I
CSI_MCLK	CSI Master Clock	O
CSI_HSYNC	CSI Horizontal SYNC	I
CSI_VSYNC	CSI Vertical SYNC	I
CSI_D[7:0]	CSI Data bit [7:0]	I
CSI_SCK	CSI Command Serial Clock Signal	I/O
CSI_SDA	CSI Command Serial Data Signal	I/O
EMAC		
RGMII_RXD3/MII_RXD3 /RMII_NULL	RGMII/MII Receive Data	I
RGMII_RXD2/MII_RXD2/ RMII_NULL	RGMII/MII Receive Data	I

Signal Name[1]	Description[2]	Type[3]
RGMII_RXD1/MII_RXD1/ RMII_RXD1	RGMII/MII /RMII Receive Data	I
RGMII_RXD0/MII_RXD0/ RMII_RXD0	RGMII/MII /RMII Receive Data	I
RGMII_RXCK/MII_RXCK/ RMII_NULL	RGMII/MII Receive Clock	I
RGMII_RXCTL/MII_RXDV/ RMII_CRS_DV	RGMII Receive Control/MII Receive Enable/RMII Carrier Sense-Receive Data Valid	I
RGMII_NULL/MII_RXERR/ RMII_RXER	MII/RMII Receive Error	I
RGMII_TXD3/MII_TXD3/ RMII_NULL	RGMII/MII Transmit Data	O
RGMII_TXD2/MII_TXD2/ RMII_NULL	RGMII/MII Transmit Data	O
RGMII_TXD1/MII_TXD1/ RMII_TXD1	RGMII/MII /RMII Transmit Data	O
RGMII_TXD0/MII_TXD0/ RMII_TXD0	RGMII/MII /RMII Transmit Data	O
RGMII_NULL/MII_CRS/ RMII_NULL	MII Carrier Sense	I
RGMII_TXCK/MII_TXCK/ RMII_TXCK	RGMII/MII /RMII Transmit Clock: Output Pin for RGMII, Input Pin for MII/RMII	I/O
RGMII_TXCTL/MII_TXEN/ RMII_TXEN	RGMII Transmit Control/MII Transmit Enable/RMII Transmit Enable: Output Pin for RGMII/RMII, Input Pin for MII	I/O
RGMII_NULL/MII_TXERR/ RMII_NULL	MII Transmit Error	O
RGMII_CLKIN/MII_COL/ RMII_NULL	RGMII Transmit Clock from External/MII Collision Detect	I
MDC	RGMII/MII /RMII Management Data Clock	O
MDIO	RGMII/MII /RMII Management Data Input/Output	I/O
Transport Stream Controller		
TS0_CLK	Transport Stream0 Clock	I
TS0_ERR	Transport Stream0 Error Indicate	I
TS0_SYNC	Transport Stream0 Sync	I
TS0_DVLD	Transport Stream0 Valid Signal	I
TS0_D[7:0]	Transport Stream0 Data	I
TS1_CLK	Transport Stream1 Clock	I
TS1_ERR	Transport Stream1 Error Indicate	I
TS1_SYNC	Transport Stream1 Sync	I
TS1_DVLD	Transport Stream1 Valid Signal	I
TS1_D0	Transport Stream1 Data	I
TS2_CLK	Transport Stream2 Clock	I
TS2_ERR	Transport Stream2 Error Indicate	I
TS2_SYNC	Transport Stream2 Sync	I
TS2_DVLD	Transport Stream2 Valid Signal	I
TS2_D[7:0]	Transport Stream2 Data	I
TS3_CLK	Transport Stream3 Clock	I
TS3_ERR	Transport Stream3 Error Indicate	I
TS3_SYNC	Transport Stream3 Sync	I
TS3_DVLD	Transport Stream3 Valid Signal	I
TS3_D0	Transport Stream3 Data	I

Signal Name[1]	Description[2]	Type[3]
SPI (x=[1:0])		
SPIx_CS	SPIx Chip Select signal, Low Active	I/O
SPIx_CLK	SPIx Clock Signal	I/O
SPIx_MOSI	SPIx Master Data Out, Slave Data In	I/O
SPIx_MISO	SPIx Master Data In, Slave Data Out	I/O
UART		
UART0_TX	UART0 Data Transmit	O
UART0_RX	UART0 Data Receive	I
UART1_TX	UART1 Data Transmit	O
UART1_RX	UART1 Data Receive	I
UART1_CTS	UART1 Data Clear To Send	I
UART1_RTS	UART1 Data Request To Send	O
UART2_TX	UART2 Data Transmit	O
UART2_RX	UART2 Data Receive	I
UART2_CTS	UART2 Data Clear To Send	I
UART2_RTS	UART2 Data Request To Send	O
UART3_TX	UART3 Data Transmit	O
UART3_RX	UART3 Data Receive	I
UART3_CTS	UART3 Data Clear To Send	I
UART3_RTS	UART3 Data Request To Send	O
S_UART_TX	UART Data Transmit	O
S_UART_RX	UART Data Receive	I
TWI (x=[2:0])		
TWIx_SCK	TWIx Serial Clock Signal	I/O
TWIx_SDA	TWIx Serial Data Signal	I/O
S_TWI_SCK	TWI Serial Clock Signal for CPUs	I/O
S_TWI_SDA	TWI Serial Data Signal for CPUs	I/O
Smart Card Reader(x=[1:0])		
SIMx_PWREN	Smart Card Power Enable	O
SIMx_CLK	Smart Card Clock	O
SIMx_DATA	Smart Card Data	I/O
SIMx_RST	Smart Card Reset	O
SIMx_DET	Smart Card Detect	I
SIMx_VPPEN	Smart Card Program Voltage Enable	O
SIMx_VPPPP	Smart Card Program Control	O
DI		
DI_TX	De-Interlacer Output	O
DI_RX	De-Interlacer Input	I
JTAG		
JTAG_MS	JTAG Mode Select Input	I
JTAG_CK	JTAG Clock Input	I
JTAG_DO	JTAG Data Output	O

Signal Name[1]	Description[2]	Type[3]
JTAG_DI	JTAG Data Input	I
S_JTAG_MS	JTAG Mode Select Input for CPUs	I
S_JTAG_CK	JTAG Clock Input for CPUs	I
S_JTAG_DO	JTAG Data Output for CPUs	O
S_JTAG_DI	JTAG Data Input for CPUs	I

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Table 5-1 specifies the absolute maximum ratings over the operating junction temperature range of commercial and extended temperature devices. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this standard may damage to the device.

Table 5-1. Absolute Maximum Ratings

Symbol	Parameter		MIN	Max	Unit
$I_{I/O}$	In/Out Current for Input and Output		-40	40	mA
T_{STG}	Storage Temperature		-40	125	℃
AVCC	Power Supply for Analog Part		-0.3	3.4	V
EPHY-VCC	Power Supply for EPHY		-0.3	3.8	V
EPHY-VDD	Power Supply for EPHY		-0.3	1.4	V
HVCC	Power Supply for HDMI		-0.3	3.6	V
V33-TV	Power Supply for TV		-0.3	3.6	V
VCC-IO	Power Supply for 3.3V Digital Part		-0.3	3.6	V
VCC-PC	Power Supply for Port C		-0.3	3.6	V
VCC-PD	Power Supply for Port D		-0.3	3.6	V
VCC-PG	Power Supply for Port G		-0.3	3.6	V
VCC-PLL	Power Supply for System PLL		-0.3	3.6	V
VCC-RTC	Power Supply for RTC		-0.3	3.6	V
VCC-USB	Power Supply for USB		-0.3	3.6	V
VCC-DRAM	Power Supply for DDR3/DDR3L		-0.3	1.65	V
VDD-CPUS	Power Supply for CPUS		-0.3	TBD	V
VDD-CPUX	Power Supply for CPU		-0.3	TBD	V
VDD-EFUSE	Power Supply for EFUSE		-0.3	3.6	V
VDD-SYS	Power Supply for System		-0.3	1.4	V
V_{ESD}	Electrostatic Discharge	Human Body Model(HBM)[1]	-4000	4000	V
		Charged Device Model(CDM)[2]	-250	250	V
$I_{Latch-up}$	Latch-up I-test performance current-pulse injection on each IO pin[3]		Pass		
	Latch-up over-voltage performance voltage injection on each IO pin[4]		Pass		

(1). Test method: JEDEC JS-001-2012(Class-3A). JEDEC publication JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2). Test method: JESD22-C101F(Class-C1). JEDEC publication JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

(3). Current test performance: Pins stressed per JEDEC JESD78D(Class I, Level A) and passed with I/O pin injection current as defined in JEDEC.

(4). Over voltage performance: Supplies stressed per JEDEC JESD78D(Class I, Level A) and passed voltage injection as defined in JEDEC.

5.2. Recommended Operating Conditions

All H5 modules are used under the operating conditions contained in Table 5-2.

Table 5-2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature	-20	-	+70	°C
Tj	Junction Temperature Range	TBD	-	TBD	°C
AVCC	Power Supply for Analog Part	-	3.3	-	V
EPHY-VCC	3.3V Power Supply for EPHY	3.0	3.3	3.6	V
EPHY-VDD	1.1V Power Supply for EPHY	1.0	1.1	1.2	V
HVCC	Power Supply for HDMI	3.24	3.3	3.36	V
V33-TV	Power Supply for TV	3.24	3.3	3.36	V
VCC-IO	Power Supply for 3.3V Digital Part	3.0	3.3	3.6	V
VCC-PC	Power Supply for Port C	1.7	1.8~3.3	3.6	V
VCC-PD	Power Supply for Port D	2.25	2.5~3.3	3.6	V
VCC-PG	Power Supply for Port G	1.7	1.8~3.3	3.6	V
VCC-PLL	Power Supply for System PLL	3.0	-	3.3	V
VCC-RTC	Power Supply for RTC	3.0	-	3.3	V
VCC-USB	Power Supply for USB	3.0	3.3	3.6	V
VCC-DRAM	Power Supply for DDR3 IO Domain	1.425	1.5	1.575	V
	Power Supply for DDR3L IO Domain	1.283	1.35	1.575	V
VDD-CPUS	Power Supply for CPUS	TBD			V
VDD-CPUX	Power Supply for CPU	TBD			V
VDD-EFUSE	Power Supply for EFUSE	-	3.3	-	V
VDD-SYS	Power Supply for System	1.1	1.2	1.3	V

5.3. DC Electrical Characteristics

Table 5-3 summarizes the DC electrical characteristics of H5.

Table 5-3. DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage	0.7 * VCC-IO	-	VCC-IO + 0.3	V
V_{IL}	Low-Level Input Voltage	-0.3	-	0.3 * VCC-IO	V
R_{PU}	Input pull-up resistance	50	100	150	KΩ

R_{PD}	Input pull-down resistance	50	100	150	KΩ
I_{IH}	High-Level Input Current	-	-	10	uA
I_{IL}	Low-Level Input Current	-	-	10	uA
V_{OH}	High-Level Output Voltage	VCC-IO - 0.2	-	VCC-IO	V
V_{OL}	Low-Level Output Voltage	0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current	-10	-	10	uA
C_{IN}	Input Capacitance	-	-	5	pF
C_{OUT}	Output Capacitance	-	-	5	pF

5.4. ADC Electrical Characteristics

KEYADC is an analog-to-digital(ADC) converter for key application. Table 5-4 lists KEYADC electrical characteristics.

Table 5-4. KEYADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	6	-	bits
Full-scale Input Range	0	-	0.667*AVCC	V
Quantizing Error	-	1	-	LSB
Clock Frequency	-	-	250	Hz
Conversion Time	-	14	-	ADC Clock Cycles

5.5. Oscillator Electrical Characteristics

H5 contains two external input clocks:X24MIN and X32KIN, two output clocks:X24MOUT and X32KOUT.The 24.000MHz frequency is used to generate the main source clock for PLL and the main digital blocks, the clock is provided through X24MIN.Table 5-5 lists the 24MHz crystal specifications.

Table 5-5. 24MHz Crystal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	-	24.000	-	MHz
t_{ST}	Startup Time	-	-	-	ms
	Frequency Tolerance at 25 °C	-50	-	+50	ppm
	Oscillation Mode	Fundamental			-
	Maximum Change Over Temperature Range	-50	-	+50	ppm
P_{ON}	Drive Level	-	-	300	uW
C_L	Equivalent Load Capacitance	12	18	22	pF
R_S	Series Resistance(ESR)	-	25	-	Ω
	Duty Cycle	30	50	70	%
C_M	Motional Capacitance	-	-	-	pF

C_{SHUT}	Shunt Capacitance	5	6.5	7.5	pF
R_{BIAS}	Internal Bias Resistor	0.5	0.6	0.7	MΩ

The 32768Hz frequency is used for low frequency operation. It supplies the wake-up domain for operation in lowest power mode. The clock is provided through X32KIN. Table 5-6 lists the 32768Hz crystal specifications.

Table 5-6. 32768Hz Crystal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	-	32768	-	Hz
t_{ST}	Startup Time	-	-	–	ms
	Frequency Tolerance at 25 °C	-20	-	+20	ppm
	Oscillation Mode	Fundamental			-
	Maximum Change Over Temperature Range	-20	-	+20	ppm
P_{ON}	Drive Level	-	-	1.0	uW
C_L	Equivalent Load Capacitance	-	12.5	-	pF
R_S	Series Resistance(ESR)	-	-	35	KΩ
	Duty Cycle	30	50	70	%
C_M	Motional Capacitance	-	2	-	fF
C_{SHUT}	Shunt Capacitance	-	1.1	-	pF

5.6. Maximum Current Consumption

Table 5-7 lists the peak power consumption of H5.

Table 5-7. Maximum Current Consumption

Parameter	Sub Parameter	Power Supply	Condition	Min	Typ	Max	Unit
Internal Core Power	CPU	VDD-CPUX	@1.1V	-	-	TBD	mA
	SYS	VDD-SYS	@1.2V	-	-	TBD	mA
GPIO Power		VCC-IO, VCC-PC, VCC-PD, VCC-PG	@3.3V @2.5V @1.8V	-	-	TBD	mA
Memory I/O Power		VCC-DRAM	@1.5V	-	-	TBD	mA
Oscillator		VCC-PLL	@3.3V	-	-	TBD	mA
USB 3.0V Power of PHY		VCC-USB	@3.3V	-	-	TBD	mA
HDMI		HVCC	@3.3V	-	-	TBD	mA
RTC Power		VCC-RTC	@3.3V	-	-	TBD	mA
ADC Analog Power		AVCC	@3.3V	-	-	TBD	mA
DAC Analog Power		AVCC	@3.3V	-	-	TBD	mA
PLL Power		VCC-PLL	@3.3V	-	-	TBD	mA

5.7. External Memory AC Electrical Characteristics

5.7.1. Nand Flash AC Electrical Characteristics

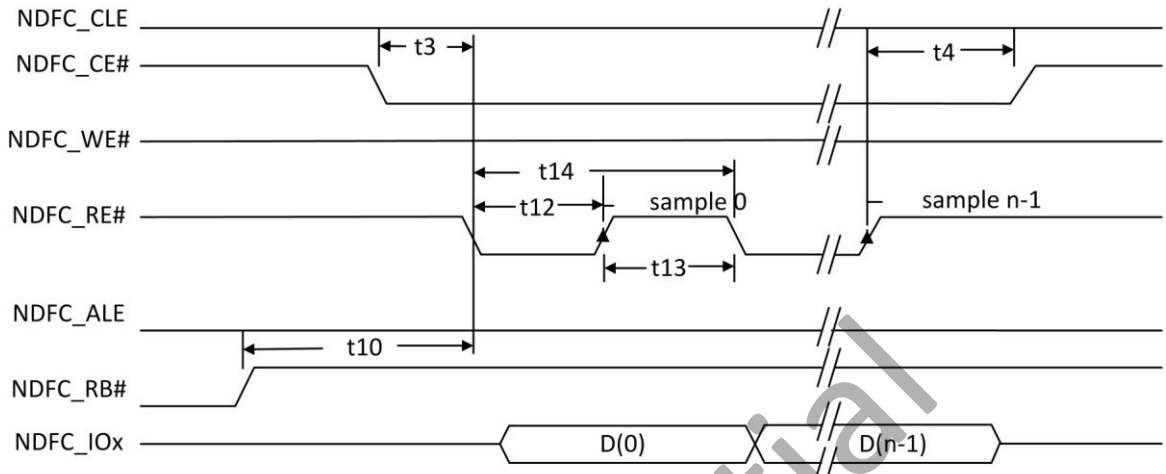


Figure 5-1. Conventional Serial Access Cycle Timing (SAM0)

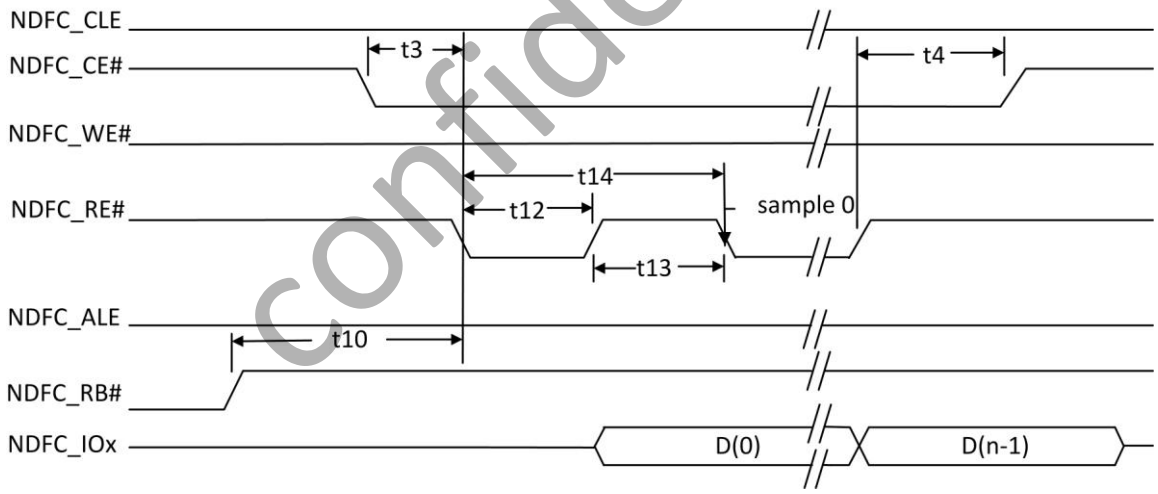


Figure 5-2. EDO Type Serial Access after Read Cycle Timing (SAM1)

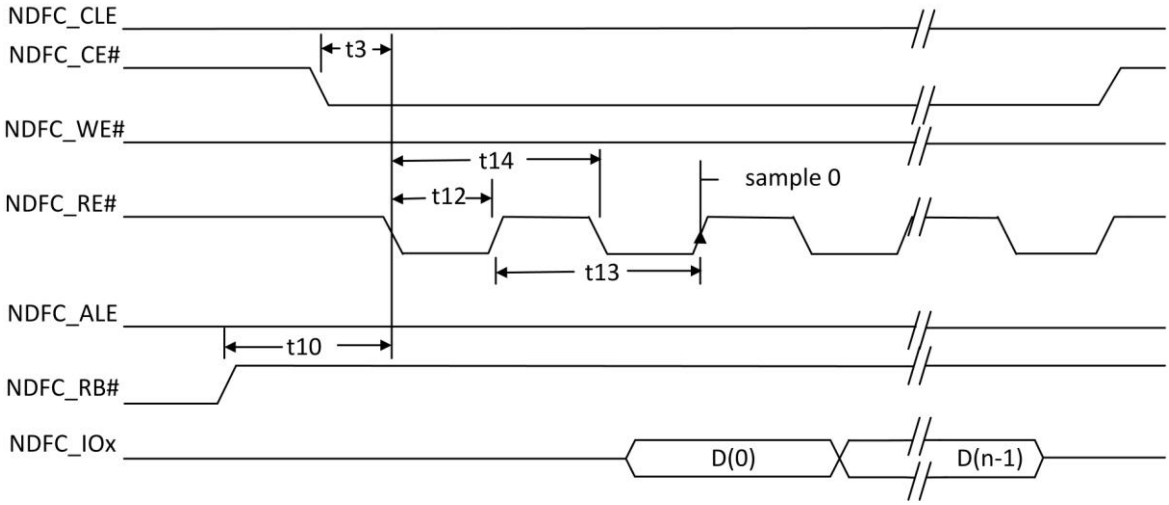


Figure 5-3. Extending EDO Type Serial Access Mode Timing (SAM2)

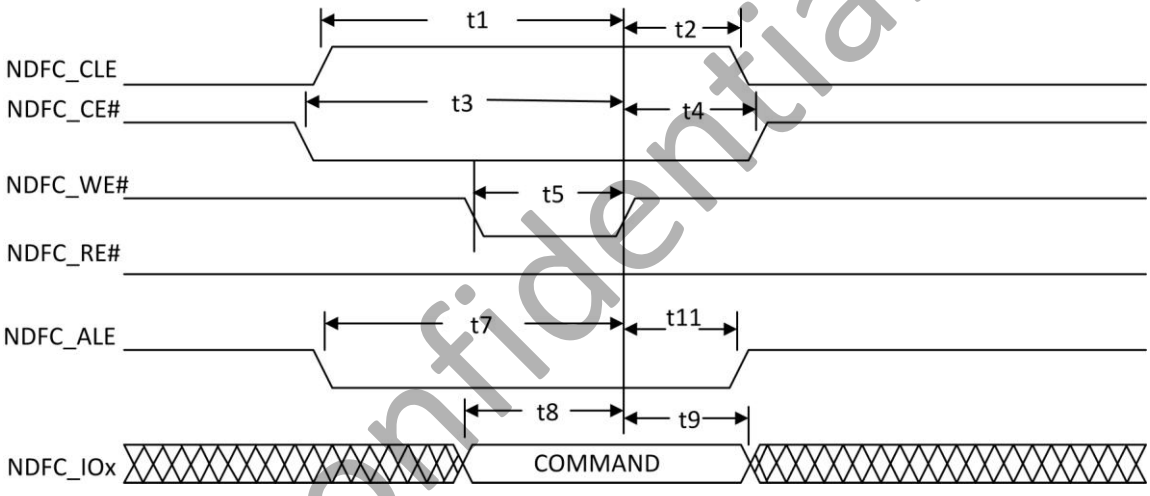


Figure 5-4. Command Latch Cycle Timing

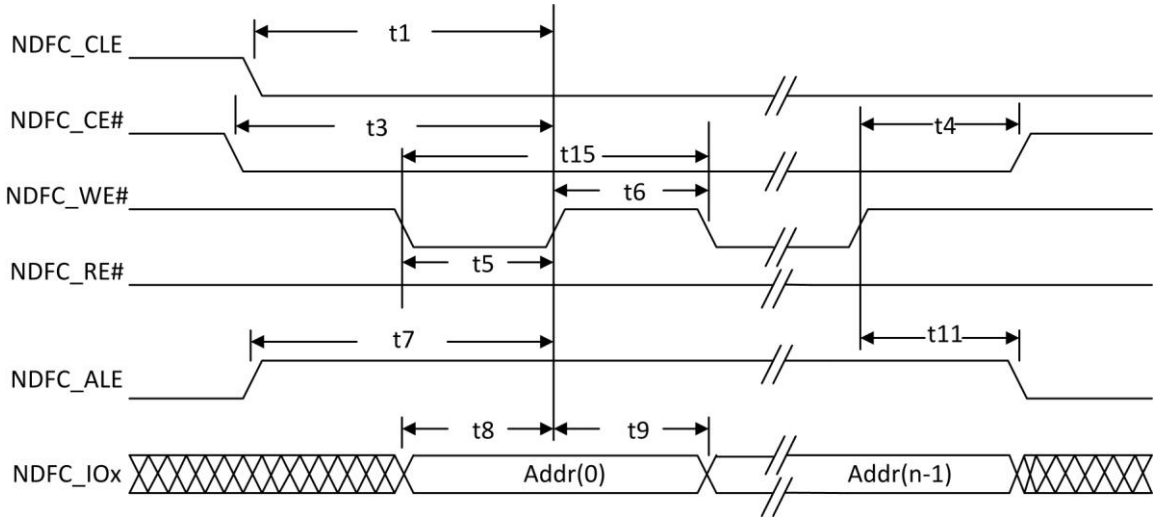


Figure 5-5. Address Latch Cycle Timing

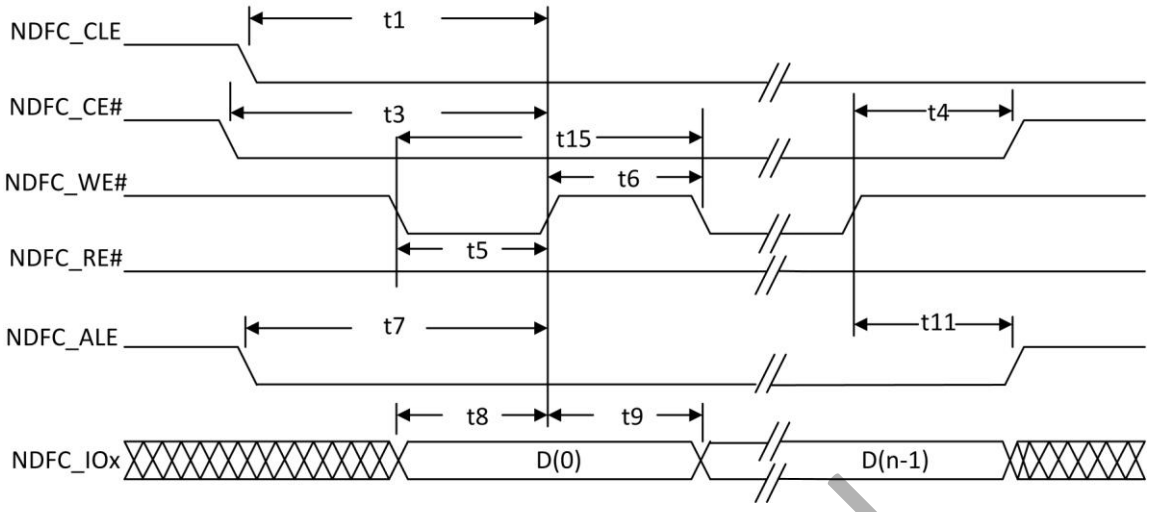


Figure 5-6. Write Data to Flash Cycle Timing

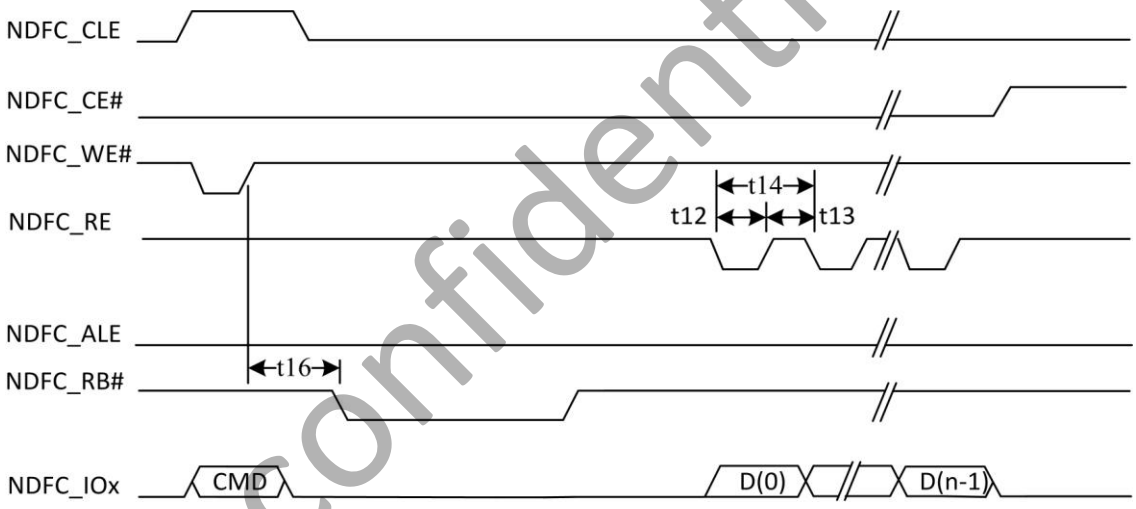


Figure 5-7. Waiting R/B# Ready Timing

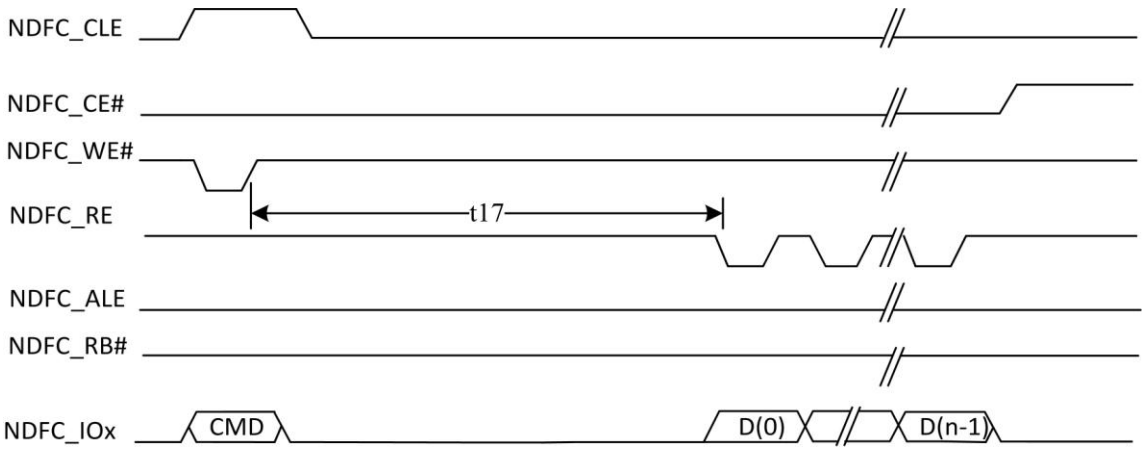


Figure 5-8. WE# High to RE# Low Timing

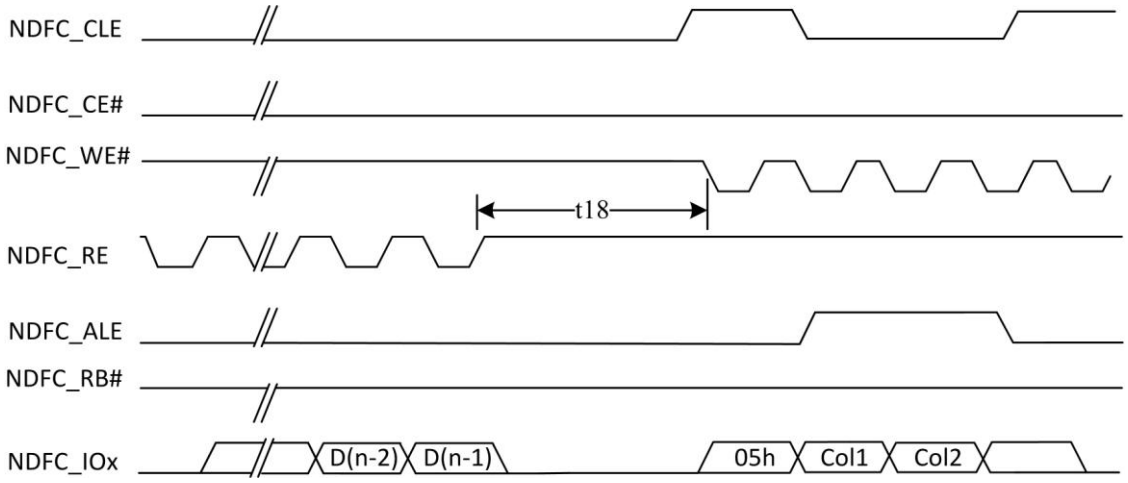


Figure 5-9. RE# High to WE# Low Timing

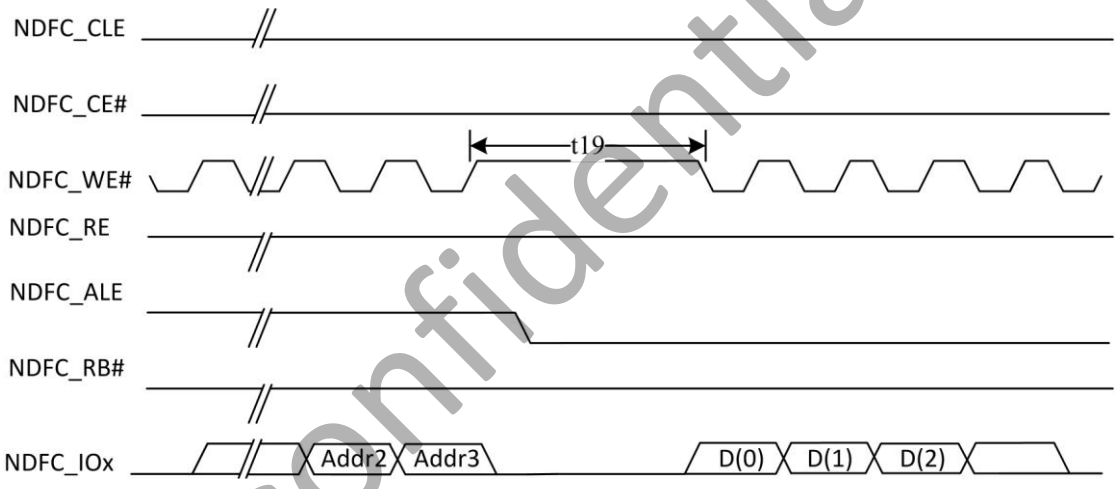


Figure 5-10. Address to Data Loading Timing

Table 5-8. NAND Timing Constants

Parameter	Symbol	Timing	Unit
NDFC_CLE setup time	t1	2T	ns
NDFC_CLE hold time	t2	2T(1)	ns
NDFC_CE setup time	t3	2T	ns
NDFC_CE hold time	t4	2T	ns
NDFC_WE# pulse width	t5	T	ns
NDFC_WE# hold time	t6	T	ns
NDFC_ALE setup time	t7	2T	ns
Data setup time	t8	T	ns
Data hold time	t9	T	ns
Ready to NDFC_RE# low	t10	3T	ns
NDFC_ALE hold time	t11	2T	ns

NDFC_RE# pulse width	t12	T	ns
NDFC_RE# hold time	t13	T	ns
Read cycle time	t14	2T	ns
Write cycle time	t15	2T	ns
NDFC_WE# high to R/B# busy	t16	T_WB(2)	ns
NDFC_WE# high to NDFC_RE# low	t17	T_WHR(3)	ns
NDFC_RE# high to NDFC_WE# low	t18	T_RHW(4)	ns
Address to Data Loading time	t19	T_ADL(5)	ns
NOTE (1):T is the cycle of clock. **NOTE (2),(3),(4),(5):**This values is configurable in Nand flash controller. The value of T_WB could be 28T/44T/60T/76T, the value of T_WHR could be 0T/12T/28T/44T, the value of T_RHW could be 8T/24T/40T/56T, the value of T_ADL could be 0T/12T/28T/44T.			

5.7.2. SMHC AC Electrical Characteristics

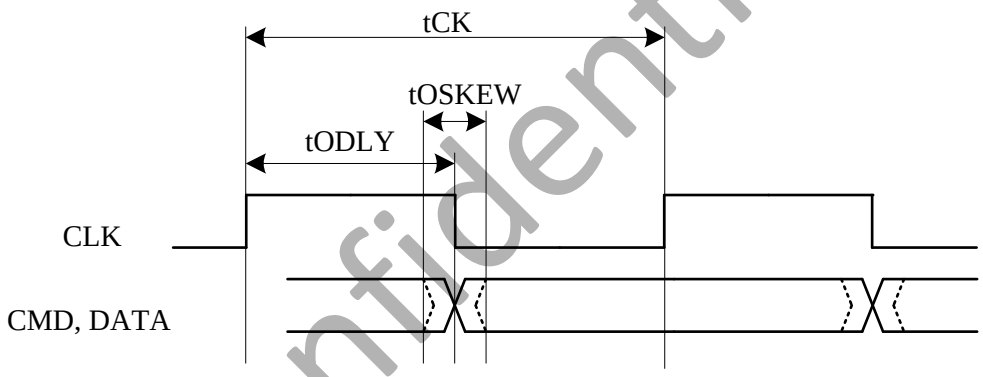


Figure 5-11. SMHC in SDR Mode Output Timing

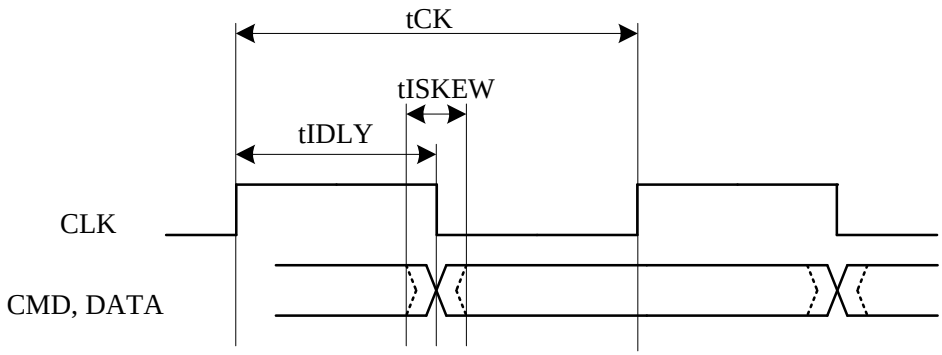


Figure 5-12. SMHC in SDR Mode Input Timing

Table 5-9. SMHC Timing Constants

Parameter	Symbol	Min	Type	Max	Unit

Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
CMD, Data output delay time	tODLY	-	-	12	ns
Data output delay skew time	tOSKEW	-	-	0.5	ns
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay.	tIDLY	-	-	21	ns
Data input skew time in SDR mode	tISKEW	-	-	0.8	ns
Note (1): Output CMD, DATA is referenced to CLK.					

5.8. External Peripheral AC Electrical Characteristics

5.8.1. LCD AC Electrical Characteristics

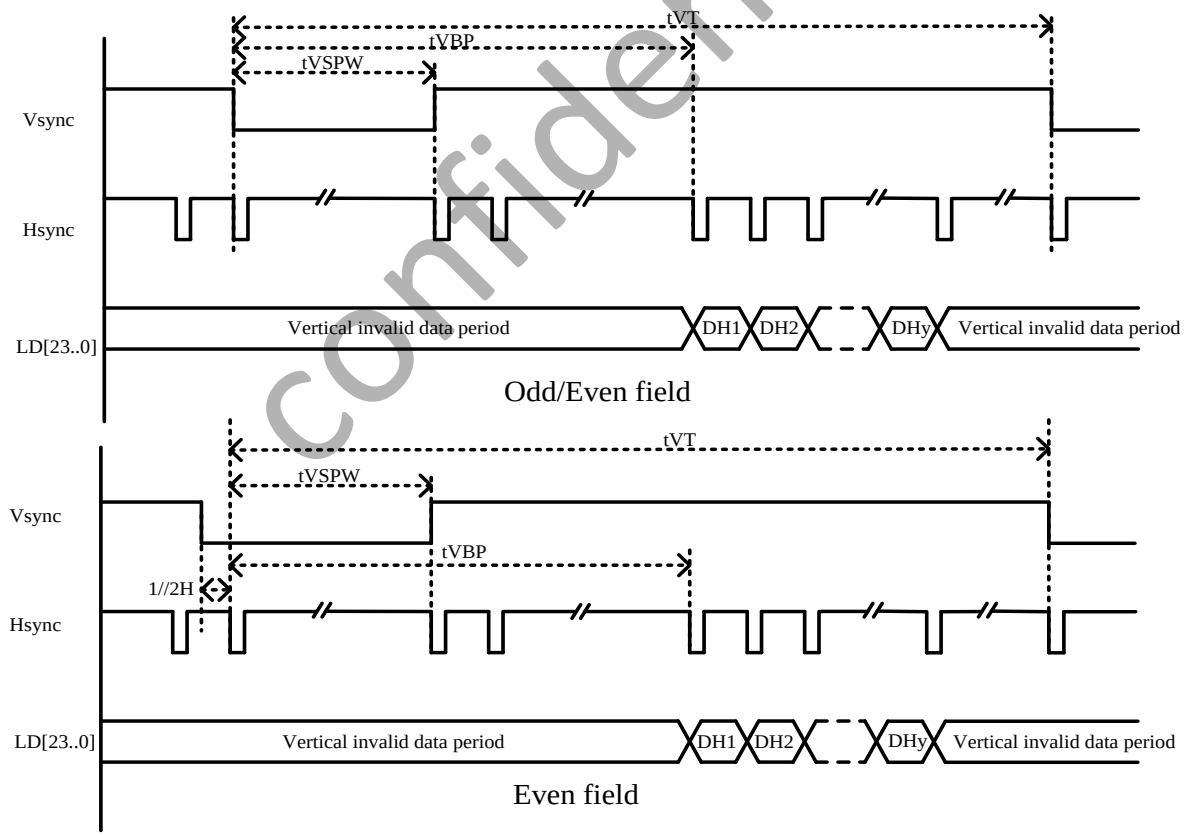


Figure 5-13. HV_IF Interface Vertical Timing

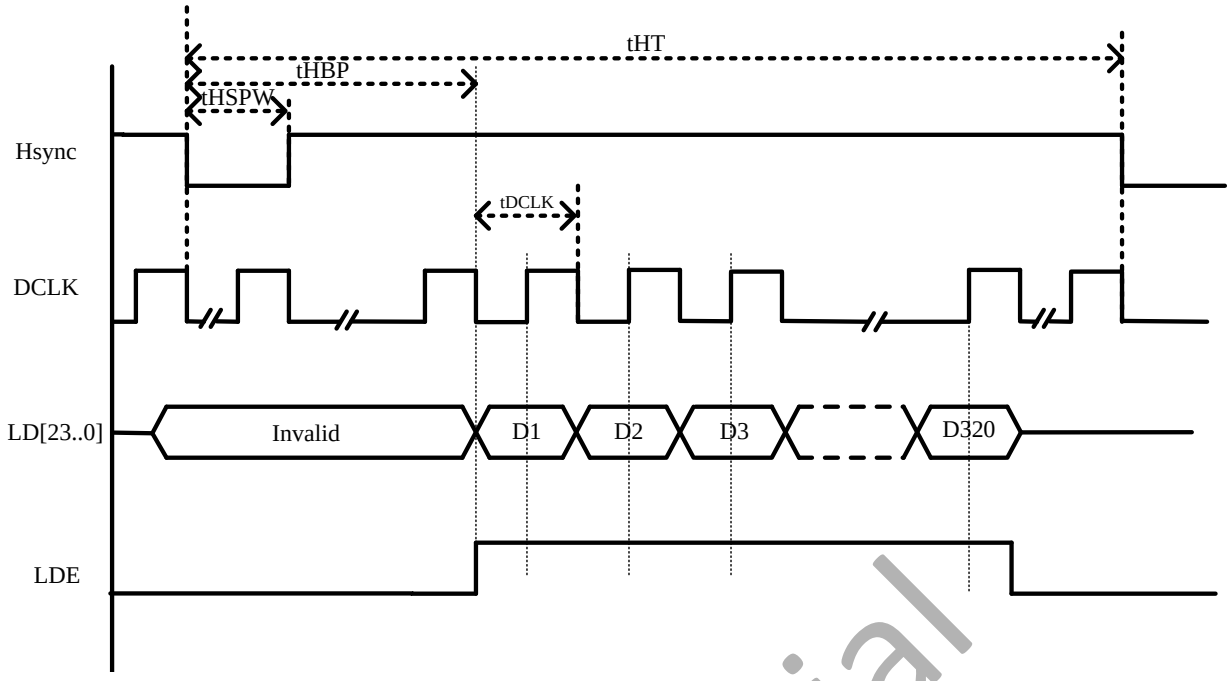


Figure 5-14. HV_IF Interface Parallel Mode Horizontal Timing

Table 5-10. LCD HV_IF Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DCLK cycle time	tDCLK	5	-	-	ns
HSYNC period time	tHT	-	HT+1	-	tDCLK
HSYNC width	tHSPW	-	HSPW+1	-	tDCLK
HSYNC back porch	tHBP	-	HBP+1	-	tDCLK
VSYNC period time	tVT	-	VT/2	-	tHT
VSYNC width	tVSPW	-	VSPW+1	-	tHT
VSYNC back porch	tVBP	-	VBP+1	-	tHT

Note:
(1). Vsync: Vertical sync, indicates one new frame
(2). Hsync: Horizontal sync, indicate one new scan line
(3). DCLK: Dot clock, pixel data are sync by this clock
(4). LDE: LCD data enable
(5). LD[23..0]: 24Bit RGB/YUV output from input FIFO for panel

5.8.2. CSI AC Electrical Characteristics

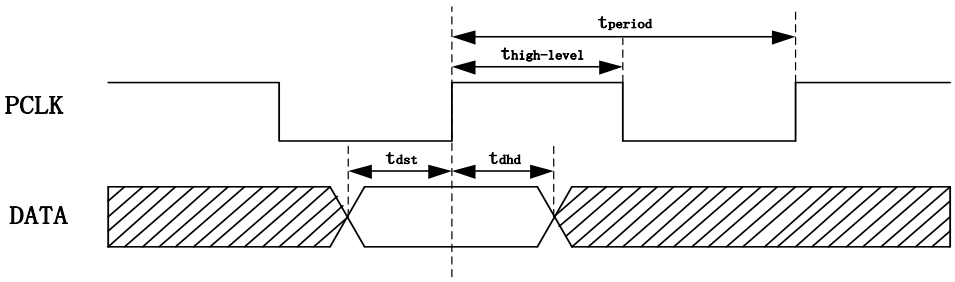


Figure 5-15. Data Sample Timing

Table 5-11. CSI Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Pclk period	t_{period}	5.95	-	-	ns
Pclk frequency	$1/t_{period}$	-	-	168	MHz
Pclk duty	$t_{high-level}/t_{period}$	40	50	60	%
Data input setup time	t_{dst}	0.6	-	-	ns
Data input hold time	t_{dhd}	0.6	-	-	ns

5.8.3. EMAC AC Electrical Characteristics

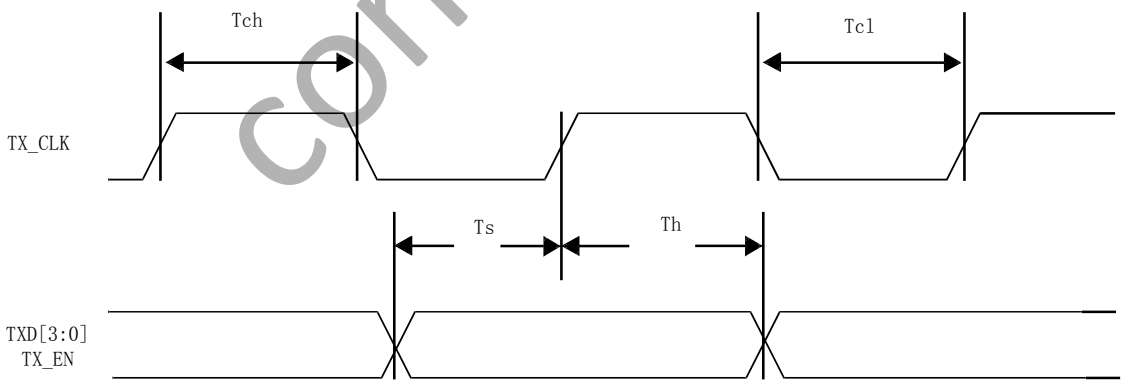


Figure 5-16. MII Interface Transmit Timing

Table 5-12. 100Mb/s MII Transmit Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
Transmit clock high time,100M mode	Tch	-	20	-	ns
Transmit clock low time,100M mode	Tcl	-	20	-	ns
TXEN/TXD setup time to TX_CLK	Ts	10	-	-	ns
TXEN/TXD hold time to TX_CLK	Th	0	-	-	ns

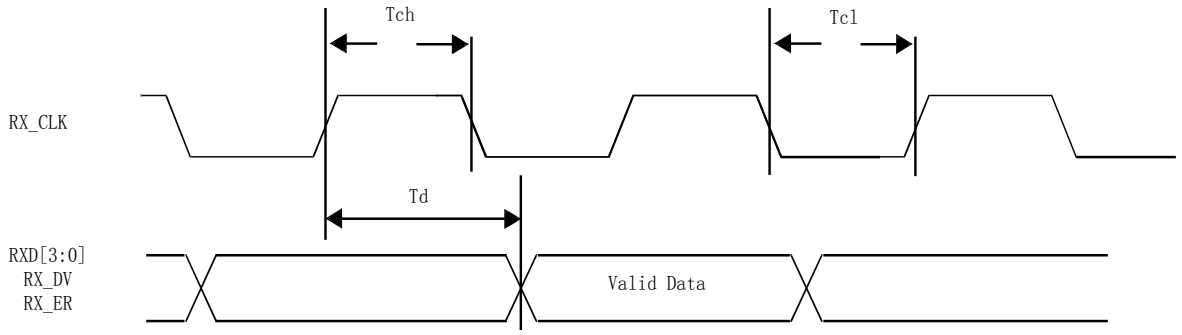


Figure 5-17. MII Interface Receive Timing

Table 5-13. 100Mb/s MII Receive Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
Receive clock high time,100M mode	Tch	-	20	-	ns
Receive clock low time,100M mode	Tcl	-	20	-	ns
RX_CLK to RXD[3:0]/RX_DV/RX_ER Delay	Td	10	-	30	ns

5.8.4. CIR Receiver AC Electrical Characteristics

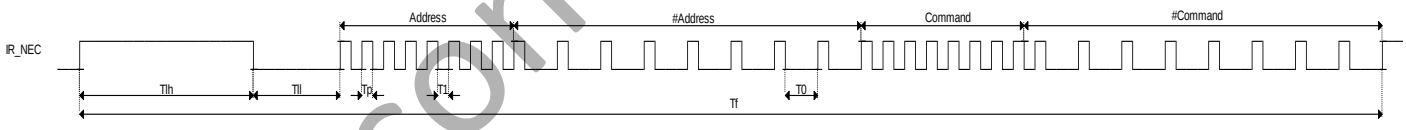


Figure 5-18. CIR Receiver Timing

Table 5-14. CIR Receiver Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
Frame period	Tf	-	67.5	-	ms
Lead code high time	Tlh	-	9	-	ms
Lead code low time	Tll	-	4.5	-	ms
Pulse time	Tp	-	560	-	us
Logical 1 low time	T1	-	1680	-	us
Logical 0 low time	T0	-	560	-	us

5.8.5. SPI AC Electrical Characteristics

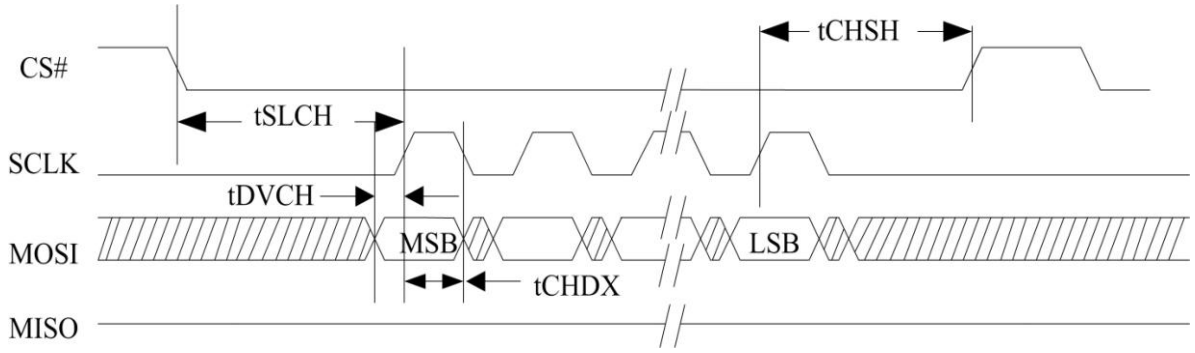


Figure 5-19. SPI MOSI Timing

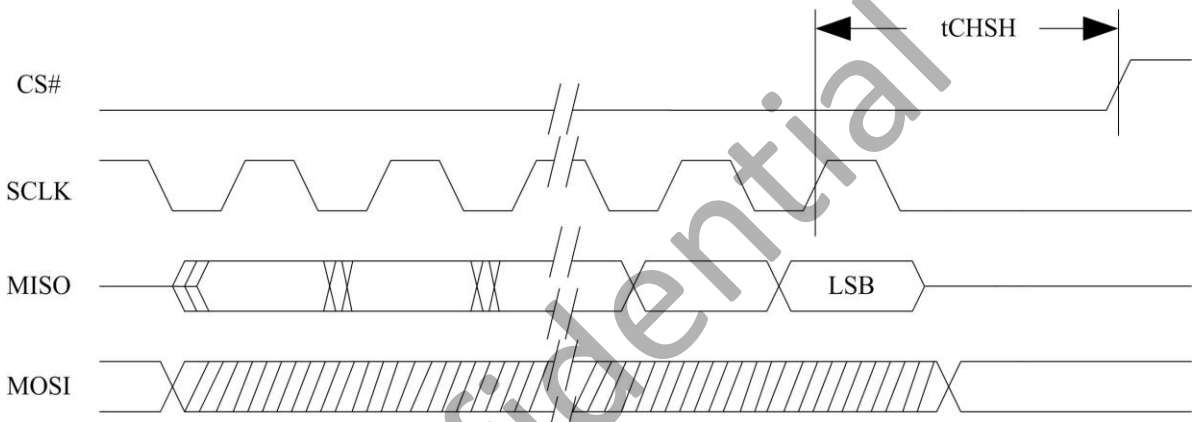


Figure 5-20. SPI MISO Timing

Table 5-15. SPI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CS# active setup time	tSLCH	-	2T	-	ns
CS# active hold time	tCHSH	-	2T(1)	-	ns
Data in setup time	tDVCH	-	T/2-3	-	ns
Data in hold time	tCHDX	-	T/2-3	-	ns
Note (1):T is the cycle of clock.					

5.8.6. UART AC Electrical Characteristics

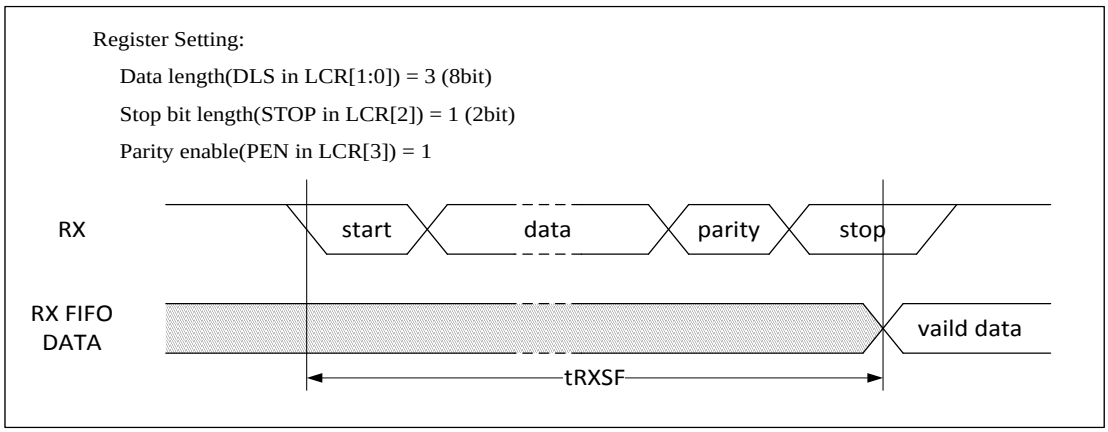


Figure 5-21. UART RX Timing

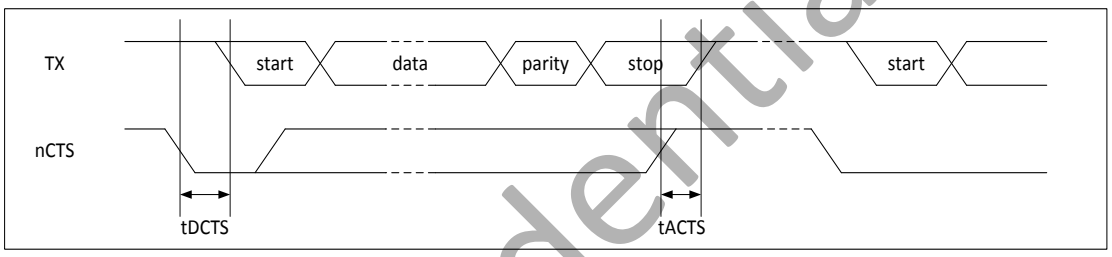


Figure 5-22. UART nCTS Timing

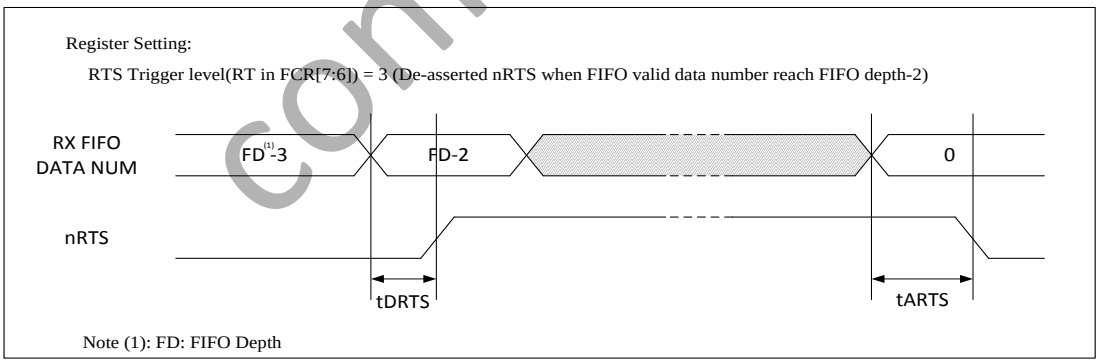


Figure 5-23. UART nRTS Timing

Table 5-16. UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	10.5× BRP(1)	-	11× BRP(1)	ns
Delay time of de-asserted nCTS to TX start	tDCTS	-	-	BRP(1)	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP(1)/4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP(1)	ns

Delay time of asserted nRTS	tARTS	-	-	BRP(1)	ns
Note (1): BRP(Baud-Rate Period).					

5.8.7. TWI AC Electrical Characteristics

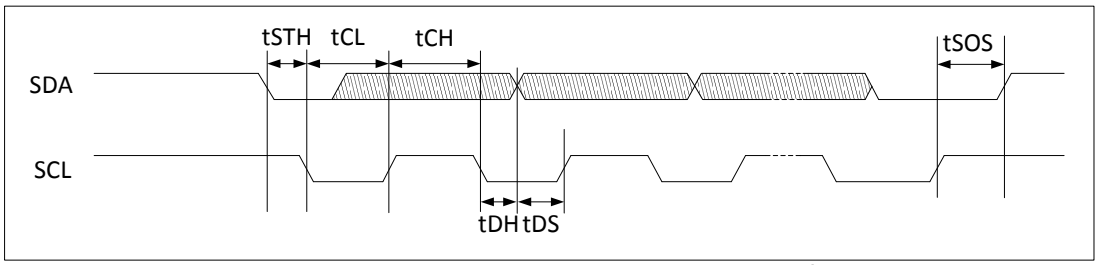


Figure 5-24. TWI Timing

Table 5-17. TWI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
High period of SCL	tCH	0.96	-	-	μs
Low period of SCL	tCL	1.5	-	-	μs
SCL hold time for START condition	tSTH	1.5	-	-	μs
SCL step time for STOP condition	tSOS	1.6	-	-	μs
SDA hold time	tDH	0.82	-	-	μs
SDA step time	tDS	0.72	-	-	μs

5.8.8. TSC AC Electrical Characteristics

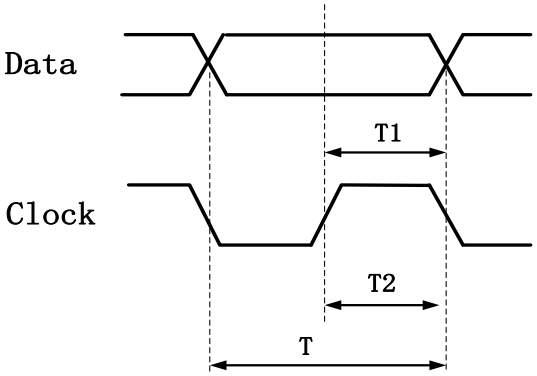


Figure 5-25. TSC Data and Clock Timing

Table 5-18. TSC Timing Constants

Parameter	Symbol	Min	Type	Max	Unit

Data hold time	T1	T/2-T/10	T[(1)]/2	T/2+T/10	us
Clock pulse width	T2	T/2-T/10	T/2	T/2+T/10	us
Note (1):T is the cycle of clock.					

5.8.9. SCR AC Electrical Characteristics

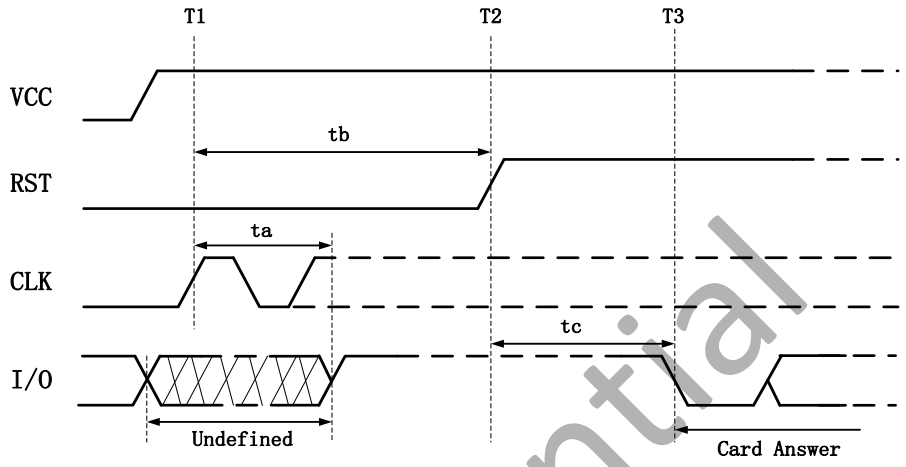


Figure 5-26. SCR Activation and Cold Reset Timing

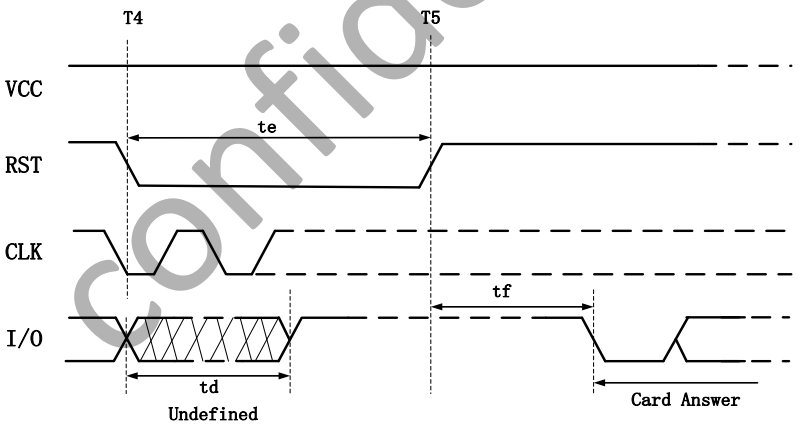


Figure 5-27. SCR Warm Reset Timing

Table 5-19. SCR Timing Constants

Symbol	Min	Type	Max	Unit
ta	-	-	200/f	us
tb	400/f	-	-	us
tc	400/f	-	40000/f	us
td	-	-	200/f	us
te	400/f	-	-	us
tf	400/f	-	40000/f	us

Note:
(1). Activation: Before time T1
(2). Cold Reset: After time T1
(3). T1: The clock signal is applied to CLK at time T1.
(4). T2: The RST is put to state H.
(5). T3: The card begin answer at time T3
(6). ta: The card shall set I/O to state H within 200 clock cycles (delay ta) after the clock signal is applied to CLK (at time T1+ta).
(7). tb: The cold reset results from maintaining RST at state L for at least 400 clock cycles (delay tb) after the clock signal is applied to CLK (at time T1+tb).
(8). tc: The answer on I/O shall begin between 400 and 40000 clock cycles (delay tc) after the rising edge of the signal on RST (at time T2+tc).
(9). td: The card shall set I/O to state H within 200 clock cycles (delay td) after state L is applied to RST (at time T4+td).
(10). te: The controller initiates a warm reset (at time T4) by putting RST to state L for at least 400 clock cycles (delay te) while VCC remains powered and CLK provided with a suitable and stabled clock signal.
(11). tf: The card answer on I/O shall begin between 400 and 40000 clock cycles (delay tf) after the rising edge of the signal on RST (at time T5+tf).
(12). f is the frequency of clock.

5.9. Power-up and Power-down Sequence

The following figure shows an example of the power-up sequence for H5 device. During the entire power-up sequence, the RESET pin must be held on low until all power domains are stable. The other power domains not in Figure 5-28 can be turned on upon the software request.

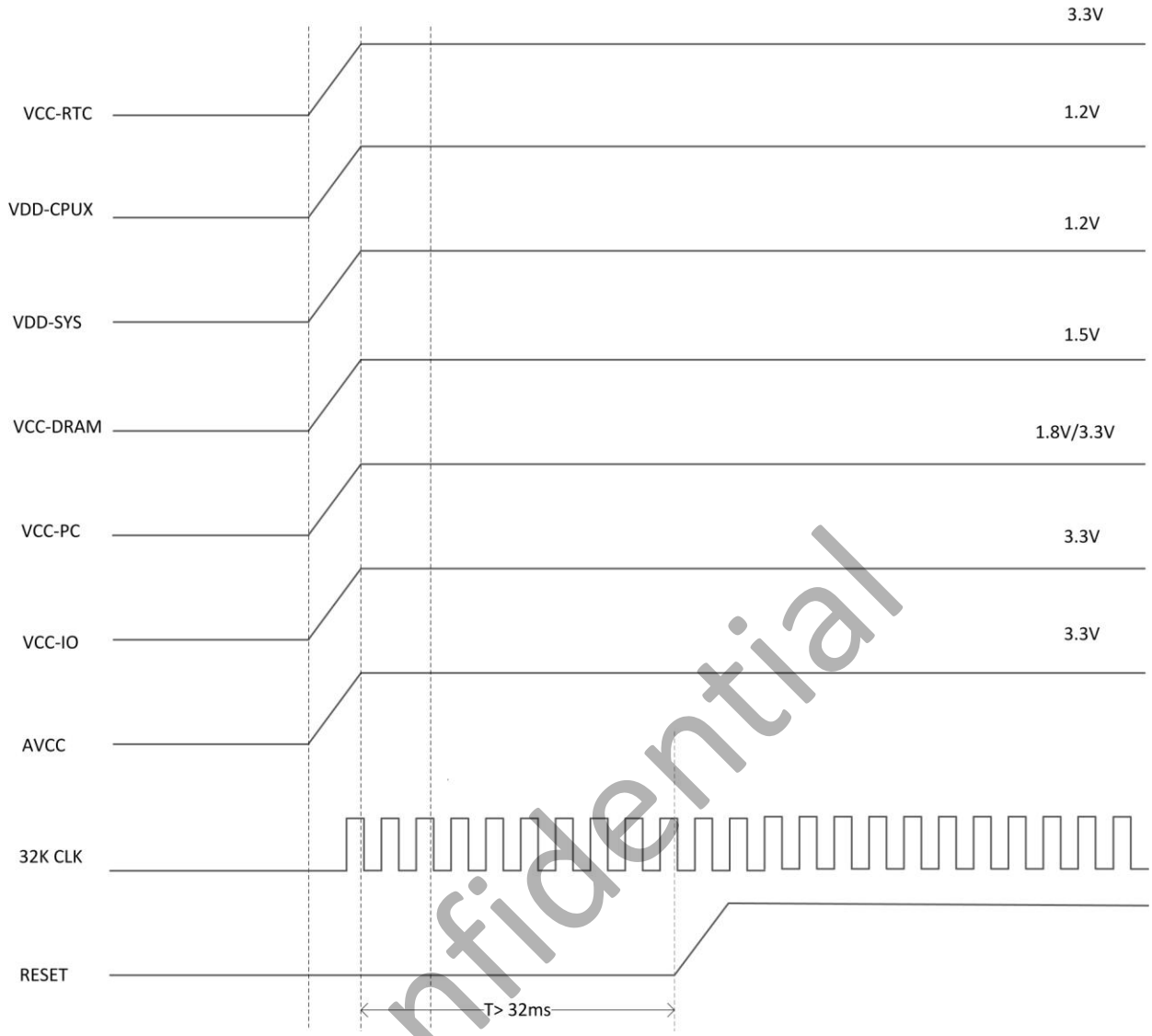


Figure 5-28. Power On Sequence

Power-down sequence is not special restrictions for H5.

5.10. Package Thermal Characteristics

For reliability and operability concerns, the absolute maximum junction temperature of H5 has to be below 125°C.The testing PCB is based on 4 layers. The following thermal resistance characteristics in Table 5-20 is based on JEDEC JESD51 standard, because the system design and temperature could be different with JEDEC JESD51 , the simulating result data is a reference only, please prevail in the actual application condition test.

Table 5-20. H5 Thermal Resistance Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature	-20	-	+70	°C
T_J	Junction Temperature	-	-	+125	°C

θ_{JA}	Junction-to-Ambient Thermal Resistance	-	27.9	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	TBD	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	TBD	-	°C/W
ψ_{JT}	Junction-to-Top Characterization Parameter	-	TBD	-	°C/W
ψ_{JB}	Junction-to-Board Characterization Parameter	-	TBD	-	°C/W

(1). These values are based on a JEDEC-defined 2S2P system and will change based on environment as well as application.

(2). °C/W : degrees Celsius per watt.

Appendix

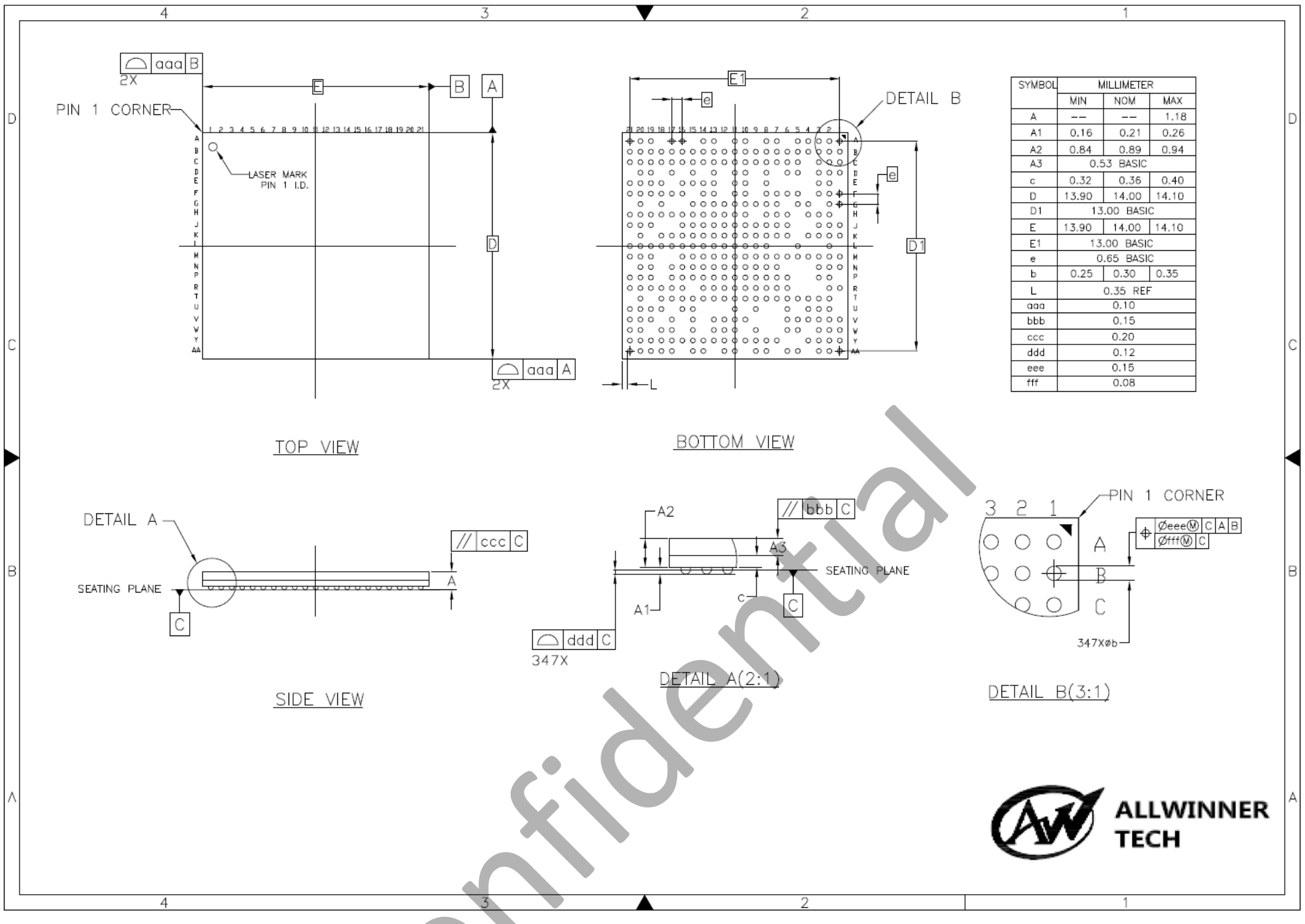
Pin Map

The following figure shows the pin maps of the 347-pin FBGA package of H5 processor.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
A	JTAG-SEL0	EPHY-LINK-LED	EPHY-TXN	EPHY-RXN	USB-DP0		USB-DP2	USB-DM2		PE1	PE11		PA20	PA21		PC7	PC5		PF1	PD4	GND	A
B	PG13	JTAG-SEL1	EPHY-TXP	EPHY-RXP	USB-DM0	USB-DP1	USB-DM1	USB-DP3	USB-DM3	PE0	PE2	PE12	PA18	PA19	PC3	PC2	PC12	PC8	PC13	PD2	PD6	B
C	PG5	PG4	PG8		PE15	PE14	PE13	PE7	PE4	PE3	PE8	PE9	PA12	PA17	PC0	PC1	PC9	PC11	PC15	PF5	PD0	C
D	PG12	PG11	PG7		PA1	PA2		PA7		PE6	PA0		PA9		PA16		PC10		PF0	PF2		D
E		HTXCN	PG9					PE10		PE5	PA10		PA3	PA6	PA13	PC6		PD7	PD12	PD8	PF4	E
F	HTX0N	HTXCP	PG3		PA4	EPHY-RTX	EPHY-SPD-LED	EPHY-VDD		TVOUT	PA11		PA8	PA15		PC4	PC14	PF3	PD5	PD11	PD9	F
G	HTX0P	HTX1N		PG6	HCEC		EPHY-VCC	GND	V33-TV	VDD-EFUSE	VCC-USB	PA14	VCC-IO	VCC-IO	VCC-PC			PF6		SDQM1		G
H		HTX1P	HSCL	PG2		PA5	VCC-PG	GND		VDD-SYS	VDD-EFUSEBP	GND	VCC-IO	VCC-IO	GND	PC16	PD1	PD3	PD10	SDQ9	SDQ10	H
J	HTX2P	HTX2N	PG0			HVCC	VDD-CPUS	VDD-CPUS	GND	VDD-SYS	VDD-SYS	VDD-GPUFB	GND	VCC-IO	VCC-PD	GND			SDQ8	SDQS1B	SDQ11	J
K	X24MOUT	X24MIN	HSDA	X24MFOUT		VCC-RTC	GND	GND	GND	VDD-SYS	VDD-SYS	VDD-SYS	GND	GND	GND	GND	PD13	PD15		SDQS1		K
L		PG1			PLLTEST			GND	GND	VDD-SYS	VDD-SYS	VDD-SYS	VDD-SYS	VDD-SYS	GND	VCC-DRAM	PD14	PD16	PD17	SDQ12	SDQ13	L
M	PL1	HHPD	PG10	RTC-VIO	GND	PL9	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC-DRAM			SDQ15	SDQM0	SDQ14	M
N	PL0	PL4	VCC-PLL				GND	VDD-CPUX	GND	GND	GND	GND	GND	GND	GND	VCC-DRAM	SA14		SA11	SDQ0		N
P		PL2	X32KFOUT			VDD-CPUX	VDD-CPUX	VDD-CPUX	VDD-CPUX	GND	GND	GND	GND	GND	GND	VCC-DRAM	VCC-DRAM		SA10	SDQ2	SDQ1	P
R	PL3	PL5				VDD-CPUX	VDD-CPUX	VDD-CPUX	GND	GND	GND	GND	GND	GND		VCC-DRAM	SA15	SA12	SDQ4	SDQS0	SDQS0B	R
T		PL8	PL7	PL6	TEST	VDD-CPUX	VDD-CPUX	VDD-CPUX	GND	VDD-CPUFB	GND	VCC-DRAM	VCC-DRAM	VCC-DRAM	VCC-DRAM	SVREF	SA0	SBA1		SDQ5		T
U		PL11	AGND	X32KOUT		VDD-CPUX			VDD-CPUX		VCC-DRAM				SCAS	SRST		SA1	SDQ6	SDQ7	SDQ3	U
V	LINEINL	PL10	AVCC	VRP	X32KIN	RESET				SZQ	SODT1	SA13	SRAS		SA7		SBA2		SA2	SA3	SA4	V
W	LINEINR	MICIN1P	MBIAS		VRA2	UBOOT			SDQ28		SODT0	SDQ24	SWE		SDQ19		SBA0	SA8		SCS0	SCS1	W
Y	MICIN1N	MICIN2P	LINEOUTR	VRA1			SDQ31	SDQ30	SDQS3B	SDQ27	SDQ26	SDQ23	SDQ22	SDQ20	SDQS2B	SDQ18	SDQ16	SA9	SA5	SA6	SCKE1	Y
AA	GND	MICIN2N	LINEOUTL		KEYADC	NMI		SDQ29	SDQS3		SDQ25	SDQM3		SDQ21	SDQS2		SDQ17	SDQM2	SCK	SCKB	SCKE0	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

Package Dimension

The following diagram shows the package dimension of H5 processor, includes the top, bottom, side views and details of the 14mmx14mm package.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.18
A1	0.16	0.21	0.26
A2	0.84	0.89	0.94
A3		0.53 BASIC	
c	0.32	0.36	0.40
D	13.90	14.00	14.10
D1		13.00 BASIC	
E	13.90	14.00	14.10
E1		13.00 BASIC	
e		0.65 BASIC	
b	0.25	0.30	0.35
L		0.35 REF	
aaa		0.10	
bbb		0.15	
ccc		0.20	
ddd		0.12	
eee		0.15	
fff		0.08	

