# Rockchip
# RK3588
# Technical Reference Manual

Rockchip Confidencial

## Revision History

| Date | Revision | Description |
|---|---|---|
| 2022-03-09 | 1.0 | Initial Release |

Copyright 2022 © Rockchip Electronics Co., Ltd.

# Table of Content

Table of Content ..... 2
Figure Index ..... 8
Table Index ..... 12
Warranty Disclaimer ..... 15
Chapter 1 System Overview ..... 16
1.1 Address Mapping ..... 16
1.2 System Boot ..... 20
1.3 System Interrupt Connection ..... 20
1.4 System DMA Hardware Request Connection ..... 27
Chapter 2 CRU ..... 29
2.1 Overview ..... 29
2.2 Block Diagram ..... 29
2.3 Function Description ..... 30
2.4 CRU Register Description ..... 33
2.5 DDR0CRU Register Description ..... 259
2.6 DDR1CRU Register Description ..... 265
2.7 DDR2CRU Register Description ..... 272
2.8 DDR3CRU Register Description ..... 278
2.9 BIGCORE0CRU Register Description ..... 284
2.10 BIGCORE1CRU Register Description ..... 292
2.11 DSUCRU Register Description ..... 300
2.12 PHPTOPCRU Register Description ..... 319
2.13 SBUSCRU Register Description ..... 323
2.14 SECURECRU Register Description ..... 328
2.15 PMU1CRU Register Description ..... 341
2.16 PMU1SCRU Register Description ..... 355
2.17 Application Notes ..... 358
Chapter 3 CPU ..... 362
3.1 Overview ..... 362
3.2 Block Diagram ..... 362
3.3 Function Description ..... 363
Chapter 4 Graphics Process Unit (GPU) ..... 364
4.1 Overview ..... 364
4.2 Block Diagram ..... 365
4.3 Function Description ..... 365
4.4 Register Description ..... 365
4.5 Interface Description ..... 365
4.6 Application Notes ..... 366
Chapter 5 VPU ..... 367
5.1 Overview ..... 367
5.2 Block Diagram ..... 368
5.3 Video frame format ..... 369
5.4 Function Description ..... 372
5.5 Register Description ..... 385
5.6 Application Notes ..... 674
Chapter 6 General Register Files (GRF) ..... 685
6.1 Overview ..... 685
6.2 Function Description ..... 685
6.3 PMU0_GRF Register Description ..... 686
6.4 PMU1_GRF Register Description ..... 691
6.5 SYS_GRF Register Description ..... 707
6.6 BIGCORE_GRF Register Description ..... 729
6.7 LITCORE_GRF Register Description ..... 732
6.8 DSU_GRF Register Description ..... 734

Rockchip Confidencial

6.9 DDR_GRF Register Description ..... 740
6.10 CENTER_GRF Register Description ..... 760
6.11 GPU_GRF Register Description ..... 763
6.12 NPU_GRF Register Description ..... 765
6.13 VOP_GRF Register Description ..... 769
6.14 VO0_GRF Register Description ..... 777
6.15 VO1_GRF Register Description ..... 786
6.16 USB_GRF Register Description ..... 800
6.17 PHP_GRF Register Description ..... 816
6.18 CSIDPHY_GRF Register Description ..... 858
6.19 PCIe3PHY_GRF Register Description ..... 859
6.20 PIPE_PHY_GRF Register Description ..... 928
6.21 USBDPPHY_GRF Register Description ..... 939
6.22 USB2PHY_GRF Register Description ..... 941
6.23 HDPTXPHY_GRF Register Description ..... 952
6.24 MIPICDPHY_GRF Register Description ..... 954
6.25 PMU1_IOC Register Description ..... 956
6.26 PMU2_IOC Register Description ..... 967
6.27 BUS_IOC Register Description ..... 983
6.28 VCCIO1_4_IOC Register Description ..... 1008
6.29 VCCIO3_5_IOC Register Description ..... 1028
6.30 VCCIO2_IOC Register Description ..... 1063
6.31 VCCIO6_IOC Register Description ..... 1068
6.32 EMMC_IOC Register Description ..... 1081
6.33 Application Notes ..... 1089
Chapter 7 Power Management Unit (PMU) ..... 1091
7.1 Overview ..... 1091
7.2 Block Diagram ..... 1091
7.3 Function Description ..... 1092
7.4 Register Description ..... 1098
7.5 Application Notes ..... 1268
Chapter 8 MMU600 ..... 1273
8.1 Overview ..... 1273
8.2 Block Diagram ..... 1275
8.3 Function Description ..... 1275
Chapter 9 MCU Subsystem ..... 1276
9.1 Overview ..... 1276
9.2 Block Diagram ..... 1276
9.3 Register Description ..... 1278
9.4 Interface Description ..... 1296
9.5 Application Notes ..... 1297
Chapter 10 Timer ..... 1301
10.1 Overview ..... 1301
10.2 Block Diagram ..... 1301
10.3 Function Description ..... 1302
10.4 Register Description ..... 1305
10.5 Application Notes ..... 1311
Chapter 11 GIC600 ..... 1312
11.1 Overview ..... 1312
11.2 Block Diagram ..... 1313
11.3 Function Description ..... 1313
Chapter 12 DMA Controller (DMAC) ..... 1314
12.1 Overview ..... 1314
12.2 Block Diagram ..... 1315
12.3 Function Description ..... 1316
12.4 Register Description ..... 1317

Rockchip Confidential

12.5 Timing Diagram ..... 1364
12.6 Application Notes ..... 1364
Chapter 13 SDMMC_BUFFER ..... 1371
13.1 Overview ..... 1371
13.2 Block Diagram ..... 1371
13.3 Function Description ..... 1371
13.4 Interface Description ..... 1371
13.5 Application Notes ..... 1371
Chapter 14 Temperature-Sensor ADC (TS-ADC) ..... 1372
14.1 Overview ..... 1372
14.2 Block Diagram ..... 1372
14.3 Function Description ..... 1372
14.4 Register Description ..... 1373
14.5 Application Notes ..... 1393
Chapter 15 Debug ..... 1394
15.1 Overview ..... 1394
15.2 Block Diagram ..... 1394
15.3 Function Description ..... 1394
15.4 Register Description ..... 1394
15.5 Interface Description ..... 1395
Chapter 16 Mailbox ..... 1397
16.1 Overview ..... 1397
16.2 Block Diagram ..... 1397
16.3 Function Description ..... 1397
16.4 Register Description ..... 1397
16.5 Application Notes ..... 1401
Chapter 17 Watchdog Timer(WDT) ..... 1403
17.1 Overview ..... 1403
17.2 Block Diagram ..... 1403
17.3 Function Description ..... 1403
17.4 Register Description ..... 1404
17.5 Application Notes ..... 1407
Chapter 18 Pulse Width Modulation (PWM) ..... 1408
18.1 Overview ..... 1408
18.2 Block Diagram ..... 1409
18.3 Function Description ..... 1409
18.4 Register Description ..... 1410
18.5 Interface Description ..... 1429
18.6 Application Notes ..... 1432
Chapter 19 UART ..... 1435
19.1 Overview ..... 1435
19.2 Block Diagram ..... 1435
19.3 Function Description ..... 1436
19.4 Register Description ..... 1438
19.5 Interface Description ..... 1457
19.6 Application Notes ..... 1464
Chapter 20 GPIO ..... 1468
20.1 Overview ..... 1468
20.2 Block Diagram ..... 1468
20.3 Function Description ..... 1468
20.4 Register Description ..... 1469
20.5 Interface Description ..... 1479
20.6 Application Notes ..... 1490
Chapter 21 I2C Interface ..... 1491
21.1 Overview ..... 1491

Rockchip Confidential

21.2 Block Diagram ..... 1491
21.3 Function Description ..... 1492
21.4 Register Description ..... 1494
21.5 Interface Description ..... 1503
21.6 Application Notes ..... 1508
Chapter 22 I2S ..... 1511
22.1 Overview ..... 1511
22.2 Block Diagram ..... 1512
22.3 Function description ..... 1513
22.4 Register description ..... 1518
22.5 Interface Description ..... 1543
22.6 Application Notes ..... 1548
Chapter 23 SPDIF Transmitter ..... 1550
23.1 Overview ..... 1550
23.2 Block Diagram ..... 1551
23.3 Function description ..... 1551
23.4 Register Description ..... 1553
23.5 Interface Description ..... 1559
23.6 Application Notes ..... 1560
Chapter 24 SPDIF Receiver ..... 1561
24.1 Overview ..... 1561
24.2 Block Diagram ..... 1561
24.3 Function description ..... 1562
24.4 Register Description ..... 1564
24.5 Interface Description ..... 1572
24.6 Application Notes ..... 1573
Chapter 25 Gigabit Media Access Controller (GMAC) ..... 1574
25.1 Overview ..... 1574
25.2 Block Diagram ..... 1577
25.3 Function Description ..... 1578
25.4 Register Description ..... 1583
25.5 Interface Description ..... 1798
25.6 Application Note ..... 1800
Chapter 26 SAR-ADC ..... 1824
26.1 Overview ..... 1824
26.2 Block Diagram ..... 1824
26.3 Function Description ..... 1824
26.4 Register Description ..... 1824
26.5 Timing Diagram ..... 1842
26.6 Application Notes ..... 1842
Chapter 27 Digital Audio Codec ..... 1843
27.1 Overview ..... 1843
27.2 Block Diagram ..... 1843
27.3 Function description ..... 1844
27.4 Register Description ..... 1844
27.5 Interface Description ..... 1855
27.6 Application Notes ..... 1855
Chapter 28 Voice Activity Detect (VAD) ..... 1857
28.1 Overview ..... 1857
28.2 Block Diagram ..... 1857
28.3 Function Description ..... 1858
28.4 Register Description ..... 1860
28.5 Application Notes ..... 1869
Chapter 29 CAN ..... 1872
29.1 Overview ..... 1872

Rockchip Confidencial

29.2 Features ..... 1872
29.3 Function Description ..... 1873
29.4 Register Description ..... 1879
29.5 Interface Description ..... 1898
29.6 Application Notes ..... 1899
Chapter 30 Flexible Serial Peripheral Interface (FSPI ) ..... 1903
30.1 Overview ..... 1903
30.2 Block Diagram ..... 1903
30.3 Function Description ..... 1903
30.4 Register Description ..... 1904
30.5 Interface Description ..... 1922
30.6 Application Notes ..... 1924
Chapter 31 Serial Peripheral Interface (SPI) ..... 1928
31.1 Overview ..... 1928
31.2 Block Diagram ..... 1928
31.3 Function Description ..... 1930
31.4 Register Description ..... 1931
31.5 Interface Description ..... 1940
31.6 Application Notes ..... 1945
Chapter 32 SPINLOCK ..... 1948
32.1 Overview ..... 1948
32.2 Block Diagram ..... 1948
32.3 Register Description ..... 1948
Chapter 33 KEYLAD ..... 1949
33.1 Overview ..... 1949
33.2 Block Diagram ..... 1949
33.3 Function Description ..... 1950
33.4 Register Description ..... 1950
33.5 Application Note ..... 1964
Chapter 34 Share Memory ..... 1965
34.1 Overview ..... 1965
34.2 Block Diagram ..... 1965
34.3 Function Description ..... 1965
34.4 Register Description ..... 1965
34.5 Application Notes ..... 1969
Chapter 35 DECOM ..... 1972
35.1 Overview ..... 1972
35.2 Block Diagram ..... 1972
35.3 Function Description ..... 1972
35.4 Register Description ..... 1974
35.5 Application Notes ..... 1983
Chapter 36 RKNN ..... 1984
36.1 Overview ..... 1984
36.2 Block Diagram ..... 1984
36.3 Function Description ..... 1985
36.4 Register Description ..... 1986
36.5 Application Notes ..... 2052
Chapter 37 Video Capture (VICAP) ..... 2058
37.1 Overview ..... 2058
37.2 Block Diagram ..... 2058
37.3 Function Description ..... 2058
37.4 VICAP Register Description ..... 2065
37.5 Interface Description ..... 2255
37.6 Application Notes ..... 2257
Chapter 38 FishEye Correction(FEC) ..... 2259

Rockchip Confidencial

38.1 Overview ..... 2259
38.2 Block Diagram ..... 2259
38.3 Function Description ..... 2259
38.4 Register Description ..... 2261
38.5 Application Notes ..... 2275
Chapter 39 Pulse Density Modulation Interface Controller ..... 2276
39.1 Overview ..... 2276
39.2 Block Diagram ..... 2276
39.3 Function Description ..... 2277
39.4 Register Description ..... 2278
39.5 Interface Description ..... 2285
39.6 Application Notes ..... 2287

Rockchip Confidential

# Figure Index

Fig. 2-1 CRU Block Diagram ..... 30
Fig. 2-2 Reset Architecture Diagram ..... 31
Fig. 2-3 FRACPLL Block Diagram ..... 32
Fig. 2-4 INTPLL Block Diagram ..... 32
Fig. 2-5 DDRPLL Block Diagram ..... 33
Fig. 2-6 PLL Start-up Operation ..... 359
Fig. 2-7 PLL Bypass Operation ..... 359
Fig. 2-8 PLL Glitch-free Scaler Operation ..... 359
Fig. 3-1 Block Diagram ..... 363
Fig. 4-1 GPU Architecture ..... 365
Fig. 5-1 Combo Block Diagram ..... 368
Fig. 5-2 VCODEC YCbCr 4:2:0 planar format ..... 369
Fig. 5-3 VCODEC YCbCr 4:2:0 Semi-planar format ..... 370
Fig. 5-4 VCODEC YCbCr4:2:2 Interleaved format ..... 370
Fig. 5-5 VCODEC AYCbCr 4:4:4 Interleaved format ..... 371
Fig. 5-6 VCODEC Tile scan mode ..... 371
Fig. 5-7 VCODEC RGB 16bpp format ..... 372
Fig. 5-8 FBC output format ..... 372
Fig. 5-9 Structure of two-level page table ..... 373
Fig. 5-10 Link table register prepare in DDR format ..... 377
Fig. 5-11 The dataflow of JPEG decoder and post-processor ..... 382
Fig. 5-12 Post-process Dataflow ..... 384
Fig. 5-13 MMU config flow ..... 674
Fig. 5-14 Link table mode work flow ..... 675
Fig. 5-15 Ccu mode work flow ..... 676
Fig. 5-16 VEPU mode mode ..... 677
Fig. 5-17 HEVC ROI configuration summary ..... 681
Fig. 5-18 H.264 ROI configuration summary ..... 683
Fig. 7-1 PMU Bock Diagram ..... 1092
Fig. 7-2 RK3588 Voltage Domain and Power Domain Partition ..... 1092
Fig. 8-1 Block Diagram ..... 1275
Fig. 9-1 Block Diagram of PMU_M0 Subsystem ..... 1277
Fig. 9-2 Block Diagram of NPU_M0 Subsystem ..... 1278
Fig. 9-3 Block Diagram of DDR_M0 Subsystem ..... 1278
Fig. 10-1 Normal Timer Block Diagram ..... 1301
Fig. 10-2 HPTIMER Block Diagram ..... 1302
Fig. 10-3 Timer Usage Flow ..... 1303
Fig. 10-4 Timing between timer_en and timer_clk ..... 1311
Fig. 11-1 Block Diagram ..... 1313
Fig. 12-1 Block Diagram of DMAC ..... 1316
Fig. 12-2 DMAC Operation State ..... 1317
Fig. 12-3 DMAC Request and Acknowledge Timing ..... 1364
Fig. 13-1 SDMMC_BUFFER Architecture ..... 1371
Fig. 14-1 TS-ADC Controller Block Diagram ..... 1372
Fig. 14-2 Timing diagram for TS-ADC ..... 1393
Fig. 15-1 Debug System Structure ..... 1394
Fig. 15-2 DAP SWJ Interface ..... 1395
Fig. 15-3 SW-DP Acknowledgement Timing ..... 1395
Fig. 16-1 Mailbox Block Diagram ..... 1397
Fig. 17-1 WDT Block Diagram ..... 1403
Fig. 17-2 WDT Operation Flow (RMOD=1) ..... 1404
Fig. 18-1 PWM Block Diagram ..... 1409
Fig. 18-2 PWM Capture Mode ..... 1409
Fig. 18-3 PWM Continuous Left-aligned Output Mode ..... 1410
Fig. 18-4 PWM Continuous Center-aligned Output Mode ..... 1410

Rockchip Confidential

Fig. 18-5 PWM One-shot Center-aligned Output Mode ..... 1410
Fig. 19-1 UART Architecture ..... 1435
Fig. 19-2 UART Serial protocol ..... 1436
Fig. 19-3 UART baud rate ..... 1436
Fig. 19-4 UART Auto flow control block diagram ..... 1437
Fig. 19-5 UART AUTO RTS TIMING ..... 1438
Fig. 19-6 UART AUTO CTS TIMING ..... 1438
Fig. 19-7 UART none fifo mode ..... 1464
Fig. 19-8 UART fifo mode ..... 1465
Fig. 19-9 UART0-UART4 clock generation ..... 1466
Fig. 19-10 UART5-UART9 clock generation ..... 1467
Fig. 20-1 GPIO Block Diagram ..... 1468
Fig. 21-1 I2C architecture ..... 1491
Fig. 21-2 I2C DATA Validity ..... 1494
Fig. 21-3 I2C Start and stop conditions ..... 1494
Fig. 21-4 I2C Acknowledge ..... 1494
Fig. 21-5 I2C byte transfer ..... 1494
Fig. 21-6 I2C Flow chat for transmit only mode ..... 1508
Fig. 21-7 I2C Flow chat for receive only mode ..... 1509
Fig. 21-8 I2C Flow chat for mix mode ..... 1510
Fig. 22-1 I2S/PCM/TDM Controller (8-channel) Block Diagram ..... 1512
Fig. 22-2 I2S/PCM Controller (2-channel) Block Diagram ..... 1512
Fig. 22-3 I2S Transmitter-Master & Receiver-Slave Condition ..... 1513
Fig. 22-4 I2S Transmitter-Slave & Receiver-Master Condition ..... 1513
Fig. 22-5 I2S Normal Mode Timing Format ..... 1514
Fig. 22-6 I2S Left Justified Mode Timing Format ..... 1514
Fig. 22-7 I2S Right Justified Mode Timing Format ..... 1514
Fig. 22-8 PCM Early Mode Timing Format ..... 1514
Fig. 22-9 PCM Late1 Mode Timing Format ..... 1515
Fig. 22-10 PCM Late2 Mode Timing Format ..... 1515
Fig. 22-11 PCM Late3 Mode Timing Format ..... 1515
Fig. 22-12 TDM Normal Mode Timing Format (PCM Format) ..... 1516
Fig. 22-13 TDM Left Shift Mode 0 Timing Format (PCM Format) ..... 1516
Fig. 22-14 TDM Left Shift Mode 1 Timing Format (PCM Format) ..... 1516
Fig. 22-15 TDM Left Shift Mode 2 Timing Format (PCM Format) ..... 1517
Fig. 22-16 TDM Left Shift Mode 3 Timing Format (PCM Format) ..... 1517
Fig. 22-17 TDM Normal Mode Timing Format (I2S Format) ..... 1517
Fig. 22-18 TDM Left Justified Mode Timing Format (I2S Format) ..... 1518
Fig. 22-19 TDM Right Justified Mode Timing Format (I2S Format) ..... 1518
Fig. 22-20 I2S/PCM/TDM Controller Transmit Operation Flow Chart ..... 1549
Fig. 23-1 SPDIF transmitter Block Diagram ..... 1551
Fig. 23-2 SPDIF Frame Format ..... 1551
Fig. 23-3 SPDIF Sub-frame Format ..... 1552
Fig. 23-4 SPDIF Channel Coding ..... 1552
Fig. 23-5 SPDIF Preamble ..... 1553
Fig. 23-6 SPDIF transmitter operation flow chart ..... 1560
Fig. 24-1 SPDIF receiver Block Diagram ..... 1561
Fig. 24-2 SPDIF Frame Format ..... 1562
Fig. 24-3 SPDIF Sub-frame Format ..... 1562
Fig. 24-4 SPDIF Channel Coding ..... 1563
Fig. 24-5 SPDIF Preamble ..... 1563
Fig. 24-6 SPDIF receiver operation flow chart ..... 1573
Fig. 25-1 GMAC Block Diagram ..... 1577
Fig. 25-2 GMAC in SOC ..... 1577
Fig. 25-3 Frame Format ..... 1578
Fig. 25-4 RMII Transmission Bit Ordering ..... 1578
Fig. 25-5 Start of MII and RMII Transmission in 100-Mbps Mode ..... 1579

Rockchip Confidential

Fig. 25-6 End of MII and RMII Transmission in 100-Mbps Mode ..... 1579
Fig. 25-7 Start of MII and RMII Transmission in 10-Mbps Mode ..... 1579
Fig. 25-8 End of MII and RMII Transmission in 10-Mbps Mode ..... 1579
Fig. 25-9 RMII Receive Bit Ordering ..... 1580
Fig. 25-10 Descriptor Ring Structure ..... 1800
Fig. 25-11 RMII Clock Architecture When Clock Source From CRU ..... 1822
Fig. 25-12 RMII Clock Architecture When Clock Source From External OSC ..... 1822
Fig. 25-13 RGMII Clock Architecture When Clock Source From CRU ..... 1822
Fig. 25-14 RGMII Clock Architecture When Clock Source From External OSC ..... 1823
Fig. 26-1 SAR-ADC Block Diagram ..... 1824
Fig. 26-2 SAR-ADC Timing Diagram ..... 1842
Fig. 27-1 Digital Audio Codec Block Diagram ..... 1843
Fig. 28-1 VAD Block Diagram ..... 1858
Fig. 28-2 VAD_DET Block Diagram ..... 1859
Fig. 28-3 VAD usage flow (only used ram write interface mode) ..... 1869
Fig. 28-4 VAD usage flow (use bus mode and ram write interface mode) ..... 1870
Fig. 29-1 CAN Controller Block Diagram ..... 1873
Fig. 29-2 Bit timing FSM ..... 1874
Fig. 29-3 Bit timing waveform diagram ..... 1874
Fig. 29-4 Three sampling diagram ..... 1875
Fig. 29-5 Hard sync waveform diagram ..... 1875
Fig. 29-6 Resynchronization ..... 1876
Fig. 29-7 Receive data state diagram ..... 1877
Fig. 29-8 Bit Stuffing ..... 1878
Fig. 30-1 FSPI Architecture ..... 1903
Fig. 30-2 Program Flow ..... 1924
Fig. 30-3 Read Flow ..... 1925
Fig. 30-4 Command with DMA Flow ..... 1926
Fig. 30-5 SPI mode ..... 1927
Fig. 30-6 Idle cycles ..... 1927
Fig. 31-1 SPI Controller Block Diagram ..... 1929
Fig. 31-2 SPI Master and Slave Interconnection ..... 1930
Fig. 31-3 SPI Format (SCPH=0 SCPOL=0) ..... 1930
Fig. 31-4 SPI Format (SCPH=0 SCPOL=1) ..... 1931
Fig. 31-5 SPI Format (SCPH=1 SCPOL=0) ..... 1931
Fig. 31-6 SPI Format (SCPH=1 SCPOL=1) ..... 1931
Fig. 31-7 SPI Master transfer flow diagram ..... 1946
Fig. 31-8 SPI Slave transfer flow diagram ..... 1947
Fig. 32-1 Spinlock in System ..... 1948
Fig. 33-1 KEYLAD Architecture ..... 1949
Fig. 34-1 Block Diagram of Share Memory ..... 1965
Fig. 35-1 DECOM Block Diagram ..... 1972
Fig. 35-2 DECOM Data Flow ..... 1974
Fig. 36-1 RKNN Triple Core Architecture ..... 1984
Fig. 36-2 RKNN Single Core Architecture ..... 1985
Fig. 36-3 PC flow ..... 2053
Fig. 36-4 Convolution flow 1 ..... 2054
Fig. 36-5 Convolution flow 2 ..... 2055
Fig. 36-6 Pooling flow ..... 2056
Fig. 36-7 DPU flying mode flow ..... 2057
Fig. 37-1 VICAP Block Diagram ..... 2058
Fig. 38-1 FEC Block Diagram ..... 2259
Fig. 38-2 FEC function description ..... 2260
Fig. 38-3 FEC meshgrid overlap ..... 2260
Fig. 38-4 FEC meshgrid order in DDR ..... 2261
Fig. 39-1 PDM Block Diagram ..... 2276
Fig. 39-2 PDM with Eight Mono MIC ..... 2277

Rockchip Confidential

Fig. 39-3 PDM with Four Stereo MIC..... 2277
Fig. 39-4 PDM interface diagram with external MIC ..... 2278
Fig. 39-5 PDM Clock Structure..... 2278
Fig. 39-6 PDM Operation Flow ..... 2287

Rockchip Confidencial

# Table Index

Table 1-1 Address Mapping ..... 16
Table 1-2 Address Remapping ..... 20
Table 1-3 RK3588 Interrupt Connection List ..... 20
Table 1-4 RK3588 DMAC Hardware Request Connection List ..... 27
Table 3-1 CPU Configuration ..... 362
Table 4-1 MCU Serial Wire Debug Interface Description ..... 365
Table 5-1 MPEG-4/H.263 feature ..... 373
Table 5-2 MPEG-2/MPEG-1 features ..... 374
Table 5-3 Video H.265 decoder features ..... 374
Table 5-4 Video H.264 decoder features ..... 375
Table 5-5 Video vp9 decoder features ..... 375
Table 5-6 Video AVS2 decoder features ..... 375
Table 5-7 Video H.265 decoder Unique input data ..... 376
Table 5-8 Video H.264 decoder Unique input data ..... 376
Table 5-9 Video VP9 decoder Unique input data ..... 376
Table 5-10 Video AVS2 decoder Unique input data ..... 377
Table 5-11 Link table write back register ..... 378
Table 5-12 Colmv uncompress info ..... 380
Table 5-13 Row or Col buffer size required ..... 381
Table 5-14 JPEG features ..... 381
Table 5-15 Post-processor features ..... 383
Table 5-16 Video H.265 decoder features ..... 384
Table 5-17 Video Jpeg encoder feature ..... 384
Table 5-18 HEVC and H.264 encoder feature ..... 385
Table 5-19 Base address of config ..... 385
Table 5-20 Link Table Node Section mapping and size ..... 678
Table 5-21 Video Source Buffer allocation ..... 678
Table 5-22 ROI_BASE_STRUCT for HEVC ..... 681
Table 5-23 ROI_CUQP_SRUCT for HEVC ..... 681
Table 5-24 ROI ROI_AMV_STRUCT for HEVC ..... 682
Table 5-25 ROI ROI_PUMV_STRUCT for HEVC ..... 682
Table 5-26 ROI_BASE_STRUCT for H.264 ..... 683
Table 5-27 ROI_QP_SRUCT for H.264 ..... 684
Table 5-28 ROI ROI_AMV_STRUCT for H.264 ..... 684
Table 5-29 ROI ROI_PUMV_STRUCT for H.264 ..... 684
Table 6-1 GRF Address Mapping Table ..... 685
Table 7-1 RK3588 Voltage Domain and Power Domain Summary ..... 1092
Table 7-2 Nested Power Domain 1 ..... 1268
Table 7-3 Nested Power Domain 2 ..... 1269
Table 7-4 Power Management IO Interface ..... 1270
Table 7-5 PMU Debug IO Interface ..... 1271
Table 7-6 PMU Debug Information Decode Before Enter Power Mode 0 ..... 1271
Table 7-7 PMU Debug Information Decode After Enter Power Mode 0 ..... 1272
Table 8-1 MMU600_PCIE Configuration ..... 1273
Table 8-2 MMU600_PHP Configuration ..... 1273
Table 9-1 MCU Subsystem Configurations ..... 1276
Table 9-2 MCU Serial Wire Debug Interface Description ..... 1297
Table 9-3 PMU_M0 Address Remap ..... 1297
Table 9-4 NPU_M0 Address Remap ..... 1297
Table 9-5 DDR_M0 Address Remap ..... 1297
Table 9-6 Address Map for the Cache RAM Debug ..... 1299
Table 10-1 TIMER attribute ..... 1311
Table 11-1 GIC600 Configuration ..... 1312
Table 12-1 DMAC Request Mapping Table ..... 1314
Table 13-1 SDMMC_BUFFER interface mapping ..... 1371

Rockchip Confidential

Table 14-1 Temperature Code Mapping ..... 1393
Table 15-1 SW-DP Interface Description ..... 1395
Table 18-1 PWM Interface Description ..... 1429
Table 19-1 UART0 Interface Description ..... 1457
Table 19-2 UART1 Interface Description ..... 1457
Table 19-3 UART2 Interface Description ..... 1458
Table 19-4 UART3 Interface Description ..... 1459
Table 19-5 UART4 Interface Description ..... 1459
Table 19-6 UART5 Interface Description ..... 1460
Table 19-7 UART6 Interface Description ..... 1461
Table 19-8 UART7 Interface Description ..... 1461
Table 19-9 UART8 Interface Description ..... 1462
Table 19-10 UART9 Interface Description ..... 1463
Table 19-11 UART baud rate configuration ..... 1467
Table 20-1 GPIO Interface Description ..... 1479
Table 21-1 I2C Interface Description ..... 1503
Table 22-1 I2S0 Interface Description ..... 1543
Table 22-2 I2S1 Group 0 Interface Description ..... 1544
Table 22-3 I2S1 Group 1 Interface Description ..... 1545
Table 22-4 I2S2 Group 0 Interface Description ..... 1546
Table 22-5 I2S2 Group 1 Interface Description ..... 1546
Table 22-6 I2S3 Interface Description ..... 1547
Table 22-7 I2S4/8 and DPTX0/1 Interface Description ..... 1547
Table 22-8 I2S5/6 and EDP TX Controller0/1 Interface Description ..... 1547
Table 22-9 I2S5/6 and HDMI TX Controller0/1 Interface Description ..... 1548
Table 22-10 I2S7 and HDMIRX Interface Description ..... 1548
Table 22-11 I2S9/10 and HDMI TX Controller0/1 Interface Description ..... 1548
Table 23-1 Maximum Frequency of MCLK for the 6 SPDIF Transmitters ..... 1550
Table 23-2 SPDIF0 Interface Description ..... 1559
Table 23-3 SPDIF1 Interface Description ..... 1559
Table 25-1 MDIO Clause 45 Frame Structure ..... 1580
Table 25-2 MDIO Clause 22 Frame Structure ..... 1581
Table 25-3 GMAC0 Interface ..... 1798
Table 25-4 GMAC1 Interface ..... 1798
Table 25-5 TDES0 Normal Descriptor (Read Format) ..... 1801
Table 25-6 TDES1 Normal Descriptor (Read Format) ..... 1801
Table 25-7 TDES2 Normal Descriptor (Read Format) ..... 1801
Table 25-8 TDES3 Normal Descriptor (Read Format) ..... 1802
Table 25-9 TDES0 Normal Descriptor (Write-Back Format) ..... 1804
Table 25-10 TDES1 Normal Descriptor (Write-Back Format) ..... 1804
Table 25-11 TDES2 Normal Descriptor (Write-Back Format) ..... 1805
Table 25-12 TDES2 Normal Descriptor (Write-Back Format) ..... 1805
Table 25-13 TDES0 Context Descriptor ..... 1812
Table 25-14 TDES1 Context Descriptor ..... 1812
Table 25-15 TDES2 Context Descriptor ..... 1812
Table 25-16 TDES3 Context Descriptor ..... 1812
Table 25-17 TDES0 Normal Descriptor(Read Format) ..... 1814
Table 25-18 TDES1 Normal Descriptor(Read Format) ..... 1814
Table 25-19 TDES2 Normal Descriptor(Read Format) ..... 1814
Table 25-20 TDES3 Normal Descriptor(Read Format) ..... 1814
Table 25-21 TDES0 Normal Descriptor(Write-Back Format) ..... 1815
Table 25-22 TDES1 Normal Descriptor(Write-Back Format) ..... 1815
Table 25-23 TDES2 Normal Descriptor(Write-Back Format) ..... 1817
Table 25-24 TDES3 Normal Descriptor(Write-Back Format) ..... 1818
Table 25-25 TDES0 Context Descriptor ..... 1820
Table 25-26 TDES1 Context Descriptor ..... 1820
Table 25-27 TDES2 Context Descriptor ..... 1821

Rockchip Confidential

Table 25-28 TDES3 Context Descriptor ..... 1821
Table 27-1 Digital Audio Codec Interface Description ..... 1855
Table 29-1 Receive FIFO message format..... 1877
Table 29-2 TXE FIFO message format..... 1879
Table 29-3 CAN Interface Description ..... 1898
Table 30-1 FSPI Address Mapping Table ..... 1904
Table 30-2 FSPI IO M0 Group Interface Description ..... 1922
Table 30-3 FSPI M1 Group Interface Description ..... 1922
Table 30-4 FSPI M2 Group Interface Description ..... 1923
Table 31-1 SPI0 interface description ..... 1940
Table 31-2 SPI1 interface description ..... 1941
Table 31-3 SPI2 interface description ..... 1942
Table 31-4 SPI3 interface description ..... 1943
Table 31-5 SPI4 interface description ..... 1944
Table 37-1 VICAP Address Mapping ..... 2065
Table 37-2 VICAP Interface Description..... 2255
Table 39-1 Relation between PDM_CLK and Sample Rate..... 2278
Table 39-2 Group 0 PDM0 IO Interface Description ..... 2285
Table 39-3 Group 1 PDM0 IO Interface Description ..... 2286
Table 39-4 Group 0 PDM1 IO Interface Description ..... 2286
Table 39-5 Group 1 PDM1 IO Interface Description ..... 2286

Rockchip Confidential

# Warranty Disclaimer

Rockchip Electronics Co., Ltd makes no warranty, representation or guarantee (expressed, implied, statutory, or otherwise) by or with respect to anything in this document, and shall not be liable for any implied warranties of non-infringement, merchantability or fitness for a particular purpose or for any indirect, special or consequential damages.

Information furnished is believed to be accurate and reliable. However, Rockchip Electronics Co.,Ltd assumes no responsibility for the consequences of use of such information or for any infringement of patents or other rights of third parties that may result from its use.

Rockchip Electronics Co., Ltd's products are not designed, intended, or authorized for using as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Rockchip Electronics Co., Ltd's product could create a situation where personal injury or death may occur, should buyer purchase or use Rockchip Electronics Co., Ltd's products for any such unintended or unauthorized application, buyers shall indemnify and hold Rockchip Electronics Co., Ltd and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, expenses, and reasonable attorney fees arising out of, either directly or indirectly, any claim of personal injury or death that may be associated with such unintended or unauthorized use, even if such claim alleges that Rockchip Electronics Co., Ltd was negligent regarding the design or manufacture of the part.

## Copyright and Patent Right

Information in this document is provided solely to enable system and software implementers to use Rockchip Electronics Co.,Ltd 's products. There are no expressed and patent or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

**Rockchip Electronics Co., Ltd does not convey any license under its copyright and patent rights nor the rights of others.**
**All copyright and patent rights referenced in this document belong to their respective owners and shall be subject to corresponding copyright and patent licensing requirements.**

## Trademarks

Rockchip and Rockchip™ logo and the name of Rockchip Electronics Co., Ltd's products are trademarks of Rockchip Electronics Co., Ltd. and are exclusively owned by Rockchip Electronics Co., Ltd. References to other companies and their products use trademarks owned by the respective companies and are for reference purpose only.

## Confidentiality

The information contained herein (including any attachments) is confidential. The recipient hereby acknowledges the confidentiality of this document, and except for the specific purpose, this document shall not be disclosed to any third party.

## Reverse engineering or disassembly is prohibited.

**ROCKCHIP ELECTRONICS CO.,LTD. RESERVES THE RIGHT TO MAKE CHANGES IN ITS PRODUCTS OR PRODUCT SPECIFICATIONS WITH THE INTENT TO IMPROVE FUNCTION OR DESIGN AT ANY TIME AND WITHOUT NOTICE AND IS NOT REQUIRED TO UNDATE THIS DOCUMENTATION TO REFLECT SUCH CHANGES.**

## Copyright © 2022 Rockchip Electronics Co., Ltd.

All rights reserved. No part of this publication may be reproduced, stored in a retrieval system, or transmitted in any form or by any means, electric or mechanical, by photocopying, recording, or otherwise, without the prior written consent of Rockchip Electronics Co., Ltd.

Rockchip Confidential

# Chapter 1 System Overview

## 1.1 Address Mapping

RK3588 boot from internal BootRom, which supports remap function by software programming. Remap is controlled by PMU_SGRF_SOC_CON2[1:0]. When remap is set to 2'b01, the BootRom is un-accessible and PMU_SRAM is mapped to address 0xFFFF0000. When remap is set to 2'b10, the BootRom is un-accessible and SYSTEM_SRAM is mapped to address 0xFFFF0000.

Table 1-1 Address Mapping

| Module | Start Address | Size | Module | Start Address | Size |
|---|---|---|---|---|---|
| PCIe3_4L_S | F0000000 | 16MB | SPDIF_RX2 | FDE18000 | 32KB |
| PCIe3_2L_S | F1000000 | 16MB | DSI HOST0 | FDE20000 | 64KB |
| PCIe3_1L0_S | F2000000 | 16MB | DSI HOST1 | FDE30000 | 64KB |
| PCIe3_1L1_S | F3000000 | 16MB | HDCP0 | FDE40000 | 32KB |
| PCIe3_1L2_S | F4000000 | 16MB | HDCP0_TRNG | FDE48000 | 32KB |
| PCIe3_4L_DBI | F5000000 | 4MB | DP0 | FDE50000 | 64KB |
| PCIe3_2L_DBI | F5400000 | 4MB | DP1 | FDE60000 | 64KB |
| PCIe3_1L0_DBI | F5800000 | 4MB | HDCP1 | FDE70000 | 32KB |
| PCIe3_1L1_DBI | F5C00000 | 4MB | HDCP1_TRNG | FDE78000 | 32KB |
| PCIe3_1L2_DBI | F6000000 | 4MB | HDMI TX0 | FDE80000 | 128KB |
| Reserved | F6400000 | 11MB | HDMI TX1 | FDEA0000 | 128KB |
| MCU_TCM | F6F00000 | 64KB | eDP0 | FDEC0000 | 64KB |
| MCU_CACHE | F6F10000 | 64KB | eDP1 | FDED0000 | 64KB |
| MCU_RAM_TEST | F6F20000 | 64KB | HDMI RX | FDEE0000 | 64KB |
| Reserved | F6F30000 | 832KB | HDCP_KEY 0 | FDEF0000 | 32KB |
| DDRCTL_0 | F7000000 | 16MB | HDCP_KEY 1 | FDEF8000 | 64KB |
| DDRCTL_1 | F8000000 | 16MB | Reserved | FDF08000 | 32KB |
| DDRCTL_2 | F9000000 | 16MB | HDMIRX_S | FDF10000 | 16KB |
| DDRCTL_3 | FA000000 | 16MB | Reserved | FDF14000 | 16KB |
| GPU G610 | FB000000 | 16MB | eDP0_S | FDF18000 | 16KB |
| USB3_0 | FC000000 | 4MB | eDP1_S | FDF1C000 | 16KB |
| USB3_1 | FC400000 | 4MB | Reserved | FDF20000 | 64KB |
| USB2HOST_0 | FC800000 | 512KB | INTERCONNECT | FDF30000 | 896KB |
| USB2HOST_1 | FC880000 | 512KB | FIREWALL_DSUDDR | FE010000 | 32KB |
| MMU600_PCIE | FC900000 | 2MB | Reserved | FE018000 | 96KB |
| MMU600_PHP | FCB00000 | 2MB | FIREWALL_DDR | FE030000 | 32KB |
| USB3_2 | FCD00000 | 4MB | FIREWALL_SYSMEM | FE038000 | 32KB |
| DAPLITE2 | FD100000 | 512KB | Reserved | FE040000 | 64KB |
| Reserved | FD180000 | 512KB | DMA2DDR | FE050000 | 64KB |
| Reserved | FD200000 | 64KB | DDR_MON0 | FE060000 | 16KB |
| Reserved | FD210000 | 3520KB | DDR_MON1 | FE064000 | 16KB |
| PMU0_SGRF | FD580000 | 8KB | DDR_MON2 | FE068000 | 16KB |
| PMU1_SGRF | FD582000 | 8KB | DDR_MON3 | FE06C000 | 16KB |
| Reserved | FD584000 | 8KB | Reserved | FE070000 | 320KB |
| BUS_SGRF | FD586000 | 4KB | DDRPHY0 | FE0C0000 | 64KB |

Rockchip Confidential

| Module | Start Address | Size | Module | Start Address | Size |
|---|---|---|---|---|---|
| DSU_SGRF | FD587000 | 4KB | DDRPHY1 | FE0D0000 | 64KB |
| PMU0_GRF | FD588000 | 8KB | DDRPHY2 | FE0E0000 | 64KB |
| PMU1_GRF | FD58A000 | 8KB | DDRPHY3 | FE0F0000 | 64KB |
| SYS_GRF | FD58C000 | 16KB | Reserved | FE100000 | 64KB |
| BIGCORE0_GRF | FD590000 | 8KB | WDT_DDR | FE110000 | 32KB |
| BIGCORE1_GRF | FD592000 | 8KB | TIMER_DDR(2CH) | FE118000 | 32KB |
| LITCORE_GRF | FD594000 | 16KB | SHARE_MEM_SLV | FE120000 | 32KB |
| DSU_GRF | FD598000 | 16KB | AHB2APB | FE128000 | 32KB |
| DDR01_GRF | FD59C000 | 4KB | Reserved | FE130000 | 128KB |
| DDR23_GRF | FD59D000 | 4KB | PCIe3_4L_APB | FE150000 | 64KB |
| CENTER_GRF | FD59E000 | 8KB | PCIe3_2L_APB | FE160000 | 64KB |
| GPU_GRF | FD5A0000 | 8KB | PCIe3_1L0_APB | FE170000 | 64KB |
| NPU_GRF | FD5A2000 | 8KB | PCIe3_1L1_APB | FE180000 | 64KB |
| VOP_GRF | FD5A4000 | 8KB | PCIe3_1L2_APB | FE190000 | 64KB |
| VO0_GRF | FD5A6000 | 8KB | Reserved | FE1A0000 | 64KB |
| VO1_GRF | FD5A8000 | 16KB | GMAC0 | FE1B0000 | 64KB |
| USB_GRF | FD5AC000 | 16KB | GMAC1 | FE1C0000 | 64KB |
| PHP_GRF | FD5B0000 | 16KB | Reserved | FE1D0000 | 256KB |
| CSIDPHY0_GRF | FD5B4000 | 4KB | SATA0 | FE210000 | 64KB |
| CSIDPHY1_GRF | FD5B5000 | 4KB | SATA1 | FE220000 | 64KB |
| Reserved | FD5B6000 | 8KB | SATA2 | FE230000 | 64KB |
| PCIe3PHY_GRF | FD5B8000 | 16KB | Reserved | FE240000 | 448KB |
| PIPE_PHY0_GRF | FD5BC000 | 16KB | FSPI | FE2B0000 | 64KB |
| PIPE_PHY1_GRF | FD5C0000 | 16KB | SDMMC | FE2C0000 | 64KB |
| PIPE_PHY2_GRF | FD5C4000 | 16KB | SDIO | FE2D0000 | 64KB |
| USBDPPHY0_GRF | FD5C8000 | 16KB | EMMC | FE2E0000 | 64KB |
| USBDPPHY1_GRF | FD5CC000 | 16KB | SDMMC_BUF | FE2F0000 | 64KB |
| USB2PHY0_GRF | FD5D0000 | 16KB | Reserved | FE300000 | 448KB |
| USB2PHY1_GRF | FD5D4000 | 16KB | CRYPTO_NS | FE370000 | 32KB |
| USB2PHY2_GRF | FD5D8000 | 16KB | TRNG_NS | FE378000 | 32KB |
| USB2PHY3_GRF | FD5DC000 | 16KB | KEYLADDER_S | FE380000 | 64KB |
| HDPTXPHY0_GRF | FD5E0000 | 16KB | CRYPTO_S(Slave) | FE390000 | 32KB |
| HDPTXPHY1_GRF | FD5E4000 | 16KB | TRNG_S | FE398000 | 32KB |
| MIPIDCPHY0_GRF | FD5E8000 | 16KB | OTP_S | FE3A0000 | 64KB |
| MIPIDCPHY1_GRF | FD5EC000 | 16KB | Reserved | FE3B0000 | 64KB |
| PMU1_IOC | FD5F0000 | 16KB | DCF | FE3C0000 | 64KB |
| PMU2_IOC | FD5F4000 | 16KB | TIMER_S_0(6CH) | FE3D0000 | 64KB |
| BUS_IOC | FD5F8000 | 4KB | WDT_S | FE3E0000 | 64KB |
| VCCIO1_4_IOC | FD5F9000 | 4KB | SEC_TRNG_CHK | FE3F0000 | 64KB |
| VCCIO3_5_IOC | FD5FA000 | 4KB | Reserved | FE400000 | 128KB |
| VCCIO2_IOC | FD5FB000 | 4KB | CRYPTO_S(By Keylad) | FE420000 | 64KB |
| VCCIO6_IOC | FD5FC000 | 4KB | Reserved | FE430000 | 256KB |
| EMMC_IOC | FD5FD000 | 4KB | I2S0_8CH | FE470000 | 64KB |
| Reserved | FD5FE000 | 8KB | I2S1_8CH | FE480000 | 64KB |

Rockchip Confidential

| Module | Start Address | Size | Module | Start Address | Size |
|---|---|---|---|---|---|
| SYSTEM_SRAM | FD600000 | 1MB | I2S2_2CH | FE490000 | 64KB |
| PMU_MEM | FD700000 | 256KB | I2S3_2CH | FE4A0000 | 64KB |
| Reserved | FD740000 | 512KB | PDM0 | FE4B0000 | 64KB |
| CRU_NS | FD7C0000 | 32KB | PDM1 | FE4C0000 | 64KB |
| PHP_PPLL_CRU | FD7C8000 | 32KB | VAD | FE4D0000 | 64KB |
| SEC_SCRU | FD7D0000 | 32KB | SPDIF_TX0 | FE4E0000 | 64KB |
| BUS_SCRU | FD7D8000 | 32KB | SPDIF_TX1 | FE4F0000 | 64KB |
| PMU1_SCRU | FD7E0000 | 64KB | ACDCDIG_DSM | FE500000 | 64KB |
| PMU1_CRU | FD7F0000 | 64KB | Reserved | FE510000 | 576KB |
| DDRPHY0_CRU | FD800000 | 16KB | SPINLOCK | FE5A0000 | 64KB |
| DDRPHY1_CRU | FD804000 | 16KB | Reserved | FE5B0000 | 320KB |
| DDRPHY2_CRU | FD808000 | 16KB | GIC600 | FE600000 | 4MB |
| DDRPHY3_CRU | FD80C000 | 16KB | DMAC0_S | FEA00000 | 64KB |
| BIGCORE0_CRU | FD810000 | 8KB | DMAC0_NS | FEA10000 | 64KB |
| BIGCORE1_CRU | FD812000 | 8KB | DMAC1_S | FEA20000 | 64KB |
| Reserved | FD814000 | 16KB | DMAC1_NS | FEA30000 | 64KB |
| DSU_CRU | FD818000 | 16KB | Reserved | FEA40000 | 64KB |
| Reserved | FD81C000 | 400KB | CAN0 | FEA50000 | 64KB |
| I2C0 | FD880000 | 64KB | CAN1 | FEA60000 | 64KB |
| UART0 | FD890000 | 64KB | CAN2 | FEA70000 | 64KB |
| GPIO0 | FD8A0000 | 64KB | DECOM | FEA80000 | 64KB |
| PWM0 | FD8B0000 | 64KB | I2C1 | FEA90000 | 64KB |
| PVTM_PMU | FD8C0000 | 32KB | I2C2 | FEAA0000 | 64KB |
| HPTIMER | FD8C8000 | 16KB | I2C3 | FEAB0000 | 64KB |
| Reserved | FD8CC000 | 16KB | I2C4 | FEAC0000 | 64KB |
| PMU | FD8D0000 | 64KB | I2C5 | FEAD0000 | 64KB |
| WDT_PMU | FD8E0000 | 64KB | TIMER_NS_0(6CH) | FEAE0000 | 32KB |
| TIMER_PMU(2CH) | FD8F0000 | 64KB | TIMER_NS_1(6CH) | FEAE8000 | 32KB |
| Reserved | FD900000 | 704KB | WDT_NS | FEAF0000 | 64KB |
| OSC_CHK | FD9B0000 | 64KB | SPI0 | FEB00000 | 64KB |
| SCRAMBLE_KEY | FD9C0000 | 64KB | SPI1 | FEB10000 | 64KB |
| Reserved | FD9D0000 | 448KB | SPI2 | FEB20000 | 64KB |
| PVTM_CORE_B0 | FDA40000 | 32KB | SPI3 | FEB30000 | 64KB |
| Reserved | FDA48000 | 32KB | UART1 | FEB40000 | 64KB |
| PVTM_CORE_B1 | FDA50000 | 32KB | UART2 | FEB50000 | 64KB |
| Reserved | FDA58000 | 32KB | UART3 | FEB60000 | 64KB |
| PVTM_CORE_L | FDA60000 | 64KB | UART4 | FEB70000 | 64KB |
| Reserved | FDA70000 | 256KB | UART5 | FEB80000 | 64KB |
| RKNN C0 | FDAB0000 | 64KB | UART6 | FEB90000 | 64KB |
| RKNN C1 | FDAC0000 | 64KB | UART7 | FEBA0000 | 64KB |
| RKNN C2 | FDAD0000 | 64KB | UART8 | FEBB0000 | 64KB |
| Reserved | FDAE0000 | 64KB | UART9 | FEBC0000 | 64KB |
| PVTM_NPU | FDAF0000 | 32KB | PWM1 | FEBD0000 | 64KB |
| WDT_NPU | FDAF8000 | 32KB | PWM2 | FEBE0000 | 64KB |

Rockchip Confidential

| Module | Start Address | Size | Module | Start Address | Size |
|---|---|---|---|---|---|
| TIMER_NPU(2CH) | FDB00000 | 32KB | PWM3 | FEBF0000 | 64KB |
| Reserved | FDB08000 | 160KB | TSADC | FEC00000 | 64KB |
| PVTM_GPU | FDB30000 | 64KB | SARADC | FEC10000 | 64KB |
| Reserved | FDB40000 | 64KB | GPIO1 | FEC20000 | 64KB |
| VDPU | FDB50000 | 64KB | GPIO2 | FEC30000 | 64KB |
| RGA3_0 | FDB60000 | 64KB | GPIO3 | FEC40000 | 64KB |
| RGA3_1 | FDB70000 | 64KB | GPIO4 | FEC50000 | 64KB |
| RGA2 | FDB80000 | 64KB | MAILBOX0(MCU_PMU) | FEC60000 | 64KB |
| JPEG_DEC | FDB90000 | 64KB | MAILBOX1(MCU_DDR) | FEC70000 | 64KB |
| JPEG_ENC0 | FDBA0000 | 16KB | I2C6 | FEC80000 | 64KB |
| JPEG_ENC1 | FDBA4000 | 16KB | I2C7 | FEC90000 | 64KB |
| JPEG_ENC2 | FDBA8000 | 16KB | I2C8 | FECA0000 | 64KB |
| JPEG_ENC3 | FDBAC000 | 16KB | SPI4 | FECB0000 | 64KB |
| IEP | FDBB0000 | 64KB | OTP_NS | FECC0000 | 64KB |
| Reserved | FDBC0000 | 64KB | Reserved | FECD0000 | 64KB |
| RKVENC0 | FDBD0000 | 64KB | MAILBOX2(MCU_NPU) | FECE0000 | 64KB |
| RKVENC1 | FDBE0000 | 64KB | INTMUX(MCU_PMU) | FECF0000 | 32KB |
| Reserved | FDBF0000 | 256KB | INTMUX(MCU_DDR) | FECF8000 | 32KB |
| RKVDEC_CCU | FDC30000 | 32KB | DMAC2_S | FED00000 | 64KB |
| RKVDEC0 | FDC38000 | 32KB | DMAC2_NS | FED10000 | 64KB |
| RKVDEC1 | FDC40000 | 64KB | JTAG_LOCK | FED20000 | 32KB |
| Reserved | FDC50000 | 128KB | Reserved | FED28000 | 32KB |
| AV1 | FDC70000 | 256KB | TIMER_S_1(6CH) | FED30000 | 64KB |
| ISP0 | FDCB0000 | 64KB | Reserved | FED40000 | 128KB |
| ISP1 | FDCC0000 | 64KB | HDPTX Combo PHY0 | FED60000 | 64KB |
| FISHEYE0 | FDCD0000 | 32KB | HDPTX Combo PHY1 | FED70000 | 64KB |
| FISHEYE1 | FDCD8000 | 32KB | USBDP PHY0 | FED80000 | 64KB |
| VICAP | FDCE0000 | 128KB | USBDP PHY1 | FED90000 | 64KB |
| Reserved | FDD00000 | 64KB | MIPI CD PHY0 | FEDA0000 | 64KB |
| CSI HOST0 | FDD10000 | 64KB | MIPI CD PHY1 | FEDB0000 | 64KB |
| CSI HOST1 | FDD20000 | 64KB | MIPI CSI DPHY0 | FEDC0000 | 32KB |
| CSI HOST2 | FDD30000 | 64KB | MIPI CSI DPHY1 | FEDC8000 | 32KB |
| CSI HOST3 | FDD40000 | 64KB | Reserved | FEDD0000 | 64KB |
| CSI HOST4 | FDD50000 | 64KB | HDMI RX PHY | FEDE0000 | 64KB |
| CSI HOST5 | FDD60000 | 64KB | Reserved | FEDF0000 | 64KB |
| Reserved | FDD70000 | 128KB | Combo PIPE PHY0 | FEE00000 | 64KB |
| VOP | FDD90000 | 64KB | Combo PIPE PHY1 | FEE10000 | 64KB |
| HDCP0_MMU | FDDA0000 | 64KB | Combo PIPE PHY2 | FEE20000 | 64KB |
| SPDIF_TX2 | FDDB0000 | 32KB | Reserved | FEE30000 | 312KB |
| SPDIF_TX5 | FDDB8000 | 32KB | PCIe3 PHY | FEE80000 | 512KB |
| I2S4_8CH | FDDC0000 | 32KB | Reserved | FEF00000 | 1MB |
| I2S8_8CH | FDDC8000 | 32KB | SYSTEM_SRAM | FF000000 | 1MB |
| HDCP1_MMU | FDDD0000 | 64KB | PMU_MEM | FF100000 | 256KB |
| SPDIF_TX3 | FDDE0000 | 32KB | PCIe3_4L_S | 900000000 | 1024MB |

Rockchip Confidential

| Module | Start Address | Size | Module | Start Address | Size |
|---|---|---|---|---|---|
| SPDIF_TX4 | FDDE8000 | 32KB | PCIe3_2L_S | 940000000 | 1024MB |
| I2S5_8CH | FDDF0000 | 16KB | PCIe3_1L0_S | 980000000 | 1024MB |
| I2S6_8CH | FDDF4000 | 16KB | PCIe3_1L1_S | 9c0000000 | 1024MB |
| I2S7_8CH | FDDF8000 | 16KB | PCIe3_1L2_S | a00000000 | 1024MB |
| I2S9_8CH | FDDFC000 | 16KB | PCIe3_4L_DBI | a40000000 | 4MB |
| I2S10_8CH | FDE00000 | 16KB | PCIe3_2L_DBI | a40400000 | 4MB |
| Reserved | FDE04000 | 16KB | PCIe3_1L0_DBI | a40800000 | 4MB |
| SPDIF_RX0 | FDE08000 | 32KB | PCIe3_1L1_DBI | a40c00000 | 4MB |
| SPDIF_RX1 | FDE10000 | 32KB | PCIe3_1L2_DBI | a41000000 | 4MB |

The following table show the boot address when before remap and after remap

Table 1-2 Address Remapping

| remap[1:0]=2'b00 | | remap[1:0]=2'b01 | | remap[1:0]=2'b10 | |
|---|---|---|---|---|---|
| | | not accessible | BootRom(32KB) | not accessible | BootRom(32KB) |
| 0xFFFF0000 | BootRom(32KB) | 0xFFFF0000 | PMU_SRAM(8KB) | 0xFFFF0000 | SYSTEM_SRAM (256KB) |
| 0xFF100000 | PMU_SRAM(8KB) | 0xFF100000 | PMU_SRAM(8KB) | 0xFF100000 | PMU_SRAM(8KB) |
| 0xFF000000 | SYSTEM_SRAM(1MB) | 0xFF000000 | SYSTEM_SRAM(1MB) | 0xFF000000 | SYSTEM_SRAM(1MB) |

## 1.2 System Boot

RK3588 provides system boot from off-chip devices such as SDMMC card, eMMC memory, serial Nand or Nor flash. When boot code is not ready in these devices, also provide system code download into them by USB OTG interface. All of the boot code will be stored in internal BootRom. The following is the whole boot procedure for boot code, which will be stored in BootRom in advance.

The following features are supported.

- Support system boot from the following device:
  - Serial Nor Flash, 1bit or 4bits data width(device layout in FSPI IO)
  - Serial Nand Flash, 1bit data width(device layout in FSPI IO)
  - eMMC Interface, 8bits data width
  - SDMMC Card, 4bits data width
  - RK3588 has two bootwom:
    - Normal Bootrom in non-secure world, which CPU_S and CPU_NS both can access
    - Secure Bootrom in secure world, only CPU_S can access
- Support system code download by USB OTG

## 1.3 System Interrupt Connection

RK3588 provides an general interrupt controller (GIC) for CPU, which has 512 SPI (shared peripheral interrupts) interrupt sources and 12 PPI(Private peripheral interrupt) interrupt source. The triggered type for each SPI interrupt is high level sensitive, and triggered type for each PPI interrupt is low level sensitive, not programmable. The detailed interrupt sources connection is in the following table.

Table 1-3 RK3588 Interrupt Connection List

| Number | Source | Polarity | Number | Source | Polarity |
|---|---|---|---|---|---|
| 0-21 PPI | NA | Low level | 238 | irq_fspi | High level |

Rockchip Confidential

| Number | Source | Polarity | Number | Source | Polarity |
|---|---|---|---|---|---|
| 22 PPI | cpu_ncommirq | Low level | 239 | irq_keylad | High level |
| 23 PPI | cpu_npmuirq | Low level | 240 | irq_crypto_s | High level |
| 24 PPI | cpu_ctiirq | Low level | 241 | irq_crypto_ns | High level |
| 25 PPI | cpu_nvcpumntirq | Low level | 242 | irq_otp_s | High level |
| 26 PPI | cpu_ncnthpirq | Low level | 243 | irq_otp_ns | High level |
| 27 PPI | cpu_ncntvirq | Low level | 244 | irq_trng_chk | High level |
| 28 PPI | cpu_ncnthvirq | Low level | 245 | irq_dcf | High level |
| 29 PPI | cpu_ncntpsirq | Low level | 246 | irq_usb2host0_arb | High level |
| 30 PPI | cpu_ncntpnsirq | Low level | 247 | irq_usb2host0_ehci | High level |
| 31 PPI | NA | Low level | 248 | irq_usb2host0_ohci | High level |
| 32 | irq_dsu_nfaultirq0 | High level | 249 | irq_usb2host1_arb | High level |
| 33 | irq_dsu_nfaultirq1 | High level | 250 | irq_usb2host1_ehci | High level |
| 34 | irq_dsu_nfaultirq2 | High level | 251 | irq_usb2host1_ohci | High level |
| 35 | irq_dsu_nfaultirq3 | High level | 252 | irq_usb3otg0 | High level |
| 36 | irq_dsu_nfaultirq4 | High level | 253 | irq_usb3otg1 | High level |
| 37 | irq_dsu_nfaultirq5 | High level | 254 | irq_usb3otg2 | High level |
| 38 | irq_dsu_nfaultirq6 | High level | 255 | irq_gmac0_mcgr_dma_req | High level |
| 39 | irq_dsu_nfaultirq7 | High level | 256 | irq_gmac1_mcgr_dma_req | High level |
| 40 | irq_dsu_nfaultirq8 | High level | 257 | irq_gmac0_lpi | High level |
| 41 | irq_dsu_nerrirq0 | High level | 258 | irq_gmac0_pmt | High level |
| 42 | irq_dsu_nerrirq1 | High level | 259 | irq_gmac0_sbd | High level |
| 43 | irq_dsu_nerrirq2 | High level | 260 | irq_gmac0_sbd_perch_rx_o0 | High level |
| 44 | irq_dsu_nerrirq3 | High level | 261 | irq_gmac0_sbd_perch_rx_o1 | High level |
| 45 | irq_dsu_nerrirq4 | High level | 262 | irq_gmac0_sbd_perch_tx_o0 | High level |
| 46 | irq_dsu_nerrirq5 | High level | 263 | irq_gmac0_sbd_perch_tx_o1 | High level |
| 47 | irq_dsu_nerrirq6 | High level | 264 | irq_gmac1_lpi | High level |
| 48 | irq_dsu_nerrirq7 | High level | 265 | irq_gmac1_pmt | High level |
| 49 | irq_dsu_nerrirq8 | High level | 266 | irq_gmac1_sbd | High level |
| 50 | irq_dsu_nclusterpmuirq | High level | 267 | irq_gmac1_sbd_perch_rx_o0 | High level |
| 51 | irq_ddrctl_sbr_done_ch0 | High level | 268 | irq_gmac1_sbd_perch_rx_o1 | High level |
| 52 | irq_ddrctl_arpoison_ch0 | High level | 269 | irq_gmac1_sbd_perch_tx_o0 | High level |
| 53 | irq_ddrctl_awpoison_ch0 | High level | 270 | irq_gmac1_sbd_perch_tx_o1 | High level |
| 54 | irq_ddrctl_ecc_corrected_err_ch0 | High level | 271 | irq_pcie30x1_0_err | High level |

Rockchip Confidential

| Number | Source | Polarity | Number | Source | Polarity |
|---|---|---|---|---|---|
| 55 | irq_ddrctl_ecc_uncorrected_err_ch0 | High level | 272 | irq_pcie30x1_0_legacy | High level |
| 56 | irq_ddrctl_ecc_ap_err_ch0 | High level | 273 | irq_pcie30x1_0_msg_rx | High level |
| 57 | irq_ddrctl_rd_linkecc_uncorr_err_ch0 | High level | 274 | irq_pcie30x1_0_pmc | High level |
| 58 | irq_ddrctl_rd_linkecc_corr_err_ch0 | High level | 275 | irq_pcie30x1_0_sys | High level |
| 59 | irq_ddrctl_derate_temp_limit_ch0 | High level | 276 | irq_pcie30x1_1_err | High level |
| 60 | irq_ddrmon_ch0 | High level | 277 | irq_pcie30x1_1_legacy | High level |
| 61 | irq_ddrctl_sbr_done_ch1 | High level | 278 | irq_pcie30x1_1_msg_rx | High level |
| 62 | irq_ddrctl_arpoison_ch1 | High level | 279 | irq_pcie30x1_1_pmc | High level |
| 63 | irq_ddrctl_awpoison_ch1 | High level | 280 | irq_pcie30x1_1_sys | High level |
| 64 | irq_ddrctl_ecc_corrected_err_ch1 | High level | 281 | irq_pcie30x1_2_err | High level |
| 65 | irq_ddrctl_ecc_uncorrected_err_ch1 | High level | 282 | irq_pcie30x1_2_legacy | High level |
| 66 | irq_ddrctl_ecc_ap_err_ch1 | High level | 283 | irq_pcie30x1_2_msg_rx | High level |
| 67 | irq_ddrctl_rd_linkecc_uncorr_err_ch1 | High level | 284 | irq_pcie30x1_2_pmc | High level |
| 68 | irq_ddrctl_rd_linkecc_corr_err_ch1 | High level | 285 | irq_pcie30x1_2_sys | High level |
| 69 | irq_ddrctl_derate_temp_limit_ch1 | High level | 286 | irq_pcie30x2_err | High level |
| 70 | irq_ddrmon_ch1 | High level | 287 | irq_pcie30x2_legacy | High level |
| 71 | irq_ddrctl_sbr_done_ch2 | High level | 288 | irq_pcie30x2_msg_rx | High level |
| 72 | irq_ddrctl_arpoison_ch2 | High level | 289 | irq_pcie30x2_pmc | High level |
| 73 | irq_ddrctl_awpoison_ch2 | High level | 290 | irq_pcie30x2_sys | High level |
| 74 | irq_ddrctl_ecc_corrected_err_ch2 | High level | 291 | irq_pcie30x4_err | High level |
| 75 | irq_ddrctl_ecc_uncorrected_err_ch2 | High level | 292 | irq_pcie30x4_legacy | High level |
| 76 | irq_ddrctl_ecc_ap_err_ch2 | High level | 293 | irq_pcie30x4_msg_rx | High level |
| 77 | irq_ddrctl_rd_linkecc_uncorr_err_ch2 | High level | 294 | irq_pcie30x4_pmc | High level |
| 78 | irq_ddrctl_rd_linkecc_corr_err_ch2 | High level | 295 | irq_pcie30x4_sys | High level |
| 79 | irq_ddrctl_derate_temp_limit_ch2 | High level | 296 | irq_pcie30x1_0_pcie_dtim | High level |
| 80 | irq_ddrmon_ch2 | High level | 297 | irq_pcie30x1_1_pcie_dtim | High level |
| 81 | irq_ddrctl_sbr_done_ch3 | High level | 298 | irq_pcie30x1_2_pcie_dtim | High level |
| 82 | irq_ddrctl_arpoison_ch3 | High level | 299 | irq_pcie30x2_pcie_dtim | High level |
| 83 | irq_ddrctl_awpoison_ch3 | High level | 300 | irq_pcie30x4_pcie_dtim | High level |

Rockchip Confidential

| Number | Source | Polarity | Number | Source | Polarity |
|---|---|---|---|---|---|
| 84 | irq_ddrctl_ecc_corrected_err_ch3 | High level | 301 | irq_pcie30x4_pcie_edma_rd0 | High level |
| 85 | irq_ddrctl_ecc_uncorrected_err_ ch3 | High level | 302 | irq_pcie30x4_pcie_edma_rd1 | High level |
| 86 | irq_ddrctl_ecc_ap_err_ch3 | High level | 303 | irq_pcie30x4_pcie_edma_wr0 | High level |
| 87 | irq_ddrctl_rd_linkecc_uncorr_err_ch3 | High level | 304 | irq_pcie30x4_pcie_edma_wr1 | High level |
| 88 | irq_ddrctl_rd_linkecc_corr_err_ch3 | High level | 305 | irq_sata0 | High level |
| 89 | irq_ddrctl_derate_temp_limit_ch3 | High level | 306 | irq_sata1 | High level |
| 90 | irq_ddrmon_ch3 | High level | 307 | irq_sata2 | High level |
| 91 | irq_ahb2apb | High level | 308 | irq_grf_sdmmc_detectn | High level |
| 92 | irq_dma2ddr | High level | 309 | irq_gpio0 | High level |
| 93 | irq_mailbox0_ap0 | High level | 310 | irq_gpio1 | High level |
| 94 | irq_mailbox0_ap1 | High level | 311 | irq_gpio2 | High level |
| 95 | irq_mailbox0_ap2 | High level | 312 | irq_gpio3 | High level |
| 96 | irq_mailbox0_ap3 | High level | 313 | irq_gpio4 | High level |
| 97 | irq_mailbox0_bb0 | High level | 314 | irq_gpio0_exp | High level |
| 98 | irq_mailbox0_bb1 | High level | 315 | irq_gpio1_exp | High level |
| 99 | irq_mailbox0_bb2 | High level | 316 | irq_gpio2_exp | High level |
| 100 | irq_mailbox0_bb3 | High level | 317 | irq_gpio3_exp | High level |
| 101 | irq_mailbox1_ap0 | High level | 318 | irq_gpio4_exp | High level |
| 102 | irq_mailbox1_ap1 | High level | 319 | irq_pmutimer0 | High level |
| 103 | irq_mailbox1_ap2 | High level | 320 | irq_pmutimer1 | High level |
| 104 | irq_mailbox1_ap3 | High level | 321 | irq_timer0_ns | High level |
| 105 | irq_mailbox1_bb0 | High level | 322 | irq_timer1_ns | High level |
| 106 | irq_mailbox1_bb1 | High level | 323 | irq_timer2_ns | High level |
| 107 | irq_mailbox1_bb2 | High level | 324 | irq_timer3_ns | High level |
| 108 | irq_mailbox1_bb3 | High level | 325 | irq_timer4_ns | High level |
| 109 | irq_mailbox2_ap0 | High level | 326 | irq_timer5_ns | High level |
| 110 | irq_mailbox2_ap1 | High level | 327 | irq_timer6_ns | High level |
| 111 | irq_mailbox2_ap2 | High level | 328 | irq_timer7_ns | High level |
| 112 | irq_mailbox2_ap3 | High level | 329 | irq_timer8_ns | High level |
| 113 | irq_mailbox2_bb0 | High level | 330 | irq_timer9_ns | High level |
| 114 | irq_mailbox2_bb1 | High level | 331 | irq_timer10_ns | High level |
| 115 | irq_mailbox2_bb2 | High level | 332 | irq_timer11_ns | High level |
| 116 | irq_mailbox2_bb3 | High level | 333 | irq_stimer0 | High level |
| 117 | irq_decom | High level | 334 | irq_stimer1 | High level |
| 118 | irq_dmac0 | High level | 335 | irq_stimer2 | High level |
| 119 | irq_dmac0_abort | High level | 336 | irq_stimer3 | High level |
| 120 | irq_dmac1 | High level | 337 | irq_stimer4 | High level |
| 121 | irq_dmac1_abort | High level | 338 | irq_stimer5 | High level |

Rockchip Confidential

| Number | Source | Polarity | Number | Source | Polarity |
|---|---|---|---|---|---|
| 122 | irq_dmac2 | High level | 339 | irq_stimer6 | High level |
| 123 | irq_dmac2_abort | High level | 340 | irq_stimer7 | High level |
| 124 | irq_gpu_job | High level | 341 | irq_stimer8 | High level |
| 125 | irq_gpu_mmu | High level | 342 | irq_stimer9 | High level |
| 126 | irq_gpu_gpu | High level | 343 | irq_stimer10 | High level |
| 127 | irq_rkvdec0_dec | High level | 344 | irq_stimer11 | High level |
| 128 | irq_rkvdec0_mmu | High level | 345 | irq_hptimer | High level |
| 129 | irq_rkvdec1_dec | High level | 346 | irq_pmuwdt | High level |
| 130 | irq_rkvdec1_mmu | High level | 347 | irq_wdtns | High level |
| 131 | irq_rkvenc0_mmu0 | High level | 348 | irq_wdts | High level |
| 132 | irq_rkvenc0_mmu2 | High level | 349 | irq_i2c0 | High level |
| 133 | irq_rkvenc0 | High level | 350 | irq_i2c1 | High level |
| 134 | irq_rkvenc1_mmu0 | High level | 351 | irq_i2c2 | High level |
| 135 | irq_rkvenc1_mmu2 | High level | 352 | irq_i2c3 | High level |
| 136 | irq_rkvenc1 | High level | 353 | irq_i2c4 | High level |
| 137 | irq_rkvenc0 or irq_rkvenc1 | High level | 354 | irq_i2c5 | High level |
| 138 | irq_av1_afbc | High level | 355 | irq_i2c6 | High level |
| 139 | irq_av1_l2cache | High level | 356 | irq_i2c7 | High level |
| 140 | irq_av1_vcd | High level | 357 | irq_i2c8 | High level |
| 141 | irq_av1_mmu | High level | 358 | irq_spi0 | High level |
| 142 | irq_rknn_c0 | High level | 359 | irq_spi1 | High level |
| 143 | irq_rknn_c1 | High level | 360 | irq_spi2 | High level |
| 144 | irq_rknn_c2 | High level | 361 | irq_spi3 | High level |
| 145 | irq_vicap_mmu | High level | 362 | irq_spi4 | High level |
| 146 | irq_rga3_0 | High level | 363 | irq_uart0 | High level |
| 147 | irq_rga3_1 | High level | 364 | irq_uart1 | High level |
| 148 | irq_rga2 | High level | 365 | irq_uart2 | High level |
| 149 | irq_iep | High level | 366 | irq_uart3 | High level |
| 150 | irq_vdpu121_mmu | High level | 367 | irq_uart4 | High level |
| 151 | irq_vdpu121_xintdec | High level | 368 | irq_uart5 | High level |
| 152 | irq_vdpu121_xintenc | High level | 369 | irq_uart6 | High level |
| 153 | irq_jpegenc0_mmu | High level | 370 | irq_uart7 | High level |
| 154 | irq_jpegenc0_xintdec | High level | 371 | irq_uart8 | High level |
| 155 | irq_jpegenc1_mmu | High level | 372 | irq_uart9 | High level |
| 156 | irq_jpegenc1_xintdec | High level | 373 | irq_can0 | High level |
| 157 | irq_jpegenc2_mmu | High level | 374 | irq_can1 | High level |
| 158 | irq_jpegenc2_xintdec | High level | 375 | irq_can2 | High level |
| 159 | irq_jpegenc3_mmu | High level | 376 | irq_pwm0 | High level |
| 160 | irq_jpegenc3_xintdec | High level | 377 | irq_pwm0_pwr | High level |
| 161 | irq_jpegdec_dec | High level | 378 | irq_pwm1 | High level |
| 162 | irq_jpegdec_mmu | High level | 379 | irq_pwm1_pwr | High level |
| 163 | irq_isp0 | High level | 380 | irq_pwm2 | High level |
| 164 | irq_isp0_mmu | High level | 381 | irq_pwm2_pwr | High level |
| 165 | irq_isp0_mi | High level | 382 | irq_pwm3 | High level |

Rockchip Confidential

| Number | Source | Polarity | Number | Source | Polarity |
|---|---|---|---|---|---|
| 166 | irq_isp0_mipi | High level | 383 | irq_pwm3_pwr | High level |
| 167 | irq_isp1 | High level | 384 | irq_pmu_pvtm | High level |
| 168 | irq_isp1_mmu | High level | 385 | irq_litcore_pvtm | High level |
| 169 | irq_isp1_mi | High level | 386 | irq_bigcore0_pvtm | High level |
| 170 | irq_isp1_mipi | High level | 387 | irq_bigcore1_pvtm | High level |
| 171 | irq_fec0 | High level | 388 | irq_npu_pvtm | High level |
| 172 | irq_fec0_ispp_mmu1 | High level | 389 | irq_gpu_pvtm | High level |
| 173 | irq_fec1 | High level | 390 | irq_npumcu_cache | High level |
| 174 | irq_fec1_ispp_mmu1 | High level | 391 | irq_pmumcu_cache | High level |
| 175 | irq_csihost0_1 | High level | 392 | irq_hdmitx0_hpd | High level |
| 176 | irq_csihost0_2 | High level | 393 | irq_hdmitx1_hpd | High level |
| 177 | irq_csihost1_1 | High level | 394 | irq_pcie_mmu600_r2_tbu0_pmu_irpt | High level |
| 178 | irq_csihost1_2 | High level | 395 | irq_pcie_mmu600_r2_tbu0_ras_irpt | High level |
| 179 | irq_csihost2_1 | High level | 396 | irq_pcie_mmu600_r2_tbu1_pmu_irpt | High level |
| 180 | irq_csihost2_2 | High level | 397 | irq_pcie_mmu600_r2_tbu1_ras_irpt | High level |
| 181 | irq_csihost3_1 | High level | 398 | irq_pcie_mmu600_r2_tcu_evento | High level |
| 182 | irq_csihost3_2 | High level | 399 | irq_pcie_mmu600_r2_tcu_cmd_sync_irpt_ns | High level |
| 183 | irq_csihost4_1 | High level | 400 | irq_pcie_mmu600_r2_tcu_cmd_sync_irpt_s | High level |
| 184 | irq_csihost4_2 | High level | 401 | irq_pcie_mmu600_r2_tcu_event_q_irpt_ns | High level |
| 185 | irq_csihost5_1 | High level | 402 | irq_pcie_mmu600_r2_tcu_event_q_irpt_s | High level |
| 186 | irq_csihost5_2 | High level | 403 | irq_pcie_mmu600_r2_tcu_global_irpt_ns | High level |
| 187 | irq_vicap | High level | 404 | irq_pcie_mmu600_r2_tcu_global_irpt_s | High level |
| 188 | irq_vop | High level | 405 | irq_pcie_mmu600_r2_tcu_pmu_irpt | High level |
| 189 | irq_vop_ddr | High level | 406 | irq_pcie_mmu600_r2_tcu_pri_q_irpt_ns | High level |
| 190 | irq_vop_lb | High level | 407 | irq_pcie_mmu600_r2_tcu_ras_irpt | High level |
| 191 | irq_hdcp0 | High level | 408 | irq_php_mmu600_r2_tbu0_pmu_irpt | High level |
| 192 | irq_hdcp1 | High level | 409 | irq_php_mmu600_r2_tbu0_ras_irpt | High level |
| 193 | irq_dp0 | High level | 410 | irq_php_mmu600_r2_tcu_evento | High level |

Rockchip Confidential

| Number | Source | Polarity | Number | Source | Polarity |
|---|---|---|---|---|---|
| 194 | irq_dp1 | High level | 411 | irq_php_mmu600_r2_tcu_cmd_sync_irpt_ns | High level |
| 195 | irq_edp0 | High level | 412 | irq_php_mmu600_r2_tcu_cmd_sync_irpt_s | High level |
| 196 | irq_edp1 | High level | 413 | irq_php_mmu600_r2_tcu_event_q_irpt_ns | High level |
| 197 | irq_vo_trng0 | High level | 414 | irq_php_mmu600_r2_tcu_event_q_irpt_s | High level |
| 198 | irq_vo_trng1 | High level | 415 | irq_php_mmu600_r2_tcu_global_irpt_ns | High level |
| 199 | irq_dsihost0 | High level | 416 | irq_php_mmu600_r2_tcu_global_irpt_s | High level |
| 200 | irq_dsihost1 | High level | 417 | irq_php_mmu600_r2_tcu_pmu_irpt | High level |
| 201 | irq_hdmitx0_oavp | High level | 418 | irq_php_mmu600_r2_tcu_pri_q_irpt_ns | High level |
| 202 | irq_hdmitx0_ocec | High level | 419 | irq_php_mmu600_r2_tcu_ras_irpt | High level |
| 203 | irq_hdmitx0_oearcrx | High level | 420 | irq_gic_fault | High level |
| 204 | irq_hdmitx0_omain | High level | 421 | irq_gic_err | High level |
| 205 | irq_hdmitx1_oavp | High level | 422 | irq_gic_pmu | High level |
| 206 | irq_hdmitx1_ocec | High level | 423 | irq_usb2host0phy_grf | High level |
| 207 | irq_hdmitx1_oearcrx | High level | 424 | irq_usb2host1phy_grf | High level |
| 208 | irq_hdmitx1_omain | High level | 425 | irq_otg0phy_grf | High level |
| 209 | irq_hdmirx_cec | High level | 426 | irq_otg1phy_grf | High level |
| 210 | irq_hdmirx_hdmi | High level | 427 | irq_otg2_lfps_beacon | High level |
| 211 | irq_hdmirx_dma | High level | 428 | irq_pmic | High level |
| 212 | irq_i2s0_8ch | High level | 429 | irq_tsadc | High level |
| 213 | irq_i2s1_8ch | High level | 430 | irq_saradc | High level |
| 214 | irq_i2s2_2ch | High level | 431 | irq_trng_s | High level |
| 215 | irq_i2s3_2ch | High level | 432 | irq_trng_ns | High level |
| 216 | irq_i2s4_8ch | High level | 433 | irq_wdt_ddr | High level |
| 217 | irq_i2s5_8ch | High level | 434 | irq_timer0_ddr | High level |
| 218 | irq_i2s6_8ch | High level | 435 | irq_timer1_ddr | High level |
| 219 | irq_i2s7_8ch | High level | 436 | irq_timer0_npu | High level |
| 220 | irq_i2s8_8ch | High level | 437 | irq_timer1_npu | High level |
| 221 | irq_i2s9_8ch | High level | 438 | irq_wdt_npu | High level |
| 222 | irq_i2s10_8ch | High level | 439 | irq_dsu_probe0_mainstat alarm | High level |
| 223 | irq_pdm0 | High level | 440 | irq_dsu_probe1_mainstat alarm | High level |
| 224 | irq_pdm1 | High level | 441 | irq_dsu_probe2_mainstat alarm | High level |

Rockchip Confidential

| Number | Source | Polarity | Number | Source | Polarity |
|---|---|---|---|---|---|
| 225 | irq_spdiftx0 | High level | 442 | irq_dsu_probe3_mainstatalarm | High level |
| 226 | irq_spdiftx1 | High level | 443 | irq_center_probep0n0_mainstatalarm | High level |
| 227 | irq_spdiftx2 | High level | 444 | irq_center_probep0n1_mainstatalarm | High level |
| 228 | irq_spdiftx3 | High level | 445 | irq_center_probep1n0_mainstatalarm | High level |
| 229 | irq_spdiftx4 | High level | 446 | irq_center_probep1n1_mainstatalarm | High level |
| 230 | irq_spdif5 | High level | 447 | irq_center_probep2n0_mainstatalarm | High level |
| 231 | irq_spdifrx0 | High level | 448 | irq_center_probep2n1_mainstatalarm | High level |
| 232 | irq_spdifrx1 | High level | 449 | irq_center_probep3n0_mainstatalarm | High level |
| 233 | irq_spdifrx2 | High level | 450 | irq_center_probep3n1_mainstatalarm | High level |
| 234 | irq_vad | High level | 451 | irq_sgrf_crc_chk_rst_req | High level |
| 235 | irq_sdmmc | High level | 452 | irq_dsusgrf_crc_chk_rst_req | High level |
| 236 | irq_sdio | High level | 453 | irq_pmusgrf_crc_chk_rst_req | High level |
| 237 | irq_emmc | High level | 454~511 | Reserved | High level |

## 1.4 System DMA Hardware Request Connection

RK3588 provides three DMA controller (DMAC) inside the system, the following tables are the DMA hardware request list.

Table 1-4 RK3588 DMAC Hardware Request Connection List

| DMAC0 | | | DMAC1 | | | DMAC2 | | |
|---|---|---|---|---|---|---|---|---|
| Req Number | Source | Polarity | Req Number | Source | Polarity | Req Number | Source | Polarity |
| 0 | I2S0_8ch_tx | High level | 0 | I2S2_2ch_tx | High level | 0 | I2S4_8ch_tx | High level |
| 1 | I2S0_8ch_rx | High level | 1 | I2S2_2ch_rx | High level | 1 | Reserved | High level |
| 2 | I2S1_8ch_tx | High level | 2 | I2S3_2ch_tx | High level | 2 | I2S5_8ch_tx | High level |
| 3 | I2S1_8ch_rx | High level | 3 | I2S3_2ch_rx | High level | 3 | Reserved | High level |
| 4 | PDM0 | High level | 4 | PDM1 | High level | 4 | I2S6_8ch_tx | High level |
| 5 | SPDIF_tx0 | High level | 5 | SPDIF_tx1 | High level | 5 | Reserved | High level |
| 6 | UART0_tx | High level | 6 | SPDIF_tx2 | High level | 6 | Reserved | High level |
| 7 | UART0_rx | High level | 7 | SPDIF_tx3 | High level | 7 | UART7_tx | High level |
| 8 | UART1_tx | High level | 8 | SPDIF_tx4 | High level | 8 | UART7_rx | High level |
| 9 | UART1_rx | High level | 9 | UART4_tx | High level | 9 | UART8_tx | High level |
| 10 | UART2_tx | High level | 10 | UART4_rx | High level | 10 | UART8_rx | High level |
| 11 | UART2_rx | High level | 11 | UART5_tx | High level | 11 | UART9_tx | High level |

Rockchip Confidential

| DMAC0 | | | DMAC1 | | | DMAC2 | | |
|---|---|---|---|---|---|---|---|---|
| Req Number | Source | Polarity | Req Number | Source | Polarity | Req Number | Source | Polarity |
| 12 | UART3_tx | High level | 12 | UART5_rx | High level | 12 | UART9_rx | High level |
| 13 | UART3_rx | High level | 13 | UART6_tx | High level | 13 | SPI4_tx | High level |
| 14 | SPI0_tx | High level | 14 | UART6_rx | High level | 14 | SPI4_rx | High level |
| 15 | SPI0_rx | High level | 15 | SPI2_tx | High level | 15 | PWM2 | High level |
| 16 | SPI1_tx | High level | 16 | SPI2_rx | High level | 16 | PWM3 | High level |
| 17 | SPI1_rx | High level | 17 | SPI3_tx | High level | 17 | CAN2_tx | High level |
| 18 | PWM0 | High level | 18 | SPI3_rx | High level | 18 | CAN2_rx | High level |
| 19 | CAN0_tx | High level | 19 | PWM1 | High level | 19 | sdmmc_buffer | High level |
| 20 | CAN0_rx | High level | 20 | CAN1_tx | High level | 20 | Reserved | High level |
| 21 | SPDIF_rx0 | High level | 21 | CAN1_rx | High level | 21 | I2S7_8ch_rx | High level |
| 22 | SPDIF_rx1 | High level | 22 | SPDIF_tx5 | High level | 22 | I2S8_8ch_tx | High level |
| 23 | SPDIF_rx2 | High level | 23 | Reserved | High level | 23 | I2S9_8ch_rx | High level |
| 24 | Reserved | High level | 24 | Reserved | High level | 24 | I2S10_8ch_rx | High level |

Rockchip Confidential

Copyright 2022 © Rockchip Electronics Co., Ltd. 

# Chapter 2 CRU

## 2.1 Overview

The CRU is an APB slave module that is designed for generating all of the internal and system clocks, resets in the chip. CRU generates system clocks from PLL output clock or external clock source, and generates system reset from external power-on-reset, watchdog timer reset or software reset or temperature sensor.
The CRU is located at several addresses.

| | Description | Base Address |
|---|---|---|
| CRU | Used for always on system. | 0xFD7C0000 |
| PHPTOPCRU | Used for php system. | 0xFD7C8000 |
| SECURECRU | Used for secure system. | 0xFD7D0000 |
| SBUSCRU | Used for secure bus system. | 0xFD7D8000 |
| PMU1SCRU | Used for secure pmu system. | 0xFD7E0000 |
| PMU1CRU | Used for pmu system. | 0xFD7F0000 |
| DDR0CRU | Used for DDR0 phy. | 0xFD800000 |
| DDR1CRU | Used for DDR1 phy. | 0xFD804000 |
| DDR2CRU | Used for DDR2 phy. | 0xFD808000 |
| DDR3CRU | Used for DDR3 phy. | 0xFD80C000 |
| BIGCORE0CRU | Used for pd bigcore0 system. | 0xFD810000 |
| BIGCORE1CRU | Used for pd bigcore1 system. | 0xFD812000 |
| DSUCRU | Used for pd dsu system. | 0xFD818000 |

The CRU supports the following features:

- Compliance with AMBA APB interface
- Embedded with 5 fractional PLLs, 5 integer PLLs and 8 DDRPLLs in different CRUs
- Flexible selection of clock source
- Support dividing clock separately
- Support gating clock separately
- Support software reset each module separately

| PLL TYPE / PD | FRACPLL | DDRPLL | INTPLL |
|---|---|---|---|
| CRU | V0PLL,AUPLL,CPLL,GPLL | | NPLL |
| BIGCORE0CRU | | | B0PLL |
| BIGCORE1CRU | | | B1PLL |
| DSUCRU | | | LPLL |
| SBUSCRU | | | SPLL |
| DDR0CRU | | D0APLL,D0BPLL | |
| DDR1CRU | | D1APLL,D1BPLL | |
| DDR2CRU | | D2APLL,D2BPLL | |
| DDR3CRU | | D3APLL,D3BPLL | |
| PHPTOPCRU | PPLL | | |

## 2.2 Block Diagram

The CRU comprises with:

- PLL
- Register configuration unit

Rockchip Confidential

- Clock generate unit
- Reset generate unit

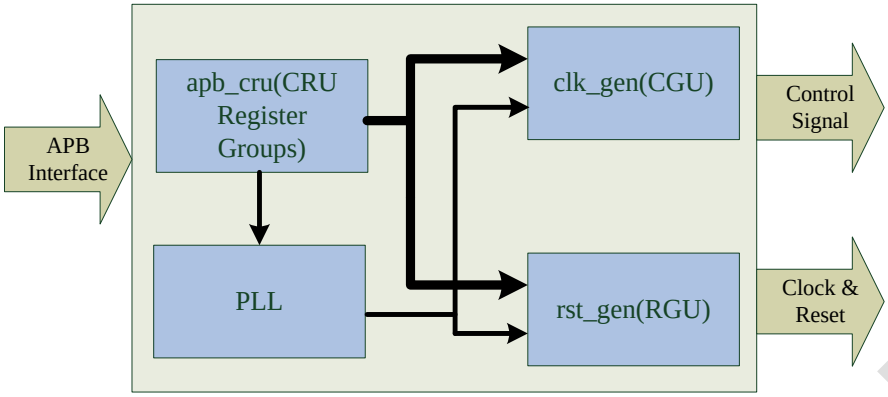



Fig. 2-1 CRU Block Diagram

## 2.3 Function Description

### 2.3.1 System Clock Solution

All R3588 PLLs receive 24MHz oscillator as input reference clock.
NPLL/GPLL/V0PLL/AUPLL/CPLL/SPLL can be set to three work modes: normal mode, slow mode and deep slow mode. When power on or changing PLL setting, we must program PLL into slow mode or deep slow mode.
To maximize the flexibility, some of clocks can select divider source from multiple PLLs.To provide some specific frequency, another solution is integrated: fractional divider. Divfree50 divider and divfree NP5 divider are also provided for some modules.All clocks can be gated by software.
The basic units for clock generation are:

- Gating
- MUX(multiplexer)
- Divfree(Glitch free divider)
  - clk_out_freq=clk_in_freq/divisor
  - When divisor is even, the clock duty cycle of clk_out is 50%
  - When divisor is odd, the clock duty cycle of clk_out is not 50%
- Fracdiv(Fractional divider)
  - clk_out_freq=clk_in_freq*numerator/denominator, both numerator and denominator are 16 bits
- Divfree50(Glitch free divider for duty cycle 50%)
  - clk_out_freq=clk_in_freq/divisor
  - When divisor is even or odd, the clock duty cycle of clk_out is 50%
- DivFreeNP5(Glitch free divider for null point 5)
  - clk_out_freq= 2*clk_in_freq/(2*div_con+3)
  - The clock duty cycle of clk_out is not 50%

The settings of all basic units are controlled by CRU registers.

### 2.3.2 System Reset Solution

Almost all module have these reset source as the following figure shows. The ‘xxx’ in the figure is the module name.

Rockchip Confidential

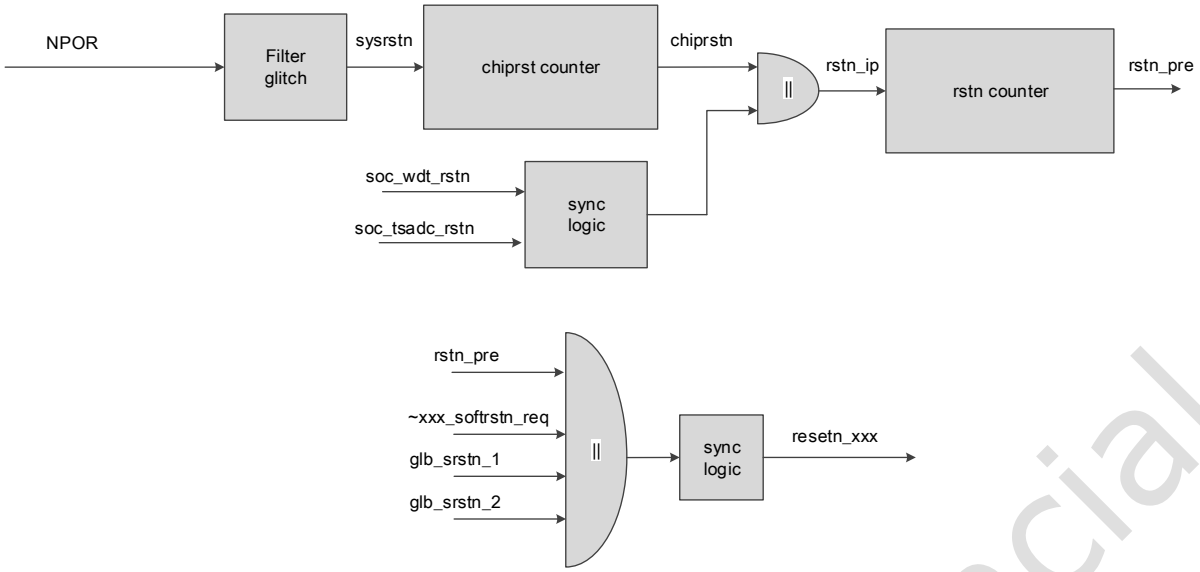



Fig. 2-2 Reset Architecture Diagram

Reset source of each reset signal includes:

- NPOR: External power on reset
- soc_wdt_rstn: Reset from WDT module
- soc_tsadc_rstn: Reset from TSADC module
- softrstn_req: Software reset request by programming CRU_SOFTRST_CON
- glb_srstn_1: First global software reset by programming CRU_GLB_SRST_FST as 0xfdb9
- glb_srstn_2: Second global software reset by programming CRU_GLB_SRST_SND as 0xeca8

### 2.3.3 PLL Introduction

PLL is a 1.8V/0.75V dual supply-voltage phase locked loop (PLL) with a wide-output-frequency-range for frequency synthesis.

| | FRACPLL | | DDRPLL | | INTPLL | |
|---|---|---|---|---|---|---|
| Parameter | MIN | MAX | MIN | MAX | MIN | MAX |
| Fin | 4.5 | 300 | 6 | 300 | 4.5 | 300 |
| p | 1 | 63 | 1 | 63 | 1 | 63 |
| m | 64 | 1023 | 64 | 1023 | 64 | 1023 |
| s | 0 | 6 | 0 | 6 | 0 | 6 |
| Fref(MHz)=Fin/p | 6 | 30 | 6 | 30 | 4.5 | 12 |
| Fvco(MHz)=(m*Fref)/p | 2250 | 4500 | 3300 | 6600 | 2250 | 4500 |
| Fout(MHz) | 35.2 | 4500 | 51.6 | 6600 | 35.2 | 4500 |
| Duty cycle | 48~52% | | 45~55% | | 47~53% | |
| Input Period Jitter | ±200ps | | ±200ps | | ±200ps | |
| PLL Period Jitter(Tjp) | Fvco<3G:±2% of Tfvco | | Fvco<3G:±2% of Tfvco | | Fvco<3G:±1.5% of Tfvco | |
| | Fvco>3G:±1% of Tfvco | | Fvco>3G:±1% of Tfvco | | Fvco>3G:±0.75% of Tfvco | |
| Lock Time(Fin/p cycles) | - | 500 | - | 500 | - | 150 |
| Modulation Method | up/down/center | | up/down/center | | - | |

# 2.3.3.1 FRACPLL Introduction

FRACPLL block diagram is shown below.

Rockchip Confidencial

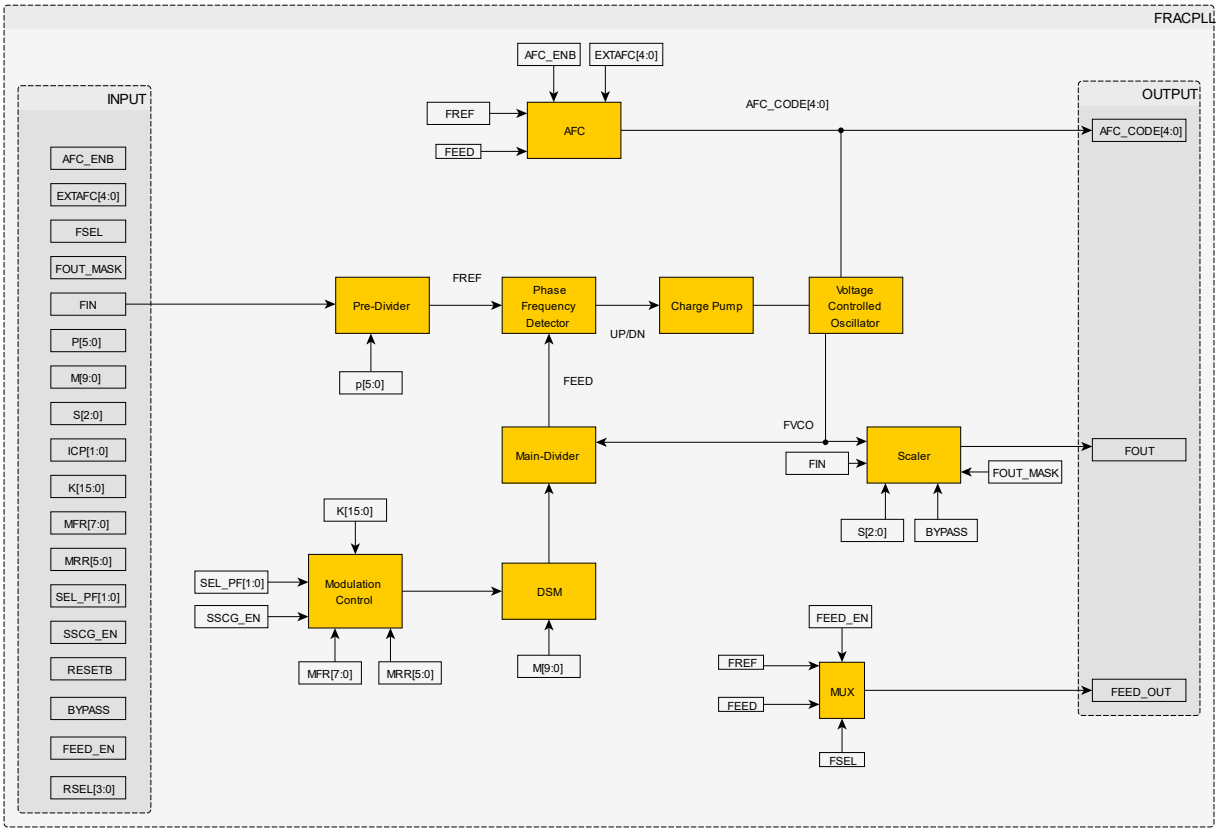



Fig. 2-3 FRACPLL Block Diagram

## 2.3.3.2 INTPLL Introduction

INTPLL block diagram is shown below.

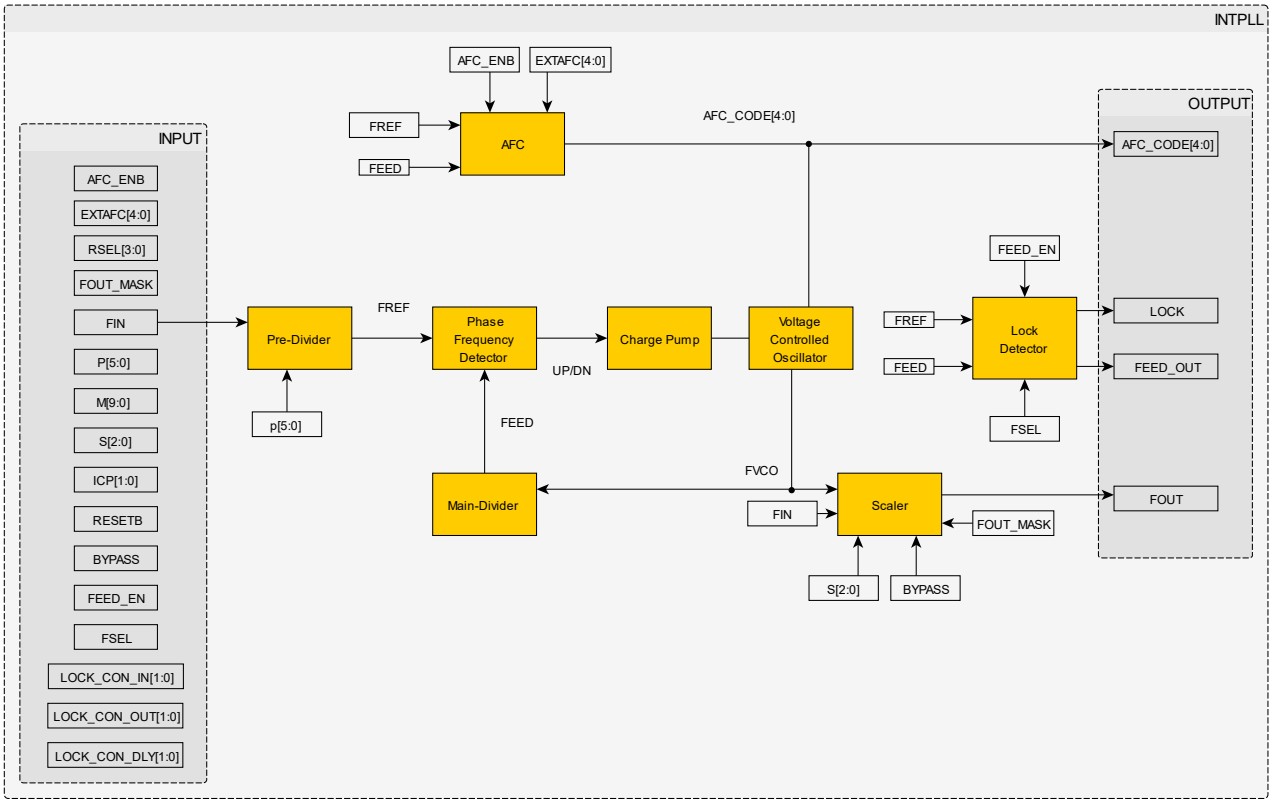



Fig. 2-4 INTPLL Block Diagram

# 2.3.3.3 DDRPLL Introduction

DDRPLL block diagram is shown below.

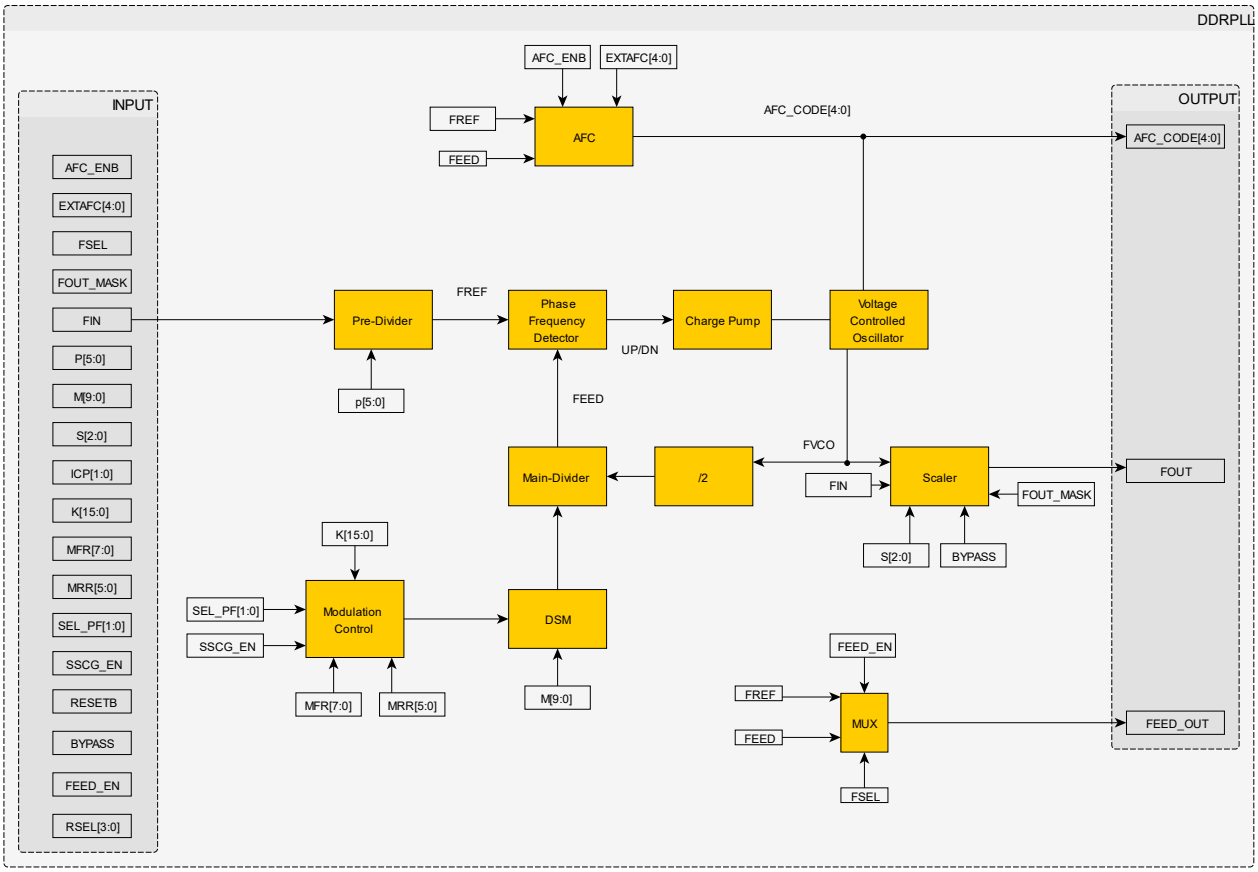



Fig. 2-5 DDRPLL Block Diagram

## 2.4 CRU Register Description

There are 2 groups of DDR, named ddr01 or ddr_*_ch01(including DDR CH0 and DDR CH1), ddr23 or ddr_*_ch23(including DDR CH2 and DDR CH3).

### 2.4.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CRU_V0PLL_CON0 | 0x0160 | W | 0x00000000 | V0PLL configuration register 0 |
| CRU_V0PLL_CON1 | 0x0164 | W | 0x00000000 | V0PLL configuration register 1 |
| CRU_V0PLL_CON2 | 0x0168 | W | 0x00000000 | V0PLL configuration register 2 |
| CRU_V0PLL_CON3 | 0x016C | W | 0x00000000 | V0PLL configuration register 3 |
| CRU_V0PLL_CON4 | 0x0170 | W | 0x00000000 | V0PLL configuration register 4 |
| CRU_V0PLL_CON5 | 0x0174 | W | 0x00000000 | V0PLL configuration register 5 |
| CRU_V0PLL_CON6 | 0x0178 | W | 0x00000000 | V0PLL configuration register 6 |
| CRU_AUPLL_CON0 | 0x0180 | W | 0x00000000 | AUPLL configuration register 0 |
| CRU_AUPLL_CON1 | 0x0184 | W | 0x00000000 | AUPLL configuration register 1 |
| CRU_AUPLL_CON2 | 0x0188 | W | 0x00000000 | AUPLL configuration register 2 |
| CRU_AUPLL_CON3 | 0x018C | W | 0x00000000 | AUPLL configuration register 3 |
| CRU_AUPLL_CON4 | 0x0190 | W | 0x00000000 | AUPLL configuration register 4 |
| CRU_AUPLL_CON5 | 0x0194 | W | 0x00000000 | AUPLL configuration register 5 |
| CRU_AUPLL_CON6 | 0x0198 | W | 0x00000000 | AUPLL configuration register 6 |
| CRU_CPLL_CON0 | 0x01A0 | W | 0x00000000 | CPLL configuration register 0 |
| CRU_CPLL_CON1 | 0x01A4 | W | 0x00000000 | CPLL configuration register 1 |
| CRU_CPLL_CON2 | 0x01A8 | W | 0x00000000 | CPLL configuration register 2 |

Rockchip C

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CRU_CPLL_CON3 | 0x01AC | W | 0x00000000 | CPLL configuration register 3 |
| CRU_CPLL_CON4 | 0x01B0 | W | 0x00000000 | CPLL configuration register 4 |
| CRU_CPLL_CON5 | 0x01B4 | W | 0x00000000 | CPLL configuration register 5 |
| CRU_CPLL_CON6 | 0x01B8 | W | 0x00000000 | CPLL configuration register 6 |
| CRU_GPLL_CON0 | 0x01C0 | W | 0x00000000 | GPLL configuration register 0 |
| CRU_GPLL_CON1 | 0x01C4 | W | 0x00000000 | GPLL configuration register 1 |
| CRU_GPLL_CON2 | 0x01C8 | W | 0x00000000 | GPLL configuration register 2 |
| CRU_GPLL_CON3 | 0x01CC | W | 0x00000000 | GPLL configuration register 3 |
| CRU_GPLL_CON4 | 0x01D0 | W | 0x00000000 | GPLL configuration register 4 |
| CRU_GPLL_CON5 | 0x01D4 | W | 0x00000000 | GPLL configuration register 5 |
| CRU_GPLL_CON6 | 0x01D8 | W | 0x00000000 | GPLL configuration register 6 |
| CRU_NPLL_CON0 | 0x01E0 | W | 0x00000000 | NPLL configuration register 0 |
| CRU_NPLL_CON1 | 0x01E4 | W | 0x00000000 | NPLL configuration register 1 |
| CRU_NPLL_CON4 | 0x01F0 | W | 0x00000002 | NPLL configuration register 4 |
| CRU_NPLL_CON5 | 0x01F4 | W | 0x000007E0 | NPLL configuration register 5 |
| CRU_NPLL_CON6 | 0x01F8 | W | 0x00000000 | NPLL configuration register 6 |
| CRU_MODE_CON00 | 0x0280 | W | 0x00000000 | Internal PLL mode select register 0 |
| CRU_CLKSEL_CON00 | 0x0300 | W | 0x00000BBD | Internal clock select and division register 0 |
| CRU_CLKSEL_CON01 | 0x0304 | W | 0x00000169 | Internal clock select and division register 1 |
| CRU_CLKSEL_CON02 | 0x0308 | W | 0x00000925 | Internal clock select and division register 2 |
| CRU_CLKSEL_CON03 | 0x030C | W | 0x000000A1 | Internal clock select and division register 3 |
| CRU_CLKSEL_CON04 | 0x0310 | W | 0x00000881 | Internal clock select and division register 4 |
| CRU_CLKSEL_CON05 | 0x0314 | W | 0x00000881 | Internal clock select and division register 5 |
| CRU_CLKSEL_CON06 | 0x0318 | W | 0x00000820 | Internal clock select and division register 6 |
| CRU_CLKSEL_CON07 | 0x031C | W | 0x00000020 | Internal clock select and division register 7 |
| CRU_CLKSEL_CON08 | 0x0320 | W | 0x00000421 | Internal clock select and division register 8 |
| CRU_CLKSEL_CON09 | 0x0324 | W | 0x00000000 | Internal clock select and division register 9 |
| CRU_CLKSEL_CON10 | 0x0328 | W | 0x000030FF | Internal clock select and division register 10 |
| CRU_CLKSEL_CON15 | 0x033C | W | 0x0000BB9D | Internal clock select and division register 15 |
| CRU_CLKSEL_CON16 | 0x0340 | W | 0x000000BB | Internal clock select and division register 16 |
| CRU_CLKSEL_CON17 | 0x0344 | W | 0x00000200 | Internal clock select and division register 17 |
| CRU_CLKSEL_CON18 | 0x0348 | W | 0x00000000 | Internal clock select and division register 18 |
| CRU_CLKSEL_CON19 | 0x034C | W | 0x00000000 | Internal clock select and division register 19 |
| CRU_CLKSEL_CON20 | 0x0350 | W | 0x00000000 | Internal clock select and division register 20 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CRU_CLKSEL_CON21 | 0x0354 | W | 0x00000000 | Internal clock select and division register 21 |
| CRU_CLKSEL_CON22 | 0x0358 | W | 0x00000000 | Internal clock select and division register 22 |
| CRU_CLKSEL_CON24 | 0x0360 | W | 0x00000010 | Internal clock select and division register 24 |
| CRU_CLKSEL_CON25 | 0x0364 | W | 0x03355460 | Internal clock select and division register 25 |
| CRU_CLKSEL_CON26 | 0x0368 | W | 0x00000007 | Internal clock select and division register 26 |
| CRU_CLKSEL_CON27 | 0x036C | W | 0x03355460 | Internal clock select and division register 27 |
| CRU_CLKSEL_CON28 | 0x0370 | W | 0x0000001B | Internal clock select and division register 28 |
| CRU_CLKSEL_CON29 | 0x0374 | W | 0x03355460 | Internal clock select and division register 29 |
| CRU_CLKSEL_CON30 | 0x0378 | W | 0x0000000F | Internal clock select and division register 30 |
| CRU_CLKSEL_CON31 | 0x037C | W | 0x03355460 | Internal clock select and division register 31 |
| CRU_CLKSEL_CON32 | 0x0380 | W | 0x0000000F | Internal clock select and division register 32 |
| CRU_CLKSEL_CON33 | 0x0384 | W | 0x03355460 | Internal clock select and division register 33 |
| CRU_CLKSEL_CON34 | 0x0388 | W | 0x00000006 | Internal clock select and division register 34 |
| CRU_CLKSEL_CON35 | 0x038C | W | 0x03355460 | Internal clock select and division register 35 |
| CRU_CLKSEL_CON36 | 0x0390 | W | 0x00000092 | Internal clock select and division register 36 |
| CRU_CLKSEL_CON38 | 0x0398 | W | 0x00000023 | Internal clock select and division register 38 |
| CRU_CLKSEL_CON39 | 0x039C | W | 0x000002CB | Internal clock select and division register 39 |
| CRU_CLKSEL_CON40 | 0x03A0 | W | 0x00000ECB | Internal clock select and division register 40 |
| CRU_CLKSEL_CON41 | 0x03A4 | W | 0x0000030B | Internal clock select and division register 41 |
| CRU_CLKSEL_CON42 | 0x03A8 | W | 0x001403DE | Internal clock select and division register 42 |
| CRU_CLKSEL_CON43 | 0x03AC | W | 0x00000006 | Internal clock select and division register 43 |
| CRU_CLKSEL_CON44 | 0x03B0 | W | 0x001403DE | Internal clock select and division register 44 |
| CRU_CLKSEL_CON45 | 0x03B4 | W | 0x00000006 | Internal clock select and division register 45 |
| CRU_CLKSEL_CON46 | 0x03B8 | W | 0x001403DE | Internal clock select and division register 46 |
| CRU_CLKSEL_CON47 | 0x03BC | W | 0x00000006 | Internal clock select and division register 47 |
| CRU_CLKSEL_CON48 | 0x03C0 | W | 0x001403DE | Internal clock select and division register 48 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CRU_CLKSEL_CON49 | 0x03C4 | W | 0x00000006 | Internal clock select and division register 49 |
| CRU_CLKSEL_CON50 | 0x03C8 | W | 0x001403DE | Internal clock select and division register 50 |
| CRU_CLKSEL_CON51 | 0x03CC | W | 0x00000006 | Internal clock select and division register 51 |
| CRU_CLKSEL_CON52 | 0x03D0 | W | 0x001403DE | Internal clock select and division register 52 |
| CRU_CLKSEL_CON53 | 0x03D4 | W | 0x00000006 | Internal clock select and division register 53 |
| CRU_CLKSEL_CON54 | 0x03D8 | W | 0x001403DE | Internal clock select and division register 54 |
| CRU_CLKSEL_CON55 | 0x03DC | W | 0x00000006 | Internal clock select and division register 55 |
| CRU_CLKSEL_CON56 | 0x03E0 | W | 0x001403DE | Internal clock select and division register 56 |
| CRU_CLKSEL_CON57 | 0x03E4 | W | 0x00000006 | Internal clock select and division register 57 |
| CRU_CLKSEL_CON58 | 0x03E8 | W | 0x001403DE | Internal clock select and division register 58 |
| CRU_CLKSEL_CON59 | 0x03EC | W | 0x0000A002 | Internal clock select and division register 59 |
| CRU_CLKSEL_CON60 | 0x03F0 | W | 0x0000020A | Internal clock select and division register 60 |
| CRU_CLKSEL_CON61 | 0x03F4 | W | 0x00000041 | Internal clock select and division register 61 |
| CRU_CLKSEL_CON62 | 0x03F8 | W | 0x000003E1 | Internal clock select and division register 62 |
| CRU_CLKSEL_CON63 | 0x03FC | W | 0x0000003F | Internal clock select and division register 63 |
| CRU_CLKSEL_CON65 | 0x0404 | W | 0x0000003F | Internal clock select and division register 65 |
| CRU_CLKSEL_CON67 | 0x040C | W | 0x0000C021 | Internal clock select and division register 67 |
| CRU_CLKSEL_CON73 | 0x0424 | W | 0x00007C84 | Internal clock select and division register 73 |
| CRU_CLKSEL_CON74 | 0x0428 | W | 0x00001010 | Internal clock select and division register 74 |
| CRU_CLKSEL_CON77 | 0x0434 | W | 0x00000590 | Internal clock select and division register 77 |
| CRU_CLKSEL_CON78 | 0x0438 | W | 0x00000164 | Internal clock select and division register 78 |
| CRU_CLKSEL_CON80 | 0x0440 | W | 0x00000288 | Internal clock select and division register 80 |
| CRU_CLKSEL_CON81 | 0x0444 | W | 0x0000070E | Internal clock select and division register 81 |
| CRU_CLKSEL_CON82 | 0x0448 | W | 0x00009D9D | Internal clock select and division register 82 |
| CRU_CLKSEL_CON83 | 0x044C | W | 0x00008B9D | Internal clock select and division register 83 |
| CRU_CLKSEL_CON84 | 0x0450 | W | 0x0000049D | Internal clock select and division register 84 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CRU_CLKSEL_CON85 | 0x0454 | W | 0x00000000 | Internal clock select and division register 85 |
| CRU_CLKSEL_CON89 | 0x0464 | W | 0x00008100 | Internal clock select and division register 89 |
| CRU_CLKSEL_CON90 | 0x0468 | W | 0x00001801 | Internal clock select and division register 90 |
| CRU_CLKSEL_CON91 | 0x046C | W | 0x00000001 | Internal clock select and division register 91 |
| CRU_CLKSEL_CON93 | 0x0474 | W | 0x00000300 | Internal clock select and division register 93 |
| CRU_CLKSEL_CON94 | 0x0478 | W | 0x000000E0 | Internal clock select and division register 94 |
| CRU_CLKSEL_CON96 | 0x0480 | W | 0x00000024 | Internal clock select and division register 96 |
| CRU_CLKSEL_CON98 | 0x0488 | W | 0x00000021 | Internal clock select and division register 98 |
| CRU_CLKSEL_CON99 | 0x048C | W | 0x00000160 | Internal clock select and division register 99 |
| CRU_CLKSEL_CON100 | 0x0490 | W | 0x00002121 | Internal clock select and division register 100 |
| CRU_CLKSEL_CON102 | 0x0498 | W | 0x00008088 | Internal clock select and division register 102 |
| CRU_CLKSEL_CON104 | 0x04A0 | W | 0x00008088 | Internal clock select and division register 104 |
| CRU_CLKSEL_CON106 | 0x04A8 | W | 0x00000021 | Internal clock select and division register 106 |
| CRU_CLKSEL_CON107 | 0x04AC | W | 0x00001801 | Internal clock select and division register 107 |
| CRU_CLKSEL_CON108 | 0x04B0 | W | 0x00003060 | Internal clock select and division register 108 |
| CRU_CLKSEL_CON110 | 0x04B8 | W | 0x00000040 | Internal clock select and division register 110 |
| CRU_CLKSEL_CON111 | 0x04BC | W | 0x00000201 | Internal clock select and division register 111 |
| CRU_CLKSEL_CON112 | 0x04C0 | W | 0x00000001 | Internal clock select and division register 112 |
| CRU_CLKSEL_CON113 | 0x04C4 | W | 0x00000005 | Internal clock select and division register 113 |
| CRU_CLKSEL_CON114 | 0x04C8 | W | 0x00000181 | Internal clock select and division register 114 |
| CRU_CLKSEL_CON115 | 0x04CC | W | 0x00000181 | Internal clock select and division register 115 |
| CRU_CLKSEL_CON116 | 0x04D0 | W | 0x00000002 | Internal clock select and division register 116 |
| CRU_CLKSEL_CON117 | 0x04D4 | W | 0x00009393 | Internal clock select and division register 117 |
| CRU_CLKSEL_CON118 | 0x04D8 | W | 0x0000002B | Internal clock select and division register 118 |
| CRU_CLKSEL_CON119 | 0x04DC | W | 0x03355460 | Internal clock select and division register 119 |
| CRU_CLKSEL_CON120 | 0x04E0 | W | 0x0000015B | Internal clock select and division register 120 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CRU_CLKSEL_CON121 | 0x04E4 | W | 0x03355460 | Internal clock select and division register 121 |
| CRU_CLKSEL_CON122 | 0x04E8 | W | 0x0000010B | Internal clock select and division register 122 |
| CRU_CLKSEL_CON123 | 0x04EC | W | 0x03355460 | Internal clock select and division register 123 |
| CRU_CLKSEL_CON124 | 0x04F0 | W | 0x00000084 | Internal clock select and division register 124 |
| CRU_CLKSEL_CON125 | 0x04F4 | W | 0x03355460 | Internal clock select and division register 125 |
| CRU_CLKSEL_CON126 | 0x04F8 | W | 0x00000000 | Internal clock select and division register 126 |
| CRU_CLKSEL_CON128 | 0x0500 | W | 0x00001140 | Internal clock select and division register 128 |
| CRU_CLKSEL_CON129 | 0x0504 | W | 0x00000140 | Internal clock select and division register 129 |
| CRU_CLKSEL_CON130 | 0x0508 | W | 0x03355460 | Internal clock select and division register 130 |
| CRU_CLKSEL_CON131 | 0x050C | W | 0x00000003 | Internal clock select and division register 131 |
| CRU_CLKSEL_CON133 | 0x0514 | W | 0x0000005C | Internal clock select and division register 133 |
| CRU_CLKSEL_CON136 | 0x0520 | W | 0x0000005C | Internal clock select and division register 136 |
| CRU_CLKSEL_CON138 | 0x0528 | W | 0x00000003 | Internal clock select and division register 138 |
| CRU_CLKSEL_CON139 | 0x052C | W | 0x03355460 | Internal clock select and division register 139 |
| CRU_CLKSEL_CON140 | 0x0530 | W | 0x000000A0 | Internal clock select and division register 140 |
| CRU_CLKSEL_CON141 | 0x0534 | W | 0x03355460 | Internal clock select and division register 141 |
| CRU_CLKSEL_CON142 | 0x0538 | W | 0x00000003 | Internal clock select and division register 142 |
| CRU_CLKSEL_CON144 | 0x0540 | W | 0x00000028 | Internal clock select and division register 144 |
| CRU_CLKSEL_CON145 | 0x0544 | W | 0x03355460 | Internal clock select and division register 145 |
| CRU_CLKSEL_CON146 | 0x0548 | W | 0x00000017 | Internal clock select and division register 146 |
| CRU_CLKSEL_CON147 | 0x054C | W | 0x03355460 | Internal clock select and division register 147 |
| CRU_CLKSEL_CON148 | 0x0550 | W | 0x0000005B | Internal clock select and division register 148 |
| CRU_CLKSEL_CON149 | 0x0554 | W | 0x03355460 | Internal clock select and division register 149 |
| CRU_CLKSEL_CON150 | 0x0558 | W | 0x00000014 | Internal clock select and division register 150 |
| CRU_CLKSEL_CON151 | 0x055C | W | 0x03355460 | Internal clock select and division register 151 |
| CRU_CLKSEL_CON152 | 0x0560 | W | 0x00004488 | Internal clock select and division register 152 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CRU_CLKSEL_CON153 | 0x0564 | W | 0x000002A2 | Internal clock select and division register 153 |
| CRU_CLKSEL_CON154 | 0x0568 | W | 0x03355460 | Internal clock select and division register 154 |
| CRU_CLKSEL_CON155 | 0x056C | W | 0x0000002B | Internal clock select and division register 155 |
| CRU_CLKSEL_CON156 | 0x0570 | W | 0x03355460 | Internal clock select and division register 156 |
| CRU_CLKSEL_CON157 | 0x0574 | W | 0x0000008B | Internal clock select and division register 157 |
| CRU_CLKSEL_CON158 | 0x0578 | W | 0x00001F80 | Internal clock select and division register 158 |
| CRU_CLKSEL_CON159 | 0x057C | W | 0x00000000 | Internal clock select and division register 159 |
| CRU_CLKSEL_CON160 | 0x0580 | W | 0x00000000 | Internal clock select and division register 160 |
| CRU_CLKSEL_CON161 | 0x0584 | W | 0x00000004 | Internal clock select and division register 161 |
| CRU_CLKSEL_CON163 | 0x058C | W | 0x00000002 | Internal clock select and division register 163 |
| CRU_CLKSEL_CON165 | 0x0594 | W | 0x00000000 | Internal clock select and division register 165 |
| CRU_CLKSEL_CON166 | 0x0598 | W | 0x00000020 | Internal clock select and division register 166 |
| CRU_CLKSEL_CON170 | 0x05A8 | W | 0x00000022 | Internal clock select and division register 170 |
| CRU_CLKSEL_CON172 | 0x05B0 | W | 0x0000000C | Internal clock select and division register 172 |
| CRU_CLKSEL_CON174 | 0x05B8 | W | 0x00004221 | Internal clock select and division register 174 |
| CRU_CLKSEL_CON176 | 0x05C0 | W | 0x00000000 | Internal clock select and division register 176 |
| CRU_CLKSEL_CON177 | 0x05C4 | W | 0x00000000 | Internal clock select and division register 177 |
| CRU_GATE_CON00 | 0x0800 | W | 0x00000000 | Internal clock gate and division register 0 |
| CRU_GATE_CON01 | 0x0804 | W | 0x00000000 | Internal clock gate and division register 1 |
| CRU_GATE_CON02 | 0x0808 | W | 0x00000050 | Internal clock gate and division register 2 |
| CRU_GATE_CON03 | 0x080C | W | 0x00000000 | Internal clock gate and division register 3 |
| CRU_GATE_CON04 | 0x0810 | W | 0x00000000 | Internal clock gate and division register 4 |
| CRU_GATE_CON05 | 0x0814 | W | 0x00000000 | Internal clock gate and division register 5 |
| CRU_GATE_CON06 | 0x0818 | W | 0x00000000 | Internal clock gate and division register 6 |
| CRU_GATE_CON07 | 0x081C | W | 0x00000000 | Internal clock gate and division register 7 |
| CRU_GATE_CON08 | 0x0820 | W | 0x00000000 | Internal clock gate and division register 8 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CRU_GATE_CON09 | 0x0824 | W | 0x00000000 | Internal clock gate and division register 9 |
| CRU_GATE_CON10 | 0x0828 | W | 0x00000000 | Internal clock gate and division register 10 |
| CRU_GATE_CON11 | 0x082C | W | 0x00000000 | Internal clock gate and division register 11 |
| CRU_GATE_CON12 | 0x0830 | W | 0x00000000 | Internal clock gate and division register 12 |
| CRU_GATE_CON13 | 0x0834 | W | 0x00000000 | Internal clock gate and division register 13 |
| CRU_GATE_CON14 | 0x0838 | W | 0x00000000 | Internal clock gate and division register 14 |
| CRU_GATE_CON15 | 0x083C | W | 0x00000000 | Internal clock gate and division register 15 |
| CRU_GATE_CON16 | 0x0840 | W | 0x00000000 | Internal clock gate and division register 16 |
| CRU_GATE_CON17 | 0x0844 | W | 0x00000000 | Internal clock gate and division register 17 |
| CRU_GATE_CON18 | 0x0848 | W | 0x00000000 | Internal clock gate and division register 18 |
| CRU_GATE_CON19 | 0x084C | W | 0x00000000 | Internal clock gate and division register 19 |
| CRU_GATE_CON20 | 0x0850 | W | 0x00000000 | Internal clock gate and division register 20 |
| CRU_GATE_CON21 | 0x0854 | W | 0x00000000 | Internal clock gate and division register 21 |
| CRU_GATE_CON22 | 0x0858 | W | 0x00000200 | Internal clock gate and division register 22 |
| CRU_GATE_CON23 | 0x085C | W | 0x00000000 | Internal clock gate and division register 23 |
| CRU_GATE_CON24 | 0x0860 | W | 0x00000000 | Internal clock gate and division register 24 |
| CRU_GATE_CON25 | 0x0864 | W | 0x00000200 | Internal clock gate and division register 25 |
| CRU_GATE_CON26 | 0x0868 | W | 0x00000000 | Internal clock gate and division register 26 |
| CRU_GATE_CON27 | 0x086C | W | 0x00000000 | Internal clock gate and division register 27 |
| CRU_GATE_CON28 | 0x0870 | W | 0x00000000 | Internal clock gate and division register 28 |
| CRU_GATE_CON29 | 0x0874 | W | 0x00000004 | Internal clock gate and division register 29 |
| CRU_GATE_CON30 | 0x0878 | W | 0x00000000 | Internal clock gate and division register 30 |
| CRU_GATE_CON31 | 0x087C | W | 0x00000000 | Internal clock gate and division register 31 |
| CRU_GATE_CON32 | 0x0880 | W | 0x00000000 | Internal clock gate and division register 32 |
| CRU_GATE_CON33 | 0x0884 | W | 0x00000000 | Internal clock gate and division register 33 |
| CRU_GATE_CON34 | 0x0888 | W | 0x00000000 | Internal clock gate and division register 34 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CRU_GATE_CON35 | 0x088C | W | 0x00000000 | Internal clock gate and division register 35 |
| CRU_GATE_CON37 | 0x0894 | W | 0x00000000 | Internal clock gate and division register 37 |
| CRU_GATE_CON38 | 0x0898 | W | 0x00000000 | Internal clock gate and division register 38 |
| CRU_GATE_CON39 | 0x089C | W | 0x00000000 | Internal clock gate and division register 39 |
| CRU_GATE_CON40 | 0x08A0 | W | 0x00000000 | Internal clock gate and division register 40 |
| CRU_GATE_CON41 | 0x08A4 | W | 0x00000000 | Internal clock gate and division register 41 |
| CRU_GATE_CON42 | 0x08A8 | W | 0x00000000 | Internal clock gate and division register 42 |
| CRU_GATE_CON43 | 0x08AC | W | 0x00000000 | Internal clock gate and division register 43 |
| CRU_GATE_CON44 | 0x08B0 | W | 0x00000000 | Internal clock gate and division register 44 |
| CRU_GATE_CON45 | 0x08B4 | W | 0x00000000 | Internal clock gate and division register 45 |
| CRU_GATE_CON47 | 0x08BC | W | 0x00000000 | Internal clock gate and division register 47 |
| CRU_GATE_CON48 | 0x08C0 | W | 0x00000000 | Internal clock gate and division register 48 |
| CRU_GATE_CON49 | 0x08C4 | W | 0x00000000 | Internal clock gate and division register 49 |
| CRU_GATE_CON50 | 0x08C8 | W | 0x00000000 | Internal clock gate and division register 50 |
| CRU_GATE_CON51 | 0x08CC | W | 0x00000000 | Internal clock gate and division register 51 |
| CRU_GATE_CON52 | 0x08D0 | W | 0x00000000 | Internal clock gate and division register 52 |
| CRU_GATE_CON53 | 0x08D4 | W | 0x00000000 | Internal clock gate and division register 53 |
| CRU_GATE_CON55 | 0x08DC | W | 0x00000000 | Internal clock gate and division register 55 |
| CRU_GATE_CON56 | 0x08E0 | W | 0x00000000 | Internal clock gate and division register 56 |
| CRU_GATE_CON57 | 0x08E4 | W | 0x00000000 | Internal clock gate and division register 57 |
| CRU_GATE_CON59 | 0x08EC | W | 0x00000000 | Internal clock gate and division register 59 |
| CRU_GATE_CON60 | 0x08F0 | W | 0x00000000 | Internal clock gate and division register 60 |
| CRU_GATE_CON61 | 0x08F4 | W | 0x00000000 | Internal clock gate and division register 61 |
| CRU_GATE_CON62 | 0x08F8 | W | 0x00000000 | Internal clock gate and division register 62 |
| CRU_GATE_CON63 | 0x08FC | W | 0x00000000 | Internal clock gate and division register 63 |
| CRU_GATE_CON64 | 0x0900 | W | 0x00000000 | Internal clock gate and division register 64 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CRU_GATE_CON65 | 0x0904 | W | 0x00000000 | Internal clock gate and division register 65 |
| CRU_GATE_CON66 | 0x0908 | W | 0x00000004 | Internal clock gate and division register 66 |
| CRU_GATE_CON67 | 0x090C | W | 0x00000000 | Internal clock gate and division register 67 |
| CRU_GATE_CON68 | 0x0910 | W | 0x00000000 | Internal clock gate and division register 68 |
| CRU_GATE_CON69 | 0x0914 | W | 0x00000000 | Internal clock gate and division register 69 |
| CRU_GATE_CON70 | 0x0918 | W | 0x00000000 | Internal clock gate and division register 70 |
| CRU_GATE_CON72 | 0x0920 | W | 0x00000000 | Internal clock gate and division register 72 |
| CRU_GATE_CON73 | 0x0924 | W | 0x00000000 | Internal clock gate and division register 73 |
| CRU_GATE_CON74 | 0x0928 | W | 0x00000000 | Internal clock gate and division register 74 |
| CRU_GATE_CON75 | 0x092C | W | 0x00000000 | Internal clock gate and division register 75 |
| CRU_GATE_CON76 | 0x0930 | W | 0x00000000 | Internal clock gate and division register 76 |
| CRU_GATE_CON77 | 0x0934 | W | 0x00000000 | Internal clock gate and division register 77 |
| CRU_SOFTRST_CON01 | 0x0A04 | W | 0x00000000 | Internal clock reset register 1 |
| CRU_SOFTRST_CON02 | 0x0A08 | W | 0x00000000 | Internal clock reset register 2 |
| CRU_SOFTRST_CON03 | 0x0A0C | W | 0x00000000 | Internal clock reset register 3 |
| CRU_SOFTRST_CON04 | 0x0A10 | W | 0x00000000 | Internal clock reset register 4 |
| CRU_SOFTRST_CON05 | 0x0A14 | W | 0x00000000 | Internal clock reset register 5 |
| CRU_SOFTRST_CON06 | 0x0A18 | W | 0x00000000 | Internal clock reset register 6 |
| CRU_SOFTRST_CON07 | 0x0A1C | W | 0x00000000 | Internal clock reset register 7 |
| CRU_SOFTRST_CON08 | 0x0A20 | W | 0x00000000 | Internal clock reset register 8 |
| CRU_SOFTRST_CON09 | 0x0A24 | W | 0x00000000 | Internal clock reset register 9 |
| CRU_SOFTRST_CON10 | 0x0A28 | W | 0x00000000 | Internal clock reset register 10 |
| CRU_SOFTRST_CON11 | 0x0A2C | W | 0x00000000 | Internal clock reset register 11 |
| CRU_SOFTRST_CON12 | 0x0A30 | W | 0x00000000 | Internal clock reset register 12 |
| CRU_SOFTRST_CON13 | 0x0A34 | W | 0x00000000 | Internal clock reset register 13 |
| CRU_SOFTRST_CON14 | 0x0A38 | W | 0x00000000 | Internal clock reset register 14 |
| CRU_SOFTRST_CON15 | 0x0A3C | W | 0x00000000 | Internal clock reset register 15 |
| CRU_SOFTRST_CON16 | 0x0A40 | W | 0x00000000 | Internal clock reset register 16 |
| CRU_SOFTRST_CON17 | 0x0A44 | W | 0x00000000 | Internal clock reset register 17 |
| CRU_SOFTRST_CON18 | 0x0A48 | W | 0x00000000 | Internal clock reset register 18 |
| CRU_SOFTRST_CON19 | 0x0A4C | W | 0x00000000 | Internal clock reset register 19 |
| CRU_SOFTRST_CON20 | 0x0A50 | W | 0x00000040 | Internal clock reset register 20 |
| CRU_SOFTRST_CON21 | 0x0A54 | W | 0x00000004 | Internal clock reset register 21 |
| CRU_SOFTRST_CON22 | 0x0A58 | W | 0x00000000 | Internal clock reset register 22 |
| CRU_SOFTRST_CON23 | 0x0A5C | W | 0x00000040 | Internal clock reset register 23 |
| CRU_SOFTRST_CON24 | 0x0A60 | W | 0x00000004 | Internal clock reset register 24 |
| CRU_SOFTRST_CON25 | 0x0A64 | W | 0x00000000 | Internal clock reset register 25 |
| CRU_SOFTRST_CON26 | 0x0A68 | W | 0x00000000 | Internal clock reset register 26 |
| CRU_SOFTRST_CON27 | 0x0A6C | W | 0x00000000 | Internal clock reset register 27 |
| CRU_SOFTRST_CON28 | 0x0A70 | W | 0x00000000 | Internal clock reset register 28 |
| CRU_SOFTRST_CON29 | 0x0A74 | W | 0x00000000 | Internal clock reset register 29 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CRU_SOFTRST_CON30 | 0x0A78 | W | 0x00000008 | Internal clock reset register 30 |
| CRU_SOFTRST_CON31 | 0x0A7C | W | 0x00000000 | Internal clock reset register 31 |
| CRU_SOFTRST_CON32 | 0x0A80 | W | 0x0000E000 | Internal clock reset register 32 |
| CRU_SOFTRST_CON33 | 0x0A84 | W | 0x00000003 | Internal clock reset register 33 |
| CRU_SOFTRST_CON34 | 0x0A88 | W | 0x00000000 | Internal clock reset register 34 |
| CRU_SOFTRST_CON35 | 0x0A8C | W | 0x00000000 | Internal clock reset register 35 |
| CRU_SOFTRST_CON37 | 0x0A94 | W | 0x00000000 | Internal clock reset register 37 |
| CRU_SOFTRST_CON40 | 0x0AA0 | W | 0x00000000 | Internal clock reset register 40 |
| CRU_SOFTRST_CON41 | 0x0AA4 | W | 0x00000000 | Internal clock reset register 41 |
| CRU_SOFTRST_CON42 | 0x0AA8 | W | 0x00000000 | Internal clock reset register 42 |
| CRU_SOFTRST_CON43 | 0x0AAC | W | 0x00000000 | Internal clock reset register 43 |
| CRU_SOFTRST_CON44 | 0x0AB0 | W | 0x00000000 | Internal clock reset register 44 |
| CRU_SOFTRST_CON45 | 0x0AB4 | W | 0x00000000 | Internal clock reset register 45 |
| CRU_SOFTRST_CON47 | 0x0ABC | W | 0x00000000 | Internal clock reset register 47 |
| CRU_SOFTRST_CON48 | 0x0AC0 | W | 0x00000000 | Internal clock reset register 48 |
| CRU_SOFTRST_CON49 | 0x0AC4 | W | 0x00000000 | Internal clock reset register 49 |
| CRU_SOFTRST_CON50 | 0x0AC8 | W | 0x00000000 | Internal clock reset register 50 |
| CRU_SOFTRST_CON51 | 0x0ACC | W | 0x00000000 | Internal clock reset register 51 |
| CRU_SOFTRST_CON52 | 0x0AD0 | W | 0x00000000 | Internal clock reset register 52 |
| CRU_SOFTRST_CON53 | 0x0AD4 | W | 0x00000000 | Internal clock reset register 53 |
| CRU_SOFTRST_CON55 | 0x0ADC | W | 0x00000000 | Internal clock reset register 55 |
| CRU_SOFTRST_CON56 | 0x0AE0 | W | 0x00000000 | Internal clock reset register 56 |
| CRU_SOFTRST_CON57 | 0x0AE4 | W | 0x00000000 | Internal clock reset register 57 |
| CRU_SOFTRST_CON59 | 0x0AEC | W | 0x00000000 | Internal clock reset register 59 |
| CRU_SOFTRST_CON60 | 0x0AF0 | W | 0x00000000 | Internal clock reset register 60 |
| CRU_SOFTRST_CON61 | 0x0AF4 | W | 0x00000000 | Internal clock reset register 61 |
| CRU_SOFTRST_CON62 | 0x0AF8 | W | 0x00000000 | Internal clock reset register 62 |
| CRU_SOFTRST_CON63 | 0x0AFC | W | 0x00000000 | Internal clock reset register 63 |
| CRU_SOFTRST_CON64 | 0x0B00 | W | 0x00000000 | Internal clock reset register 64 |
| CRU_SOFTRST_CON65 | 0x0B04 | W | 0x00000000 | Internal clock reset register 65 |
| CRU_SOFTRST_CON66 | 0x0B08 | W | 0x00000000 | Internal clock reset register 66 |
| CRU_SOFTRST_CON67 | 0x0B0C | W | 0x00000000 | Internal clock reset register 67 |
| CRU_SOFTRST_CON68 | 0x0B10 | W | 0x00000000 | Internal clock reset register 68 |
| CRU_SOFTRST_CON69 | 0x0B14 | W | 0x00004000 | Internal clock reset register 69 |
| CRU_SOFTRST_CON70 | 0x0B18 | W | 0x00000000 | Internal clock reset register 70 |
| CRU_SOFTRST_CON72 | 0x0B20 | W | 0x00000000 | Internal clock reset register 72 |
| CRU_SOFTRST_CON73 | 0x0B24 | W | 0x00000000 | Internal clock reset register 73 |
| CRU_SOFTRST_CON74 | 0x0B28 | W | 0x00000000 | Internal clock reset register 74 |
| CRU_SOFTRST_CON75 | 0x0B2C | W | 0x00000000 | Internal clock reset register 75 |
| CRU_SOFTRST_CON76 | 0x0B30 | W | 0x00000000 | Internal clock reset register 76 |
| CRU_SOFTRST_CON77 | 0x0B34 | W | 0x00000000 | Internal clock reset register 77 |
| CRU_GLB_CNT_TH | 0x0C00 | W | 0x00000064 | System control register |
| CRU_GLBRST_ST | 0x0C04 | W | 0x00000000 | System control register |
| CRU_GLB_SRST_FST_VALUE | 0x0C08 | W | 0x00000000 | System control register |
| CRU_GLB_SRST_SND_VALUE | 0x0C0C | W | 0x00000000 | System control register |
| CRU_GLB_RST_CON | 0x0C10 | W | 0x00000000 | System control register |
| CRU_SDIO_CON0 | 0x0C24 | W | 0x00000000 | System control register |
| CRU_SDIO_CON1 | 0x0C28 | W | 0x00000000 | System control register |
| CRU_SDMMC_CON0 | 0x0C30 | W | 0x00000000 | System control register |
| CRU_SDMMC_CON1 | 0x0C34 | W | 0x00000000 | System control register |

FIRST RELEASE

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CRU_PHYREF_ALT_GATE_CON | 0x0C38 | W | 0x00000000 | System control register |
| CRU_CM0_GATEMASK_CON | 0x0C3C | W | 0x00000000 | System control register |
| CRU_QCHANNEL_CON01 | 0x0CA4 | W | 0x00000000 | Qchannel control register 1 |
| CRU_SMOTH_DIVFREE_CON08 | 0x0CC0 | W | 0x00000000 | Smoothdiv control register |
| CRU_SMOTH_DIVFREE_CON09 | 0x0CC4 | W | 0x00000000 | Smoothdiv control register |
| CRU_SMOTH_DIVFREE_CON10 | 0x0CC8 | W | 0x00000000 | Smoothdiv control register |
| CRU_SMOTH_DIVFREE_CON11 | 0x0CCC | W | 0x00000000 | Smoothdiv control register |
| CRU_SMOTH_DIVFREE_CON12 | 0x0CD0 | W | 0x00000000 | Smoothdiv control register |
| CRU_AUTOCS_ACLK_TOP_ROOT_CON0 | 0x0D00 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_TOP_ROOT_CON1 | 0x0D04 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_LOW_TOP_ROOT_CON0 | 0x0D08 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_LOW_TOP_ROOT_CON1 | 0x0D0C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_TOP_M400_ROOT_CON0 | 0x0D10 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_TOP_M400_ROOT_CON1 | 0x0D14 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_TOP_S400_ROOT_CON0 | 0x0D18 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_TOP_S400_ROOT_CON1 | 0x0D1C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_BUS_ROOT_CON0 | 0x0D20 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_BUS_ROOT_CON1 | 0x0D24 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_ISP1_ROOT_CON0 | 0x0D28 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_ISP1_ROOT_CON1 | 0x0D2C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_CLK_RKNN_DSU0_CON0 | 0x0D30 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_CLK_RKNN_DSU0_CON1 | 0x0D34 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_HCLK_RKNN_ROOT_CON0 | 0x0D38 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_HCLK_RKNN_ROOT_CON1 | 0x0D3C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_NVM_ROOT_CON0 | 0x0D40 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_NVM_ROOT_CON1 | 0x0D44 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_PHP_ROOT_CON0 | 0x0D48 | W | 0x00200004 | Auto clock switch control register 0 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CRU_AUTOCS_ACLK_PHP_ROOT_CON1 | 0x0D4C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_RKVDEC0_ROOT_CON0 | 0x0D50 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_RKVDEC0_ROOT_CON1 | 0x0D54 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_RKVDEC_CCU_CON0 | 0x0D58 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_RKVDEC_CCU_CON1 | 0x0D5C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_RKVDEC1_ROOT_CON0 | 0x0D60 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_RKVDEC1_ROOT_CON1 | 0x0D64 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_USB_ROOT_CON0 | 0x0D68 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_USB_ROOT_CON1 | 0x0D6C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_VDPU_ROOT_CON0 | 0x0D70 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_VDPU_ROOT_CON1 | 0x0D74 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_VDPU_LOW_ROOT_CON0 | 0x0D78 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_VDPU_LOW_ROOT_CON1 | 0x0D7C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_JPEG_DECODER_ROOT_CON0 | 0x0D80 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_JPEG_DECODER_ROOT_CON1 | 0x0D84 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_RKVENC0_ROOT_CON0 | 0x0D88 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_RKVENC0_ROOT_CON1 | 0x0D8C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_RKVENC1_ROOT_CON0 | 0x0D90 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_RKVENC1_ROOT_CON1 | 0x0D94 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_VI_ROOT_CON0 | 0x0D98 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_VI_ROOT_CON1 | 0x0D9C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_VOP_ROOT_CON0 | 0x0DA0 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_VOP_ROOT_CON1 | 0x0DA4 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_VO0_ROOT_CON0 | 0x0DA8 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_VO0_ROOT_CON1 | 0x0DAC | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_HDCP1_ROOT_CON0 | 0x0DB0 | W | 0x00200004 | Auto clock switch control register 0 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CRU_AUTOCS_ACLK_HDCP1_ROOT_CON1 | 0x0DB4 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_HDMIRX_ROOT_CON0 | 0x0DB8 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_HDMIRX_ROOT_CON1 | 0x0DBC | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_CLK_GPU_COREGROUP_CON0 | 0x0DC0 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_CLK_GPU_COREGROUP_CON1 | 0x0DC4 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_AV1_ROOT_CON0 | 0x0DE0 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_AV1_ROOT_CON1 | 0x0DE4 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_CENTER_ROOT_CON0 | 0x0DE8 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_CENTER_ROOT_CON1 | 0x0DEC | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_CENTER_LOW_ROOT_CON0 | 0x0DF0 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_CENTER_LOW_ROOT_CON1 | 0x0DF4 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_CENTER_S400_ROOT_CON0 | 0x0DF8 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_CENTER_S400_ROOT_CON1 | 0x0DFC | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_VO1USB_TOP_ROOT_CON0 | 0x0E00 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_VO1USB_TOP_ROOT_CON1 | 0x0E04 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_RGA3_ROOT_CON0 | 0x0E08 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_RGA3_ROOT_CON1 | 0x0E0C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_PCLK_AV1_ROOT_CON0 | 0x0E10 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_PCLK_AV1_ROOT_CON1 | 0x0E14 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_HCLK_ISP1_ROOT_CON0 | 0x0E18 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_HCLK_ISP1_ROOT_CON1 | 0x0E1C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_PCLK_NPUTOP_ROOT_CON0 | 0x0E20 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_PCLK_NPUTOP_ROOT_CON1 | 0x0E24 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_HCLK_NPU_CM0_ROOT_CON0 | 0x0E28 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_HCLK_NPU_CM0_ROOT_CON1 | 0x0E2C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_HCLK_NVM_ROOT_CON0 | 0x0E30 | W | 0x00200004 | Auto clock switch control register 0 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CRU_AUTOCS_HCLK_NVM_ROOT_CON1 | 0x0E34 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_PCLK_PHP_ROOT_CON0 | 0x0E38 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_PCLK_PHP_ROOT_CON1 | 0x0E3C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_PCIE_ROOT_CON0 | 0x0E40 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_PCIE_ROOT_CON1 | 0x0E44 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_HCLK_RKVDEC0_ROOT_CON0 | 0x0E48 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_HCLK_RKVDEC0_ROOT_CON1 | 0x0E4C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_HCLK_RKVDEC1_ROOT_CON0 | 0x0E50 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_HCLK_RKVDEC1_ROOT_CON1 | 0x0E54 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_PCLK_TOP_ROOT_CON0 | 0x0E58 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_PCLK_TOP_ROOT_CON1 | 0x0E5C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_TOP_M500_ROOT_CON0 | 0x0E60 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_TOP_M500_ROOT_CON1 | 0x0E64 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_TOP_S200_ROOT_CON0 | 0x0E68 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_TOP_S200_ROOT_CON1 | 0x0E6C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_HCLK_USB_ROOT_CON0 | 0x0E70 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_HCLK_USB_ROOT_CON1 | 0x0E74 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_HCLK_VDPU_ROOT_CON0 | 0x0E78 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_HCLK_VDPU_ROOT_CON1 | 0x0E7C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_HCLK_RKVENC0_ROOT_CON0 | 0x0E80 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_HCLK_RKVENC0_ROOT_CON1 | 0x0E84 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_HCLK_RKVENC1_ROOT_CON0 | 0x0E88 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_HCLK_RKVENC1_ROOT_CON1 | 0x0E8C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_HCLK_VI_ROOT_CON0 | 0x0E90 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_HCLK_VI_ROOT_CON1 | 0x0E94 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_PCLK_VI_ROOT_CON0 | 0x0E98 | W | 0x00200004 | Auto clock switch control register 0 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CRU_AUTOCS_PCLK_VI_ROOT_CON1 | 0x0E9C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_VOP_LOW_ROOT_CON0 | 0x0EA0 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_VOP_LOW_ROOT_CON1 | 0x0EA4 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_HCLK_VOP_ROOT_CON0 | 0x0EA8 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_HCLK_VOP_ROOT_CON1 | 0x0EAC | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_PCLK_VOP_ROOT_CON0 | 0x0EB0 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_PCLK_VOP_ROOT_CON1 | 0x0EB4 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_HCLK_VO0_ROOT_CON0 | 0x0EB8 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_HCLK_VO0_ROOT_CON1 | 0x0EBC | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_HCLK_VO0_S_ROOT_CON0 | 0x0EC0 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_HCLK_VO0_S_ROOT_CON1 | 0x0EC4 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_PCLK_VO0_ROOT_CON0 | 0x0EC8 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_PCLK_VO0_ROOT_CON1 | 0x0ECC | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_PCLK_VO0_S_ROOT_CON0 | 0x0ED0 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_PCLK_VO0_S_ROOT_CON1 | 0x0ED4 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_HCLK_VO1_ROOT_CON0 | 0x0ED8 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_HCLK_VO1_ROOT_CON1 | 0x0EDC | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_HCLK_VO1_S_ROOT_CON0 | 0x0EE0 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_HCLK_VO1_S_ROOT_CON1 | 0x0EE4 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_PCLK_VO1_ROOT_CON0 | 0x0EE8 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_PCLK_VO1_ROOT_CON1 | 0x0EEC | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_PCLK_VO1_S_ROOT_CON0 | 0x0EF0 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_PCLK_VO1_S_ROOT_CON1 | 0x0EF4 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_PCLK_GPU_ROOT_CON0 | 0x0EF8 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_PCLK_GPU_ROOT_CON1 | 0x0EFC | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_HCLK_CENTER_ROOT_CON0 | 0x0F00 | W | 0x00200004 | Auto clock switch control register 0 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CRU_AUTOCS_HCLK_CENTER_ROOT_CON1 | 0x0F04 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_PCLK_CENTER_ROOT_CON0 | 0x0F08 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_PCLK_CENTER_ROOT_CON1 | 0x0F0C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_CENTER_S200_ROOT_CON0 | 0x0F10 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_CENTER_S200_ROOT_CON1 | 0x0F14 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_HCLK_SDIO_ROOT_CON0 | 0x0F18 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_HCLK_SDIO_ROOT_CON1 | 0x0F1C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_HCLK_RGA3_ROOT_CON0 | 0x0F20 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_HCLK_RGA3_ROOT_CON1 | 0x0F24 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_HCLK_VO1USB_TOP_ROOT_CON0 | 0x0F28 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_HCLK_VO1USB_TOP_ROOT_CON1 | 0x0F2C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_ACLK_TOP_M300_ROOT_CON0 | 0x0F30 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_ACLK_TOP_M300_ROOT_CON1 | 0x0F34 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_CLK_RKNN_DSU0_SRC_T_CON0 | 0x0F38 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_CLK_RKNN_DSU0_SRC_T_CON1 | 0x0F3C | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_HCLK_AUDIO_ROOT_CON0 | 0x0F40 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_HCLK_AUDIO_ROOT_CON1 | 0x0F44 | W | 0x00000000 | Auto clock switch control register 1 |
| CRU_AUTOCS_PCLK_AUDIO_ROOT_CON0 | 0x0F48 | W | 0x00200004 | Auto clock switch control register 0 |
| CRU_AUTOCS_PCLK_AUDIO_ROOT_CON1 | 0x0F4C | W | 0x00000000 | Auto clock switch control register 1 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 2.4.2 Detail Registers Description

**CRU_V0PLL_CON0**

Address: Operational Base + offset (0x0160)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | v0pll_bp<br>BYPASS: Bypass mode control signal.<br>1'b1: bypass mode is enabled. (FOUT = FIN).<br>1'b0: PLL operates normally. |
| 14:10 | RO | 0x00 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9:0 | RW | 0x000 | v0pll_m<br>M: Division value of the 10-bit programmable main-divider.<br>PLL has to be reset if M value is changed.<br>64 <= pll_m <= 1023 |

**CRU_V0PLL_CON1**

Address: Operational Base + offset (0x0164)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | v0pll_resetb<br>RESETB: Power down control signal.<br>1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time.<br>1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset. |
| 12:9 | RO | 0x0 | reserved |
| 8:6 | RW | 0x0 | v0pll_s<br>Division value of the 3-bit programmable scaler.<br>0 <= pll_s <= 6 |
| 5:0 | RW | 0x00 | v0pll_p<br>P: Division value of the 6-bit programmable pre-divider.<br>PLL has to be reset if P value is changed.<br>1 <= pll_p <= 63 |

**CRU_V0PLL_CON2**

Address: Operational Base + offset (0x0168)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | v0pll_k<br>K: Value of 16-bit DSM.<br>pll_k[15:0] is a two's complement integer. |

**CRU_V0PLL_CON3**

Address: Operational Base + offset (0x016C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | v0pll_sel_pf<br>SEL_PF: Value of 2-bit modulation method control.<br>2'b00: down spread;<br>2'b01: up spread;<br>2'b1x: center spread.<br>PLL has to be reset if pll_sel_pf is changed. |
| 13:8 | RW | 0x00 | v0pll_mrr<br>MRR: Value of 6-bit modulation rate control.<br>PLL has to be reset if pll_mrr is changed. |
| 7:0 | RW | 0x00 | v0pll_mfr<br>MFR: Value of 8-bit modulation frequency control.<br>PLL has to be reset if pll_mfr is changed. |

Rockchip Confidential

**CRU_V0PLL_CON4**

Address: Operational Base + offset (0x0170)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | v0pll_fsel<br>FSEL: Monitoring pin.<br>1'b0: FEED_OUT = FREF.<br>1'b1: FEED_OUT = FEED. |
| 14 | RW | 0x0 | v0pll_feed_en<br>FEED_EN: Monitoring pin.<br>1'b0: FEED_OUT is disabled.<br>1'b1: FEED_OUT is enabled. |
| 13:9 | RO | 0x00 | reserved |
| 8:4 | RW | 0x00 | v0pll_extafc<br>EXTAFC: Monitoring pin.<br>If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 3 | RW | 0x0 | v0pll_afc_enb<br>AFC_ENB: Monitoring pin.<br>1'b0: AFC is enabled and VCO is calibrated automatically.<br>1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | v0pll_sscg_en<br>SSCG_EN: Enable pin for dithered mode.<br>1'b0: disable dithered mode.<br>1'b1: enable dithered mode. |

**CRU_V0PLL_CON5**

Address: Operational Base + offset (0x0174)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | v0pll_fout_mask<br>FOUT_MASK: Scaler's re-initialization time control pin. |

**CRU_V0PLL_CON6**

Address: Operational Base + offset (0x0178)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | v0pll_lock<br>LOCK: PLL lock flag.<br>1'b0: PLL is unlocked.<br>1'b1: PLL is locked. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14:10 | RW | 0x00 | v0pll_afc_code<br>AFC_CODE: Monitoring pin.<br>Output code of AFC(5 bits). |
| 9:0 | RO | 0x000 | reserved |

**CRU_AUPLL_CON0**

Address: Operational Base + offset (0x0180)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | aupll_bp<br>BYPASS: Bypass mode control signal.<br>1'b1: bypass mode is enabled. (FOUT = FIN).<br>1'b0: PLL operates normally. |
| 14:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | aupll_m<br>M: Division value of the 10-bit programmable main-divider.<br>PLL has to be reset if M value is changed.<br>64 <= pll_m <= 1023 |

**CRU_AUPLL_CON1**

Address: Operational Base + offset (0x0184)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | aupll_resetb<br>RESETB: Power down control signal.<br>1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time.<br>1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset. |
| 12:9 | RO | 0x0 | reserved |
| 8:6 | RW | 0x0 | aupll_s<br>Division value of the 3-bit programmable scaler.<br>0 <= pll_s <= 6 |
| 5:0 | RW | 0x00 | aupll_p<br>P: Division value of the 6-bit programmable pre-divider.<br>PLL has to be reset if P value is changed.<br>1 <= pll_p <= 63 |

**CRU_AUPLL_CON2**

Address: Operational Base + offset (0x0188)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | aupll_k<br>K: Value of 16-bit DSM.<br>pll_k[15:0] is a two's complement integer. |

**CRU_AUPLL_CON3**

Address: Operational Base + offset (0x018C)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aupll_sel_pf<br>SEL_PF: Value of 2-bit modulation method control.<br>2'b00: down spread;<br>2'b01: up spread;<br>2'b1x: center spread.<br>PLL has to be reset if pll_sel_pf is changed. |
| 13:8 | RW | 0x00 | aupll_mrr<br>MRR: Value of 6-bit modulation rate control.<br>PLL has to be reset if pll_mrr is changed. |
| 7:0 | RW | 0x00 | aupll_mfr<br>MFR: Value of 8-bit modulation frequency control.<br>PLL has to be reset if pll_mfr is changed. |

**CRU_AUPLL_CON4**

Address: Operational Base + offset (0x0190)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | aupll_fsel<br>FSEL: Monitoring pin.<br>1'b0: FEED_OUT = FREF.<br>1'b1: FEED_OUT = FEED. |
| 14 | RW | 0x0 | aupll_feed_en<br>FEED_EN: Monitoring pin.<br>1'b0: FEED_OUT is disabled.<br>1'b1: FEED_OUT is enabled. |
| 13:9 | RO | 0x00 | reserved |
| 8:4 | RW | 0x00 | aupll_extafc<br>EXTAFC: Monitoring pin.<br>If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 3 | RW | 0x0 | aupll_afc_enb<br>AFC_ENB: Monitoring pin.<br>1'b0: AFC is enabled and VCO is calibrated automatically.<br>1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | aupll_sscg_en<br>SSCG_EN: Enable pin for dithered mode.<br>1'b0: disable dithered mode.<br>1'b1: enable dithered mode. |

**CRU_AUPLL_CON5**

Address: Operational Base + offset (0x0194)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | aupll_fout_mask<br>FOUT_MASK: Scaler's re-initialization time control pin. |

**CRU_AUPLL_CON6**

Address: Operational Base + offset (0x0198)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | aupll_lock<br>LOCK: PLL lock flag.<br>1'b0: PLL is unlocked.<br>1'b1: PLL is locked. |
| 14:10 | RW | 0x00 | aupll_afc_code<br>AFC_CODE: Monitoring pin.<br>Output code of AFC(5 bits). |
| 9:0 | RO | 0x000 | reserved |

**CRU_CPLL_CON0**

Address: Operational Base + offset (0x01A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | cpll_bp<br>BYPASS: Bypass mode control signal.<br>1'b1: bypass mode is enabled. (FOUT = FIN).<br>1'b0: PLL operates normally. |
| 14:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | cpll_m<br>M: Division value of the 10-bit programmable main-divider.<br>PLL has to be reset if M value is changed.<br>64 <= pll_m <= 1023 |

**CRU_CPLL_CON1**

Address: Operational Base + offset (0x01A4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | cpll_resetb<br>RESETB: Power down control signal.<br>1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time.<br>1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset. |
| 12:9 | RO | 0x0 | reserved |
| 8:6 | RW | 0x0 | cpll_s<br>Division value of the 3-bit programmable scaler.<br>0 <= pll_s <= 6 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5:0 | RW | 0x00 | cpll_p<br>P: Division value of the 6-bit programmable pre-divider.<br>PLL has to be reset if P value is changed.<br>1 <= pll_p <= 63 |

**CRU_CPLL_CON2**

Address: Operational Base + offset (0x01A8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | cpll_k<br>K: Value of 16-bit DSM.<br>pll_k[15:0] is a two's complement integer. |

**CRU_CPLL_CON3**

Address: Operational Base + offset (0x01AC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | cpll_sel_pf<br>SEL_PF: Value of 2-bit modulation method control.<br>2'b00: down spread;<br>2'b01: up spread;<br>2'b1x: center spread.<br>PLL has to be reset if pll_sel_pf is changed. |
| 13:8 | RW | 0x00 | cpll_mrr<br>MRR: Value of 6-bit modulation rate control.<br>PLL has to be reset if pll_mrr is changed. |
| 7:0 | RW | 0x00 | cpll_mfr<br>MFR: Value of 8-bit modulation frequency control.<br>PLL has to be reset if pll_mfr is changed. |

**CRU_CPLL_CON4**

Address: Operational Base + offset (0x01B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | cpll_fsel<br>FSEL: Monitoring pin.<br>1'b0: FEED_OUT = FREF.<br>1'b1: FEED_OUT = FEED. |
| 14 | RW | 0x0 | cpll_feed_en<br>FEED_EN: Monitoring pin.<br>1'b0: FEED_OUT is disabled.<br>1'b1: FEED_OUT is enabled. |
| 13:9 | RO | 0x00 | reserved |
| 8:4 | RW | 0x00 | cpll_extafc<br>EXTAFC: Monitoring pin.<br>If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | cpll_afc_enb<br>AFC_ENB: Monitoring pin.<br>1'b0: AFC is enabled and VCO is calibrated automatically.<br>1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | cpll_sscg_en<br>SSCG_EN: Enable pin for dithered mode.<br>1'b0: disable dithered mode.<br>1'b1: enable dithered mode. |

**CRU_CPLL_CON5**

Address: Operational Base + offset (0x01B4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | cpll_fout_mask<br>FOUT_MASK: Scaler's re-initialization time control pin. |

**CRU_CPLL_CON6**

Address: Operational Base + offset (0x01B8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | cpll_lock<br>LOCK: PLL lock flag.<br>1'b0: PLL is unlocked.<br>1'b1: PLL is locked. |
| 14:10 | RW | 0x00 | cpll_afc_code<br>AFC_CODE: Monitoring pin.<br>Output code of AFC(5 bits). |
| 9:0 | RO | 0x000 | reserved |

**CRU_GPLL_CON0**

Address: Operational Base + offset (0x01C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | gpll_bp<br>BYPASS: Bypass mode control signal.<br>1'b1: bypass mode is enabled. (FOUT = FIN).<br>1'b0: PLL operates normally. |
| 14:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | gpll_m<br>M: Division value of the 10-bit programmable main-divider.<br>PLL has to be reset if M value is changed.<br>64 <= pll_m <= 1023 |

Rockchip Confidencial

**CRU_GPLL_CON1**

Address: Operational Base + offset (0x01C4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | gpll_resetb<br>RESETB: Power down control signal.<br>1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time.<br>1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset. |
| 12:9 | RO | 0x0 | reserved |
| 8:6 | RW | 0x0 | gpll_s<br>Division value of the 3-bit programmable scaler.<br>0 <= pll_s <= 6 |
| 5:0 | RW | 0x00 | gpll_p<br>P: Division value of the 6-bit programmable pre-divider.<br>PLL has to be reset if P value is changed.<br>1 <= pll_p <= 63 |

**CRU_GPLL_CON2**

Address: Operational Base + offset (0x01C8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | gpll_k<br>K: Value of 16-bit DSM.<br>pll_k[15:0] is a two's complement integer. |

**CRU_GPLL_CON3**

Address: Operational Base + offset (0x01CC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | gpll_sel_pf<br>SEL_PF: Value of 2-bit modulation method control.<br>2'b00: down spread;<br>2'b01: up spread;<br>2'b1x: center spread.<br>PLL has to be reset if pll_sel_pf is changed. |
| 13:8 | RW | 0x00 | gpll_mrr<br>MRR: Value of 6-bit modulation rate control.<br>PLL has to be reset if pll_mrr is changed. |
| 7:0 | RW | 0x00 | gpll_mfr<br>MFR: Value of 8-bit modulation frequency control.<br>PLL has to be reset if pll_mfr is changed. |

**CRU_GPLL_CON4**

Address: Operational Base + offset (0x01D0)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | gpll_fsel<br>FSEL: Monitoring pin.<br>1'b0: FEED_OUT = FREF.<br>1'b1: FEED_OUT = FEED. |
| 14 | RW | 0x0 | gpll_feed_en<br>FEED_EN: Monitoring pin.<br>1'b0: FEED_OUT is disabled.<br>1'b1: FEED_OUT is enabled. |
| 13:9 | RO | 0x00 | reserved |
| 8:4 | RW | 0x00 | gpll_extafc<br>EXTAFC: Monitoring pin.<br>If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 3 | RW | 0x0 | gpll_afc_enb<br>AFC_ENB: Monitoring pin.<br>1'b0: AFC is enabled and VCO is calibrated automatically.<br>1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | gpll_sscg_en<br>SSCG_EN: Enable pin for dithered mode.<br>1'b0: disable dithered mode.<br>1'b1: enable dithered mode. |

**CRU_GPLL_CON5**

Address: Operational Base + offset (0x01D4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | gpll_fout_mask<br>FOUT_MASK: Scaler's re-initialization time control pin. |

**CRU_GPLL_CON6**

Address: Operational Base + offset (0x01D8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | gpll_lock<br>LOCK: PLL lock flag.<br>1'b0: PLL is unlocked.<br>1'b1: PLL is locked. |
| 14:10 | RW | 0x00 | gpll_afc_code<br>AFC_CODE: Monitoring pin.<br>Output code of AFC(5 bits). |
| 9:0 | RO | 0x000 | reserved |

Rockchip Confidential

**CRU_NPLL_CON0**

Address: Operational Base + offset (0x01E0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | npll_bp<br>BYPASS: Bypass mode control signal.<br>1'b1: bypass mode is enabled. (FOUT = FIN).<br>1'b0: PLL operates normally. |
| 14:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | npll_m<br>M: Division value of the 10-bit programmable main-divider.<br>PLL has to be reset if M value is changed.<br>64 <= pll_m <= 1023 |

**CRU_NPLL_CON1**

Address: Operational Base + offset (0x01E4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | npll_resetb<br>RESETB: Power down control signal.<br>1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time.<br>1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset. |
| 12:9 | RO | 0x0 | reserved |
| 8:6 | RW | 0x0 | npll_s<br>Division value of the 3-bit programmable scaler.<br>0 <= pll_s <= 6 |
| 5:0 | RW | 0x00 | npll_p<br>P: Division value of the 6-bit programmable pre-divider.<br>PLL has to be reset if P value is changed.<br>1 <= pll_p <= 63 |

**CRU_NPLL_CON4**

Address: Operational Base + offset (0x01F0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | npll_fsel<br>FSEL: Monitoring pin.<br>1'b0: FEED_OUT = FREF.<br>1'b1: FEED_OUT = FEED. |
| 14 | RW | 0x0 | npll_feed_en<br>FEED_EN: Monitoring pin.<br>1'b0: FEED_OUT is disabled.<br>1'b1: FEED_OUT is enabled. |
| 13:9 | RO | 0x00 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8:4 | RW | 0x00 | npll_extafc<br>EXTAFC: Monitoring pin.<br>If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 3 | RW | 0x0 | npll_afc_enb<br>AFC_ENB: Monitoring pin.<br>1'b0: AFC is enabled and VCO is calibrated automatically.<br>1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 2:1 | RW | 0x1 | npll_icp<br>Charge-pump current control signal. |
| 0 | RO | 0x0 | reserved |

**CRU_NPLL_CON5**

Address: Operational Base + offset (0x01F4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10:9 | RW | 0x3 | npll_lock_con_dly<br>LOCK_CON_DLY: Lock detector setting of the detection resolution. |
| 8:7 | RW | 0x3 | npll_lock_con_out<br>LOCK_CON_OUT: Lock detector setting of the output margin. |
| 6:5 | RW | 0x3 | npll_lock_con_in<br>LOCK_CON_IN: Lock detector setting of the input margin. |
| 4:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | npll_fout_mask<br>FOUT_MASK: Scaler's re-initialization time control pin. |

**CRU_NPLL_CON6**

Address: Operational Base + offset (0x01F8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | npll_lock<br>LOCK: PLL lock flag.<br>1'b0: PLL is unlocked.<br>1'b1: PLL is locked. |
| 14:10 | RW | 0x00 | npll_afc_code<br>AFC_CODE: Monitoring pin.<br>Output code of AFC(5 bits). |
| 9:0 | RO | 0x000 | reserved |

**CRU_MODE_CON00**

Address: Operational Base + offset (0x0280)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:10 | RO | 0x00 | reserved |
| 9:8 | RW | 0x0 | clk_cpll_mode<br>clk_cpll_mux clock mux.<br>2'b00: xin_osc0_func<br>2'b01: clk_cpll<br>2'b10: clk_deepslow |
| 7:6 | RW | 0x0 | clk_aupll_mode<br>clk_aupll_mux clock mux.<br>2'b00: xin_osc0_func<br>2'b01: clk_aupll<br>2'b10: clk_deepslow |
| 5:4 | RW | 0x0 | clk_v0pll_mode<br>clk_v0pll_mux clock mux.<br>2'b00: xin_osc0_func<br>2'b01: clk_v0pll<br>2'b10: clk_deepslow |
| 3:2 | RW | 0x0 | clk_gpll_mode<br>clk_gpll_mux clock mux.<br>2'b00: xin_osc0_func<br>2'b01: clk_gpll<br>2'b10: clk_deepslow |
| 1:0 | RW | 0x0 | clk_npll_mode<br>clk_npll_mux clock mux.<br>2'b00: xin_osc0_func<br>2'b01: clk_npll<br>2'b10: clk_deepslow |

**CRU_CLKSEL_CON00**

Address: Operational Base + offset (0x0300)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x1 | clk_matrix_100m_src_sel<br>clk_matrix_100m_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 10:6 | RW | 0x0e | clk_matrix_100m_src_div<br>Divide clk_matrix_100m_src by (div_con + 1). |
| 5 | RW | 0x1 | clk_matrix_50m_src_sel<br>clk_matrix_50m_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 4:0 | RW | 0x1d | clk_matrix_50m_src_div<br>Divide clk_matrix_50m_src by (div_con + 1). |

**CRU_CLKSEL_CON01**

Address: Operational Base + offset (0x0304)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | clk_matrix_200m_src_sel<br>clk_matrix_200m_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 10:6 | RW | 0x05 | clk_matrix_200m_src_div<br>Divide clk_matrix_200m_src by (div_con + 1). |
| 5 | RW | 0x1 | clk_matrix_150m_src_sel<br>clk_matrix_150m_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 4:0 | RW | 0x09 | clk_matrix_150m_src_div<br>Divide clk_matrix_150m_src by (div_con + 1). |

**CRU_CLKSEL_CON02**

Address: Operational Base + offset (0x0308)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x1 | clk_matrix_300m_src_sel<br>clk_matrix_300m_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 10:6 | RW | 0x04 | clk_matrix_300m_src_div<br>Divide clk_matrix_300m_src by (div_con + 1). |
| 5 | RW | 0x1 | clk_matrix_250m_src_sel<br>clk_matrix_250m_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 4:0 | RW | 0x05 | clk_matrix_250m_src_div<br>Divide clk_matrix_250m_src by (div_con + 1). |

**CRU_CLKSEL_CON03**

Address: Operational Base + offset (0x030C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | clk_matrix_400m_src_sel<br>clk_matrix_400m_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 10:6 | RW | 0x02 | clk_matrix_400m_src_div<br>Divide clk_matrix_400m_src by (div_con + 1). |
| 5 | RW | 0x1 | clk_matrix_350m_src_sel<br>clk_matrix_350m_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_spll_mux |
| 4:0 | RW | 0x01 | clk_matrix_350m_src_div<br>Divide clk_matrix_350m_src by (div_con + 1). |

Rockchip Confidencial

**CRU_CLKSEL_CON04**

Address: Operational Base + offset (0x0310)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x1 | clk_matrix_500m_src_sel<br>clk_matrix_500m_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 10:6 | RW | 0x02 | clk_matrix_500m_src_div<br>Divide clk_matrix_500m_src by (div_con + 1). |
| 5 | RW | 0x0 | clk_matrix_450m_src_sel<br>clk_matrix_450m_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 4:0 | RW | 0x01 | clk_matrix_450m_src_div<br>NP5 division register.<br>Divide clk_matrix_450m_src by ((2 * div_con + 3) / 2). |

**CRU_CLKSEL_CON05**

Address: Operational Base + offset (0x0314)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x1 | clk_matrix_650m_src_sel<br>clk_matrix_650m_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_lpll_mux |
| 10:6 | RW | 0x02 | clk_matrix_650m_src_div<br>Divide clk_matrix_650m_src by (div_con + 1). |
| 5 | RW | 0x0 | clk_matrix_600m_src_sel<br>clk_matrix_600m_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 4:0 | RW | 0x01 | clk_matrix_600m_src_div<br>Divide clk_matrix_600m_src by (div_con + 1). |

**CRU_CLKSEL_CON06**

Address: Operational Base + offset (0x0318)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x1 | clk_matrix_800m_src_sel<br>clk_matrix_800m_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_aupll_mux |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10:6 | RW | 0x00 | clk_matrix_800m_src_div<br>Divide clk_matrix_800m_src by (div_con + 1). |
| 5 | RW | 0x1 | clk_matrix_700m_src_sel<br>clk_matrix_700m_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_spll_mux |
| 4:0 | RW | 0x00 | clk_matrix_700m_src_div<br>Divide clk_matrix_700m_src by (div_con + 1). |

**CRU_CLKSEL_CON07**

Address: Operational Base + offset (0x031C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | clk_matrix_1200m_src_sel<br>clk_matrix_1200m_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 11:7 | RW | 0x00 | clk_matrix_1200m_src_div<br>Divide clk_matrix_1200m_src by (div_con + 1). |
| 6:5 | RW | 0x1 | clk_matrix_1000m_src_sel<br>clk_matrix_1000m_src clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_npll_mux<br>2'b11: clk_v0pll_mux |
| 4:0 | RW | 0x00 | clk_matrix_1000m_src_div<br>NP5 division register.<br>Divide clk_matrix_1000m_src by ((2 * div_con + 3) / 2). |

**CRU_CLKSEL_CON08**

Address: Operational Base + offset (0x0320)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | aclk_low_top_root_sel<br>aclk_low_top_root clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 13:9 | RW | 0x02 | aclk_low_top_root_div<br>Divide aclk_low_top_root by (div_con + 1). |
| 8:7 | RW | 0x0 | pclk_top_root_sel<br>pclk_top_root clock mux.<br>2'b00: clk_matrix_100m_src<br>2'b01: clk_matrix_50m_src<br>2'b10: xin_osc0_func |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6:5 | RW | 0x1 | aclk_top_root_sel<br>aclk_top_root clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_aupll_mux |
| 4:0 | RW | 0x01 | aclk_top_root_div<br>Divide aclk_top_root by (div_con + 1). |

**CRU_CLKSEL_CON09**

Address: Operational Base + offset (0x0324)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9:8 | RW | 0x0 | aclk_top_s400_root_sel<br>aclk_top_s400_root clock mux.<br>2'b00: clk_matrix_400m_src<br>2'b01: clk_matrix_200m_src<br>2'b10: clk_matrix_100m_src<br>2'b11: xin_osc0_func |
| 7:6 | RW | 0x0 | aclk_top_s200_root_sel<br>aclk_top_s200_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |
| 5:4 | RW | 0x0 | aclk_top_m400_root_sel<br>aclk_top_m400_root clock mux.<br>2'b00: clk_matrix_400m_src<br>2'b01: clk_matrix_200m_src<br>2'b10: clk_matrix_100m_src<br>2'b11: xin_osc0_func |
| 3:2 | RW | 0x0 | aclk_top_m500_root_sel<br>aclk_top_m500_root clock mux.<br>2'b00: clk_matrix_500m_src<br>2'b01: clk_matrix_300m_src<br>2'b10: clk_matrix_100m_src<br>2'b11: xin_osc0_func |
| 1:0 | RW | 0x0 | aclk_top_m300_root_sel<br>aclk_top_m300_root clock mux.<br>2'b00: clk_matrix_300m_src<br>2'b01: clk_matrix_200m_src<br>2'b10: clk_matrix_100m_src<br>2'b11: xin_osc0_func |

**CRU_CLKSEL_CON10**

Address: Operational Base + offset (0x0328)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14:12 | RW | 0x3 | clk_testout_grp0_sel<br>clk_testout_grp0 clock mux.<br>3'b000: clk_ref_pipe_phy0<br>3'b001: clk_ref_pipe_phy1<br>3'b010: clk_ref_pipe_phy2<br>3'b011: clk_testout_top<br>3'b100: clk_testout_gpu<br>3'b101: clk_testout_npu |
| 11:9 | RW | 0x0 | clk_testout_sel<br>clk_testout clock mux.<br>3'b000: clk_testout_grp0<br>3'b001: clk_testout_b0<br>3'b010: clk_testout_b1<br>3'b011: clk_testout_l<br>3'b100: clk_testout_ddr01<br>3'b101: clk_testout_ddr23 |
| 8:6 | RW | 0x3 | clk_testout_top_sel<br>clk_testout_top clock mux.<br>3'b000: clk_gpll_mux<br>3'b001: clk_cpll_mux<br>3'b010: clk_aupll_mux<br>3'b011: clk_spll_mux<br>3'b100: clk_v0pll_mux<br>3'b101: clk_deepslow |
| 5:0 | RW | 0x3f | clk_testout_top_div<br>Divide clk_testout_top by (div_con + 1). |

**CRU_CLKSEL_CON15**

Address: Operational Base + offset (0x033C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | refclko25m_eth0_out_sel<br>refclko25m_eth0_out clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 14:8 | RW | 0x3b | refclko25m_eth0_out_div<br>Divide refclko25m_eth0_out by (div_con + 1). |
| 7 | RW | 0x1 | mclk_gmac0_out_sel<br>mclk_gmac0_out clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 6:0 | RW | 0x1d | mclk_gmac0_out_div<br>Divide mclk_gmac0_out by (div_con + 1). |

**CRU_CLKSEL_CON16**

Address: Operational Base + offset (0x0340)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x1 | refclko25m_eth1_out_sel<br>refclko25m_eth1_out clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 6:0 | RW | 0x3b | refclko25m_eth1_out_div<br>Divide refclko25m_eth1_out by (div_con + 1). |

**CRU_CLKSEL_CON17**

Address: Operational Base + offset (0x0344)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9:8 | RW | 0x2 | clk_cifout_out_sel<br>clk_cifout_out clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: xin_osc0_func<br>2'b11: clk_spll_mux |
| 7:0 | RW | 0x00 | clk_cifout_out_div<br>Divide clk_cifout_out by (div_con + 1). |

**CRU_CLKSEL_CON18**

Address: Operational Base + offset (0x0348)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9:8 | RW | 0x0 | clk_mipi_camaraout_m0_sel<br>clk_mipi_camaraout_m0 clock mux.<br>2'b00: xin_osc0_func<br>2'b01: clk_spll_mux<br>2'b10: clk_gpll_mux<br>2'b11: clk_cpll_mux |
| 7:0 | RW | 0x00 | clk_mipi_camaraout_m0_div<br>Divide clk_mipi_camaraout_m0 by (div_con + 1). |

**CRU_CLKSEL_CON19**

Address: Operational Base + offset (0x034C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9:8 | RW | 0x0 | clk_mipi_camaraout_m1_sel<br>clk_mipi_camaraout_m1 clock mux.<br>2'b00: xin_osc0_func<br>2'b01: clk_spll_mux<br>2'b10: clk_gpll_mux<br>2'b11: clk_cpll_mux |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:0 | RW | 0x00 | clk_mipi_camaraout_m1_div<br>Divide clk_mipi_camaraout_m1 by (div_con + 1). |

**CRU_CLKSEL_CON20**

Address: Operational Base + offset (0x0350)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9:8 | RW | 0x0 | clk_mipi_camaraout_m2_sel<br>clk_mipi_camaraout_m2 clock mux.<br>2'b00: xin_osc0_func<br>2'b01: clk_spll_mux<br>2'b10: clk_gpll_mux<br>2'b11: clk_cpll_mux |
| 7:0 | RW | 0x00 | clk_mipi_camaraout_m2_div<br>Divide clk_mipi_camaraout_m2 by (div_con + 1). |

**CRU_CLKSEL_CON21**

Address: Operational Base + offset (0x0354)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9:8 | RW | 0x0 | clk_mipi_camaraout_m3_sel<br>clk_mipi_camaraout_m3 clock mux.<br>2'b00: xin_osc0_func<br>2'b01: clk_spll_mux<br>2'b10: clk_gpll_mux<br>2'b11: clk_cpll_mux |
| 7:0 | RW | 0x00 | clk_mipi_camaraout_m3_div<br>Divide clk_mipi_camaraout_m3 by (div_con + 1). |

**CRU_CLKSEL_CON22**

Address: Operational Base + offset (0x0358)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9:8 | RW | 0x0 | clk_mipi_camaraout_m4_sel<br>clk_mipi_camaraout_m4 clock mux.<br>2'b00: xin_osc0_func<br>2'b01: clk_spll_mux<br>2'b10: clk_gpll_mux<br>2'b11: clk_cpll_mux |
| 7:0 | RW | 0x00 | clk_mipi_camaraout_m4_div<br>Divide clk_mipi_camaraout_m4 by (div_con + 1). |

**CRU_CLKSEL_CON24**

Rockchip Confidencial

Address: Operational Base + offset (0x0360)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | clk_i2s0_8ch_tx_src_sel<br>clk_i2s0_8ch_tx_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_aupll_mux |
| 8:4 | RW | 0x01 | clk_i2s0_8ch_tx_src_div<br>Divide clk_i2s0_8ch_tx_src by (div_con + 1). |
| 3:2 | RW | 0x0 | pclk_audio_root_sel<br>pclk_audio_root clock mux.<br>2'b00: clk_matrix_100m_src<br>2'b01: clk_matrix_50m_src<br>2'b10: xin_osc0_func |
| 1:0 | RW | 0x0 | hclk_audio_root_sel<br>hclk_audio_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |

**CRU_CLKSEL_CON25**

Address: Operational Base + offset (0x0364)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x03355460 | clk_i2s0_8ch_tx_frac_div<br>clk_i2s0_8ch_tx_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON26**

Address: Operational Base + offset (0x0368)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | clk_i2s0_8ch_rx_src_sel<br>clk_i2s0_8ch_rx_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_aupll_mux |
| 6:2 | RW | 0x01 | clk_i2s0_8ch_rx_src_div<br>Divide clk_i2s0_8ch_rx_src by (div_con + 1). |
| 1:0 | RW | 0x3 | mclk_i2s0_8ch_tx_sel<br>mclk_i2s0_8ch_tx clock mux.<br>2'b00: clk_i2s0_8ch_tx_src<br>2'b01: clk_i2s0_8ch_tx_frac<br>2'b10: i2s0_mclkin<br>2'b11: xin_osc0_half |

**CRU_CLKSEL_CON27**

Address: Operational Base + offset (0x036C)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x03355460 | clk_i2s0_8ch_rx_frac_div<br>clk_i2s0_8ch_rx_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON28**

Address: Operational Base + offset (0x0370)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | clk_i2s2_2ch_src_sel<br>clk_i2s2_2ch_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_aupll_mux |
| 8:4 | RW | 0x01 | clk_i2s2_2ch_src_div<br>Divide clk_i2s2_2ch_src by (div_con + 1). |
| 3:2 | RW | 0x2 | i2s0_8ch_mclkout_sel<br>i2s0_8ch_mclkout clock mux.<br>2'b00: mclk_i2s0_8ch_tx<br>2'b01: mclk_i2s0_8ch_rx<br>2'b10: xin_osc0_half |
| 1:0 | RW | 0x3 | mclk_i2s0_8ch_rx_sel<br>mclk_i2s0_8ch_rx clock mux.<br>2'b00: clk_i2s0_8ch_rx_src<br>2'b01: clk_i2s0_8ch_rx_frac<br>2'b10: i2s0_mclkin<br>2'b11: xin_osc0_half |

**CRU_CLKSEL_CON29**

Address: Operational Base + offset (0x0374)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x03355460 | clk_i2s2_2ch_frac_div<br>clk_i2s2_2ch_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON30**

Address: Operational Base + offset (0x0378)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | clk_i2s3_2ch_src_sel<br>clk_i2s3_2ch_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_aupll_mux |
| 7:3 | RW | 0x01 | clk_i2s3_2ch_src_div<br>Divide clk_i2s3_2ch_src by (div_con + 1). |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x1 | i2s2_2ch_mclkout_sel<br>i2s2_2ch_mclkout clock mux.<br>1'b0: mclk_i2s2_2ch<br>1'b1: xin_osc0_half |
| 1:0 | RW | 0x3 | mclk_i2s2_2ch_sel<br>mclk_i2s2_2ch clock mux.<br>2'b00: clk_i2s2_2ch_src<br>2'b01: clk_i2s2_2ch_frac<br>2'b10: i2s2_mclkin<br>2'b11: xin_osc0_half |

**CRU_CLKSEL_CON31**

Address: Operational Base + offset (0x037C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x03355460 | clk_i2s3_2ch_frac_div<br>clk_i2s3_2ch_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON32**

Address: Operational Base + offset (0x0380)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | clk_spdif0_src_sel<br>clk_spdif0_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_aupll_mux |
| 7:3 | RW | 0x01 | clk_spdif0_src_div<br>Divide clk_spdif0_src by (div_con + 1). |
| 2 | RW | 0x1 | i2s3_2ch_mclkout_sel<br>i2s3_2ch_mclkout clock mux.<br>1'b0: mclk_i2s3_2ch<br>1'b1: xin_osc0_half |
| 1:0 | RW | 0x3 | mclk_i2s3_2ch_sel<br>mclk_i2s3_2ch clock mux.<br>2'b00: clk_i2s3_2ch_src<br>2'b01: clk_i2s3_2ch_frac<br>2'b10: i2s3_mclkin<br>2'b11: xin_osc0_half |

**CRU_CLKSEL_CON33**

Address: Operational Base + offset (0x0384)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x03355460 | clk_spdif0_frac_div<br>clk_spdif0_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON34**

Address: Operational Base + offset (0x0388)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | clk_spdif1_src_sel<br>clk_spdif1_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_aupll_mux |
| 6:2 | RW | 0x01 | clk_spdif1_src_div<br>Divide clk_spdif1_src by (div_con + 1). |
| 1:0 | RW | 0x2 | mclk_spdif0_sel<br>mclk_spdif0 clock mux.<br>2'b00: clk_spdif0_src<br>2'b01: clk_spdif0_frac<br>2'b10: xin_osc0_half |

**CRU_CLKSEL_CON35**

Address: Operational Base + offset (0x038C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x03355460 | clk_spdif1_frac_div<br>clk_spdif1_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON36**

Address: Operational Base + offset (0x0390)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8:7 | RW | 0x1 | mclk_pdm1_sel<br>mclk_pdm1 clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_aupll_mux |
| 6:2 | RW | 0x04 | mclk_pdm1_div<br>Divide mclk_pdm1 by (div_con + 1). |
| 1:0 | RW | 0x2 | mclk_spdif1_sel<br>mclk_spdif1 clock mux.<br>2'b00: clk_spdif1_src<br>2'b01: clk_spdif1_frac<br>2'b10: xin_osc0_half |

**CRU_CLKSEL_CON38**

Address: Operational Base + offset (0x0398)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | clk_i2c8_sel<br>clk_i2c8 clock mux.<br>1'b0: clk_matrix_200m_src<br>1'b1: clk_matrix_100m_src |
| 12 | RW | 0x0 | clk_i2c7_sel<br>clk_i2c7 clock mux.<br>1'b0: clk_matrix_200m_src<br>1'b1: clk_matrix_100m_src |
| 11 | RW | 0x0 | clk_i2c6_sel<br>clk_i2c6 clock mux.<br>1'b0: clk_matrix_200m_src<br>1'b1: clk_matrix_100m_src |
| 10 | RW | 0x0 | clk_i2c5_sel<br>clk_i2c5 clock mux.<br>1'b0: clk_matrix_200m_src<br>1'b1: clk_matrix_100m_src |
| 9 | RW | 0x0 | clk_i2c4_sel<br>clk_i2c4 clock mux.<br>1'b0: clk_matrix_200m_src<br>1'b1: clk_matrix_100m_src |
| 8 | RW | 0x0 | clk_i2c3_sel<br>clk_i2c3 clock mux.<br>1'b0: clk_matrix_200m_src<br>1'b1: clk_matrix_100m_src |
| 7 | RW | 0x0 | clk_i2c2_sel<br>clk_i2c2 clock mux.<br>1'b0: clk_matrix_200m_src<br>1'b1: clk_matrix_100m_src |
| 6 | RW | 0x0 | clk_i2c1_sel<br>clk_i2c1 clock mux.<br>1'b0: clk_matrix_200m_src<br>1'b1: clk_matrix_100m_src |
| 5 | RW | 0x1 | aclk_bus_root_sel<br>aclk_bus_root clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 4:0 | RW | 0x03 | aclk_bus_root_div<br>Divide aclk_bus_root by (div_con + 1). |

**CRU_CLKSEL_CON39**

Address: Operational Base + offset (0x039C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | clk_can1_sel<br>clk_can1 clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 10:6 | RW | 0x0b | clk_can1_div<br>Divide clk_can1 by (div_con + 1). |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | clk_can0_sel<br>clk_can0 clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 4:0 | RW | 0x0b | clk_can0_div<br>Divide clk_can0 by (div_con + 1). |

**CRU_CLKSEL_CON40**

Address: Operational Base + offset (0x03A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | clk_saradc_sel<br>clk_saradc clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: xin_osc0_func |
| 13:6 | RW | 0x3b | clk_saradc_div<br>Divide clk_saradc by (div_con + 1). |
| 5 | RW | 0x0 | clk_can2_sel<br>clk_can2 clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 4:0 | RW | 0x0b | clk_can2_div<br>Divide clk_can2 by (div_con + 1). |

**CRU_CLKSEL_CON41**

Address: Operational Base + offset (0x03A4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | clk_uart1_src_sel<br>clk_uart1_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 13:9 | RW | 0x01 | clk_uart1_src_div<br>Divide clk_uart1_src by (div_con + 1). |
| 8 | RW | 0x1 | clk_tsadc_sel<br>clk_tsadc clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: xin_osc0_func |
| 7:0 | RW | 0x0b | clk_tsadc_div<br>Divide clk_tsadc by (div_con + 1). |

**CRU_CLKSEL_CON42**

Address: Operational Base + offset (0x03A8)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x001403de | clk_uart1_frac_div<br>clk_uart1_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON43**

Address: Operational Base + offset (0x03AC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | clk_uart2_src_sel<br>clk_uart2_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 6:2 | RW | 0x01 | clk_uart2_src_div<br>Divide clk_uart2_src by (div_con + 1). |
| 1:0 | RW | 0x2 | sclk_uart1_sel<br>sclk_uart1 clock mux.<br>2'b00: clk_uart1_src<br>2'b01: clk_uart1_frac<br>2'b10: xin_osc0_func |

**CRU_CLKSEL_CON44**

Address: Operational Base + offset (0x03B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x001403de | clk_uart2_frac_div<br>clk_uart2_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON45**

Address: Operational Base + offset (0x03B4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | clk_uart3_src_sel<br>clk_uart3_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 6:2 | RW | 0x01 | clk_uart3_src_div<br>Divide clk_uart3_src by (div_con + 1). |
| 1:0 | RW | 0x2 | sclk_uart2_sel<br>sclk_uart2 clock mux.<br>2'b00: clk_uart2_src<br>2'b01: clk_uart2_frac<br>2'b10: xin_osc0_func |

**CRU_CLKSEL_CON46**

Address: Operational Base + offset (0x03B8)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x001403de | clk_uart3_frac_div<br>clk_uart3_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON47**

Address: Operational Base + offset (0x03BC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | clk_uart4_src_sel<br>clk_uart4_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 6:2 | RW | 0x01 | clk_uart4_src_div<br>Divide clk_uart4_src by (div_con + 1). |
| 1:0 | RW | 0x2 | sclk_uart3_sel<br>sclk_uart3 clock mux.<br>2'b00: clk_uart3_src<br>2'b01: clk_uart3_frac<br>2'b10: xin_osc0_func |

**CRU_CLKSEL_CON48**

Address: Operational Base + offset (0x03C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x001403de | clk_uart4_frac_div<br>clk_uart4_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON49**

Address: Operational Base + offset (0x03C4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | clk_uart5_src_sel<br>clk_uart5_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 6:2 | RW | 0x01 | clk_uart5_src_div<br>Divide clk_uart5_src by (div_con + 1). |
| 1:0 | RW | 0x2 | sclk_uart4_sel<br>sclk_uart4 clock mux.<br>2'b00: clk_uart4_src<br>2'b01: clk_uart4_frac<br>2'b10: xin_osc0_func |

**CRU_CLKSEL_CON50**

Address: Operational Base + offset (0x03C8)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x001403de | clk_uart5_frac_div<br>clk_uart5_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON51**

Address: Operational Base + offset (0x03CC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | clk_uart6_src_sel<br>clk_uart6_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 6:2 | RW | 0x01 | clk_uart6_src_div<br>Divide clk_uart6_src by (div_con + 1). |
| 1:0 | RW | 0x2 | sclk_uart5_sel<br>sclk_uart5 clock mux.<br>2'b00: clk_uart5_src<br>2'b01: clk_uart5_frac<br>2'b10: xin_osc0_func |

**CRU_CLKSEL_CON52**

Address: Operational Base + offset (0x03D0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x001403de | clk_uart6_frac_div<br>clk_uart6_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON53**

Address: Operational Base + offset (0x03D4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | clk_uart7_src_sel<br>clk_uart7_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 6:2 | RW | 0x01 | clk_uart7_src_div<br>Divide clk_uart7_src by (div_con + 1). |
| 1:0 | RW | 0x2 | sclk_uart6_sel<br>sclk_uart6 clock mux.<br>2'b00: clk_uart6_src<br>2'b01: clk_uart6_frac<br>2'b10: xin_osc0_func |

**CRU_CLKSEL_CON54**

Address: Operational Base + offset (0x03D8)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x001403de | clk_uart7_frac_div<br>clk_uart7_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON55**

Address: Operational Base + offset (0x03DC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | clk_uart8_src_sel<br>clk_uart8_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 6:2 | RW | 0x01 | clk_uart8_src_div<br>Divide clk_uart8_src by (div_con + 1). |
| 1:0 | RW | 0x2 | sclk_uart7_sel<br>sclk_uart7 clock mux.<br>2'b00: clk_uart7_src<br>2'b01: clk_uart7_frac<br>2'b10: xin_osc0_func |

**CRU_CLKSEL_CON56**

Address: Operational Base + offset (0x03E0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x001403de | clk_uart8_frac_div<br>clk_uart8_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON57**

Address: Operational Base + offset (0x03E4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | clk_uart9_src_sel<br>clk_uart9_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 6:2 | RW | 0x01 | clk_uart9_src_div<br>Divide clk_uart9_src by (div_con + 1). |
| 1:0 | RW | 0x2 | sclk_uart8_sel<br>sclk_uart8 clock mux.<br>2'b00: clk_uart8_src<br>2'b01: clk_uart8_frac<br>2'b10: xin_osc0_func |

**CRU_CLKSEL_CON58**

Address: Operational Base + offset (0x03E8)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x001403de | clk_uart9_frac_div<br>clk_uart9_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON59**

Address: Operational Base + offset (0x03EC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x2 | clk_pwm2_sel<br>clk_pwm2 clock mux.<br>2'b00: clk_matrix_100m_src<br>2'b01: clk_matrix_50m_src<br>2'b10: xin_osc0_func |
| 13:12 | RW | 0x2 | clk_pwm1_sel<br>clk_pwm1 clock mux.<br>2'b00: clk_matrix_100m_src<br>2'b01: clk_matrix_50m_src<br>2'b10: xin_osc0_func |
| 11:10 | RW | 0x0 | clk_spi4_sel<br>clk_spi4 clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_150m_src<br>2'b10: xin_osc0_func |
| 9:8 | RW | 0x0 | clk_spi3_sel<br>clk_spi3 clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_150m_src<br>2'b10: xin_osc0_func |
| 7:6 | RW | 0x0 | clk_spi2_sel<br>clk_spi2 clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_150m_src<br>2'b10: xin_osc0_func |
| 5:4 | RW | 0x0 | clk_spi1_sel<br>clk_spi1 clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_150m_src<br>2'b10: xin_osc0_func |
| 3:2 | RW | 0x0 | clk_spi0_sel<br>clk_spi0 clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_150m_src<br>2'b10: xin_osc0_func |
| 1:0 | RW | 0x2 | sclk_uart9_sel<br>sclk_uart9 clock mux.<br>2'b00: clk_uart9_src<br>2'b01: clk_uart9_frac<br>2'b10: xin_osc0_func |

**CRU_CLKSEL_CON60**

Address: Operational Base + offset (0x03F0)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | dbclk_gpio2_sel<br>dbclk_gpio2 clock mux.<br>1'b0: xin_osc0_func<br>1'b1: clk_deepslow |
| 13:9 | RW | 0x01 | dbclk_gpio2_div<br>Divide dbclk_gpio2 by (div_con + 1). |
| 8 | RW | 0x0 | dbclk_gpio1_sel<br>dbclk_gpio1 clock mux.<br>1'b0: xin_osc0_func<br>1'b1: clk_deepslow |
| 7:3 | RW | 0x01 | dbclk_gpio1_div<br>Divide dbclk_gpio1 by (div_con + 1). |
| 2 | RW | 0x0 | clk_bus_timer_root_sel<br>clk_bus_timer_root clock mux.<br>1'b0: xin_osc0_func<br>1'b1: clk_matrix_100m_src |
| 1:0 | RW | 0x2 | clk_pwm3_sel<br>clk_pwm3 clock mux.<br>2'b00: clk_matrix_100m_src<br>2'b01: clk_matrix_50m_src<br>2'b10: xin_osc0_func |

**CRU_CLKSEL_CON61**

Address: Operational Base + offset (0x03F4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | dbclk_gpio4_sel<br>dbclk_gpio4 clock mux.<br>1'b0: xin_osc0_func<br>1'b1: clk_deepslow |
| 10:6 | RW | 0x01 | dbclk_gpio4_div<br>Divide dbclk_gpio4 by (div_con + 1). |
| 5 | RW | 0x0 | dbclk_gpio3_sel<br>dbclk_gpio3 clock mux.<br>1'b0: xin_osc0_func<br>1'b1: clk_deepslow |
| 4:0 | RW | 0x01 | dbclk_gpio3_div<br>Divide dbclk_gpio3 by (div_con + 1). |

**CRU_CLKSEL_CON62**

Address: Operational Base + offset (0x03F8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:11 | RO | 0x00 | reserved |
| 10:6 | RW | 0x0f | clk_bisrintf_pllsrc_div<br>Divide clk_bisrintf_pllsrc by (div_con + 1). |
| 5 | RW | 0x1 | dclk_decom_sel<br>dclk_decom clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_spll_mux |
| 4:0 | RW | 0x01 | dclk_decom_div<br>Divide dclk_decom by (div_con + 1). |

**CRU_CLKSEL_CON63**

Address: Operational Base + offset (0x03FC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x0 | clk_testout_ddr01_sel<br>clk_testout_ddr01 clock mux.<br>1'b0: clk_dfi_ch0<br>1'b1: clk_dfi_ch1 |
| 5:0 | RW | 0x3f | clk_testout_ddr01_div<br>Divide clk_testout_ddr01 by (div_con + 1). |

**CRU_CLKSEL_CON65**

Address: Operational Base + offset (0x0404)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x0 | clk_testout_ddr23_sel<br>clk_testout_ddr23 clock mux.<br>1'b0: clk_dfi_ch2<br>1'b1: clk_dfi_ch3 |
| 5:0 | RW | 0x3f | clk_testout_ddr23_div<br>Divide clk_testout_ddr23 by (div_con + 1). |

**CRU_CLKSEL_CON67**

Address: Operational Base + offset (0x040C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x3 | clk_isp1_core_sel<br>clk_isp1_core clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_aupll_mux<br>2'b11: clk_spll_mux |
| 13:9 | RW | 0x00 | clk_isp1_core_div<br>Divide clk_isp1_core by (div_con + 1). |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8:7 | RW | 0x0 | hclk_isp1_root_sel<br>hclk_isp1_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |
| 6:5 | RW | 0x1 | aclk_isp1_root_sel<br>aclk_isp1_root clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_aupll_mux<br>2'b11: clk_spll_mux |
| 4:0 | RW | 0x01 | aclk_isp1_root_div<br>Divide aclk_isp1_root by (div_con + 1). |

**CRU_CLKSEL_CON73**

Address: Operational Base + offset (0x0424)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | clk_testout_npu_sel<br>clk_testout_npu clock mux.<br>1'b0: clk_rknn_dsu0_src_t<br>1'b1: clk_npu_pvtpll |
| 14:10 | RW | 0x1f | clk_testout_npu_div<br>Divide clk_testout_npu by (div_con + 1). |
| 9:7 | RW | 0x1 | clk_rknn_dsu0_src_t_sel<br>clk_rknn_dsu0_src_t clock mux.<br>3'b000: clk_gpll_mux<br>3'b001: clk_cpll_mux<br>3'b010: clk_aupll_mux<br>3'b011: clk_npll_mux<br>3'b100: clk_spll_mux |
| 6:2 | RW | 0x01 | clk_rknn_dsu0_src_t_div<br>Divide clk_rknn_dsu0_src_t by (div_con + 1). |
| 1:0 | RW | 0x0 | hclk_rknn_root_sel<br>hclk_rknn_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |

**CRU_CLKSEL_CON74**

Address: Operational Base + offset (0x0428)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x1 | clk_npu_cm0_rtc_sel<br>clk_npu_cm0_rtc clock mux.<br>1'b0: xin_osc0_func<br>1'b1: clk_deepslow |
| 11:7 | RW | 0x00 | clk_npu_cm0_rtc_div<br>Divide clk_npu_cm0_rtc by (div_con + 1). |
| 6:5 | RW | 0x0 | hclk_npu_cm0_root_sel<br>hclk_npu_cm0_root clock mux.<br>2'b00: clk_matrix_400m_src<br>2'b01: clk_matrix_200m_src<br>2'b10: clk_matrix_100m_src<br>2'b11: xin_osc0_func |
| 4 | RW | 0x1 | clk_npu_pvtpll_sel<br>clk_npu_pvtpll clock mux.<br>1'b0: clk_rknn_dsu0_src_t<br>1'b1: xin_osc0_func |
| 3 | RW | 0x0 | clk_nputimer_root_sel<br>clk_nputimer_root clock mux.<br>1'b0: xin_osc0_func<br>1'b1: clk_matrix_100m_src |
| 2:1 | RW | 0x0 | pclk_nputop_root_sel<br>pclk_nputop_root clock mux.<br>2'b00: clk_matrix_100m_src<br>2'b01: clk_matrix_50m_src<br>2'b10: xin_osc0_func |
| 0 | RW | 0x0 | clk_rknn_dsu0_sel<br>clk_rknn_dsu0 clock mux.<br>1'b0: clk_rknn_dsu0_src_t<br>1'b1: clk_npu_pvtpll |

**CRU_CLKSEL_CON77**

Address: Operational Base + offset (0x0434)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | cclk_emmc_sel<br>cclk_emmc clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: xin_osc0_func |
| 13:8 | RW | 0x05 | cclk_emmc_div<br>DT50 division register.<br>Divide cclk_emmc by (div_con + 1). |
| 7 | RW | 0x1 | aclk_nvm_root_sel<br>aclk_nvm_root clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 6:2 | RW | 0x04 | aclk_nvm_root_div<br>Divide aclk_nvm_root by (div_con + 1). |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1:0 | RW | 0x0 | hclk_nvm_root_sel<br>hclk_nvm_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |

**CRU_CLKSEL_CON78**

Address: Operational Base + offset (0x0438)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13:12 | RW | 0x0 | sclk_sfc_sel<br>sclk_sfc clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: xin_osc0_func |
| 11:6 | RW | 0x05 | sclk_sfc_div<br>Divide sclk_sfc by (div_con + 1). |
| 5 | RW | 0x1 | bclk_emmc_sel<br>bclk_emmc clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 4:0 | RW | 0x04 | bclk_emmc_div<br>Divide bclk_emmc by (div_con + 1). |

**CRU_CLKSEL_CON80**

Address: Operational Base + offset (0x0440)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | aclk_php_root_sel<br>aclk_php_root clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 12:8 | RW | 0x02 | aclk_php_root_div<br>Divide aclk_php_root by (div_con + 1). |
| 7 | RW | 0x1 | aclk_pcie_root_sel<br>aclk_pcie_root clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 6:2 | RW | 0x02 | aclk_pcie_root_div<br>Divide aclk_pcie_root by (div_con + 1). |
| 1:0 | RW | 0x0 | pclk_php_root_sel<br>pclk_php_root clock mux.<br>2'b00: clk_matrix_150m_src<br>2'b01: clk_matrix_50m_src<br>2'b10: xin_osc0_func |

Rockchip Confidencial

**CRU_CLKSEL_CON81**

Address: Operational Base + offset (0x0444)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | clk_gmac1_ptp_ref_sel<br>clk_gmac1_ptp_ref clock mux.<br>1'b0: clk_cpll_mux<br>1'b1: clk_gmac1_ptprefo |
| 12:7 | RW | 0x0e | clk_gmac1_ptp_ref_div<br>Divide clk_gmac1_ptp_ref by (div_con + 1). |
| 6 | RW | 0x0 | clk_gmac0_ptp_ref_sel<br>clk_gmac0_ptp_ref clock mux.<br>1'b0: clk_cpll_mux<br>1'b1: clk_gmac0_ptprefo |
| 5:0 | RW | 0x0e | clk_gmac0_ptp_ref_div<br>Divide clk_gmac0_ptp_ref by (div_con + 1). |

**CRU_CLKSEL_CON82**

Address: Operational Base + offset (0x0448)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | clk_rxoob1_sel<br>clk_rxoob1 clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 14:8 | RW | 0x1d | clk_rxoob1_div<br>Divide clk_rxoob1 by (div_con + 1). |
| 7 | RW | 0x1 | clk_rxoob0_sel<br>clk_rxoob0 clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 6:0 | RW | 0x1d | clk_rxoob0_div<br>Divide clk_rxoob0 by (div_con + 1). |

**CRU_CLKSEL_CON83**

Address: Operational Base + offset (0x044C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | clk_gmac_125m_cru_i_sel<br>clk_gmac_125m_cru_i clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 14:8 | RW | 0x0b | clk_gmac_125m_cru_i_div<br>Divide clk_gmac_125m_cru_i by (div_con + 1). |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x1 | clk_rxoob2_sel<br>clk_rxoob2 clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 6:0 | RW | 0x1d | clk_rxoob2_div<br>Divide clk_rxoob2 by (div_con + 1). |

**CRU_CLKSEL_CON84**

Address: Operational Base + offset (0x0450)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13:12 | RW | 0x0 | clk_utmi_otg2_sel<br>clk_utmi_otg2 clock mux.<br>2'b00: clk_matrix_150m_src<br>2'b01: clk_matrix_50m_src<br>2'b10: xin_osc0_func |
| 11:8 | RW | 0x4 | clk_utmi_otg2_div<br>Divide clk_utmi_otg2 by (div_con + 1). |
| 7 | RW | 0x1 | clk_gmac_50m_cru_i_sel<br>clk_gmac_50m_cru_i clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 6:0 | RW | 0x1d | clk_gmac_50m_cru_i_div<br>Divide clk_gmac_50m_cru_i by (div_con + 1). |

**CRU_CLKSEL_CON85**

Address: Operational Base + offset (0x0454)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11:6 | RW | 0x00 | clk_gmac1_tx_125m_o_div<br>Divide clk_gmac1_tx_125m_o by (div_con + 1). |
| 5:0 | RW | 0x00 | clk_gmac0_tx_125m_o_div<br>Divide clk_gmac0_tx_125m_o by (div_con + 1). |

**CRU_CLKSEL_CON89**

Address: Operational Base + offset (0x0464)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x2 | aclk_rkvdec_ccu_sel<br>aclk_rkvdec_ccu clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_aupll_mux<br>2'b11: clk_spll_mux |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:9 | RW | 0x00 | aclk_rkvdec_ccu_div<br>Divide aclk_rkvdec_ccu by (div_con + 1). |
| 8:7 | RW | 0x2 | aclk_rkvdec0_root_sel<br>aclk_rkvdec0_root clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_aupll_mux<br>2'b11: clk_spll_mux |
| 6:2 | RW | 0x00 | aclk_rkvdec0_root_div<br>Divide aclk_rkvdec0_root by (div_con + 1). |
| 1:0 | RW | 0x0 | hclk_rkvdec0_root_sel<br>hclk_rkvdec0_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |

**CRU_CLKSEL_CON90**

Address: Operational Base + offset (0x0468)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12:11 | RW | 0x3 | clk_rkvdec0_hevc_ca_sel<br>clk_rkvdec0_hevc_ca clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_npll_mux<br>2'b11: clk_matrix_1000m_src |
| 10:6 | RW | 0x00 | clk_rkvdec0_hevc_ca_div<br>Divide clk_rkvdec0_hevc_ca by (div_con + 1). |
| 5 | RW | 0x0 | clk_rkvdec0_ca_sel<br>clk_rkvdec0_ca clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 4:0 | RW | 0x01 | clk_rkvdec0_ca_div<br>Divide clk_rkvdec0_ca by (div_con + 1). |

**CRU_CLKSEL_CON91**

Address: Operational Base + offset (0x046C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x0 | clk_rkvdec0_core_sel<br>clk_rkvdec0_core clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 4:0 | RW | 0x01 | clk_rkvdec0_core_div<br>Divide clk_rkvdec0_core by (div_con + 1). |

Rockchip Confidencial

**CRU_CLKSEL_CON93**

Address: Operational Base + offset (0x0474)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | clk_rkvdec1_ca_sel<br>clk_rkvdec1_ca clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 13:9 | RW | 0x01 | clk_rkvdec1_ca_div<br>Divide clk_rkvdec1_ca by (div_con + 1). |
| 8:7 | RW | 0x2 | aclk_rkvdec1_root_sel<br>aclk_rkvdec1_root clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_aupll_mux<br>2'b11: clk_npll_mux |
| 6:2 | RW | 0x00 | aclk_rkvdec1_root_div<br>Divide aclk_rkvdec1_root by (div_con + 1). |
| 1:0 | RW | 0x0 | hclk_rkvdec1_root_sel<br>hclk_rkvdec1_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |

**CRU_CLKSEL_CON94**

Address: Operational Base + offset (0x0478)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | clk_rkvdec1_core_sel<br>clk_rkvdec1_core clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 11:7 | RW | 0x01 | clk_rkvdec1_core_div<br>Divide clk_rkvdec1_core by (div_con + 1). |
| 6:5 | RW | 0x3 | clk_rkvdec1_hevc_ca_sel<br>clk_rkvdec1_hevc_ca clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_npll_mux<br>2'b11: clk_matrix_1000m_src |
| 4:0 | RW | 0x00 | clk_rkvdec1_hevc_ca_div<br>Divide clk_rkvdec1_hevc_ca by (div_con + 1). |

**CRU_CLKSEL_CON96**

Address: Operational Base + offset (0x0480)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7:6 | RW | 0x0 | hclk_usb_root_sel<br>hclk_usb_root clock mux.<br>2'b00: clk_matrix_150m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |
| 5 | RW | 0x1 | aclk_usb_root_sel<br>aclk_usb_root clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 4:0 | RW | 0x04 | aclk_usb_root_div<br>Divide aclk_usb_root by (div_con + 1). |

**CRU_CLKSEL_CON98**

Address: Operational Base + offset (0x0488)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10:9 | RW | 0x0 | hclk_vdpu_root_sel<br>hclk_vdpu_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |
| 8:7 | RW | 0x0 | aclk_vdpu_low_root_sel<br>aclk_vdpu_low_root clock mux.<br>2'b00: clk_matrix_400m_src<br>2'b01: clk_matrix_200m_src<br>2'b10: clk_matrix_100m_src<br>2'b11: xin_osc0_func |
| 6:5 | RW | 0x1 | aclk_vdpu_root_sel<br>aclk_vdpu_root clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_aupll_mux |
| 4:0 | RW | 0x01 | aclk_vdpu_root_div<br>Divide aclk_vdpu_root by (div_con + 1). |

**CRU_CLKSEL_CON99**

Address: Operational Base + offset (0x048C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | clk_iep2p0_core_sel<br>clk_iep2p0_core clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 11:7 | RW | 0x02 | clk_iep2p0_core_div<br>Divide clk_iep2p0_core by (div_con + 1). |
| 6:5 | RW | 0x3 | aclk_jpeg_decoder_root_sel<br>aclk_jpeg_decoder_root clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_aupll_mux<br>2'b11: clk_spll_mux |
| 4:0 | RW | 0x00 | aclk_jpeg_decoder_root_div<br>Divide aclk_jpeg_decoder_root by (div_con + 1). |

**CRU_CLKSEL_CON100**

Address: Operational Base + offset (0x0490)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RW | 0x1 | clk_rga3_0_core_sel<br>clk_rga3_0_core clock mux.<br>3'b000: clk_gpll_mux<br>3'b001: clk_cpll_mux<br>3'b010: clk_npll_mux<br>3'b011: clk_aupll_mux<br>3'b100: clk_spll_mux |
| 12:8 | RW | 0x01 | clk_rga3_0_core_div<br>Divide clk_rga3_0_core by (div_con + 1). |
| 7:5 | RW | 0x1 | clk_rga2_core_sel<br>clk_rga2_core clock mux.<br>3'b000: clk_gpll_mux<br>3'b001: clk_cpll_mux<br>3'b010: clk_npll_mux<br>3'b011: clk_aupll_mux<br>3'b100: clk_spll_mux |
| 4:0 | RW | 0x01 | clk_rga2_core_div<br>Divide clk_rga2_core by (div_con + 1). |

**CRU_CLKSEL_CON102**

Address: Operational Base + offset (0x0498)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x2 | clk_rkvenc0_core_sel<br>clk_rkvenc0_core clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_aupll_mux<br>2'b11: clk_npll_mux |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:9 | RW | 0x00 | clk_rkvenc0_core_div<br>Divide clk_rkvenc0_core by (div_con + 1). |
| 8:7 | RW | 0x1 | aclk_rkvenc0_root_sel<br>aclk_rkvenc0_root clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_npll_mux |
| 6:2 | RW | 0x02 | aclk_rkvenc0_root_div<br>Divide aclk_rkvenc0_root by (div_con + 1). |
| 1:0 | RW | 0x0 | hclk_rkvenc0_root_sel<br>hclk_rkvenc0_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |

**CRU_CLKSEL_CON104**

Address: Operational Base + offset (0x04A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x2 | clk_rkvenc1_core_sel<br>clk_rkvenc1_core clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_aupll_mux<br>2'b11: clk_npll_mux |
| 13:9 | RW | 0x00 | clk_rkvenc1_core_div<br>Divide clk_rkvenc1_core by (div_con + 1). |
| 8:7 | RW | 0x1 | aclk_rkvenc1_root_sel<br>aclk_rkvenc1_root clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_npll_mux |
| 6:2 | RW | 0x02 | aclk_rkvenc1_root_div<br>Divide aclk_rkvenc1_root by (div_con + 1). |
| 1:0 | RW | 0x0 | hclk_rkvenc1_root_sel<br>hclk_rkvenc1_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |

**CRU_CLKSEL_CON106**

Address: Operational Base + offset (0x04A8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:10 | RW | 0x0 | pclk_vi_root_sel<br>pclk_vi_root clock mux.<br>2'b00: clk_matrix_100m_src<br>2'b01: clk_matrix_50m_src<br>2'b10: xin_osc0_func |
| 9:8 | RW | 0x0 | hclk_vi_root_sel<br>hclk_vi_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |
| 7:5 | RW | 0x1 | aclk_vi_root_sel<br>aclk_vi_root clock mux.<br>3'b000: clk_gpll_mux<br>3'b001: clk_cpll_mux<br>3'b010: clk_npll_mux<br>3'b011: clk_aupll_mux<br>3'b100: clk_spll_mux |
| 4:0 | RW | 0x01 | aclk_vi_root_div<br>Divide aclk_vi_root by (div_con + 1). |

**CRU_CLKSEL_CON107**

Address: Operational Base + offset (0x04AC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12:11 | RW | 0x3 | clk_isp0_core_sel<br>clk_isp0_core clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_aupll_mux<br>2'b11: clk_spll_mux |
| 10:6 | RW | 0x00 | clk_isp0_core_div<br>Divide clk_isp0_core by (div_con + 1). |
| 5 | RW | 0x0 | dclk_vicap_sel<br>dclk_vicap clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 4:0 | RW | 0x01 | dclk_vicap_div<br>Divide dclk_vicap by (div_con + 1). |

**CRU_CLKSEL_CON108**

Address: Operational Base + offset (0x04B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:14 | RW | 0x0 | iclk_csihost01_sel<br>iclk_csihost01 clock mux.<br>2'b00: clk_matrix_400m_src<br>2'b01: clk_matrix_200m_src<br>2'b10: clk_matrix_100m_src<br>2'b11: xin_osc0_func |
| 13:12 | RW | 0x3 | clk_fisheye1_core_sel<br>clk_fisheye1_core clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_aupll_mux<br>2'b11: clk_spll_mux |
| 11:7 | RW | 0x00 | clk_fisheye1_core_div<br>Divide clk_fisheye1_core by (div_con + 1). |
| 6:5 | RW | 0x3 | clk_fisheye0_core_sel<br>clk_fisheye0_core clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_aupll_mux<br>2'b11: clk_spll_mux |
| 4:0 | RW | 0x00 | clk_fisheye0_core_div<br>Divide clk_fisheye0_core by (div_con + 1). |

**CRU_CLKSEL_CON110**

Address: Operational Base + offset (0x04B8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13:12 | RW | 0x0 | pclk_vop_root_sel<br>pclk_vop_root clock mux.<br>2'b00: clk_matrix_100m_src<br>2'b01: clk_matrix_50m_src<br>2'b10: xin_osc0_func |
| 11:10 | RW | 0x0 | hclk_vop_root_sel<br>hclk_vop_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |
| 9:8 | RW | 0x0 | aclk_vop_low_root_sel<br>aclk_vop_low_root clock mux.<br>2'b00: clk_matrix_400m_src<br>2'b01: clk_matrix_200m_src<br>2'b10: clk_matrix_100m_src<br>2'b11: xin_osc0_func |
| 7:5 | RW | 0x2 | aclk_vop_root_sel<br>aclk_vop_root clock mux.<br>3'b000: clk_gpll_mux<br>3'b001: clk_cpll_mux<br>3'b010: clk_aupll_mux<br>3'b011: clk_npll_mux<br>3'b100: clk_spll_mux |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4:0 | RW | 0x00 | aclk_vop_root_div<br>Divide aclk_vop_root by (div_con + 1). |

**CRU_CLKSEL_CON111**

Address: Operational Base + offset (0x04BC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | dclk_vp1_src_sel<br>dclk_vp1_src clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_v0pll_mux<br>2'b11: clk_aupll_mux |
| 13:9 | RW | 0x01 | dclk_vp1_src_div<br>Divide dclk_vp1_src by (div_con + 1). |
| 8:7 | RW | 0x0 | dclk_vp0_src_sel<br>dclk_vp0_src clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_v0pll_mux<br>2'b11: clk_aupll_mux |
| 6:0 | RW | 0x01 | dclk_vp0_src_div<br>Divide dclk_vp0_src by (div_con + 1). |

**CRU_CLKSEL_CON112**

Address: Operational Base + offset (0x04C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12:11 | RW | 0x0 | dclk_vp2_sel<br>dclk_vp2 clock mux.<br>2'b00: dclk_vp2_src<br>2'b01: clk_hdmiphy_pixel0_o<br>2'b10: clk_hdmiphy_pixel1_o |
| 10:9 | RW | 0x0 | dclk_vp1_sel<br>dclk_vp1 clock mux.<br>2'b00: dclk_vp1_src<br>2'b01: clk_hdmiphy_pixel0_o<br>2'b10: clk_hdmiphy_pixel1_o |
| 8:7 | RW | 0x0 | dclk_vp0_sel<br>dclk_vp0 clock mux.<br>2'b00: dclk_vp0_src<br>2'b01: clk_hdmiphy_pixel0_o<br>2'b10: clk_hdmiphy_pixel1_o |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6:5 | RW | 0x0 | dclk_vp2_src_sel<br>dclk_vp2_src clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_v0pll_mux<br>2'b11: clk_aupll_mux |
| 4:0 | RW | 0x01 | dclk_vp2_src_div<br>Divide dclk_vop2_src by (div_con + 1). |

**CRU_CLKSEL_CON113**

Address: Operational Base + offset (0x04C4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8:7 | RW | 0x0 | dclk_vp3_sel<br>dclk_vp3 clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_v0pll_mux<br>2'b11: clk_aupll_mux |
| 6:0 | RW | 0x05 | dclk_vp3_div<br>Divide dclk_vp3 by (div_con + 1). |

**CRU_CLKSEL_CON114**

Address: Operational Base + offset (0x04C8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8:7 | RW | 0x3 | clk_dsihost0_sel<br>clk_dsihost0 clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_v0pll_mux<br>2'b11: clk_spll_mux |
| 6:0 | RW | 0x01 | clk_dsihost0_div<br>Divide clk_dsihost0 by (div_con + 1). |

**CRU_CLKSEL_CON115**

Address: Operational Base + offset (0x04CC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | aclk_vop_sub_src_sel<br>aclk_vop_sub_src clock mux.<br>1'b0: aclk_vop_root<br>1'b1: aclk_vop_div2_src |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8:7 | RW | 0x3 | clk_dsihost1_sel<br>clk_dsihost1 clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_v0pll_mux<br>2'b11: clk_spll_mux |
| 6:0 | RW | 0x01 | clk_dsihost1_div<br>Divide clk_dsihost1 by (div_con + 1). |

**CRU_CLKSEL_CON116**

Address: Operational Base + offset (0x04D0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13:12 | RW | 0x0 | pclk_vo0_s_root_sel<br>pclk_vo0_s_root clock mux.<br>2'b00: clk_matrix_100m_src<br>2'b01: clk_matrix_50m_src<br>2'b10: xin_osc0_func |
| 11:10 | RW | 0x0 | pclk_vo0_root_sel<br>pclk_vo0_root clock mux.<br>2'b00: clk_matrix_100m_src<br>2'b01: clk_matrix_50m_src<br>2'b10: xin_osc0_func |
| 9:8 | RW | 0x0 | hclk_vo0_s_root_sel<br>hclk_vo0_s_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |
| 7:6 | RW | 0x0 | hclk_vo0_root_sel<br>hclk_vo0_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |
| 5 | RW | 0x0 | aclk_vo0_root_sel<br>aclk_vo0_root clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 4:0 | RW | 0x02 | aclk_vo0_root_div<br>Divide aclk_vo0_root by (div_con + 1). |

**CRU_CLKSEL_CON117**

Address: Operational Base + offset (0x04D4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RW | 0x93 | clk_aux16mhz_1_div<br>Divide clk_aux16mhz_1 by (div_con + 1). |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:0 | RW | 0x93 | clk_aux16mhz_0_div<br>Divide clk_aux16mhz_0 by (div_con + 1). |

**CRU_CLKSEL_CON118**

Address: Operational Base + offset (0x04D8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x1 | clk_i2s4_8ch_tx_src_sel<br>clk_i2s4_8ch_tx_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_aupll_mux |
| 4:0 | RW | 0x0b | clk_i2s4_8ch_tx_src_div<br>Divide clk_i2s4_8ch_tx_src by (div_con + 1). |

**CRU_CLKSEL_CON119**

Address: Operational Base + offset (0x04DC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x03355460 | clk_i2s4_8ch_tx_frac_div<br>clk_i2s4_8ch_tx_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON120**

Address: Operational Base + offset (0x04E0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x1 | clk_i2s8_8ch_tx_src_sel<br>clk_i2s8_8ch_tx_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_aupll_mux |
| 7:3 | RW | 0x0b | clk_i2s8_8ch_tx_src_div<br>Divide clk_i2s8_8ch_tx_src by (div_con + 1). |
| 2 | RO | 0x0 | reserved |
| 1:0 | RW | 0x3 | mclk_i2s4_8ch_tx_sel<br>mclk_i2s4_8ch_tx clock mux.<br>2'b00: clk_i2s4_8ch_tx_src<br>2'b01: clk_i2s4_8ch_tx_frac<br>2'b10: i2s4_mclkin<br>2'b11: xin_osc0_half |

**CRU_CLKSEL_CON121**

Address: Operational Base + offset (0x04E4)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x03355460 | clk_i2s8_8ch_tx_frac_div<br>clk_i2s8_8ch_tx_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON122**

Address: Operational Base + offset (0x04E8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x1 | clk_spdif2_dp0_src_sel<br>clk_spdif2_dp0_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_aupll_mux |
| 7:3 | RW | 0x01 | clk_spdif2_dp0_src_div<br>Divide clk_spdif2_dp0_src by (div_con + 1). |
| 2 | RO | 0x0 | reserved |
| 1:0 | RW | 0x3 | mclk_i2s8_8ch_tx_sel<br>mclk_i2s8_8ch_tx clock mux.<br>2'b00: clk_i2s8_8ch_tx_src<br>2'b01: clk_i2s8_8ch_tx_frac<br>2'b10: i2s8_mclkin<br>2'b11: xin_osc0_half |

**CRU_CLKSEL_CON123**

Address: Operational Base + offset (0x04EC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x03355460 | clk_spdif2_dp0_frac_div<br>clk_spdif2_dp0_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON124**

Address: Operational Base + offset (0x04F0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x1 | clk_spdif5_dp1_src_sel<br>clk_spdif5_dp1_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_aupll_mux |
| 6:2 | RW | 0x01 | clk_spdif5_dp1_src_div<br>Divide clk_spdif5_dp1_src by (div_con + 1). |
| 1:0 | RW | 0x0 | mclk_4x_spdif2_dp0_sel<br>mclk_4x_spdif2_dp0 clock mux.<br>2'b00: clk_spdif2_dp0_src<br>2'b01: clk_spdif2_dp0_frac<br>2'b10: xin_osc0_half |

Rockchip Confidencial

**CRU_CLKSEL_CON125**

Address: Operational Base + offset (0x04F4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x03355460 | clk_spdif5_dp1_frac_div<br>clk_spdif5_dp1_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON126**

Address: Operational Base + offset (0x04F8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1:0 | RW | 0x0 | mclk_4x_spdif5_dp1_sel<br>mclk_4x_spdif5_dp1 clock mux.<br>2'b00: clk_spdif5_dp1_src<br>2'b01: clk_spdif5_dp1_frac<br>2'b10: xin_osc0_half |

**CRU_CLKSEL_CON128**

Address: Operational Base + offset (0x0500)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:13 | RW | 0x0 | hclk_vo1_root_sel<br>hclk_vo1_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |
| 12 | RW | 0x1 | aclk_hdmirx_root_sel<br>aclk_hdmirx_root clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 11:7 | RW | 0x02 | aclk_hdmirx_root_div<br>Divide aclk_hdmirx_root by (div_con + 1). |
| 6:5 | RW | 0x2 | aclk_hdcp1_root_sel<br>aclk_hdcp1_root clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_hdmitrx_refsrc |
| 4:0 | RW | 0x00 | aclk_hdcp1_root_div<br>Divide aclk_hdcp1_root by (div_con + 1). |

**CRU_CLKSEL_CON129**

Address: Operational Base + offset (0x0504)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | clk_i2s7_8ch_rx_src_sel<br>clk_i2s7_8ch_rx_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_aupll_mux |
| 10:6 | RW | 0x05 | clk_i2s7_8ch_rx_src_div<br>Divide clk_i2s7_8ch_rx_src by (div_con + 1). |
| 5:4 | RW | 0x0 | pclk_vo1_s_root_sel<br>pclk_vo1_s_root clock mux.<br>2'b00: clk_matrix_100m_src<br>2'b01: clk_matrix_50m_src<br>2'b10: xin_osc0_func |
| 3:2 | RW | 0x0 | pclk_vo1_root_sel<br>pclk_vo1_root clock mux.<br>2'b00: clk_matrix_150m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: xin_osc0_func |
| 1:0 | RW | 0x0 | hclk_vo1_s_root_sel<br>hclk_vo1_s_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |

**CRU_CLKSEL_CON130**

Address: Operational Base + offset (0x0508)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x03355460 | clk_i2s7_8ch_rx_frac_div<br>clk_i2s7_8ch_rx_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON131**

Address: Operational Base + offset (0x050C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1:0 | RW | 0x3 | mclk_i2s7_8ch_rx_sel<br>mclk_i2s7_8ch_rx clock mux.<br>2'b00: clk_i2s7_8ch_rx_src<br>2'b01: clk_i2s7_8ch_rx_frac<br>2'b10: i2s7_mclkin<br>2'b11: xin_osc0_half |

**CRU_CLKSEL_CON133**

Address: Operational Base + offset (0x0514)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x1 | clk_hdmitx0_earc_sel<br>clk_hdmitx0_earc clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 5:1 | RW | 0x0e | clk_hdmitx0_earc_div<br>Divide clk_hdmitx0_earc by (div_con + 1). |
| 0 | RO | 0x0 | reserved |

**CRU_CLKSEL_CON136**

Address: Operational Base + offset (0x0520)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x1 | clk_hdmitx1_earc_sel<br>clk_hdmitx1_earc clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 5:1 | RW | 0x0e | clk_hdmitx1_earc_div<br>Divide clk_hdmitx1_earc by (div_con + 1). |
| 0 | RO | 0x0 | reserved |

**CRU_CLKSEL_CON138**

Address: Operational Base + offset (0x0528)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | clk_hdmirx_aud_src_sel<br>clk_hdmirx_aud_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_aupll_mux |
| 7:0 | RW | 0x03 | clk_hdmirx_aud_src_div<br>Divide clk_hdmirx_aud_src by (div_con + 1). |

**CRU_CLKSEL_CON139**

Address: Operational Base + offset (0x052C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x03355460 | clk_hdmirx_aud_frac_div<br>clk_hdmirx_aud_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON140**

Address: Operational Base + offset (0x0530)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | clk_i2s5_8ch_tx_src_sel<br>clk_i2s5_8ch_tx_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_aupll_mux |
| 9:5 | RW | 0x05 | clk_i2s5_8ch_tx_src_div<br>Divide clk_i2s5_8ch_tx_src by (div_con + 1). |
| 4:3 | RW | 0x0 | clk_edp1_200m_sel<br>clk_edp1_200m clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |
| 2:1 | RW | 0x0 | clk_edp0_200m_sel<br>clk_edp0_200m clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |
| 0 | RW | 0x0 | clk_hdmirx_aud_sel<br>clk_hdmirx_aud clock mux.<br>1'b0: clk_hdmirx_aud_src<br>1'b1: clk_hdmirx_aud_frac |

**CRU_CLKSEL_CON141**

Address: Operational Base + offset (0x0534)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x03355460 | clk_i2s5_8ch_tx_frac_div<br>clk_i2s5_8ch_tx_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON142**

Address: Operational Base + offset (0x0538)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1:0 | RW | 0x3 | mclk_i2s5_8ch_tx_sel<br>mclk_i2s5_8ch_tx clock mux.<br>2'b00: clk_i2s5_8ch_tx_src<br>2'b01: clk_i2s5_8ch_tx_frac<br>2'b10: i2s5_mclkin<br>2'b11: xin_osc0_half |

**CRU_CLKSEL_CON144**

Address: Operational Base + offset (0x0540)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | clk_i2s6_8ch_tx_src_sel<br>clk_i2s6_8ch_tx_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_aupll_mux |
| 7:3 | RW | 0x05 | clk_i2s6_8ch_tx_src_div<br>Divide clk_i2s6_8ch_tx_src by (div_con + 1). |
| 2:0 | RO | 0x0 | reserved |

**CRU_CLKSEL_CON145**

Address: Operational Base + offset (0x0544)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x03355460 | clk_i2s6_8ch_tx_frac_div<br>clk_i2s6_8ch_tx_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON146**

Address: Operational Base + offset (0x0548)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | clk_i2s6_8ch_rx_src_sel<br>clk_i2s6_8ch_rx_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_aupll_mux |
| 6:2 | RW | 0x05 | clk_i2s6_8ch_rx_src_div<br>Divide clk_i2s6_8ch_rx_src by (div_con + 1). |
| 1:0 | RW | 0x3 | mclk_i2s6_8ch_tx_sel<br>mclk_i2s6_8ch_tx clock mux.<br>2'b00: clk_i2s6_8ch_tx_src<br>2'b01: clk_i2s6_8ch_tx_frac<br>2'b10: i2s6_mclkin<br>2'b11: xin_osc0_half |

**CRU_CLKSEL_CON147**

Address: Operational Base + offset (0x054C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x03355460 | clk_i2s6_8ch_rx_frac_div<br>clk_i2s6_8ch_rx_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON148**

Address: Operational Base + offset (0x0550)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | clk_spdif3_src_sel<br>clk_spdif3_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_aupll_mux |
| 8:4 | RW | 0x05 | clk_spdif3_src_div<br>Divide clk_spdif3_src by (div_con + 1). |
| 3:2 | RW | 0x2 | i2s6_8ch_mclkout_sel<br>i2s6_8ch_mclkout clock mux.<br>2'b00: mclk_i2s6_8ch_tx<br>2'b01: mclk_i2s6_8ch_rx<br>2'b10: xin_osc0_half |
| 1:0 | RW | 0x3 | mclk_i2s6_8ch_rx_sel<br>mclk_i2s6_8ch_rx clock mux.<br>2'b00: clk_i2s6_8ch_rx_src<br>2'b01: clk_i2s6_8ch_rx_frac<br>2'b10: i2s6_mclkin<br>2'b11: xin_osc0_half |

**CRU_CLKSEL_CON149**

Address: Operational Base + offset (0x0554)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x03355460 | clk_spdif3_frac_div<br>clk_spdif3_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON150**

Address: Operational Base + offset (0x0558)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | clk_spdif4_src_sel<br>clk_spdif4_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_aupll_mux |
| 6:2 | RW | 0x05 | clk_spdif4_src_div<br>Divide clk_spdif4_src by (div_con + 1). |
| 1:0 | RW | 0x0 | mclk_spdif3_sel<br>mclk_spdif3 clock mux.<br>2'b00: clk_spdif3_src<br>2'b01: clk_spdif3_frac<br>2'b10: xin_osc0_half |

**CRU_CLKSEL_CON151**

Address: Operational Base + offset (0x055C)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x03355460 | clk_spdif4_frac_div<br>clk_spdif4_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON152**

Address: Operational Base + offset (0x0560)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x1 | mclk_spdifrx1_sel<br>mclk_spdifrx1 clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_aupll_mux |
| 13:9 | RW | 0x02 | mclk_spdifrx1_div<br>Divide mclk_spdifrx1 by (div_con + 1). |
| 8:7 | RW | 0x1 | mclk_spdifrx0_sel<br>mclk_spdifrx0 clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_aupll_mux |
| 6:2 | RW | 0x02 | mclk_spdifrx0_div<br>Divide mclk_spdifrx0 by (div_con + 1). |
| 1:0 | RW | 0x0 | mclk_spdif4_sel<br>mclk_spdif4 clock mux.<br>2'b00: clk_spdif4_src<br>2'b01: clk_spdif4_frac<br>2'b10: xin_osc0_half |

**CRU_CLKSEL_CON153**

Address: Operational Base + offset (0x0564)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | clk_i2s9_8ch_rx_src_sel<br>clk_i2s9_8ch_rx_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_aupll_mux |
| 11:7 | RW | 0x05 | clk_i2s9_8ch_rx_src_div<br>Divide clk_i2s9_8ch_rx_src by (div_con + 1). |
| 6:5 | RW | 0x1 | mclk_spdifrx2_sel<br>mclk_spdifrx2 clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_aupll_mux |
| 4:0 | RW | 0x02 | mclk_spdifrx2_div<br>Divide mclk_spdifrx2 by (div_con + 1). |

**CRU_CLKSEL_CON154**

Rockchip Confidencial

Address: Operational Base + offset (0x0568)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x03355460 | clk_i2s9_8ch_rx_frac_div<br>clk_i2s9_8ch_rx_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON155**

Address: Operational Base + offset (0x056C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | clk_i2s10_8ch_rx_src_sel<br>clk_i2s10_8ch_rx_src clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_aupll_mux |
| 7:3 | RW | 0x05 | clk_i2s10_8ch_rx_src_div<br>Divide clk_i2s10_8ch_rx_src by (div_con + 1). |
| 2 | RO | 0x0 | reserved |
| 1:0 | RW | 0x3 | mclk_i2s9_8ch_rx_sel<br>mclk_i2s9_8ch_rx clock mux.<br>2'b00: clk_i2s9_8ch_rx_src<br>2'b01: clk_i2s9_8ch_rx_frac<br>2'b10: i2s9_mclkin<br>2'b11: xin_osc0_half |

**CRU_CLKSEL_CON156**

Address: Operational Base + offset (0x0570)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x03355460 | clk_i2s10_8ch_rx_frac_div<br>clk_i2s10_8ch_rx_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**CRU_CLKSEL_CON157**

Address: Operational Base + offset (0x0574)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x1 | clk_hdmitrx_refsrc_sel<br>clk_hdmitrx_refsrc clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 6:2 | RW | 0x02 | clk_hdmitrx_refsrc_div<br>NP5 division register.<br>Divide clk_hdmitrx_refsrc by ((2 * div_con + 3) / 2). |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1:0 | RW | 0x3 | mclk_i2s10_8ch_rx_sel<br>mclk_i2s10_8ch_rx clock mux.<br>2'b00: clk_i2s10_8ch_rx_src<br>2'b01: clk_i2s10_8ch_rx_frac<br>2'b10: i2s10_mclkin<br>2'b11: xin_osc0_half |

**CRU_CLKSEL_CON158**

Address: Operational Base + offset (0x0578)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | clk_gpu_src_sel<br>clk_gpu_src clock mux.<br>1'b0: clk_gpu_src_t<br>1'b1: clk_gpu_pvtpll |
| 13 | RW | 0x0 | clk_testout_gpu_sel<br>clk_testout_gpu clock mux.<br>1'b0: clk_gpu_src_t<br>1'b1: clk_gpu_pvtpll |
| 12:8 | RW | 0x1f | clk_testout_gpu_div<br>Divide clk_testout_gpu by (div_con + 1). |
| 7:5 | RW | 0x4 | clk_gpu_src_t_sel<br>clk_gpu_src_t clock mux.<br>3'b000: clk_gpll_mux<br>3'b001: clk_cpll_mux<br>3'b010: clk_aupll_mux<br>3'b011: clk_npll_mux<br>3'b100: clk_spll_mux |
| 4:0 | RW | 0x00 | clk_gpu_src_t_div<br>Divide clk_gpu_src_t by (div_con + 1). |

**CRU_CLKSEL_CON159**

Address: Operational Base + offset (0x057C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:10 | RW | 0x00 | aclk_m0_gpu_biu_div<br>Divide aclk_m0_gpu_biu by (div_con + 1). |
| 9:5 | RW | 0x00 | aclk_s_gpu_biu_div<br>Divide aclk_s_gpu_biu by (div_con + 1). |
| 4:0 | RW | 0x00 | clk_gpu_stacks_div<br>Divide clk_gpu_stacks by (div_con + 1). |

**CRU_CLKSEL_CON160**

Address: Operational Base + offset (0x0580)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:10 | RW | 0x00 | aclk_m3_gpu_biu_div<br>Divide aclk_m3_gpu_biu by (div_con + 1). |
| 9:5 | RW | 0x00 | aclk_m2_gpu_biu_div<br>Divide aclk_m2_gpu_biu by (div_con + 1). |
| 4:0 | RW | 0x00 | aclk_m1_gpu_biu_div<br>Divide aclk_m1_gpu_biu by (div_con + 1). |

**CRU_CLKSEL_CON161**

Address: Operational Base + offset (0x0584)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:3 | RO | 0x0000 | reserved |
| 2 | RW | 0x1 | clk_gpu_pvtpll_sel<br>clk_gpu_pvtpll clock mux.<br>1'b0: clk_gpu_src_t<br>1'b1: xin_osc0_func |
| 1:0 | RW | 0x0 | pclk_gpu_root_sel<br>pclk_gpu_root clock mux.<br>2'b00: clk_matrix_100m_src<br>2'b01: clk_matrix_50m_src<br>2'b10: xin_osc0_func |

**CRU_CLKSEL_CON163**

Address: Operational Base + offset (0x058C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8:7 | RW | 0x0 | pclk_av1_root_sel<br>pclk_av1_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |
| 6:5 | RW | 0x0 | aclk_av1_root_sel<br>aclk_av1_root clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_aupll_mux |
| 4:0 | RW | 0x02 | aclk_av1_root_div<br>Divide aclk_av1_root by (div_con + 1). |

**CRU_CLKSEL_CON165**

Address: Operational Base + offset (0x0594)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | clk_ddr_timer_root_sel<br>clk_ddr_timer_root clock mux.<br>1'b0: xin_osc0_func<br>1'b1: clk_matrix_100m_src |
| 11:10 | RW | 0x0 | aclk_center_s400_root_sel<br>aclk_center_s400_root clock mux.<br>2'b00: clk_matrix_400m_src<br>2'b01: clk_matrix_200m_src<br>2'b10: clk_matrix_100m_src<br>2'b11: xin_osc0_func |
| 9:8 | RW | 0x0 | aclk_center_s200_root_sel<br>aclk_center_s200_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |
| 7:6 | RW | 0x0 | pclk_center_root_sel<br>pclk_center_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |
| 5:4 | RW | 0x0 | hclk_center_root_sel<br>hclk_center_root clock mux.<br>2'b00: clk_matrix_400m_src<br>2'b01: clk_matrix_200m_src<br>2'b10: clk_matrix_100m_src<br>2'b11: xin_osc0_func |
| 3:2 | RW | 0x0 | aclk_center_low_root_sel<br>aclk_center_low_root clock mux.<br>2'b00: clk_matrix_500m_src<br>2'b01: clk_matrix_250m_src<br>2'b10: clk_matrix_100m_src<br>2'b11: xin_osc0_func |
| 1:0 | RW | 0x0 | aclk_center_root_sel<br>aclk_center_root clock mux.<br>2'b00: clk_matrix_700m_src<br>2'b01: clk_matrix_400m_src<br>2'b10: clk_matrix_200m_src<br>2'b11: xin_osc0_func |

**CRU_CLKSEL_CON166**

Address: Operational Base + offset (0x0598)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x1 | clk_ddr_cm0_rtc_sel<br>clk_ddr_cm0_rtc clock mux.<br>1'b0: xin_osc0_func<br>1'b1: clk_deepslow |
| 4:0 | RW | 0x00 | clk_ddr_cm0_rtc_div<br>Divide clk_ddr_cm0_rtc by (div_con + 1). |

**CRU_CLKSEL_CON170**

Address: Operational Base + offset (0x05A8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7:6 | RW | 0x0 | hclk_vo1usb_top_root_sel<br>hclk_vo1usb_top_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |
| 5 | RW | 0x1 | aclk_vo1usb_top_root_sel<br>aclk_vo1usb_top_root clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_cpll_mux |
| 4:0 | RW | 0x02 | aclk_vo1usb_top_root_div<br>Divide aclk_vo1usb_top_root by (div_con + 1). |

**CRU_CLKSEL_CON172**

Address: Operational Base + offset (0x05B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9:8 | RW | 0x0 | cclk_src_sdio_sel<br>cclk_src_sdio clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: xin_osc0_func |
| 7:2 | RW | 0x03 | cclk_src_sdio_div<br>DT50 division register.<br>Divide cclk_src_sdio by (div_con + 1). |
| 1:0 | RW | 0x0 | hclk_sdio_root_sel<br>hclk_sdio_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |

**CRU_CLKSEL_CON174**

Address: Operational Base + offset (0x05B8)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x1 | clk_rga3_1_core_sel<br>clk_rga3_1_core clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_aupll_mux<br>2'b11: clk_spll_mux |
| 13:9 | RW | 0x01 | clk_rga3_1_core_div<br>Divide clk_rga3_1_core by (div_con + 1). |
| 8:7 | RW | 0x0 | hclk_rga3_root_sel<br>hclk_rga3_root clock mux.<br>2'b00: clk_matrix_200m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |
| 6:5 | RW | 0x1 | aclk_rga3_root_sel<br>aclk_rga3_root clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_cpll_mux<br>2'b10: clk_aupll_mux |
| 4:0 | RW | 0x01 | aclk_rga3_root_div<br>Divide aclk_rga3_root by (div_con + 1). |

**CRU_CLKSEL_CON176**

Address: Operational Base + offset (0x05C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11:6 | RW | 0x00 | clk_ref_pipe_phy1_pll_src_div<br>Divide clk_ref_pipe_phy1_pll_src by (div_con + 1). |
| 5:0 | RW | 0x00 | clk_ref_pipe_phy0_pll_src_div<br>Divide clk_ref_pipe_phy0_pll_src by (div_con + 1). |

**CRU_CLKSEL_CON177**

Address: Operational Base + offset (0x05C4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | clk_ref_pipe_phy2_sel<br>clk_ref_pipe_phy2 clock mux.<br>1'b0: clk_ref_pipe_phy2_osc_src<br>1'b1: clk_ref_pipe_phy2_pll_src |
| 7 | RW | 0x0 | clk_ref_pipe_phy1_sel<br>clk_ref_pipe_phy1 clock mux.<br>1'b0: clk_ref_pipe_phy1_osc_src<br>1'b1: clk_ref_pipe_phy1_pll_src |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | clk_ref_pipe_phy0_sel<br>clk_ref_pipe_phy0 clock mux.<br>1'b0: clk_ref_pipe_phy0_osc_src<br>1'b1: clk_ref_pipe_phy0_pll_src |
| 5:0 | RW | 0x00 | clk_ref_pipe_phy2_pll_src_div<br>Divide clk_ref_pipe_phy2_pll_src by (div_con + 1). |

**CRU_GATE_CON00**

Address: Operational Base + offset (0x0800)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | clk_matrix_1200m_src_en<br>clk_matrix_1200m_src clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | clk_matrix_1000m_src_en<br>clk_matrix_1000m_src clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | clk_matrix_800m_src_en<br>clk_matrix_800m_src clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | clk_matrix_700m_src_en<br>clk_matrix_700m_src clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | clk_matrix_650m_src_en<br>clk_matrix_650m_src clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | clk_matrix_600m_src_en<br>clk_matrix_600m_src clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | clk_matrix_500m_src_en<br>clk_matrix_500m_src clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | clk_matrix_450m_src_en<br>clk_matrix_450m_src clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | clk_matrix_400m_src_en<br>clk_matrix_400m_src clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_matrix_350m_src_en<br>clk_matrix_350m_src clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | clk_matrix_300m_src_en<br>clk_matrix_300m_src clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | clk_matrix_250m_src_en<br>clk_matrix_250m_src clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | clk_matrix_200m_src_en<br>clk_matrix_200m_src clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | clk_matrix_150m_src_en<br>clk_matrix_150m_src clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_matrix_100m_src_en<br>clk_matrix_100m_src clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | clk_matrix_50m_src_en<br>clk_matrix_50m_src clock gating control.<br>When high, disable clock |

**CRU_GATE_CON01**

Address: Operational Base + offset (0x0804)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | aclk_top_m500_biu_en<br>aclk_top_m500_biu clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | aclk_top_s400_root_en<br>aclk_top_s400_root clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | aclk_top_s200_root_en<br>aclk_top_s200_root clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | aclk_top_m400_root_en<br>aclk_top_m400_root clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | aclk_top_m500_root_en<br>aclk_top_m500_root clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | aclk_top_m300_root_en<br>aclk_top_m300_root clock gating control.<br>When high, disable clock |
| 9 | RO | 0x0 | reserved |
| 8 | RW | 0x0 | pclk_csiphy1_en<br>pclk_csiphy1 clock gating control.<br>When high, disable clock |
| 7 | RO | 0x0 | reserved |
| 6 | RW | 0x0 | pclk_csiphy0_en<br>pclk_csiphy0 clock gating control.<br>When high, disable clock |
| 5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | pclk_top_biu_en<br>pclk_top_biu clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | aclk_top_biu_en<br>aclk_top_biu clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | aclk_low_top_root_en<br>aclk_low_top_root clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | pclk_top_root_en<br>pclk_top_root clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | aclk_top_root_en<br>aclk_top_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON02**

Address: Operational Base + offset (0x0808)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | clk_usbdp_combo_phy1_immortal_en<br>clk_usbdp_combo_phy1_immortal clock gating control.<br>When high, disable clock |
| 14:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | clk_usbdp_combo_phy0_immortal_en<br>clk_usbdp_combo_phy0_immortal clock gating control.<br>When high, disable clock |
| 7 | RO | 0x0 | reserved |
| 6 | RW | 0x1 | clk_testout_grp0_en<br>clk_testout_grp0 clock gating control.<br>When high, disable clock |
| 5 | RO | 0x0 | reserved |
| 4 | RW | 0x1 | clk_testout_top_en<br>clk_testout_top clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | aclk_top_m300_biu_en<br>aclk_top_m300_biu clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | aclk_top_s400_biu_en<br>aclk_top_s400_biu clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | aclk_top_s200_biu_en<br>aclk_top_s200_biu clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | aclk_top_m400_biu_en<br>aclk_top_m400_biu clock gating control.<br>When high, disable clock |

**CRU_GATE_CON03**

Address: Operational Base + offset (0x080C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pclk_mipi_dcphy0_grf_en<br>pclk_mipi_dcphy0_grf clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | pclk_mipi_dcphy0_en<br>pclk_mipi_dcphy0 clock gating control.<br>When high, disable clock |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:0 | RO | 0x0000 | reserved |

**CRU_GATE_CON04**

Address: Operational Base + offset (0x0810)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | pclk_apb2asb_slv_ioc_right_en<br>pclk_apb2asb_slv_ioc_right clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | pclk_apb2asb_slv_ioc_top_en<br>pclk_apb2asb_slv_ioc_top clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | pclk_apb2asb_slv_emmcio_en<br>pclk_apb2asb_slv_emmcio clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | pclk_apb2asb_slv_vccio6_en<br>pclk_apb2asb_slv_vccio6 clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | pclk_apb2asb_slv_vccio3_5_en<br>pclk_apb2asb_slv_vccio3_5 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | pclk_apb2asb_slv_csiphy_en<br>pclk_apb2asb_slv_csiphy clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | pclk_apb2asb_slv_cdphy_en<br>pclk_apb2asb_slv_cdphy clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_mipi_dcphy1_grf_en<br>pclk_mipi_dcphy1_grf clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_mipi_dcphy1_en<br>pclk_mipi_dcphy1 clock gating control.<br>When high, disable clock |
| 2:0 | RO | 0x0 | reserved |

**CRU_GATE_CON05**

Address: Operational Base + offset (0x0814)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | hclk_channel_secure2center_en<br>hclk_channel_secure2center clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | hclk_channel_secure2vo1usb_en<br>hclk_channel_secure2vo1usb clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | clk_mipi_cameraout_m4_en<br>clk_mipi_camaraout_m4 clock gating control.<br>When high, disable clock |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | clk_mipi_cameraout_m3_en<br>clk_mipi_camaraout_m3 clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | clk_mipi_cameraout_m2_en<br>clk_mipi_camaraout_m2 clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | clk_mipi_cameraout_m1_en<br>clk_mipi_camaraout_m1 clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | clk_mipi_cameraout_m0_en<br>clk_mipi_camaraout_m0 clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | aclk_channel_secure2center_en<br>aclk_channel_secure2center clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | aclk_channel_secure2vo1usb_en<br>aclk_channel_secure2vo1usb clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_cifout_out_en<br>clk_cifout_out clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | refclko25m_eth1_out_en<br>refclko25m_eth1_out clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | refclko25m_eth0_out_en<br>refclko25m_eth0_out clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | mclk_gmac0_out_en<br>mclk_gmac0_out clock gating control.<br>When high, disable clock |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | pclk_cru_en<br>pclk_cru clock gating control.<br>When high, disable clock |

**CRU_GATE_CON06**

Address: Operational Base + offset (0x0818)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | pclk_channel_secure2center_en<br>pclk_channel_secure2center clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | pclk_channel_secure2vo1usb_en<br>pclk_channel_secure2vo1usb clock gating control.<br>When high, disable clock |

**CRU_GATE_CON07**

Address: Operational Base + offset (0x081C)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | clk_i2s2_2ch_frac_en<br>clk_i2s2_2ch_frac clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | clk_i2s2_2ch_en<br>clk_i2s2_2ch_src clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | hclk_i2s3_2ch_en<br>hclk_i2s3_2ch clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | hclk_i2s2_2ch_en<br>hclk_i2s2_2ch clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | pclk_acdcdig_en<br>pclk_acdcdig clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | mclk_i2s0_8ch_rx_en<br>mclk_i2s0_8ch_rx clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | clk_i2s0_8ch_frac_rx_en<br>clk_i2s0_8ch_rx_frac clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | clk_i2s0_8ch_rx_en<br>clk_i2s0_8ch_rx_src clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | mclk_i2s0_8ch_tx_en<br>mclk_i2s0_8ch_tx clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_i2s0_8ch_frac_tx_en<br>clk_i2s0_8ch_tx_frac clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | clk_i2s0_8ch_tx_en<br>clk_i2s0_8ch_tx_src clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | hclk_i2s0_8ch_en<br>hclk_i2s0_8ch clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_audio_biu_en<br>pclk_audio_biu clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | hclk_audio_biu_en<br>hclk_audio_biu clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | pclk_audio_root_en<br>pclk_audio_root clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | hclk_audio_root_en<br>hclk_audio_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON08**

Address: Operational Base + offset (0x0820)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | clk_spdif0_en<br>clk_spdif0_src clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | hclk_spdif0_en<br>hclk_spdif0 clock gating control.<br>When high, disable clock |
| 13:5 | RO | 0x000 | reserved |
| 4 | RW | 0x0 | clk_dac_acdcdig_en<br>clk_dac_acdcdig clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | mclk_i2s3_2ch_en<br>mclk_i2s3_2ch clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | clk_i2s3_2ch_frac_en<br>clk_i2s3_2ch_frac clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_i2s3_2ch_en<br>clk_i2s3_2ch_src clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | mclk_i2s2_2ch_en<br>mclk_i2s2_2ch clock gating control.<br>When high, disable clock |

**CRU_GATE_CON09**

Address: Operational Base + offset (0x0824)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | mclk_pdm1_en<br>mclk_pdm1 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | hclk_pdm1_en<br>hclk_pdm1 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | mclk_spdif1_en<br>mclk_spdif1 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | clk_spdif1_frac_en<br>clk_spdif1_frac clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | clk_spdif1_en<br>clk_spdif1_src clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | hclk_spdif1_en<br>hclk_spdif1 clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | mclk_spdif0_en<br>mclk_spdif0 clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | clk_spdif0_frac_en<br>clk_spdif0_frac clock gating control.<br>When high, disable clock |

**CRU_GATE_CON10**

Address: Operational Base + offset (0x0828)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pclk_i2c8_en<br>pclk_i2c8 clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | pclk_i2c7_en<br>pclk_i2c7 clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | pclk_i2c6_en<br>pclk_i2c6 clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | pclk_i2c5_en<br>pclk_i2c5 clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | pclk_i2c4_en<br>pclk_i2c4 clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | pclk_i2c3_en<br>pclk_i2c3 clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | pclk_i2c2_en<br>pclk_i2c2 clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | pclk_i2c1_en<br>pclk_i2c1 clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | aclk_dmac2_en<br>aclk_dmac2 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | aclk_dmac1_en<br>aclk_dmac1 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | aclk_dmac0_en<br>aclk_dmac0 clock gating control.<br>When high, disable clock |
| 4 | RO | 0x0 | reserved |
| 3 | RW | 0x0 | aclk_gic_en<br>aclk_gic clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | pclk_bus_biu_en<br>pclk_bus_biu clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | aclk_bus_biu_en<br>aclk_bus_biu clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | aclk_bus_root_en<br>aclk_bus_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON11**

Address: Operational Base + offset (0x082C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | clk_saradc_en<br>clk_saradc clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | pclk_saradc_en<br>pclk_saradc clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | clk_can2_en<br>clk_can2 clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | pclk_can2_en<br>pclk_can2 clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | clk_can1_en<br>clk_can1 clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | pclk_can1_en<br>pclk_can1 clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | clk_can0_en<br>clk_can0 clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | pclk_can0_en<br>pclk_can0 clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | clk_i2c8_en<br>clk_i2c8 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_i2c7_en<br>clk_i2c7 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | clk_i2c6_en<br>clk_i2c6 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | clk_i2c5_en<br>clk_i2c5 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | clk_i2c4_en<br>clk_i2c4 clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | clk_i2c3_en<br>clk_i2c3 clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_i2c2_en<br>clk_i2c2 clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | clk_i2c1_en<br>clk_i2c1 clock gating control.<br>When high, disable clock |

**CRU_GATE_CON12**

Address: Operational Base + offset (0x0830)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | clk_uart2_frac_en<br>clk_uart2_frac clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | clk_uart2_en<br>clk_uart2_src clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | sclk_uart1_en<br>sclk_uart1 clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | clk_uart1_frac_en<br>clk_uart1_frac clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | clk_uart1_en<br>clk_uart1_src clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | pclk_uart9_en<br>pclk_uart9 clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | pclk_uart8_en<br>pclk_uart8 clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | pclk_uart7_en<br>pclk_uart7 clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | pclk_uart6_en<br>pclk_uart6 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | pclk_uart5_en<br>pclk_uart5 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | pclk_uart4_en<br>pclk_uart4 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_uart3_en<br>pclk_uart3 clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | pclk_uart2_en<br>pclk_uart2 clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | pclk_uart1_en<br>pclk_uart1 clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_tsadc_en<br>clk_tsadc clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | pclk_tsadc_en<br>pclk_tsadc clock gating control.<br>When high, disable clock |

**CRU_GATE_CON13**

Address: Operational Base + offset (0x0834)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | sclk_uart7_en<br>sclk_uart7 clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | clk_uart7_frac_en<br>clk_uart7_frac clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | clk_uart7_en<br>clk_uart7_src clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | sclk_uart6_en<br>sclk_uart6 clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | clk_uart6_frac_en<br>clk_uart6_frac clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | clk_uart6_en<br>clk_uart6_src clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | sclk_uart5_en<br>sclk_uart5 clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | clk_uart5_frac_en<br>clk_uart5_frac clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | clk_uart5_en<br>clk_uart5_src clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | sclk_uart4_en<br>sclk_uart4 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | clk_uart4_frac_en<br>clk_uart4_frac clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | clk_uart4_en<br>clk_uart4_src clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | sclk_uart3_en<br>sclk_uart3 clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | clk_uart3_frac_en<br>clk_uart3_frac clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_uart3_en<br>clk_uart3_src clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | sclk_uart2_en<br>sclk_uart2 clock gating control.<br>When high, disable clock |

**CRU_GATE_CON14**

Address: Operational Base + offset (0x0838)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | clk_spi4_en<br>clk_spi4 clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | clk_spi3_en<br>clk_spi3 clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | clk_spi2_en<br>clk_spi2 clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | clk_spi1_en<br>clk_spi1 clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | clk_spi0_en<br>clk_spi0 clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | pclk_spi4_en<br>pclk_spi4 clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | pclk_spi3_en<br>pclk_spi3 clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | pclk_spi2_en<br>pclk_spi2 clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | pclk_spi1_en<br>pclk_spi1 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | pclk_spi0_en<br>pclk_spi0 clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | sclk_uart9_en<br>sclk_uart9 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | clk_uart9_frac_en<br>clk_uart9_frac clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | clk_uart9_en<br>clk_uart9_src clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | sclk_uart8_en<br>sclk_uart8 clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_uart8_frac_en<br>clk_uart8_frac clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | clk_uart8_en<br>clk_uart8_src clock gating control.<br>When high, disable clock |

**CRU_GATE_CON15**

Address: Operational Base + offset (0x083C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | clk_bustimer0_en<br>clk_bustimer0 clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | clk_bustimer_root_en<br>clk_bus_timer_root clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | pclk_bustimer1_en<br>pclk_bustimer1 clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | pclk_bustimer0_en<br>pclk_bustimer0 clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | clk_pwm3_capture_en<br>clk_pwm3_capture clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | clk_pwm3_en<br>clk_pwm3 clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | pclk_pwm3_en<br>pclk_pwm3 clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | clk_pwm2_capture_en<br>clk_pwm2_capture clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | clk_pwm2_en<br>clk_pwm2 clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | pclk_pwm2_en<br>pclk_pwm2 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | clk_pwm1_capture_en<br>clk_pwm1_capture clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | clk_pwm1_en<br>clk_pwm1 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_pwm1_en<br>pclk_pwm1 clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | pclk_sys_grf_en<br>pclk_sys_grf clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | tclk_wdt0_en<br>tclk_wdt0 clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | pclk_wdt0_en<br>pclk_wdt0 clock gating control.<br>When high, disable clock |

**CRU_GATE_CON16**

Address: Operational Base + offset (0x0840)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | dbclk_gpio1_en<br>dbclk_gpio1 clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | pclk_gpio1_en<br>pclk_gpio1 clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | pclk_mailbox2_en<br>pclk_mailbox2 clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | pclk_mailbox1_en<br>pclk_mailbox1 clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | pclk_mailbox0_en<br>pclk_mailbox0 clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | clk_bustimer11_en<br>clk_bustimer11 clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | clk_bustimer10_en<br>clk_bustimer10 clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | clk_bustimer9_en<br>clk_bustimer9 clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x0 | clk_bustimer8_en<br>clk_bustimer8 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_bustimer7_en<br>clk_bustimer7 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | clk_bustimer6_en<br>clk_bustimer6 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | clk_bustimer5_en<br>clk_bustimer5 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | clk_bustimer4_en<br>clk_bustimer4 clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | clk_bustimer3_en<br>clk_bustimer3 clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_bustimer2_en<br>clk_bustimer2 clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | clk_bustimer1_en<br>clk_bustimer1 clock gating control.<br>When high, disable clock |

**CRU_GATE_CON17**

Address: Operational Base + offset (0x0844)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pclk_apb2asb_mst_bot_right_en<br>pclk_apb2asb_mst_bot_right clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | pclk_apb2asb_mst_cdphy_en<br>pclk_apb2asb_mst_cdphy clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | pclk_apb2asb_mst_top_en<br>pclk_apb2asb_mst_top clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | pclk_dft2apb_en<br>pclk_dft2apb clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | aclk_gicadb_gic2core_bus_en<br>aclk_gicadb_gic2core_bus clock gating control.<br>When high, disable clock |
| 10 | RO | 0x0 | reserved |
| 9 | RW | 0x0 | pclk_top_en<br>pclk_top clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | dclk_decom_en<br>dclk_decom clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x0 | pclk_decom_en<br>pclk_decom clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | aclk_decom_en<br>aclk_decom clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | dbclk_gpio4_en<br>dbclk_gpio4 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_gpio4_en<br>pclk_gpio4 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | dbclk_gpio3_en<br>dbclk_gpio3 clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | pclk_gpio3_en<br>pclk_gpio3 clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | dbclk_gpio2_en<br>dbclk_gpio2 clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | pclk_gpio2_en<br>pclk_gpio2 clock gating control.<br>When high, disable clock |

**CRU_GATE_CON18**

Address: Operational Base + offset (0x0848)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | clk_otp_phy_en<br>clk_otp_phy_g clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | clk_otpc_auto_rd_en<br>clk_otpc_auto_rd_g clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | clk_otpc_arb_en<br>clk_otpc_arb clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | clk_otpc_ns_en<br>clk_otpc_ns clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | pclk_otpc_ns_en<br>pclk_otpc_ns clock gating control.<br>When high, disable clock |
| 8:7 | RO | 0x0 | reserved |
| 6 | RW | 0x0 | aclk_spinlock_en<br>aclk_spinlock clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | pclk_apb2asb_mst_emmcio_en<br>pclk_apb2asb_mst_emmcio clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | pclk_apb2asb_mst_vccio6_en<br>pclk_apb2asb_mst_vccio6 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_apb2asb_mst_vccio3_5_en<br>pclk_apb2asb_mst_vccio3_5 clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | pclk_apb2asb_mst_csiphy_en<br>pclk_apb2asb_mst_csiphy clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | pclk_apb2asb_mst_ioc_right_en<br>pclk_apb2asb_mst_ioc_right clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | pclk_apb2asb_mst_ioc_top_en<br>pclk_apb2asb_mst_ioc_top clock gating control.<br>When high, disable clock |

**CRU_GATE_CON19**

Address: Operational Base + offset (0x084C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x0 | pclk_ddrcm0_intmux_en<br>pclk_ddrcm0_intmux clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_pmucm0_intmux_en<br>pclk_pmucm0_intmux clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_pmu2_en<br>pclk_pmu2 clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | clk_bisrintf_en<br>clk_bisrintf clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_bisrintf_pllsrc_en<br>clk_bisrintf_pllsrc clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | pclk_busioc_en<br>pclk_busioc clock gating control.<br>When high, disable clock |

**CRU_GATE_CON20**

Address: Operational Base + offset (0x0850)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pclk_ddr_standby_ch1_en<br>pclk_ddr_standby_ch1 clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14 | RW | 0x0 | pclk_ddr_mon_ch1_en<br>pclk_ddr_mon_ch1 clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | pclk_ddr_dfictl_ch1_en<br>pclk_ddr_dfictl_ch1 clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | aclk_ddr_upctl_ch0_en<br>aclk_ddr_upctl_ch0 clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | clk_ddr_standby_ch0_en<br>clk_ddr_standby_ch0 clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | clk_ddr_mon_ch0_en<br>clk_ddr_mon_ch0 clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | clk_ddr_dfictl_ch0_en<br>clk_ddr_dfictl_ch0 clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | clk_ddr_upctl_ch0_en<br>clk_ddr_upctl_ch0 clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | clk_sbr_ch0_en<br>clk_sbr_ch0 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_dfi_ch0_en<br>clk_dfi_ch0 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | pclk_ddr_grf_ch01_en<br>pclk_ddr_grf_ch01 clock gating control, both ddr ch0 and ddr ch1.<br>When high, disable clock |
| 4 | RW | 0x0 | tmclk_ddr_mon_ch0_en<br>tmclk_ddr_mon_ch0 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_ddr_upctl_ch0_en<br>pclk_ddr_upctl_ch0 clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | pclk_ddr_standby_ch0_en<br>pclk_ddr_standby_ch0 clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | pclk_ddr_mon_ch0_en<br>pclk_ddr_mon_ch0 clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | pclk_ddr_dfictl_ch0_en<br>pclk_ddr_dfictl_ch0 clock gating control.<br>When high, disable clock |

**CRU_GATE_CON21**

Address: Operational Base + offset (0x0854)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x0 | aclk_ddr_frs_ddrsch0_en<br>aclk_ddr_frs_ddrsch0 clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | aclk_ddr_rs_ddrsch0_en<br>aclk_ddr_rs_ddrsch0 clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | aclk_ddr_ddrsch0_en<br>aclk_ddr_ddrsch0 clock gating control.<br>When high, disable clock |
| 12:9 | RO | 0x0 | reserved |
| 8 | RW | 0x0 | aclk_ddr_upctl_ch1_en<br>aclk_ddr_upctl_ch1 clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | clk_ddr_standby_ch1_en<br>clk_ddr_standby_ch1 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_ddr_mon_ch1_en<br>clk_ddr_mon_ch1 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | clk_ddr_dfictl_ch1_en<br>clk_ddr_dfictl_ch1 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | clk_ddr_upctl_ch1_en<br>clk_ddr_upctl_ch1 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | clk_sbr_ch1_en<br>clk_sbr_ch1 clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | clk_dfi_ch1_en<br>clk_dfi_ch1 clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | tmclk_ddr_mon_ch1_en<br>tmclk_ddr_mon_ch1 clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | pclk_ddr_upctl_ch1_en<br>pclk_ddr_upctl_ch1 clock gating control.<br>When high, disable clock |

**CRU_GATE_CON22**

Address: Operational Base + offset (0x0858)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x1 | clk_testout_ddr01_en<br>clk_testout_ddr01 clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | pclk_ddr_ddrsch1_en<br>pclk_ddr_ddrsch1 clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | pclk_ddr_ddrsch0_en<br>pclk_ddr_ddrsch0 clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | aclk_ddr_frs_scramble1_en<br>aclk_ddr_frs_scramble1 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | aclk_ddr_scramble1_en<br>aclk_ddr_scramble1 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | aclk_ddr_frs_ddrsch1_en<br>aclk_ddr_frs_ddrsch1 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | aclk_ddr_rs_ddrsch1_en<br>aclk_ddr_rs_ddrsch1 clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | aclk_ddr_ddrsch1_en<br>aclk_ddr_ddrsch1 clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | aclk_ddr_frs_scramble0_en<br>aclk_ddr_frs_scramble0 clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | aclk_ddr_scramble0_en<br>aclk_ddr_scramble0 clock gating control.<br>When high, disable clock |

**CRU_GATE_CON23**

Address: Operational Base + offset (0x085C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pclk_ddr_standby_ch3_en<br>pclk_ddr_standby_ch3 clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | pclk_ddr_mon_ch3_en<br>pclk_ddr_mon_ch3 clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | pclk_ddr_dfictl_ch3_en<br>pclk_ddr_dfictl_ch3 clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | aclk_ddr_upctl_ch2_en<br>aclk_ddr_upctl_ch2 clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | clk_ddr_standby_ch2_en<br>clk_ddr_standby_ch2 clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | clk_ddr_mon_ch2_en<br>clk_ddr_mon_ch2 clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | clk_ddr_dfictl_ch2_en<br>clk_ddr_dfictl_ch2 clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | clk_ddr_upctl_ch2_en<br>clk_ddr_upctl_ch2 clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x0 | clk_sbr_ch2_en<br>clk_sbr_ch2 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_dfi_ch2_en<br>clk_dfi_ch2 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | pclk_ddr_grf_ch23_en<br>pclk_ddr_grf_ch23 clock gating control, both ddr ch2 and ddr ch3.<br>When high, disable clock |
| 4 | RW | 0x0 | tmclk_ddr_mon_ch2_en<br>tmclk_ddr_mon_ch2 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_ddr_upctl_ch2_en<br>pclk_ddr_upctl_ch2 clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | pclk_ddr_standby_ch2_en<br>pclk_ddr_standby_ch2 clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | pclk_ddr_mon_ch2_en<br>pclk_ddr_mon_ch2 clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | pclk_ddr_dfictl_ch2_en<br>pclk_ddr_dfictl_ch2 clock gating control.<br>When high, disable clock |

**CRU_GATE_CON24**

Address: Operational Base + offset (0x0860)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | aclk_ddr_frs_ddrsch2_en<br>aclk_ddr_frs_ddrsch2 clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | aclk_ddr_rs_ddrsch2_en<br>aclk_ddr_rs_ddrsch2 clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | aclk_ddr_ddrsch2_en<br>aclk_ddr_ddrsch2 clock gating control.<br>When high, disable clock |
| 12:9 | RO | 0x0 | reserved |
| 8 | RW | 0x0 | aclk_ddr_upctl_ch3_en<br>aclk_ddr_upctl_ch3 clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | clk_ddr_standby_ch3_en<br>clk_ddr_standby_ch3 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_ddr_mon_ch3_en<br>clk_ddr_mon_ch3 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | clk_ddr_dfictl_ch3_en<br>clk_ddr_dfictl_ch3 clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | clk_ddr_upctl_ch3_en<br>clk_ddr_upctl_ch3 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | clk_sbr_ch3_en<br>clk_sbr_ch3 clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | clk_dfi_ch3_en<br>clk_dfi_ch3 clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | tmclk_ddr_mon_ch3_en<br>tmclk_ddr_mon_ch3 clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | pclk_ddr_upctl_ch3_en<br>pclk_ddr_upctl_ch3 clock gating control.<br>When high, disable clock |

**CRU_GATE_CON25**

Address: Operational Base + offset (0x0864)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x1 | clk_testout_ddr23_en<br>clk_testout_ddr23 clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | pclk_ddr_ddrsch3_en<br>pclk_ddr_ddrsch3 clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | pclk_ddr_ddrsch2_en<br>pclk_ddr_ddrsch2 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | aclk_ddr_frs_scramble3_en<br>aclk_ddr_frs_scramble3 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | aclk_ddr_scramble3_en<br>aclk_ddr_scramble3 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | aclk_ddr_frs_ddrsch3_en<br>aclk_ddr_frs_ddrsch3 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | aclk_ddr_rs_ddrsch3_en<br>aclk_ddr_rs_ddrsch3 clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | aclk_ddr_ddrsch3_en<br>aclk_ddr_ddrsch3 clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | aclk_ddr_frs_scramble2_en<br>aclk_ddr_frs_scramble2 clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | aclk_ddr_scramble2_en<br>aclk_ddr_scramble2 clock gating control.<br>When high, disable clock |

Rockchip Confidencial

**CRU_GATE_CON26**

Address: Operational Base + offset (0x0868)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | hclk_isp1_biu_en<br>hclk_isp1_biu clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | hclk_isp1_en<br>hclk_isp1 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | aclk_isp1_biu_en<br>aclk_isp1_biu clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | aclk_isp1_en<br>aclk_isp1 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | clk_isp1_core_vicap_en<br>clk_isp1_core_vicap clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | clk_isp1_core_marvin_en<br>clk_isp1_core_marvin clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | clk_isp1_core_en<br>clk_isp1_core clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | hclk_isp1_root_en<br>hclk_isp1_root clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | aclk_isp1_root_en<br>aclk_isp1_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON27**

Address: Operational Base + offset (0x086C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | hclk_rknn1_biu_en<br>hclk_rknn1_biu clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | hclk_rknn1_en<br>hclk_rknn1 clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | aclk_rknn1_biu_en<br>aclk_rknn1_biu clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | aclk_rknn1_en<br>aclk_rknn1 clock gating control.<br>When high, disable clock |

Rockchip Confidencial

**CRU_GATE_CON28**

Address: Operational Base + offset (0x0870)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | hclk_rknn2_biu_en<br>hclk_rknn2_biu clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | hclk_rknn2_en<br>hclk_rknn2 clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | aclk_rknn2_biu_en<br>aclk_rknn2_biu clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | aclk_rknn2_en<br>aclk_rknn2 clock gating control.<br>When high, disable clock |

**CRU_GATE_CON29**

Address: Operational Base + offset (0x0874)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | clk_npu_pvtm_en<br>clk_npu_pvtm clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | clk_pvtm1_en<br>clk_pvtm1 clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | pclk_npu_grf_en<br>pclk_npu_grf clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | pclk_pvtm1_en<br>pclk_pvtm1 clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | tclk_npu_wdt_en<br>tclk_npu_wdt clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | pclk_npu_wdt_en<br>pclk_npu_wdt clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | clk_nputimer1_en<br>clk_nputimer1 clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | clk_nputimer0_en<br>clk_nputimer0 clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | clk_nputimer_root_en<br>clk_nputimer_root clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | pclk_npu_timer_en<br>pclk_npu_timer clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | pclk_nputop_biu_en<br>pclk_nputop_biu clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_nputop_root_en<br>pclk_nputop_root clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | clk_rknn_dsu0_en<br>clk_rknn_dsu0 clock gating control.<br>When high, disable clock |
| 2 | RW | 0x1 | clk_testout_npu_en<br>clk_testout_npu clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_rknn_dsu0_df_en<br>clk_rknn_dsu0_src_t clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | hclk_rknn_root_en<br>hclk_rknn_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON30**

Address: Operational Base + offset (0x0878)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | hclk_rknn0_biu_en<br>hclk_rknn0_biu clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | hclk_rknn0_en<br>hclk_rknn0 clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | aclk_rknn0_biu_en<br>aclk_rknn0_biu clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | aclk_rknn0_en<br>aclk_rknn0 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | clk_npu_cm0_rtc_en<br>clk_npu_cm0_rtc clock gating control.<br>When high, disable clock |
| 4 | RO | 0x0 | reserved |
| 3 | RW | 0x0 | fclk_npu_cm0_core_en<br>fclk_npu_cm0_core clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | hclk_npu_cm0_biu_en<br>hclk_npu_cm0_biu clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | hclk_npu_cm0_root_en<br>hclk_npu_cm0_root clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | clk_npu_pvtpll_en<br>clk_npu_pvtpll clock gating control.<br>When high, disable clock |

**CRU_GATE_CON31**

Address: Operational Base + offset (0x087C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | hclk_sfc_xip_en<br>hclk_sfc_xip clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | hclk_sfc_en<br>hclk_sfc clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | sclk_sfc_en<br>sclk_sfc clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | tmclk_emmc_en<br>tmclk_emmc clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | bclk_emmc_en<br>bclk_emmc clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | cclk_emmc_en<br>cclk_emmc clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | aclk_emmc_en<br>aclk_emmc clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | hclk_emmc_en<br>hclk_emmc clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | aclk_nvm_biu_en<br>aclk_nvm_biu clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | hclk_nvm_biu_en<br>hclk_nvm_biu clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | aclk_nvm_root_en<br>aclk_nvm_root clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | hclk_nvm_root_en<br>hclk_nvm_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON32**

Address: Operational Base + offset (0x0880)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | aclk_pcie_1l0_dbi_en<br>aclk_pcie_1l0_dbi clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | aclk_pcie_2l_dbi_en<br>aclk_pcie_2l_dbi clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | aclk_pcie_4l_dbi_en<br>aclk_pcie_4l_dbi clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | aclk_pcie_biu_en<br>aclk_pcie_biu clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | aclk_gmac1_en<br>aclk_gmac1 clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | aclk_gmac0_en<br>aclk_gmac0 clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | aclk_php_biu_en<br>aclk_php_biu clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | aclk_pcie_bridge_en<br>aclk_pcie_gridge clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | aclk_php_root_en<br>aclk_php_root clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | aclk_pcie_root_en<br>aclk_pcie_root clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | pclk_php_biu_en<br>pclk_php_biu clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_gmac1_en<br>pclk_gmac1 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_gmac0_en<br>pclk_gmac0 clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | pclk_dec_biu_en<br>pclk_dec_biu clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | pclk_grf_en<br>pclk_grf clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | pclk_php_root_en<br>pclk_php_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON33**

Address: Operational Base + offset (0x0884)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pclk_pcie_1l1_en<br>pclk_pcie_1l1 clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | pclk_pcie_1l0_en<br>pclk_pcie_1l0 clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | pclk_pcie_2l_en<br>pclk_pcie_2l clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | pclk_pcie_4l_en<br>pclk_pcie_4l clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | aclk_pcie_1l2_slv_en<br>aclk_pcie_1l2_slv clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | aclk_pcie_1l1_slv_en<br>aclk_pcie_1l1_slv clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | aclk_pcie_1l0_slv_en<br>aclk_pcie_1l0_slv clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | aclk_pcie_2l_slv_en<br>aclk_pcie_2l_slv clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | aclk_pcie_4l_slv_en<br>aclk_pcie_4l_slv clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | aclk_pcie_1l2_mstr_en<br>aclk_pcie_1l2_mstr clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | aclk_pcie_1l1_mstr_en<br>aclk_pcie_1l1_mstr clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | aclk_pcie_1l0_mstr_en<br>aclk_pcie_1l0_mstr clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | aclk_pcie_2l_mstr_en<br>aclk_pcie_2l_mstr clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | aclk_pcie_4l_mstr_en<br>aclk_pcie_4l_mstr clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | aclk_pcie_1l2_dbi_en<br>aclk_pcie_1l2_dbi clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | aclk_pcie_1l1_dbi_en<br>aclk_pcie_1l1_dbi clock gating control.<br>When high, disable clock |

**CRU_GATE_CON34**

Address: Operational Base + offset (0x0888)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | clk_gmac1_ptp_ref_en<br>clk_gmac1_ptp_ref clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | clk_gmac0_ptp_ref_en<br>clk_gmac0_ptp_ref clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | aclk_mmu_biu_en<br>aclk_mmu_biu clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | aclk_mmu_php_en<br>aclk_mmu_php clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | aclk_mmu_pcie_en<br>aclk_mmu_pcie clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | aclk_php_gic_its_en<br>aclk_php_gic_its clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | clk_pcie_1l2_aux_en<br>clk_pcie_1l2_aux clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | clk_pcie_1l1_aux_en<br>clk_pcie_1l1_aux clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | clk_pcie_1l0_aux_en<br>clk_pcie_1l0_aux clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | clk_pcie_2l_aux_en<br>clk_pcie_2l_aux clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_pcie_4l_aux_en<br>clk_pcie_4l_aux clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | pclk_pcie_1l2_en<br>pclk_pcie_1l2 clock gating control.<br>When high, disable clock |

**CRU_GATE_CON35**

Address: Operational Base + offset (0x088C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | clk_utmi_otg2_en<br>clk_utmi_otg2 clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RW | 0x0 | ref_clk_usb3otg2_en<br>ref_clk_usb3otg2 clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | suspend_clk_usb3otg2_en<br>suspend_clk_usb3otg2 clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | aclk_usb3otg2_en<br>aclk_usb3otg2 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_gmac_50m_cru_en<br>clk_gmac_50m_cru_i clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | clk_gmac_125m_cru_en<br>clk_gmac_125m_cru_i clock gating control.<br>When high, disable clock |
| 4:0 | RO | 0x00 | reserved |

**CRU_GATE_CON37**

Address: Operational Base + offset (0x0894)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | clk_rxoob2_en<br>clk_rxoob2 clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | clk_rxoob1_en<br>clk_rxoob1 clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | clk_rxoob0_en<br>clk_rxoob0 clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | aclk_sata2_en<br>aclk_sata2 clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | aclk_sata1_en<br>aclk_sata1 clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | aclk_sata0_en<br>aclk_sata0 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_pmalive2_en<br>clk_pmalive2 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | clk_pmalive1_en<br>clk_pmalive1 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | clk_pmalive0_en<br>clk_pmalive0 clock gating control.<br>When high, disable clock |
| 3 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | clk_pipephy2_ref_en<br>clk_pipephy2_ref clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_pipephy1_ref_en<br>clk_pipephy1_ref clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | clk_pipephy0_ref_en<br>clk_pipephy0_ref clock gating control.<br>When high, disable clock |

**CRU_GATE_CON38**

Address: Operational Base + offset (0x0898)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | clk_pcie_1l1_pipe_en<br>clk_pcie_1l1_pipe clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | clk_pcie_1l0_pipe_en<br>clk_pcie_1l0_pipe clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | clk_pcie_1l2_pipe_en<br>clk_pcie_1l2_pipe clock gating control.<br>When high, disable clock |
| 12:10 | RO | 0x0 | reserved |
| 9 | RW | 0x0 | clk_pipephy2_pipe_u3_g_en<br>clk_pipephy2_pipe_u3_g clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | clk_pipephy2_pipe_asic_g_en<br>clk_pipephy2_pipe_asic_g clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | clk_pipephy1_pipe_asic_g_en<br>clk_pipephy1_pipe_asic_g clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_pipephy0_pipe_asic_g_en<br>clk_pipephy0_pipe_asic_g clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | clk_pipephy2_pipe_g_en<br>clk_pipephy2_pipe_g clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | clk_pipephy1_pipe_g_en<br>clk_pipephy1_pipe_g clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | clk_pipephy0_pipe_g_en<br>clk_pipephy0_pipe_g clock gating control.<br>When high, disable clock |
| 2:0 | RO | 0x0 | reserved |

**CRU_GATE_CON39**

Address: Operational Base + offset (0x089C)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | clk_pcie_2l_pipe_en<br>clk_pcie_2l_pipe clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | clk_pcie_4l_pipe_en<br>clk_pcie_4l_pipe clock gating control.<br>When high, disable clock |

**CRU_GATE_CON40**

Address: Operational Base + offset (0x08A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | clk_rkvdec0_core_en<br>clk_rkvdec0_core clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | clk_rkvdec0_hevc_ca_en<br>clk_rkvdec0_hevc_ca clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | clk_rkvdec0_ca_en<br>clk_rkvdec0_ca clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | aclk_rkvdec0_biu_en<br>aclk_rkvdec0_biu clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | hclk_rkvdec0_biu_en<br>hclk_rkvdec0_biu clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | aclk_rkvdec0_en<br>aclk_rkvdec0 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | hclk_rkvdec0_en<br>hclk_rkvdec0 clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | aclk_rkvdec_ccu_en<br>aclk_rkvdec_ccu clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | aclk_rkvdec0_root_en<br>aclk_rkvdec0_root clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | hclk_rkvdec0_root_en<br>hclk_rkvdec0_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON41**

Address: Operational Base + offset (0x08A4)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | clk_rkvdec1_core_en<br>clk_rkvdec1_core clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | clk_rkvdec1_hevc_ca_en<br>clk_rkvdec1_hevc_ca clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_rkvdec1_ca_en<br>clk_rkvdec1_ca clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | aclk_rkvdec1_biu_en<br>aclk_rkvdec1_biu clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | hclk_rkvdec1_biu_en<br>hclk_rkvdec1_biu clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | aclk_rkvdec1_en<br>aclk_rkvdec1 clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | hclk_rkvdec1_en<br>hclk_rkvdec1 clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | aclk_rkvdec1_root_en<br>aclk_rkvdec1_root clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | hclk_rkvdec1_root_en<br>hclk_rkvdec1_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON42**

Address: Operational Base + offset (0x08A8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | utmi_ohci_clk48_host0_en<br>utmi_ohci_clk48_host0 clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | aclk_usb_grf_en<br>aclk_usb_grf clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | hclk_host_arb1_en<br>hclk_host_arb1 clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | hclk_host1_en<br>hclk_host1 clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | hclk_host_arb0_en<br>hclk_host_arb0 clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10 | RW | 0x0 | hclk_host0_en<br>hclk_host0 clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | ref_clk_usb3otg1_en<br>ref_clk_usb3otg1 clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | suspend_clk_usb3otg1_en<br>suspend_clk_usb3otg1 clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | aclk_usb3otg1_en<br>aclk_usb3otg1 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | ref_clk_usb3otg0_en<br>ref_clk_usb3otg0 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | suspend_clk_usb3otg0_en<br>suspend_clk_usb3otg0 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | aclk_usb3otg0_en<br>aclk_usb3otg0 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | hclk_usb_biu_en<br>hclk_usb_biu clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | aclk_usb_biu_en<br>aclk_usb_biu clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | hclk_usb_root_en<br>hclk_usb_root clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | aclk_usb_root_en<br>aclk_usb_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON43**

Address: Operational Base + offset (0x08AC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | utmi_ohci_clk48_host1_en<br>utmi_ohci_clk48_host1 clock gating control.<br>When high, disable clock |

**CRU_GATE_CON44**

Address: Operational Base + offset (0x08B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x0 | hclk_jpeg_encoder2_en<br>hclk_jpeg_encoder2 clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | aclk_jpeg_encoder2_en<br>aclk_jpeg_encoder2 clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | hclk_jpeg_encoder1_en<br>hclk_jpeg_encoder1 clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | aclk_jpeg_encoder1_en<br>aclk_jpeg_encoder1 clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | hclk_jpeg_encoder0_en<br>hclk_jpeg_encoder0 clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | aclk_jpeg_encoder0_en<br>aclk_jpeg_encoder0 clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | hclk_vpu_en<br>hclk_vpu clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | aclk_vpu_en<br>aclk_vpu clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | aclk_jpeg_decoder_biu_en<br>aclk_jpeg_decoder_biu clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | hclk_vdpu_biu_en<br>hclk_vdpu_biu clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | aclk_vdpu_low_biu_en<br>aclk_vdpu_low_biu clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | aclk_vdpu_biu_en<br>aclk_vdpu_biu clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | aclk_jpeg_decoder_root_en<br>aclk_jpeg_decoder_root clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | hclk_vdpu_root_en<br>hclk_vdpu_root clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | aclk_vdpu_low_root_en<br>aclk_vdpu_low_root clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | aclk_vdpu_root_en<br>aclk_vdpu_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON45**

Address: Operational Base + offset (0x08B4)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | clk_rga3_0_core_en<br>clk_rga3_0_core clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | aclk_rga3_0_en<br>aclk_rga3_0 clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | hclk_rga3_0_en<br>hclk_rga3_0 clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | clk_rga2_core_en<br>clk_rga2_core clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | aclk_rga2_en<br>aclk_rga2 clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | hclk_rga2_en<br>hclk_rga2 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_iep2p0_core_en<br>clk_iep2p0_core clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | aclk_iep2p0_en<br>aclk_iep2p0 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | hclk_iep2p0_en<br>hclk_iep2p0 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | hclk_jpeg_decoder_en<br>hclk_jpeg_decoder clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | aclk_jpeg_decoder_en<br>aclk_jpeg_decoder clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | hclk_jpeg_encoder3_en<br>hclk_jpeg_encoder3 clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | aclk_jpeg_encoder3_en<br>aclk_jpeg_encoder3 clock gating control.<br>When high, disable clock |

**CRU_GATE_CON47**

Address: Operational Base + offset (0x08BC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | clk_rkvenc0_core_en<br>clk_rkvenc0_core clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | aclk_rkvenc0_en<br>aclk_rkvenc0 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | hclk_rkvenc0_en<br>hclk_rkvenc0 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | aclk_rkvenc0_biu_en<br>aclk_rkvenc0_biu clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | hclk_rkvenc0_biu_en<br>hclk_rkvenc0_biu clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | aclk_rkvenc0_root_en<br>aclk_rkvenc0_root clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | hclk_rkvenc0_root_en<br>hclk_rkvenc0_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON48**

Address: Operational Base + offset (0x08C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x0 | clk_rkvenc1_core_en<br>clk_rkvenc1_core clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | aclk_rkvenc1_en<br>aclk_rkvenc1 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | hclk_rkvenc1_en<br>hclk_rkvenc1 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | aclk_rkvenc1_biu_en<br>aclk_rkvenc1_biu clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | hclk_rkvenc1_biu_en<br>hclk_rkvenc1_biu clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | aclk_rkvenc1_root_en<br>aclk_rkvenc1_root clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | hclk_rkvenc1_root_en<br>hclk_rkvenc1_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON49**

Address: Operational Base + offset (0x08C4)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | hclk_fisheye0_en<br>hclk_fisheye0 clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | aclk_fisheye0_en<br>aclk_fisheye0 clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | hclk_isp0_en<br>hclk_isp0 clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | aclk_isp0_en<br>aclk_isp0 clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | clk_isp0_core_vicap_en<br>clk_isp0_core_vicap clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | clk_isp0_core_marvin_en<br>clk_isp0_core_marvin clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | clk_isp0_core_en<br>clk_isp0_core clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | hclk_vicap_en<br>hclk_vicap clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | aclk_vicap_en<br>aclk_vicap clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | dclk_vicap_en<br>dclk_vicap clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | pclk_vi_biu_en<br>pclk_vi_biu clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | hclk_vi_biu_en<br>hclk_vi_biu clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | aclk_vi_biu_en<br>aclk_vi_biu clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | pclk_vi_root_en<br>pclk_vi_root clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | hclk_vi_root_en<br>hclk_vi_root clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | aclk_vi_root_en<br>aclk_vi_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON50**

Address: Operational Base + offset (0x08C8)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | pclk_csi_host_5_en<br>pclk_csi_host_5 clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | pclk_csi_host_4_en<br>pclk_csi_host_4 clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | pclk_csi_host_3_en<br>pclk_csi_host_3 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | pclk_csi_host_2_en<br>pclk_csi_host_2 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | pclk_csi_host_1_en<br>pclk_csi_host_1 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_csi_host_0_en<br>pclk_csi_host_0 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | clk_fisheye1_core_en<br>clk_fisheye1_core clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | hclk_fisheye1_en<br>hclk_fisheye1 clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | aclk_fisheye1_en<br>aclk_fisheye1 clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | clk_fisheye0_core_en<br>clk_fisheye0_core clock gating control.<br>When high, disable clock |

**CRU_GATE_CON51**

Address: Operational Base + offset (0x08CC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | iclk_csihost1_en<br>iclk_csihost1 clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | iclk_csihost0_en<br>iclk_csihost0 clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | iclk_csihost01_en<br>iclk_csihost01 clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RW | 0x0 | clk_csihost5_vicap_en<br>clk_csihost5_vicap clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | clk_csihost4_vicap_en<br>clk_csihost4_vicap clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | clk_csihost3_vicap_en<br>clk_csihost3_vicap clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_csihost2_vicap_en<br>clk_csihost2_vicap clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | clk_csihost1_vicap_en<br>clk_csihost1_vicap clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | clk_csihost0_vicap_en<br>clk_csihost0_vicap clock gating control.<br>When high, disable clock |
| 3:0 | RO | 0x0 | reserved |

**CRU_GATE_CON52**

Address: Operational Base + offset (0x08D0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | dclk_vp0_en<br>dclk_vp0 clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | dclk_vp2_src_en<br>dclk_vp2_src clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | dclk_vp1_src_en<br>dclk_vp1_src clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | dclk_vp0_src_en<br>dclk_vp0_src clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | aclk_vop_en<br>aclk_vop clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | hclk_vop_en<br>hclk_vop clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | pclk_vop_biu_en<br>pclk_vop_biu clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | hclk_vop_biu_en<br>hclk_vop_biu clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | aclk_vop_low_biu_en<br>aclk_vop_low_biu clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | aclk_vop_biu_en<br>aclk_vop_biu clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_vop_root_en<br>pclk_vop_root clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | hclk_vop_root_en<br>hclk_vop_root clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | aclk_vop_low_root_en<br>aclk_vop_low_root clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | aclk_vop_root_en<br>aclk_vop_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON53**

Address: Operational Base + offset (0x08D4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | aclk_vop_doby_en<br>aclk_vop_doby clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | pclk_vop_channel_biu_en<br>pclk_vop_channel_biu clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | clk_vop_pmu_en<br>clk_vop_pmu clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | clk_dsihost1_en<br>clk_dsihost1 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_dsihost0_en<br>clk_dsihost0 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | pclk_dsihost1_en<br>pclk_dsihost1 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_dsihost0_en<br>pclk_dsihost0 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_vopgrf_en<br>pclk_vopgrf clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | dclk_vp3_en<br>dclk_vp3 clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | dclk_vp2_en<br>dclk_vp2 clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | dclk_vp1_en<br>dclk_vp1 clock gating control.<br>When high, disable clock |

**CRU_GATE_CON55**

Address: Operational Base + offset (0x08DC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | pclk_hdcp0_en<br>pclk_hdcp0 clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | hclk_hdcp0_en<br>hclk_hdcp0 clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | aclk_hdcp0_en<br>aclk_hdcp0 clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | hclk_hdcp_key0_en<br>hclk_hdcp_key0 clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | pclk_vo0grf_en<br>pclk_vo0grf clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | aclk_hdcp0_biu_en<br>aclk_hdcp0_biu clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | pclk_vo0_s_biu_en<br>pclk_vo0_s_biu clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | pclk_vo0_biu_en<br>pclk_vo0_biu clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | hclk_vo0_s_biu_en<br>hclk_vo0_s_biu clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | hclk_vo0_biu_en<br>hclk_vo0_biu clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_vo0_s_root_en<br>pclk_vo0_s_root clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_vo0_root_en<br>pclk_vo0_root clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | hclk_vo0_s_root_en<br>hclk_vo0_s_root clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | hclk_vo0_root_en<br>hclk_vo0_root clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | aclk_vo0_root_en<br>aclk_vo0_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON56**

Address: Operational Base + offset (0x08E0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | clk_i2s8_8ch_tx_en<br>clk_i2s8_8ch_tx_src clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | hclk_i2s8_8ch_en<br>hclk_i2s8_8ch clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | mclk_i2s4_8ch_tx_en<br>mclk_i2s4_8ch_tx clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | clk_i2s4_8ch_frac_tx_en<br>clk_i2s4_8ch_tx_frac clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | clk_i2s4_8ch_tx_en<br>clk_i2s4_8ch_tx_src clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | hclk_i2s4_8ch_en<br>hclk_i2s4_8ch clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | clk_dp1_en<br>clk_dp1 clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | clk_dp0_en<br>clk_dp0 clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | pclk_s_dp1_en<br>pclk_s_dp1 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | pclk_s_dp0_en<br>pclk_s_dp0 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | pclk_dp1_en<br>pclk_dp1 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_dp0_en<br>pclk_dp0 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | clk_aux16mhz_1_en<br>clk_aux16mhz_1 clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | clk_aux16mhz_0_en<br>clk_aux16mhz_0 clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | pclk_trng0_en<br>pclk_trng0 clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | aclk_trng0_en<br>aclk_trng0 clock gating control.<br>When high, disable clock |

**CRU_GATE_CON57**

Address: Operational Base + offset (0x08E4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | mclk_spdif5_en<br>mclk_spdif5 clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | mclk_spdif5_dp1_en<br>mclk_spdif5_dp1 clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | clk_spdif5_dp1_frac_en<br>clk_spdif5_dp1_frac clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | clk_spdif5_dp1_en<br>clk_spdif5_dp1_src clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | hclk_spdif5_dp1_en<br>hclk_spdif5_dp1 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | mclk_spdif2_en<br>mclk_spdif2 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | mclk_spdif2_dp0_en<br>mclk_spdif2_dp0 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | clk_spdif2_dp0_frac_en<br>clk_spdif2_dp0_frac clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | clk_spdif2_dp0_en<br>clk_spdif2_dp0_src clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | hclk_spdif2_dp0_en<br>hclk_spdif2_dp0 clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | mclk_i2s8_8ch_tx_en<br>mclk_i2s8_8ch_tx clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | clk_i2s8_8ch_frac_tx_en<br>clk_i2s8_8ch_tx_frac clock gating control.<br>When high, disable clock |

**CRU_GATE_CON59**

Address: Operational Base + offset (0x08EC)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pclk_s_edp1_en<br>pclk_s_edp1 clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | pclk_s_edp0_en<br>pclk_s_edp0 clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | pclk_vo1_s_biu_en<br>pclk_vo1_s_biu clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | pclk_vo1grf_en<br>pclk_vo1grf clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | pclk_vo1_biu_en<br>pclk_vo1_biu clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | hclk_vo1_s_biu_en<br>hclk_vo1_s_biu clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | hclk_vo1_biu_en<br>hclk_vo1_biu clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | aclk_vo1_biu_en<br>aclk_vo1_biu clock gating control.<br>When high, disable clock |
| 7 | RO | 0x0 | reserved |
| 6 | RW | 0x0 | aclk_hdcp1_biu_en<br>aclk_hdcp1_biu clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | pclk_vo1_s_root_en<br>pclk_vo1_s_root clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_vo1_root_en<br>pclk_vo1_root clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | hclk_vo1_s_root_en<br>hclk_vo1_s_root clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | hclk_vo1_root_en<br>hclk_vo1_root clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | aclk_hdmirx_root_en<br>aclk_hdmirx_root clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | aclk_hdcp1_root_en<br>aclk_hdcp1_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON60**

Address: Operational Base + offset (0x08F0)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | clk_hdmitx0_earc_en<br>clk_hdmitx0_earc clock gating control.<br>When high, disable clock |
| 14:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | pclk_hdmitx0_en<br>pclk_hdmitx0 clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | pclk_trng1_en<br>pclk_trng1 clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | aclk_trng1_en<br>aclk_trng1 clock gating control.<br>When high, disable clock |
| 8 | RO | 0x0 | reserved |
| 7 | RW | 0x0 | pclk_hdcp1_en<br>pclk_hdcp1 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | hclk_hdcp1_en<br>hclk_hdcp1 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | aclk_hdcp1_en<br>aclk_hdcp1 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | hclk_hdcp_key1_en<br>hclk_hdcp_key1 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | mclk_i2s7_8ch_rx_en<br>mclk_i2s7_8ch_rx clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | clk_i2s7_8ch_frac_rx_en<br>clk_i2s7_8ch_rx_frac clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_i2s7_8ch_rx_en<br>clk_i2s7_8ch_rx_src clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | hclk_i2s7_8ch_en<br>hclk_i2s7_8ch clock gating control.<br>When high, disable clock |

**CRU_GATE_CON61**

Address: Operational Base + offset (0x08F4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | clk_hdmirx_tmdsqp_en<br>clk_hdmirx_tmdsqp clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14 | RW | 0x0 | clk_hdmirx_aud_en<br>clk_hdmirx_aud clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | clk_hdmirx_aud_frac_en<br>clk_hdmirx_aud_frac clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | clk_hdmirx_aud_src_en<br>clk_hdmirx_aud_src clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | clk_hdmirx_ref_en<br>clk_hdmirx_ref clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | pclk_hdmirx_en<br>pclk_hdmirx clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | aclk_hdmirx_en<br>aclk_hdmirx clock gating control.<br>When high, disable clock |
| 8 | RO | 0x0 | reserved |
| 7 | RW | 0x0 | clk_hdmitx1_ref_en<br>clk_hdmitx1_ref clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_hdmitx1_earc_en<br>clk_hdmitx1_earc clock gating control.<br>When high, disable clock |
| 5:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | pclk_hdmitx1_en<br>pclk_hdmitx1 clock gating control.<br>When high, disable clock |
| 1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | clk_hdmitx0_ref_en<br>clk_hdmitx0_ref clock gating control.<br>When high, disable clock |

**CRU_GATE_CON62**

Address: Operational Base + offset (0x08F8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | mclk_i2s6_8ch_tx_en<br>mclk_i2s6_8ch_tx clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | clk_i2s6_8ch_frac_tx_en<br>clk_i2s6_8ch_tx_frac clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | clk_i2s6_8ch_tx_en<br>clk_i2s6_8ch_tx_src clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | hclk_i2s5_8ch_en<br>hclk_i2s5_8ch clock gating control.<br>When high, disable clock |
| 11:9 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | mclk_i2s5_8ch_tx_en<br>mclk_i2s5_8ch_tx clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | clk_i2s5_8ch_frac_tx_en<br>clk_i2s5_8ch_tx_frac clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_i2s5_8ch_tx_en<br>clk_i2s5_8ch_tx_src clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | clk_edp1_200m_en<br>clk_edp1_200m clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | clk_edp1_24m_en<br>clk_edp1_24m clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_edp1_en<br>pclk_edp1 clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | clk_edp0_200m_en<br>clk_edp0_200m clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_edp0_24m_en<br>clk_edp0_24m clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | pclk_edp0_en<br>pclk_edp0 clock gating control.<br>When high, disable clock |

**CRU_GATE_CON63**

Address: Operational Base + offset (0x08FC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | mclk_spdifrx1_en<br>mclk_spdifrx1 clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | hclk_spdifrx1_en<br>hclk_spdifrx1 clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | mclk_spdifrx0_en<br>mclk_spdifrx0 clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | hclk_spdifrx0_en<br>hclk_spdifrx0 clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | mclk_spdif4_en<br>mclk_spdif4 clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | clk_spdif4_frac_en<br>clk_spdif4_frac clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RW | 0x0 | clk_spdif4_en<br>clk_spdif4_src clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | hclk_spdif4_en<br>hclk_spdif4 clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | mclk_spdif3_en<br>mclk_spdif3 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_spdif3_frac_en<br>clk_spdif3_frac clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | clk_spdif3_en<br>clk_spdif3_src clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | hclk_spdif3_en<br>hclk_spdif3 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | hclk_i2s6_8ch_en<br>hclk_i2s6_8ch clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | mclk_i2s6_8ch_rx_en<br>mclk_i2s6_8ch_rx clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_i2s6_8ch_frac_rx_en<br>clk_i2s6_8ch_rx_frac clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | clk_i2s6_8ch_rx_en<br>clk_i2s6_8ch_rx_src clock gating control.<br>When high, disable clock |

**CRU_GATE_CON64**

Address: Operational Base + offset (0x0900)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | dclk_vp2hdmi_bridge1_vo1_en<br>dclk_vp2hdmi_bridge1_vo1 clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | dclk_vp2hdmi_bridge0_vo1_en<br>dclk_vp2hdmi_bridge0_vo1 clock gating control.<br>When high, disable clock |
| 13:2 | RO | 0x000 | reserved |
| 1 | RW | 0x0 | mclk_spdifrx2_en<br>mclk_spdifrx2 clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | hclk_spdifrx2_en<br>hclk_spdifrx2 clock gating control.<br>When high, disable clock |

**CRU_GATE_CON65**

Address: Operational Base + offset (0x0904)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | clk_hdmitrx_refsrc_en<br>clk_hdmitrx_refsrc clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | pclk_s_hdmirx_en<br>pclk_s_hdmirx clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | mclk_i2s10_8ch_rx_en<br>mclk_i2s10_8ch_rx clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_i2s10_8ch_frac_rx_en<br>clk_i2s10_8ch_rx_frac clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | clk_i2s10_8ch_rx_en<br>clk_i2s10_8ch_rx_src clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | hclk_i2s10_8ch_en<br>hclk_i2s10_8ch clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | mclk_i2s9_8ch_rx_en<br>mclk_i2s9_8ch_rx clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | clk_i2s9_8ch_frac_rx_en<br>clk_i2s9_8ch_rx_frac clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_i2s9_8ch_rx_en<br>clk_i2s9_8ch_rx_src clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | hclk_i2s9_8ch_en<br>hclk_i2s9_8ch clock gating control.<br>When high, disable clock |

**CRU_GATE_CON66**

Address: Operational Base + offset (0x0908)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pclk_pvtm2_en<br>pclk_pvtm2 clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | pclk_gpu_biu_en<br>pclk_gpu_biu clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | pclk_gpu_root_en<br>pclk_gpu_root clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | aclk_m3_gpu_biu_en<br>aclk_m3_gpu_biu clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11 | RW | 0x0 | aclk_m2_gpu_biu_en<br>aclk_m2_gpu_biu clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | aclk_m1_gpu_biu_en<br>aclk_m1_gpu_biu clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | aclk_m0_gpu_biu_en<br>aclk_m0_gpu_biu clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | aclk_s_gpu_biu_en<br>aclk_s_gpu_biu clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | clk_gpu_stacks_en<br>clk_gpu_stacks clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_gpu_coregroup_en<br>clk_gpu_coregroup clock gating control.<br>When high, disable clock |
| 5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | clk_gpu_en<br>clk_gpu clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | clk_gpu_src_en<br>clk_gpu_src clock gating control.<br>When high, disable clock |
| 2 | RW | 0x1 | clk_testout_gpu_en<br>clk_testout_gpu clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_gpu_src_df_en<br>clk_gpu_src_t clock gating control.<br>When high, disable clock |
| 0 | RO | 0x0 | reserved |

**CRU_GATE_CON67**

Address: Operational Base + offset (0x090C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | clk_gpu_pvtpll_en<br>clk_gpu_pvtpll clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | pclk_gpu_grf_en<br>pclk_gpu_grf clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_gpu_pvtm_en<br>clk_gpu_pvtm clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | clk_pvtm2_en<br>clk_pvtm2 clock gating control.<br>When high, disable clock |

**CRU_GATE_CON68**

Rockchip Confidencial

Address: Operational Base + offset (0x0910)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x0 | pclk_av1_en<br>pclk_av1 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_av1_biu_en<br>pclk_av1_biu clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_av1_root_en<br>pclk_av1_root clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | aclk_av1_en<br>aclk_av1 clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | aclk_av1_biu_en<br>aclk_av1_biu clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | aclk_av1_root_en<br>aclk_av1_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON69**

Address: Operational Base + offset (0x0914)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | clk_ddr_timer_root_en<br>clk_ddr_timer_root clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | fclk_ddr_cm0_core_en<br>fclk_ddr_cm0_core clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | hclk_center_biu_en<br>hclk_center_biu clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | hclk_ahb2apb_en<br>hclk_ahb2apb clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | aclk_center_s400_biu_en<br>aclk_center_s400_biu clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | aclk_center_s200_biu_en<br>aclk_center_s200_biu clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | aclk_center_s400_root_en<br>aclk_center_s400_root clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | aclk_center_s200_root_en<br>aclk_center_s200_root clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | aclk_ddr_sharemem_biu_en<br>aclk_ddr_sharemem_biu clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | aclk_ddr_sharemem_en<br>aclk_ddr_sharemem clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | aclk_dma2ddr_en<br>aclk_dma2ddr clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | aclk_ddr_biu_en<br>aclk_ddr_biu clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_center_root_en<br>pclk_center_root clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | hclk_center_root_en<br>hclk_center_root clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | aclk_center_low_root_en<br>aclk_center_low_root clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | aclk_center_root_en<br>aclk_center_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON70**

Address: Operational Base + offset (0x0918)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | pclk_center_channel_biu_en<br>pclk_center_channel_biu clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | pclk_center_biu_en<br>pclk_center_biu clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | pclk_sharemem_en<br>pclk_sharemem clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | pclk_dma2ddr_en<br>pclk_dma2ddr clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | pclk_timer_en<br>pclk_timer clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | pclk_wdt_en<br>pclk_wdt clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | pclk_ahb2apb_en<br>pclk_ahb2apb clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | pclk_center_grf_en<br>pclk_center_grf clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | clk_ddr_cm0_rtc_en<br>clk_ddr_cm0_rtc clock gating control.<br>When high, disable clock |
| 3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | tclk_wdt_ddr_en<br>tclk_wdt_ddr clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_ddr_timer1_en<br>clk_ddr_timer1 clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | clk_ddr_timer0_en<br>clk_ddr_timer0 clock gating control.<br>When high, disable clock |

**CRU_GATE_CON72**

Address: Operational Base + offset (0x0920)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | pclk_usb2phy_u2_1_grf0_en<br>pclk_usb2phy_u2_1_grf0 clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | pclk_usb2phy_u2_0_grf0_en<br>pclk_usb2phy_u2_0_grf0 clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | pclk_usb2phy_u3_1_grf0_en<br>pclk_usb2phy_u3_1_grf0 clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | pclk_usb2phy_u3_0_grf0_en<br>pclk_usb2phy_u3_0_grf0 clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | pclk_apb2asb_slv_bot_right_en<br>pclk_apb2asb_slv_bot_right clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | pclk_hdptx1_en<br>pclk_hdptx1 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | pclk_hdptx0_en<br>pclk_hdptx0 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_usbdpphy1_en<br>pclk_usbdpphy1 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_usbdpgrf1_en<br>pclk_usbdpgrf1 clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | pclk_usbdpphy0_en<br>pclk_usbdpphy0 clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | pclk_usbdpgrf0_en<br>pclk_usbdpgrf0 clock gating control.<br>When high, disable clock |
| 0 | RO | 0x0 | reserved |

**CRU_GATE_CON73**

Address: Operational Base + offset (0x0924)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | clk_hdmihdp1_en<br>clk_hdmihdp1 clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | clk_hdmihdp0_en<br>clk_hdmihdp0 clock gating control.<br>When high, disable clock |
| 11:0 | RO | 0x000 | reserved |

**CRU_GATE_CON74**

Address: Operational Base + offset (0x0928)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | hclk_vo1usb_top_biu_en<br>hclk_vo1usb_top_biu clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | hclk_vo1usb_top_root_en<br>hclk_vo1usb_top_root clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | aclk_vo1usb_top_biu_en<br>aclk_vo1usb_top_biu clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | aclk_vo1usb_top_root_en<br>aclk_vo1usb_top_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON75**

Address: Operational Base + offset (0x092C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | cclk_src_sdio_en<br>cclk_src_sdio clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | hclk_sdio_en<br>hclk_sdio clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | hclk_sdio_biu_en<br>hclk_sdio_biu clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | hclk_sdio_root_en<br>hclk_sdio_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON76**

Address: Operational Base + offset (0x0930)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x0 | clk_rga3_1_core_en<br>clk_rga3_1_core clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | aclk_rga3_1_en<br>aclk_rga3_1 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | hclk_rga3_1_en<br>hclk_rga3_1 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | aclk_rga3_biu_en<br>aclk_rga3_biu clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | hclk_rga3_biu_en<br>hclk_rga3_biu clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | hclk_rga3_root_en<br>hclk_rga3_root clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | aclk_rga3_root_en<br>aclk_rga3_root clock gating control.<br>When high, disable clock |

**CRU_GATE_CON77**

Address: Operational Base + offset (0x0934)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x0 | clk_ref_pipe_phy2_pll_src_en<br>clk_ref_pipe_phy2_pll_src clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | clk_ref_pipe_phy1_pll_src_en<br>clk_ref_pipe_phy1_pll_src clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | clk_ref_pipe_phy0_pll_src_en<br>clk_ref_pipe_phy0_pll_src clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | clk_ref_pipe_phy2_osc_src_en<br>clk_ref_pipe_phy2_osc_src clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_ref_pipe_phy1_osc_src_en<br>clk_ref_pipe_phy1_osc_src clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | clk_ref_pipe_phy0_osc_src_en<br>clk_ref_pipe_phy0_osc_src clock gating control.<br>When high, disable clock |

**CRU_SOFTRST_CON01**

Address: Operational Base + offset (0x0A04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | aresetn_top_m500_biu<br>When high, reset relative logic |
| 14:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | presetn_csiphy1<br>When high, reset relative logic |
| 7 | RO | 0x0 | reserved |
| 6 | RW | 0x0 | presetn_csiphy0<br>When high, reset relative logic |
| 5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | presetn_top_biu<br>When high, reset relative logic |
| 3 | RW | 0x0 | aresetn_top_biu<br>When high, reset relative logic |
| 2:0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON02**

Address: Operational Base + offset (0x0A08)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | resetn_usbdp_combo_phy1_init<br>When high, reset relative logic |
| 14:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | resetn_usbdp_combo_phy0_pcs<br>When high, reset relative logic |
| 10 | RW | 0x0 | resetn_usbdp_combo_phy0_lane<br>When high, reset relative logic |
| 9 | RW | 0x0 | resetn_usbdp_combo_phy0_cmn<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | resetn_usbdp_combo_phy0_init<br>When high, reset relative logic |
| 7:4 | RO | 0x0 | reserved |
| 3 | RW | 0x0 | aresetn_top_m300_biu<br>When high, reset relative logic |
| 2 | RW | 0x0 | aresetn_top_s400_biu<br>When high, reset relative logic |
| 1 | RW | 0x0 | aresetn_top_s200_biu<br>When high, reset relative logic |
| 0 | RW | 0x0 | aresetn_top_m400_biu<br>When high, reset relative logic |

**CRU_SOFTRST_CON03**

Address: Operational Base + offset (0x0A0C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | presetn_mipi_dcphy0_grf<br>When high, reset relative logic |
| 14 | RW | 0x0 | presetn_mipi_dcphy0<br>When high, reset relative logic |
| 13:3 | RO | 0x000 | reserved |
| 2 | RW | 0x0 | resetn_usbdp_combo_phy1_pcs<br>When high, reset relative logic |
| 1 | RW | 0x0 | resetn_usbdp_combo_phy1_lane<br>When high, reset relative logic |
| 0 | RW | 0x0 | resetn_usbdp_combo_phy1_cmn<br>When high, reset relative logic |

**CRU_SOFTRST_CON04**

Address: Operational Base + offset (0x0A10)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | presetn_apb2asb_slv_ioc_right<br>When high, reset relative logic |
| 10 | RW | 0x0 | presetn_apb2asb_slv_ioc_top<br>When high, reset relative logic |
| 9 | RW | 0x0 | presetn_apb2asb_slv_emmcio<br>When high, reset relative logic |
| 8 | RW | 0x0 | presetn_apb2asb_slv_vccio6<br>When high, reset relative logic |
| 7 | RW | 0x0 | presetn_apb2asb_slv_vccio3_5<br>When high, reset relative logic |
| 6 | RW | 0x0 | presetn_apb2asb_slv_csiphy<br>When high, reset relative logic |
| 5 | RW | 0x0 | presetn_apb2asb_slv_cdphy<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | presetn_mipi_dcphy1_grf<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_mipi_dcphy1<br>When high, reset relative logic |
| 2:0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON05**

Address: Operational Base + offset (0x0A14)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | hresetn_channel_secure2center<br>When high, reset relative logic |
| 14 | RW | 0x0 | hresetn_channel_secure2vo1usb<br>When high, reset relative logic |
| 13:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | aresetn_channel_secure2center<br>When high, reset relative logic |
| 7 | RW | 0x0 | aresetn_channel_secure2vo1usb<br>When high, reset relative logic |
| 6:1 | RO | 0x00 | reserved |
| 0 | RW | 0x0 | presetn_cru<br>When high, reset relative logic |

**CRU_SOFTRST_CON06**

Address: Operational Base + offset (0x0A18)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | presetn_channel_secure2center<br>When high, reset relative logic |
| 0 | RW | 0x0 | presetn_channel_secure2vo1usb<br>When high, reset relative logic |

**CRU_SOFTRST_CON07**

Address: Operational Base + offset (0x0A1C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | hresetn_i2s3_2ch<br>When high, reset relative logic |
| 12 | RW | 0x0 | hresetn_i2s2_2ch<br>When high, reset relative logic |
| 11 | RW | 0x0 | presetn_acdcdig<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10 | RW | 0x0 | mresetn_i2s0_8ch_rx<br>When high, reset relative logic |
| 9:8 | RO | 0x0 | reserved |
| 7 | RW | 0x0 | mresetn_i2s0_8ch_tx<br>When high, reset relative logic |
| 6:5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | hresetn_i2s0_8ch<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_audio_biu<br>When high, reset relative logic |
| 2 | RW | 0x0 | hresetn_audio_biu<br>When high, reset relative logic |
| 1:0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON08**

Address: Operational Base + offset (0x0A20)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | hresetn_spdif0<br>When high, reset relative logic |
| 13:5 | RO | 0x000 | reserved |
| 4 | RW | 0x0 | resetn_dac_acdcdig<br>When high, reset relative logic |
| 3 | RW | 0x0 | mresetn_i2s3_2ch<br>When high, reset relative logic |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | mresetn_i2s2_2ch<br>When high, reset relative logic |

**CRU_SOFTRST_CON09**

Address: Operational Base + offset (0x0A24)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | resetn_pdm1<br>When high, reset relative logic |
| 6 | RW | 0x0 | hresetn_pdm1<br>When high, reset relative logic |
| 5 | RW | 0x0 | mresetn_spdif1<br>When high, reset relative logic |
| 4:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | hresetn_spdif1<br>When high, reset relative logic |
| 1 | RW | 0x0 | mresetn_spdif0<br>When high, reset relative logic |
| 0 | RO | 0x0 | reserved |

Rockchip Confidencial

**CRU_SOFTRST_CON10**

Address: Operational Base + offset (0x0A28)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | presetn_i2c8<br>When high, reset relative logic |
| 14 | RW | 0x0 | presetn_i2c7<br>When high, reset relative logic |
| 13 | RW | 0x0 | presetn_i2c6<br>When high, reset relative logic |
| 12 | RW | 0x0 | presetn_i2c5<br>When high, reset relative logic |
| 11 | RW | 0x0 | presetn_i2c4<br>When high, reset relative logic |
| 10 | RW | 0x0 | presetn_i2c3<br>When high, reset relative logic |
| 9 | RW | 0x0 | presetn_i2c2<br>When high, reset relative logic |
| 8 | RW | 0x0 | presetn_i2c1<br>When high, reset relative logic |
| 7 | RW | 0x0 | aresetn_dmac2<br>When high, reset relative logic |
| 6 | RW | 0x0 | aresetn_dmac1<br>When high, reset relative logic |
| 5 | RW | 0x0 | aresetn_dmac0<br>When high, reset relative logic |
| 4 | RW | 0x0 | aresetn_gic_dbg<br>When high, reset relative logic |
| 3 | RW | 0x0 | aresetn_gic<br>When high, reset relative logic |
| 2 | RW | 0x0 | presetn_bus_biu<br>When high, reset relative logic |
| 1 | RW | 0x0 | aresetn_bus_biu<br>When high, reset relative logic |
| 0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON11**

Address: Operational Base + offset (0x0A2C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | presetn_saradc<br>When high, reset relative logic |
| 13 | RW | 0x0 | resetn_can2<br>When high, reset relative logic |
| 12 | RW | 0x0 | presetn_can2<br>When high, reset relative logic |
| 11 | RW | 0x0 | resetn_can1<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10 | RW | 0x0 | presetn_can1<br>When high, reset relative logic |
| 9 | RW | 0x0 | resetn_can0<br>When high, reset relative logic |
| 8 | RW | 0x0 | presetn_can0<br>When high, reset relative logic |
| 7 | RW | 0x0 | resetn_i2c8<br>When high, reset relative logic |
| 6 | RW | 0x0 | resetn_i2c7<br>When high, reset relative logic |
| 5 | RW | 0x0 | resetn_i2c6<br>When high, reset relative logic |
| 4 | RW | 0x0 | resetn_i2c5<br>When high, reset relative logic |
| 3 | RW | 0x0 | resetn_i2c4<br>When high, reset relative logic |
| 2 | RW | 0x0 | resetn_i2c3<br>When high, reset relative logic |
| 1 | RW | 0x0 | resetn_i2c2<br>When high, reset relative logic |
| 0 | RW | 0x0 | resetn_i2c1<br>When high, reset relative logic |

**CRU_SOFTRST_CON12**

Address: Operational Base + offset (0x0A30)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | sresetn_uart1<br>When high, reset relative logic |
| 12:11 | RO | 0x0 | reserved |
| 10 | RW | 0x0 | presetn_uart9<br>When high, reset relative logic |
| 9 | RW | 0x0 | presetn_uart8<br>When high, reset relative logic |
| 8 | RW | 0x0 | presetn_uart7<br>When high, reset relative logic |
| 7 | RW | 0x0 | presetn_uart6<br>When high, reset relative logic |
| 6 | RW | 0x0 | presetn_uart5<br>When high, reset relative logic |
| 5 | RW | 0x0 | presetn_uart4<br>When high, reset relative logic |
| 4 | RW | 0x0 | presetn_uart3<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_uart2<br>When high, reset relative logic |
| 2 | RW | 0x0 | presetn_uart1<br>When high, reset relative logic |
| 1 | RW | 0x0 | resetn_tsadc<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | presetn_tsadc<br>When high, reset relative logic |

**CRU_SOFTRST_CON13**

Address: Operational Base + offset (0x0A34)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | sresetn_uart7<br>When high, reset relative logic |
| 14:13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | sresetn_uart6<br>When high, reset relative logic |
| 11:10 | RO | 0x0 | reserved |
| 9 | RW | 0x0 | sresetn_uart5<br>When high, reset relative logic |
| 8:7 | RO | 0x0 | reserved |
| 6 | RW | 0x0 | sresetn_uart4<br>When high, reset relative logic |
| 5:4 | RO | 0x0 | reserved |
| 3 | RW | 0x0 | sresetn_uart3<br>When high, reset relative logic |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | sresetn_uart2<br>When high, reset relative logic |

**CRU_SOFTRST_CON14**

Address: Operational Base + offset (0x0A38)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | resetn_spi4<br>When high, reset relative logic |
| 14 | RW | 0x0 | resetn_spi3<br>When high, reset relative logic |
| 13 | RW | 0x0 | resetn_spi2<br>When high, reset relative logic |
| 12 | RW | 0x0 | resetn_spi1<br>When high, reset relative logic |
| 11 | RW | 0x0 | resetn_spi0<br>When high, reset relative logic |
| 10 | RW | 0x0 | presetn_spi4<br>When high, reset relative logic |
| 9 | RW | 0x0 | presetn_spi3<br>When high, reset relative logic |
| 8 | RW | 0x0 | presetn_spi2<br>When high, reset relative logic |
| 7 | RW | 0x0 | presetn_spi1<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | presetn_spi0<br>When high, reset relative logic |
| 5 | RW | 0x0 | sresetn_uart9<br>When high, reset relative logic |
| 4:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | sresetn_uart8<br>When high, reset relative logic |
| 1:0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON15**

Address: Operational Base + offset (0x0A3C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | resetn_bustimer0<br>When high, reset relative logic |
| 14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | presetn_bustimer1<br>When high, reset relative logic |
| 12 | RW | 0x0 | presetn_bustimer0<br>When high, reset relative logic |
| 11 | RO | 0x0 | reserved |
| 10 | RW | 0x0 | resetn_pwm3<br>When high, reset relative logic |
| 9 | RW | 0x0 | presetn_pwm3<br>When high, reset relative logic |
| 8 | RO | 0x0 | reserved |
| 7 | RW | 0x0 | resetn_pwm2<br>When high, reset relative logic |
| 6 | RW | 0x0 | presetn_pwm2<br>When high, reset relative logic |
| 5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | resetn_pwm1<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_pwm1<br>When high, reset relative logic |
| 2 | RW | 0x0 | presetn_sys_grf<br>When high, reset relative logic |
| 1 | RW | 0x0 | tresetn_wdt0<br>When high, reset relative logic |
| 0 | RW | 0x0 | presetn_wdt0<br>When high, reset relative logic |

**CRU_SOFTRST_CON16**

Address: Operational Base + offset (0x0A40)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | dbresetn_gpio1<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14 | RW | 0x0 | presetn_gpio1<br>When high, reset relative logic |
| 13 | RW | 0x0 | presetn_mailbox2<br>When high, reset relative logic |
| 12 | RW | 0x0 | presetn_mailbox1<br>When high, reset relative logic |
| 11 | RW | 0x0 | presetn_mailbox0<br>When high, reset relative logic |
| 10 | RW | 0x0 | resetn_bustimer11<br>When high, reset relative logic |
| 9 | RW | 0x0 | resetn_bustimer10<br>When high, reset relative logic |
| 8 | RW | 0x0 | resetn_bustimer9<br>When high, reset relative logic |
| 7 | RW | 0x0 | resetn_bustimer8<br>When high, reset relative logic |
| 6 | RW | 0x0 | resetn_bustimer7<br>When high, reset relative logic |
| 5 | RW | 0x0 | resetn_bustimer6<br>When high, reset relative logic |
| 4 | RW | 0x0 | resetn_bustimer5<br>When high, reset relative logic |
| 3 | RW | 0x0 | resetn_bustimer4<br>When high, reset relative logic |
| 2 | RW | 0x0 | resetn_bustimer3<br>When high, reset relative logic |
| 1 | RW | 0x0 | resetn_bustimer2<br>When high, reset relative logic |
| 0 | RW | 0x0 | resetn_bustimer1<br>When high, reset relative logic |

**CRU_SOFTRST_CON17**

Address: Operational Base + offset (0x0A44)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | presetn_apb2asb_mst_bot_right<br>When high, reset relative logic |
| 14 | RW | 0x0 | presetn_apb2asb_mst_cdphy<br>When high, reset relative logic |
| 13 | RW | 0x0 | presetn_apb2asb_mst_top<br>When high, reset relative logic |
| 12 | RW | 0x0 | presetn_dft2apb<br>When high, reset relative logic |
| 11 | RW | 0x0 | aresetn_gicadb_gic2core_bus<br>When high, reset relative logic |
| 10 | RO | 0x0 | reserved |
| 9 | RW | 0x0 | presetn_top<br>When high, reset relative logic |
| 8 | RW | 0x0 | dresetn_decom<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x0 | presetn_decom<br>When high, reset relative logic |
| 6 | RW | 0x0 | aresetn_decom<br>When high, reset relative logic |
| 5 | RW | 0x0 | dbresetn_gpio4<br>When high, reset relative logic |
| 4 | RW | 0x0 | presetn_gpio4<br>When high, reset relative logic |
| 3 | RW | 0x0 | dbresetn_gpio3<br>When high, reset relative logic |
| 2 | RW | 0x0 | presetn_gpio3<br>When high, reset relative logic |
| 1 | RW | 0x0 | dbresetn_gpio2<br>When high, reset relative logic |
| 0 | RW | 0x0 | presetn_gpio2<br>When high, reset relative logic |

**CRU_SOFTRST_CON18**

Address: Operational Base + offset (0x0A48)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | resetn_otpc_arb<br>When high, reset relative logic |
| 10 | RW | 0x0 | resetn_otpc_ns<br>When high, reset relative logic |
| 9 | RW | 0x0 | presetn_otpc_ns<br>When high, reset relative logic |
| 8:7 | RO | 0x0 | reserved |
| 6 | RW | 0x0 | aresetn_spinlock<br>When high, reset relative logic |
| 5 | RW | 0x0 | presetn_apb2asb_mst_emmcio<br>When high, reset relative logic |
| 4 | RW | 0x0 | presetn_apb2asb_mst_vccio6<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_apb2asb_mst_vccio3_5<br>When high, reset relative logic |
| 2 | RW | 0x0 | presetn_apb2asb_mst_csiphy<br>When high, reset relative logic |
| 1 | RW | 0x0 | presetn_apb2asb_mst_ioc_right<br>When high, reset relative logic |
| 0 | RW | 0x0 | presetn_apb2asb_mst_ioc_top<br>When high, reset relative logic |

**CRU_SOFTRST_CON19**

Address: Operational Base + offset (0x0A4C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x0 | presetn_ddrcm0_intmux<br>When high, reset relative logic |
| 4 | RW | 0x0 | presetn_pmucm0_intmux<br>When high, reset relative logic |
| 3:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | presetn_busioc<br>When high, reset relative logic |

**CRU_SOFTRST_CON20**

Address: Operational Base + offset (0x0A50)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | presetn_ddr_standby_ch1<br>When high, reset relative logic |
| 14 | RW | 0x0 | presetn_ddr_mon_ch1<br>When high, reset relative logic |
| 13 | RW | 0x0 | presetn_ddr_dfictl_ch1<br>When high, reset relative logic |
| 12 | RW | 0x0 | aresetn_ddr_upctl_ch0<br>When high, reset relative logic |
| 11 | RW | 0x0 | resetn_ddr_standby_ch0<br>When high, reset relative logic |
| 10 | RW | 0x0 | resetn_ddr_mon_ch0<br>When high, reset relative logic |
| 9 | RW | 0x0 | resetn_ddr_dfictl_ch0<br>When high, reset relative logic |
| 8 | RW | 0x0 | resetn_ddr_upctl_ch0<br>When high, reset relative logic |
| 7 | RW | 0x0 | resetn_sbr_ch0<br>When high, reset relative logic |
| 6 | RW | 0x1 | resetn_dfi_ch0<br>When high, reset relative logic |
| 5 | RW | 0x0 | presetn_ddr_grf_ch01<br>ddr ch0 and ch1 grf presetn<br>When high, reset relative logic |
| 4 | RW | 0x0 | tmresetn_ddr_mon_ch0<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_ddr_upctl_ch0<br>When high, reset relative logic |
| 2 | RW | 0x0 | presetn_ddr_standby_ch0<br>When high, reset relative logic |
| 1 | RW | 0x0 | presetn_ddr_mon_ch0<br>When high, reset relative logic |
| 0 | RW | 0x0 | presetn_ddr_dfictl_ch0<br>When high, reset relative logic |

**CRU_SOFTRST_CON21**

Address: Operational Base + offset (0x0A54)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | aresetn_ddr_frs_ddrsch0<br>When high, reset relative logic |
| 14 | RW | 0x0 | aresetn_ddr_rs_ddrsch0<br>When high, reset relative logic |
| 13 | RW | 0x0 | aresetn_ddr_ddrsch0<br>When high, reset relative logic |
| 12:9 | RO | 0x0 | reserved |
| 8 | RW | 0x0 | aresetn_ddr_upctl_ch1<br>When high, reset relative logic |
| 7 | RW | 0x0 | resetn_ddr_standby_ch1<br>When high, reset relative logic |
| 6 | RW | 0x0 | resetn_ddr_mon_ch1<br>When high, reset relative logic |
| 5 | RW | 0x0 | resetn_ddr_dfictl_ch1<br>When high, reset relative logic |
| 4 | RW | 0x0 | resetn_ddr_upctl_ch1<br>When high, reset relative logic |
| 3 | RW | 0x0 | resetn_sbr_ch1<br>When high, reset relative logic |
| 2 | RW | 0x1 | resetn_dfi_ch1<br>When high, reset relative logic |
| 1 | RW | 0x0 | tmresetn_ddr_mon_ch1<br>When high, reset relative logic |
| 0 | RW | 0x0 | presetn_ddr_upctl_ch1<br>When high, reset relative logic |

**CRU_SOFTRST_CON22**

Address: Operational Base + offset (0x0A58)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | presetn_ddr_ddrsch1<br>When high, reset relative logic |
| 7 | RW | 0x0 | presetn_ddr_ddrsch0<br>When high, reset relative logic |
| 6 | RW | 0x0 | aresetn_ddr_frs_scramble1<br>When high, reset relative logic |
| 5 | RW | 0x0 | aresetn_ddr_scramble1<br>When high, reset relative logic |
| 4 | RW | 0x0 | aresetn_ddr_frs_ddrsch1<br>When high, reset relative logic |
| 3 | RW | 0x0 | aresetn_ddr_rs_ddrsch1<br>When high, reset relative logic |
| 2 | RW | 0x0 | aresetn_ddr_ddrsch1<br>When high, reset relative logic |
| 1 | RW | 0x0 | aresetn_ddr_frs_scramble0<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | aresetn_ddr_scramble0<br>When high, reset relative logic |

**CRU_SOFTRST_CON23**

Address: Operational Base + offset (0x0A5C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | presetn_ddr_standby_ch3<br>When high, reset relative logic |
| 14 | RW | 0x0 | presetn_ddr_mon_ch3<br>When high, reset relative logic |
| 13 | RW | 0x0 | presetn_ddr_dfictl_ch3<br>When high, reset relative logic |
| 12 | RW | 0x0 | aresetn_ddr_upctl_ch2<br>When high, reset relative logic |
| 11 | RW | 0x0 | resetn_ddr_standby_ch2<br>When high, reset relative logic |
| 10 | RW | 0x0 | resetn_ddr_mon_ch2<br>When high, reset relative logic |
| 9 | RW | 0x0 | resetn_ddr_dfictl_ch2<br>When high, reset relative logic |
| 8 | RW | 0x0 | resetn_ddr_upctl_ch2<br>When high, reset relative logic |
| 7 | RW | 0x0 | resetn_sbr_ch2<br>When high, reset relative logic |
| 6 | RW | 0x1 | resetn_dfi_ch2<br>When high, reset relative logic |
| 5 | RW | 0x0 | presetn_ddr_grf_ch23<br>ddr ch2 and ch3 grf presetn<br>When high, reset relative logic |
| 4 | RW | 0x0 | tmresetn_ddr_mon_ch2<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_ddr_upctl_ch2<br>When high, reset relative logic |
| 2 | RW | 0x0 | presetn_ddr_standby_ch2<br>When high, reset relative logic |
| 1 | RW | 0x0 | presetn_ddr_mon_ch2<br>When high, reset relative logic |
| 0 | RW | 0x0 | presetn_ddr_dfictl_ch2<br>When high, reset relative logic |

**CRU_SOFTRST_CON24**

Address: Operational Base + offset (0x0A60)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | aresetn_ddr_frs_ddrsch2<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14 | RW | 0x0 | aresetn_ddr_rs_ddrsch2<br>When high, reset relative logic |
| 13 | RW | 0x0 | aresetn_ddr_ddrsch2<br>When high, reset relative logic |
| 12:9 | RO | 0x0 | reserved |
| 8 | RW | 0x0 | aresetn_ddr_upctl_ch3<br>When high, reset relative logic |
| 7 | RW | 0x0 | resetn_ddr_standby_ch3<br>When high, reset relative logic |
| 6 | RW | 0x0 | resetn_ddr_mon_ch3<br>When high, reset relative logic |
| 5 | RW | 0x0 | resetn_ddr_dfictl_ch3<br>When high, reset relative logic |
| 4 | RW | 0x0 | resetn_ddr_upctl_ch3<br>When high, reset relative logic |
| 3 | RW | 0x0 | resetn_sbr_ch3<br>When high, reset relative logic |
| 2 | RW | 0x1 | resetn_dfi_ch3<br>When high, reset relative logic |
| 1 | RW | 0x0 | tmresetn_ddr_mon_ch3<br>When high, reset relative logic |
| 0 | RW | 0x0 | presetn_ddr_upctl_ch3<br>When high, reset relative logic |

**CRU_SOFTRST_CON25**

Address: Operational Base + offset (0x0A64)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | presetn_ddr_ddrsch3<br>When high, reset relative logic |
| 7 | RW | 0x0 | presetn_ddr_ddrsch2<br>When high, reset relative logic |
| 6 | RW | 0x0 | aresetn_ddr_frs_scramble3<br>When high, reset relative logic |
| 5 | RW | 0x0 | aresetn_ddr_scramble3<br>When high, reset relative logic |
| 4 | RW | 0x0 | aresetn_ddr_frs_ddrsch3<br>When high, reset relative logic |
| 3 | RW | 0x0 | aresetn_ddr_rs_ddrsch3<br>When high, reset relative logic |
| 2 | RW | 0x0 | aresetn_ddr_ddrsch3<br>When high, reset relative logic |
| 1 | RW | 0x0 | aresetn_ddr_frs_scramble2<br>When high, reset relative logic |
| 0 | RW | 0x0 | aresetn_ddr_scramble2<br>When high, reset relative logic |

**CRU_SOFTRST_CON26**

Address: Operational Base + offset (0x0A68)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | hresetn_isp1_biu<br>When high, reset relative logic |
| 7 | RO | 0x0 | reserved |
| 6 | RW | 0x0 | aresetn_isp1_biu<br>When high, reset relative logic |
| 5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | resetn_isp1_vicap<br>When high, reset relative logic |
| 3 | RW | 0x0 | resetn_isp1<br>When high, reset relative logic |
| 2:0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON27**

Address: Operational Base + offset (0x0A6C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | hresetn_rknn1_biu<br>When high, reset relative logic |
| 2 | RW | 0x0 | hresetn_rknn1<br>When high, reset relative logic |
| 1 | RW | 0x0 | aresetn_rknn1_biu<br>When high, reset relative logic |
| 0 | RW | 0x0 | aresetn_rknn1<br>When high, reset relative logic |

**CRU_SOFTRST_CON28**

Address: Operational Base + offset (0x0A70)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | hresetn_rknn2_biu<br>When high, reset relative logic |
| 2 | RW | 0x0 | hresetn_rknn2<br>When high, reset relative logic |
| 1 | RW | 0x0 | aresetn_rknn2_biu<br>When high, reset relative logic |
| 0 | RW | 0x0 | aresetn_rknn2<br>When high, reset relative logic |

**CRU_SOFTRST_CON29**

Address: Operational Base + offset (0x0A74)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | resetn_pvtm1<br>When high, reset relative logic |
| 13 | RW | 0x0 | presetn_npu_grf<br>When high, reset relative logic |
| 12 | RW | 0x0 | presetn_pvtm1<br>When high, reset relative logic |
| 11 | RW | 0x0 | tresetn_npu_wdt<br>When high, reset relative logic |
| 10 | RW | 0x0 | presetn_npu_wdt<br>When high, reset relative logic |
| 9 | RW | 0x0 | resetn_nputimer1<br>When high, reset relative logic |
| 8 | RW | 0x0 | resetn_nputimer0<br>When high, reset relative logic |
| 7 | RO | 0x0 | reserved |
| 6 | RW | 0x0 | presetn_npu_timer<br>When high, reset relative logic |
| 5 | RW | 0x0 | presetn_nputop_biu<br>When high, reset relative logic |
| 4 | RO | 0x0 | reserved |
| 3 | RW | 0x0 | aresetn_rknn_dsu0<br>When high, reset relative logic |
| 2:0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON30**

Address: Operational Base + offset (0x0A78)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | hresetn_rknn0_biu<br>When high, reset relative logic |
| 8 | RW | 0x0 | hresetn_rknn0<br>When high, reset relative logic |
| 7 | RW | 0x0 | aresetn_rknn0_biu<br>When high, reset relative logic |
| 6 | RW | 0x0 | aresetn_rknn0<br>When high, reset relative logic |
| 5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | tresetn_npu_cm0_jtag<br>When high, reset relative logic |
| 3 | RW | 0x1 | fresetn_npu_cm0_core<br>When high, reset relative logic |
| 2 | RW | 0x0 | hresetn_npu_cm0_biu<br>When high, reset relative logic |
| 1 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | resetn_npu_pvtpll<br>When high, reset relative logic |

**CRU_SOFTRST_CON31**

Address: Operational Base + offset (0x0A7C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | hresetn_sfc_xip<br>When high, reset relative logic |
| 10 | RW | 0x0 | hresetn_sfc<br>When high, reset relative logic |
| 9 | RW | 0x0 | sresetn_sfc<br>When high, reset relative logic |
| 8 | RW | 0x0 | tresetn_emmc<br>When high, reset relative logic |
| 7 | RW | 0x0 | bresetn_emmc<br>When high, reset relative logic |
| 6 | RW | 0x0 | cresetn_emmc<br>When high, reset relative logic |
| 5 | RW | 0x0 | aresetn_emmc<br>When high, reset relative logic |
| 4 | RW | 0x0 | hresetn_emmc<br>When high, reset relative logic |
| 3 | RW | 0x0 | aresetn_nvm_biu<br>When high, reset relative logic |
| 2 | RW | 0x0 | hresetn_nvm_biu<br>When high, reset relative logic |
| 1:0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON32**

Address: Operational Base + offset (0x0A80)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | resetn_pcie_1l0_power_up<br>When high, reset relative logic |
| 14 | RW | 0x1 | resetn_pcie_2l_power_up<br>When high, reset relative logic |
| 13 | RW | 0x1 | resetn_pcie_4l_power_up<br>When high, reset relative logic |
| 12 | RW | 0x0 | aresetn_pcie_biu<br>When high, reset relative logic |
| 11 | RW | 0x0 | aresetn_gmac1<br>When high, reset relative logic |
| 10 | RW | 0x0 | aresetn_gmac0<br>When high, reset relative logic |
| 9 | RW | 0x0 | aresetn_php_biu<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | aresetn_pcie_bridge<br>When high, reset relative logic |
| 7:6 | RO | 0x0 | reserved |
| 5 | RW | 0x0 | presetn_php_biu<br>When high, reset relative logic |
| 4:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | presetn_dec_biu<br>When high, reset relative logic |
| 1 | RW | 0x0 | presetn_grf<br>When high, reset relative logic |
| 0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON33**

Address: Operational Base + offset (0x0A84)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | presetn_pcie_1l1<br>When high, reset relative logic |
| 14 | RW | 0x0 | presetn_pcie_1l0<br>When high, reset relative logic |
| 13 | RW | 0x0 | presetn_pcie_2l<br>When high, reset relative logic |
| 12 | RW | 0x0 | presetn_pcie_4l<br>When high, reset relative logic |
| 11:2 | RO | 0x000 | reserved |
| 1 | RW | 0x1 | resetn_pcie_1l2_power_up<br>When high, reset relative logic |
| 0 | RW | 0x1 | resetn_pcie_1l1_power_up<br>When high, reset relative logic |

**CRU_SOFTRST_CON34**

Address: Operational Base + offset (0x0A88)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | aresetn_mmu_biu<br>When high, reset relative logic |
| 8 | RW | 0x0 | aresetn_mmu_php<br>When high, reset relative logic |
| 7 | RW | 0x0 | aresetn_mmu_pcie<br>When high, reset relative logic |
| 6 | RW | 0x0 | aresetn_php_gic_its<br>When high, reset relative logic |
| 5:1 | RO | 0x00 | reserved |
| 0 | RW | 0x0 | presetn_pcie_1l2<br>When high, reset relative logic |

**CRU_SOFTRST_CON35**

Rockchip Confidencial

Address: Operational Base + offset (0x0A8C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | aresetn_usb3otg2<br>When high, reset relative logic |
| 6:0 | RO | 0x00 | reserved |

**CRU_SOFTRST_CON37**

Address: Operational Base + offset (0x0A94)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | resetn_asic2<br>When high, reset relative logic |
| 14 | RW | 0x0 | resetn_asic1<br>When high, reset relative logic |
| 13 | RW | 0x0 | resetn_asic0<br>When high, reset relative logic |
| 12 | RW | 0x0 | resetn_rxoob2<br>When high, reset relative logic |
| 11 | RW | 0x0 | resetn_rxoob1<br>When high, reset relative logic |
| 10 | RW | 0x0 | resetn_rxoob0<br>When high, reset relative logic |
| 9 | RW | 0x0 | aresetn_sata2<br>When high, reset relative logic |
| 8 | RW | 0x0 | aresetn_sata1<br>When high, reset relative logic |
| 7 | RW | 0x0 | aresetn_sata0<br>When high, reset relative logic |
| 6 | RW | 0x0 | resetn_pmalive2<br>When high, reset relative logic |
| 5 | RW | 0x0 | resetn_pmalive1<br>When high, reset relative logic |
| 4 | RW | 0x0 | resetn_pmalive0<br>When high, reset relative logic |
| 3:0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON40**

Address: Operational Base + offset (0x0AA0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | resetn_rkvdec0_core<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | resetn_rkvdec0_hevc_ca<br>When high, reset relative logic |
| 7 | RW | 0x0 | resetn_rkvdec0_ca<br>When high, reset relative logic |
| 6 | RW | 0x0 | aresetn_rkvdec0_biu<br>When high, reset relative logic |
| 5 | RW | 0x0 | hresetn_rkvdec0_biu<br>When high, reset relative logic |
| 4 | RW | 0x0 | aresetn_rkvdec0<br>When high, reset relative logic |
| 3 | RW | 0x0 | hresetn_rkvdec0<br>When high, reset relative logic |
| 2 | RW | 0x0 | aresetn_rkvdec_ccu<br>When high, reset relative logic |
| 1:0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON41**

Address: Operational Base + offset (0x0AA4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | resetn_rkvdec1_core<br>When high, reset relative logic |
| 7 | RW | 0x0 | resetn_rkvdec1_hevc_ca<br>When high, reset relative logic |
| 6 | RW | 0x0 | resetn_rkvdec1_ca<br>When high, reset relative logic |
| 5 | RW | 0x0 | aresetn_rkvdec1_biu<br>When high, reset relative logic |
| 4 | RW | 0x0 | hresetn_rkvdec1_biu<br>When high, reset relative logic |
| 3 | RW | 0x0 | aresetn_rkvdec1<br>When high, reset relative logic |
| 2 | RW | 0x0 | hresetn_rkvdec1<br>When high, reset relative logic |
| 1:0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON42**

Address: Operational Base + offset (0x0AA8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | cresetn_usb2p0_host0<br>When high, reset relative logic |
| 14 | RW | 0x0 | aresetn_usb_grf<br>When high, reset relative logic |
| 13 | RW | 0x0 | hresetn_host_arb1<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | hresetn_host1<br>When high, reset relative logic |
| 11 | RW | 0x0 | hresetn_host_arb0<br>When high, reset relative logic |
| 10 | RW | 0x0 | hresetn_host0<br>When high, reset relative logic |
| 9:8 | RO | 0x0 | reserved |
| 7 | RW | 0x0 | aresetn_usb3otg1<br>When high, reset relative logic |
| 6:5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | aresetn_usb3otg0<br>When high, reset relative logic |
| 3 | RW | 0x0 | hresetn_usb_biu<br>When high, reset relative logic |
| 2 | RW | 0x0 | aresetn_usb_biu<br>When high, reset relative logic |
| 1:0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON43**

Address: Operational Base + offset (0x0AAC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:3 | RO | 0x0000 | reserved |
| 2 | RW | 0x0 | resetn_host_utmi1<br>When high, reset relative logic |
| 1 | RW | 0x0 | resetn_host_utmi0<br>When high, reset relative logic |
| 0 | RW | 0x0 | cresetn_usb2p0_host1<br>When high, reset relative logic |

**CRU_SOFTRST_CON44**

Address: Operational Base + offset (0x0AB0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | hresetn_jpeg_encoder2<br>When high, reset relative logic |
| 14 | RW | 0x0 | aresetn_jpeg_encoder2<br>When high, reset relative logic |
| 13 | RW | 0x0 | hresetn_jpeg_encoder1<br>When high, reset relative logic |
| 12 | RW | 0x0 | aresetn_jpeg_encoder1<br>When high, reset relative logic |
| 11 | RW | 0x0 | hresetn_jpeg_encoder0<br>When high, reset relative logic |
| 10 | RW | 0x0 | aresetn_jpeg_encoder0<br>When high, reset relative logic |
| 9 | RW | 0x0 | hresetn_vpu<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | aresetn_vpu<br>When high, reset relative logic |
| 7 | RW | 0x0 | aresetn_jpeg_decoder_biu<br>When high, reset relative logic |
| 6 | RW | 0x0 | hresetn_vdpu_biu<br>When high, reset relative logic |
| 5 | RW | 0x0 | aresetn_vdpu_low_biu<br>When high, reset relative logic |
| 4 | RW | 0x0 | aresetn_vdpu_biu<br>When high, reset relative logic |
| 3:0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON45**

Address: Operational Base + offset (0x0AB4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | resetn_rga3_0_core<br>When high, reset relative logic |
| 11 | RW | 0x0 | aresetn_rga3_0<br>When high, reset relative logic |
| 10 | RW | 0x0 | hresetn_rga3_0<br>When high, reset relative logic |
| 9 | RW | 0x0 | resetn_rga2_core<br>When high, reset relative logic |
| 8 | RW | 0x0 | aresetn_rga2<br>When high, reset relative logic |
| 7 | RW | 0x0 | hresetn_rga2<br>When high, reset relative logic |
| 6 | RW | 0x0 | resetn_iep2p0_core<br>When high, reset relative logic |
| 5 | RW | 0x0 | aresetn_iep2p0<br>When high, reset relative logic |
| 4 | RW | 0x0 | hresetn_iep2p0<br>When high, reset relative logic |
| 3 | RW | 0x0 | hresetn_jpeg_decoder<br>When high, reset relative logic |
| 2 | RW | 0x0 | aresetn_jpeg_decoder<br>When high, reset relative logic |
| 1 | RW | 0x0 | hresetn_jpeg_encoder3<br>When high, reset relative logic |
| 0 | RW | 0x0 | aresetn_jpeg_encoder3<br>When high, reset relative logic |

**CRU_SOFTRST_CON47**

Address: Operational Base + offset (0x0ABC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x0 | resetn_rkvenc0_core<br>When high, reset relative logic |
| 5 | RW | 0x0 | aresetn_rkvenc0<br>When high, reset relative logic |
| 4 | RW | 0x0 | hresetn_rkvenc0<br>When high, reset relative logic |
| 3 | RW | 0x0 | aresetn_rkvenc0_biu<br>When high, reset relative logic |
| 2 | RW | 0x0 | hresetn_rkvenc0_biu<br>When high, reset relative logic |
| 1:0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON48**

Address: Operational Base + offset (0x0AC0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x0 | resetn_rkvenc1_core<br>When high, reset relative logic |
| 5 | RW | 0x0 | aresetn_rkvenc1<br>When high, reset relative logic |
| 4 | RW | 0x0 | hresetn_rkvenc1<br>When high, reset relative logic |
| 3 | RW | 0x0 | aresetn_rkvenc1_biu<br>When high, reset relative logic |
| 2 | RW | 0x0 | hresetn_rkvenc1_biu<br>When high, reset relative logic |
| 1:0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON49**

Address: Operational Base + offset (0x0AC4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | resetn_isp0_vicap<br>When high, reset relative logic |
| 10 | RW | 0x0 | resetn_isp0<br>When high, reset relative logic |
| 9 | RO | 0x0 | reserved |
| 8 | RW | 0x0 | hresetn_vicap<br>When high, reset relative logic |
| 7 | RW | 0x0 | aresetn_vicap<br>When high, reset relative logic |
| 6 | RW | 0x0 | dresetn_vicap<br>When high, reset relative logic |
| 5 | RW | 0x0 | presetn_vi_biu<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | hresetn_vi_biu<br>When high, reset relative logic |
| 3 | RW | 0x0 | aresetn_vi_biu<br>When high, reset relative logic |
| 2:0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON50**

Address: Operational Base + offset (0x0AC8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | presetn_csi_host_5<br>When high, reset relative logic |
| 8 | RW | 0x0 | presetn_csi_host_4<br>When high, reset relative logic |
| 7 | RW | 0x0 | presetn_csi_host_3<br>When high, reset relative logic |
| 6 | RW | 0x0 | presetn_csi_host_2<br>When high, reset relative logic |
| 5 | RW | 0x0 | presetn_csi_host_1<br>When high, reset relative logic |
| 4 | RW | 0x0 | presetn_csi_host_0<br>When high, reset relative logic |
| 3 | RW | 0x0 | resetn_fisheye1<br>When high, reset relative logic |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | resetn_fisheye0<br>When high, reset relative logic |

**CRU_SOFTRST_CON51**

Address: Operational Base + offset (0x0ACC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | resetn_cifin<br>When high, reset relative logic |
| 12:10 | RO | 0x0 | reserved |
| 9 | RW | 0x0 | resetn_csihost5_vicap<br>When high, reset relative logic |
| 8 | RW | 0x0 | resetn_csihost4_vicap<br>When high, reset relative logic |
| 7 | RW | 0x0 | resetn_csihost3_vicap<br>When high, reset relative logic |
| 6 | RW | 0x0 | resetn_csihost2_vicap<br>When high, reset relative logic |
| 5 | RW | 0x0 | resetn_csihost1_vicap<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | resetn_csihost0_vicap<br>When high, reset relative logic |
| 3:0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON52**

Address: Operational Base + offset (0x0AD0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | dresetn_vp2hdmi_bridge1<br>When high, reset relative logic |
| 14 | RW | 0x0 | dresetn_vp2hdmi_bridge0<br>When high, reset relative logic |
| 13 | RW | 0x0 | dresetn_vp0<br>When high, reset relative logic |
| 12:10 | RO | 0x0 | reserved |
| 9 | RW | 0x0 | aresetn_vop<br>When high, reset relative logic |
| 8 | RW | 0x0 | hresetn_vop<br>When high, reset relative logic |
| 7 | RW | 0x0 | presetn_vop_biu<br>When high, reset relative logic |
| 6 | RW | 0x0 | hresetn_vop_biu<br>When high, reset relative logic |
| 5 | RW | 0x0 | aresetn_vop_low_biu<br>When high, reset relative logic |
| 4 | RW | 0x0 | aresetn_vop_biu<br>When high, reset relative logic |
| 3:0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON53**

Address: Operational Base + offset (0x0AD4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | presetn_vop_channel_biu<br>When high, reset relative logic |
| 8 | RW | 0x0 | resetn_vop_pmu<br>When high, reset relative logic |
| 7 | RW | 0x0 | resetn_dsihost1<br>When high, reset relative logic |
| 6 | RW | 0x0 | resetn_dsihost0<br>When high, reset relative logic |
| 5 | RW | 0x0 | presetn_dsihost1<br>When high, reset relative logic |
| 4 | RW | 0x0 | presetn_dsihost0<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_vopgrf<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | dresetn_vp3<br>When high, reset relative logic |
| 1 | RW | 0x0 | dresetn_vp2<br>When high, reset relative logic |
| 0 | RW | 0x0 | dresetn_vp1<br>When high, reset relative logic |

**CRU_SOFTRST_CON55**

Address: Operational Base + offset (0x0ADC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | resetn_hdcp0<br>When high, reset relative logic |
| 14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | hresetn_hdcp0<br>When high, reset relative logic |
| 12 | RW | 0x0 | aresetn_hdcp0<br>When high, reset relative logic |
| 11 | RW | 0x0 | hresetn_hdcp_key0<br>When high, reset relative logic |
| 10 | RW | 0x0 | presetn_vo0grf<br>When high, reset relative logic |
| 9 | RW | 0x0 | aresetn_hdcp0_biu<br>When high, reset relative logic |
| 8 | RW | 0x0 | presetn_vo0_s_biu<br>When high, reset relative logic |
| 7 | RW | 0x0 | presetn_vo0_biu<br>When high, reset relative logic |
| 6 | RW | 0x0 | hresetn_vo0_s_biu<br>When high, reset relative logic |
| 5 | RW | 0x0 | hresetn_vo0_biu<br>When high, reset relative logic |
| 4:0 | RO | 0x00 | reserved |

**CRU_SOFTRST_CON56**

Address: Operational Base + offset (0x0AE0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | hresetn_i2s8_8ch<br>When high, reset relative logic |
| 13 | RW | 0x0 | mresetn_i2s4_8ch_tx<br>When high, reset relative logic |
| 12:11 | RO | 0x0 | reserved |
| 10 | RW | 0x0 | hresetn_i2s4_8ch<br>When high, reset relative logic |
| 9 | RW | 0x0 | resetn_dp1<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | resetn_dp0<br>When high, reset relative logic |
| 7:2 | RO | 0x00 | reserved |
| 1 | RW | 0x0 | presetn_trng0<br>When high, reset relative logic |
| 0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON57**

Address: Operational Base + offset (0x0AE4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | mresetn_spdif5_dp1<br>When high, reset relative logic |
| 10:8 | RO | 0x0 | reserved |
| 7 | RW | 0x0 | hresetn_spdif5_dp1<br>When high, reset relative logic |
| 6 | RW | 0x0 | mresetn_spdif2_dp0<br>When high, reset relative logic |
| 5:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | hresetn_spdif2_dp0<br>When high, reset relative logic |
| 1 | RW | 0x0 | mresetn_i2s8_8ch_tx<br>When high, reset relative logic |
| 0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON59**

Address: Operational Base + offset (0x0AEC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | presetn_vo1_s_biu<br>When high, reset relative logic |
| 12 | RW | 0x0 | presetn_vo1grf<br>When high, reset relative logic |
| 11 | RW | 0x0 | hresetn_vo1_biu<br>When high, reset relative logic |
| 10 | RW | 0x0 | hresetn_vo1_s_biu<br>When high, reset relative logic |
| 9 | RW | 0x0 | hresetn_vo1_biu<br>When high, reset relative logic |
| 8 | RW | 0x0 | aresetn_vo1_biu<br>When high, reset relative logic |
| 7 | RO | 0x0 | reserved |
| 6 | RW | 0x0 | aresetn_hdcp1_biu<br>When high, reset relative logic |
| 5:0 | RO | 0x00 | reserved |

Rockchip Confidencial

**CRU_SOFTRST_CON60**

Address: Operational Base + offset (0x0AF0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | presetn_hdmitx0<br>When high, reset relative logic |
| 10 | RW | 0x0 | presetn_trng1<br>When high, reset relative logic |
| 9 | RO | 0x0 | reserved |
| 8 | RW | 0x0 | resetn_hdcp1<br>When high, reset relative logic |
| 7 | RO | 0x0 | reserved |
| 6 | RW | 0x0 | hresetn_hdcp1<br>When high, reset relative logic |
| 5 | RW | 0x0 | aresetn_hdcp1<br>When high, reset relative logic |
| 4 | RW | 0x0 | hresetn_hdcp_key1<br>When high, reset relative logic |
| 3 | RW | 0x0 | mresetn_i2s7_8ch_rx<br>When high, reset relative logic |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | hresetn_i2s7_8ch<br>When high, reset relative logic |

**CRU_SOFTRST_CON61**

Address: Operational Base + offset (0x0AF4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | resetn_hdmirx_ref<br>When high, reset relative logic |
| 10 | RW | 0x0 | presetn_hdmirx<br>When high, reset relative logic |
| 9 | RW | 0x0 | aresetn_hdmirx<br>When high, reset relative logic |
| 8 | RO | 0x0 | reserved |
| 7 | RW | 0x0 | resetn_hdmitx1_ref<br>When high, reset relative logic |
| 6:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | presetn_hdmitx1<br>When high, reset relative logic |
| 1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | resetn_hdmitx0_ref<br>When high, reset relative logic |

**CRU_SOFTRST_CON62**

Address: Operational Base + offset (0x0AF8)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | mresetn_i2s6_8ch_tx<br>When high, reset relative logic |
| 14:13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | hresetn_i2s5_8ch<br>When high, reset relative logic |
| 11:9 | RO | 0x0 | reserved |
| 8 | RW | 0x0 | mresetn_i2s5_8ch_tx<br>When high, reset relative logic |
| 7:5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | resetn_edp1_24m<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_edp1<br>When high, reset relative logic |
| 2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | resetn_edp0_24m<br>When high, reset relative logic |
| 0 | RW | 0x0 | presetn_edp0<br>When high, reset relative logic |

**CRU_SOFTRST_CON63**

Address: Operational Base + offset (0x0AFC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | mresetn_spdifrx1<br>When high, reset relative logic |
| 14 | RW | 0x0 | hresetn_spdifrx1<br>When high, reset relative logic |
| 13 | RW | 0x0 | mresetn_spdifrx0<br>When high, reset relative logic |
| 12 | RW | 0x0 | hresetn_spdifrx0<br>When high, reset relative logic |
| 11 | RW | 0x0 | mresetn_spdif4<br>When high, reset relative logic |
| 10:9 | RO | 0x0 | reserved |
| 8 | RW | 0x0 | hresetn_spdif4<br>When high, reset relative logic |
| 7 | RW | 0x0 | mresetn_spdif3<br>When high, reset relative logic |
| 6:5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | hresetn_spdif3<br>When high, reset relative logic |
| 3 | RW | 0x0 | hresetn_i2s6_8ch<br>When high, reset relative logic |
| 2 | RW | 0x0 | mresetn_i2s6_8ch_rx<br>When high, reset relative logic |
| 1:0 | RO | 0x0 | reserved |

Rockchip Confidencial

**CRU_SOFTRST_CON64**

Address: Operational Base + offset (0x0B00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | resetn_vo1_bridge1<br>When high, reset relative logic |
| 14 | RW | 0x0 | resetn_vo1_bridge0<br>When high, reset relative logic |
| 13 | RW | 0x0 | resetn_linksym_hdmitxphy1<br>When high, reset relative logic |
| 12 | RW | 0x0 | resetn_linksym_hdmitxphy0<br>When high, reset relative logic |
| 11:2 | RO | 0x000 | reserved |
| 1 | RW | 0x0 | mresetn_spdifrx2<br>When high, reset relative logic |
| 0 | RW | 0x0 | hresetn_spdifrx2<br>When high, reset relative logic |

**CRU_SOFTRST_CON65**

Address: Operational Base + offset (0x0B04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | presetn_s_hdmirx<br>When high, reset relative logic |
| 7 | RW | 0x0 | mresetn_i2s10_8ch_rx<br>When high, reset relative logic |
| 6:5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | hresetn_i2s10_8ch<br>When high, reset relative logic |
| 3 | RW | 0x0 | mresetn_i2s9_8ch_rx<br>When high, reset relative logic |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | hresetn_i2s9_8ch<br>When high, reset relative logic |

**CRU_SOFTRST_CON66**

Address: Operational Base + offset (0x0B08)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | presetn_pvtm2<br>When high, reset relative logic |
| 14 | RW | 0x0 | presetn_gpu_biu<br>When high, reset relative logic |
| 13 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | aresetn_m3_gpu_biu<br>When high, reset relative logic |
| 11 | RW | 0x0 | aresetn_m2_gpu_biu<br>When high, reset relative logic |
| 10 | RW | 0x0 | aresetn_m1_gpu_biu<br>When high, reset relative logic |
| 9 | RW | 0x0 | aresetn_m0_gpu_biu<br>When high, reset relative logic |
| 8 | RW | 0x0 | aresetn_s_gpu_biu<br>When high, reset relative logic |
| 7:6 | RO | 0x0 | reserved |
| 5 | RW | 0x0 | sysresetn_gpu<br>When high, reset relative logic |
| 4 | RW | 0x0 | resetn_gpu<br>When high, reset relative logic |
| 3:0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON67**

Address: Operational Base + offset (0x0B0C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:5 | RO | 0x000 | reserved |
| 4 | RW | 0x0 | poresetn_gpu_jtag<br>When high, reset relative logic |
| 3 | RW | 0x0 | resetn_gpu_pvtpll<br>When high, reset relative logic |
| 2 | RW | 0x0 | presetn_gpu_grf<br>When high, reset relative logic |
| 1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | resetn_pvtm2<br>When high, reset relative logic |

**CRU_SOFTRST_CON68**

Address: Operational Base + offset (0x0B10)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x0 | presetn_av1<br>When high, reset relative logic |
| 4 | RW | 0x0 | presetn_av1_biu<br>When high, reset relative logic |
| 3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | aresetn_av1<br>When high, reset relative logic |
| 1 | RW | 0x0 | aresetn_av1_biu<br>When high, reset relative logic |
| 0 | RO | 0x0 | reserved |

Rockchip Confidencial

**CRU_SOFTRST_CON69**

Address: Operational Base + offset (0x0B14)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x1 | fresetn_ddr_cm0_core<br>When high, reset relative logic |
| 13 | RW | 0x0 | hresetn_center_biu<br>When high, reset relative logic |
| 12 | RW | 0x0 | hresetn_ahb2apb<br>When high, reset relative logic |
| 11 | RW | 0x0 | aresetn_center_s400_biu<br>When high, reset relative logic |
| 10 | RW | 0x0 | aresetn_center_s200_biu<br>When high, reset relative logic |
| 9:8 | RO | 0x0 | reserved |
| 7 | RW | 0x0 | aresetn_ddr_sharemem_biu<br>When high, reset relative logic |
| 6 | RW | 0x0 | aresetn_ddr_sharemem<br>When high, reset relative logic |
| 5 | RW | 0x0 | aresetn_dma2ddr<br>When high, reset relative logic |
| 4 | RW | 0x0 | aresetn_ddr_biu<br>When high, reset relative logic |
| 3:0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON70**

Address: Operational Base + offset (0x0B18)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | presetn_center_channel_biu<br>When high, reset relative logic |
| 11 | RW | 0x0 | presetn_center_biu<br>When high, reset relative logic |
| 10 | RW | 0x0 | presetn_sharemem<br>When high, reset relative logic |
| 9 | RW | 0x0 | presetn_dma2ddr<br>When high, reset relative logic |
| 8 | RW | 0x0 | presetn_timer<br>When high, reset relative logic |
| 7 | RW | 0x0 | presetn_wdt<br>When high, reset relative logic |
| 6 | RW | 0x0 | presetn_ahb2apb<br>When high, reset relative logic |
| 5 | RW | 0x0 | presetn_center_grf<br>When high, reset relative logic |
| 4 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | tresetn_ddr_cm0_jtag<br>When high, reset relative logic |
| 2 | RW | 0x0 | tresetn_wdt_ddr<br>When high, reset relative logic |
| 1 | RW | 0x0 | resetn_ddr_timer1<br>When high, reset relative logic |
| 0 | RW | 0x0 | resetn_ddr_timer0<br>When high, reset relative logic |

**CRU_SOFTRST_CON72**

Address: Operational Base + offset (0x0B20)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | presetn_usb2phy_u2_1_grf0<br>When high, reset relative logic |
| 10 | RW | 0x0 | presetn_usb2phy_u2_0_grf0<br>When high, reset relative logic |
| 9 | RW | 0x0 | presetn_usb2phy_u3_1_grf0<br>When high, reset relative logic |
| 8 | RW | 0x0 | presetn_usb2phy_u3_0_grf0<br>When high, reset relative logic |
| 7 | RW | 0x0 | presetn_apb2asb_slv_bot_right<br>When high, reset relative logic |
| 6 | RW | 0x0 | presetn_hdptx1<br>When high, reset relative logic |
| 5 | RW | 0x0 | presetn_hdptx0<br>When high, reset relative logic |
| 4 | RW | 0x0 | presetn_usbdpphy1<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_usbdpgrf1<br>When high, reset relative logic |
| 2 | RW | 0x0 | presetn_usbdpphy0<br>When high, reset relative logic |
| 1 | RW | 0x0 | presetn_usbdpgrf0<br>When high, reset relative logic |
| 0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON73**

Address: Operational Base + offset (0x0B24)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | resetn_hdmihdp1<br>When high, reset relative logic |
| 12 | RW | 0x0 | resetn_hdmihdp0<br>When high, reset relative logic |
| 11:0 | RO | 0x000 | reserved |

Rockchip Confidencial

**CRU_SOFTRST_CON74**

Address: Operational Base + offset (0x0B28)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | hresetn_vo1usb_top_biu<br>When high, reset relative logic |
| 2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | aresetn_vo1usb_top_biu<br>When high, reset relative logic |
| 0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON75**

Address: Operational Base + offset (0x0B2C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | resetn_sdio<br>When high, reset relative logic |
| 2 | RW | 0x0 | hresetn_sdio<br>When high, reset relative logic |
| 1 | RW | 0x0 | hresetn_sdio_biu<br>When high, reset relative logic |
| 0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON76**

Address: Operational Base + offset (0x0B30)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x0 | resetn_rga3_1_core<br>When high, reset relative logic |
| 5 | RW | 0x0 | aresetn_rga3_1<br>When high, reset relative logic |
| 4 | RW | 0x0 | hresetn_rga3_1<br>When high, reset relative logic |
| 3 | RW | 0x0 | aresetn_rga3_biu<br>When high, reset relative logic |
| 2 | RW | 0x0 | hresetn_rga3_biu<br>When high, reset relative logic |
| 1:0 | RO | 0x0 | reserved |

**CRU_SOFTRST_CON77**

Address: Operational Base + offset (0x0B34)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | resetn_ref_pipe_phy2<br>When high, reset relative logic |
| 7 | RW | 0x0 | resetn_ref_pipe_phy1<br>When high, reset relative logic |
| 6 | RW | 0x0 | resetn_ref_pipe_phy0<br>When high, reset relative logic |
| 5:0 | RO | 0x00 | reserved |

**CRU_GLB_CNT_TH**

Address: Operational Base + offset (0x0C00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9:0 | RW | 0x064 | global_reset_counter_threshold<br>global_reset_counter_threshold<br>Global soft reset, wdt reset or tsadc_shut reset asserted time counter threshold. Measured in OSC clock cycles |

**CRU_GLBRST_ST**

Address: Operational Base + offset (0x0C04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15 | RW | 0x0 | glbrst_wdt4_rst<br>glbrst_wdt4_rst<br>If High, global reset by WDT4. |
| 14 | RW | 0x0 | glbrst_wdt3_rst<br>glbrst_wdt3_rst<br>If High, global reset by WDT3. |
| 13 | RW | 0x0 | glbrst_wdt2_rst<br>glbrst_wdt2_rst<br>If High, global reset by WDT2. |
| 12 | RW | 0x0 | glbrst_wdt1_rst<br>glbrst_wdt1_rst<br>If High, global reset by WDT1. |
| 11 | RW | 0x0 | glbrst_wdt0_rst<br>glbrst_wdt0_rst<br>If High, global reset by WDT0. |
| 10 | RW | 0x0 | glbrst_sgrf_crc_chk_rst<br>glbrst_sgrf_crc_chk_rst<br>If High, global reset by SGRF_CRC check. |
| 9 | RW | 0x0 | glbrst_dsusgrf_crc_chk_rst<br>glbrst_dsusgrf_crc_chk_rst<br>If High, global reset by DSUSGRF_CRC check. |
| 8 | RW | 0x0 | glbrst_pmusgrf_crc_chk_rst<br>glbrst_pmusgrf_crc_chk_rst<br>If High, global reset by PMUSGRF_CRC check. |
| 7 | RW | 0x0 | glbrst_osc_chk_rst<br>glbrst_osc_chk_rst<br>If High, global reset by OSC check. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | glbrst_wdt_rst<br>glbrst_wdt_rst<br>If High, global reset by WDT.<br>Check CRU_GLBRST_ST[15:11] for detail. |
| 5 | RW | 0x0 | second_glbrst_wdt_rst<br>second_glbrst_wdt_rst<br>If High, second global reset by WDT. |
| 4 | RW | 0x0 | first_glbrst_wdt_rst<br>first_glbrst_wdt_rst<br>If High, first global reset by WDT. |
| 3 | RW | 0x0 | second_glbrst_tsadc_rst<br>second_glbrst_tsadc_rst<br>If High, second global reset by TSADC. |
| 2 | RW | 0x0 | first_glbrst_tsadc_rst<br>first_glbrst_tsadc_rst<br>If High, first global reset by TSADC. |
| 1 | RW | 0x0 | second_glbrst_register_rst<br>second_glbrst_register_rst<br>If High, second global reset by register. |
| 0 | RW | 0x0 | first_glbrst_register_rst<br>first_glbrst_register_rst<br>If High, first global reset by register. |

**CRU_GLB_SRST_FST_VALUE**

Address: Operational Base + offset (0x0C08)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | glb_srsc_first_value<br>GLB_SRST_FST<br>The first global software reset configuration value.<br>Set 0xfdb9 enable. |

**CRU_GLB_SRST_SND_VALUE**

Address: Operational Base + offset (0x0C0C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | glb_srsc_second_value<br>GLB_SRST_SND<br>The second global software reset configuration value.<br>Set 0xeca8 enable. |

**CRU_GLB_RST_CON**

Address: Operational Base + offset (0x0C10)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15 | RW | 0x0 | crc_sgrf_chk_trig_glbrst_sel<br>crc_sgrf_chk_trig_glbrst_sel<br>1'b1: CRC_SGRF check trigger first global reset.<br>1'b0: CRC_SGRF check trigger second global reset. |
| 14 | RW | 0x0 | crc_dsusgrf_chk_trig_glbrst_sel<br>crc_dsusgrf_chk_trig_glbrst_sel<br>1'b1: CRC_DSUSGRF check trigger first global reset.<br>1'b0: CRC_DSUSGRF check trigger second global reset. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | crc_pmusgrf_chk_trig_glbrst_sel<br>crc_pmusgrf_chk_trig_glbrst_sel<br>1'b1: CRC_PMUSGRF check trigger first global reset.<br>1'b0: CRC_PMUSGRF check trigger second global reset. |
| 12 | RW | 0x0 | osc_chk_trig_glbrst_sel<br>osc_chk_trig_glbrst_sel<br>1'b1: OSC check trigger first global reset.<br>1'b0: OSC check trigger second global reset. |
| 11 | RW | 0x0 | wdt_trig_glbrst_sel<br>wdt_trig_glbrst_sel<br>1'b1: WDT trigger first global reset.<br>1'b0: WDT trigger second global reset. |
| 10 | RW | 0x0 | crc_sgrf_chk_trig_glbrst_en<br>crc_sgrf_chk_trig_glbrst_en<br>1'b1: Enable CRC_SGRF check trigger global reset.<br>1'b0: Disable CRC_SGRF check trigger global reset. |
| 9 | RW | 0x0 | crc_dsusgrf_chk_trig_glbrst_en<br>crc_dsusgrf_chk_trig_glbrst_en<br>1'b1: Enable CRC_DSUSGRF check trigger global reset.<br>1'b0: Disable CRC_DSUSGRF check trigger global reset. |
| 8 | RW | 0x0 | crc_pmusgrf_chk_trig_glbrst_en<br>crc_pmusgrf_chk_trig_glbrst_en<br>1'b1: Enable CRC_PMUSGRF check trigger global reset.<br>1'b0: Disable CRC_PMUSGRF check trigger global reset. |
| 7 | RW | 0x0 | osc_chk_trig_glbrst_en<br>osc_chk_trig_glbrst_en<br>1'b1: Enable OSC check trigger global reset.<br>1'b0: Disable OSC check trigger global reset. |
| 6 | RW | 0x0 | wdt_trig_glbrst_en<br>wdt_trig_glbrst_en<br>1'b1: Enable WDT trigger global reset.<br>1'b0: Disable WDT trigger global reset. |
| 5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | wdt_trig_pmu_en<br>wdt_trig_pmu_en<br>1'b1: Enable wdt reset trigger pmu reset.<br>1'b0: Disable wdt reset trigger pmu reset. |
| 3 | RW | 0x0 | glbrst_trig_pmu_en<br>glbrst_trig_pmu_en<br>1'b1: Enable global reset trigger pmu reset.<br>1'b0: Disable global reset trigger pmu reset. |
| 2 | RW | 0x0 | glbrst_trig_pmu_sel<br>glbrst_trig_pmu_sel<br>1'b1: First global reset trigger pmu reset.<br>1'b0: Second global reset trigger pmu reset. |
| 1 | RW | 0x0 | tsadc_trig_glbrst_en<br>tsadc_trig_glbrst_en<br>1'b1: Enable tsadc trigger global reset.<br>1'b0: Disable tsadc trigger global reset. |
| 0 | RW | 0x0 | tsadc_trig_glbrst_sel<br>tsadc_trig_glbrst_sel<br>1'b1: tsadc trigger first global reset.<br>1'b0: tsadc trigger second global reset. |

**CRU_SDIO_CON0**

Rockchip Confidential

Address: Operational Base + offset (0x0C24)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | sdio_con0<br>Refer to chapter SDIO. |

**CRU_SDIO_CON1**

Address: Operational Base + offset (0x0C28)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | sdio_con1<br>Refer to chapter SDIO. |

**CRU_SDMMC_CON0**

Address: Operational Base + offset (0x0C30)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | sdmmc_con0<br>Refer to chapter SDMMC. |

**CRU_SDMMC_CON1**

Address: Operational Base + offset (0x0C34)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | sdmmc_con1<br>Refer to chapter SDMMC. |

**CRU_PHYREF_ALT_GATE_CON**

Address: Operational Base + offset (0x0C38)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | phy1_ref_alt_clk_m_en<br>phy1_ref_alt_clk_m clock gating control.<br>When high, disable clock. |
| 2 | RW | 0x0 | phy1_ref_alt_clk_p_en<br>phy1_ref_alt_clk_p clock gating control.<br>When high, disable clock. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | phy0_ref_alt_clk_m_en<br>phy0_ref_alt_clk_m clock gating control.<br>When high, disable clock. |
| 0 | RW | 0x0 | phy0_ref_alt_clk_p_en<br>phy0_ref_alt_clk_p clock gating control.<br>When high, disable clock. |

**CRU_CM0_GATEMASK_CON**

Address: Operational Base + offset (0x0C3C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x0 | ddrcm0_sclk_cm0s_en<br>ddrcm0_sclk_cm0s clock gating control.<br>When high, disable clock. |
| 4 | RW | 0x0 | ddrcm0_hclk_cm0s_en<br>ddrcm0_hclk_cm0s clock gating control.<br>When high, disable clock. |
| 3 | RW | 0x0 | ddrcm0_dclk_cm0s_en<br>ddrcm0_dclk_cm0s clock gating control.<br>When high, disable clock. |
| 2 | RW | 0x0 | npucm0_sclk_cm0s_en<br>npucm0_sclk_cm0s clock gating control.<br>When high, disable clock. |
| 1 | RW | 0x0 | npucm0_hclk_cm0s_en<br>npucm0_hclk_cm0s clock gating control.<br>When high, disable clock. |
| 0 | RW | 0x0 | npucm0_dclk_cm0s_en<br>npucm0_dclk_cm0s clock gating control.<br>When high, disable clock. |

**CRU_QCHANNEL_CON01**

Address: Operational Base + offset (0x0CA4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | clk_gpu_qc_gate_en<br>qc_gate_en<br>1'b1: Enable clk_gpu qchannel gate function.<br>1'b1: Disable clk_gpu qchannel gate function. |
| 6 | RW | 0x0 | clk_gpu_qc_en<br>qc_en<br>1'b1: Enable clk_gpu qchannel.<br>1'b1: Disable clk_gpu qchannel. |
| 5 | RW | 0x0 | aclk_php_gic_its_qc_gate_en<br>qc_gate_en<br>1'b1: Enable aclk_php_gic_its qchannel gate function.<br>1'b1: Disable aclk_php_gic_its qchannel gate function. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | aclk_php_gic_its_qc_en<br>qc_en<br>1'b1: Enable aclk_php_gic_its qchannel.<br>1'b1: Disable aclk_php_gic_its qchannel. |
| 3 | RW | 0x0 | aclk_gicadb_gic2core_bus_qc_gate_en<br>qc_gate_en<br>1'b1: Enable aclk_gicadb_gic2core_bus qchannel gate function.<br>1'b1: Disable aclk_gicadb_gic2core_bus qchannel gate function. |
| 2 | RW | 0x0 | aclk_gicadb_gic2core_bus_qc_en<br>qc_en<br>1'b1: Enable aclk_gicadb_gic2core_bus qchannel.<br>1'b1: Disable aclk_gicadb_gic2core_bus qchannel. |
| 1 | RW | 0x0 | aclk_gic_qc_gate_en<br>qc_gate_en<br>1'b1: Enable aclk_gic qchannel gate function.<br>1'b1: Disable aclk_gic qchannel gate function. |
| 0 | RW | 0x0 | aclk_gic_qc_en<br>qc_en<br>1'b1: Enable aclk_gic qchannel.<br>1'b1: Disable aclk_gic qchannel. |

**CRU_SMOTH_DIVFREE_CON08**

Address: Operational Base + offset (0x0CC0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | aclk_m0_gpu_freq_keep<br>freq_keep<br>Cycles to keep every step. |
| 15 | RW | 0x0 | aclk_m0_gpu_bypass<br>bypass<br>Division signal bypass.<br>1'b1: Bypass.<br>1'b0: Use Smoothdiv to control clock division. |
| 14 | RW | 0x0 | aclk_m0_gpu_gate_smth_en<br>gate_smth_en<br>If trigger smoothdiv function when clk been gated.<br>1'b1: Enable.<br>1'b0: Disable. |
| 13 | RW | 0x0 | aclk_m0_gpu_smdiv_clk_off<br>smdiv_clk_off<br>Turn off smoothdiv module clk.<br>1'b1: Turn off.<br>1'b0: Turn on. |
| 12:5 | RO | 0x00 | reserved |
| 4:0 | RW | 0x00 | aclk_m0_gpu_step<br>step<br>Step of div from 0x1f to setting configuration . |

**CRU_SMOTH_DIVFREE_CON09**

Address: Operational Base + offset (0x0CC4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | aclk_m1_gpu_freq_keep<br>freq_keep<br>Cycles to keep every step. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x0 | aclk_m1_gpu_bypass<br>bypass<br>Division signal bypass.<br>1'b1: Bypass.<br>1'b0: Use Smoothdiv to control clock division. |
| 14 | RW | 0x0 | aclk_m1_gpu_gate_smth_en<br>gate_smth_en<br>If trigger smoothdiv function when clk been gated.<br>1'b1: Enable.<br>1'b0: Disable. |
| 13 | RW | 0x0 | aclk_m1_gpu_smdiv_clk_off<br>smdiv_clk_off<br>Turn off smoothdiv module clk.<br>1'b1: Turn off.<br>1'b0: Turn on. |
| 12:5 | RO | 0x00 | reserved |
| 4:0 | RW | 0x00 | aclk_m1_gpu_step<br>step<br>Step of div from 0x1f to setting configuration . |

**CRU_SMOTH_DIVFREE_CON10**

Address: Operational Base + offset (0x0CC8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | aclk_m2_gpu_freq_keep<br>freq_keep<br>Cycles to keep every step. |
| 15 | RW | 0x0 | aclk_m2_gpu_bypass<br>bypass<br>Division signal bypass.<br>1'b1: Bypass.<br>1'b0: Use Smoothdiv to control clock division. |
| 14 | RW | 0x0 | aclk_m2_gpu_gate_smth_en<br>gate_smth_en<br>If trigger smoothdiv function when clk been gated.<br>1'b1: Enable.<br>1'b0: Disable. |
| 13 | RW | 0x0 | aclk_m2_gpu_smdiv_clk_off<br>smdiv_clk_off<br>Turn off smoothdiv module clk.<br>1'b1: Turn off.<br>1'b0: Turn on. |
| 12:5 | RO | 0x00 | reserved |
| 4:0 | RW | 0x00 | aclk_m2_gpu_step<br>step<br>Step of div from 0x1f to setting configuration . |

**CRU_SMOTH_DIVFREE_CON11**

Address: Operational Base + offset (0x0CCC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | aclk_m3_gpu_freq_keep<br>freq_keep<br>Cycles to keep every step. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x0 | aclk_m3_gpu_bypass<br>bypass<br>Division signal bypass.<br>1'b1: Bypass.<br>1'b0: Use Smoothdiv to control clock division. |
| 14 | RW | 0x0 | aclk_m3_gpu_gate_smth_en<br>gate_smth_en<br>If trigger smoothdiv function when clk been gated.<br>1'b1: Enable.<br>1'b0: Disable. |
| 13 | RW | 0x0 | aclk_m3_gpu_smdiv_clk_off<br>smdiv_clk_off<br>Turn off smoothdiv module clk.<br>1'b1: Turn off.<br>1'b0: Turn on. |
| 12:5 | RO | 0x00 | reserved |
| 4:0 | RW | 0x00 | aclk_m3_gpu_step<br>step<br>Step of div from 0x1f to setting configuration . |

**CRU_SMOTH_DIVFREE_CON12**

Address: Operational Base + offset (0x0CD0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | clk_rknn_dsu0_src_freq_keep<br>freq_keep<br>Cycles to keep every step. |
| 15 | RW | 0x0 | clk_rknn_dsu0_src_bypass<br>bypass<br>Division signal bypass.<br>1'b1: Bypass.<br>1'b0: Use Smoothdiv to control clock division. |
| 14 | RW | 0x0 | clk_rknn_dsu0_src_gate_smth_en<br>gate_smth_en<br>If trigger smoothdiv function when clk been gated.<br>1'b1: Enable.<br>1'b0: Disable. |
| 13 | RW | 0x0 | clk_rknn_dsu0_src_smdiv_clk_off<br>smdiv_clk_off<br>Turn off smoothdiv module clk.<br>1'b1: Turn off.<br>1'b0: Turn on. |
| 12:5 | RO | 0x00 | reserved |
| 4:0 | RW | 0x00 | clk_rknn_dsu0_src_step<br>step<br>Step of div from 0x1f to setting configuration . |

**CRU_AUTOCS_ACLK_TOP_ROOT_CON0**

Address: Operational Base + offset (0x0D00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_top_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_top_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

Rockchip Confidencial

**CRU_AUTOCS_ACLK_TOP_ROOT_CON1**

Address: Operational Base + offset (0x0D04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_top_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_top_root_switch_en<br>switch_en<br>1'b1: Enable aclk_top_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_top_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_top_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_top_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_top_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_LOW_TOP_ROOT_CON0**

Address: Operational Base + offset (0x0D08)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_low_top_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_low_top_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_LOW_TOP_ROOT_CON1**

Address: Operational Base + offset (0x0D0C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_low_top_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | aclk_low_top_root_switch_en<br>switch_en<br>1'b1: Enable aclk_low_top_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_low_top_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_low_top_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_low_top_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_low_top_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_TOP_M400_ROOT_CON0**

Address: Operational Base + offset (0x0D10)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_top_m400_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_top_m400_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_TOP_M400_ROOT_CON1**

Address: Operational Base + offset (0x0D14)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_top_m400_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_top_m400_root_switch_en<br>switch_en<br>1'b1: Enable aclk_top_m400_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_top_m400_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_top_m400_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_top_m400_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_top_m400_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_TOP_S400_ROOT_CON0**

Address: Operational Base + offset (0x0D18)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_top_s400_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_top_s400_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_TOP_S400_ROOT_CON1**

Address: Operational Base + offset (0x0D1C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_top_s400_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_top_s400_root_switch_en<br>switch_en<br>1'b1: Enable aclk_top_s400_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_top_s400_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_top_s400_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_top_s400_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_top_s400_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_BUS_ROOT_CON0**

Address: Operational Base + offset (0x0D20)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_bus_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_bus_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_BUS_ROOT_CON1**

Address: Operational Base + offset (0x0D24)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:14 | RW | 0x0 | aclk_bus_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_bus_root_switch_en<br>switch_en<br>1'b1: Enable aclk_bus_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_bus_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_bus_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_bus_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_bus_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_ISP1_ROOT_CON0**

Address: Operational Base + offset (0x0D28)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_isp1_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_isp1_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_ISP1_ROOT_CON1**

Address: Operational Base + offset (0x0D2C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_isp1_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_isp1_root_switch_en<br>switch_en<br>1'b1: Enable aclk_isp1_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_isp1_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_isp1_root switch to lower frequency.<br>1'b0: Disable. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:0 | RW | 0x000 | aclk_isp1_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_isp1_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_CLK_RKNN_DSU0_CON0**

Address: Operational Base + offset (0x0D30)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | clk_rknn_dsu0_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | clk_rknn_dsu0_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_CLK_RKNN_DSU0_CON1**

Address: Operational Base + offset (0x0D34)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | clk_rknn_dsu0_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | clk_rknn_dsu0_switch_en<br>switch_en<br>1'b1: Enable clk_rknn_dsu0 switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | clk_rknn_dsu0_autocs_en<br>autocs_en<br>1'b1: Enable clk_rknn_dsu0 switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | clk_rknn_dsu0_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable clk_rknn_dsu0 switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_HCLK_RKNN_ROOT_CON0**

Address: Operational Base + offset (0x0D38)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_rknn_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_rknn_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_HCLK_RKNN_ROOT_CON1**

Rockchip Confidencial

Address: Operational Base + offset (0x0D3C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | hclk_rknn_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_rknn_root_switch_en<br>switch_en<br>1'b1: Enable hclk_rknn_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_rknn_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_rknn_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | hclk_rknn_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_rknn_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_NVM_ROOT_CON0**

Address: Operational Base + offset (0x0D40)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_nvm_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_nvm_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_NVM_ROOT_CON1**

Address: Operational Base + offset (0x0D44)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_nvm_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_nvm_root_switch_en<br>switch_en<br>1'b1: Enable aclk_nvm_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | aclk_nvm_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_nvm_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_nvm_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_nvm_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_PHP_ROOT_CON0**

Address: Operational Base + offset (0x0D48)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_php_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_php_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_PHP_ROOT_CON1**

Address: Operational Base + offset (0x0D4C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_php_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_php_root_switch_en<br>switch_en<br>1'b1: Enable aclk_php_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_php_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_php_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_php_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_php_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_RKVDEC0_ROOT_CON0**

Address: Operational Base + offset (0x0D50)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_rkvdec0_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0004 | aclk_rkvdec0_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_RKVDEC0_ROOT_CON1**

Address: Operational Base + offset (0x0D54)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_rkvdec0_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_rkvdec0_root_switch_en<br>switch_en<br>1'b1: Enable aclk_rkvdec0_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_rkvdec0_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_rkvdec0_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_rkvdec0_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_rkvdec0_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_RKVDEC_CCU_CON0**

Address: Operational Base + offset (0x0D58)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_rkvdec_ccu_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_rkvdec_ccu_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_RKVDEC_CCU_CON1**

Address: Operational Base + offset (0x0D5C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_rkvdec_ccu_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | aclk_rkvdec_ccu_switch_en<br>switch_en<br>1'b1: Enable aclk_rkvdec_ccu switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_rkvdec_ccu_autocs_en<br>autocs_en<br>1'b1: Enable aclk_rkvdec_ccu switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_rkvdec_ccu_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_rkvdec_ccu switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_RKVDEC1_ROOT_CON0**

Address: Operational Base + offset (0x0D60)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_rkvdec1_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_rkvdec1_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_RKVDEC1_ROOT_CON1**

Address: Operational Base + offset (0x0D64)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_rkvdec1_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_rkvdec1_root_switch_en<br>switch_en<br>1'b1: Enable aclk_rkvdec1_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_rkvdec1_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_rkvdec1_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_rkvdec1_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_rkvdec1_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_USB_ROOT_CON0**

Address: Operational Base + offset (0x0D68)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_usb_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_usb_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_USB_ROOT_CON1**

Address: Operational Base + offset (0x0D6C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_usb_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_usb_root_switch_en<br>switch_en<br>1'b1: Enable aclk_usb_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_usb_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_usb_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_usb_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_usb_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_VDPU_ROOT_CON0**

Address: Operational Base + offset (0x0D70)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_vdpu_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_vdpu_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_VDPU_ROOT_CON1**

Address: Operational Base + offset (0x0D74)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:14 | RW | 0x0 | aclk_vdpu_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_vdpu_root_switch_en<br>switch_en<br>1'b1: Enable aclk_vdpu_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_vdpu_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_vdpu_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_vdpu_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_vdpu_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_VDPU_LOW_ROOT_CON0**

Address: Operational Base + offset (0x0D78)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_vdpu_low_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_vdpu_low_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_VDPU_LOW_ROOT_CON1**

Address: Operational Base + offset (0x0D7C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_vdpu_low_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_vdpu_low_root_switch_en<br>switch_en<br>1'b1: Enable aclk_vdpu_low_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_vdpu_low_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_vdpu_low_root switch to lower frequency.<br>1'b0: Disable. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:0 | RW | 0x000 | aclk_vdpu_low_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_vdpu_low_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_JPEG_DECODER_ROOT_CON0**

Address: Operational Base + offset (0x0D80)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_jpeg_decoder_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_jpeg_decoder_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_JPEG_DECODER_ROOT_CON1**

Address: Operational Base + offset (0x0D84)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_jpeg_decoder_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_jpeg_decoder_root_switch_en<br>switch_en<br>1'b1: Enable aclk_jpeg_decoder_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_jpeg_decoder_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_jpeg_decoder_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_jpeg_decoder_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_jpeg_decoder_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_RKVENC0_ROOT_CON0**

Address: Operational Base + offset (0x0D88)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_rkvenc0_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_rkvenc0_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

Rockchip Confidencial

**CRU_AUTOCS_ACLK_RKVENC0_ROOT_CON1**

Address: Operational Base + offset (0x0D8C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_rkvenc0_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_rkvenc0_root_switch_en<br>switch_en<br>1'b1: Enable aclk_rkvenc0_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_rkvenc0_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_rkvenc0_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_rkvenc0_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_rkvenc0_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_RKVENC1_ROOT_CON0**

Address: Operational Base + offset (0x0D90)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_rkvenc1_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_rkvenc1_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_RKVENC1_ROOT_CON1**

Address: Operational Base + offset (0x0D94)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_rkvenc1_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_rkvenc1_root_switch_en<br>switch_en<br>1'b1: Enable aclk_rkvenc1_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | aclk_rkvenc1_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_rkvenc1_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_rkvenc1_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_rkvenc1_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_VI_ROOT_CON0**

Address: Operational Base + offset (0x0D98)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_vi_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_vi_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_VI_ROOT_CON1**

Address: Operational Base + offset (0x0D9C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_vi_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_vi_root_switch_en<br>switch_en<br>1'b1: Enable aclk_vi_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_vi_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_vi_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_vi_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_vi_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_VOP_ROOT_CON0**

Address: Operational Base + offset (0x0DA0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_vop_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0004 | aclk_vop_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_VOP_ROOT_CON1**

Address: Operational Base + offset (0x0DA4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_vop_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_vop_root_switch_en<br>switch_en<br>1'b1: Enable aclk_vop_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_vop_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_vop_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_vop_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_vop_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_VO0_ROOT_CON0**

Address: Operational Base + offset (0x0DA8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_vo0_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_vo0_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_VO0_ROOT_CON1**

Address: Operational Base + offset (0x0DAC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_vo0_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | aclk_vo0_root_switch_en<br>switch_en<br>1'b1: Enable aclk_vo0_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_vo0_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_vo0_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_vo0_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_vo0_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_HDCP1_ROOT_CON0**

Address: Operational Base + offset (0x0DB0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_hdcp1_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_hdcp1_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_HDCP1_ROOT_CON1**

Address: Operational Base + offset (0x0DB4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_hdcp1_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_hdcp1_root_switch_en<br>switch_en<br>1'b1: Enable aclk_hdcp1_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_hdcp1_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_hdcp1_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_hdcp1_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_hdcp1_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_HDMIRX_ROOT_CON0**

Address: Operational Base + offset (0x0DB8)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_hdmirx_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_hdmirx_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_HDMIRX_ROOT_CON1**

Address: Operational Base + offset (0x0DBC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_hdmirx_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_hdmirx_root_switch_en<br>switch_en<br>1'b1: Enable aclk_hdmirx_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_hdmirx_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_hdmirx_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_hdmirx_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_hdmirx_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_CLK_GPU_COREGROUP_CON0**

Address: Operational Base + offset (0x0DC0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | clk_gpu_coregroup_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | clk_gpu_coregroup_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_CLK_GPU_COREGROUP_CON1**

Address: Operational Base + offset (0x0DC4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:14 | RW | 0x0 | clk_gpu_coregroup_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | clk_gpu_coregroup_switch_en<br>switch_en<br>1'b1: Enable clk_gpu_coregroup switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | clk_gpu_coregroup_autocs_en<br>autocs_en<br>1'b1: Enable clk_gpu_coregroup switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | clk_gpu_coregroup_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable clk_gpu_coregroup switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_AV1_ROOT_CON0**

Address: Operational Base + offset (0x0DE0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_av1_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_av1_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_AV1_ROOT_CON1**

Address: Operational Base + offset (0x0DE4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_av1_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_av1_root_switch_en<br>switch_en<br>1'b1: Enable aclk_av1_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_av1_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_av1_root switch to lower frequency.<br>1'b0: Disable. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:0 | RW | 0x000 | aclk_av1_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_av1_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_CENTER_ROOT_CON0**

Address: Operational Base + offset (0x0DE8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_center_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_center_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_CENTER_ROOT_CON1**

Address: Operational Base + offset (0x0DEC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_center_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_center_root_switch_en<br>switch_en<br>1'b1: Enable aclk_center_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_center_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_center_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_center_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_center_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_CENTER_LOW_ROOT_CON0**

Address: Operational Base + offset (0x0DF0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_center_low_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_center_low_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_CENTER_LOW_ROOT_CON1**

Rockchip Confidencial

Address: Operational Base + offset (0x0DF4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_center_low_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_center_low_root_switch_en<br>switch_en<br>1'b1: Enable aclk_center_low_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_center_low_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_center_low_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_center_low_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_center_low_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_CENTER_S400_ROOT_CON0**

Address: Operational Base + offset (0x0DF8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_center_s400_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_center_s400_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_CENTER_S400_ROOT_CON1**

Address: Operational Base + offset (0x0DFC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_center_s400_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_center_s400_root_switch_en<br>switch_en<br>1'b1: Enable aclk_center_s400_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | aclk_center_s400_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_center_s400_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_center_s400_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_center_s400_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_VO1USB_TOP_ROOT_CON0**

Address: Operational Base + offset (0x0E00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_vo1usb_top_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_vo1usb_top_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_VO1USB_TOP_ROOT_CON1**

Address: Operational Base + offset (0x0E04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_vo1usb_top_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_vo1usb_top_root_switch_en<br>switch_en<br>1'b1: Enable aclk_vo1usb_top_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_vo1usb_top_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_vo1usb_top_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_vo1usb_top_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_vo1usb_top_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_RGA3_ROOT_CON0**

Address: Operational Base + offset (0x0E08)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_rga3_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0004 | aclk_rga3_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_RGA3_ROOT_CON1**

Address: Operational Base + offset (0x0E0C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_rga3_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_rga3_root_switch_en<br>switch_en<br>1'b1: Enable aclk_rga3_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_rga3_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_rga3_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_rga3_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_rga3_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_PCLK_AV1_ROOT_CON0**

Address: Operational Base + offset (0x0E10)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | pclk_av1_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | pclk_av1_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_PCLK_AV1_ROOT_CON1**

Address: Operational Base + offset (0x0E14)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | pclk_av1_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | pclk_av1_root_switch_en<br>switch_en<br>1'b1: Enable pclk_av1_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | pclk_av1_root_autocs_en<br>autocs_en<br>1'b1: Enable pclk_av1_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | pclk_av1_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable pclk_av1_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_HCLK_ISP1_ROOT_CON0**

Address: Operational Base + offset (0x0E18)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_isp1_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_isp1_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_HCLK_ISP1_ROOT_CON1**

Address: Operational Base + offset (0x0E1C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | hclk_isp1_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_isp1_root_switch_en<br>switch_en<br>1'b1: Enable hclk_isp1_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_isp1_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_isp1_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | hclk_isp1_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_isp1_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_PCLK_NPUTOP_ROOT_CON0**

Address: Operational Base + offset (0x0E20)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | pclk_nputop_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | pclk_nputop_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_PCLK_NPUTOP_ROOT_CON1**

Address: Operational Base + offset (0x0E24)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | pclk_nputop_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | pclk_nputop_root_switch_en<br>switch_en<br>1'b1: Enable pclk_nputop_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | pclk_nputop_root_autocs_en<br>autocs_en<br>1'b1: Enable pclk_nputop_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | pclk_nputop_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable pclk_nputop_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_HCLK_NPU_CM0_ROOT_CON0**

Address: Operational Base + offset (0x0E28)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_npu_cm0_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_npu_cm0_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_HCLK_NPU_CM0_ROOT_CON1**

Address: Operational Base + offset (0x0E2C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:14 | RW | 0x0 | hclk_npu_cm0_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_npu_cm0_root_switch_en<br>switch_en<br>1'b1: Enable hclk_npu_cm0_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_npu_cm0_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_npu_cm0_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | hclk_npu_cm0_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_npu_cm0_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_HCLK_NVM_ROOT_CON0**

Address: Operational Base + offset (0x0E30)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_nvm_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_nvm_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_HCLK_NVM_ROOT_CON1**

Address: Operational Base + offset (0x0E34)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | hclk_nvm_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_nvm_root_switch_en<br>switch_en<br>1'b1: Enable hclk_nvm_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_nvm_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_nvm_root switch to lower frequency.<br>1'b0: Disable. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:0 | RW | 0x000 | hclk_nvm_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_nvm_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_PCLK_PHP_ROOT_CON0**

Address: Operational Base + offset (0x0E38)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | pclk_php_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | pclk_php_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_PCLK_PHP_ROOT_CON1**

Address: Operational Base + offset (0x0E3C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | pclk_php_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | pclk_php_root_switch_en<br>switch_en<br>1'b1: Enable pclk_php_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | pclk_php_root_autocs_en<br>autocs_en<br>1'b1: Enable pclk_php_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | pclk_php_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable pclk_php_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_PCIE_ROOT_CON0**

Address: Operational Base + offset (0x0E40)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_pcie_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_pcie_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_PCIE_ROOT_CON1**

Rockchip Confidencial

Address: Operational Base + offset (0x0E44)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_pcie_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_pcie_root_switch_en<br>switch_en<br>1'b1: Enable aclk_pcie_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_pcie_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_pcie_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_pcie_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_pcie_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_HCLK_RKVDEC0_ROOT_CON0**

Address: Operational Base + offset (0x0E48)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_rkvdec0_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_rkvdec0_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_HCLK_RKVDEC0_ROOT_CON1**

Address: Operational Base + offset (0x0E4C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | hclk_rkvdec0_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_rkvdec0_root_switch_en<br>switch_en<br>1'b1: Enable hclk_rkvdec0_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | hclk_rkvdec0_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_rkvdec0_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | hclk_rkvdec0_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_rkvdec0_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_HCLK_RKVDEC1_ROOT_CON0**

Address: Operational Base + offset (0x0E50)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_rkvdec1_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_rkvdec1_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_HCLK_RKVDEC1_ROOT_CON1**

Address: Operational Base + offset (0x0E54)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | hclk_rkvdec1_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_rkvdec1_root_switch_en<br>switch_en<br>1'b1: Enable hclk_rkvdec1_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_rkvdec1_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_rkvdec1_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | hclk_rkvdec1_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_rkvdec1_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_PCLK_TOP_ROOT_CON0**

Address: Operational Base + offset (0x0E58)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | pclk_top_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0004 | pclk_top_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_PCLK_TOP_ROOT_CON1**

Address: Operational Base + offset (0x0E5C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | pclk_top_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | pclk_top_root_switch_en<br>switch_en<br>1'b1: Enable pclk_top_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | pclk_top_root_autocs_en<br>autocs_en<br>1'b1: Enable pclk_top_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | pclk_top_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable pclk_top_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_TOP_M500_ROOT_CON0**

Address: Operational Base + offset (0x0E60)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_top_m500_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_top_m500_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_TOP_M500_ROOT_CON1**

Address: Operational Base + offset (0x0E64)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_top_m500_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | aclk_top_m500_root_switch_en<br>switch_en<br>1'b1: Enable aclk_top_m500_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_top_m500_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_top_m500_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_top_m500_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_top_m500_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_TOP_S200_ROOT_CON0**

Address: Operational Base + offset (0x0E68)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_top_s200_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_top_s200_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_TOP_S200_ROOT_CON1**

Address: Operational Base + offset (0x0E6C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_top_s200_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_top_s200_root_switch_en<br>switch_en<br>1'b1: Enable aclk_top_s200_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_top_s200_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_top_s200_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_top_s200_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_top_s200_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_HCLK_USB_ROOT_CON0**

Address: Operational Base + offset (0x0E70)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_usb_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_usb_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_HCLK_USB_ROOT_CON1**

Address: Operational Base + offset (0x0E74)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | hclk_usb_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_usb_root_switch_en<br>switch_en<br>1'b1: Enable hclk_usb_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_usb_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_usb_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | hclk_usb_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_usb_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_HCLK_VDPU_ROOT_CON0**

Address: Operational Base + offset (0x0E78)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_vdpu_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_vdpu_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_HCLK_VDPU_ROOT_CON1**

Address: Operational Base + offset (0x0E7C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:14 | RW | 0x0 | hclk_vdpu_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_vdpu_root_switch_en<br>switch_en<br>1'b1: Enable hclk_vdpu_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_vdpu_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_vdpu_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | hclk_vdpu_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_vdpu_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_HCLK_RKVENC0_ROOT_CON0**

Address: Operational Base + offset (0x0E80)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_rkvenc0_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_rkvenc0_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_HCLK_RKVENC0_ROOT_CON1**

Address: Operational Base + offset (0x0E84)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | hclk_rkvenc0_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_rkvenc0_root_switch_en<br>switch_en<br>1'b1: Enable hclk_rkvenc0_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_rkvenc0_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_rkvenc0_root switch to lower frequency.<br>1'b0: Disable. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:0 | RW | 0x000 | hclk_rkvenc0_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_rkvenc0_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_HCLK_RKVENC1_ROOT_CON0**

Address: Operational Base + offset (0x0E88)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_rkvenc1_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_rkvenc1_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_HCLK_RKVENC1_ROOT_CON1**

Address: Operational Base + offset (0x0E8C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | hclk_rkvenc1_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_rkvenc1_root_switch_en<br>switch_en<br>1'b1: Enable hclk_rkvenc1_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_rkvenc1_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_rkvenc1_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | hclk_rkvenc1_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_rkvenc1_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_HCLK_VI_ROOT_CON0**

Address: Operational Base + offset (0x0E90)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_vi_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_vi_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_HCLK_VI_ROOT_CON1**

Rockchip Confidencial

Address: Operational Base + offset (0x0E94)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | hclk_vi_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_vi_root_switch_en<br>switch_en<br>1'b1: Enable hclk_vi_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_vi_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_vi_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | hclk_vi_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_vi_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_PCLK_VI_ROOT_CON0**

Address: Operational Base + offset (0x0E98)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | pclk_vi_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | pclk_vi_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_PCLK_VI_ROOT_CON1**

Address: Operational Base + offset (0x0E9C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | pclk_vi_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | pclk_vi_root_switch_en<br>switch_en<br>1'b1: Enable pclk_vi_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | pclk_vi_root_autocs_en<br>autocs_en<br>1'b1: Enable pclk_vi_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | pclk_vi_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable pclk_vi_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_VOP_LOW_ROOT_CON0**

Address: Operational Base + offset (0x0EA0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_vop_low_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_vop_low_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_VOP_LOW_ROOT_CON1**

Address: Operational Base + offset (0x0EA4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_vop_low_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_vop_low_root_switch_en<br>switch_en<br>1'b1: Enable aclk_vop_low_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_vop_low_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_vop_low_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_vop_low_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_vop_low_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_HCLK_VOP_ROOT_CON0**

Address: Operational Base + offset (0x0EA8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_vop_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0004 | hclk_vop_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_HCLK_VOP_ROOT_CON1**

Address: Operational Base + offset (0x0EAC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | hclk_vop_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_vop_root_switch_en<br>switch_en<br>1'b1: Enable hclk_vop_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_vop_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_vop_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | hclk_vop_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_vop_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_PCLK_VOP_ROOT_CON0**

Address: Operational Base + offset (0x0EB0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | pclk_vop_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | pclk_vop_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_PCLK_VOP_ROOT_CON1**

Address: Operational Base + offset (0x0EB4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | pclk_vop_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | pclk_vop_root_switch_en<br>switch_en<br>1'b1: Enable pclk_vop_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | pclk_vop_root_autocs_en<br>autocs_en<br>1'b1: Enable pclk_vop_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | pclk_vop_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable pclk_vop_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_HCLK_VO0_ROOT_CON0**

Address: Operational Base + offset (0x0EB8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_vo0_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_vo0_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_HCLK_VO0_ROOT_CON1**

Address: Operational Base + offset (0x0EBC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | hclk_vo0_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_vo0_root_switch_en<br>switch_en<br>1'b1: Enable hclk_vo0_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_vo0_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_vo0_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | hclk_vo0_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_vo0_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_HCLK_VO0_S_ROOT_CON0**

Address: Operational Base + offset (0x0EC0)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_vo0_s_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_vo0_s_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_HCLK_VO0_S_ROOT_CON1**

Address: Operational Base + offset (0x0EC4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | hclk_vo0_s_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_vo0_s_root_switch_en<br>switch_en<br>1'b1: Enable hclk_vo0_s_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_vo0_s_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_vo0_s_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | hclk_vo0_s_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_vo0_s_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_PCLK_VO0_ROOT_CON0**

Address: Operational Base + offset (0x0EC8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | pclk_vo0_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | pclk_vo0_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_PCLK_VO0_ROOT_CON1**

Address: Operational Base + offset (0x0ECC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:14 | RW | 0x0 | pclk_vo0_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | pclk_vo0_root_switch_en<br>switch_en<br>1'b1: Enable pclk_vo0_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | pclk_vo0_root_autocs_en<br>autocs_en<br>1'b1: Enable pclk_vo0_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | pclk_vo0_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable pclk_vo0_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_PCLK_VO0_S_ROOT_CON0**

Address: Operational Base + offset (0x0ED0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | pclk_vo0_s_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | pclk_vo0_s_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_PCLK_VO0_S_ROOT_CON1**

Address: Operational Base + offset (0x0ED4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | pclk_vo0_s_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | pclk_vo0_s_root_switch_en<br>switch_en<br>1'b1: Enable pclk_vo0_s_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | pclk_vo0_s_root_autocs_en<br>autocs_en<br>1'b1: Enable pclk_vo0_s_root switch to lower frequency.<br>1'b0: Disable. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:0 | RW | 0x000 | pclk_vo0_s_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable pclk_vo0_s_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_HCLK_VO1_ROOT_CON0**

Address: Operational Base + offset (0x0ED8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_vo1_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_vo1_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_HCLK_VO1_ROOT_CON1**

Address: Operational Base + offset (0x0EDC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | hclk_vo1_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_vo1_root_switch_en<br>switch_en<br>1'b1: Enable hclk_vo1_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_vo1_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_vo1_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | hclk_vo1_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_vo1_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_HCLK_VO1_S_ROOT_CON0**

Address: Operational Base + offset (0x0EE0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_vo1_s_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_vo1_s_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_HCLK_VO1_S_ROOT_CON1**

Rockchip Confidencial

Address: Operational Base + offset (0x0EE4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | hclk_vo1_s_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_vo1_s_root_switch_en<br>switch_en<br>1'b1: Enable hclk_vo1_s_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_vo1_s_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_vo1_s_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | hclk_vo1_s_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_vo1_s_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_PCLK_VO1_ROOT_CON0**

Address: Operational Base + offset (0x0EE8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | pclk_vo1_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | pclk_vo1_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_PCLK_VO1_ROOT_CON1**

Address: Operational Base + offset (0x0EEC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | pclk_vo1_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | pclk_vo1_root_switch_en<br>switch_en<br>1'b1: Enable pclk_vo1_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | pclk_vo1_root_autocs_en<br>autocs_en<br>1'b1: Enable pclk_vo1_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | pclk_vo1_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable pclk_vo1_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_PCLK_VO1_S_ROOT_CON0**

Address: Operational Base + offset (0x0EF0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | pclk_vo1_s_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | pclk_vo1_s_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_PCLK_VO1_S_ROOT_CON1**

Address: Operational Base + offset (0x0EF4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | pclk_vo1_s_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | pclk_vo1_s_root_switch_en<br>switch_en<br>1'b1: Enable pclk_vo1_s_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | pclk_vo1_s_root_autocs_en<br>autocs_en<br>1'b1: Enable pclk_vo1_s_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | pclk_vo1_s_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable pclk_vo1_s_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_PCLK_GPU_ROOT_CON0**

Address: Operational Base + offset (0x0EF8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | pclk_gpu_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0004 | pclk_gpu_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_PCLK_GPU_ROOT_CON1**

Address: Operational Base + offset (0x0EFC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | pclk_gpu_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | pclk_gpu_root_switch_en<br>switch_en<br>1'b1: Enable pclk_gpu_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | pclk_gpu_root_autocs_en<br>autocs_en<br>1'b1: Enable pclk_gpu_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | pclk_gpu_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable pclk_gpu_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_HCLK_CENTER_ROOT_CON0**

Address: Operational Base + offset (0x0F00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_center_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_center_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_HCLK_CENTER_ROOT_CON1**

Address: Operational Base + offset (0x0F04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | hclk_center_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | hclk_center_root_switch_en<br>switch_en<br>1'b1: Enable hclk_center_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_center_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_center_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | hclk_center_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_center_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_PCLK_CENTER_ROOT_CON0**

Address: Operational Base + offset (0x0F08)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | pclk_center_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | pclk_center_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_PCLK_CENTER_ROOT_CON1**

Address: Operational Base + offset (0x0F0C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | pclk_center_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | pclk_center_root_switch_en<br>switch_en<br>1'b1: Enable pclk_center_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | pclk_center_root_autocs_en<br>autocs_en<br>1'b1: Enable pclk_center_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | pclk_center_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable pclk_center_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_CENTER_S200_ROOT_CON0**

Address: Operational Base + offset (0x0F10)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_center_s200_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_center_s200_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_CENTER_S200_ROOT_CON1**

Address: Operational Base + offset (0x0F14)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_center_s200_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_center_s200_root_switch_en<br>switch_en<br>1'b1: Enable aclk_center_s200_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_center_s200_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_center_s200_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_center_s200_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_center_s200_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_HCLK_SDIO_ROOT_CON0**

Address: Operational Base + offset (0x0F18)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_sdio_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_sdio_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_HCLK_SDIO_ROOT_CON1**

Address: Operational Base + offset (0x0F1C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:14 | RW | 0x0 | hclk_sdio_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_sdio_root_switch_en<br>switch_en<br>1'b1: Enable hclk_sdio_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_sdio_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_sdio_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | hclk_sdio_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_sdio_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_HCLK_RGA3_ROOT_CON0**

Address: Operational Base + offset (0x0F20)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_rga3_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_rga3_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_HCLK_RGA3_ROOT_CON1**

Address: Operational Base + offset (0x0F24)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | hclk_rga3_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_rga3_root_switch_en<br>switch_en<br>1'b1: Enable hclk_rga3_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_rga3_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_rga3_root switch to lower frequency.<br>1'b0: Disable. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:0 | RW | 0x000 | hclk_rga3_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_rga3_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_HCLK_VO1USB_TOP_ROOT_CON0**

Address: Operational Base + offset (0x0F28)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_vo1usb_top_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_vo1usb_top_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_HCLK_VO1USB_TOP_ROOT_CON1**

Address: Operational Base + offset (0x0F2C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | hclk_vo1usb_top_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_vo1usb_top_root_switch_en<br>switch_en<br>1'b1: Enable hclk_vo1usb_top_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_vo1usb_top_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_vo1usb_top_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | hclk_vo1usb_top_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_vo1usb_top_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_ACLK_TOP_M300_ROOT_CON0**

Address: Operational Base + offset (0x0F30)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_top_m300_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_top_m300_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_ACLK_TOP_M300_ROOT_CON1**

Rockchip Confidencial

Address: Operational Base + offset (0x0F34)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_top_m300_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_top_m300_root_switch_en<br>switch_en<br>1'b1: Enable aclk_top_m300_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_top_m300_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_top_m300_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_top_m300_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_top_m300_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_CLK_RKNN_DSU0_SRC_T_CON0**

Address: Operational Base + offset (0x0F38)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | clk_rknn_dsu0_src_t_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | clk_rknn_dsu0_src_t_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_CLK_RKNN_DSU0_SRC_T_CON1**

Address: Operational Base + offset (0x0F3C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | clk_rknn_dsu0_src_t_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | clk_rknn_dsu0_src_t_switch_en<br>switch_en<br>1'b1: Enable clk_rknn_dsu0_src_t switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | clk_rknn_dsu0_src_t_autocs_en<br>autocs_en<br>1'b1: Enable clk_rknn_dsu0_src_t switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | clk_rknn_dsu0_src_t_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable clk_rknn_dsu0_src_t switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_HCLK_AUDIO_ROOT_CON0**

Address: Operational Base + offset (0x0F40)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_audio_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_audio_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_HCLK_AUDIO_ROOT_CON1**

Address: Operational Base + offset (0x0F44)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | hclk_audio_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_audio_root_switch_en<br>switch_en<br>1'b1: Enable hclk_audio_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_audio_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_audio_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | hclk_audio_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_audio_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**CRU_AUTOCS_PCLK_AUDIO_ROOT_CON0**

Address: Operational Base + offset (0x0F48)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | pclk_audio_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0004 | pclk_audio_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**CRU_AUTOCS_PCLK_AUDIO_ROOT_CON1**

Address: Operational Base + offset (0x0F4C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | pclk_audio_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | pclk_audio_root_switch_en<br>switch_en<br>1'b1: Enable pclk_audio_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | pclk_audio_root_autocs_en<br>autocs_en<br>1'b1: Enable pclk_audio_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | pclk_audio_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable pclk_audio_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

# 2.5 DDR0CRU Register Description

## 2.5.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| DDR0CRU_D0APLL_CON0 | 0x0000 | W | 0x00008000 | D0APLL configuration register 0 |
| DDR0CRU_D0APLL_CON1 | 0x0004 | W | 0x00000000 | D0APLL configuration register 1 |
| DDR0CRU_D0APLL_CON2 | 0x0008 | W | 0x00000000 | D0APLL configuration register 2 |
| DDR0CRU_D0APLL_CON3 | 0x000C | W | 0x00000000 | D0APLL configuration register 3 |
| DDR0CRU_D0APLL_CON4 | 0x0010 | W | 0x00000000 | D0APLL configuration register 4 |
| DDR0CRU_D0APLL_CON5 | 0x0014 | W | 0x00000000 | D0APLL configuration register 5 |
| DDR0CRU_D0APLL_CON6 | 0x0018 | W | 0x00000000 | D0APLL configuration register 6 |
| DDR0CRU_D0BPLL_CON0 | 0x0020 | W | 0x00008000 | D0BPLL configuration register 0 |
| DDR0CRU_D0BPLL_CON1 | 0x0024 | W | 0x00000000 | D0BPLL configuration register 1 |
| DDR0CRU_D0BPLL_CON2 | 0x0028 | W | 0x00000000 | D0BPLL configuration register 2 |
| DDR0CRU_D0BPLL_CON3 | 0x002C | W | 0x00000000 | D0BPLL configuration register 3 |
| DDR0CRU_D0BPLL_CON4 | 0x0030 | W | 0x00000000 | D0BPLL configuration register 4 |
| DDR0CRU_D0BPLL_CON5 | 0x0034 | W | 0x00000000 | D0BPLL configuration register 5 |
| DDR0CRU_D0BPLL_CON6 | 0x0038 | W | 0x00000000 | D0BPLL configuration register 6 |

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| DDR0CRU_CLKSEL_CON00 | 0x0300 | W | 0x00000000 | Internal clock select and division register 0 |
| DDR0CRU_GATE_CON00 | 0x0800 | W | 0x00000000 | Internal clock gate and division register 0 |
| DDR0CRU_SOFTRST_CON00 | 0x0A00 | W | 0x00000006 | Internal clock reset register 0 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 2.5.2 Detail Registers Description

**DDR0CRU_D0APLL_CON0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | d0apll_bp<br>BYPASS: Bypass mode control signal.<br>1'b1: bypass mode is enabled. (FOUT = FIN).<br>1'b0: PLL operates normally. |
| 14:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | d0apll_m<br>M: Division value of the 10-bit programmable main-divider.<br>PLL has to be reset if M value is changed.<br>64 <= pll_m <= 1023 |

**DDR0CRU_D0APLL_CON1**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | d0apll_resetb<br>RESETB: Power down control signal.<br>1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time.<br>1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset. |
| 12:9 | RO | 0x0 | reserved |
| 8:6 | RW | 0x0 | d0apll_s<br>Division value of the 3-bit programmable scaler.<br>0 <= pll_s <= 6 |
| 5:0 | RW | 0x00 | d0apll_p<br>P: Division value of the 6-bit programmable pre-divider.<br>PLL has to be reset if P value is changed.<br>1 <= pll_p <= 63 |

**DDR0CRU_D0APLL_CON2**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0000 | d0apll_k<br>K: Value of 16-bit DSM.<br>pll_k[15:0] is a two's complement integer. |

**DDR0CRU_D0APLL_CON3**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | d0apll_sel_pf<br>SEL_PF: Value of 2-bit modulation method control.<br>2'b00: down spread;<br>2'b01: up spread;<br>2'b1x: center spread.<br>PLL has to be reset if pll_sel_pf is changed. |
| 13:8 | RW | 0x00 | d0apll_mrr<br>MRR: Value of 6-bit modulation rate control.<br>PLL has to be reset if pll_mrr is changed. |
| 7:0 | RW | 0x00 | d0apll_mfr<br>MFR: Value of 8-bit modulation frequency control.<br>PLL has to be reset if pll_mfr is changed. |

**DDR0CRU_D0APLL_CON4**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | d0apll_fsel<br>FSEL: Monitoring pin.<br>1'b0: FEED_OUT = FREF.<br>1'b1: FEED_OUT = FEED. |
| 14 | RW | 0x0 | d0apll_feed_en<br>FEED_EN: Monitoring pin.<br>1'b0: FEED_OUT is disabled.<br>1'b1: FEED_OUT is enabled. |
| 13:9 | RO | 0x00 | reserved |
| 8:4 | RW | 0x00 | d0apll_extafc<br>EXTAFC: Monitoring pin.<br>If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 3 | RW | 0x0 | d0apll_afc_enb<br>AFC_ENB: Monitoring pin.<br>1'b0: AFC is enabled and VCO is calibrated automatically.<br>1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | d0apll_sscg_en<br>SSCG_EN: Enable pin for dithered mode.<br>1'b0: disable dithered mode.<br>1'b1: enable dithered mode. |

Rockchip Confidential

**DDR0CRU_D0APLL_CON5**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | d0apll_fout_mask<br>FOUT_MASK: Scaler's re-initialization time control pin. |

**DDR0CRU_D0APLL_CON6**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | d0apll_lock<br>LOCK: PLL lock flag.<br>1'b0: PLL is unlocked.<br>1'b1: PLL is locked. |
| 14:10 | RW | 0x00 | d0apll_afc_code<br>AFC_CODE: Monitoring pin.<br>Output code of AFC(5 bits). |
| 9:0 | RO | 0x000 | reserved |

**DDR0CRU_D0BPLL_CON0**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | d0bpll_bp<br>BYPASS: Bypass mode control signal.<br>1'b1: bypass mode is enabled. (FOUT = FIN).<br>1'b0: PLL operates normally. |
| 14:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | d0bpll_m<br>M: Division value of the 10-bit programmable main-divider.<br>PLL has to be reset if M value is changed.<br>64 <= pll_m <= 1023 |

**DDR0CRU_D0BPLL_CON1**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | d0bpll_resetb<br>RESETB: Power down control signal.<br>1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time.<br>1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset. |
| 12:9 | RO | 0x0 | reserved |
| 8:6 | RW | 0x0 | d0bpll_s<br>Division value of the 3-bit programmable scaler.<br>0 <= pll_s <= 6 |
| 5:0 | RW | 0x00 | d0bpll_p<br>P: Division value of the 6-bit programmable pre-divider.<br>PLL has to be reset if P value is changed.<br>1 <= pll_p <= 63 |

**DDR0CRU_D0BPLL_CON2**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | d0bpll_k<br>K: Value of 16-bit DSM.<br>pll_k[15:0] is a two's complement integer. |

**DDR0CRU_D0BPLL_CON3**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | d0bpll_sel_pf<br>SEL_PF: Value of 2-bit modulation method control.<br>2'b00: down spread;<br>2'b01: up spread;<br>2'b1x: center spread.<br>PLL has to be reset if pll_sel_pf is changed. |
| 13:8 | RW | 0x00 | d0bpll_mrr<br>MRR: Value of 6-bit modulation rate control.<br>PLL has to be reset if pll_mrr is changed. |
| 7:0 | RW | 0x00 | d0bpll_mfr<br>MFR: Value of 8-bit modulation frequency control.<br>PLL has to be reset if pll_mfr is changed. |

**DDR0CRU_D0BPLL_CON4**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | d0bpll_fsel<br>FSEL: Monitoring pin.<br>1'b0: FEED_OUT = FREF.<br>1'b1: FEED_OUT = FEED. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14 | RW | 0x0 | d0bpll_feed_en<br>FEED_EN: Monitoring pin.<br>1'b0: FEED_OUT is disabled.<br>1'b1: FEED_OUT is enabled. |
| 13:9 | RO | 0x00 | reserved |
| 8:4 | RW | 0x00 | d0bpll_extafc<br>EXTAFC: Monitoring pin.<br>If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 3 | RW | 0x0 | d0bpll_afc_enb<br>AFC_ENB: Monitoring pin.<br>1'b0: AFC is enabled and VCO is calibrated automatically.<br>1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | d0bpll_sscg_en<br>SSCG_EN: Enable pin for dithered mode.<br>1'b0: disable dithered mode.<br>1'b1: enable dithered mode. |

**DDR0CRU_D0BPLL_CON5**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | d0bpll_fout_mask<br>FOUT_MASK: Scaler's re-initialization time control pin. |

**DDR0CRU_D0BPLL_CON6**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | d0bpll_lock<br>LOCK: PLL lock flag.<br>1'b0: PLL is unlocked.<br>1'b1: PLL is locked. |
| 14:10 | RW | 0x00 | d0bpll_afc_code<br>AFC_CODE: Monitoring pin.<br>Output code of AFC(5 bits). |
| 9:0 | RO | 0x000 | reserved |

**DDR0CRU_CLKSEL_CON00**

Address: Operational Base + offset (0x0300)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | clk_ddrphy2x_ch0_sel<br>clk_ddrphy2x_ch0 clock mux.<br>1'b0: clk_d0apll_t<br>1'b1: clk_d0bpll |

**DDR0CRU_GATE_CON00**

Address: Operational Base + offset (0x0800)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x0 | clk_osc_ddrphy_ch0_en<br>clk_osc_ddrphy_ch0 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_ddrphy_ch0_en<br>pclk_ddrphy_ch0 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_ddr_cru_ch0_en<br>pclk_ddr_cru_ch0 clock gating control.<br>When high, disable clock |
| 2:0 | RO | 0x0 | reserved |

**DDR0CRU_SOFTRST_CON00**

Address: Operational Base + offset (0x0A00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:5 | RO | 0x000 | reserved |
| 4 | RW | 0x0 | presetn_ddrphy_ch0<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_ddr_cru_ch0<br>When high, reset relative logic |
| 2 | RW | 0x1 | resetn_ddrphy2x_ch0<br>When high, reset relative logic |
| 1 | RW | 0x1 | resetn_ddrphy2xdiv_ch0<br>div_rst_n at ddr ch0<br>When high, reset relative logic |
| 0 | RO | 0x0 | reserved |

# 2.6 DDR1CRU Register Description

## 2.6.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| DDR1CRU_D1APLL_CON0 | 0x0000 | W | 0x00008000 | D1APLL configuration register 0 |
| DDR1CRU_D1APLL_CON1 | 0x0004 | W | 0x00000000 | D1APLL configuration register 1 |
| DDR1CRU_D1APLL_CON2 | 0x0008 | W | 0x00000000 | D1APLL configuration register 2 |
| DDR1CRU_D1APLL_CON3 | 0x000C | W | 0x00000000 | D1APLL configuration register 3 |

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| DDR1CRU_D1APLL_CON4 | 0x0010 | W | 0x00000000 | D1APLL configuration register 4 |
| DDR1CRU_D1APLL_CON5 | 0x0014 | W | 0x00000000 | D1APLL configuration register 5 |
| DDR1CRU_D1APLL_CON6 | 0x0018 | W | 0x00000000 | D1APLL configuration register 6 |
| DDR1CRU_D1BPLL_CON0 | 0x0020 | W | 0x00008000 | D1BPLL configuration register 0 |
| DDR1CRU_D1BPLL_CON1 | 0x0024 | W | 0x00000000 | D1BPLL configuration register 1 |
| DDR1CRU_D1BPLL_CON2 | 0x0028 | W | 0x00000000 | D1BPLL configuration register 2 |
| DDR1CRU_D1BPLL_CON3 | 0x002C | W | 0x00000000 | D1BPLL configuration register 3 |
| DDR1CRU_D1BPLL_CON4 | 0x0030 | W | 0x00000000 | D1BPLL configuration register 4 |
| DDR1CRU_D1BPLL_CON5 | 0x0034 | W | 0x00000000 | D1BPLL configuration register 5 |
| DDR1CRU_D1BPLL_CON6 | 0x0038 | W | 0x00000000 | D1BPLL configuration register 6 |
| DDR1CRU_CLKSEL_CON00 | 0x0300 | W | 0x00000000 | Internal clock select and division register 0 |
| DDR1CRU_GATE_CON00 | 0x0800 | W | 0x00000000 | Internal clock gate and division register 0 |
| DDR1CRU_SOFTRST_CON00 | 0x0A00 | W | 0x00000006 | Internal clock reset register 0 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 2.6.2 Detail Registers Description

**DDR1CRU_D1APLL_CON0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | d1apll_bp<br>BYPASS: Bypass mode control signal.<br>1'b1: bypass mode is enabled. (FOUT = FIN).<br>1'b0: PLL operates normally. |
| 14:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | d1apll_m<br>M: Division value of the 10-bit programmable main-divider.<br>PLL has to be reset if M value is changed.<br>64 <= pll_m <= 1023 |

**DDR1CRU_D1APLL_CON1**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | d1apll_resetb<br>RESETB: Power down control signal.<br>1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time.<br>1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset. |
| 12:9 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8:6 | RW | 0x0 | d1apll_s<br>Division value of the 3-bit programmable scaler.<br>0 <= pll_s <= 6 |
| 5:0 | RW | 0x00 | d1apll_p<br>P: Division value of the 6-bit programmable pre-divider.<br>PLL has to be reset if P value is changed.<br>1 <= pll_p <= 63 |

**DDR1CRU_D1APLL_CON2**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | d1apll_k<br>K: Value of 16-bit DSM.<br>pll_k[15:0] is a two's complement integer. |

**DDR1CRU_D1APLL_CON3**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | d1apll_sel_pf<br>SEL_PF: Value of 2-bit modulation method control.<br>2'b00: down spread;<br>2'b01: up spread;<br>2'b1x: center spread.<br>PLL has to be reset if pll_sel_pf is changed. |
| 13:8 | RW | 0x00 | d1apll_mrr<br>MRR: Value of 6-bit modulation rate control.<br>PLL has to be reset if pll_mrr is changed. |
| 7:0 | RW | 0x00 | d1apll_mfr<br>MFR: Value of 8-bit modulation frequency control.<br>PLL has to be reset if pll_mfr is changed. |

**DDR1CRU_D1APLL_CON4**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | d1apll_fsel<br>FSEL: Monitoring pin.<br>1'b0: FEED_OUT = FREF.<br>1'b1: FEED_OUT = FEED. |
| 14 | RW | 0x0 | d1apll_feed_en<br>FEED_EN: Monitoring pin.<br>1'b0: FEED_OUT is disabled.<br>1'b1: FEED_OUT is enabled. |
| 13:9 | RO | 0x00 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8:4 | RW | 0x00 | d1apll_extafc<br>EXTAFC: Monitoring pin.<br>If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 3 | RW | 0x0 | d1apll_afc_enb<br>AFC_ENB: Monitoring pin.<br>1'b0: AFC is enabled and VCO is calibrated automatically.<br>1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | d1apll_sscg_en<br>SSCG_EN: Enable pin for dithered mode.<br>1'b0: disable dithered mode.<br>1'b1: enable dithered mode. |

**DDR1CRU_D1APLL_CON5**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | d1apll_fout_mask<br>FOUT_MASK: Scaler's re-initialization time control pin. |

**DDR1CRU_D1APLL_CON6**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | d1apll_lock<br>LOCK: PLL lock flag.<br>1'b0: PLL is unlocked.<br>1'b1: PLL is locked. |
| 14:10 | RW | 0x00 | d1apll_afc_code<br>AFC_CODE: Monitoring pin.<br>Output code of AFC(5 bits). |
| 9:0 | RO | 0x000 | reserved |

**DDR1CRU_D1BPLL_CON0**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | d1bpll_bp<br>BYPASS: Bypass mode control signal.<br>1'b1: bypass mode is enabled. (FOUT = FIN).<br>1'b0: PLL operates normally. |
| 14:10 | RO | 0x00 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9:0 | RW | 0x000 | d1bpll_m<br>M: Division value of the 10-bit programmable main-divider.<br>PLL has to be reset if M value is changed.<br>64 <= pll_m <= 1023 |

**DDR1CRU_D1BPLL_CON1**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | d1bpll_resetb<br>RESETB: Power down control signal.<br>1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time.<br>1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset. |
| 12:9 | RO | 0x0 | reserved |
| 8:6 | RW | 0x0 | d1bpll_s<br>Division value of the 3-bit programmable scaler.<br>0 <= pll_s <= 6 |
| 5:0 | RW | 0x00 | d1bpll_p<br>P: Division value of the 6-bit programmable pre-divider.<br>PLL has to be reset if P value is changed.<br>1 <= pll_p <= 63 |

**DDR1CRU_D1BPLL_CON2**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | d1bpll_k<br>K: Value of 16-bit DSM.<br>pll_k[15:0] is a two's complement integer. |

**DDR1CRU_D1BPLL_CON3**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | d1bpll_sel_pf<br>SEL_PF: Value of 2-bit modulation method control.<br>2'b00: down spread;<br>2'b01: up spread;<br>2'b1x: center spread.<br>PLL has to be reset if pll_sel_pf is changed. |
| 13:8 | RW | 0x00 | d1bpll_mrr<br>MRR: Value of 6-bit modulation rate control.<br>PLL has to be reset if pll_mrr is changed. |
| 7:0 | RW | 0x00 | d1bpll_mfr<br>MFR: Value of 8-bit modulation frequency control.<br>PLL has to be reset if pll_mfr is changed. |

Rockchip Confidential

**DDR1CRU_D1BPLL_CON4**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | d1bpll_fsel<br>FSEL: Monitoring pin.<br>1'b0: FEED_OUT = FREF.<br>1'b1: FEED_OUT = FEED. |
| 14 | RW | 0x0 | d1bpll_feed_en<br>FEED_EN: Monitoring pin.<br>1'b0: FEED_OUT is disabled.<br>1'b1: FEED_OUT is enabled. |
| 13:9 | RO | 0x00 | reserved |
| 8:4 | RW | 0x00 | d1bpll_extafc<br>EXTAFC: Monitoring pin.<br>If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 3 | RW | 0x0 | d1bpll_afc_enb<br>AFC_ENB: Monitoring pin.<br>1'b0: AFC is enabled and VCO is calibrated automatically.<br>1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | d1bpll_sscg_en<br>SSCG_EN: Enable pin for dithered mode.<br>1'b0: disable dithered mode.<br>1'b1: enable dithered mode. |

**DDR1CRU_D1BPLL_CON5**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | d1bpll_fout_mask<br>FOUT_MASK: Scaler's re-initialization time control pin. |

**DDR1CRU_D1BPLL_CON6**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | d1bpll_lock<br>LOCK: PLL lock flag.<br>1'b0: PLL is unlocked.<br>1'b1: PLL is locked. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14:10 | RW | 0x00 | d1bpll_afc_code<br>AFC_CODE: Monitoring pin.<br>Output code of AFC(5 bits). |
| 9:0 | RO | 0x000 | reserved |

**DDR1CRU_CLKSEL_CON00**

Address: Operational Base + offset (0x0300)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | clk_ddrphy2x_ch1_sel<br>clk_ddrphy2x_ch1 clock mux.<br>1'b0: clk_d1apll_t<br>1'b1: clk_d1bpll |

**DDR1CRU_GATE_CON00**

Address: Operational Base + offset (0x0800)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x0 | clk_osc_ddrphy_ch1_en<br>clk_osc_ddrphy_ch1 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_ddrphy_ch1_en<br>pclk_ddrphy_ch1 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_ddr_cru_ch1_en<br>pclk_ddr_cru_ch1 clock gating control.<br>When high, disable clock |
| 2:0 | RO | 0x0 | reserved |

**DDR1CRU_SOFTRST_CON00**

Address: Operational Base + offset (0x0A00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:5 | RO | 0x000 | reserved |
| 4 | RW | 0x0 | presetn_ddrphy_ch1<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_ddr_cru_ch1<br>When high, reset relative logic |
| 2 | RW | 0x1 | resetn_ddrphy2x_ch1<br>When high, reset relative logic |
| 1 | RW | 0x1 | resetn_ddrphy2xdiv_ch1<br>div_rst_n at ddr ch1<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RO | 0x0 | reserved |

# 2.7 DDR2CRU Register Description

## 2.7.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| DDR2CRU_D2APLL_CON0 | 0x0000 | W | 0x00008000 | D2APLL configuration register 0 |
| DDR2CRU_D2APLL_CON1 | 0x0004 | W | 0x00000000 | D2APLL configuration register 1 |
| DDR2CRU_D2APLL_CON2 | 0x0008 | W | 0x00000000 | D2APLL configuration register 2 |
| DDR2CRU_D2APLL_CON3 | 0x000C | W | 0x00000000 | D2APLL configuration register 3 |
| DDR2CRU_D2APLL_CON4 | 0x0010 | W | 0x00000000 | D2APLL configuration register 4 |
| DDR2CRU_D2APLL_CON5 | 0x0014 | W | 0x00000000 | D2APLL configuration register 5 |
| DDR2CRU_D2APLL_CON6 | 0x0018 | W | 0x00000000 | D2APLL configuration register 6 |
| DDR2CRU_D2BPLL_CON0 | 0x0020 | W | 0x00008000 | D2BPLL configuration register 0 |
| DDR2CRU_D2BPLL_CON1 | 0x0024 | W | 0x00000000 | D2BPLL configuration register 1 |
| DDR2CRU_D2BPLL_CON2 | 0x0028 | W | 0x00000000 | D2BPLL configuration register 2 |
| DDR2CRU_D2BPLL_CON3 | 0x002C | W | 0x00000000 | D2BPLL configuration register 3 |
| DDR2CRU_D2BPLL_CON4 | 0x0030 | W | 0x00000000 | D2BPLL configuration register 4 |
| DDR2CRU_D2BPLL_CON5 | 0x0034 | W | 0x00000000 | D2BPLL configuration register 5 |
| DDR2CRU_D2BPLL_CON6 | 0x0038 | W | 0x00000000 | D2BPLL configuration register 6 |
| DDR2CRU_CLKSEL_CON00 | 0x0300 | W | 0x00000000 | Internal clock select and division register 0 |
| DDR2CRU_GATE_CON00 | 0x0800 | W | 0x00000000 | Internal clock gate and division register 0 |
| DDR2CRU_SOFTRST_CON00 | 0x0A00 | W | 0x00000006 | Internal clock reset register 0 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 2.7.2 Detail Registers Description

**DDR2CRU_D2APLL_CON0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | d2apll_bp<br>BYPASS: Bypass mode control signal.<br>1'b1: bypass mode is enabled. (FOUT = FIN).<br>1'b0: PLL operates normally. |
| 14:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | d2apll_m<br>M: Division value of the 10-bit programmable main-divider.<br>PLL has to be reset if M value is changed.<br>64 <= pll_m <= 1023 |

**DDR2CRU_D2APLL_CON1**

Address: Operational Base + offset (0x0004)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | d2apll_resetb<br>RESETB: Power down control signal.<br>1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time.<br>1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset |
| 12:9 | RO | 0x0 | reserved |
| 8:6 | RW | 0x0 | d2apll_s<br>Division value of the 3-bit programmable scaler.<br>0 <= pll_s <= 6 |
| 5:0 | RW | 0x00 | d2apll_p<br>P: Division value of the 6-bit programmable pre-divider.<br>PLL has to be reset if P value is changed.<br>1 <= pll_p <= 63 |

**DDR2CRU_D2APLL_CON2**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | d2apll_k<br>K: Value of 16-bit DSM.<br>pll_k[15:0] is a two's complement integer. |

**DDR2CRU_D2APLL_CON3**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | d2apll_sel_pf<br>SEL_PF: Value of 2-bit modulation method control.<br>2'b00: down spread;<br>2'b01: up spread;<br>2'b1x: center spread.<br>PLL has to be reset if pll_sel_pf is changed. |
| 13:8 | RW | 0x00 | d2apll_mrr<br>MRR: Value of 6-bit modulation rate control.<br>PLL has to be reset if pll_mrr is changed. |
| 7:0 | RW | 0x00 | d2apll_mfr<br>MFR: Value of 8-bit modulation frequency control.<br>PLL has to be reset if pll_mfr is changed. |

**DDR2CRU_D2APLL_CON4**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x0 | d2apll_fsel<br>FSEL: Monitoring pin.<br>1'b0: FEED_OUT = FREF.<br>1'b1: FEED_OUT = FEED. |
| 14 | RW | 0x0 | d2apll_feed_en<br>FEED_EN: Monitoring pin.<br>1'b0: FEED_OUT is disabled.<br>1'b1: FEED_OUT is enabled. |
| 13:9 | RO | 0x00 | reserved |
| 8:4 | RW | 0x00 | d2apll_extafc<br>EXTAFC: Monitoring pin.<br>If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 3 | RW | 0x0 | d2apll_afc_enb<br>AFC_ENB: Monitoring pin.<br>1'b0: AFC is enabled and VCO is calibrated automatically.<br>1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | d2apll_sscg_en<br>SSCG_EN: Enable pin for dithered mode.<br>1'b0: disable dithered mode.<br>1'b1: enable dithered mode. |

**DDR2CRU_D2APLL_CON5**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | d2apll_fout_mask<br>FOUT_MASK: Scaler's re-initialization time control pin. |

**DDR2CRU_D2APLL_CON6**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | d2apll_lock<br>LOCK: PLL lock flag.<br>1'b0: PLL is unlocked.<br>1'b1: PLL is locked. |
| 14:10 | RW | 0x00 | d2apll_afc_code<br>AFC_CODE: Monitoring pin.<br>Output code of AFC(5 bits). |
| 9:0 | RO | 0x000 | reserved |

**DDR2CRU_D2BPLL_CON0**

Address: Operational Base + offset (0x0020)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | d2bpll_bp<br>BYPASS: Bypass mode control signal.<br>1'b1: bypass mode is enabled. (FOUT = FIN).<br>1'b0: PLL operates normally. |
| 14:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | d2bpll_m<br>M: Division value of the 10-bit programmable main-divider.<br>PLL has to be reset if M value is changed.<br>64 <= pll_m <= 1023 |

**DDR2CRU_D2BPLL_CON1**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | d2bpll_resetb<br>RESETB: Power down control signal.<br>1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time.<br>1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset. |
| 12:9 | RO | 0x0 | reserved |
| 8:6 | RW | 0x0 | d2bpll_s<br>Division value of the 3-bit programmable scaler.<br>0 <= pll_s <= 6 |
| 5:0 | RW | 0x00 | d2bpll_p<br>P: Division value of the 6-bit programmable pre-divider.<br>PLL has to be reset if P value is changed.<br>1 <= pll_p <= 63 |

**DDR2CRU_D2BPLL_CON2**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | d2bpll_k<br>K: Value of 16-bit DSM.<br>pll_k[15:0] is a two's complement integer. |

**DDR2CRU_D2BPLL_CON3**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:14 | RW | 0x0 | d2bpll_sel_pf<br>SEL_PF: Value of 2-bit modulation method control.<br>2'b00: down spread;<br>2'b01: up spread;<br>2'b1x: center spread.<br>PLL has to be reset if pll_sel_pf is changed. |
| 13:8 | RW | 0x00 | d2bpll_mrr<br>MRR: Value of 6-bit modulation rate control.<br>PLL has to be reset if pll_mrr is changed. |
| 7:0 | RW | 0x00 | d2bpll_mfr<br>MFR: Value of 8-bit modulation frequency control.<br>PLL has to be reset if pll_mfr is changed. |

**DDR2CRU_D2BPLL_CON4**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | d2bpll_fsel<br>FSEL: Monitoring pin.<br>1'b0: FEED_OUT = FREF.<br>1'b1: FEED_OUT = FEED. |
| 14 | RW | 0x0 | d2bpll_feed_en<br>FEED_EN: Monitoring pin.<br>1'b0: FEED_OUT is disabled.<br>1'b1: FEED_OUT is enabled. |
| 13:9 | RO | 0x00 | reserved |
| 8:4 | RW | 0x00 | d2bpll_extafc<br>EXTAFC: Monitoring pin.<br>If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 3 | RW | 0x0 | d2bpll_afc_enb<br>AFC_ENB: Monitoring pin.<br>1'b0: AFC is enabled and VCO is calibrated automatically.<br>1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | d2bpll_sscg_en<br>SSCG_EN: Enable pin for dithered mode.<br>1'b0: disable dithered mode.<br>1'b1: enable dithered mode. |

**DDR2CRU_D2BPLL_CON5**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | d2bpll_fout_mask<br>FOUT_MASK: Scaler's re-initialization time control pin. |

Rockchip Confidencial

**DDR2CRU_D2BPLL_CON6**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | d2bpll_lock<br>LOCK: PLL lock flag.<br>1'b0: PLL is unlocked.<br>1'b1: PLL is locked. |
| 14:10 | RW | 0x00 | d2bpll_afc_code<br>AFC_CODE: Monitoring pin.<br>Output code of AFC(5 bits). |
| 9:0 | RO | 0x000 | reserved |

**DDR2CRU_CLKSEL_CON00**

Address: Operational Base + offset (0x0300)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | clk_ddrphy2x_ch2_sel<br>clk_ddrphy2x_ch2 clock mux.<br>1'b0: clk_d2apll_t<br>1'b1: clk_d2bpll |

**DDR2CRU_GATE_CON00**

Address: Operational Base + offset (0x0800)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x0 | clk_osc_ddrphy_ch2_en<br>clk_osc_ddrphy_ch2 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_ddrphy_ch2_en<br>pclk_ddrphy_ch2 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_ddr_cru_ch2_en<br>pclk_ddr_cru_ch2 clock gating control.<br>When high, disable clock |
| 2:0 | RO | 0x0 | reserved |

**DDR2CRU_SOFTRST_CON00**

Address: Operational Base + offset (0x0A00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:5 | RO | 0x000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | presetn_ddrphy_ch2<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_ddr_cru_ch2<br>When high, reset relative logic |
| 2 | RW | 0x1 | resetn_ddrphy2x_ch2<br>When high, reset relative logic |
| 1 | RW | 0x1 | resetn_ddrphy2xdiv_ch2<br>div_rst_n at ddr ch2<br>When high, reset relative logic |
| 0 | RO | 0x0 | reserved |

# 2.8 DDR3CRU Register Description

## 2.8.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| DDR3CRU_D3APLL_CON0 | 0x0000 | W | 0x00008000 | D3APLL configuration register 0 |
| DDR3CRU_D3APLL_CON1 | 0x0004 | W | 0x00000000 | D3APLL configuration register 1 |
| DDR3CRU_D3APLL_CON2 | 0x0008 | W | 0x00000000 | D3APLL configuration register 2 |
| DDR3CRU_D3APLL_CON3 | 0x000C | W | 0x00000000 | D3APLL configuration register 3 |
| DDR3CRU_D3APLL_CON4 | 0x0010 | W | 0x00000000 | D3APLL configuration register 4 |
| DDR3CRU_D3APLL_CON5 | 0x0014 | W | 0x00000000 | D3APLL configuration register 5 |
| DDR3CRU_D3APLL_CON6 | 0x0018 | W | 0x00000000 | D3APLL configuration register 6 |
| DDR3CRU_D3BPLL_CON0 | 0x0020 | W | 0x00008000 | D3BPLL configuration register 0 |
| DDR3CRU_D3BPLL_CON1 | 0x0024 | W | 0x00000000 | D3BPLL configuration register 1 |
| DDR3CRU_D3BPLL_CON2 | 0x0028 | W | 0x00000000 | D3BPLL configuration register 2 |
| DDR3CRU_D3BPLL_CON3 | 0x002C | W | 0x00000000 | D3BPLL configuration register 3 |
| DDR3CRU_D3BPLL_CON4 | 0x0030 | W | 0x00000000 | D3BPLL configuration register 4 |
| DDR3CRU_D3BPLL_CON5 | 0x0034 | W | 0x00000000 | D3BPLL configuration register 5 |
| DDR3CRU_D3BPLL_CON6 | 0x0038 | W | 0x00000000 | D3BPLL configuration register 6 |
| DDR3CRU_CLKSEL_CON00 | 0x0300 | W | 0x00000000 | Internal clock select and division register 0 |
| DDR3CRU_GATE_CON00 | 0x0800 | W | 0x00000000 | Internal clock gate and division register 0 |
| DDR3CRU_SOFTRST_CON00 | 0x0A00 | W | 0x00000006 | Internal clock reset register 0 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 2.8.2 Detail Registers Description

**DDR3CRU_D3APLL_CON0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | d3apll_bp<br>BYPASS: Bypass mode control signal.<br>1'b1: bypass mode is enabled. (FOUT = FIN).<br>1'b0: PLL operates normally. |
| 14:10 | RO | 0x00 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9:0 | RW | 0x000 | d3apll_m<br>M: Division value of the 10-bit programmable main-divider.<br>PLL has to be reset if M value is changed.<br>64 <= pll_m <= 1023 |

**DDR3CRU_D3APLL_CON1**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | d3apll_resetb<br>RESETB: Power down control signal.<br>1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time.<br>1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset. |
| 12:9 | RO | 0x0 | reserved |
| 8:6 | RW | 0x0 | d3apll_s<br>Division value of the 3-bit programmable scaler.<br>0 <= pll_s <= 6 |
| 5:0 | RW | 0x00 | d3apll_p<br>P: Division value of the 6-bit programmable pre-divider.<br>PLL has to be reset if P value is changed.<br>1 <= pll_p <= 63 |

**DDR3CRU_D3APLL_CON2**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | d3apll_k<br>K: Value of 16-bit DSM.<br>pll_k[15:0] is a two's complement integer. |

**DDR3CRU_D3APLL_CON3**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | d3apll_sel_pf<br>SEL_PF: Value of 2-bit modulation method control.<br>2'b00: down spread;<br>2'b01: up spread;<br>2'b1x: center spread.<br>PLL has to be reset if pll_sel_pf is changed. |
| 13:8 | RW | 0x00 | d3apll_mrr<br>MRR: Value of 6-bit modulation rate control.<br>PLL has to be reset if pll_mrr is changed. |
| 7:0 | RW | 0x00 | d3apll_mfr<br>MFR: Value of 8-bit modulation frequency control.<br>PLL has to be reset if pll_mfr is changed. |

Rockchip Confidential

**DDR3CRU_D3APLL_CON4**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | d3apll_fsel<br>FSEL: Monitoring pin.<br>1'b0: FEED_OUT = FREF.<br>1'b1: FEED_OUT = FEED. |
| 14 | RW | 0x0 | d3apll_feed_en<br>FEED_EN: Monitoring pin.<br>1'b0: FEED_OUT is disabled.<br>1'b1: FEED_OUT is enabled. |
| 13:9 | RO | 0x00 | reserved |
| 8:4 | RW | 0x00 | d3apll_extafc<br>EXTAFC: Monitoring pin.<br>If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 3 | RW | 0x0 | d3apll_afc_enb<br>AFC_ENB: Monitoring pin.<br>1'b0: AFC is enabled and VCO is calibrated automatically.<br>1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | d3apll_sscg_en<br>SSCG_EN: Enable pin for dithered mode.<br>1'b0: disable dithered mode.<br>1'b1: enable dithered mode. |

**DDR3CRU_D3APLL_CON5**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | d3apll_fout_mask<br>FOUT_MASK: Scaler's re-initialization time control pin. |

**DDR3CRU_D3APLL_CON6**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | d3apll_lock<br>LOCK: PLL lock flag.<br>1'b0: PLL is unlocked.<br>1'b1: PLL is locked. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14:10 | RW | 0x00 | d3apll_afc_code<br>AFC_CODE: Monitoring pin.<br>Output code of AFC(5 bits). |
| 9:0 | RO | 0x000 | reserved |

**DDR3CRU_D3BPLL_CON0**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | d3bpll_bp<br>BYPASS: Bypass mode control signal.<br>1'b1: bypass mode is enabled. (FOUT = FIN).<br>1'b0: PLL operates normally. |
| 14:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | d3bpll_m<br>M: Division value of the 10-bit programmable main-divider.<br>PLL has to be reset if M value is changed.<br>64 <= pll_m <= 1023 |

**DDR3CRU_D3BPLL_CON1**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | d3bpll_resetb<br>RESETB: Power down control signal.<br>1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time.<br>1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset.. |
| 12:9 | RO | 0x0 | reserved |
| 8:6 | RW | 0x0 | d3bpll_s<br>Division value of the 3-bit programmable scaler.<br>0 <= pll_s <= 6 |
| 5:0 | RW | 0x00 | d3bpll_p<br>P: Division value of the 6-bit programmable pre-divider.<br>PLL has to be reset if P value is changed.<br>1 <= pll_p <= 63 |

**DDR3CRU_D3BPLL_CON2**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | d3bpll_k<br>K: Value of 16-bit DSM.<br>pll_k[15:0] is a two's complement integer. |

**DDR3CRU_D3BPLL_CON3**

Address: Operational Base + offset (0x002C)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | d3bpll_sel_pf<br>SEL_PF: Value of 2-bit modulation method control.<br>2'b00: down spread;<br>2'b01: up spread;<br>2'b1x: center spread.<br>PLL has to be reset if pll_sel_pf is changed. |
| 13:8 | RW | 0x00 | d3bpll_mrr<br>MRR: Value of 6-bit modulation rate control.<br>PLL has to be reset if pll_mrr is changed. |
| 7:0 | RW | 0x00 | d3bpll_mfr<br>MFR: Value of 8-bit modulation frequency control.<br>PLL has to be reset if pll_mfr is changed. |

**DDR3CRU_D3BPLL_CON4**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | d3bpll_fsel<br>FSEL: Monitoring pin.<br>1'b0: FEED_OUT = FREF.<br>1'b1: FEED_OUT = FEED. |
| 14 | RW | 0x0 | d3bpll_feed_en<br>FEED_EN: Monitoring pin.<br>1'b0: FEED_OUT is disabled.<br>1'b1: FEED_OUT is enabled. |
| 13:9 | RO | 0x00 | reserved |
| 8:4 | RW | 0x00 | d3bpll_extafc<br>EXTAFC: Monitoring pin.<br>If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 3 | RW | 0x0 | d3bpll_afc_enb<br>AFC_ENB: Monitoring pin.<br>1'b0: AFC is enabled and VCO is calibrated automatically.<br>1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | d3bpll_sscg_en<br>SSCG_EN: Enable pin for dithered mode.<br>1'b0: disable dithered mode.<br>1'b1: enable dithered mode. |

**DDR3CRU_D3BPLL_CON5**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | d3bpll_fout_mask<br>FOUT_MASK: Scaler's re-initialization time control pin. |

**DDR3CRU_D3BPLL_CON6**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | d3bpll_lock<br>LOCK: PLL lock flag.<br>1'b0: PLL is unlocked.<br>1'b1: PLL is locked. |
| 14:10 | RW | 0x00 | d3bpll_afc_code<br>AFC_CODE: Monitoring pin.<br>Output code of AFC(5 bits). |
| 9:0 | RO | 0x000 | reserved |

**DDR3CRU_CLKSEL_CON00**

Address: Operational Base + offset (0x0300)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | clk_ddrphy2x_ch3_sel<br>clk_ddrphy2x_ch3 clock mux.<br>1'b0: clk_d3apll_t<br>1'b1: clk_d3bpll |

**DDR3CRU_GATE_CON00**

Address: Operational Base + offset (0x0800)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x0 | clk_osc_ddrphy_ch3_en<br>clk_osc_ddrphy_ch3 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_ddrphy_ch3_en<br>pclk_ddrphy_ch3 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_ddr_cru_ch3_en<br>pclk_ddr_cru_ch3 clock gating control.<br>When high, disable clock |
| 2:0 | RO | 0x0 | reserved |

**DDR3CRU_SOFTRST_CON00**

Address: Operational Base + offset (0x0A00)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:5 | RO | 0x000 | reserved |
| 4 | RW | 0x0 | presetn_ddrphy_ch3<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_ddr_cru_ch3<br>When high, reset relative logic |
| 2 | RW | 0x1 | resetn_ddrphy2x_ch3<br>When high, reset relative logic |
| 1 | RW | 0x1 | resetn_ddrphy2xdiv_ch3<br>div_rst_n at ddr ch3<br>When high, reset relative logic |
| 0 | RO | 0x0 | reserved |

# 2.9 BIGCORE0CRU Register Description

## 2.9.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| BIGCORE0CRU_B0PLL_CON0 | 0x0000 | W | 0x00000000 | B0PLL configuration register 0 |
| BIGCORE0CRU_B0PLL_CON1 | 0x0004 | W | 0x00000000 | B0PLL configuration register 1 |
| BIGCORE0CRU_B0PLL_CON4 | 0x0010 | W | 0x00000002 | B0PLL configuration register 4 |
| BIGCORE0CRU_B0PLL_CON5 | 0x0014 | W | 0x000007E0 | B0PLL configuration register 5 |
| BIGCORE0CRU_B0PLL_CON6 | 0x0018 | W | 0x00000000 | B0PLL configuration register 6 |
| BIGCORE0CRU_MODE_CON00 | 0x0280 | W | 0x00000000 | Internal PLL mode select register 0 |
| BIGCORE0CRU_CLKSEL_CON00 | 0x0300 | W | 0x00000102 | Internal clock select and division register 0 |
| BIGCORE0CRU_CLKSEL_CON01 | 0x0304 | W | 0x00005F81 | Internal clock select and division register 1 |
| BIGCORE0CRU_CLKSEL_CON02 | 0x0308 | W | 0x00000000 | Internal clock select and division register 2 |
| BIGCORE0CRU_GATE_CON00 | 0x0800 | W | 0x00000400 | Internal clock gate and division register 0 |
| BIGCORE0CRU_GATE_CON01 | 0x0804 | W | 0x00000000 | Internal clock gate and division register 1 |
| BIGCORE0CRU_SOFTRST_CON00 | 0x0A00 | W | 0x00000330 | Internal clock reset register 0 |
| BIGCORE0CRU_SOFTRST_CON01 | 0x0A04 | W | 0x00000000 | Internal clock reset register 1 |
| BIGCORE0CRU_SMOTH_DIVFREE_CON04 | 0x0CC0 | W | 0x00000000 | Smoothdiv control register |
| BIGCORE0CRU_SMOTH_DIVFREE_CON05 | 0x0CC4 | W | 0x00000000 | Smoothdiv control register |

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| BIGCORE0CRU_AUTOCS_CLK_CORE_B01_I_CON0 | 0x0D00 | W | 0x00200004 | Auto clock switch control register 0 |
| BIGCORE0CRU_AUTOCS_CLK_CORE_B01_I_CON1 | 0x0D04 | W | 0x00000000 | Auto clock switch control register 1 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 2.9.2 Detail Registers Description

**BIGCORE0CRU_B0PLL_CON0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | b0pll_bp<br>BYPASS: Bypass mode control signal.<br>1'b1: bypass mode is enabled. (FOUT = FIN).<br>1'b0: PLL operates normally. |
| 14:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | b0pll_m<br>M: Division value of the 10-bit programmable main-divider.<br>PLL has to be reset if M value is changed.<br>64 <= pll_m <= 1023 |

**BIGCORE0CRU_B0PLL_CON1**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | b0pll_resetb<br>RESETB: Power down control signal.<br>1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time.<br>1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset. |
| 12:9 | RO | 0x0 | reserved |
| 8:6 | RW | 0x0 | b0pll_s<br>Division value of the 3-bit programmable scaler.<br>0 <= pll_s <= 6 |
| 5:0 | RW | 0x00 | b0pll_p<br>P: Division value of the 6-bit programmable pre-divider.<br>PLL has to be reset if P value is changed.<br>1 <= pll_p <= 63 |

**BIGCORE0CRU_B0PLL_CON4**

Address: Operational Base + offset (0x0010)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | b0pll_fsel<br>FSEL: Monitoring pin.<br>1'b0: FEED_OUT = FREF.<br>1'b1: FEED_OUT = FEED. |
| 14 | RW | 0x0 | b0pll_feed_en<br>FEED_EN: Monitoring pin.<br>1'b0: FEED_OUT is disabled.<br>1'b1: FEED_OUT is enabled. |
| 13:9 | RO | 0x00 | reserved |
| 8:4 | RW | 0x00 | b0pll_extafc<br>EXTAFC: Monitoring pin.<br>If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 3 | RW | 0x0 | b0pll_afc_enb<br>AFC_ENB: Monitoring pin.<br>1'b0: AFC is enabled and VCO is calibrated automatically.<br>1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 2:1 | RW | 0x1 | b0pll_icp<br>Charge-pump current control signal. |
| 0 | RO | 0x0 | reserved |

**BIGCORE0CRU_B0PLL_CON5**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10:9 | RW | 0x3 | b0pll_lock_con_dly<br>LOCK_CON_DLY: Lock detector setting of the detection resolution. |
| 8:7 | RW | 0x3 | b0pll_lock_con_out<br>LOCK_CON_OUT: Lock detector setting of the output margin. |
| 6:5 | RW | 0x3 | b0pll_lock_con_in<br>LOCK_CON_IN: Lock detector setting of the input margin. |
| 4:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | b0pll_fout_mask<br>FOUT_MASK: Scaler's re-initialization time control pin. |

**BIGCORE0CRU_B0PLL_CON6**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | b0pll_lock<br>LOCK: PLL lock flag.<br>1'b0: PLL is unlocked.<br>1'b1: PLL is locked. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14:10 | RW | 0x00 | b0pll_afc_code<br>AFC_CODE: Monitoring pin.<br>Output code of AFC(5 bits). |
| 9:0 | RO | 0x000 | reserved |

**BIGCORE0CRU_MODE_CON00**

Address: Operational Base + offset (0x0280)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1:0 | RW | 0x0 | clk_b0pll_mode<br>clk_b0pll_mux clock mux.<br>2'b00: xin_osc0_func<br>2'b01: clk_b0pll<br>2'b10: clk_deepslow |

**BIGCORE0CRU_CLKSEL_CON00**

Address: Operational Base + offset (0x0300)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:13 | RW | 0x0 | clk_core_b0_sel<br>clk_core_b0 clock mux.<br>2'b00: clk_core_b0_uc<br>2'b01: clk_core_b0_clean<br>2'b10: clk_core_b01_pvtpll_t |
| 12:8 | RW | 0x01 | clk_core_b0_uc_div<br>Divide clk_core_b0_uc by (div_con + 1). |
| 7:6 | RW | 0x0 | clk_core_b01_src_sel<br>clk_core_b01_src clock mux.<br>2'b00: clk_core_b01_slow_src<br>2'b01: clk_core_b01_gpll_src<br>2'b10: clk_b0pll |
| 5:1 | RW | 0x01 | clk_core_b01_gpll_src_div<br>Divide clk_core_b01_gpll_src by (div_con + 1). |
| 0 | RW | 0x0 | clk_core_b01_slow_src_sel<br>clk_core_b01_slow_src clock mux.<br>1'b0: xin_osc0_func<br>1'b1: clk_deepslow |

**BIGCORE0CRU_CLKSEL_CON01**

Address: Operational Base + offset (0x0304)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14 | RW | 0x1 | refclk_bigcore0_pvtpll_sel<br>refclk_bigcore0_pvtpll clock mux.<br>1'b0: clk_core_b01<br>1'b1: xin_osc0_func |
| 13 | RW | 0x0 | clk_testout_b0_sel<br>clk_testout_b0 clock mux.<br>1'b0: clk_b0pll<br>1'b1: clk_core_b01_pvtpll |
| 12:7 | RW | 0x3f | clk_testout_b0_div<br>Divide clk_testout_b0 by (div_con + 1). |
| 6:5 | RW | 0x0 | clk_core_b1_sel<br>clk_core_b1 clock mux.<br>2'b00: clk_core_b1_uc<br>2'b01: clk_core_b1_clean<br>2'b10: clk_core_b01_pvtpll_t |
| 4:0 | RW | 0x01 | clk_core_b1_uc_div<br>Divide clk_core_b1_uc by (div_con + 1). |

**BIGCORE0CRU_CLKSEL_CON02**

Address: Operational Base + offset (0x0308)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:3 | RO | 0x0000 | reserved |
| 2 | RW | 0x0 | clk_core_b01_pvtpll_t_sel<br>clk_core_b01_pvtpll_t clock mux.<br>1'b0: clk_deepslow<br>1'b1: clk_core_b01_pvtpll |
| 1:0 | RW | 0x0 | pclk_bigcore0_root_sel<br>pclk_bigcore0_root clock mux.<br>2'b00: clk_matrix_100m_src<br>2'b01: clk_matrix_50m_src<br>2'b10: xin_osc0_func |

**BIGCORE0CRU_GATE_CON00**

Address: Operational Base + offset (0x0800)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pclk_bigcore0_biu_en<br>pclk_bigcore0_biu clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | pclk_bigcore0_root_en<br>pclk_bigcore0_root clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | clk_core_bigcore0_pvtm_en<br>clk_core_bigcore0_pvtm clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | clk_bigcore0_pvtm_en<br>clk_bigcore0_pvtm clock gating control.<br>When high, disable clock |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11 | RW | 0x0 | refclk_bigcore0_pvtpll_en<br>refclk_bigcore0_pvtpll clock gating control.<br>When high, disable clock |
| 10 | RW | 0x1 | clk_testout_b0_en<br>clk_testout_b0 clock gating control.<br>When high, disable clock |
| 9:8 | RO | 0x0 | reserved |
| 7 | RW | 0x0 | clk_core_b1_uc_en<br>clk_core_b1_uc clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_core_b1_clean_en<br>clk_core_b1_clean clock gating control.<br>When high, disable clock |
| 5:4 | RO | 0x0 | reserved |
| 3 | RW | 0x0 | clk_core_b0_uc_en<br>clk_core_b0_uc clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | clk_core_b0_clean_en<br>clk_core_b0_clean clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_core_b01_i_en<br>clk_core_b01_i clock gating control.<br>When high, disable clock |
| 0 | RO | 0x0 | reserved |

**BIGCORE0CRU_GATE_CON01**

Address: Operational Base + offset (0x0804)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:5 | RO | 0x000 | reserved |
| 4 | RW | 0x0 | clk_24m_bigcore0_cpuboost_en<br>clk_24m_bigcore0_cpuboost clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_bigcore0_cpuboost_en<br>pclk_bigcore0_cpuboost clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | pclk_bigcore0_cru_en<br>pclk_bigcore0_cru clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | pclk_bigcore0_grf_en<br>pclk_bigcore0_grf clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | pclk_bigcore0_pvtm_en<br>pclk_bigcore0_pvtm clock gating control.<br>When high, disable clock |

**BIGCORE0CRU_SOFTRST_CON00**

Address: Operational Base + offset (0x0A00)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | presetn_bigcore0_biu<br>When high, reset relative logic |
| 14:13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | resetn_bigcore0_pvtm<br>When high, reset relative logic |
| 11 | RW | 0x0 | resetn_bigcore0_pvtpll<br>When high, reset relative logic |
| 10 | RO | 0x0 | reserved |
| 9 | RW | 0x1 | ncorereset_b1<br>When high, reset relative logic |
| 8 | RW | 0x1 | ncpuporeset_b1<br>When high, reset relative logic |
| 7:6 | RO | 0x0 | reserved |
| 5 | RW | 0x1 | ncorereset_b0<br>When high, reset relative logic |
| 4 | RW | 0x1 | ncpuporeset_b0<br>When high, reset relative logic |
| 3:0 | RO | 0x0 | reserved |

**BIGCORE0CRU_SOFTRST_CON01**

Address: Operational Base + offset (0x0A04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:5 | RO | 0x000 | reserved |
| 4 | RW | 0x0 | resetn_24m_bigcore0_cpuboost<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_bigcore0_cpuboost<br>When high, reset relative logic |
| 2 | RW | 0x0 | presetn_bigcore0_cru<br>When high, reset relative logic |
| 1 | RW | 0x0 | presetn_bigcore0_grf<br>When high, reset relative logic |
| 0 | RW | 0x0 | presetn_bigcore0_pvtm<br>When high, reset relative logic |

**BIGCORE0CRU_SMOTH_DIVFREE_CON04**

Address: Operational Base + offset (0x0CC0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | clk_core_b0_uc_freq_keep<br>freq_keep<br>Cycles to keep every step. |
| 15 | RW | 0x0 | clk_core_b0_uc_bypass<br>bypass<br>Division signal bypass.<br>1'b1: Bypass.<br>1'b0: Use Smoothdiv to control clock division. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14 | RW | 0x0 | clk_core_b0_uc_gate_smth_en<br>gate_smth_en<br>If trigger smoothdiv function when clk been gated.<br>1'b1: Enable.<br>1'b0: Disable. |
| 13 | RW | 0x0 | clk_core_b0_uc_smdiv_clk_off<br>smdiv_clk_off<br>Turn off smoothdiv module clk.<br>1'b1: Turn off.<br>1'b0: Turn on. |
| 12:5 | RO | 0x00 | reserved |
| 4:0 | RW | 0x00 | clk_core_b0_uc_step<br>step<br>Step of div from 0x1f to setting configuration . |

**BIGCORE0CRU_SMOTH_DIVFREE_CON05**

Address: Operational Base + offset (0x0CC4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | clk_core_b1_uc_freq_keep<br>freq_keep<br>Cycles to keep every step. |
| 15 | RW | 0x0 | clk_core_b1_uc_bypass<br>bypass<br>Division signal bypass.<br>1'b1: Bypass.<br>1'b0: Use Smoothdiv to control clock division. |
| 14 | RW | 0x0 | clk_core_b1_uc_gate_smth_en<br>gate_smth_en<br>If trigger smoothdiv function when clk been gated.<br>1'b1: Enable.<br>1'b0: Disable. |
| 13 | RW | 0x0 | clk_core_b1_uc_smdiv_clk_off<br>smdiv_clk_off<br>Turn off smoothdiv module clk.<br>1'b1: Turn off.<br>1'b0: Turn on. |
| 12:5 | RO | 0x00 | reserved |
| 4:0 | RW | 0x00 | clk_core_b1_uc_step<br>step<br>Step of div from 0x1f to setting configuration . |

**BIGCORE0CRU_AUTOCS_CLK_CORE_B01_I_CON0**

Address: Operational Base + offset (0x0D00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | clk_core_b01_i_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | clk_core_b01_i_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**BIGCORE0CRU_AUTOCS_CLK_CORE_B01_I_CON1**

Address: Operational Base + offset (0x0D04)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | clk_core_b01_i_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | clk_core_b01_i_switch_en<br>switch_en<br>1'b1: Enable clk_core_b01_i switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | clk_core_b01_i_autocs_en<br>autocs_en<br>1'b1: Enable clk_core_b01_i switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | clk_core_b01_i_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable clk_core_b01_i switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

## 2.10 BIGCORE1CRU Register Description

### 2.10.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| BIGCORE1CRU_B1PLL_CON0 | 0x0020 | W | 0x00000000 | B1PLL configuration register 0 |
| BIGCORE1CRU_B1PLL_CON1 | 0x0024 | W | 0x00000000 | B1PLL configuration register 1 |
| BIGCORE1CRU_B1PLL_CON4 | 0x0030 | W | 0x00000002 | B1PLL configuration register 4 |
| BIGCORE1CRU_B1PLL_CON5 | 0x0034 | W | 0x000007E0 | B1PLL configuration register 5 |
| BIGCORE1CRU_B1PLL_CON6 | 0x0038 | W | 0x00000000 | B1PLL configuration register 6 |
| BIGCORE1CRU_MODE_CON00 | 0x0280 | W | 0x00000000 | Internal PLL mode select register 0 |
| BIGCORE1CRU_CLKSEL_CON00 | 0x0300 | W | 0x00000102 | Internal clock select and division register 0 |
| BIGCORE1CRU_CLKSEL_CON01 | 0x0304 | W | 0x00005F81 | Internal clock select and division register 1 |
| BIGCORE1CRU_CLKSEL_CON02 | 0x0308 | W | 0x00000000 | Internal clock select and division register 2 |
| BIGCORE1CRU_GATE_CON00 | 0x0800 | W | 0x00000400 | Internal clock gate and division register 0 |
| BIGCORE1CRU_GATE_CON01 | 0x0804 | W | 0x00000000 | Internal clock gate and division register 1 |

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| BIGCORE1CRU_SOFTRST_CON00 | 0x0A00 | W | 0x00000330 | Internal clock reset register 0 |
| BIGCORE1CRU_SOFTRST_CON01 | 0x0A04 | W | 0x00000000 | Internal clock reset register 1 |
| BIGCORE1CRU_SMOTH_DIVFREE_CON06 | 0x0CC0 | W | 0x00000000 | Smoothdiv control register |
| BIGCORE1CRU_SMOTH_DIVFREE_CON07 | 0x0CC4 | W | 0x00000000 | Smoothdiv control register |
| BIGCORE1CRU_AUTOCS_CLK_CORE_B23_I_CON0 | 0x0D00 | W | 0x00200004 | Auto clock switch control register 0 |
| BIGCORE1CRU_AUTOCS_CLK_CORE_B23_I_CON1 | 0x0D04 | W | 0x00000000 | Auto clock switch control register 1 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 2.10.2 Detail Registers Description

**BIGCORE1CRU_B1PLL_CON0**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | b1pll_bp<br>BYPASS: Bypass mode control signal.<br>1'b1: bypass mode is enabled. (FOUT = FIN).<br>1'b0: PLL operates normally. |
| 14:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | b1pll_m<br>M: Division value of the 10-bit programmable main-divider.<br>PLL has to be reset if M value is changed.<br>64 <= pll_m <= 1023 |

**BIGCORE1CRU_B1PLL_CON1**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | b1pll_resetb<br>RESETB: Power down control signal.<br>1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time.<br>1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset. |
| 12:9 | RO | 0x0 | reserved |
| 8:6 | RW | 0x0 | b1pll_s<br>Division value of the 3-bit programmable scaler.<br>0 <= pll_s <= 6 |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5:0 | RW | 0x00 | b1pll_p<br>P: Division value of the 6-bit programmable pre-divider.<br>PLL has to be reset if P value is changed.<br>1 <= pll_p <= 63 |

**BIGCORE1CRU_B1PLL_CON4**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | b1pll_fsel<br>FSEL: Monitoring pin.<br>1'b0: FEED_OUT = FREF.<br>1'b1: FEED_OUT = FEED. |
| 14 | RW | 0x0 | b1pll_feed_en<br>FEED_EN: Monitoring pin.<br>1'b0: FEED_OUT is disabled.<br>1'b1: FEED_OUT is enabled. |
| 13:9 | RO | 0x00 | reserved |
| 8:4 | RW | 0x00 | b1pll_extafc<br>EXTAFC: Monitoring pin.<br>If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 3 | RW | 0x0 | b1pll_afc_enb<br>AFC_ENB: Monitoring pin.<br>1'b0: AFC is enabled and VCO is calibrated automatically.<br>1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 2:1 | RW | 0x1 | b1pll_icp<br>Charge-pump current control signal. |
| 0 | RO | 0x0 | reserved |

**BIGCORE1CRU_B1PLL_CON5**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10:9 | RW | 0x3 | b1pll_lock_con_dly<br>LOCK_CON_DLY: Lock detector setting of the detection resolution. |
| 8:7 | RW | 0x3 | b1pll_lock_con_out<br>LOCK_CON_OUT: Lock detector setting of the output margin. |
| 6:5 | RW | 0x3 | b1pll_lock_con_in<br>LOCK_CON_IN: Lock detector setting of the input margin. |
| 4:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | b1pll_fout_mask<br>FOUT_MASK: Scaler's re-initialization time control pin. |

**BIGCORE1CRU_B1PLL_CON6**

Address: Operational Base + offset (0x0038)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | b1pll_lock<br>LOCK: PLL lock flag.<br>1'b0: PLL is unlocked.<br>1'b1: PLL is locked. |
| 14:10 | RW | 0x00 | b1pll_afc_code<br>AFC_CODE: Monitoring pin.<br>Output code of AFC(5 bits). |
| 9:0 | RO | 0x000 | reserved |

**BIGCORE1CRU_MODE_CON00**

Address: Operational Base + offset (0x0280)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1:0 | RW | 0x0 | clk_b1pll_mode<br>clk_b1pll_mux clock mux.<br>2'b00: xin_osc0_func<br>2'b01: clk_b1pll<br>2'b10: clk_deepslow |

**BIGCORE1CRU_CLKSEL_CON00**

Address: Operational Base + offset (0x0300)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:13 | RW | 0x0 | clk_core_b2_sel<br>clk_core_b2 clock mux.<br>2'b00: clk_core_b2_uc<br>2'b01: clk_core_b2_clean<br>2'b10: clk_core_b23_pvtpll_t |
| 12:8 | RW | 0x01 | clk_core_b2_uc_div<br>Divide clk_core_b2_uc by (div_con + 1). |
| 7:6 | RW | 0x0 | clk_core_b23_src_sel<br>clk_core_b23_src clock mux.<br>2'b00: clk_core_b23_slow_src<br>2'b01: clk_core_b23_gpll_src<br>2'b10: clk_b1pll |
| 5:1 | RW | 0x01 | clk_core_b23_gpll_src_div<br>Divide clk_core_b23_gpll_src by (div_con + 1). |
| 0 | RW | 0x0 | clk_core_b23_slow_src_sel<br>clk_core_b23_slow_src clock mux.<br>1'b0: xin_osc0_func<br>1'b1: clk_deepslow |

**BIGCORE1CRU_CLKSEL_CON01**

Rockchip Confidencial

Address: Operational Base + offset (0x0304)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x1 | refclk_bigcore1_pvtpll_sel<br>refclk_bigcore1_pvtpll clock mux.<br>1'b0: clk_core_b23<br>1'b1: xin_osc0_func |
| 13 | RW | 0x0 | clk_testout_b1_sel<br>clk_testout_b1 clock mux.<br>1'b0: clk_b1pll<br>1'b1: clk_core_b23_pvtpll |
| 12:7 | RW | 0x3f | clk_testout_b1_div<br>Divide clk_testout_b1 by (div_con + 1). |
| 6:5 | RW | 0x0 | clk_core_b3_sel<br>clk_core_b3 clock mux.<br>2'b00: clk_core_b3_uc<br>2'b01: clk_core_b3_clean<br>2'b10: clk_core_b23_pvtpll_t |
| 4:0 | RW | 0x01 | clk_core_b3_uc_div<br>Divide clk_core_b3_uc by (div_con + 1). |

**BIGCORE1CRU_CLKSEL_CON02**

Address: Operational Base + offset (0x0308)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:3 | RO | 0x0000 | reserved |
| 2 | RW | 0x0 | clk_core_b23pvtpll_t_sel<br>clk_core_b23pvtpll_t clock mux.<br>1'b0: clk_deepslow<br>1'b1: clk_core_b23pvtpll |
| 1:0 | RW | 0x0 | pclk_bigcore1_root_sel<br>pclk_bigcore1_root clock mux.<br>2'b00: clk_matrix_100m_src<br>2'b01: clk_matrix_50m_src<br>2'b10: xin_osc0_func |

**BIGCORE1CRU_GATE_CON00**

Address: Operational Base + offset (0x0800)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pclk_bigcore1_biu_en<br>pclk_bigcore1_biu clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | pclk_bigcore1_root_en<br>pclk_bigcore1_root clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | clk_core_bigcore1_pvtm_en<br>clk_core_bigcore1_pvtm clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | clk_bigcore1_pvtm_en<br>clk_bigcore1_pvtm clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | refclk_bigcore1_pvtpll_en<br>refclk_bigcore1_pvtpll clock gating control.<br>When high, disable clock |
| 10 | RW | 0x1 | clk_testout_b1_en<br>clk_testout_b1 clock gating control.<br>When high, disable clock |
| 9:8 | RO | 0x0 | reserved |
| 7 | RW | 0x0 | clk_core_b3_uc_en<br>clk_core_b3_uc clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_core_b3_clean_en<br>clk_core_b3_clean clock gating control.<br>When high, disable clock |
| 5:4 | RO | 0x0 | reserved |
| 3 | RW | 0x0 | clk_core_b2_uc_en<br>clk_core_b2_uc clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | clk_core_b2_clean_en<br>clk_core_b2_clean clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_core_b23_i_en<br>clk_core_b23_i clock gating control.<br>When high, disable clock |
| 0 | RO | 0x0 | reserved |

**BIGCORE1CRU_GATE_CON01**

Address: Operational Base + offset (0x0804)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:5 | RO | 0x000 | reserved |
| 4 | RW | 0x0 | clk_24m_bigcore1_cpuboost_en<br>clk_24m_bigcore1_cpuboost clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_bigcore1_cpuboost_en<br>pclk_bigcore1_cpuboost clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | pclk_bigcore1_cru_en<br>pclk_bigcore1_cru clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | pclk_bigcore1_grf_en<br>pclk_bigcore1_grf clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | pclk_bigcore1_pvtm_en<br>pclk_bigcore1_pvtm clock gating control.<br>When high, disable clock |

Rockchip Confidencial

**BIGCORE1CRU_SOFTRST_CON00**

Address: Operational Base + offset (0x0A00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | presetn_bigcore1_biu<br>When high, reset relative logic |
| 14:13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | resetn_bigcore1_pvtm<br>When high, reset relative logic |
| 11 | RW | 0x0 | resetn_bigcore1_pvtpll<br>When high, reset relative logic |
| 10 | RO | 0x0 | reserved |
| 9 | RW | 0x1 | ncorereset_b3<br>When high, reset relative logic |
| 8 | RW | 0x1 | ncpuporeset_b3<br>When high, reset relative logic |
| 7:6 | RO | 0x0 | reserved |
| 5 | RW | 0x1 | ncorereset_b2<br>When high, reset relative logic |
| 4 | RW | 0x1 | ncpuporeset_b2<br>When high, reset relative logic |
| 3:0 | RO | 0x0 | reserved |

**BIGCORE1CRU_SOFTRST_CON01**

Address: Operational Base + offset (0x0A04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:5 | RO | 0x000 | reserved |
| 4 | RW | 0x0 | resetn_24m_bigcore1_cpuboost<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_bigcore1_cpuboost<br>When high, reset relative logic |
| 2 | RW | 0x0 | presetn_bigcore1_cru<br>When high, reset relative logic |
| 1 | RW | 0x0 | presetn_bigcore1_grf<br>When high, reset relative logic |
| 0 | RW | 0x0 | presetn_bigcore1_pvtm<br>When high, reset relative logic |

**BIGCORE1CRU_SMOTH_DIVFREE_CON06**

Address: Operational Base + offset (0x0CC0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | clk_core_b2_uc_freq_keep<br>freq_keep<br>Cycles to keep every step. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x0 | clk_core_b2_uc_bypass<br>bypass<br>Division signal bypass.<br>1'b1: Bypass.<br>1'b0: Use Smoothdiv to control clock division. |
| 14 | RW | 0x0 | clk_core_b2_uc_gate_smth_en<br>gate_smth_en<br>If trigger smoothdiv function when clk been gated.<br>1'b1: Enable.<br>1'b0: Disable. |
| 13 | RW | 0x0 | clk_core_b2_uc_smdiv_clk_off<br>smdiv_clk_off<br>Turn off smoothdiv module clk.<br>1'b1: Turn off.<br>1'b0: Turn on. |
| 12:5 | RO | 0x00 | reserved |
| 4:0 | RW | 0x00 | clk_core_b2_uc_step<br>step<br>Step of div from 0x1f to setting configuration . |

**BIGCORE1CRU_SMOTH_DIVFREE_CON07**

Address: Operational Base + offset (0x0CC4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | clk_core_b3_uc_freq_keep<br>freq_keep<br>Cycles to keep every step. |
| 15 | RW | 0x0 | clk_core_b3_uc_bypass<br>bypass<br>Division signal bypass.<br>1'b1: Bypass.<br>1'b0: Use Smoothdiv to control clock division. |
| 14 | RW | 0x0 | clk_core_b3_uc_gate_smth_en<br>gate_smth_en<br>If trigger smoothdiv function when clk been gated.<br>1'b1: Enable.<br>1'b0: Disable. |
| 13 | RW | 0x0 | clk_core_b3_uc_smdiv_clk_off<br>smdiv_clk_off<br>Turn off smoothdiv module clk.<br>1'b1: Turn off.<br>1'b0: Turn on. |
| 12:5 | RO | 0x00 | reserved |
| 4:0 | RW | 0x00 | clk_core_b3_uc_step<br>step<br>Step of div from 0x1f to setting configuration . |

**BIGCORE1CRU_AUTOCS_CLK_CORE_B23_I_CON0**

Address: Operational Base + offset (0x0D00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | clk_core_b23_i_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | clk_core_b23_i_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

Rockchip Confidencial

**BIGCORE1CRU_AUTOCS_CLK_CORE_B23_I_CON1**

Address: Operational Base + offset (0x0D04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | clk_core_b23_i_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | clk_core_b23_i_switch_en<br>switch_en<br>1'b1: Enable clk_core_b23_i switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | clk_core_b23_i_autocs_en<br>autocs_en<br>1'b1: Enable clk_core_b23_i switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | clk_core_b23_i_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable clk_core_b23_i switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

# 2.11 DSUCRU Register Description

## 2.11.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| DSUCRU_LPLL_CON0 | 0x0040 | W | 0x00000000 | LPLL configuration register 0 |
| DSUCRU_LPLL_CON1 | 0x0044 | W | 0x00000000 | LPLL configuration register 1 |
| DSUCRU_LPLL_CON4 | 0x0050 | W | 0x00000002 | LPLL configuration register 4 |
| DSUCRU_LPLL_CON5 | 0x0054 | W | 0x000007E0 | LPLL configuration register 5 |
| DSUCRU_LPLL_CON6 | 0x0058 | W | 0x00000000 | LPLL configuration register 6 |
| DSUCRU_MODE_CON00 | 0x0280 | W | 0x00000000 | Internal PLL mode select register 0 |
| DSUCRU_CLKSEL_CON00 | 0x0300 | W | 0x00002000 | Internal clock select and division register 0 |
| DSUCRU_CLKSEL_CON01 | 0x0304 | W | 0x00001082 | Internal clock select and division register 1 |
| DSUCRU_CLKSEL_CON02 | 0x0308 | W | 0x00000843 | Internal clock select and division register 2 |
| DSUCRU_CLKSEL_CON03 | 0x030C | W | 0x00000063 | Internal clock select and division register 3 |
| DSUCRU_CLKSEL_CON04 | 0x0310 | W | 0x00000643 | Internal clock select and division register 4 |
| DSUCRU_CLKSEL_CON05 | 0x0314 | W | 0x0000023F | Internal clock select and division register 5 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| DSUCRU_CLKSEL_CON06 | 0x0318 | W | 0x00000081 | Internal clock select and division register 6 |
| DSUCRU_CLKSEL_CON07 | 0x031C | W | 0x00000081 | Internal clock select and division register 7 |
| DSUCRU_GATE_CON00 | 0x0800 | W | 0x00000000 | Internal clock gate and division register 0 |
| DSUCRU_GATE_CON01 | 0x0804 | W | 0x00000000 | Internal clock gate and division register 1 |
| DSUCRU_GATE_CON02 | 0x0808 | W | 0x00000020 | Internal clock gate and division register 2 |
| DSUCRU_GATE_CON03 | 0x080C | W | 0x00000000 | Internal clock gate and division register 3 |
| DSUCRU_SOFTRST_CON00 | 0x0A00 | W | 0x00000000 | Internal clock reset register 0 |
| DSUCRU_SOFTRST_CON01 | 0x0A04 | W | 0x00000000 | Internal clock reset register 1 |
| DSUCRU_SOFTRST_CON02 | 0x0A08 | W | 0x00000000 | Internal clock reset register 2 |
| DSUCRU_SOFTRST_CON03 | 0x0A0C | W | 0x00000000 | Internal clock reset register 3 |
| DSUCRU_AUTOCS_ACLK_M_DSU_BIU_CON0 | 0x0D00 | W | 0x00200004 | Auto clock switch control register 0 |
| DSUCRU_AUTOCS_ACLK_M_DSU_BIU_CON1 | 0x0D04 | W | 0x00000000 | Auto clock switch control register 1 |
| DSUCRU_AUTOCS_ACLK_S_DSU_BIU_CON0 | 0x0D08 | W | 0x00200004 | Auto clock switch control register 0 |
| DSUCRU_AUTOCS_ACLK_S_DSU_BIU_CON1 | 0x0D0C | W | 0x00000000 | Auto clock switch control register 1 |
| DSUCRU_AUTOCS_ACLK_MP_DSU_BIU_CON0 | 0x0D10 | W | 0x00200004 | Auto clock switch control register 0 |
| DSUCRU_AUTOCS_ACLK_MP_DSU_BIU_CON1 | 0x0D14 | W | 0x00000000 | Auto clock switch control register 1 |
| DSUCRU_AUTOCS_SCLK_DSU_SRC_CON0 | 0x0D18 | W | 0x00200004 | Auto clock switch control register 0 |
| DSUCRU_AUTOCS_SCLK_DSU_SRC_CON1 | 0x0D1C | W | 0x00000000 | Auto clock switch control register 1 |
| DSUCRU_AUTOCS_CLK_CORE_L_CON0 | 0x0D20 | W | 0x00200004 | Auto clock switch control register 0 |
| DSUCRU_AUTOCS_CLK_CORE_L_CON1 | 0x0D24 | W | 0x00000000 | Auto clock switch control register 1 |
| DSUCRU_QCHANNEL_CON00 | 0x0F00 | W | 0x00000000 | Qchannel control register 1 |
| DSUCRU_SMOTH_DIVFREE_CON00 | 0x0F10 | W | 0x00000000 | Smoothdiv control register |
| DSUCRU_SMOTH_DIVFREE_CON01 | 0x0F14 | W | 0x00000000 | Smoothdiv control register |
| DSUCRU_SMOTH_DIVFREE_CON02 | 0x0F18 | W | 0x00000000 | Smoothdiv control register |
| DSUCRU_SMOTH_DIVFREE_CON03 | 0x0F1C | W | 0x00000000 | Smoothdiv control register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 2.11.2 Detail Registers Description

Rockchip Confidential

**DSUCRU_LPLL_CON0**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | lpll_bp<br>BYPASS: Bypass mode control signal.<br>1'b1: bypass mode is enabled. (FOUT = FIN).<br>1'b0: PLL operates normally. |
| 14:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | lpll_m<br>M: Division value of the 10-bit programmable main-divider.<br>PLL has to be reset if M value is changed.<br>64 <= pll_m <= 1023 |

**DSUCRU_LPLL_CON1**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | lpll_resetb<br>RESETB: Power down control signal.<br>1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time.<br>1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset. |
| 12:9 | RO | 0x0 | reserved |
| 8:6 | RW | 0x0 | lpll_s<br>Division value of the 3-bit programmable scaler.<br>0 <= pll_s <= 6 |
| 5:0 | RW | 0x00 | lpll_p<br>P: Division value of the 6-bit programmable pre-divider.<br>PLL has to be reset if P value is changed.<br>1 <= pll_p <= 63 |

**DSUCRU_LPLL_CON4**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | lpll_fsel<br>FSEL: Monitoring pin.<br>1'b0: FEED_OUT = FREF.<br>1'b1: FEED_OUT = FEED. |
| 14 | RW | 0x0 | lpll_feed_en<br>FEED_EN: Monitoring pin.<br>1'b0: FEED_OUT is disabled.<br>1'b1: FEED_OUT is enabled. |
| 13:9 | RO | 0x00 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8:4 | RW | 0x00 | lpll_extafc<br>EXTAFC: Monitoring pin.<br>If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 3 | RW | 0x0 | lpll_afc_enb<br>AFC_ENB: Monitoring pin.<br>1'b0: AFC is enabled and VCO is calibrated automatically.<br>1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 2:1 | RW | 0x1 | lpll_icp<br>Charge-pump current control signal. |
| 0 | RO | 0x0 | reserved |

**DSUCRU_LPLL_CON5**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10:9 | RW | 0x3 | lpll_lock_con_dly<br>LOCK_CON_DLY: Lock detector setting of the detection resolution. |
| 8:7 | RW | 0x3 | lpll_lock_con_out<br>LOCK_CON_OUT: Lock detector setting of the output margin. |
| 6:5 | RW | 0x3 | lpll_lock_con_in<br>LOCK_CON_IN: Lock detector setting of the input margin. |
| 4:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | lpll_fout_mask<br>FOUT_MASK: Scaler's re-initialization time control pin. |

**DSUCRU_LPLL_CON6**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | lpll_lock<br>LOCK: PLL lock flag.<br>1'b0: PLL is unlocked.<br>1'b1: PLL is locked. |
| 14:10 | RW | 0x00 | lpll_afc_code<br>AFC_CODE: Monitoring pin.<br>Output code of AFC(5 bits). |
| 9:0 | RO | 0x000 | reserved |

**DSUCRU_MODE_CON00**

Address: Operational Base + offset (0x0280)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:2 | RO | 0x0000 | reserved |
| 1:0 | RW | 0x0 | clk_lpll_mode<br>clk_lpll_mux clock mux.<br>2'b00: xin_osc0_func<br>2'b01: clk_lpll<br>2'b10: clk_deepslow |

**DSUCRU_CLKSEL_CON00**

Address: Operational Base + offset (0x0300)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13:12 | RW | 0x2 | sclk_dsu_df_src_sel<br>sclk_dsu_df_src clock mux.<br>2'b00: clk_b0pll_mux<br>2'b01: clk_b1pll_mux<br>2'b10: clk_lpll_mux<br>2'b11: clk_gpll_mux |
| 11:7 | RW | 0x00 | sclk_dsu_df_src_div<br>Divide sclk_dsu_df_src by (div_con + 1). |
| 6:0 | RO | 0x00 | reserved |

**DSUCRU_CLKSEL_CON01**

Address: Operational Base + offset (0x0304)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RW | 0x02 | aclk_mp_dsu_div<br>Divide aclk_mp_dsu by (div_con + 1). |
| 10:6 | RW | 0x02 | aclks_dsu_div<br>Divide aclks_dsu by (div_con + 1). |
| 5:1 | RW | 0x01 | aclkm_dsu_div<br>Divide aclkm_dsu by (div_con + 1). |
| 0 | RW | 0x0 | sclk_dsu_src_t_sel<br>sclk_dsu_src_t clock mux.<br>1'b0: sclk_dsu_src<br>1'b1: clk_dsu_pvtpll_t |

**DSUCRU_CLKSEL_CON02**

Address: Operational Base + offset (0x0308)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:10 | RW | 0x02 | tsclk_dsu_div<br>Divide tsclk_dsu by (div_con + 1). |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9:5 | RW | 0x02 | cntclk_dsu_div<br>Divide cntclk_dsu by (div_con + 1). |
| 4:0 | RW | 0x03 | periphclk_dsu_div<br>Divide periphclk_dsu by (div_con + 1). |

**DSUCRU_CLKSEL_CON03**

Address: Operational Base + offset (0x030C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9:5 | RW | 0x03 | gicclk_dsu_t_div<br>Divide gicclk_dsu_t by (div_con + 1). |
| 4:0 | RW | 0x03 | atclk_dsu_div<br>Divide atclk_dsu by (div_con + 1). |

**DSUCRU_CLKSEL_CON04**

Address: Operational Base + offset (0x0310)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12:11 | RW | 0x0 | pclk_dsu_s_root_sel<br>pclk_dsu_s_root clock mux.<br>2'b00: clk_matrix_100m_src<br>2'b01: clk_matrix_50m_src<br>2'b10: xin_osc0_func |
| 10 | RW | 0x1 | refclk_dsu_pvtpll_sel<br>refclk_dsu_pvtpll clock mux.<br>1'b0: sclk_dsu_src<br>1'b1: xin_osc0_func |
| 9 | RW | 0x1 | refclk_litcore_pvtpll_sel<br>refclk_litcore_pvtpll clock mux.<br>1'b0: clk_core_l<br>1'b1: xin_osc0_func |
| 8:7 | RW | 0x0 | pclk_dsu_ns_root_sel<br>pclk_dsu_ns_root clock mux.<br>2'b00: clk_matrix_100m_src<br>2'b01: clk_matrix_50m_src<br>2'b10: xin_osc0_func |
| 6:5 | RW | 0x2 | pclk_dsu_root_sel<br>pclk_dsu_root clock mux.<br>2'b00: clk_b0pll_mux<br>2'b01: clk_b1pll_mux<br>2'b10: clk_lpll_mux<br>2'b11: clk_gpll_mux |
| 4:0 | RW | 0x03 | pclk_dsu_root_div<br>Divide pclk_dsu_root by (div_con + 1). |

**DSUCRU_CLKSEL_CON05**

Address: Operational Base + offset (0x0314)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | clk_core_l_src_sel<br>clk_core_l_src clock mux.<br>2'b00: clk_core_l_slow_src<br>2'b01: clk_core_l_gpll_src<br>2'b10: clk_lpll |
| 13:9 | RW | 0x01 | clk_core_l_gpll_src_div<br>Divide clk_core_l_gpll_src by (div_con + 1). |
| 8 | RW | 0x0 | clk_core_l_slow_src_sel<br>clk_core_l_slow_src clock mux.<br>1'b0: xin_osc0_func<br>1'b1: clk_deepslow |
| 7:6 | RW | 0x0 | clk_testout_l_sel<br>clk_testout_l clock mux.<br>2'b00: clk_lpll<br>2'b01: clk_core_l_pvtpll<br>2'b10: sclk_dsu_src<br>2'b11: clk_dsu_pvtpll |
| 5:0 | RW | 0x3f | clk_testout_l_div<br>Divide clk_testout_l by (div_con + 1). |

**DSUCRU_CLKSEL_CON06**

Address: Operational Base + offset (0x0318)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13:12 | RW | 0x0 | clk_core_l1_sel<br>clk_core_l1 clock mux.<br>2'b00: clk_core_l1_uc<br>2'b01: clk_core_l1_clean<br>2'b10: clk_core_l_pvtpll_t |
| 11:7 | RW | 0x01 | clk_core_l1_uc_div<br>Divide clk_core_l1_uc by (div_con + 1). |
| 6:5 | RW | 0x0 | clk_core_l0_sel<br>clk_core_l0 clock mux.<br>2'b00: clk_core_l0_uc<br>2'b01: clk_core_l0_clean<br>2'b10: clk_core_l_pvtpll_t |
| 4:0 | RW | 0x01 | clk_core_l0_uc_div<br>Divide clk_core_l0_uc by (div_con + 1). |

**DSUCRU_CLKSEL_CON07**

Address: Operational Base + offset (0x031C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x0 | clk_dsu_pvtpll_t_sel<br>clk_dsu_pvtpll_t clock mux.<br>1'b0: clk_deepslow<br>1'b1: clk_dsu_pvtpll |
| 14 | RW | 0x0 | clk_core_l_pvtpll_t_sel<br>clk_core_l_pvtpll_t clock mux.<br>1'b0: clk_deepslow<br>1'b1: clk_core_l_pvtpll |
| 13:12 | RW | 0x0 | clk_core_l3_sel<br>clk_core_l3 clock mux.<br>2'b00: clk_core_l3_uc<br>2'b01: clk_core_l3_clean<br>2'b10: clk_core_l_pvtpll_t |
| 11:7 | RW | 0x01 | clk_core_l3_uc_div<br>Divide clk_core_l3_uc by (div_con + 1). |
| 6:5 | RW | 0x0 | clk_core_l2_sel<br>clk_core_l2 clock mux.<br>2'b00: clk_core_l2_uc<br>2'b01: clk_core_l2_clean<br>2'b10: clk_core_l_pvtpll_t |
| 4:0 | RW | 0x01 | clk_core_l2_uc_div<br>Divide clk_core_l2_uc by (div_con + 1). |

**DSUCRU_GATE_CON00**

Address: Operational Base + offset (0x0800)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | tsclk_dsu_en<br>tsclk_dsu clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | cntclk_dsu_en<br>cntclk_dsu clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | periphclk_dsu_en<br>periphclk_dsu clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | aclk_mp_dsu_en<br>aclk_mp_dsu clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | aclk_s_dsu_biu_en<br>aclk_s_dsu_biu clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | aclk_m_dsu_biu_en<br>aclk_m_dsu_biu clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | aclks_dsu_en<br>aclks_dsu clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | aclkm_dsu_en<br>aclkm_dsu clock gating control.<br>When high, disable clock |
| 7 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | sclk_dsu_en<br>sclk_dsu clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | sclk_dsu_src_t_en<br>sclk_dsu_src_t clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | sclk_dsu_src_en<br>sclk_dsu_src clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | sclk_dsu_np5_div2_src_en<br>sclk_dsu_np5_div2_src clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | sclk_dsu_np5_src_en<br>sclk_dsu_np5_src clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | sclk_dsu_df_div2_src_en<br>sclk_dsu_df_div2_src clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | sclk_dsu_df_src_en<br>sclk_dsu_df_src clock gating control.<br>When high, disable clock |

**DSUCRU_GATE_CON01**

Address: Operational Base + offset (0x0804)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | refclk_dsu_pvtpll_en<br>refclk_dsu_pvtpll clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | refclk_litcore_pvtpll_en<br>refclk_litcore_pvtpll clock gating control.<br>When high, disable clock |
| 13:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | pclk_dsu_grf_en<br>pclk_dsu_grf clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | pclk_m_daplite_biu_en<br>pclk_m_daplite_biu clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | pclk_m_daplite_en<br>pclk_m_daplite clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | pclk_s_daplite_en<br>pclk_s_daplite clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | pclk_dbg_en<br>pclk_dbg clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | pclk_dsu_en<br>pclk_dsu clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | pclk_dsu_biu_en<br>pclk_dsu_biu clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_dsu_ns_root_en<br>pclk_dsu_ns_root clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_dsu_root_en<br>pclk_dsu_root clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | aclk_adb_dsu_en<br>aclk_adb_dsu clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | gicclk_dsu_t_en<br>gicclk_dsu_t clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | atclk_dsu_en<br>atclk_dsu clock gating control.<br>When high, disable clock |

**DSUCRU_GATE_CON02**

Address: Operational Base + offset (0x0808)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | clk_core_l_div2_src_en<br>clk_core_l_div2_src clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | clk_core_l3_clean_en<br>clk_core_l3_clean clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | clk_core_l2_clean_en<br>clk_core_l2_clean clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | clk_core_l1_clean_en<br>clk_core_l1_clean clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | clk_core_l0_clean_en<br>clk_core_l0_clean clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | clk_24m_litcore_cpuboost_en<br>clk_24m_litcore_cpuboost clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | pclk_litcore_cpuboost_en<br>pclk_litcore_cpuboost clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | pclk_dsu_cru_en<br>pclk_dsu_cru clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | pclk_litcore_grf_en<br>pclk_litcore_grf clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | pclk_litcore_pvtm_en<br>pclk_litcore_pvtm clock gating control.<br>When high, disable clock |
| 5 | RW | 0x1 | clk_testout_l_en<br>clk_testout_l clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_dsu_sgrf_en<br>pclk_dsu_sgrf clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_dsu_s_biu_en<br>pclk_dsu_s_biu clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | pclk_dsu_s_root_en<br>pclk_dsu_s_root clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_core_litcore_pvtm_en<br>clk_core_litcore_pvtm clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | clk_litcore_pvtm_en<br>clk_litcore_pvtm clock gating control.<br>When high, disable clock |

**DSUCRU_GATE_CON03**

Address: Operational Base + offset (0x080C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | gicclk_dsu_en<br>gicclk_dsu clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | aclk_mp_dsu_biu_en<br>aclk_mp_dsu_biu clock gating control.<br>When high, disable clock |
| 12:11 | RO | 0x0 | reserved |
| 10 | RW | 0x0 | clk_core_l3_uc_en<br>clk_core_l3_uc clock gating control.<br>When high, disable clock |
| 9:8 | RO | 0x0 | reserved |
| 7 | RW | 0x0 | clk_core_l2_uc_en<br>clk_core_l2_uc clock gating control.<br>When high, disable clock |
| 6:5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | clk_core_l1_uc_en<br>clk_core_l1_uc clock gating control.<br>When high, disable clock |
| 3:2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | clk_core_l0_uc_en<br>clk_core_l0_uc clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | clk_core_l_en<br>clk_core_l clock gating control.<br>When high, disable clock |

Rockchip Confidencial

**DSUCRU_SOFTRST_CON00**

Address: Operational Base + offset (0x0A00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | nperiphreset_dsu<br>When high, reset relative logic |
| 12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | aresetn_s_dsu_biu<br>When high, reset relative logic |
| 10 | RW | 0x0 | aresetn_m_dsu_biu<br>When high, reset relative logic |
| 9:8 | RO | 0x0 | reserved |
| 7 | RW | 0x0 | nsreset_dsu<br>When high, reset relative logic |
| 6 | RW | 0x0 | nsporeset_dsu<br>When high, reset relative logic |
| 5:0 | RO | 0x00 | reserved |

**DSUCRU_SOFTRST_CON01**

Address: Operational Base + offset (0x0A04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | resetn_dsu_pvtpll<br>When high, reset relative logic |
| 14 | RW | 0x0 | resetn_litcore_pvtpll<br>When high, reset relative logic |
| 13 | RW | 0x0 | ntreset_jtag<br>When high, reset relative logic |
| 12 | RW | 0x0 | poresetn_jtag<br>When high, reset relative logic |
| 11 | RW | 0x0 | presetn_dsu_grf<br>When high, reset relative logic |
| 10 | RW | 0x0 | presetn_m_daplite_biu<br>When high, reset relative logic |
| 9 | RW | 0x0 | presetn_m_daplite<br>When high, reset relative logic |
| 8 | RW | 0x0 | presetn_s_daplite<br>When high, reset relative logic |
| 7 | RW | 0x0 | presetn_dbg<br>When high, reset relative logic |
| 6 | RW | 0x0 | npreset_dsu<br>When high, reset relative logic |
| 5 | RW | 0x0 | presetn_dsu_biu<br>When high, reset relative logic |
| 4:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | aresetn_adb_dsu<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | natreset_dsu<br>When high, reset relative logic |

**DSUCRU_SOFTRST_CON02**

Address: Operational Base + offset (0x0A08)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | resetn_24m_litcore_cpuboost<br>When high, reset relative logic |
| 9 | RW | 0x0 | presetn_litcore_cpuboost<br>When high, reset relative logic |
| 8 | RW | 0x0 | presetn_dsu_cru<br>When high, reset relative logic |
| 7 | RW | 0x0 | presetn_litcore_grf<br>When high, reset relative logic |
| 6 | RW | 0x0 | presetn_litcore_pvtm<br>When high, reset relative logic |
| 5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | presetn_dsu_sgrf<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_dsu_s_biu<br>When high, reset relative logic |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | resetn_litcore_pvtm<br>When high, reset relative logic |

**DSUCRU_SOFTRST_CON03**

Address: Operational Base + offset (0x0A0C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | ngicreset_dsu<br>When high, reset relative logic |
| 13 | RW | 0x0 | aresetn_mp_dsu_biu<br>When high, reset relative logic |
| 12 | RW | 0x0 | ncorereset_l3<br>When high, reset relative logic |
| 11 | RW | 0x0 | ncpuporeset_l3<br>When high, reset relative logic |
| 10 | RO | 0x0 | reserved |
| 9 | RW | 0x0 | ncorereset_l2<br>When high, reset relative logic |
| 8 | RW | 0x0 | ncpuporeset_l2<br>When high, reset relative logic |
| 7 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | ncorereset_l1<br>When high, reset relative logic |
| 5 | RW | 0x0 | ncpuporeset_l1<br>When high, reset relative logic |
| 4 | RO | 0x0 | reserved |
| 3 | RW | 0x0 | ncorereset_l0<br>When high, reset relative logic |
| 2 | RW | 0x0 | ncpuporeset_l0<br>When high, reset relative logic |
| 1:0 | RO | 0x0 | reserved |

**DSUCRU_AUTOCS_ACLK_M_DSU_BIU_CON0**

Address: Operational Base + offset (0x0D00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_m_dsu_biu_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_m_dsu_biu_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**DSUCRU_AUTOCS_ACLK_M_DSU_BIU_CON1**

Address: Operational Base + offset (0x0D04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_m_dsu_biu_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_m_dsu_biu_switch_en<br>switch_en<br>1'b1: Enable aclk_m_dsu_biu switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_m_dsu_biu_autocs_en<br>autocs_en<br>1'b1: Enable aclk_m_dsu_biu switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_m_dsu_biu_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_m_dsu_biu switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**DSUCRU_AUTOCS_ACLK_S_DSU_BIU_CON0**

Address: Operational Base + offset (0x0D08)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_s_dsu_biu_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0004 | aclk_s_dsu_biu_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**DSUCRU_AUTOCS_ACLK_S_DSU_BIU_CON1**

Address: Operational Base + offset (0x0D0C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_s_dsu_biu_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_s_dsu_biu_switch_en<br>switch_en<br>1'b1: Enable aclk_s_dsu_biu switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_s_dsu_biu_autocs_en<br>autocs_en<br>1'b1: Enable aclk_s_dsu_biu switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_s_dsu_biu_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_s_dsu_biu switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**DSUCRU_AUTOCS_ACLK_MP_DSU_BIU_CON0**

Address: Operational Base + offset (0x0D10)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_mp_dsu_biu_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_mp_dsu_biu_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**DSUCRU_AUTOCS_ACLK_MP_DSU_BIU_CON1**

Address: Operational Base + offset (0x0D14)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_mp_dsu_biu_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | aclk_mp_dsu_biu_switch_en<br>switch_en<br>1'b1: Enable aclk_mp_dsu_biu switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_mp_dsu_biu_autocs_en<br>autocs_en<br>1'b1: Enable aclk_mp_dsu_biu switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_mp_dsu_biu_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_mp_dsu_biu switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**DSUCRU_AUTOCS_SCLK_DSU_SRC_CON0**

Address: Operational Base + offset (0x0D18)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | sclk_dsu_src_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | sclk_dsu_src_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**DSUCRU_AUTOCS_SCLK_DSU_SRC_CON1**

Address: Operational Base + offset (0x0D1C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | sclk_dsu_src_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | sclk_dsu_src_switch_en<br>switch_en<br>1'b1: Enable sclk_dsu_src switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | sclk_dsu_src_autocs_en<br>autocs_en<br>1'b1: Enable sclk_dsu_src switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | sclk_dsu_src_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable sclk_dsu_src switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**DSUCRU_AUTOCS_CLK_CORE_L_CON0**

Address: Operational Base + offset (0x0D20)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | clk_core_l_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | clk_core_l_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**DSUCRU_AUTOCS_CLK_CORE_L_CON1**

Address: Operational Base + offset (0x0D24)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | clk_core_l_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | clk_core_l_switch_en<br>switch_en<br>1'b1: Enable clk_core_l switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | clk_core_l_autocs_en<br>autocs_en<br>1'b1: Enable clk_core_l switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | clk_core_l_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable clk_core_l switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**DSUCRU_QCHANNEL_CON00**

Address: Operational Base + offset (0x0F00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | pclk_dbg_qc_gate_en<br>qc_gate_en<br>1'b1: Enable pclk_dbg qchannel gate function.<br>1'b1: Disable pclk_dbg qchannel gate function. |
| 10 | RW | 0x0 | pclk_dbg_qc_en<br>qc_en<br>1'b1: Enable pclk_dbg qchannel.<br>1'b1: Disable pclk_dbg qchannel. |
| 9 | RW | 0x0 | pclk_dsu_qc_gate_en<br>qc_gate_en<br>1'b1: Enable pclk_dsu qchannel gate function.<br>1'b1: Disable pclk_dsu qchannel gate function. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | pclk_dsu_qc_en<br>qc_en<br>1'b1: Enable pclk_dsu qchannel.<br>1'b1: Disable pclk_dsu qchannel. |
| 7 | RW | 0x0 | aclk_adb_dsu_qc_gate_en<br>qc_gate_en<br>1'b1: Enable aclk_adb_dsu qchannel gate function.<br>1'b1: Disable aclk_adb_dsu qchannel gate function. |
| 6 | RW | 0x0 | aclk_adb_dsu_qc_en<br>qc_en<br>1'b1: Enable aclk_adb_dsu qchannel.<br>1'b1: Disable aclk_adb_dsu qchannel. |
| 5 | RW | 0x0 | gicclk_dsu_qc_gate_en<br>qc_gate_en<br>1'b1: Enable gicclk_dsu qchannel gate function.<br>1'b1: Disable gicclk_dsu qchannel gate function. |
| 4 | RW | 0x0 | gicclk_dsu_qc_en<br>qc_en<br>1'b1: Enable gicclk_dsu qchannel.<br>1'b1: Disable gicclk_dsu qchannel. |
| 3 | RW | 0x0 | atclk_dsu_qc_gate_en<br>qc_gate_en<br>1'b1: Enable atclk_dsu qchannel gate function.<br>1'b1: Disable atclk_dsu qchannel gate function. |
| 2 | RW | 0x0 | atclk_dsu_qc_en<br>qc_en<br>1'b1: Enable atclk_dsu qchannel.<br>1'b1: Disable atclk_dsu qchannel. |
| 1 | RW | 0x0 | sclk_dsu_qc_gate_en<br>qc_gate_en<br>1'b1: Enable sclk_dsu qchannel gate function.<br>1'b1: Disable sclk_dsu qchannel gate function. |
| 0 | RW | 0x0 | sclk_dsu_qc_en<br>qc_en<br>1'b1: Enable sclk_dsu qchannel.<br>1'b1: Disable sclk_dsu qchannel. |

**DSUCRU_SMOTH_DIVFREE_CON00**

Address: Operational Base + offset (0x0F10)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | clk_core_l0_uc_freq_keep<br>freq_keep<br>Cycles to keep every step. |
| 15 | RW | 0x0 | clk_core_l0_uc_bypass<br>bypass<br>Division signal bypass.<br>1'b1: Bypass.<br>1'b0: Use Smoothdiv to control clock division. |
| 14 | RW | 0x0 | clk_core_l0_uc_gate_smth_en<br>gate_smth_en<br>If trigger smoothdiv function when clk been gated.<br>1'b1: Enable.<br>1'b0: Disable. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | clk_core_l0_uc_smdiv_clk_off<br>smdiv_clk_off<br>Turn off smoothdiv module clk.<br>1'b1: Turn off.<br>1'b0: Turn on. |
| 12:5 | RO | 0x00 | reserved |
| 4:0 | RW | 0x00 | clk_core_l0_uc_step<br>step<br>Step of div from 0x1f to setting configuration . |

**DSUCRU_SMOTH_DIVFREE_CON01**

Address: Operational Base + offset (0x0F14)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | clk_core_l1_uc_freq_keep<br>freq_keep<br>Cycles to keep every step. |
| 15 | RW | 0x0 | clk_core_l1_uc_bypass<br>bypass<br>Division signal bypass.<br>1'b1: Bypass.<br>1'b0: Use Smoothdiv to control clock division. |
| 14 | RW | 0x0 | clk_core_l1_uc_gate_smth_en<br>gate_smth_en<br>If trigger smoothdiv function when clk been gated.<br>1'b1: Enable.<br>1'b0: Disable. |
| 13 | RW | 0x0 | clk_core_l1_uc_smdiv_clk_off<br>smdiv_clk_off<br>Turn off smoothdiv module clk.<br>1'b1: Turn off.<br>1'b0: Turn on. |
| 12:5 | RO | 0x00 | reserved |
| 4:0 | RW | 0x00 | clk_core_l1_uc_step<br>step<br>Step of div from 0x1f to setting configuration . |

**DSUCRU_SMOTH_DIVFREE_CON02**

Address: Operational Base + offset (0x0F18)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | clk_core_l2_uc_freq_keep<br>freq_keep<br>Cycles to keep every step. |
| 15 | RW | 0x0 | clk_core_l2_uc_bypass<br>bypass<br>Division signal bypass.<br>1'b1: Bypass.<br>1'b0: Use Smoothdiv to control clock division. |
| 14 | RW | 0x0 | clk_core_l2_uc_gate_smth_en<br>gate_smth_en<br>If trigger smoothdiv function when clk been gated.<br>1'b1: Enable.<br>1'b0: Disable. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | clk_core_l2_uc_smdiv_clk_off<br>smdiv_clk_off<br>Turn off smoothdiv module clk.<br>1'b1: Turn off.<br>1'b0: Turn on. |
| 12:5 | RO | 0x00 | reserved |
| 4:0 | RW | 0x00 | clk_core_l2_uc_step<br>step<br>Step of div from 0x1f to setting configuration . |

**DSUCRU_SMOTH_DIVFREE_CON03**

Address: Operational Base + offset (0x0F1C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | clk_core_l3_uc_freq_keep<br>freq_keep<br>Cycles to keep every step. |
| 15 | RW | 0x0 | clk_core_l3_uc_bypass<br>bypass<br>Division signal bypass.<br>1'b1: Bypass.<br>1'b0: Use Smoothdiv to control clock division. |
| 14 | RW | 0x0 | clk_core_l3_uc_gate_smth_en<br>gate_smth_en<br>If trigger smoothdiv function when clk been gated.<br>1'b1: Enable.<br>1'b0: Disable. |
| 13 | RW | 0x0 | clk_core_l3_uc_smdiv_clk_off<br>smdiv_clk_off<br>Turn off smoothdiv module clk.<br>1'b1: Turn off.<br>1'b0: Turn on. |
| 12:5 | RO | 0x00 | reserved |
| 4:0 | RW | 0x00 | clk_core_l3_uc_step<br>step<br>Step of div from 0x1f to setting configuration . |

# 2.12 PHPTOPCRU Register Description

## 2.12.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PHPTOPCRU_PPLL_CON0 | 0x0200 | W | 0x00000000 | PPLL configuration register 0 |
| PHPTOPCRU_PPLL_CON1 | 0x0204 | W | 0x00000000 | PPLL configuration register 1 |
| PHPTOPCRU_PPLL_CON2 | 0x0208 | W | 0x00000000 | PPLL configuration register 2 |
| PHPTOPCRU_PPLL_CON3 | 0x020C | W | 0x00000000 | PPLL configuration register 3 |
| PHPTOPCRU_PPLL_CON4 | 0x0210 | W | 0x00000000 | PPLL configuration register 4 |
| PHPTOPCRU_PPLL_CON5 | 0x0214 | W | 0x00000000 | PPLL configuration register 5 |
| PHPTOPCRU_PPLL_CON6 | 0x0218 | W | 0x00000000 | PPLL configuration register 6 |
| PHPTOPCRU_GATE_CON00 | 0x0800 | W | 0x00000000 | Internal clock gate and division register 0 |
| PHPTOPCRU_SOFTRST_CON00 | 0x0A00 | W | 0x00000000 | Internal clock reset register 0 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-*

Rockchip Confidential

*Double WORD (64 bits) access*

## 2.12.2 Detail Registers Description

**PHPTOPCRU_PPLL_CON0**

Address: Operational Base + offset (0x0200)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | ppll_bp<br>BYPASS: Bypass mode control signal.<br>1'b1: bypass mode is enabled. (FOUT = FIN).<br>1'b0: PLL operates normally. |
| 14:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | ppll_m<br>M: Division value of the 10-bit programmable main-divider.<br>PLL has to be reset if M value is changed.<br>64 <= pll_m <= 1023 |

**PHPTOPCRU_PPLL_CON1**

Address: Operational Base + offset (0x0204)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | ppll_resetb<br>RESETB: Power down control signal.<br>1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time.<br>1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset. |
| 12:9 | RO | 0x0 | reserved |
| 8:6 | RW | 0x0 | ppll_s<br>Division value of the 3-bit programmable scaler.<br>0 <= pll_s <= 6 |
| 5:0 | RW | 0x00 | ppll_p<br>P: Division value of the 6-bit programmable pre-divider.<br>PLL has to be reset if P value is changed.<br>1 <= pll_p <= 63 |

**PHPTOPCRU_PPLL_CON2**

Address: Operational Base + offset (0x0208)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | ppll_k<br>K: Value of 16-bit DSM.<br>pll_k[15:0] is a two's complement integer. |

**PHPTOPCRU_PPLL_CON3**

Address: Operational Base + offset (0x020C)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | ppll_sel_pf<br>SEL_PF: Value of 2-bit modulation method control.<br>2'b00: down spread;<br>2'b01: up spread;<br>2'b1x: center spread.<br>PLL has to be reset if pll_sel_pf is changed. |
| 13:8 | RW | 0x00 | ppll_mrr<br>MRR: Value of 6-bit modulation rate control.<br>PLL has to be reset if pll_mrr is changed. |
| 7:0 | RW | 0x00 | ppll_mfr<br>MFR: Value of 8-bit modulation frequency control.<br>PLL has to be reset if pll_mfr is changed. |

**PHPTOPCRU_PPLL_CON4**

Address: Operational Base + offset (0x0210)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | ppll_fsel<br>FSEL: Monitoring pin.<br>1'b0: FEED_OUT = FREF.<br>1'b1: FEED_OUT = FEED. |
| 14 | RW | 0x0 | ppll_feed_en<br>FEED_EN: Monitoring pin.<br>1'b0: FEED_OUT is disabled.<br>1'b1: FEED_OUT is enabled. |
| 13:9 | RO | 0x00 | reserved |
| 8:4 | RW | 0x00 | ppll_extafc<br>EXTAFC: Monitoring pin.<br>If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 3 | RW | 0x0 | ppll_afc_enb<br>AFC_ENB: Monitoring pin.<br>1'b0: AFC is enabled and VCO is calibrated automatically.<br>1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | ppll_sscg_en<br>SSCG_EN: Enable pin for dithered mode.<br>1'b0: disable dithered mode.<br>1'b1: enable dithered mode. |

**PHPTOPCRU_PPLL_CON5**

Address: Operational Base + offset (0x0214)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | ppll_fout_mask<br>FOUT_MASK: Scaler's re-initialization time control pin. |

**PHPTOPCRU_PPLL_CON6**

Address: Operational Base + offset (0x0218)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | ppll_lock<br>LOCK: PLL lock flag.<br>1'b0: PLL is unlocked.<br>1'b1: PLL is locked. |
| 14:10 | RW | 0x00 | ppll_afc_code<br>AFC_CODE: Monitoring pin.<br>Output code of AFC(5 bits). |
| 9:0 | RO | 0x000 | reserved |

**PHPTOPCRU_GATE_CON00**

Address: Operational Base + offset (0x0800)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | pclk_apb2asb_slv_chip_top_en<br>pclk_apb2asb_slv_chip_top clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | pclk_pcie3_phy_en<br>pclk_pcie3_phy clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | pclk_pcie_combo_pipe_phy2_en<br>pclk_pcie_combo_pipe_phy2 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | pclk_pcie_combo_pipe_phy1_en<br>pclk_pcie_combo_pipe_phy1 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | pclk_pcie_combo_pipe_phy0_en<br>pclk_pcie_combo_pipe_phy0 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_pcie_combo_pipe_grf2_en<br>pclk_pcie_combo_pipe_grf2 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_pcie_combo_pipe_grf1_en<br>pclk_pcie_combo_pipe_grf1 clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | pclk_pcie_combo_pipe_grf0_en<br>pclk_pcie_combo_pipe_grf0 clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | pclk_phptop_cru_en<br>pclk_phptop_cru clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RO | 0x0 | reserved |

**PHPTOPCRU_SOFTRST_CON00**

Address: Operational Base + offset (0x0A00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | resetn_pcie3_phy<br>When high, reset relative logic |
| 9 | RW | 0x0 | presetn_apb2asb_slv_chip_top<br>When high, reset relative logic |
| 8 | RW | 0x0 | presetn_pcie3_phy<br>When high, reset relative logic |
| 7 | RW | 0x0 | presetn_pcie_combo_pipe_phy2<br>When high, reset relative logic |
| 6 | RW | 0x0 | presetn_pcie_combo_pipe_phy1<br>When high, reset relative logic |
| 5 | RW | 0x0 | presetn_pcie_combo_pipe_phy0<br>When high, reset relative logic |
| 4 | RW | 0x0 | presetn_pcie_combo_pipe_grf2<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_pcie_combo_pipe_grf1<br>When high, reset relative logic |
| 2 | RW | 0x0 | presetn_pcie_combo_pipe_grf0<br>When high, reset relative logic |
| 1 | RW | 0x0 | presetn_phptop_cru<br>When high, reset relative logic |
| 0 | RO | 0x0 | reserved |

# 2.13 SBUSCRU Register Description

## 2.13.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| SBUSCRU_SPLL_CON0 | 0x0220 | W | 0x00000000 | SPLL configuration register 0 |
| SBUSCRU_SPLL_CON1 | 0x0224 | W | 0x00000000 | SPLL configuration register 1 |
| SBUSCRU_SPLL_CON4 | 0x0230 | W | 0x00000002 | SPLL configuration register 4 |
| SBUSCRU_SPLL_CON5 | 0x0234 | W | 0x000007E0 | SPLL configuration register 5 |
| SBUSCRU_SPLL_CON6 | 0x0238 | W | 0x00000000 | SPLL configuration register 6 |
| SBUSCRU_MODE_CON00 | 0x0280 | W | 0x00000000 | Internal PLL mode select register 0 |
| SBUSCRU_CLKSEL_CON00 | 0x0300 | W | 0x000000C6 | Internal clock select and division register 0 |
| SBUSCRU_GATE_CON00 | 0x0800 | W | 0x00000000 | Internal clock gate and division register 0 |
| SBUSCRU_SOFTRST_CON00 | 0x0A00 | W | 0x00000000 | Internal clock reset register 0 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

Rockchip Confidencial

## 2.13.2 Detail Registers Description

**SBUSCRU_SPLL_CON0**

Address: Operational Base + offset (0x0220)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | spll_bp<br>BYPASS: Bypass mode control signal.<br>1'b1: bypass mode is enabled. (FOUT = FIN).<br>1'b0: PLL operates normally. |
| 14:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | spll_m<br>M: Division value of the 10-bit programmable main-divider.<br>PLL has to be reset if M value is changed.<br>64 <= pll_m <= 1023 |

**SBUSCRU_SPLL_CON1**

Address: Operational Base + offset (0x0224)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | spll_resetb<br>RESETB: Power down control signal.<br>1'b0: RESETB=0 from 1, PLL starts its normal operation after lock time.<br>1'b1: RESETB=1, power down mode is enabled and all digital blocks are reset. |
| 12:9 | RO | 0x0 | reserved |
| 8:6 | RW | 0x0 | spll_s<br>Division value of the 3-bit programmable scaler.<br>0 <= pll_s <= 6 |
| 5:0 | RW | 0x00 | spll_p<br>P: Division value of the 6-bit programmable pre-divider.<br>PLL has to be reset if P value is changed.<br>1 <= pll_p <= 63 |

**SBUSCRU_SPLL_CON4**

Address: Operational Base + offset (0x0230)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | spll_fsel<br>FSEL: Monitoring pin.<br>1'b0: FEED_OUT = FREF.<br>1'b1: FEED_OUT = FEED. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14 | RW | 0x0 | spll_feed_en<br>FEED_EN: Monitoring pin.<br>1'b0: FEED_OUT is disabled.<br>1'b1: FEED_OUT is enabled. |
| 13:9 | RO | 0x00 | reserved |
| 8:4 | RW | 0x00 | spll_extafc<br>EXTAFC: Monitoring pin.<br>If pll_afc_enb=1, AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 3 | RW | 0x0 | spll_afc_enb<br>AFC_ENB: Monitoring pin.<br>1'b0: AFC is enabled and VCO is calibrated automatically.<br>1'b1: AFC is disabled and VCO is calibrated manually by pll_extafc[4:0] for the test of VCO range. |
| 2:1 | RW | 0x1 | spll_icp<br>Charge-pump current control signal. |
| 0 | RO | 0x0 | reserved |

**SBUSCRU_SPLL_CON5**

Address: Operational Base + offset (0x0234)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10:9 | RW | 0x3 | spll_lock_con_dly<br>LOCK_CON_DLY: Lock detector setting of the detection resolution. |
| 8:7 | RW | 0x3 | spll_lock_con_out<br>LOCK_CON_OUT: Lock detector setting of the output margin. |
| 6:5 | RW | 0x3 | spll_lock_con_in<br>LOCK_CON_IN: Lock detector setting of the input margin. |
| 4:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | spll_fout_mask<br>FOUT_MASK: Scaler's re-initialization time control pin. |

**SBUSCRU_SPLL_CON6**

Address: Operational Base + offset (0x0238)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | spll_lock<br>LOCK: PLL lock flag.<br>1'b0: PLL is unlocked.<br>1'b1: PLL is locked. |
| 14:10 | RW | 0x00 | spll_afc_code<br>AFC_CODE: Monitoring pin.<br>Output code of AFC(5 bits). |
| 9:0 | RO | 0x000 | reserved |

**SBUSCRU_MODE_CON00**

Address: Operational Base + offset (0x0280)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1:0 | RW | 0x0 | clk_spll_mode<br>clk_spll_mux clock mux.<br>2'b00: xin_osc0_func<br>2'b01: clk_spll<br>2'b10: clk_deepslow |

**SBUSCRU_CLKSEL_CON00**

Address: Operational Base + offset (0x0300)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | clk_sbus_timer_root_sel<br>clk_sbus_timer_root clock mux.<br>1'b0: xin_osc0_func<br>1'b1: clk_matrix_sbus_100m_src |
| 10 | RW | 0x0 | clk_matrix_sbus_100m_src_sel<br>clk_matrix_sbus_100m_src clock mux.<br>1'b0: clk_spll_mux<br>1'b1: clk_cpll_mux |
| 9:5 | RW | 0x06 | clk_matrix_sbus_100m_src_div<br>Divide clk_matrix_sbus_100m_src by (div_con + 1). |
| 4:0 | RW | 0x06 | pclk_sbus_root_div<br>Divide pclk_sbus_root by (div_con + 1). |

**SBUSCRU_GATE_CON00**

Address: Operational Base + offset (0x0800)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | clk_stimer11_en<br>clk_stimer11 clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | clk_stimer10_en<br>clk_stimer10 clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | clk_stimer9_en<br>clk_stimer9 clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | clk_stimer8_en<br>clk_stimer8 clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | clk_stimer7_en<br>clk_stimer7 clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RW | 0x0 | clk_stimer6_en<br>clk_stimer6 clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | clk_sbus_timer_en<br>clk_sbus_timer_root clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | pclk_stimer1_en<br>pclk_stimer1 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_matrix_sbus_100m_src_en<br>clk_matrix_sbus_100m_src clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | clk_jdbck_dap_en<br>clk_jdbck_dap clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_jdbck_dap_en<br>pclk_jdbck_dap clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_sbus_sgrf_en<br>pclk_sbus_sgrf clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | pclk_sbus_cru_en<br>pclk_sbus_cru clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | pclk_sbus_biu_en<br>pclk_sbus_biu clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | pclk_sbus_root_en<br>pclk_sbus_root clock gating control.<br>When high, disable clock |

**SBUSCRU_SOFTRST_CON00**

Address: Operational Base + offset (0x0A00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | resetn_stimer11<br>When high, reset relative logic |
| 13 | RW | 0x0 | resetn_stimer10<br>When high, reset relative logic |
| 12 | RW | 0x0 | resetn_stimer9<br>When high, reset relative logic |
| 11 | RW | 0x0 | resetn_stimer8<br>When high, reset relative logic |
| 10 | RW | 0x0 | resetn_stimer7<br>When high, reset relative logic |
| 9 | RW | 0x0 | resetn_stimer6<br>When high, reset relative logic |
| 8 | RO | 0x0 | reserved |
| 7 | RW | 0x0 | presetn_stimer1<br>When high, reset relative logic |
| 6 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | resetn_jdbck_dap<br>When high, reset relative logic |
| 4 | RW | 0x0 | presetn_jdbck_dap<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_sbus_sgrf<br>When high, reset relative logic |
| 2 | RW | 0x0 | presetn_sbus_cru<br>When high, reset relative logic |
| 1 | RW | 0x0 | presetn_sbus_biu<br>When high, reset relative logic |
| 0 | RO | 0x0 | reserved |

# 2.14 SECURECRU Register Description

## 2.14.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| SECURECRU_CLKSEL_CON00 | 0x0300 | W | 0x0000144B | Internal clock select and division register 0 |
| SECURECRU_CLKSEL_CON01 | 0x0304 | W | 0x00000000 | Internal clock select and division register 1 |
| SECURECRU_CLKSEL_CON02 | 0x0308 | W | 0x00000000 | Internal clock select and division register 2 |
| SECURECRU_CLKSEL_CON03 | 0x030C | W | 0x000000C5 | Internal clock select and division register 3 |
| SECURECRU_GATE_CON00 | 0x0800 | W | 0x00000000 | Internal clock gate and division register 0 |
| SECURECRU_GATE_CON01 | 0x0804 | W | 0x00000000 | Internal clock gate and division register 1 |
| SECURECRU_GATE_CON02 | 0x0808 | W | 0x00000000 | Internal clock gate and division register 2 |
| SECURECRU_GATE_CON03 | 0x080C | W | 0x00000000 | Internal clock gate and division register 3 |
| SECURECRU_SOFTRST_CON00 | 0x0A00 | W | 0x00000000 | Internal clock reset register 0 |
| SECURECRU_SOFTRST_CON01 | 0x0A04 | W | 0x00000000 | Internal clock reset register 1 |
| SECURECRU_SOFTRST_CON02 | 0x0A08 | W | 0x00000000 | Internal clock reset register 2 |
| SECURECRU_SOFTRST_CON03 | 0x0A0C | W | 0x00000000 | Internal clock reset register 3 |
| SECURECRU_AUTOCS_ACLK_SECURE_NS_ROOT_CON0 | 0x0D00 | W | 0x00200004 | Auto clock switch control register 0 |
| SECURECRU_AUTOCS_ACLK_SECURE_NS_ROOT_CON1 | 0x0D04 | W | 0x00000000 | Auto clock switch control register 1 |
| SECURECRU_AUTOCS_HCLK_SECURE_NS_ROOT_CON0 | 0x0D08 | W | 0x00200004 | Auto clock switch control register 0 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| SECURECRU_AUTOCS_HCLK_SECURE_NS_ROOT_CON1 | 0x0D0C | W | 0x00000000 | Auto clock switch control register 1 |
| SECURECRU_AUTOCS_ACLK_SECURE_S_ROOT_CON0 | 0x0D10 | W | 0x00200004 | Auto clock switch control register 0 |
| SECURECRU_AUTOCS_ACLK_SECURE_S_ROOT_CON1 | 0x0D14 | W | 0x00000000 | Auto clock switch control register 1 |
| SECURECRU_AUTOCS_HCLK_SECURE_S_ROOT_CON0 | 0x0D18 | W | 0x00200004 | Auto clock switch control register 0 |
| SECURECRU_AUTOCS_HCLK_SECURE_S_ROOT_CON1 | 0x0D1C | W | 0x00000000 | Auto clock switch control register 1 |
| SECURECRU_AUTOCS_PCLK_SECURE_S_ROOT_CON0 | 0x0D20 | W | 0x00200004 | Auto clock switch control register 0 |
| SECURECRU_AUTOCS_PCLK_SECURE_S_ROOT_CON1 | 0x0D24 | W | 0x00000000 | Auto clock switch control register 1 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 2.14.2 Detail Registers Description

**SECURECRU_CLKSEL_CON00**

Address: Operational Base + offset (0x0300)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x1 | clk_matrix_sec_350m_src_div<br>Divide clk_matrix_sec_350m_src by (div_con + 1). |
| 11:9 | RW | 0x2 | clk_matrix_sec_233m_src_div<br>Divide clk_matrix_sec_233m_src by (div_con + 1). |
| 8:6 | RW | 0x1 | clk_matrix_sec_175m_src_div<br>Divide clk_matrix_sec_175m_src by (div_con + 1). |
| 5:3 | RW | 0x1 | clk_matrix_sec_116m_src_div<br>Divide clk_matrix_sec_116m_src by (div_con + 1). |
| 2:0 | RW | 0x3 | clk_matrix_sec_58m_src_div<br>Divide clk_matrix_sec_58m_src by (div_con + 1). |

**SECURECRU_CLKSEL_CON01**

Address: Operational Base + offset (0x0304)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:14 | RW | 0x0 | clk_crypto_rng_sel<br>clk_crypto_rng clock mux.<br>2'b00: clk_matrix_sec_175m_src<br>2'b01: clk_matrix_sec_116m_src<br>2'b10: clk_matrix_sec_58m_src<br>2'b11: xin_osc0_func |
| 13:12 | RW | 0x0 | clk_crypto_pka_sel<br>clk_crypto_pka clock mux.<br>2'b00: clk_matrix_sec_350m_src<br>2'b01: clk_matrix_sec_233m_src<br>2'b10: clk_matrix_sec_116m_src<br>2'b11: xin_osc0_func |
| 11:10 | RW | 0x0 | clk_crypto_core_sel<br>clk_crypto_core clock mux.<br>2'b00: clk_matrix_sec_350m_src<br>2'b01: clk_matrix_sec_233m_src<br>2'b10: clk_matrix_sec_116m_src<br>2'b11: xin_osc0_func |
| 9:8 | RW | 0x0 | pclk_secure_s_root_sel<br>pclk_secure_s_root clock mux.<br>2'b00: clk_matrix_sec_116m_src<br>2'b01: clk_matrix_sec_58m_src<br>2'b10: xin_osc0_func |
| 7:6 | RW | 0x0 | hclk_secure_s_root_sel<br>hclk_secure_s_root clock mux.<br>2'b00: clk_matrix_sec_175m_src<br>2'b01: clk_matrix_sec_116m_src<br>2'b10: clk_matrix_sec_58m_src<br>2'b11: xin_osc0_func |
| 5:4 | RW | 0x0 | aclk_secure_s_root_sel<br>aclk_secure_s_root clock mux.<br>2'b00: clk_matrix_sec_350m_src<br>2'b01: clk_matrix_sec_233m_src<br>2'b10: clk_matrix_sec_116m_src<br>2'b11: xin_osc0_func |
| 3:2 | RW | 0x0 | hclk_secure_ns_root_sel<br>hclk_secure_ns_root clock mux.<br>2'b00: clk_matrix_150m_src<br>2'b01: clk_matrix_100m_src<br>2'b10: clk_matrix_50m_src<br>2'b11: xin_osc0_func |
| 1:0 | RW | 0x0 | aclk_secure_ns_root_sel<br>aclk_secure_ns_root clock mux.<br>2'b00: clk_matrix_350m_src<br>2'b01: clk_matrix_200m_src<br>2'b10: clk_matrix_100m_src<br>2'b11: xin_osc0_func |

**SECURECRU_CLKSEL_CON02**

Address: Operational Base + offset (0x0308)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | clk_stimer_root_sel<br>clk_stimer_root clock mux.<br>1'b0: xin_osc0_func<br>1'b1: clk_matrix_sec_116m_src |
| 9:8 | RW | 0x0 | clk_keyladder_rng_sel<br>clk_keyladder_rng clock mux.<br>2'b00: clk_matrix_sec_175m_src<br>2'b01: clk_matrix_sec_116m_src<br>2'b10: clk_matrix_sec_58m_src<br>2'b11: xin_osc0_func |
| 7:6 | RW | 0x0 | clk_keyladder_core_sel<br>clk_keyladder_core clock mux.<br>2'b00: clk_matrix_sec_350m_src<br>2'b01: clk_matrix_sec_233m_src<br>2'b10: clk_matrix_sec_116m_src<br>2'b11: xin_osc0_func |
| 5:4 | RW | 0x0 | clk_scrypto_rng_sel<br>clk_scrypto_rng clock mux.<br>2'b00: clk_matrix_sec_175m_src<br>2'b01: clk_matrix_sec_116m_src<br>2'b10: clk_matrix_sec_58m_src<br>2'b11: xin_osc0_func |
| 3:2 | RW | 0x0 | clk_scrypto_pka_sel<br>clk_scrypto_pka clock mux.<br>2'b00: clk_matrix_sec_350m_src<br>2'b01: clk_matrix_sec_233m_src<br>2'b10: clk_matrix_sec_116m_src<br>2'b11: xin_osc0_func |
| 1:0 | RW | 0x0 | clk_scrypto_core_sel<br>clk_scrypto_core clock mux.<br>2'b00: clk_matrix_sec_350m_src<br>2'b01: clk_matrix_sec_233m_src<br>2'b10: clk_matrix_sec_116m_src<br>2'b11: xin_osc0_func |

**SECURECRU_CLKSEL_CON03**

Address: Operational Base + offset (0x030C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13:12 | RW | 0x0 | cclk_src_sdmmc_sel<br>cclk_src_sdmmc clock mux.<br>2'b00: clk_gpll_mux<br>2'b01: clk_spll_mux<br>2'b10: xin_osc0_func |
| 11:6 | RW | 0x03 | cclk_src_sdmmc_div<br>DT50 division register.<br>Divide cclk_src_sdmmc by (div_con + 1). |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | dclk_sdmmc_buffer_sel<br>dclk_sdmmc_buffer clock mux.<br>1'b0: clk_gpll_mux<br>1'b1: clk_spll_mux |
| 4:0 | RW | 0x05 | dclk_sdmmc_buffer_div<br>Divide dclk_sdmmc_buffer by (div_con + 1). |

**SECURECRU_GATE_CON00**

Address: Operational Base + offset (0x0800)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | clk_crypto_core_en<br>clk_crypto_core clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | pclk_secure_s_biu_en<br>pclk_secure_s_biu clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | hclk_secure_s_biu_en<br>hclk_secure_s_biu clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | aclk_secure_s_biu_en<br>aclk_secure_s_biu clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | hclk_secure_ns_biu_en<br>hclk_secure_ns_biu clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | aclk_secure_ns_biu_en<br>aclk_secure_ns_biu clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | pclk_secure_s_root_en<br>pclk_secure_s_root clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | hclk_secure_s_root_en<br>hclk_secure_s_root clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | aclk_secure_s_root_en<br>aclk_secure_s_root clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | hclk_secure_ns_root_en<br>hclk_secure_ns_root clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | aclk_secure_ns_root_en<br>aclk_secure_ns_root clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | clk_matrix_sec_333m_src_en<br>clk_matrix_sec_350m_src clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | clk_matrix_sec_200m_src_en<br>clk_matrix_sec_233m_src clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | clk_matrix_sec_175m_src_en<br>clk_matrix_sec_175m_src clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_matrix_sec_100m_src_en<br>clk_matrix_sec_116m_src clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | clk_matrix_sec_50m_src_en<br>clk_matrix_sec_58m_src clock gating control.<br>When high, disable clock |

**SECURECRU_GATE_CON01**

Address: Operational Base + offset (0x0804)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pclk_wdt_s_en<br>pclk_wdt_s clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | clk_otpc_s_en<br>clk_otpc_s clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | pclk_otpc_s_en<br>pclk_otpc_s clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | hclk_keyladder_en<br>hclk_keyladder clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | aclk_keyladder_en<br>aclk_keyladder clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | clk_keyladder_rng_en<br>clk_keyladder_rng clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | clk_keyladder_core_en<br>clk_keyladder_core clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | hclk_scrypto_en<br>hclk_scrypto clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | aclk_scrypto_en<br>aclk_scrypto clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_scrypto_rng_en<br>clk_scrypto_rng clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | clk_scrypto_pka_en<br>clk_scrypto_pka clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | clk_scrypto_core_en<br>clk_scrypto_core clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | hclk_crypto_en<br>hclk_crypto clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | aclk_crypto_en<br>aclk_crypto clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_crypto_rng_en<br>clk_crypto_rng clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | clk_crypto_pka_en<br>clk_crypto_pka clock gating control.<br>When high, disable clock |

**SECURECRU_GATE_CON02**

Address: Operational Base + offset (0x0808)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | hclk_trng_s_en<br>hclk_trng_s clock gating control.<br>When high, disable clock |
| 14 | RW | 0x0 | pclk_keylad_en<br>pclk_keylad clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | pclk_scrypto_en<br>pclk_scrypto clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | clk_stimer5_en<br>clk_stimer5 clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | clk_stimer4_en<br>clk_stimer4 clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | clk_stimer3_en<br>clk_stimer3 clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | clk_stimer2_en<br>clk_stimer2 clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | clk_stimer1_en<br>clk_stimer1 clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | clk_stimer0_en<br>clk_stimer0 clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_stimer_root_en<br>clk_stimer_root clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | hclk_bootrom_ns_en<br>hclk_bootrom_ns clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | pclk_stimer0_en<br>pclk_stimer0 clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_dcf_en<br>pclk_dcf clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | aclk_dcf_en<br>aclk_dcf clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | hclk_bootrom_en<br>hclk_bootrom clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | tclk_wdt_s_en<br>tclk_wdt_s clock gating control.<br>When high, disable clock |

**SECURECRU_GATE_CON03**

Address: Operational Base + offset (0x080C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | pclk_secure_cru_en<br>pclk_secure_cru clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | clk_trng_s_en<br>clk_trng_s clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | pclk_trng_chk_en<br>pclk_trng_chk clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | cclk_src_sdmmc_en<br>cclk_src_sdmmc clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | hclk_sdmmc_buffer_en<br>hclk_sdmmc_buffer clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | hclk_sdmmc_en<br>hclk_sdmmc clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | dclk_sdmmc_buffer_en<br>dclk_sdmmc_buffer clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | hclk_trng_ns_en<br>hclk_trng_ns clock gating control.<br>When high, disable clock |

**SECURECRU_SOFTRST_CON00**

Address: Operational Base + offset (0x0A00)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | resetn_crypto_core<br>When high, reset relative logic |
| 14 | RW | 0x0 | presetn_secure_s_biu<br>When high, reset relative logic |
| 13 | RW | 0x0 | hresetn_secure_s_biu<br>When high, reset relative logic |
| 12 | RW | 0x0 | aresetn_secure_s_biu<br>When high, reset relative logic |
| 11 | RW | 0x0 | hresetn_secure_ns_biu<br>When high, reset relative logic |
| 10 | RW | 0x0 | aresetn_secure_ns_biu<br>When high, reset relative logic |
| 9:0 | RO | 0x000 | reserved |

**SECURECRU_SOFTRST_CON01**

Address: Operational Base + offset (0x0A04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | presetn_wdt_s<br>When high, reset relative logic |
| 14 | RW | 0x0 | resetn_otpc_s<br>When high, reset relative logic |
| 13 | RW | 0x0 | presetn_otpc_s<br>When high, reset relative logic |
| 12 | RW | 0x0 | hresetn_keyladder<br>When high, reset relative logic |
| 11 | RW | 0x0 | aresetn_keyladder<br>When high, reset relative logic |
| 10 | RW | 0x0 | resetn_keyladder_rng<br>When high, reset relative logic |
| 9 | RW | 0x0 | resetn_keyladder_core<br>When high, reset relative logic |
| 8 | RW | 0x0 | hresetn_scrypto<br>When high, reset relative logic |
| 7 | RW | 0x0 | aresetn_scrypto<br>When high, reset relative logic |
| 6 | RW | 0x0 | resetn_scrypto_rng<br>When high, reset relative logic |
| 5 | RW | 0x0 | resetn_scrypto_pka<br>When high, reset relative logic |
| 4 | RW | 0x0 | resetn_scrypto_core<br>When high, reset relative logic |
| 3 | RW | 0x0 | hresetn_crypto<br>When high, reset relative logic |
| 2 | RW | 0x0 | aresetn_crypto<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | resetn_crypto_rng<br>When high, reset relative logic |
| 0 | RW | 0x0 | resetn_crypto_pka<br>When high, reset relative logic |

**SECURECRU_SOFTRST_CON02**

Address: Operational Base + offset (0x0A08)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | hresetn_trng_s<br>When high, reset relative logic |
| 14 | RW | 0x0 | presetn_keylad<br>When high, reset relative logic |
| 13 | RW | 0x0 | presetn_scrypto<br>When high, reset relative logic |
| 12 | RW | 0x0 | resetn_stimer5<br>When high, reset relative logic |
| 11 | RW | 0x0 | resetn_stimer4<br>When high, reset relative logic |
| 10 | RW | 0x0 | resetn_stimer3<br>When high, reset relative logic |
| 9 | RW | 0x0 | resetn_stimer2<br>When high, reset relative logic |
| 8 | RW | 0x0 | resetn_stimer1<br>When high, reset relative logic |
| 7 | RW | 0x0 | resetn_stimer0<br>When high, reset relative logic |
| 6 | RO | 0x0 | reserved |
| 5 | RW | 0x0 | hresetn_bootrom_ns<br>When high, reset relative logic |
| 4 | RW | 0x0 | presetn_stimer0<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_dcf<br>When high, reset relative logic |
| 2 | RW | 0x0 | aresetn_dcf<br>When high, reset relative logic |
| 1 | RW | 0x0 | hresetn_bootrom<br>When high, reset relative logic |
| 0 | RW | 0x0 | tresetn_wdt_s<br>When high, reset relative logic |

**SECURECRU_SOFTRST_CON03**

Address: Operational Base + offset (0x0A0C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | presetn_secure_cru<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | resetn_trng_s<br>When high, reset relative logic |
| 5 | RW | 0x0 | presetn_trng_chk<br>When high, reset relative logic |
| 4 | RW | 0x0 | resetn_sdmmc<br>When high, reset relative logic |
| 3 | RW | 0x0 | hresetn_sdmmc_buffer<br>When high, reset relative logic |
| 2 | RW | 0x0 | hresetn_sdmmc<br>When high, reset relative logic |
| 1 | RW | 0x0 | dresetn_sdmmc_buffer<br>When high, reset relative logic |
| 0 | RW | 0x0 | hresetn_trng_ns<br>When high, reset relative logic |

**SECURECRU_AUTOCS_ACLK_SECURE_NS_ROOT_CON0**

Address: Operational Base + offset (0x0D00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_secure_ns_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_secure_ns_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**SECURECRU_AUTOCS_ACLK_SECURE_NS_ROOT_CON1**

Address: Operational Base + offset (0x0D04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | aclk_secure_ns_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_secure_ns_root_switch_en<br>switch_en<br>1'b1: Enable aclk_secure_ns_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_secure_ns_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_secure_ns_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_secure_ns_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_secure_ns_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**SECURECRU_AUTOCS_HCLK_SECURE_NS_ROOT_CON0**

Address: Operational Base + offset (0x0D08)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_secure_ns_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_secure_ns_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**SECURECRU_AUTOCS_HCLK_SECURE_NS_ROOT_CON1**

Address: Operational Base + offset (0x0D0C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | hclk_secure_ns_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_secure_ns_root_switch_en<br>switch_en<br>1'b1: Enable hclk_secure_ns_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_secure_ns_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_secure_ns_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | hclk_secure_ns_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_secure_ns_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**SECURECRU_AUTOCS_ACLK_SECURE_S_ROOT_CON0**

Address: Operational Base + offset (0x0D10)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | aclk_secure_s_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | aclk_secure_s_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**SECURECRU_AUTOCS_ACLK_SECURE_S_ROOT_CON1**

Address: Operational Base + offset (0x0D14)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:14 | RW | 0x0 | aclk_secure_s_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | aclk_secure_s_root_switch_en<br>switch_en<br>1'b1: Enable aclk_secure_s_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | aclk_secure_s_root_autocs_en<br>autocs_en<br>1'b1: Enable aclk_secure_s_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | aclk_secure_s_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable aclk_secure_s_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**SECURECRU_AUTOCS_HCLK_SECURE_S_ROOT_CON0**

Address: Operational Base + offset (0x0D18)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_secure_s_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_secure_s_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**SECURECRU_AUTOCS_HCLK_SECURE_S_ROOT_CON1**

Address: Operational Base + offset (0x0D1C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | hclk_secure_s_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_secure_s_root_switch_en<br>switch_en<br>1'b1: Enable hclk_secure_s_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_secure_s_root_autocs_en<br>autocs_en<br>1'b1: Enable hclk_secure_s_root switch to lower frequency.<br>1'b0: Disable. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:0 | RW | 0x000 | hclk_secure_s_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_secure_s_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

**SECURECRU_AUTOCS_PCLK_SECURE_S_ROOT_CON0**

Address: Operational Base + offset (0x0D20)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | pclk_secure_s_root_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | pclk_secure_s_root_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**SECURECRU_AUTOCS_PCLK_SECURE_S_ROOT_CON1**

Address: Operational Base + offset (0x0D24)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | pclk_secure_s_root_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | pclk_secure_s_root_switch_en<br>switch_en<br>1'b1: Enable pclk_secure_s_root switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | pclk_secure_s_root_autocs_en<br>autocs_en<br>1'b1: Enable pclk_secure_s_root switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | pclk_secure_s_root_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable pclk_secure_s_root switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

# 2.15 PMU1CRU Register Description

## 2.15.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PMU1CRU_CLKSEL_CON00 | 0x0300 | W | 0x000000B7 | Internal clock select and division register 0 |
| PMU1CRU_CLKSEL_CON01 | 0x0304 | W | 0x00000200 | Internal clock select and division register 1 |

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PMU1CRU_CLKSEL_CON02 | 0x0308 | W | 0x00000420 | Internal clock select and division register 2 |
| PMU1CRU_CLKSEL_CON03 | 0x030C | W | 0x00000080 | Internal clock select and division register 3 |
| PMU1CRU_CLKSEL_CON04 | 0x0310 | W | 0x001403DE | Internal clock select and division register 4 |
| PMU1CRU_CLKSEL_CON05 | 0x0314 | W | 0x00000006 | Internal clock select and division register 5 |
| PMU1CRU_CLKSEL_CON06 | 0x0318 | W | 0x03355460 | Internal clock select and division register 6 |
| PMU1CRU_CLKSEL_CON07 | 0x031C | W | 0x00000007 | Internal clock select and division register 7 |
| PMU1CRU_CLKSEL_CON08 | 0x0320 | W | 0x03355460 | Internal clock select and division register 8 |
| PMU1CRU_CLKSEL_CON09 | 0x0324 | W | 0x0000000B | Internal clock select and division register 9 |
| PMU1CRU_CLKSEL_CON12 | 0x0330 | W | 0x00000000 | Internal clock select and division register 12 |
| PMU1CRU_CLKSEL_CON14 | 0x0338 | W | 0x00000000 | Internal clock select and division register 14 |
| PMU1CRU_CLKSEL_CON15 | 0x033C | W | 0x00000000 | Internal clock select and division register 15 |
| PMU1CRU_CLKSEL_CON17 | 0x0344 | W | 0x00000000 | Internal clock select and division register 17 |
| PMU1CRU_GATE_CON00 | 0x0800 | W | 0x00000000 | Internal clock gate and division register 0 |
| PMU1CRU_GATE_CON01 | 0x0804 | W | 0x00000000 | Internal clock gate and division register 1 |
| PMU1CRU_GATE_CON02 | 0x0808 | W | 0x00000000 | Internal clock gate and division register 2 |
| PMU1CRU_GATE_CON03 | 0x080C | W | 0x00000000 | Internal clock gate and division register 3 |
| PMU1CRU_GATE_CON04 | 0x0810 | W | 0x00000000 | Internal clock gate and division register 4 |
| PMU1CRU_GATE_CON05 | 0x0814 | W | 0x00000000 | Internal clock gate and division register 5 |
| PMU1CRU_SOFTRST_CON00 | 0x0A00 | W | 0x00002000 | Internal clock reset register 0 |
| PMU1CRU_SOFTRST_CON01 | 0x0A04 | W | 0x00000000 | Internal clock reset register 1 |
| PMU1CRU_SOFTRST_CON02 | 0x0A08 | W | 0x00000000 | Internal clock reset register 2 |
| PMU1CRU_SOFTRST_CON03 | 0x0A0C | W | 0x00000000 | Internal clock reset register 3 |
| PMU1CRU_SOFTRST_CON04 | 0x0A10 | W | 0x00000000 | Internal clock reset register 4 |
| PMU1CRU_SOFTRST_CON05 | 0x0A14 | W | 0x00000000 | Internal clock reset register 5 |
| PMU1CRU_AUTOCS_HCLK_PMU_CM0_ROOT_I_CON0 | 0x0D00 | W | 0x00200004 | Auto clock switch control register 0 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PMU1CRU_AUTOCS_HCLK_PMU_CM0_ROOT_I_CON1 | 0x0D04 | W | 0x00000000 | Auto clock switch control register 1 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 2.15.2 Detail Registers Description

**PMU1CRU_CLKSEL_CON00**

Address: Operational Base + offset (0x0300)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | clk_matrix_pmu1_300m_src_sel<br>clk_matrix_pmu1_300m_src clock mux.<br>1'b0: clk_matrix_300m_src<br>1'b1: xin_osc0_func |
| 14:10 | RW | 0x00 | clk_matrix_pmu1_300m_src_div<br>Divide clk_matrix_pmu1_300m_src by (div_con + 1). |
| 9:7 | RW | 0x1 | clk_matrix_pmu1_200m_src_div<br>Divide clk_matrix_pmu1_200m_src by (div_con + 1). |
| 6:4 | RW | 0x3 | clk_matrix_pmu1_100m_src_div<br>Divide clk_matrix_pmu1_100m_src by (div_con + 1). |
| 3:0 | RW | 0x7 | clk_matrix_pmu1_50m_src_div<br>Divide clk_matrix_pmu1_50m_src by (div_con + 1). |

**PMU1CRU_CLKSEL_CON01**

Address: Operational Base + offset (0x0304)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11:10 | RW | 0x0 | hclk_pmu_cm0_root_i_sel<br>hclk_pmu_cm0_root_i clock mux.<br>2'b00: clk_matrix_pmu1_400m_src<br>2'b01: clk_matrix_pmu1_200m_src<br>2'b10: clk_matrix_pmu1_100m_src<br>2'b11: xin_osc0_func |
| 9:8 | RW | 0x2 | pclk_pmu1_root_i_sel<br>pclk_pmu1_root_i clock mux.<br>2'b00: clk_matrix_pmu1_100m_src<br>2'b01: clk_matrix_pmu1_50m_src<br>2'b10: xin_osc0_func |
| 7:6 | RW | 0x0 | hclk_pmu1_root_i_sel<br>hclk_pmu1_root_i clock mux.<br>2'b00: clk_matrix_pmu1_200m_src<br>2'b01: clk_matrix_pmu1_100m_src<br>2'b10: clk_matrix_pmu1_50m_src<br>2'b11: xin_osc0_func |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | clk_matrix_pmu1_400m_src_sel<br>clk_matrix_pmu1_400m_src clock mux.<br>1'b0: clk_matrix_400m_src<br>1'b1: xin_osc0_func |
| 4:0 | RW | 0x00 | clk_matrix_pmu1_400m_src_div<br>Divide clk_matrix_pmu1_400m_src by (div_con + 1). |

**PMU1CRU_CLKSEL_CON02**

Address: Operational Base + offset (0x0308)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10:9 | RW | 0x2 | clk_pmu1pwm_sel<br>clk_pmu1pwm clock mux.<br>2'b00: clk_matrix_pmu1_100m_src<br>2'b01: clk_matrix_pmu1_50m_src<br>2'b10: xin_osc0_func |
| 8:7 | RW | 0x0 | clk_pmu1timer_root_sel<br>clk_pmu1timer_root clock mux.<br>2'b00: xin_osc0_func<br>2'b01: clk_deepslow<br>2'b10: clk_matrix_pmu1_100m_src |
| 6 | RW | 0x0 | tclk_pmu1wdt_sel<br>tclk_pmu1wdt clock mux.<br>1'b0: xin_osc0_func<br>1'b1: clk_deepslow |
| 5 | RW | 0x1 | clk_pmu_cm0_rtc_sel<br>clk_pmu_cm0_rtc clock mux.<br>1'b0: xin_osc0_func<br>1'b1: clk_deepslow |
| 4:0 | RW | 0x00 | clk_pmu_cm0_rtc_div<br>Divide clk_pmu_cm0_rtc by (div_con + 1). |

**PMU1CRU_CLKSEL_CON03**

Address: Operational Base + offset (0x030C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11:7 | RW | 0x01 | clk_uart0_src_div<br>Divide clk_uart0_src by (div_con + 1). |
| 6 | RW | 0x0 | clk_i2c0_sel<br>clk_i2c0 clock mux.<br>1'b0: clk_matrix_pmu1_200m_src<br>1'b1: clk_matrix_pmu1_100m_src |
| 5:0 | RO | 0x00 | reserved |

**PMU1CRU_CLKSEL_CON04**

Address: Operational Base + offset (0x0310)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x001403de | clk_uart0_frac_div<br>clk_uart0_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**PMU1CRU_CLKSEL_CON05**

Address: Operational Base + offset (0x0314)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6:2 | RW | 0x01 | clk_i2s1_8ch_tx_src_div<br>Divide clk_i2s1_8ch_tx_src by (div_con + 1). |
| 1:0 | RW | 0x2 | sclk_uart0_sel<br>sclk_uart0 clock mux.<br>2'b00: clk_uart0_src<br>2'b01: clk_uart0_frac<br>2'b10: xin_osc0_func |

**PMU1CRU_CLKSEL_CON06**

Address: Operational Base + offset (0x0318)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x03355460 | clk_i2s1_8ch_tx_frac_div<br>clk_i2s1_8ch_tx_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**PMU1CRU_CLKSEL_CON07**

Address: Operational Base + offset (0x031C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6:2 | RW | 0x01 | clk_i2s1_8ch_rx_src_div<br>Divide clk_i2s1_8ch_rx_src by (div_con + 1). |
| 1:0 | RW | 0x3 | mclk_i2s1_8ch_tx_sel<br>mclk_i2s1_8ch_tx clock mux.<br>2'b00: clk_i2s1_8ch_tx_src<br>2'b01: clk_i2s1_8ch_tx_frac<br>2'b10: i2s1_mclkin<br>2'b11: xin_osc0_half |

**PMU1CRU_CLKSEL_CON08**

Address: Operational Base + offset (0x0320)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x03355460 | clk_i2s1_8ch_rx_frac_div<br>clk_i2s1_8ch_rx_frac fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**PMU1CRU_CLKSEL_CON09**

Rockchip Confidencial

Address: Operational Base + offset (0x0324)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | clk_usbdp_combo_phy0_ref_xtal_sel<br>clk_usbdp_combo_phy0_ref_xtal clock mux.<br>1'b0: xin_osc0_func<br>1'b1: clk_ppll |
| 9:5 | RW | 0x00 | clk_usbdp_combo_phy0_ref_xtal_div<br>Divide clk_usbdp_combo_phy0_ref_xtal by (div_con + 1). |
| 4 | RW | 0x0 | mclk_pdm0_sel<br>mclk_pdm0 clock mux.<br>1'b0: clk_matrix_pmu1_300m_src<br>1'b1: clk_matrix_pmu1_200m_src |
| 3:2 | RW | 0x2 | i2s1_8ch_mclkout_sel<br>i2s1_8ch_mclkout clock mux.<br>2'b00: mclk_i2s1_8ch_tx<br>2'b01: mclk_i2s1_8ch_rx<br>2'b10: xin_osc0_half |
| 1:0 | RW | 0x3 | mclk_i2s1_8ch_rx_sel<br>mclk_i2s1_8ch_rx clock mux.<br>2'b00: clk_i2s1_8ch_rx_src<br>2'b01: clk_i2s1_8ch_rx_frac<br>2'b10: i2s1_mclkin<br>2'b11: xin_osc0_half |

**PMU1CRU_CLKSEL_CON12**

Address: Operational Base + offset (0x0330)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | clk_hdptx0_ref_xtal_sel<br>clk_hdptx0_ref_xtal clock mux.<br>1'b0: xin_osc0_func<br>1'b1: clk_ppll |
| 10:6 | RW | 0x00 | clk_hdptx0_ref_xtal_div<br>Divide clk_hdptx0_ref_xtal by (div_con + 1). |
| 5:0 | RO | 0x00 | reserved |

**PMU1CRU_CLKSEL_CON14**

Address: Operational Base + offset (0x0338)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14 | RW | 0x0 | clk_otgphy_u3_0_sel<br>clk_otgphy_u3_0 clock mux.<br>1'b0: xin_osc0_func<br>1'b1: clk_ppll |
| 13:9 | RW | 0x00 | clk_otgphy_u3_0_div<br>Divide clk_otgphy_u3_0 by (div_con + 1). |
| 8:7 | RW | 0x0 | clk_ref_mipi_dcphy0_sel<br>clk_ref_mipi_dcphy0 clock mux.<br>2'b00: xin_osc0_func<br>2'b01: clk_ppll<br>2'b10: clk_spll_mux |
| 6:0 | RW | 0x00 | clk_ref_mipi_dcphy0_div<br>Divide clk_ref_mipi_dcphy0 by (div_con + 1). |

**PMU1CRU_CLKSEL_CON15**

Address: Operational Base + offset (0x033C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6:5 | RW | 0x0 | clk_cr_para_sel<br>clk_cr_para clock mux.<br>2'b00: xin_osc0_func<br>2'b01: clk_ppll<br>2'b10: clk_spll_mux |
| 4:0 | RW | 0x00 | clk_cr_para_div<br>Divide clk_cr_para by (div_con + 1). |

**PMU1CRU_CLKSEL_CON17**

Address: Operational Base + offset (0x0344)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | dbclk_gpio0_sel<br>dbclk_gpio0 clock mux.<br>1'b0: xin_osc0_func<br>1'b1: clk_deepslow |

**PMU1CRU_GATE_CON00**

Address: Operational Base + offset (0x0800)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | clk_pmu_cm0_rtc_en<br>clk_pmu_cm0_rtc clock gating control.<br>When high, disable clock |
| 14 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | fclk_pmu_cm0_core_en<br>fclk_pmu_cm0_core clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | hclk_pmu_cm0_biu_en<br>hclk_pmu_cm0_biu clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | pclk_pmu1_biu_en<br>pclk_pmu1_biu clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | hclk_pmu1_biu_en<br>hclk_pmu1_biu clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | hclk_pmu_cm0_root_en<br>hclk_pmu_cm0_root clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | hclk_pmu_cm0_root_i_en<br>hclk_pmu_cm0_root_i clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | pclk_pmu1_root_i_en<br>pclk_pmu1_root_i clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | hclk_pmu1_root_en<br>hclk_pmu1_root clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | hclk_pmu1_root_i_en<br>hclk_pmu1_root_i clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | clk_matrix_pmu1_400m_src_en<br>clk_matrix_pmu1_400m_src clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | clk_matrix_pmu1_300m_src_en<br>clk_matrix_pmu1_300m_src clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | clk_matrix_pmu1_200m_src_en<br>clk_matrix_pmu1_200m_src clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_matrix_pmu1_100m_src_en<br>clk_matrix_pmu1_100m_src clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | clk_matrix_pmu1_50m_src_en<br>clk_matrix_pmu1_50m_src clock gating control.<br>When high, disable clock |

**PMU1CRU_GATE_CON01**

Address: Operational Base + offset (0x0804)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | clk_pmu1pwm_capture_en<br>clk_pmu1pwm_capture clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | clk_pmu1pwm_en<br>clk_pmu1pwm clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | pclk_pmu1pwm_en<br>pclk_pmu1pwm clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | clk_pmu1timer1_en<br>clk_pmu1timer1 clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | clk_pmu1timer0_en<br>clk_pmu1timer0 clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | clk_pmu1timer_root_en<br>clk_pmu1timer_root clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | pclk_pmu1timer_en<br>pclk_pmu1timer clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | tclk_pmu1wdt_en<br>tclk_pmu1wdt clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | pclk_pmu1wdt_en<br>pclk_pmu1wdt clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | pclk_pmu1_ioc_en<br>pclk_pmu1_ioc clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_pmu1_grf_en<br>pclk_pmu1_grf clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | clk_pmu1_en<br>clk_pmu1 clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | pclk_pmu1_cru_en<br>pclk_pmu1_cru clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | clk_ddr_fail_safe_en<br>clk_ddr_fail_safe clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | pclk_pmu1_en<br>pclk_pmu1 clock gating control.<br>When high, disable clock |

**PMU1CRU_GATE_CON02**

Address: Operational Base + offset (0x0808)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | mclk_pdm0_en<br>mclk_pdm0 clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14 | RW | 0x0 | hclk_pdm0_en<br>hclk_pdm0 clock gating control.<br>When high, disable clock |
| 13 | RW | 0x0 | mclk_i2s1_8ch_rx_en<br>mclk_i2s1_8ch_rx clock gating control.<br>When high, disable clock |
| 12 | RW | 0x0 | clk_i2s1_8ch_frac_rx_en<br>clk_i2s1_8ch_rx_frac clock gating control.<br>When high, disable clock |
| 11 | RW | 0x0 | clk_i2s1_8ch_rx_en<br>clk_i2s1_8ch_rx_src clock gating control.<br>When high, disable clock |
| 10 | RW | 0x0 | mclk_i2s1_8ch_tx_en<br>mclk_i2s1_8ch_tx clock gating control.<br>When high, disable clock |
| 9 | RW | 0x0 | clk_i2s1_8ch_frac_tx_en<br>clk_i2s1_8ch_tx_frac clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | clk_i2s1_8ch_tx_en<br>clk_i2s1_8ch_tx_src clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | hclk_i2s1_8ch_en<br>hclk_i2s1_8ch clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | pclk_uart0_en<br>pclk_uart0 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | sclk_uart0_en<br>sclk_uart0 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | clk_uart0_frac_en<br>clk_uart0_frac clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | clk_uart0_en<br>clk_uart0_src clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | clk_i2c0_en<br>clk_i2c0 clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | pclk_i2c0_en<br>pclk_i2c0 clock gating control.<br>When high, disable clock |
| 0 | RO | 0x0 | reserved |

**PMU1CRU_GATE_CON03**

Address: Operational Base + offset (0x080C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | clk_hdptx0_ref_xtal_en<br>clk_hdptx0_ref_xtal clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10:6 | RO | 0x00 | reserved |
| 5 | RW | 0x0 | clk_usbdp_combo_phy0_ref_xtal_en<br>clk_usbdp_combo_phy0_ref_xtal clock gating control.<br>When high, disable clock |
| 4:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | hclk_vad_en<br>hclk_vad clock gating control.<br>When high, disable clock |

**PMU1CRU_GATE_CON04**

Address: Operational Base + offset (0x0810)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | clk_cr_para_en<br>clk_cr_para clock gating control.<br>When high, disable clock |
| 10:8 | RO | 0x0 | reserved |
| 7 | RW | 0x0 | clk_otgphy_u3_0_en<br>clk_otgphy_u3_0 clock gating control.<br>When high, disable clock |
| 6:4 | RO | 0x0 | reserved |
| 3 | RW | 0x0 | clk_ref_mipi_dcphy0_en<br>clk_ref_mipi_dcphy0 clock gating control.<br>When high, disable clock |
| 2:0 | RO | 0x0 | reserved |

**PMU1CRU_GATE_CON05**

Address: Operational Base + offset (0x0814)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x0 | dbclk_gpio0_en<br>dbclk_gpio0 clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | pclk_gpio0_en<br>pclk_gpio0 clock gating control.<br>When high, disable clock |
| 4 | RW | 0x0 | pclk_pmu0ioc_en<br>pclk_pmu0ioc clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_pmu0grf_en<br>pclk_pmu0grf clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | pclk_pmu0_en<br>pclk_pmu0 clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | clk_pmu0_en<br>clk_pmu0 clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | pclk_pmu0_root_en<br>pclk_pmu0_root clock gating control.<br>When high, disable clock |

**PMU1CRU_SOFTRST_CON00**

Address: Operational Base + offset (0x0A00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | tresetn_pmu1_cm0_jtag<br>When high, reset relative logic |
| 13 | RW | 0x1 | fresetn_pmu_cm0_core<br>When high, reset relative logic |
| 12 | RW | 0x0 | hresetn_pmu_cm0_biu<br>When high, reset relative logic |
| 11 | RW | 0x0 | presetn_pmu1_biu<br>When high, reset relative logic |
| 10 | RW | 0x0 | hresetn_pmu1_biu<br>When high, reset relative logic |
| 9:0 | RO | 0x000 | reserved |

**PMU1CRU_SOFTRST_CON01**

Address: Operational Base + offset (0x0A04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | resetn_pmu1pwm<br>When high, reset relative logic |
| 12 | RW | 0x0 | presetn_pmu1pwm<br>When high, reset relative logic |
| 11 | RW | 0x0 | resetn_pmu1timer1<br>When high, reset relative logic |
| 10 | RW | 0x0 | resetn_pmu1timer0<br>When high, reset relative logic |
| 9 | RO | 0x0 | reserved |
| 8 | RW | 0x0 | presetn_pmu1timer<br>When high, reset relative logic |
| 7 | RW | 0x0 | tresetn_pmu1wdt<br>When high, reset relative logic |
| 6 | RW | 0x0 | presetn_pmu1wdt<br>When high, reset relative logic |
| 5 | RW | 0x0 | presetn_pmu1_ioc<br>When high, reset relative logic |
| 4 | RW | 0x0 | presetn_pmu1_grf<br>When high, reset relative logic |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | presetn_cru_pmu1<br>When high, reset relative logic |
| 1 | RW | 0x0 | resetn_ddr_fail_safe<br>When high, reset relative logic |
| 0 | RO | 0x0 | reserved |

**PMU1CRU_SOFTRST_CON02**

Address: Operational Base + offset (0x0A08)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | resetn_pdm0<br>When high, reset relative logic |
| 14 | RW | 0x0 | hresetn_pdm0<br>When high, reset relative logic |
| 13 | RW | 0x0 | mresetn_i2s1_8ch_rx<br>When high, reset relative logic |
| 12:11 | RO | 0x0 | reserved |
| 10 | RW | 0x0 | mresetn_i2s1_8ch_tx<br>When high, reset relative logic |
| 9:8 | RO | 0x0 | reserved |
| 7 | RW | 0x0 | hresetn_i2s1_8ch<br>When high, reset relative logic |
| 6 | RW | 0x0 | presetn_uart0<br>When high, reset relative logic |
| 5 | RW | 0x0 | sresetn_uart0<br>When high, reset relative logic |
| 4:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | resetn_i2c0<br>When high, reset relative logic |
| 1 | RW | 0x0 | presetn_i2c0<br>When high, reset relative logic |
| 0 | RO | 0x0 | reserved |

**PMU1CRU_SOFTRST_CON03**

Address: Operational Base + offset (0x0A0C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | resetn_hdptx1_init<br>When high, reset relative logic |
| 14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | resetn_hdptx0_lane<br>When high, reset relative logic |
| 12 | RW | 0x0 | resetn_hdptx0_cmn<br>When high, reset relative logic |
| 11 | RW | 0x0 | resetn_hdptx0_init<br>When high, reset relative logic |
| 10:1 | RO | 0x000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | hresetn_vad<br>When high, reset relative logic |

**PMU1CRU_SOFTRST_CON04**

Address: Operational Base + offset (0x0A10)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | resetn_otgphy_u2_1<br>When high, reset relative logic |
| 9 | RW | 0x0 | resetn_otgphy_u2_0<br>When high, reset relative logic |
| 8 | RW | 0x0 | resetn_otgphy_u3_1<br>When high, reset relative logic |
| 7 | RW | 0x0 | resetn_otgphy_u3_0<br>When high, reset relative logic |
| 6 | RW | 0x0 | sresetn_mipi_dcphy1<br>When high, reset relative logic |
| 5 | RW | 0x0 | mresetn_mipi_dcphy1<br>When high, reset relative logic |
| 4 | RW | 0x0 | sresetn_mipi_dcphy0<br>When high, reset relative logic |
| 3 | RW | 0x0 | mresetn_mipi_dcphy0<br>When high, reset relative logic |
| 2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | resetn_hdptx1_lane<br>When high, reset relative logic |
| 0 | RW | 0x0 | resetn_hdptx1_cmn<br>When high, reset relative logic |

**PMU1CRU_SOFTRST_CON05**

Address: Operational Base + offset (0x0A14)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x0 | dbresetn_gpio0<br>When high, reset relative logic |
| 5 | RW | 0x0 | presetn_gpio0<br>When high, reset relative logic |
| 4 | RW | 0x0 | presetn_pmu0ioc<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_pmu0grf<br>When high, reset relative logic |
| 2:0 | RO | 0x0 | reserved |

**PMU1CRU_AUTOCS_HCLK_PMU_CM0_ROOT_I_CON0**

Address: Operational Base + offset (0x0D00)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0020 | hclk_pmu_cm0_root_i_wait_th<br>wait_th<br>Wait time threshold, measured by original clk. |
| 15:0 | RW | 0x0004 | hclk_pmu_cm0_root_i_idle_th<br>idle_th<br>Idle time threshold, measured by original clk. |

**PMU1CRU_AUTOCS_HCLK_PMU_CM0_ROOT_I_CON1**

Address: Operational Base + offset (0x0D04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x0 | hclk_pmu_cm0_root_i_clksel_cfg<br>clksel_cfg<br>Auto switch clock selection.<br>2'b00: Original clk<br>2'b01: xin_osc0_func_div<br>2'b10: clk_rtc_32k |
| 13 | RW | 0x0 | hclk_pmu_cm0_root_i_switch_en<br>switch_en<br>1'b1: Enable hclk_pmu_cm0_root_i switched to lower frequency when module is inactive.<br>1'b0: Disable auto switch function. |
| 12 | RW | 0x0 | hclk_pmu_cm0_root_i_autocs_en<br>autocs_en<br>1'b1: Enable hclk_pmu_cm0_root_i switch to lower frequency.<br>1'b0: Disable. |
| 11:0 | RW | 0x000 | hclk_pmu_cm0_root_i_autocs_ctrl<br>autocs_ctrl<br>12'hfff: Enable hclk_pmu_cm0_root_i switch to lower frequency.<br>12'h000: Disable.<br>Others: Reserved. |

# 2.16 PMU1SCRU Register Description

## 2.16.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PMU1SCRU_CLKSEL_CON00 | 0x0300 | W | 0x00000000 | Internal clock select and division register 0 |
| PMU1SCRU_CLKSEL_CON02 | 0x0308 | W | 0x0040B71B | Internal clock select and division register 2 |
| PMU1SCRU_GATE_CON00 | 0x0800 | W | 0x00000000 | Internal clock gate and division register 0 |
| PMU1SCRU_GATE_CON01 | 0x0804 | W | 0x00000000 | Internal clock gate and division register 1 |
| PMU1SCRU_SOFTRST_CON00 | 0x0A00 | W | 0x00000000 | Internal clock reset register 0 |
| PMU1SCRU_SOFTRST_CON01 | 0x0A04 | W | 0x00000000 | Internal clock reset register 1 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-*

Rockchip Confidencial

*Double WORD (64 bits) access*

## 2.16.2 Detail Registers Description

**PMU1SCRU_CLKSEL_CON00**

Address: Operational Base + offset (0x0300)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3:2 | RW | 0x0 | pclk_pmu1_s_root_i_sel<br>pclk_pmu1_s_root_i clock mux.<br>2'b00: clk_matrix_pmu1_100m_src<br>2'b01: clk_matrix_pmu1_50m_src<br>2'b10: xin_osc0_func |
| 1:0 | RW | 0x0 | hclk_pmu1_s_root_i_sel<br>hclk_pmu1_s_root_i clock mux.<br>2'b00: clk_matrix_pmu1_200m_src<br>2'b01: clk_matrix_pmu1_100m_src<br>2'b10: clk_matrix_pmu1_50m_src<br>2'b11: xin_osc0_func |

**PMU1SCRU_CLKSEL_CON02**

Address: Operational Base + offset (0x0308)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x0040b71b | xin_osc0_div_div<br>xin_osc0_div fraction division register.<br>High 16-bit for numerator<br>Low 16-bit for denominator |

**PMU1SCRU_GATE_CON00**

Address: Operational Base + offset (0x0800)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | pclk_pmu1_cru_s_en<br>pclk_pmu1_cru_s clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | pclk_pmu1_sgrf_en<br>pclk_pmu1_sgrf clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | hclk_pmu1_mem_en<br>hclk_pmu1_mem clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | pclk_pmu1_osc_chk_en<br>pclk_pmu1_osc_chk clock gating control.<br>When high, disable clock |
| 5 | RW | 0x0 | pclk_pmu1_s_biu_en<br>pclk_pmu1_s_biu clock gating control.<br>When high, disable clock |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | hclk_pmu1_s_biu_en<br>hclk_pmu1_s_biu clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_pmu1_s_root_en<br>pclk_pmu1_s_root_i clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | hclk_pmu1_s_root_en<br>hclk_pmu1_s_root clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | hclk_pmu1_s_root_i_en<br>hclk_pmu1_s_root_i clock gating control.<br>When high, disable clock |
| 0 | RO | 0x0 | reserved |

**PMU1SCRU_GATE_CON01**

Address: Operational Base + offset (0x0804)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | clk_pmu0_32k_hp_timer_en<br>clk_pmu0_32k_hp_timer clock gating control.<br>When high, disable clock |
| 8 | RW | 0x0 | clk_pmu0_hp_timer_en<br>clk_pmu0_hp_timer clock gating control.<br>When high, disable clock |
| 7 | RW | 0x0 | pclk_pmu0_hp_timer_en<br>pclk_pmu0_hp_timer clock gating control.<br>When high, disable clock |
| 6 | RW | 0x0 | pclk_pmu0_scrkeygen_en<br>pclk_pmu0_scrkeygen clock gating control.<br>When high, disable clock |
| 5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | pclk_pmu0_sgrf_en<br>pclk_pmu0_sgrf clock gating control.<br>When high, disable clock |
| 3 | RW | 0x0 | pclk_pmu0pvtm_en<br>pclk_pmu0pvtm clock gating control.<br>When high, disable clock |
| 2 | RW | 0x0 | clk_pmu0pvtm_en<br>clk_pmu0pvtm clock gating control.<br>When high, disable clock |
| 1 | RW | 0x0 | pclk_pmu0_s_root_en<br>pclk_pmu0_s_root clock gating control.<br>When high, disable clock |
| 0 | RW | 0x0 | xin_osc0_div_en<br>xin_osc0_div clock gating control.<br>When high, disable clock |

**PMU1SCRU_SOFTRST_CON00**

Address: Operational Base + offset (0x0A00)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | presetn_pmu1_cru_s<br>When high, reset relative logic |
| 8 | RW | 0x0 | presetn_pmu1_sgrf<br>When high, reset relative logic |
| 7 | RW | 0x0 | hresetn_pmu1_mem<br>When high, reset relative logic |
| 6 | RW | 0x0 | presetn_pmu1_osc_chk<br>When high, reset relative logic |
| 5 | RW | 0x0 | presetn_pmu1_s_biu<br>When high, reset relative logic |
| 4 | RW | 0x0 | hresetn_pmu1_s_biu<br>When high, reset relative logic |
| 3:0 | RO | 0x0 | reserved |

**PMU1SCRU_SOFTRST_CON01**

Address: Operational Base + offset (0x0A04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | resetn_pmu0_32k_hp_timer<br>When high, reset relative logic |
| 8 | RW | 0x0 | resetn_pmu0_hp_timer<br>When high, reset relative logic |
| 7 | RW | 0x0 | presetn_pmu0_hp_timer<br>When high, reset relative logic |
| 6 | RO | 0x0 | reserved |
| 5 | RW | 0x0 | presetn_pmu0_sgrf_remap<br>When high, reset relative logic |
| 4 | RW | 0x0 | presetn_pmu0_sgrf<br>When high, reset relative logic |
| 3 | RW | 0x0 | presetn_pmu0pvtm<br>When high, reset relative logic |
| 2 | RW | 0x0 | resetn_pmu0pvtm<br>When high, reset relative logic |
| 1:0 | RO | 0x0 | reserved |

# 2.17 Application Notes

## 2.17.1 PLL Usage

### 2.17.1.1 Start-up Operation

Set the registers (such as P[5:0], M[9:0] and so on) at time t3 after setting the power from 0V to VDD at time t2.

Set RESETB=0 before PLL starts to operate. Then set RESETB=1 at t4 to initialize PLL and to start AFC. Note that PLL generates a clock signal with the desired frequency only after Lock time has been passed.

Rockchip Confidencial

To change the P[5:0] and M[9:0], PLL must be initialized. However S[2:0] and BYPASS can be changed without the initialization of PLL. The other input pins are not allowed to be changed after PLL is locked.
To ensure that the register values and operation-mode controls are stable, the time intervals of Δt2(t4-t2) and Δt3(t4-t3) should be greater than 1μs and 1/$F_{FREF}$ respectively.

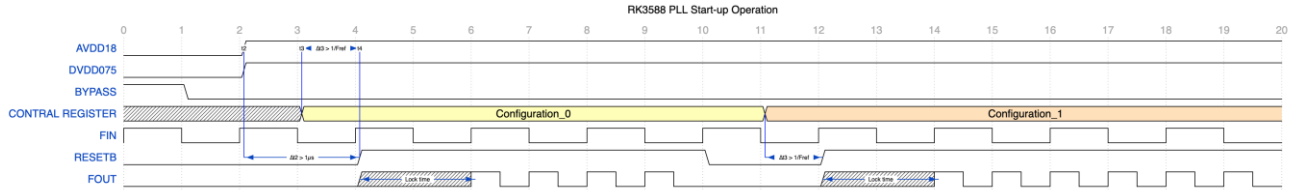



Fig. 2-6 PLL Start-up Operation

### 2.17.1.2 Bypass Operation

Bypass mode functions only when PLL is operating (RESETB=1). When ΔT > lock time (as illustrated in Fig. 2-7), PLL generates a stable clock signal with desired target frequency.

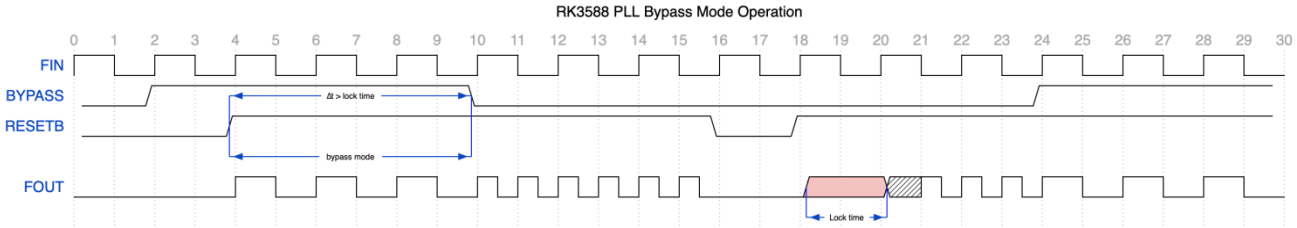



Fig. 2-7 PLL Bypass Operation

### 2.17.1.3 Glitch-free Scaler Operation

S[2:0] can be changed after PLL is locked. The timing diagram of glitch-free scaler is illustrated in figure below.
When S[2:0] or BYPASS is changed, FOUT first maintains output frequency during max. 3 cycles of FIN and then moves to logic low for 2 cycles of FIN. After completing the re-initialization time, FOUT goes to the desired frequency.
To guarantee the glitch-free functionality of scaler in PLL which needs re-initialization time for max 5 cycles of FIN, FIN has to be lower than FOUT. If FIN is higher than FOUT, set FOUT_MASK=1. Note that the maximum re-initialization time for the case of FOUT_MASK=1 takes 8 times longer than that for the case of FOUT_MASK=0.

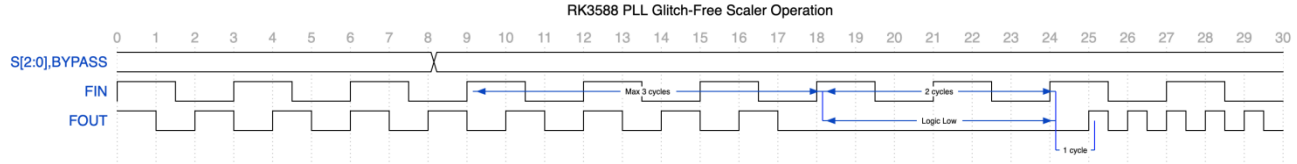



Fig. 2-8 PLL Glitch-free Scaler Operation

### 2.17.1.4 Setting Guide on P, M, S, and K

p, m, s, and k are decimal values of P[5:0], M[9:0], S[2:0], and K[15:0], respectively. (where p = P[5:0], m = M[9:0], s = S[2:0], and k = K[15:0])
FFVCO and FFOUT are calculated by the following equation.

| PLL Type | Equation |
|---|---|
| FRACPLL | FFVCO = ((m + k / 65536) * FFIN) / p<br>FFOUT = ((m + k / 65536) * FFIN) / (p * $2^s$) |
| DDRPLL | FFVCO = ((m + k / 65536) * 2 * FFIN) / p<br>FFOUT = ((m + k / 65536) * 2 * FFIN) / (p * $2^s$) |
| INTPLL | FFVCO = (m * FFIN) / p<br>FFOUT = (m * FFIN) / (p * $2^s$) |
| Parameter | 1 <= p <= 63, 64 <= m <= 1023, 0 <= s <= 6 |

P[5:0], M[9:0] and S[2:0] are unsigned integers. K[15:0] is a two's complement integer.
6'b00_0001 <= P[5:0] <= 6'b11_1111

Rockchip Confidential

10'b00_0100_0000 <= M[9:0] <= 10'b11_1111_1111
3'b000 <= S[2:0] <= 3'b110
16'b1000_0000_0000_0000 <= K[15:0] <= 16'b0111_1111_1111_1111
Setting P[5:0] or M[9:0] to all zeros is strictly prohibited while RESETB = 1. (6'b00_0000 / 10'b00_0000_0000) The division ratio of scaler is controlled by S[2:0] as summarized.

#### 2.17.1.5 Setting Guide on SSCG_EN, SEL_PF, MFR and MRR

When SSCG_EN is set to logic high, the spread spectrum mode is enabled.
sel_pf, mfr, and mrr are decimal values of SEL_PF[1:0], MFR[7:0] and MRR[5:0], respectively. (where sel_pf = SEL_PF[1:0], mfr = MFR[7:0], mrr = MRR[5:0])
Modulation frequency, MF, is determined by the following equation:
MF = FFIN / p / mfr / ($2^5$)[Hz].
Modulation rate(pk-pk), MR, is determined by the following equation:
MR = mfr * mrr / m / ($2^6$) * 100 [%].
Modulation mode is determined by sel_pf.
00: down spread, 01: up spread, 1x: center spread
Range of registers.
8'b0000_0000 <= MFR[7:0] <= 8'b1111_1111
6'b00_0001 <= MRR[5:0] <= 6'b11_1111
0 <= mrr * mfr <= 512
2'b00 <= SEL_PF[1:0] <= 2'b10

#### 2.17.1.6 Setting Guide on RESETB and BYPASS

RESETB is a reset signal of PLL. PLL enters the power down mode when RESETB = 0.
BYPASS enables the bypass mode of PLL. When BYPASS = 1, PLL enters the bypass mode and FOUT is equal to FIN.

### 2.17.2 Divider Usage

CRU supports multi-dividers for different clock requirement.

- Divider free divider
- Fractional divider
- DivfreeDT50 divider(DT50)
- DivfreeNP5 divider(NP5)

#### 2.17.2.1 DivFree Divider Usage

Frequency of this divider=clk_src/(n+1).

#### 2.17.2.2 Fractional Divider Usage

To get specific frequency, clocks of I2S, audio PWM, UART and SPDIF can be generated by fractional divider. Generally you should set that denominator 20 times larger than numerator to generate precise clock frequency. So the fractional divider applies only to generate low frequency clock.

#### 2.17.2.3 DivfreeDT50 Divider Usage

Some modules like EMMC, SDIO, SDMMC need clock of 50% duty cycle, divfree50 can generate clock of 50% duty cycle even in odd value divisor.

#### 2.17.2.4 DivFreeNP5 Divider Usage

Some modules need some special frequency can use this divider. Frequency of this divider=clk_src/((2*n+3)/2).

### 2.17.3 Global Software Reset

Two global software resets are designed in RK3588. These two software resets are self-de-asserted by hardware. Hold time of global software reset (glb_srstn_1, glb_srstn_2, wdt_rstn, tsadc_rstn) can be programed up to 1ms.

- CRU_GLB_SRST_FST_VALUE[15:0] = 0xfdb9 to assert the first global software reset glb_srstn_1
- CRU_GLB_SRST_SND_VALUE[15:0] = 0xeca8 to assert the second global software reset glb_srstn_2

Rockchip Confidencial

- glb_srstn_1 resets almost all logic except some registers just supporting hardware reset
- glb_srstn_2 resets almost all logic except GRFs and GPIOs

Reset for IP in PD_PMU can be hold if its reset_hold_enable in PMUGRF_PMU_SOC_CON1 or PMUGRF_PMU_SOC_CON2 is high even if glb_srstn_1 or glb_srstn_2 active.

Rockchip Confidencial

# Chapter 3 CPU

## 3.1 Overview

The RK3588 has a cluster with quad-core Cortex-A55 and quad-core Cortex-A76 of which the cores are all single-threaded. Cortex-A55 processor, which is a mid-range, low-power processor that implements the ARMv8-A architecture. And the Cortex-A76 core is a high-performance and low-power Arm product that implements the Armv8-A architecture.

The processor includes following features:

- Full implementation of the Armv8.2-A A64, A32, and T32 instruction sets
- Both the AArch32 and AArch64 execution states at all Exception levels (EL0 to EL3)
- In-order pipeline with direct and indirect branch prediction
- Separate L1 data and instruction side memory systems with a Memory Management Unit (MMU)
- Support for Arm TrustZone technology
- Support data engine that implements the Advanced SIMD and floating-point architecture support
- Support Cryptographic Extension
- ARMv8 debug logic
- Support Generic Interrupt Controller (GIC) CPU interface to connect to an external distributor
- Generic Timers supporting 64-bit count input from an external system counter

The configuration details are shown in following tables

Table 3-1 CPU Configuration

| | |
|---|---|
| Number of little cores(A55) | 4 |
| Number of big cores(A76) | 4 |
| L1 I cache size of A55 | 32K |
| L1 D cache size of A55 | 32K |
| L2 cache size of A55 | 128K |
| L1 I cache size of A76 | 64K |
| L1 D cache size of A76 | 64K |
| L2 cache size of A76 | 512K |
| L3 cache size | 3072K |
| L3 data RAM output latency | 3 cycles |
| L3 data RAM input latency | 2p cycles |
| CPU cache protection | No |
| DSU L3 cache protection | No |
| BUS master interface | AXI4 |
| NEON and floating-point support | Yes |
| Cryptography extension | Yes |

## 3.2 Block Diagram

The quad-core Cortex-A55 and quad-core Cortex-A76 subsystem is shown as below. As illustrated, the cores connect to system bus through DSU-L3 which can handle with CDC (clock domain crossing) issue.

The Cortex-A55 and Cortex-A76 is connected with system counter, which can run under a constant frequency clock, for PPI interrupt generation.

Rockchip Confidencial

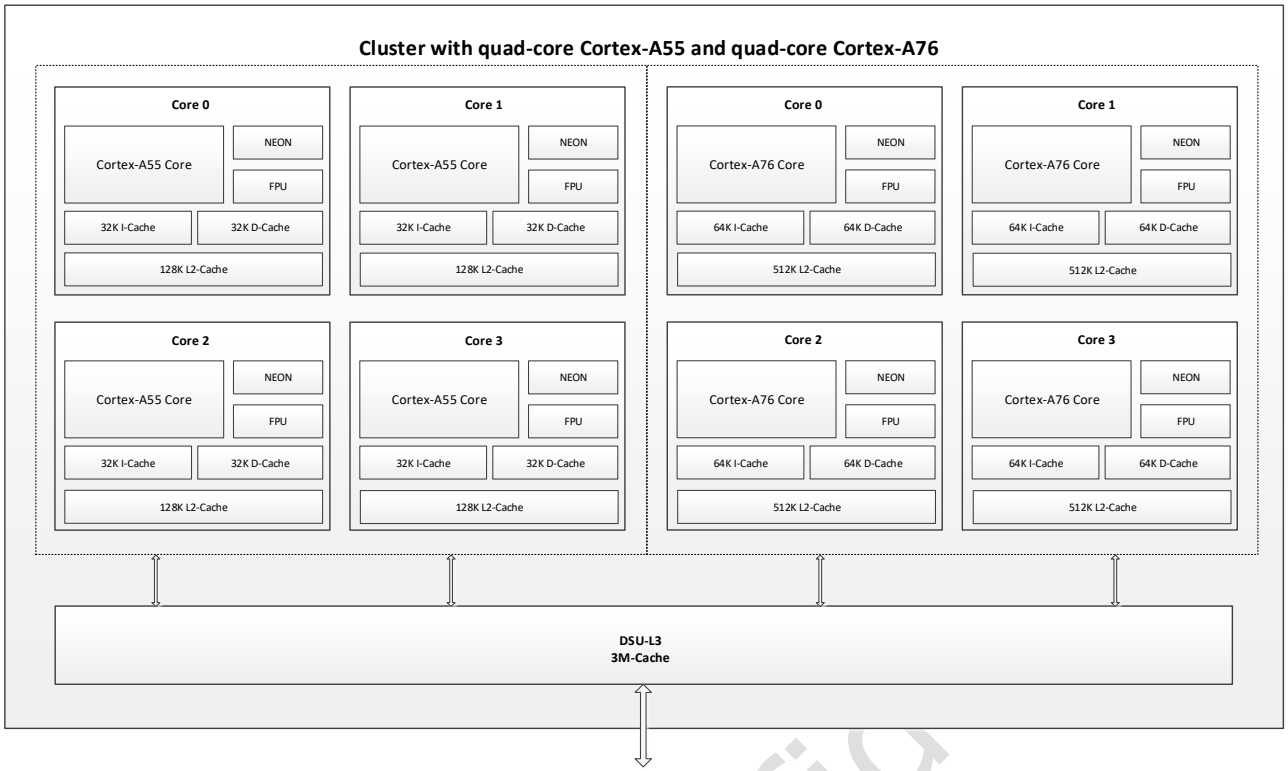



Fig. 3-1 Block Diagram

## 3.3 Function Description

Please refer to the document cortex_a55_r2p0_trm.pdf, cortex_a76_r4p0_trm.pdf and dsu_r4p1_trm.pdf for the detail function description.

Rockchip Confid

# Chapter 4 Graphics Process Unit (GPU)

## 4.1 Overview

The Mali-G610 GPU is a graphics acceleration platform that is based on open standards. It supports 2D graphics, 3D graphics, and General Purpose computing on GPU (GPGPU).

### 4.1.1 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

The Arm Mali-G610 GPU has significant features and properties.

- Support of multiple clock and voltage domains, allowing you to maximize performance within a given power budget.
- Programmable architecture.
- API feature set with support for shader-based and fixed-function graphics APIs.
- Anti-aliasing capabilities.
- Effective core for General Purpose computing on GPU (GPGPU) applications.
- High memory bandwidth and low power consumption for 3D graphics content.
- Scalability for products from smartphones to high-end mobile computing.
- Performance leading 3D graphics.
- AMBA 4 AXI-Lite slave interface for GPU configuration.
- 128-bit or 256-bit AMBA 4 ACE master interface for external memory access.
- Easy integration.
- Latency tolerance.
- Compressed texture formats.
- Configurable per-core power management for enabling the optimal power and performance combination for each application.
- Coherency aware interconnects for system memory and resource sharing.
- Arm Frame Buffer Compression (AFBC) 1.3.
- 8-bit, 10-bit, and 16-bit YUV input and output formats.
- Secure processing of DRM-protected content.
- Support Serial Wire debug for embedded MCU

### 4.1.2 Standard

The GPU hardware and software support compute standards and graphics API standards.

The GPU supports these compute API standards:

- OpenCL 2.2 Full Profile

The GPU supports these graphics API standards:

- OpenGLES 1.1, 2.0, and 3.2
- Vulkan 1.2

Rockchip Confidential

## 4.2 Block Diagram

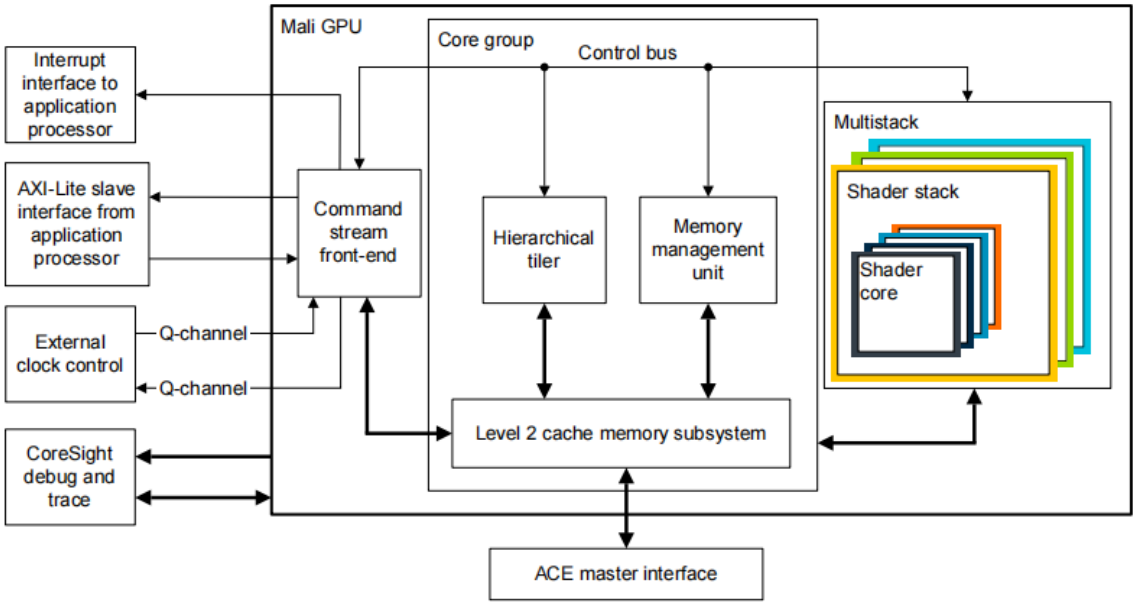



Fig. 4-1 GPU Architecture

## 4.3 Function Description

Please refer to the document "ARM_Odin_r0p0_00eac0_TechnicalReferenceManual.pdf" for the GPU detail description.

## 4.4 Register Description

Please refer to the document "ARM_Odin_r0p0_00eac0_TechnicalReferenceManual.pdf" for the GPU detail description.

## 4.5 Interface Description

There are two sets of serial debug interface for the embedded MCU. When we debug using serial wire, not only set IOMUX, but also configure the bit[11:10] of SYS_GRF_SOC_CON10 to select the GPU MCU.

Table 4-1 MCU Serial Wire Debug Interface Description

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| mcujtag_tckm0 | I | SDMMC_CMD/PDM1_CLK1_M0/MCU_JTAG_TCK_M0/CAN0_TX_M1/UART5_RX_M0/PWM7_IR_M1/GPIO4_D4_u | BUS_IOC_GPIO4D_IOMUX_SEL_H[3:0] = 4'h5 |
| mcujtag_tmsm0 | I/O | SDMMC_CLK/PDM1_CLK0_M0/TEST_CLKOUT_M0/MCU_JTAG_TMS_M0/CAN0_RX_M1/UART5_TX_M0/GPIO4_D5_d | BUS_IOC_GPIO4D_IOMUX_SEL_H[7:4] = 4'h5 |
| mcujtag_tckm1 | I | HDMI_TX0_HPD_M1/PCIE30X2_PERSTN_M2/HDMI_RX_HPDOUT_M1/MCU_JTAG_TCK_M1/UART9_RX_M2/SPI0_CS0_M3/GPIO3_D4_d | BUS_IOC_GPIO3D_IOMUX_SEL_H[3:0] = 4'h6 |
| mcujtag_tmsm1 | I/O | PCIE30X4_BUTTON_RSTN/DP1_HPDIN_M0/MCU_JTAG_TMS_M1/UART9_TX_M2/PWM11_IR_M3/SPI0_CS1_M3/GPIO3_D5_d | BUS_IOC_GPIO3D_IOMUX_SEL_H[7:4] = 4'h6 |

*Notes: I=input, O=output, I/O=input/output, bidirectional*

Rockchip Confidential

## 4.6 Application Notes

Please refer to the document "ARM_Odin_r0p0_00eac0_TechnicalReferenceManual.pdf" for the GPU detail description.

Rockchip Confidencial

# Chapter 5 VPU

## 5.1 Overview

VPU is composed by VDPU121, VDPU381, AV1, VDPU720, VEPU121(JPEG encoder only) and VEPU580 to realize the high quality video decoding and encoding.
VDPU121 can support such as H.263, MPEG1/2/4 and so on, max solution is up to 1920x1088.
VDPU381 is a multi-format video decoder which supports H265, H264, VP9 and AVS2. It also supports dual-core decoding, max solution is up 64Kx64K.
VDPU720 is JPEG decoder.
VDPU981 is AV1 decoder.
VEPU121 is JPEG encoder.
VEPU580 is H264 and H264 combo video encoder.

### 5.1.1 Feature

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

The features of VDPU121 decoder are listed as follows:
- MMU embedded with MMU interrupt support
- VP8 verision2, up to 1920x1088@60fps
- VC1 Simple Profile@low, medium, high levels, Main Profile@low, medium, high levels, Advanced Profile@level0~3,up to 1920x1088@60fps
- MPEG-4 Simple Profile@L0~6,Advanced Simple Profile@L0~5,up to 1920x1088@60fps
- MPEG-2 Main Profile, low, medium and high levels, up to 1920x1088@60fps
- MPEG-1 Main Profile, low, medium and high levels, up to 1920x1088@60fps
- H.263 Profile0, levels 10-70, up to 720x576@60fps
- JPEG Baseline interleaved, up to 8176x8176@76 milion pixels per second

The features of VDPU381 decoder are listed as follows:
- MMU embedded with MMU interrupt support
- Dual-core decoding support
- H.265 HEVC/MVC Main10 Profile yuv420@L6.1 up to 7680x4320@60fps, max solution up to 65472x65472
- H.264 AVC/MVC Main10 Profile yuv400/yuv420/yuv422/@L6.0 up to 7680x4320@30fps, max solution up to 65520x65520
- VP9 Profile0/2 yuv420@L6.1 up to 7680x4320@60fps, max solution up to 65472x65472
- AVS2 Profile0/2 yuv420@L10.2.6 up to 7680x4320@60fps, max solution up to 16383x16383

The features of VDPU720 decoder are listed as follows:
- Supports JPEG decoding
  - 48x48 to 65536x65536(4295Mpixels), Step size 8 pixels
  - Baseline interleaved, and supports ROI (region of image) decode

The features of VDPU981 decoder are listed as follows:
- MMU embedded with MMU interrupt support
- AV1 Main8/10 Profile yuv420 up to 3840x2160@60fps, max solution up to 7680x4320

The features of VEPU121 encoder are listed as follows:
- MMU embedded with MMU interrupt support
- Supports H264 encoding
- Supports JPEG encoding
  - JPEG: Baseline (DCT sequential)
  - JFIF file format 1.02
  - Non-progressive JPEG
  - Support image size from 96x32 to 8192x8192, step size 4 pixels
  - Up to 90 million pixels per second

The features of VEPU580 are listed as follows:
- HEVC Main Profile, Level 6.0 High Tier

Rockchip Confidencial

- H.264 High Profile, level 6.0
- Resolution upto 16384x8192
- Bitrate upto 800Mbps with CBR/VBR/FixQP/QPMAP bitrate control
- YUV420 and YUV400 format
- Slice/TILE split
- Block Mapping ROI
- 8-area OSD
- Link table configuration mode
- YUV/RGB video source with crop, rotation and mirror
- Frame Buffer Compression
- MMU Inside

## 5.2 Block Diagram

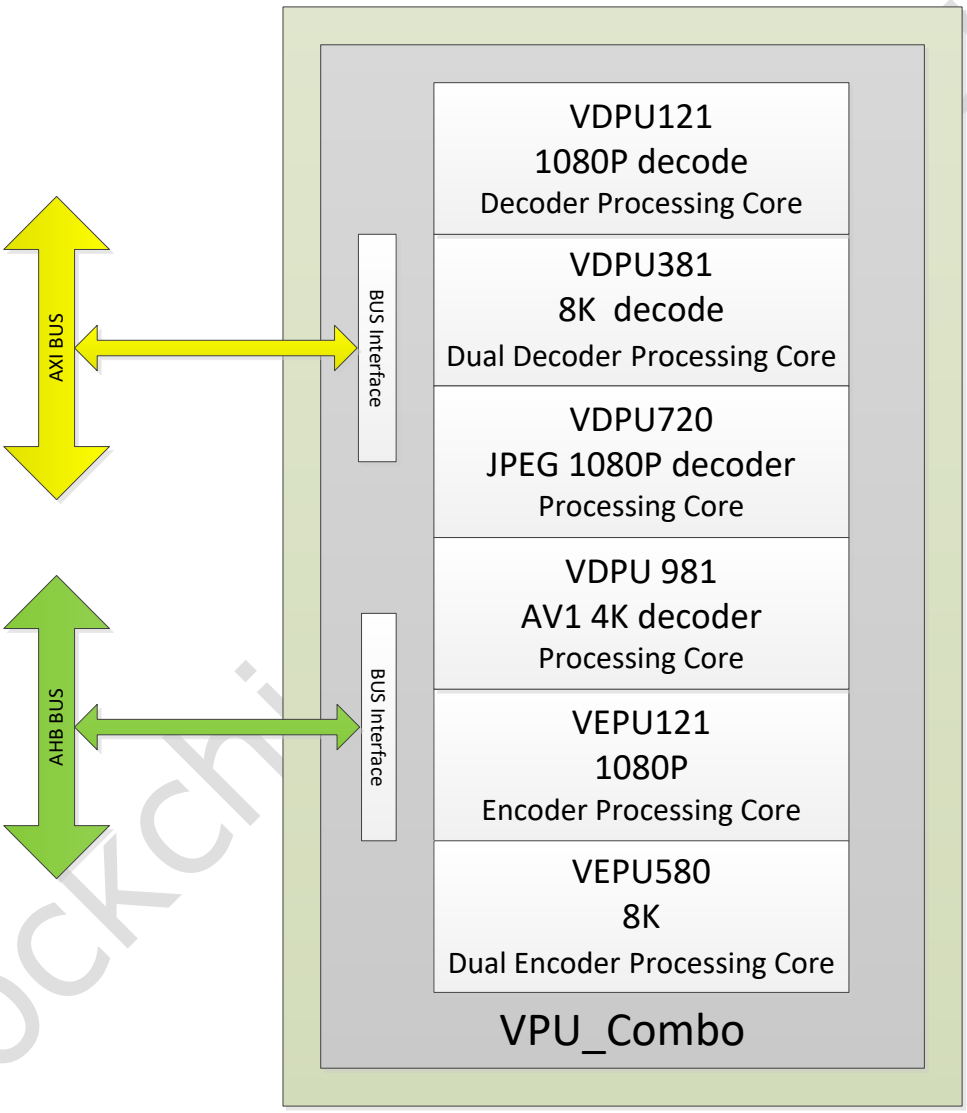



Fig. 5-1 Combo Block Diagram

As shown in the figures above, CPU accesses to the decoder register bank through AHB bus. Bitstream and other necessary data are fed into processing core though AXI read channel, and after several steps of decoding process, decoded pictures and other information data are transferred to designated location in the DDR through AXI write channel.
VDPU121 1080P processing core support multi-format decoder, such as mpeg4, h.263 and so on.
VDPU381 mult-core decoder: can support h.265/vp9/h.264/AVS2 video standard decoder, support dual-core decoding, max solution is up 64Kx64K.

Rockchip Confidential

VDPU720 processing core support jpeg decoder.
VDPU981 processing core support AV1 decoder.
VEPU121 1080P processing core support jpeg encoder.
VEPU580 mult-core encoder processing core can support HEVC/H.264 video encoder, max solution size is 16Kx16K
Please note that VDPU121 and VDPU381 and VDPU720 and AV1 and VEPU121 and VEPU580 is different IP cores, so these processing core can be work together.

# 5.3 Video frame format

This chapter describes different input and output video frame formats supported by VCODEC. Each function module has its own supported video frame formats, and this chapter describes all the video frame formats.

## 5.3.1 YCbCr 4:2:0 Planar Format

In the planar format, each video sample component forms one memory plane. Within one plane, the data has to be stored linearly and contiguously in the memory as shown in fellows. The luminance samples are stored in raster-scan order (Y0Y1 Y2Y3 Y4….). The chrominance samples are stored in two planes also in raster scan order (Cb0Cb1 Cb2Cb3 Cb4…. and Cr0Cr1 Cr2Cr3 Cr4….). In this format each pixel takes 12 bits of memory.

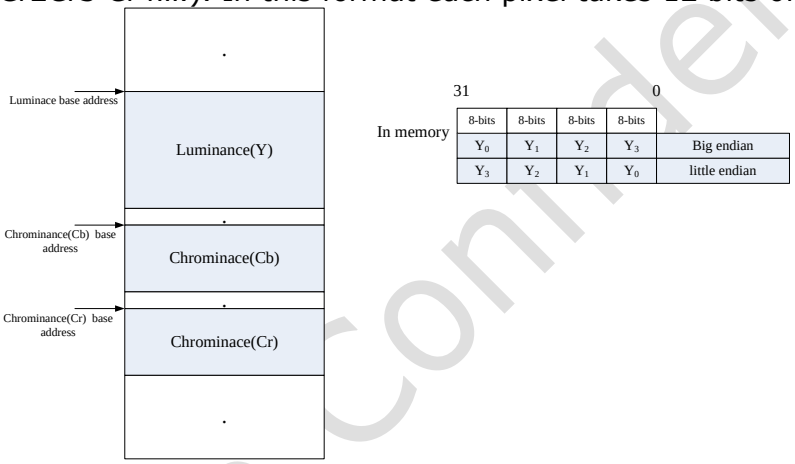



Fig. 5-2 VCODEC YCbCr 4:2:0 planar format

## 5.3.2 YCbCr 4:2:0 Semi-Planar format

In semi-planar YcbCr4:2:0 format the luminance samples from one plane in memory, and chrominance samples from another. Within one plane, the data has to be stored linearly and contiguously in the memory. The luminance pixels are stored in raster-scan order (Y0Y1 Y2Y3 Y4….). The interleaved chrominance CbCr samples are stored in raster-scan order in memory as Cb0Cr0 Cb1Cr1 Cb2 Cr2 Cb3Cr3 Cb4 Cr4….
Semi-Planar format supports both progressive and interlaced format as presented in Fig. 5-3 VCODEC YCbCr 4:2:0 Semi-planar format
. The interlaced format may be alternative line or each line.

Rockchip Confidential

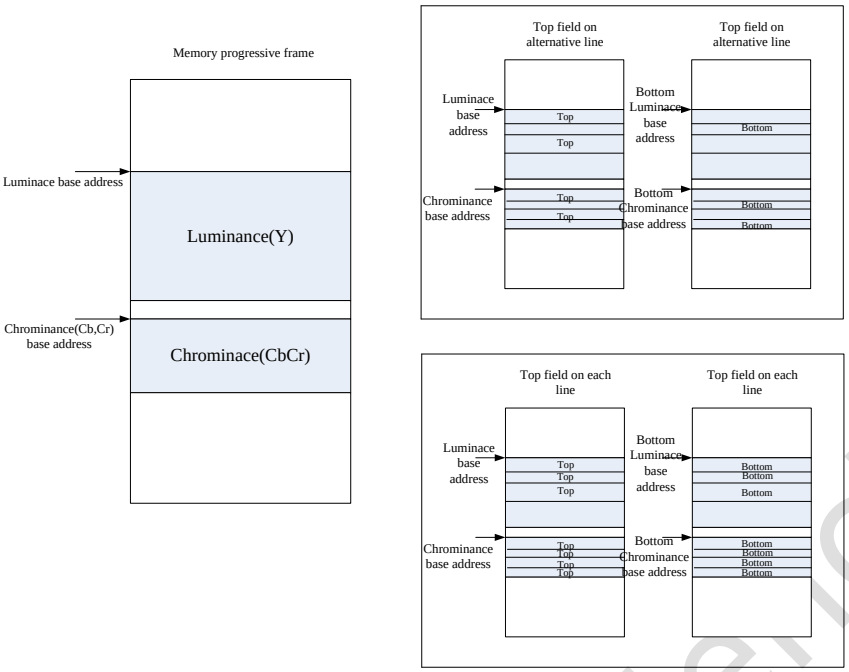



Fig. 5-3 VCODEC YCbCr 4:2:0 Semi-planar format

## 5.3.3 YCbCr 4:2:2 Interleaved Format

In the interleaved YCbCr 4:2:2 format the pixel samples from a single plane in which the data has to be stored linearly and contiguously as shown in Fig. 5-4 VCODEC YCbCr4:2:2 Interleaved format

. The pixel data is in raster scan order and the chrominance samples are interleaved between the luminance samples as Y0Cb0 Y1Cr0 Y2 Cb1 Y3Cr1 Y4 Cb2…. YCrCb, CbYCrY and CrYCbY component orders are supported also. In this format, each pixel takes 16 bits in the memory.

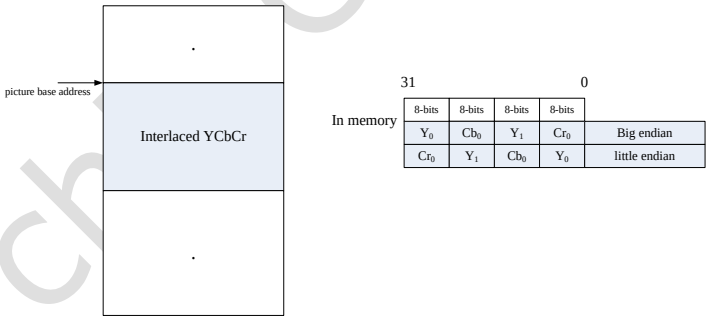



Fig. 5-4 VCODEC YCbCr4:2:2 Interleaved format

## 5.3.4 AYCbCr 4:4:4 Interleaved Format

In the interleaved YcbCr 4:2:2 format, the pixel samples from a single plane in which the data has to be stored linearly and contiguously as show in Fig. 5-5 VCODEC AYCbCr 4:4:4 Interleaved format

. The pixel data is in raster scan order and the chrominance and alpha channel samples are interleaved between the luminance samples as A0Y0 Cb0Cr0 A1 Y1 Cb1Cr1….

Rockchip Confidential

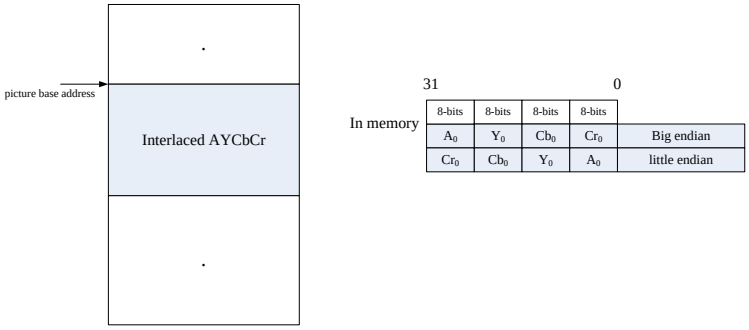



Fig. 5-5 VCODEC AYCbCr 4:4:4 Interleaved format

## 5.3.5 YCbCr Tiled Semi-Planar Format

Like the YUV semi-planar format, the tiled semi-planar format is also organized in the memory on two separate planes. The difference between these formats is that in tiled format the pixel samples are not anymore in raster-scan order but are stored macroblock (16x16 pixels or 8x8 pixels) by macroblock. The samples of each macroblock are stored in consecutive addresses and the macroblocks are ordered from left to right and from top to down as Fig. 5-6 VCODEC Tile scan mode
. When this format used as input data format, it causes the lowest bus load to the system as there is minimal amount of non-sequential memory addressing required when reading the input data to the post-processor.

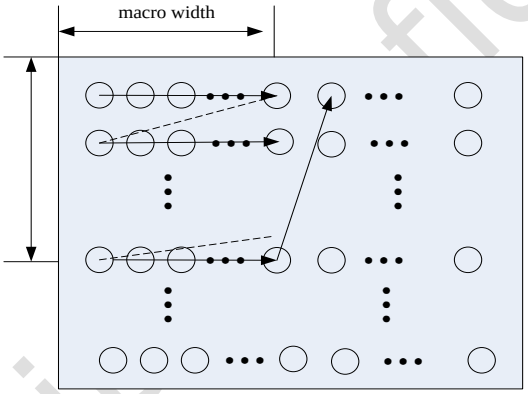



Fig. 5-6 VCODEC Tile scan mode

## 5.3.6 RGB 16bpp Format

In this format each pixel is represented by 16 or less bits containing the red, blue and green samples. There are several 16bpp formats which use different number of bits for each sample. For example the RGB 5-5-5 format uses 5 bits for each sample and 1 bit is left unused or can represent a transparency flag, where RGB 5-6-5 uses 6 bits for the G sample and 5 bits for R and B samples. Common for all 16bpp types is that two pixels fit into one 32-bit space.

Rockchip Confidential

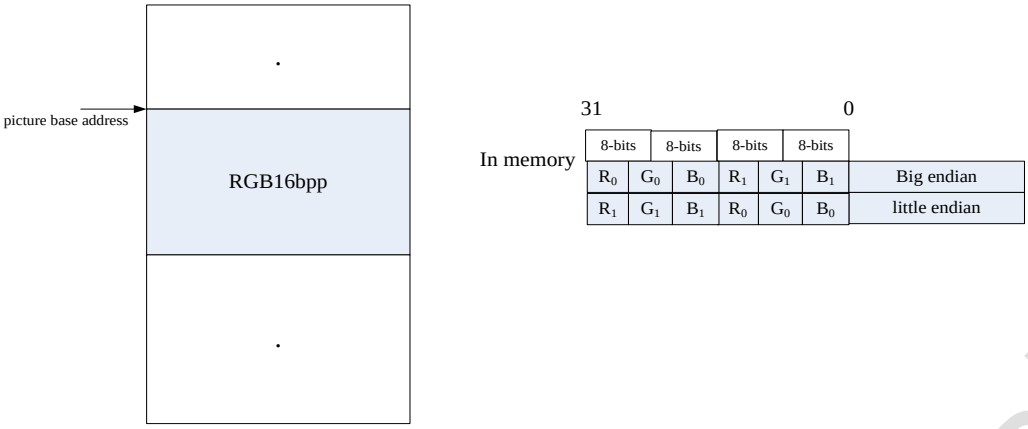



Fig. 5-7 VCODEC RGB 16bpp format

### 5.3.7 RGB 32bpp Format

Any RGB format that has its pixels represented by more than 16bits each is considered to be of 32bpp type. Typically in this format each pixel is represented by three bytes containing a red, blue and green sample and a 4th byte which can be empty or hold an alpha blending value. Common for all 32bpp types is that only one pixel fit into one 32-bit space. The data has to be stored linearly and contiguously in the memory.

### 5.3.8 Frame Buffer Compress (FBC) Format

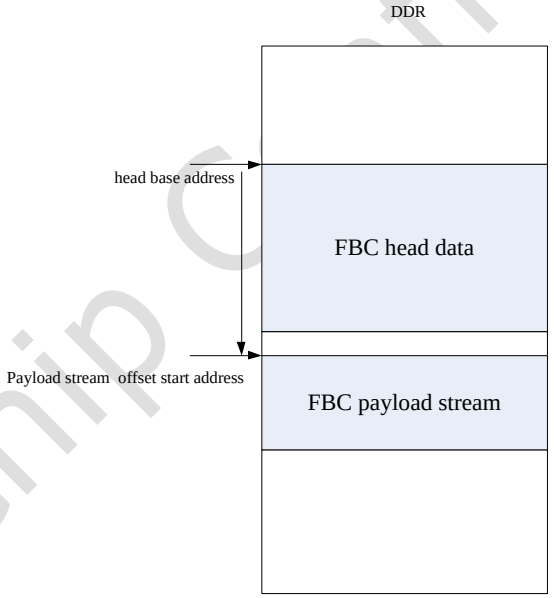



Fig. 5-8 FBC output format

As shown in the figures above, FBC output format include FBC head data and FBC payload stream. Every 16x16 block used one FBC head, every FBC head will take up 128bit ddr space, FBC HEAD is raster store and can support virtual stride. The payload stream use compact mode, and the maximum ddr space which be required is equal to uncompress picture size.

## 5.4 Function Description

### 5.4.1 MMU

The MMU divides memory into 4KB pages, where each page can be individually configured. For each page the following parameters are specified:

- Address translation of virtual memory, this enables the processor to work using address that differ from the physical address in the memory system.

Rockchip Confidential

- The permitted types of accesses to that page. Each page can permit read, write, both, or none.

The MMU use 2-level page table structure:
1. The first level, the page directory consists of 1024 directory table entries(DTEs), each pointing to a page table.
2. The second level, the page table consists of 1024 page table entries(PTEs), each pointing to a page in memory.

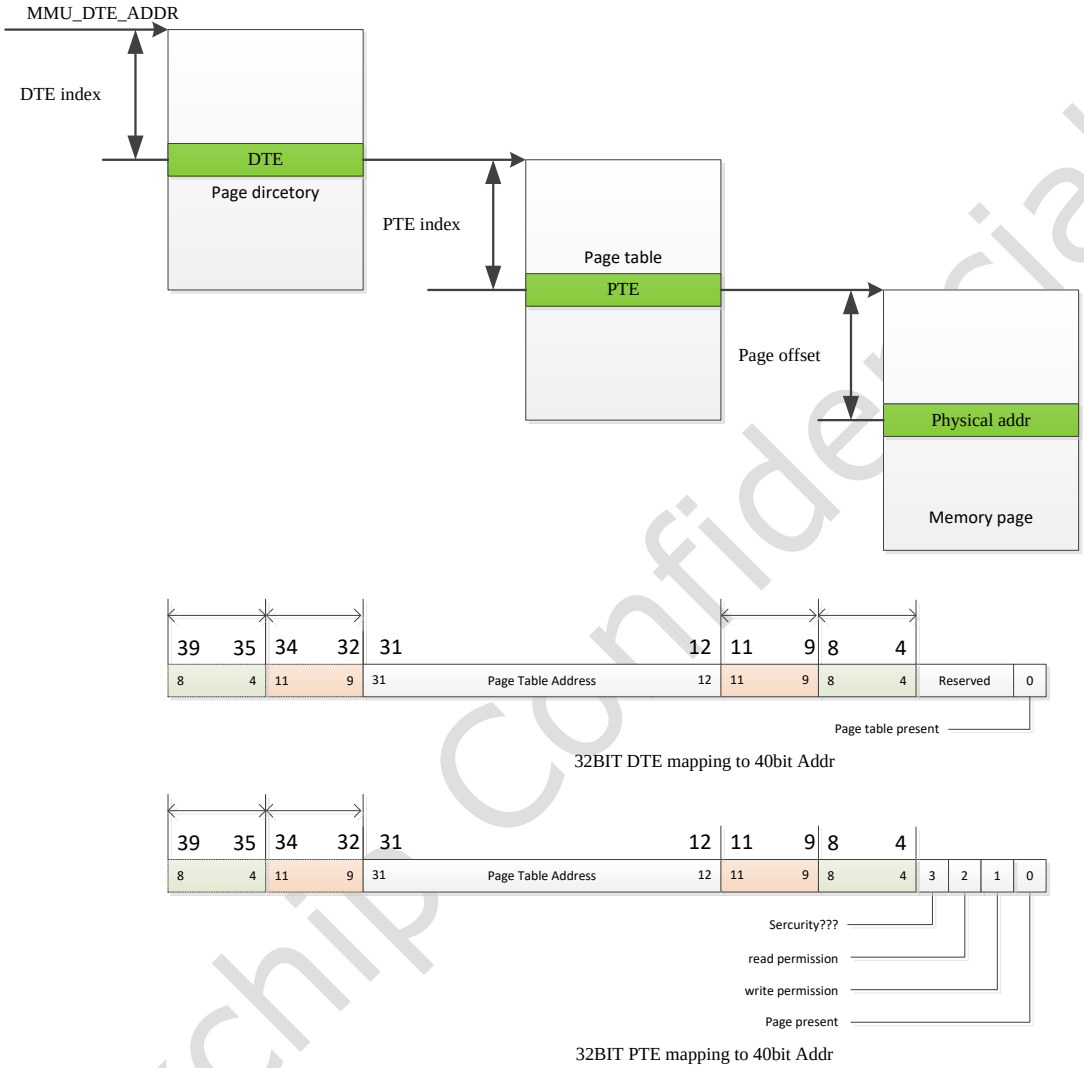



Fig. 5-9 Structure of two-level page table

## 5.4.2 VDPU121 feature supported

1. MPEG-4 decoder

The features that video decoder supports about MPEG-4/H.263 shows as below Table 5-1 MPEG-4/H.263 feature

.

Table 5-1 MPEG-4/H.263 feature

| Feature | Decoder support |
|---|---|
| Input data format | MPEG-4/H.263 elementary video stream |
| Decoding scheme | Frame by frame(or field by field)<br>Video packet by video packet |
| Output data format | YCbCr 4:2:0 semi-planar |
| Supported image size | 48x48 to 1920x1088(MPEG-4)<br>48x48 to 720x576(H.263) |

Rockchip Confidential

| Feature | Decoder support |
|---|---|
| | Step size 16 pixels |
| Maximum frame rate | 60fps at 1920x1088 |
| Maximum bit rate | As specified by MPEG-4 ASP level5 |
| Error detection and concealment | Supported |

The decoder of MPEG-4/H.263 has two operating modes: in the primary mode the HW performs entropy decoding, and in the secondary mode SW performs entropy decoding. Secondary mode is used in MPEG-4 data partitioned stream decoding.

2. MPEG-2/MPEG-1 decoder

The features of MPEG-2/MPEG-1 supported by decoder are shown as Table 5-2 MPEG-2/MPEG-1 features

.

Table 5-2 MPEG-2/MPEG-1 features

| Feature | Decoder support |
|---|---|
| Input data format | MPEG-2/MPEG-1 elementary video stream |
| Decoding scheme | Frame by frame(or field by field)<br>Video packet by video packet |
| Output data format | YCbCr 4:2:0 semi-planar |
| Supported image size | 48x48 to 1920x1088<br>Step size 16 pixels |
| Maximum frame rate | 60fps at 1920x1088 |
| Maximum bit rate | As specified by MPEG-2 MP high level |
| Error detection and concealment | Supported |

The dataflow of MPEG-2/MPEG-1 is the same of H.264 HW performs entropy decoding as **Error! Reference source not found.**.

### 5.4.3 VDPU381 feature supported

1. H265/MVC

Table 5-3 Video H.265 decoder features

| Feature | Decoder support |
|---|---|
| Input data format | H265 byte unit stream/MVC stream |
| Decoding scheme | Frame by frame |
| Output data format | YCbCr 4:2:0 Semi-Planar<br>FBC output format<br>YCbCr Tiled Semi-Planar(Scale Down work mode) |
| Supported image size | 64x64 to 65472x65472<br>step size 16pixels |
| Profile/level | Main<br>Main10<br>level 6.1 |
| Maximum frame rate | YCbCr 4:2:0 60fps @7680x4320 |
| Maximum bit rate | 2133MBPS |
| Other feature | Dual core decoder<br>Error detection and concealment<br>Linked List Pointer mode<br>Colmv compress<br>Scale Down work mode<br>Qos mode<br>W2DDR buffer<br>performance statistics and analysis |

Rockchip Confidential

2. H264/MVC

Table 5-4 Video H.264 decoder features

| Feature | Decoder support |
|---|---|
| Input data format | H264byte or NAL unit stream/SVC stream/MVC stream |
| Decoding scheme | Frame by frame(or field by field)<br>Slice by slice |
| Output data format | YCbCr 4:0:0 (monochrome)<br>YCbCr 4:2:0 semi-planar raster-scan<br>YCbCr 4:2:2 semi-planar raster-scan<br>FBC output format<br>YCbCr Tiled Semi-Planar(Scale Down work mode) |
| Supported image size | 16x16 to 65520x65520<br>step size 16 pixels |
| Profile and Level | Main<br>Main10<br>level 6.0 |
| Maximum frame rate | 30fps @7680x4320 |
| Maximum bit rate | more than 1600MBPS |
| Other feature | Dual core decoder<br>Error detection and concealment<br>Linked List Pointer mode<br>Colmv compress<br>Scale Down work mode<br>Qos mode<br>W2DDR buffer<br>performance statistics and analysis |

3. VP9

Table 5-5 Video vp9 decoder features

| Feature | Decoder support |
|---|---|
| Input data format | VP9 byte unit stream |
| Decoding scheme | Frame by frame |
| Output data format | YCbCr 4:2:0 Semi-Planar<br>FBC output format<br>YCbCr Tiled Semi-Planar(Scale Down work mode) |
| Supported image size | 64x64 to 4096x2304<br>step size 16pixels |
| Profile/level | Profile0<br>Profile2<br>level 6.1 |
| Maximum frame rate | 60fps @7680x4320 |
| Maximum bit rate | more than 1600MBPS |
| Other feature | Dual core decoder<br>Linked List Pointer mode<br>Colmv compress<br>Scale Down work mode<br>Qos mode<br>W2DDR buffer<br>performance statistics and analysis |

4. AVS2

Table 5-6 Video AVS2 decoder features

| Feature | Decoder support |
|---|---|
| Input data format | AVS2 stream |
| Decoding scheme | Frame by frame |
| Output data format | YCbCr 4:2:0 semi-planar raster-scan<br>FBC output format |
| Supported image size | 64x64 to 16383x16383 |

Rockchip Confidencial

| Feature | Decoder support |
|---|---|
| Profile/level | Main profile<br>Main 10bit profile<br>Level 10.2.60 |
| Maximum frame rate | 60fps @7680x4320 |
| Maximum bit rate | more than 1600MBPS |
| Other feature | Dual core decoder<br>Error detection and concealment<br>Linked List Pointer mode<br>Colmv compress<br>Scale Down work mode<br>Qos mode<br>W2DDR buffer<br>performance statistics and analysis |

## 5.4.4 VDPU381 DDR buf size requirements

### 5.4.4.1VDPU381 Input Buffer Size Requested

(1).H265 Unique input data

Table 5-7 Video H.265 decoder Unique input data

| buffer name | buffer size |
|---|---|
| MMU_table | Determined according to whether the MMU is turned on and the actual space of the MMU table |
| PPS+SPS | 7x128bit |
| RPS | 32x128bit |
| Cabac table | 11x128bit |
| Scanlist | 84x128bit |
| Stream_in | According to the actual situation |
| dpb_frame | According to the reference frame size, max reference frame num is 16 |

1-2.H264 Unique input data

Table 5-8 Video H.264 decoder Unique input data

| buffer name | buffer size |
|---|---|
| MMU_table | Determined according to whether the MMU is turned on and the actual space of the MMU table |
| PPS | 3x128bit |
| RPS | 8x128bit |
| Cabac table | 58x128bit |
| Scanlist | 13x128bit |
| Stream_in | According to the actual situation |
| dpb_frame | According to the reference frame size, max reference frame num is 16 |

1-3.VP9 Unique input data

Table 5-9 Video VP9 decoder Unique input data

| buffer name | buffer size |
|---|---|
| MMU_table | Determined according to whether the MMU is turned on and the actual space of the MMU table |
| segid | ((pic_widthxpic_height)/(8x8))x3bit |
| prob_intra | 165x128bit |
| prob_inter | 172x128bit |
| cabac_table | 368Byte |
| stream_in | According to the actual situation |
| dbp_frame | According to the reference frame size, max reference frame num is 3 |

1-4.AVS2 Unique input data

Rockchip Confidential

Table 5-10 Video AVS2 decoder Unique input data

| buffer name | buffer size |
|---|---|
| MMU_table | Determined according to whether the MMU is turned on and the actual space of the MMU table |
| PPS data | 11x128bit |
| Scanlist | |
| stream_in | According to the actual situation |
| dbp_frame | According to the reference frame size, max reference frame num is 7 |

2. Config Register Linked List Pointer mode(LLP mode)

VDPU346 Video decoder support link table mode to improve decoder continuity and reduce CPU participate and interrupt response time. In this mode, the register which used for config will be prepare into DDR, after that user enable link table mode, and then our decoder will fetch the register config information through AXI bus frame by frame. On link table mode, the decoder will auto finish all the frame decoder which be prepared in DDR, and not need CPU participate.

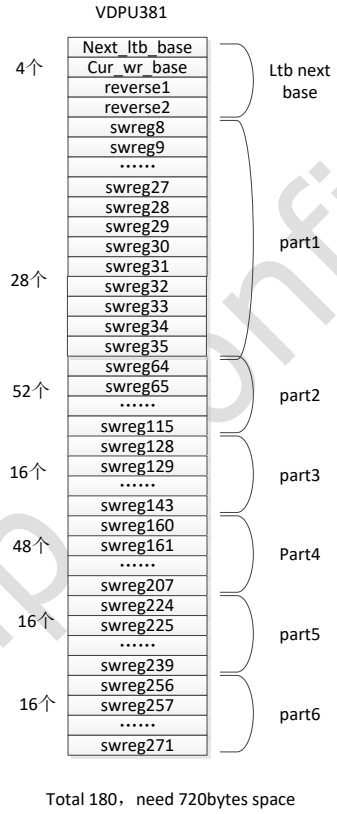



Fig. 5-10 Link table register prepare in DDR format

As show in the above Fig, Link table register prepare in DDR format, each frame config information need 720bytes in DDR. When Link table register work mode be actived, MMU should be config in first, and then parpare register to ddr, at last to config LLP ctrl register to start decoder.

For LLP work mode, LLP register buffer will be required. Every frame will require 512 byte DDR space. Then, buffer size calculate formula be defined as follows:

LLP_register_buffer_size = frame_num * 720 byte

After hardware decoder one frame, will write back some information to DDR where the write back base address is current config storage addr base. All the write back information are listed in the follows table.

Rockchip Confidential

Table 5-11 Link table write back register

| offset | Description |
|---|---|
| 0x0 | swreg224_sta_int |
| 0x4 | swreg225_sta_err_info |
| 0x8 | swreg226_sta_cabac_error_status |
| 0xc | swreg227_sta_colmv_error_ref_picidx |
| 0x10 | swreg228_sta_cabac_error_ctu_offset |
| 0x14 | swreg229_sta_saowr_ctu_offset |
| 0x18 | swreg230_sta_slice_dec_num |
| 0x1c | swreg231_sta_frame_error_ctu_num |
| 0x20 | swreg232_sta_error_packet_num |
| 0x24 | swreg233_sta_err_ctu_num_in_ro |
| 0x28 | swreg258_debug_perf_rd_max_latency_num |
| 0x2c | swreg259_perf_rd_latency_samp_num |
| 0x30 | swreg260_debug_perf_rd_latency_acc_sum |
| 0x34 | swreg261_debug_perf_rd_axi_total_byte |
| 0x38 | swreg262_debug_perf_wr_axi_total_byte |
| 0x3c | swreg263_debug_perf_working_cnt |
| 0x40 | assign info_data0[31:0] = {8'h0,dec_sw_ctu_num[23:0]}; |
| 0x44 | assign info_data1[31:0] = inter_sw_reflst_idx_use[31:0]; |
| 0x48 | assign info_data2[31:0] = {12'h0,inter_sw_pu_cnt_sum[19:0]}; |
| 0x4c | assign info_data3[31:0] = {inter_sw_mv_y_min_out[15:0],inter_sw_mv_x_min_out[15:0]}; |
| 0x50 | assign info_data4[31:0] = |

Rockchip Confidencial

| offset | Description |
|---|---|
| | {inter_sw_mv_y_max_out[15:0],inter_sw_mv_x_max_out[15:0]}; |
| 0x54 | assign info_data5[31:0] =<br>inter_sw_mv_x_out_sum[31:0]; |
| 0x58 | assign info_data6[31:0] =<br>inter_sw_mv_y_out_sum[31:0]; |
| 0x5c | assign info_data7[31:0] =<br>inter_sw_mv_x_out_abs_sum[31:0]; |
| 0x60 | assign info_data8[31:0] =<br>inter_sw_mv_y_out_abs_sum[31:0]; |
| 0x64 | assign info_data9[31:0] =<br>{{(40-MV_BIT_WIDTH){1'b0}},inter_sw_mv_y_out_abs_sum[MV_BIT_WIDTH-1:32],<br>{(40-MV_BIT_WIDTH){1'b0}},inter_sw_mv_x_out_abs_sum[MV_BIT_WIDTH-1:32],<br>{(40-MV_BIT_WIDTH){inter_sw_mv_y_out_sum[MV_BIT_WIDTH-1]}},inter_sw_mv_y_out_sum[MV_BIT_WIDTH-1:32],<br>{(40-MV_BIT_WIDTH){inter_sw_mv_x_out_sum[MV_BIT_WIDTH-1]}},inter_sw_mv_x_out_sum[MV_BIT_WIDTH-1:32]}; |
| 0x68 | assign info_data10[31:0] =<br>{16'h0,cu8x8_skip_num[15:0]}; |
| 0x6c | assign info_data11[31:0] =<br>{{(32-TU_SKIP_SUM_WIDTH){1'b0}},tu_skip_sum[TU_SKIP_SUM_WIDTH-1:0]}; |
| 0x70 | assign info_data12[31:0] =<br>{8'b0,1'b0,cr_qp_max[6:0],1'b0,cb_qp_max[6:0],1'b0,luma_qp_max[6:0]}; |
| 0x74 | assign info_data13[31:0] =<br>{8'b0,1'b0,cr_qp_min[6:0],1'b0,cb_qp_min[6:0],1'b0,luma_qp_min[6:0]}; |
| 0x78 | assign info_data14[31:0] =<br>{{(32-QP_SUM_WIDTH){1'b0}},luma_qp_sum[QP_SUM_WIDTH-1:0]}; |
| 0x7c | assign info_data15[31:0] =<br>{{(32-QP_SUM_WIDTH){1'b0}},cb_qp_sum[QP_SUM_WIDTH-1:0]}; |
| 0x80 | assign info_data16[31:0] = |

Rockchip Confidencial

| offset | Description |
|---|---|
| | {{(32-QP_SUM_WIDTH){1'b0}},cr_qp_sum[QP_SUM_WIDTH-1:0]}; |
| 0x84 | assign info_data17[31:0] =<br>{12'd0,inter_sw_mv_x_pu_cnt_sum[19:0]}; |
| 0x88 | assign info_data18[31:0] =<br>{12'd0,inter_sw_mv_y_pu_cnt_sum[19:0]}; |
| 0x8c | swreg274_sta_ pix_range_y |
| 0x90 | swreg275_sta_ pix_range_u |
| 0x94 | swreg276_sta_ pix_range_v |

The base address of config link table mode is RKVDEC_BASE+0x100.

#### 5.4.4.2VDPU381 Output Buffer Size Requested

We define variables ceilM(N) as follows:

ceil(M,N)=$ceilM(N) = ((N + M - 1) / M) * M$

(1). Output frame decoder buffer size

If output select YCbCr 4:2:0 semi-planar raster-scan format, you can use follows formula to calculate the decoder frame buffer size.

$$luma_frame_buffer_size = y_vir_hor_stride * pic_h * bit_depth_y / 8$$

$$chroma_frame_buffer_size = uv_vir_hor_stride * (pic_h / 2) * bit_depth_c / 8$$

$$frame_buffer_size = luma_frame_buffer_size + chroma_frame_buffer_size$$

There:

- y_vir_hor_stirde: The virtual stride of luma, it must should more bigger than picture width
- uv_vir_hor_stride: The virtual stride of chroma, it must should more big than picture width for YCbCr 4:2:0
- bit_depth_y/c: Main10 or main, its value will be 10 or 8

Second, if FBC format be selected, you can use follows formula to calculate the decoder frame buffer size.

fbc_head_buffer_size = vir_hor_fbc_head*(ceil64(pic_h)+16)/16
payload_buffer_size = celi64(pic_w)*(ceil64(pic_h)+16)*pixel_byte_num
max_fbc_buffer_size = fbc_head_buffer_size + payload_buffaer_size

There:

- vir_hor_fbc_head:the horizontal virtual stride of fbc head, its valud should more bigger than $ceil64(pic_w)/16$.
- pixel_byte_num: yuv400 and yuv444 is 3xbitdepth/8; yuv420 is 1.5xbitdepth/8; yuv422 is 2xbitdepth/8

But payload real buffer size space used will less than payload_buffer_size, it will according to FBC compress rate.

(2). Output frame colmv buffer size

If colmv compress be disabled, you can use follows formula to calculate the decoder frame buffer size.

Table 5-12 Colmv uncompress info

| Format | Colmv_size | Colmv space(bytes unit) |
|---|---|---|
| h264 | 4x4 | 8 |
| hevc | 16x16 | 16 |
| vp9 | 8x8 | 16 |
| avs2 | 16x16 | 8 |

So, the colmv uncompress size is:

Rockchip Confidencial

$$colmv_buffer_size0 = (ceil64(pic_w) * ceil64(pic_h) / (colmv_size * colmv_size)) * colmv_bytes$$

The buffer size unit is byte unit.

If colmv compress be active, you can use follows formula to calculate the decoder frame buffer size.

segment_w = (64 * colmv_size * colmv_size) / ctu_size

segment_h = ctu_size

pic_w_align = ceil(pic_w, segment_w)

pic_h_align = ceil(pic_h, segment_h)

seg_cnt_w=pic_w_align/segment_w

seg_cnt_h=pic_h_align/segment_h

segment_head_line_size=ceil(seg_cnt_w,16)

seg_head_size=segment_head_line_size*seg_cnt_h

seg_payload_size=seg_cnt_w*seg_cnt_h*64*colmv_bytes

colmv_compress_size=seg_head_size+seg_payload_size

where:

- ctu_size: ctu size;
- colmv_size: the block size for each colmv
- colmv_bytes: each colmv space used

(3). Error info buffer size

If error infomation be enable write to DDR, the error info buffer size will be required, and we can use the follows formula to calculate the error info buffer size.

$$error_info_buffer_size = ceil2(slice_num) * 8$$

only h264 and h265 support error info output.

#### 5.4.4.3 VDPU381 Decoder temporary Buffer Size Requested

The temporary buffer only used when VDPU346 on working status.The data write to temporary buffer size is row and col buffer data, we suggest row buffer used internal sram buffer will enhance the decoder performance.

Row buffer and Col buffer size require are listed as fellows.

Table 5-13 Row or Col buffer size required

| data type | required condtion | buffer size |
|---|---|---|
| STRMD Row | H.265/H.264/VP9/AVS2 | 3*pic_width |
| Inter Row | H.265/H.264/VP9/AVS2 | 6*pic_width |
| Inter Col | H.265/H.264/VP9/AVS2 | 3*pic_height |
| Transd Row | H.265/H.264/VP9/AVS2 | 0.4* pic_width |
| Transd col | H.265/H.264/VP9/AVS2 | 0.1* pic_height |
| Recon Row | H.265/H.264/VP9/AVS2 | 6*pic_width |
| Dblk Row | H.265/H.264/VP9/AVS2 | 22*pic_width |
| Sao Row | H.265/H.264/VP9/AVS2 | 6*pic_width |
| FBC Row | H.265/H.264/VP9/AVS2 | 11*pic_width |
| Filterd Col | H.265/VP9, have col tile | 67* pic_height |

### 5.4.5 VDPU720 feature supported

1. JPEG Decoder

JPEG features supported by decoder are as shown in **Error! Reference source not found.**.

Table 5-14 JPEG features

| Feature | Decoder support |
|---|---|
| Input data format | JFIF file format 1.02<br>YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar |
| Decoding scheme | frame by frame |
| Output data format | YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar |
| Supported image size | 48x48 to 65536x65536(4295Mpixels) |

Rockchip Confidencial

| Feature | Decoder support |
|---|---|
| | Step size 8 pixels |
| Maximum frame rate | Up to 560 million pixels per second |
| Thumbnail decoding | JPEG compressed thumbnails supported |
| Restart marker frequency decoding | Supported |
| MJPEG | Supported |
| Error detection | Supported |

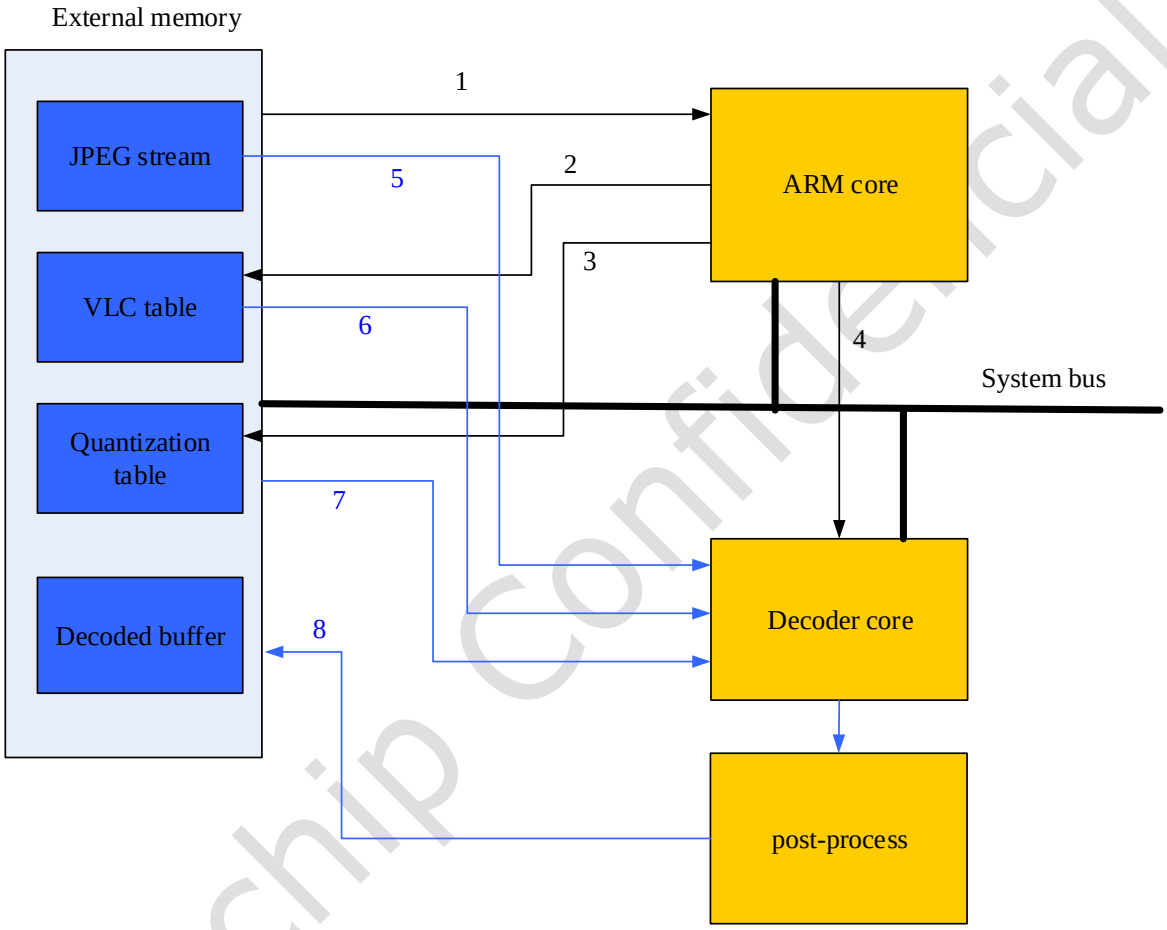



Fig. 5-11 The dataflow of JPEG decoder and post-processor

The data flow of jpeg decoder is as Fig. 5-11 The dataflow of JPEG decoder and post-processor
shown. The decoder software starts decoding the picture by parsing the stream headers (1) and then writes the following items to external memory:
VLC tables (2)
Quantization tables (3)
Last step for the software is to write the hardware control registers and to enable the hardware (4). After starting hardware, SW waits interrupt from HW.
Hardware decodes the picture by reading stream (5), VLC (6) and QP (7) tables. Hardware writes the decoded output picture memory one macroblock at a time (8). When the picture has been fully decoded, or the hardware has run out of stream data, it gives an interrupt with a proper status flag and provides stream end address for software to continue and returns to initial state.
The follow image post-processor only support combined mode.

2. Image Post-processor
The features supported by Post-processor are as show in **Error! Reference source not f**

Rockchip Confidential

**ound.**.

Table 5-15 Post-processor features

| Feature | Post-processor support |
|---|---|
| Input data format | Any format generated by the decoder in combined mode<br>YCbCr 4:2:0 semi-planar<br>YCbCr 4:2:0 planar<br>YCbYCr 4:2:2<br>YCrYCb 4:2:2<br>CbYCrY 4:2:2<br>CrYCbY 4:2:2 |
| Post-processor scheme | Frame by frame. Post-processor handles the image macroblock by macroblock. |
| Input image source | Internal source |
| Output data format | YCbCr 4:2:0 semi-planar<br>YCbCr 4:2:2<br>YCrYCb 4:2:2<br>CbYCrY 4:2:2<br>CrYCbY 4:2:2<br>Fully configurable RGB channel lengths and locations inside 24 bits, e.g. RGB 24-bit (8-8-8), RGB 16-bit(5-6-5). |
| Input image size | 48x48 to 65536x65536<br>Step size 8 pixels |
| Output image size | 16x16 to 65536x65536<br>Horizontal step size 1<br>Vertical step size 1 |
| Image down-scaling | Proprietary averaging filter<br>Arbitrary, integer scaling ratio separately for both dimensions<br>0/2/4/8 down-scaling ratio |
| YCbCr to RGB color conversion | BT.601 compliant<br>BT.709 compliant<br>User definable conversion coefficient |
| Dithering | 2x2 ordered spatial dithering for 4, 5 and 6 bit RGB channel precision |
| Output picture | support raster or tile mode picture out<br>luma 8x8 block tile |

In pipe-line mode, the post-processor works together with the multi-format decoder. The PP will take its input directly from the decoder. The dataflow is as Fig. 5-12 Post-process Dataflow
show.

Rockchip Confidencial

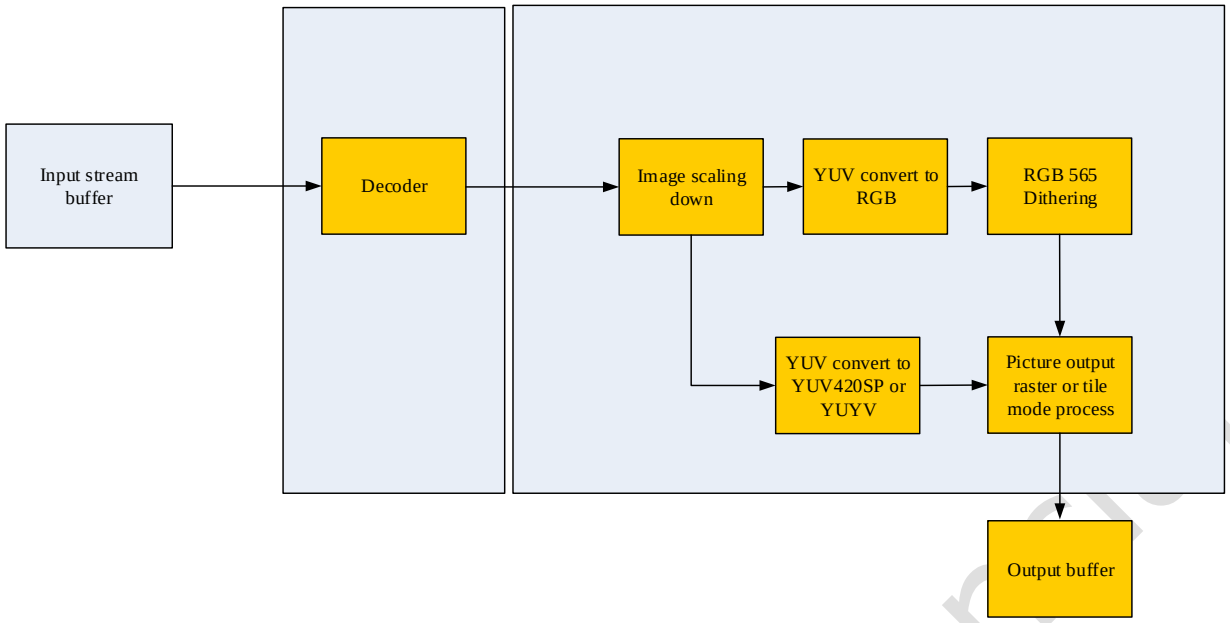



Fig. 5-12 Post-process Dataflow

## 5.4.6 VDPU981 feature supported

1.AV1

Table 5-16 Video H.265 decoder features

| Feature | Decoder support |
|---|---|
| Input data format | AV1 byte unit stream |
| Decoding scheme | Frame by frame |
| Output data format | YCbCr 4:2:0 Semi-Planar<br>FBC output format<br>YCbCr Tiled Semi-Planar |
| Supported image size | 64x64 to 7680x4320<br>step size 16pixels |
| Profile/level | Main<br>Main10<br>level 6.0 |
| Maximum frame rate | YCbCr 4:2:0 60fps @3840x2160 |
| Maximum bit rate | 240MBPS |

## 5.4.7 VEPU121 feature supported

1. JPEG encoder

The JPEG features supported by encoder are shown as follows.

Table 5-17 Video Jpeg encoder feature

| Feature | Encoder support |
|---|---|
| Input data format | YCbCr formats:<br>YCbCr 4:2:0 planar<br>YCbCr 4:2:0 semi-planar<br>YCbYCr 4:2:2①<br>CbYCrY 4:2:2 Interleaved①<br>RGB formats:①<br>RGB444 to BGR444<br>RGB555 to BGR555<br>RGB565 to BGR565<br>RGB888 to BRG888<br>RGB101010 and BRG 101010 |
| Output data format | JFIF FILE format 1.02<br>Non-progressive JPEG |
| Supported image size | 96x96 to 8192x8192(64 million pixels) |

Rockchip Confidential

| Feature | Encoder support |
|---|---|
| | Step size 4 pixels |
| Maximum Data rate | Up to 90 million pixels per second |

①internally encoder handles image only in 4:2:0 format

### 5.4.8 VEPU580 feature supported

Table 5-18 HEVC and H.264 encoder feature

| Feature | Decoder support |
|---|---|
| Input data format | YCbCr formats:<br>YCbCr 4:2:0 planar<br>YCbCr 4:2:0 semi-planar<br>YCbYCr 4:2:2<br>CbYCrY 4:2:2 Interleaved<br>Frame Buffer Compression<br>RGB formats:<br>RGB888<br>ARGB8888 |
| Decoding scheme | Frame by frame |
| Output data format | HEVC and H.264 Bit Stream |
| Supported image size | 64x64 to 16384x8192 |
| Maximum bit rate | 800Mbps |

## 5.5 Register Description

### 5.5.1 Internal Address Mapping

This section describes the control/status registers of the codec.
If VDPU121 decoder is chosen to work, the register base address is VDPU121_base.
If VDPU381 ccu is chosen to work, the register base address is VDPU381_CCU_base.
If VDPU381 core0 is chosen to work, the register base address is VDPU381_core0_base.
If VDPU381 core1 is chosen to work, the register base address is VDPU381_core1_base.
If VDPU720 decoder is chosen to work, the register base address is VDPU720_base.
If VDPU981 decoder is chosen to work, the register base address is VDPU981_base.
If VEPU121 core0 is chosen to work, the register base address is VEPU121_core0_base.
If VEPU121 core1 is chosen to work, the register base address is VEPU121_core1_base.
If VEPU121 core2 is chosen to work, the register base address is VEPU121_core2_base.
If VEPU121 core3 is chosen to work, the register base address is VEPU121_core3_base.
If VEPU121 core4 is chosen to work, the register base address is VEPU121_core4_base.
If VEPU580 core0 is chosen to work, the register base address is VEPU580_core0_base.
If VEPU580 core1 is chosen to work, the register base address is VEPU580_core1_base.
All the register config base are listed as follows:

Table 5-19 Base address of config

| Config Register | Base addr |
|---|---|
| VDPU121 function config base | VDPU121_base |
| VDPU121 mmu config base | VDPU121_base+0x400 |
| VDPU121 cache config base | VDPU121_base+0xC00 |
| VDPU381 core0/1 link table config base | VDPU381_core0/1_base+0x000 |
| VDPU381 core0/1 function config base | VDPU381_core0/1_base+0x100 |
| VDPU381 core0/1 cache config base | VDPU381_core0/1_base+0x600 for Y channel<br>VDPU381_core0/1_base+0x640 for C channel<br>VDPU381_core0/1_base+0x680 for head channel |
| VDPU381 core0/1 mmu config base | VDPU381_core0/1_base0/1+0x700 for rd channel<br>VDPU381_core0/1_base0/1+0x740 for wr channel |
| VDPU720 function config base | VDPU720_base0/1 |
| VDPU720 mmu config base | VDPU720_base0/1+0x480 |

Rockchip Confidencial

| Config Register | Base addr |
|---|---|
| VDPU720 link table config base | VDPU720_base0/1+0x300 |
| VDPU981 VCD base | VDPU981_base |
| VDPU981 L2CACHE base | VDPU981_base + 0x10000 |
| VDPU981 AFBC base | VDPU981_base + 0x20000 |
| VDPU981 MMU base | VDPU981_base + 0x30000 |
| VEPU121 core0/1/2/3/4 function config base | VEPU121_core0/1/2/3/4_base |
| VEPU121 mmu config base | VEPU121_core0/1/2/3/4_base +0x800 |
| VEPU580 function config base | VEPU580_core0/1_base |

Table 29-15 Base address value

| Base addr | value |
|---|---|
| VDPU121_base | 0xFDB5_0400 |
| VDPU381_CCU_base | 0xFDC3_0000 |
| VDPU381_core0_base | 0xFDC3_8000 |
| VDPU381_core1_base | 0xFDC4_0000 |
| VDPU720_base | 0xFDB9_0000 |
| VDPU981_base | 0xFDC7_0000 |
| VEPU121_core0_base | 0xFDB5_0000 |
| VEPU121_core1_base | 0xFDBA_0000 |
| VEPU121_core2_base | 0xFDBA_4000 |
| VEPU121_core3_base | 0xFDBA_8000 |
| VEPU121_core4_base | 0xFDBA_C000 |
| VEPU580_core0_base | 0xFDBD_0000 |
| VEPU580_core1_base | 0xFDBE_0000 |

### 5.5.2 VDPU121 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VDPU_SWREG0_NEW_VERSION | 0x0000 | W | 0x03680000 | ID register(read only)when vpu share memory with hevc, this register is not be used. |
| VDPU_SWREG0 | 0x0000 | W | 0x00000000 | Version |
| VDPU_SWREG1 | 0x0004 | W | 0x00000000 | Interrupt register decoder |
| VDPU_SWREG2 | 0x0008 | W | 0x01000400 | Device configuration register decoder |
| VDPU_SWREG3 | 0x000c | W | 0x00000001 | Device control register 0 (decode, picture type etc) |
| VDPU_SWREG4_H264 | 0x0010 | W | 0x00000000 | Decoder control register 1 (picture parameters) |
| VDPU_SWREG4 | 0x0010 | W | 0x00000000 | Decoder control register 1(picture parameters) |
| VDPU_SWREG5 | 0x0014 | W | 0x00000000 | Decoder control register2 (stream decoding table selects) |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VDPU_SWREG5_H264 | 0x0014 | W | 0x00000000 | Decoder control register2 (stream decoding table selects) |
| VDPU_SWREG6 | 0x0018 | W | 0x00000000 | Decoder control register 3 (stream buffer information) |
| VDPU_SWREG7 | 0x001c | W | 0x00000000 | Decoder control register 4 (H264, VC-1 control ) |
| VDPU_SWREG8 | 0x0020 | W | 0x00000000 | Decoder control register 5(H264, VC-1 control) |
| VDPU_SWREG9 | 0x0024 | W | 0x00000000 | Base address for MB-control (RLC) /VC-1 intensity control 0. |
| VDPU_SREG10_H264_RLC | 0x0028 | W | 0x00000000 | Base address for differential motion vector base address (RLC-mode)/H264 P initial fwd ref pic list register(4-9)/ VC-1 intensity control 1. |
| VDPU_SREG10_H264 | 0x0028 | W | 0x00000000 | Base address for differential motion vector base address (RLC-mode)/H264 P initial fwd ref pic list register(4-9)/VC-1 intensity control 1. |
| VDPU_SWREG11_H264_RLC | 0x002c | W | 0x00000000 | Base address for H.264 intra prediction 4x4/base address for MPEG-4 DC component (RLC)/H264 P initial fwd ref pic list register(10-15)/VC-1 intensity control 2 |
| VDPU_SWREG11_H264 | 0x002c | W | 0x00000000 | Base address for H.264 intra prediction 4x4/base address for MPEG-4 DC component (RLC)/H264 P initial fwd ref pic list register(10-15)/VC-1 intensity control 2 |
| VDPU_SWREG12 | 0x0030 | W | 0x00000000 | Base address for RLC data (RLC)/ stream start address/decoded end addr register (VLC) |
| VDPU_SWREG13 | 0x0034 | W | 0x00000000 | Base address for decoded picture/ base address for JPEG decoder output luminance picture |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VDPU_SWREG14 | 0x0038 | W | 0x00000000 | Base address for reference picture index 0/base address for JPEG decoder output chrominance picture |
| VDPU_SWREG15_JPEG_ROI | 0x003c | W | 0x00000000 | JPEG roi control |
| VDPU_SWREG15 | 0x003c | W | 0x00000000 | Base address for reference picture index 1/JPEG control |
| VDPU_SWREG16 | 0x0040 | W | 0x00000000 | Base address for reference picture index 2/List of VLC code lengths in first JPEG AC table |
| VDPU_SWREG17 | 0x0044 | W | 0x00000000 | Base address for reference picture index 3/List of VLC code lengths in first JPEG AC table |
| VDPU_SWREG18 | 0x0048 | W | 0x00000000 | Base address for reference picture index 4/VC1 control/MPEG4 MVD control/List of VLC code lengths in first JPEG AC table/VC-1 intensity control 4. |
| VDPU_SWREG19 | 0x004c | W | 0x00000000 | Base address for reference picture index 5/MPEG4 TRB/TRD delta 0/VC-1 intensity control 3 List of VLC code lengths in first/second JPEG AC table. |
| VDPU_SWREG20 | 0x0050 | W | 0x00000000 | Base address for reference picture index 6/MPEG4 TRB/TRD delta -1/List of VLC code lengths in second JPEG AC table. Note: The h264 decoder will use these bits. |
| VDPU_SWREG21 | 0x0054 | W | 0x00000000 | Base address for reference picture index 7/MPEG4 TRB/TRD delta 1 / List of VLC code lengths in second JPEG AC table. Note: The h264 decoder will use these bits. |
| VDPU_SWREG22 | 0x0058 | W | 0x00000000 | Base address for reference picture index 8/List of VLC code lengths in second JPEG AC table. Note: The h264 decoder will use these bits. |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VDPU_SWREG23 | 0x005c | W | 0x00000000 | Base address for reference picture index 9 / List of VLC code lengths in first JPEG DC table. Note: The h264 decoder will use these bits. |
| VDPU_SWREG24 | 0x0060 | W | 0x00000000 | Base address for reference picture index 10/List of VLC code lengths in first JPEG DC table. Note: The h264 decoder will use these bits. |
| VDPU_SWREG25 | 0x0064 | W | 0x00000000 | Base address for reference picture index 11/List of VLC code lengths in second JPEG DC table. Note: The h264 decoder will use these bits. |
| VDPU_SWREG26 | 0x0068 | W | 0x00000000 | Base address for reference picture index 12/list of VLC code lengths in second JPEG DC table. Note: The h264 decoder will use these bits. |
| VDPU_SWREG27 | 0x006c | W | 0x00000000 | Base address for reference picture index 13/VC-1 bitpl mbctrl. Note: the h264 decoder will use these bits. |
| VDPU_SWREG28 | 0x0070 | W | 0x00000000 | Base address for reference picture index14. Note: The h264 decoder will use these bits. |
| VDPU_SWREG29 | 0x0074 | W | 0x00000000 | Base address for reference picture index15. Note: The h264 decoder will use these bits. |
| VDPU_SWREG30 | 0x0078 | W | 0x00000000 | Reference picture numbers for index 0 and 1 (H264 VLC). |
| VDPU_SWREG31 | 0x007c | W | 0x00000000 | Reference picture numbers for index 2 and 3 (H264 VLC). |
| VDPU_SWREG32 | 0x0080 | W | 0x00000000 | Reference picture numbers for index 4 and 5 (H264 VLC). |
| VDPU_SWREG33 | 0x0084 | W | 0x00000000 | Reference picture numbers for index 6 and 7 (H264 VLC). |
| VDPU_SWREG34 | 0x0088 | W | 0x00000000 | Reference picture numbers for index 8 and 9 (H264 VLC)/MPEG4, VC1 prediction filter taps |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VDPU_SWREG35_JPEG_ROI | 0x008c | W | 0x00000000 | JPEG roi offset/dc base address |
| VDPU_SWREG35 | 0x008c | W | 0x00000000 | Reference picture numbers for index 10 and 11 (H264 VLC)/VC1 prediction filter taps |
| VDPU_SWREG36 | 0x0090 | W | 0x00000000 | Reference picture numbers for index 12 and 13 (H264 VLC)/VC1 prediction filter taps |
| VDPU_SWREG36_JPEG_ROI | 0x0090 | W | 0x00000000 | JPEG roi offset/dc length |
| VDPU_SWREG37 | 0x0094 | W | 0x00000000 | Reference picture numbers for index 14 and 15 (H264 VLC). |
| VDPU_SWREG38 | 0x0098 | W | 0x00000000 | Reference picture long term flags (H264 VLC). |
| VDPU_SWREG38_H264 | 0x0098 | W | 0x00000000 | Reference picture numbers for index 12 and 13 (H264 VLC)/VC1 prediction filter taps |
| VDPU_SWREG39 | 0x009c | W | 0x00000000 | Reference picture valid flags (H264 VLC). |
| VDPU_SWREG39_H264 | 0x009c | W | 0x00000000 | Reference picture numbers for index 12 and 13 (H264 VLC)/VC1 prediction filter taps |
| VDPU_SWREG40 | 0x00a0 | W | 0x00000000 | Base address for standard dependent tables |
| VDPU_SWREG41 | 0x00a4 | W | 0x00000000 | Base address for direct mode motion vectorsNote: The h264 decoder will use these bits. |
| VDPU_SWREG42 | 0x00a8 | W | 0x00000000 | Bi_dir initial ref pic list register (0-2). Note: The h264 decoder will use these bits. |
| VDPU_SWREG43 | 0x00ac | W | 0x00000000 | Bi-dir initial ref pic list register (3-5). Note: The h264 decoder will use these bits. |
| VDPU_SWREG44 | 0x00b0 | W | 0x00000000 | Bi-dir initial ref pic list register (6-8). Note: The h264 decoder will use these bits. |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VDPU_SWREG45 | 0x00b4 | W | 0x00000000 | Bi-dir initial ref pic list register (9-11). Note: The h264 decoder will use these bits. |
| VDPU_SWREG46 | 0x00b8 | W | 0x00000000 | Bi-dir initial ref pic list register (12- 14). Note: The h264 decoder will use these bits. |
| VDPU_SWREG47 | 0x00bc | W | 0x00000000 | Bi-dir and P fwd initial ref pic list register (15 and P 0-3). Note: The h264 decoder will use these bits. |
| VDPU_SWREG48 | 0x00c0 | W | 0x00000000 | Error concealment register |
| VDPU_SWREG49 | 0x00c4 | W | 0x00000000 | Prediction filter tap register for H264, MPEG4, VC1 |
| VDPU_SWREG50 | 0x00c8 | W | 0xfbb56f80 | Synthesis configuration register decoder 0 (read only) |
| VDPU_SWREG51 | 0x00cc | W | 0x00000000 | Reference picture buffer control register |
| VDPU_SWREG52 | 0x00d0 | W | 0x00000000 | Reference picture buffer information register 1 (read only) |
| VDPU_SWREG53 | 0x00d4 | W | 0x00000000 | Reference picture buffer information register 2 (read only) |
| VDPU_SWREG54 | 0x00d8 | W | 0xe5da0000 | Synthesis configuration register decoder 1 (read only) |
| VDPU_SWREG55 | 0x00dc | W | 0x00000000 | Reference picture buffer 2/Advanced prefetch control register |
| VDPU_SWREG56 | 0x00e0 | W | 0x00000000 | Reference buffer information register 3 (read only) |
| VDPU_SWREG57_INTRA_INTER | 0x00e4 | W | 0x00000000 | Intra_dll3t,intra_dblspeed, inter_dblspeed, stream_len_hi |
| VDPU_SWREG57 | 0x00e4 | W | 0x00000000 | Intra_dll3t,intra_dblspeed, inter_dblspeed, stream_len_hi |
| VDPU_SWREG58 | 0x00e8 | W | 0x00000000 | Decoder debug register 0 (read only) |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VDPU_SWREG59 | 0x00ec | W | 0x00000000 | H264 Chrominance 8 pixel interleaved data base |
| VDPU_SWREG60 | 0x00f0 | W | 0x00000000 | Interrupt register post-processor |
| VDPU_SWREG61 | 0x00f4 | W | 0x01010100 | Device configuration register post-processor |
| VDPU_SWREG62 | 0x00f8 | W | 0x00000000 | Deinterlace control register |
| VDPU_SWREG63 | 0x00fc | W | 0x00000000 | Base address for reading post-processing input picture uminance (top field/frame) |
| VDPU_SWREG64 | 0x0100 | W | 0x00000000 | Base address for reading post-processing input picture Cb/Ch (topfield/frame) |
| VDPU_SWREG65 | 0x0104 | W | 0x00000000 | Base address for reading post-processing input picture Cr |
| VDPU_SWREG66 | 0x0108 | W | 0x00000000 | Base address for writing post-processed picture luminance/RGB |
| VDPU_SWREG67 | 0x010c | W | 0x00000000 | Base address for writing post-processed picture Ch |
| VDPU_SWREG68 | 0x0110 | W | 0x00000000 | Register for contrast adjusting |
| VDPU_SWREG69 | 0x0114 | W | 0x00000000 | Register for colour conversion and contrast adjusting |
| VDPU_SWREG70 | 0x0118 | W | 0x00000000 | Register for colour conversion 0 |
| VDPU_SWREG71 | 0x011c | W | 0x00000000 | Register for colour conversion 1 + rotation mode |
| VDPU_SWREG72 | 0x0120 | W | 0x00000000 | PP input size and cropping register |
| VDPU_SWREG73 | 0x0124 | W | 0x00000000 | PP input picture base address for Y bottom field |
| VDPU_SWREG74 | 0x0128 | W | 0x00000000 | PP input picture base for Ch bottom field |
| VDPU_SWREG79 | 0x013c | W | 0x00000000 | Scaling ratio register 1 & padding for B |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VDPU_SWREG80 | 0x0140 | W | 0x00000000 | Scaling register 0 ratio & padding for R and G |
| VDPU_SWREG81 | 0x0144 | W | 0x00000000 | Scaling ratio register 2 |
| VDPU_SWREG82 | 0x0148 | W | 0x00000000 | Rmask register |
| VDPU_SWREG83 | 0x014c | W | 0x00000000 | Gmask register |
| VDPU_SWREG84 | 0x0150 | W | 0x00000000 | Bmask register |
| VDPU_SWREG85 | 0x0154 | W | 0x00000000 | Post-processor control register |
| VDPU_SWREG86 | 0x0158 | W | 0x00000000 | Mask 1 start coordinate register |
| VDPU_SWREG87 | 0x015c | W | 0x00000000 | Mask 2 start coordinate register |
| VDPU_SWREG88 | 0x0160 | W | 0x00000000 | Mask 1 size and PP original width register |
| VDPU_SWREG89 | 0x0164 | W | 0x00000000 | Mask 2 size register |
| VDPU_SWREG90 | 0x0168 | W | 0x00000000 | PiP register 0 |
| VDPU_SWREG91 | 0x016c | W | 0x00000000 | PiP register 1 and dithering control |
| VDPU_SWREG92 | 0x0170 | W | 0x00000000 | Display width and PP input size extension register |
| VDPU_SWREG93 | 0x0174 | W | 0x00000000 | Display width and PP input size extension register |
| VDPU_SWREG94 | 0x0178 | W | 0x00000000 | Base address for alpha blend 2 gui component |
| VDPU_SWREG95 | 0x017c | W | 0x00000000 | Base address for alpha blend 2 gui component |
| VDPU_SWREG98 | 0x0188 | W | 0x00000000 | PP outupt width/height extension |
| VDPU_SWREG99 | 0x018c | W | 0xe000f000 | PP fuse register (read only) |
| VDPU_SWREG100 | 0x0190 | W | 0xff874780 | Synthesis configuration register post-processor (read only) |
| VDPU_SWREG101 | 0x0194 | W | 0x00000000 | Soft reset signals |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VDPU_SWREG103 | 0x019c | W | 0x00000000 | Axi ddr rdata num, the unit is byte |
| VDPU_SWREG104 | 0x01a0 | W | 0x00000000 | Vdpu write data byte num |
| VDPU_SWREG105 | 0x01a4 | W | 0x00000000 | Monitor signal sellected |
| VDPU_SWREG106 | 0x01a8 | W | 0x00000000 | Performance montor cnt0 |
| VDPU_SWREG107 | 0x01ac | W | 0x00000000 | Performance montor cnt1 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

### 5.5.3 VDPU121 Detail Registers Description

**VDPU_SWREG0_NEW_VERSION**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | Reserved |
| 27:24 | RO | 0x3 | Major_version<br>1'b0: 1080p support<br>1'b1: 2160p support |
| 23:16 | RO | 0x68 | Minor_version<br>8'd0: Audis<br>8'd1: Audi<br>8'd2: Maybach<br>8'd3: Audib<br>FF: Share memory with hevc, so should read version from hevc register |
| 15:0 | RW | 0x0000 | Build<br>The rtl's svn num in ic server |

**VDPU_SWREG0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | Pro_num<br>project number |
| 15:12 | RW | 0x0 | Major_version<br>Major version |
| 11:4 | RW | 0x00 | Minor_version<br>Minor version |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | ID_ASCII_EN<br>ASCII type product ID enable |
| 2:0 | RW | 0x0 | Build_version<br>Build version |

**VDPU_SWREG1**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x00 | Reserved |
| 24 | RW | 0x0 | Sw_dec_pic_inf<br>B slice detected. This signal is driven high during picture ready interrupt if B-type slice is found. This bit does not launch interrupt but is used to inform SW about h264 tools.<br>Note: The h264 decoder will use these bits. |
| 23:19 | RO | 0x00 | Reserved |
| 18 | RW | 0x0 | Sw_dec_timeout<br>Interrupt status bit decoder timeout. When high the decoder 0 has been idling for too long. HW will self reset. Possible only if timeout interrupt is enabled.<br>Note: The h264 decoder will use these bits. |
| 17 | RW | 0x0 | Sw_dec_slice_int<br>Interrupt status bit dec_slice_decoded. When high SW must set new base addresses for Sw_dec_out_base and.<br>Sw_jpg_ch_out_base before reseting this status bit. Used for JPEG snapshot modes.<br>Note: The JPEG decoder will use these bits. |
| 16 | RW | 0x0 | Sw_dec_error_int<br>Interrupt status bit input stream error. When high, an error is found in input data stream decoding. HW will self reset.<br>Note: The h264 decoder will use these bits. |
| 15 | RW | 0x0 | Sw_dec_aso_int<br>Interrupt status bit ASO (Arbitrary Slice Ordering) detected.When high, ASO detected in input data stream decoding. HW will self reset.<br>Note: The h264 decoder will use these bits. |
| 14 | RW | 0x0 | Sw_dec_buffer_int<br>Interrupt status bit input buffer empty. When high, Input stream buffer is empty but picture is not ready. HW will not self reset.<br>Note: The h264 decoder will use these bits. |
| 13 | RW | 0x0 | Sw_dec_bus_int<br>Interrupt status bit bus. Error response from bus. HW will self reset.<br>Note: The h264 decoder will use these bits. |
| 12 | RW | 0x0 | Sw_dec_rdy_int<br>Interrupt status bit decoder. When this bit is high decoder has decoded a picture. HW will self reset.<br>Note: The h264 decoder will use these bits. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:9 | RO | 0x0 | Reserved |
| 8 | RW | 0x0 | Sw_dec_irq<br>Decoder IRQ. When high, decoder requests an interrupt. SW will reset this after interrupt is handled.<br>Note: The h264 decoder will use these bits. |
| 7:5 | RO | 0x0 | Reserved |
| 4 | RW | 0x0 | Sw_dec_irq_dis<br>Decoder IRQ disable. When high, there are no interrupts concerning decoder from HW. Polling must be used to see the interrupt statuses.<br>Note: The h264 decoder will use these bits. |
| 3:1 | RO | 0x0 | Reserved |
| 0 | RW | 0x0 | Sw_dec_en<br>Decoder enable. Setting this bit high will start the decoding operation. HW will reset this when picture is processed or ASO or stream error is detected or bus error or timeout interrupt is given.<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG2**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x01 | Sw_dec_axi_rd_id<br>Read ID used for decoder reading services in AXI bus (if connected to AXI).<br>Note: The h264 decoder will use these bits. |
| 23 | RW | 0x0 | Sw_dec_timeout_e<br>Timeout interrupt enable. If enabled HW may return timeout interrupt in case HW gets stucked while decoding picture.<br>Note: The h264 decoder will use these bits. |
| 22 | RW | 0x0 | Sw_dec_strswap32_e<br>Decoder input 32bit data swap for stream data (may be used for 64 bit environment):<br>1'b0: No swapping of 32 bit words<br>1'b1: 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order(also little endian should be enabled)).<br>Note: The h264 decoder will use these bits. |
| 21 | RW | 0x0 | Sw_dec_strendian_e<br>Decoder input endian mode for stream data:<br>1'b0: Big endian (0-1-2-3 order)<br>1'b1: Little endian (3-2-1-0 order)<br>Note: The h264 decoder will use these bits. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 20 | RW | 0x0 | Sw_dec_inswap32_e<br>Decoder input 32bit data swap for other than stream data (may be used for 64 bit environment):<br>1'b0: No swapping of 32 bit words<br>1'b1: 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order(also little endian should be enabled))<br>Note: The h264 decoder will use these bits. |
| 19 | RW | 0x0 | Sw_dec_outswap32_e<br>Decoder output 32bit data swap (may be used for 64 bit environment):<br>1'b0: No swapping of 32 bit words<br>1'b1: 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order(also little endian should be enabled)).<br>Note: The h264 decoder will use these bits. |
| 18 | RW | 0x0 | Sw_dec_data_disc_e<br>Data discard enable. Precise burst lengths are used with reading services. Extra data is discarded internally.<br>Note: The h264 decoder will use these bits. |
| 17 | RW | 0x0 | sw_tiled_mode_msb<br>Tiled mode msb. Concanated to Tiled mode lsb which form 2 bit tiled mode. Definition of tiledmode:<br>2'd0: Tiled mode not enabled<br>2'd1: Tiled mode enabled for 8x4 tile size<br>2'd2, 2'd3: Reserved<br>Note: The h264 decoder will use these bits. |
| 16:11 | RW | 0x00 | Sw_dec_latency<br>Decoder master interface additional latency. Can be used to slow down decoder HW between services in steps of 8 clock cycles:<br>6'd0: No latency<br>6'd1: Minimum 8 cycles of IDLE between services<br>6'd2: Minimum 16 cycles of IDLE between services<br>...<br>6'd63: Minimum latency of 504 cycles of IDLE between services<br>Note: The h264 decoder will use these bits. |
| 10 | RW | 0x1 | Sw_dec_clk_gate_e<br>Decoder dynamic clock gating enable:<br>1'b0: Clock is running for all structures<br>1'b1: Clock is gated for decoder structures that are not used<br>Note: Clock gating value can be changed only when decoder is disabled. |
| 9 | RW | 0x0 | Sw_dec_in_endian<br>Decoder input endian mode for other than stream data:<br>1'b0: Big endian (0-1-2-3 order)<br>1'b1: Little endian (3-2-1-0 order)<br>Note: The h264 decoder will use these bits. |
| 8 | RW | 0x0 | Sw_dec_out_endian<br>Decoder output endian mode:<br>1'b0: Big endian (0-1-2-3 order)<br>1'b1: Little endian (3-2-1-0 order)<br>Note: The h264 decoder will use these bits. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x0 | Sw_tiled_mode_lsb<br>Tiled mode lsb. Concatenated to Tiled mode msb which form 2 bit tiled mode. Defined in tiled_mode_msb.<br>Note: The h264 decoder will use these bits. |
| 6 | RW | 0x0 | Sw_dec_adv_pre_dis<br>Advanced PREFETCH mode disable (advanced reference picture reading mode for video).<br>Note: The h264 decoder will use these bits. |
| 5 | RW | 0x0 | Sw_dec_scmd_dis<br>AXI Single Command Multiple Data 0 disable. (where only the first addresses of the burst are given from address generator). This bit is used to disable the feature (possible SW workaround if something is not working correctly).<br>Note: The h264 decoder will use these bits. |
| 4:0 | RW | 0x00 | Sw_dec_max_burst<br>Maximum burst length for decoder bus transactions. Valid values:<br>AXI: 1-16<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG3**

Address: Operational Base + offset (0x000c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RW | 0x0 | Sw_dec_mode<br>Decoding mode:<br>4'd0: H.264,<br>4'd1: MPEG-4,<br>4'd2: H.263,<br>4'd3: JPEG,<br>4'd4: VC-1,<br>4'd5: MPEG-2,<br>4'd6: MPEG-1,<br>4'd11: AVS,<br>Others: Reserved<br>Note: All the decoder mode will use these bits. |
| 27 | RW | 0x0 | Sw_rlc_mode_e<br>RLC mode enable:<br>1'b1: HW decodes video from RLC input data + side information (Differential MV's, separate DC coeffs, Intra 4x4 modes, MB control). Valid only for H.264 Baseline and MPEG- 4 SP.<br>1'b0: HW decodes video from bit stream (VLC mode) + side information (bitplane data in VC-1).<br>Note: The h264 and MPEG4 decoder will use these bits. |
| 26 | RW | 0x0 | Sw_skip_mode<br>AVS:<br>1'b0: Special MB type code indicates skipped mbs<br>1'b1: Means that skipped mbs are indicated using skip_run - syntax element like in |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 24 | RW | 0x0 | Sw_pjpeg_e<br>Progressive JPEG enable:<br>1'b0: Baseline JPEG<br>1'b1: Progressive JPEG |
| 23 | RW | 0x0 | Sw_pic_interlace_e<br>Coding mode of the current picture:<br>1'b0: Progressive<br>1'b1: Interlaced<br>Note: The h264 decoder will use these bits. |
| 22 | RW | 0x0 | Sw_pic_fieldmode_e<br>Structure of the current picture (residual structure)<br>1'b0: Frame structure, this means MBAFF structured picture for interlaced sequence 1 = field structure<br>Note: The h264 decoder will use these bits. |
| 21 | RW | 0x0 | Sw_pic_b_e<br>B picture enable for current picture:<br>1'b0: Picture type is I or P depending on sw_pic_inter_e<br>1'b1: Picture type is BI (vc1)/D (mpeg1) or B depending on sw_pic_inter_e (not valid for H264 since its slice based information) |
| 20 | RW | 0x0 | Sw_pic_inter_e<br>Picture type.<br>1'b1: Inter type (P)<br>1'b0: Intra type (I)  See also sw_pic_b_e |
| 19 | RW | 0x0 | Sw_pic_topfield_e<br>If field structure is enabled this bit informs which one of the fields is being decoded:<br>1'b0: Bottom field<br>1'b1: Top field<br>Note: The h264 decoder will use these bits. |
| 18 | RW | 0x0 | Sw_fwd_interlace_e<br>Coding mode of forward reference picture:<br>1'b0: Progressive<br>1'b1: Interlaced<br>Note: For backward reference picture the coding mode is always same as for current picture. |
| 16 | RW | 0x0 | Sw_ref_topfield_e<br>Indicates which field should be used as reference if sw_ref_frames = 0 :<br>1'b0: Bottom field<br>1'b1: Top field<br>Used only in VC-1 mode |
| 15 | RW | 0x0 | Sw_dec_out_dis<br>Disable decoder output picture writing:<br>1'b0: Decoder output picture is written to external memory<br>1'b1: Decoder output picture is not written to external memory<br>Note: The h264 decoder will use these bits. |
| 14 | RW | 0x0 | Sw_filtering_dis<br>De-block filtering disable<br>1'b1: Filtering is disabled for current picture<br>1'b0: Filtering is enabled for current picture<br>Note: The h264 decoder will use these bits. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | Sw_pic_fixed_quant<br>Sw_pic_fixed_quant (DEC mode is VC-1 and AVS)<br>1'b0: Quantization parameter can vary inside picture<br>1'b1: Quantization parameter is fixed (pquant)<br>Sw_mvc_e(DEC mode is H264)<br>Multi view coding enable. Possible for H264 only<br>Note: The h264 decoder will use these bits. |
| 12 | RW | 0x0 | Sw_write_mvs_e<br>Direct mode motion vector write enable for current picture / MPEG2 motion vector write enable for error concealment Purposes:<br>1'b0: Writing disabled for current picture<br>1'b1: The direct mode motion vectors are written to external Memory. H264 direct mode motion vectors are written to DPB aside with the corresponding reference picture. Other decoding mode dir mode mvs are written to external memory starting from Sw_dir_mv_base.<br>Note: The h264 decoder will use these bits. |
| 11 | RW | 0x0 | Sw_reftopfirst_e<br>Indicates which FWD reference field has been decoded first.<br>1'b0: FWD reference bottom field<br>1'b1: FWD reference top field<br>Note: The h264 decoder will use these bits. |
| 10 | RW | 0x0 | Sw_seq_mbaff_e<br>Sequence includes MBAFF coded pictures.<br>Note: The h264 decoder will use these bits. |
| 9 | RW | 0x0 | Sw_picord_count_e<br>H264_high config: Picture order count table read enable. If enabled HW will read picture order counts from memory in the beginning of picture.<br>Note: The h264 decoder will use these bits. |
| 8 | RW | 0x0 | Sw_dec_timeout_mode<br>When 1'b0 , timeout cycle is 181'b1<br>When 1'b1, timeout cycle is 221'b1<br>Note: The h264 decoder will use these bits. |
| 7:0 | RW | 0x01 | Sw_dec_axi_wr_id<br>Write ID used for decoder writing services in AXI bus (if connected to AXI).<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG4_H264**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RW | 0x000 | Sw_pic_mb_width<br>Picture width in macroblocks = ((width in pixels + 15) /16)<br>Note: The h264 decoder will use these bits. |
| 22:19 | RO | 0x0 | Reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 18:11 | RW | 0x00 | Sw_pic_mb_height_p<br>Picture height in macroblocks =((height in pixels+15)/16).<br>Picture height is informed as size of the (progressive) frame also<br>For single field (of interlaced content) is being decoded<br>Note: The h264 decoder will use these bits. |
| 10:5 | RO | 0x00 | Reserved |
| 4:0 | RW | 0x00 | Sw_ref_frames<br>H.264: Num_ref_frames, maximum number of short and long term reference frames in decoded picture buffer. |

**VDPU_SWREG4**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RW | 0x000 | Sw_pic_mb_width<br>Picture width in macroblocks = ((width in pixels + 15)/16). |
| 22:19 | RW | 0x0 | Sw_mb_width_off<br>The amount of meaningfull horizontal pixels in last MB (width offset) 0 if exactly 16 pixels multiple picture and all the horizontal pixels in last MB are meaningfull. |
| 18:11 | RW | 0x00 | Sw_pic_mb_height_p<br>Picture height in macroblocks =((height in pixels+15)/16).<br>Picture height is informed as size of the (progressive) frame also for single field (of interlaced content) is being decoded. |
| 10:7 | RW | 0x0 | Sw_mb_height_off<br>The amount of meaningfull vertical pixels in last MB (height offset 0 if exactly 16 pixels multiple picture and all the vertical pixels in last MB are meaningfull. |
| 6 | RW | 0x0 | Sw_alt_scan_e<br>Indicates alternative vertical scan method used for interlaced frames. |
| 5:3 | RW | 0x0 | Sw_pic_mb_w_ext<br>Picture mb width extension. If sw_pic_mb_width does not fit to 9 bits then these bits are used to increase the range up to 11 bits (used as 3 msb). |
| 2:0 | RW | 0x0 | Sw_pic_mb_h_ext<br>Picture mb height extension. If sw_pic_mb_height_p does not fit to 9 bits then these bits are used to increase the range up to 11 bits (used as 3 msb). |

**VDPU_SWREG5**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RW | 0x00 | Sw_strm_start_bit<br>Exact bit of stream start word where decoding can be started (associates with sw_rlc_vlc_base). |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 25 | RW | 0x0 | Sw_sync_marker_e<br>Sync markers enable:<br>1'b0: Synch markers are not used.<br>1'b1: Synch markers are used. For progressive JPEG this indicates that there are restart markers in the stream after restart interval steps. |
| 24 | RW | 0x0 | Sw_type1_quant_e<br>MPEG4: Type 1 quantization enable<br>1'b0: Type 2 inverse Q method<br>1'b1: Type 1 inverse Q method (Q-tables used)<br>H264 (h264_high config), scaling matrix enable:<br>1'b0: Normal transform<br>1'b1: Use scaling matrix for transform (read from external |
| 23:19 | RW | 0x00 | Sw_ch_qp_offset<br>Chroma Qp filter offset. (For H.264 this offset concerns Cb only) |
| 18:14 | RW | 0x00 | Sw_ch_qp_offset2<br>Chroma Qp filter offset for cr type. |
| 13:1 | RO | 0x0000 | Reserved |
| 0 | RW | 0x0 | Sw_fieldpic_flag_e<br>Flag for stream that field_pic_flag exists in stream. |

**VDPU_SWREG5_H264**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RW | 0x00 | Sw_strm_start_bit<br>Exact bit of stream start word where decoding can be started (associates with sw_rlc_vlc_base). |
| 25 | RO | 0x0 | Reserved |
| 24 | RW | 0x0 | Sw_type1_quant_e<br>MPEG4: Type 1 quantization enable<br>1'b0: Type 2 inverse Q method<br>1'b1: Type 1 inverse Q method (Q-tables used)<br>H264 (h264_high config), scaling matrix enable:<br>1'b0: Normal transform<br>1'b1: Use scaling matrix for transform (read from external |
| 23:19 | RW | 0x00 | Sw_ch_qp_offset<br>Chroma Qp filter offset. (For H.264 this offset concerns Cb only) |
| 18:14 | RW | 0x00 | Sw_ch_qp_offset2<br>Chroma Qp filter offset for cr type. |
| 13:1 | RO | 0x0000 | Reserved |
| 0 | RW | 0x0 | Sw_fieldpic_flag_e<br>Flag for stream that field_pic_flag exists in stream. |

**VDPU_SWREG6**

Rockchip Confidencial

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | Sw_start_code_e<br>Bit for indicating stream start code existence:<br>1'b0: Stream doesn't contain start codes<br>1'b1: Stream contains start codes<br>Note: The h264 decoder will use these bits. |
| 30:25 | RW | 0x00 | Sw_init_qp<br>Initial value for quantization parameter (picture quantizer).<br>Note: The h264 decoder will use these bits. |
| 24 | RW | 0x0 | Sw_ch_8pix_ileav_e<br>Enable for additional chrominance data format writing where decoder writes chrominance in group of 8 pixels of Cb and then corresponding 8 pixels of Cr.<br>Data is written to sw_dec_ch8pix_base. Cannot be used if tiled mode is enabled.<br>Note: The h264 decoder will use these bits. |
| 23:0 | RW | 0x000000 | Sw_stream_len<br>Amount of stream data bytes in input buffer. If the given buffer size is not enough for finishing the picture the corresponding interrupt is given and new stream buffer base address and stream buffer size information should be given (associates with Sw_rlc_vlc_base).<br>For VC-1 the buffer must include data for one picture/slice of the picture.<br>For H264/MPEG4/H263/MPEG2/MPEG1 the buffer must include at least data for one slice/VP of the picture.<br>For JPEG the buffer size must be a multiple of 256 bytes or the amount of data for one picture.<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG7**

Address: Operational Base + offset (0x001c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | Sw_cabac_e<br>CABAC enable<br>Note: The h264 decoder will use these bits. |
| 30 | RW | 0x0 | Sw_blackwhite_e<br>1'b0: 4:2:0 sampling format<br>1'b1: 4:0:0 sampling format (H264 monochroma)<br>Note: The h264 decoder will use these bits. |
| 29 | RW | 0x0 | Sw_dir_8x8_infer_e<br>Specifies the method to use to derive luma motion vectors in B_skip, B_Direct_16x16 and B_direct_8x8_inference_flag (see direct_8x8_inference flag).<br>Note: The h264 decoder will use these bits. |
| 28 | RW | 0x0 | Sw_weight_pred_e<br>Weighted prediction enable for P slices.<br>Note: The h264 decoder will use these bits. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 27:26 | RW | 0x0 | Sw_weight_bipr_idc<br>Weighted prediction specification for B slices:<br>2'b00: Default weighted prediction is applied to B slices<br>2'b01: Explicit weighted prediction shall be applied to B slices<br>2'b10: Implicit weighted prediction shall be applied to B slices<br>Note: The h264 decoder will use these bits. |
| 25:21 | RO | 0x00 | Reserved |
| 20:16 | RW | 0x00 | Sw_framenum_len<br>H.264: Bit length of frame_num in data stream.<br>Note: The h264 decoder will use these bits. |
| 15:0 | RW | 0x0000 | Sw_framenum<br>Current frame_num, used to identify short-term reference frames. Used in reference picture reordering.<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG8**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | Sw_const_intra_e<br>Constrained_intra_pred_flag equal to 1 specifies that intra prediction uses only.<br>Neighbouring intra macroblocks in prediction. When equal to 0 also neighbouring.<br>Inter macroblocks are used in intra prediction process.<br>Note: The h264 decoder will use these bits. |
| 30 | RW | 0x0 | Sw_filt_ctrl_pres<br>Deblocking_filter_control_present_flag indicates whether extra variables controlling characteristics of the deblocking filter are present in the slice header.<br>Note: The h264 decoder will use these bits. |
| 29 | RW | 0x0 | Sw_rdpic_cnt_pres<br>Redundant_pic_cnt_present_flag specifies whether.<br>Redundant_pic_cnt syntax elements.<br>Note: The h264 decoder will use these bits. |
| 28 | RW | 0x0 | Sw_8x8trans_flag_e<br>8x8 transform flag enable for stream decoding.<br>Note: The h264 decoder will use these bits. |
| 27:17 | RW | 0x000 | Sw_refpic_mk_len<br>Length of decoded reference picture marking bits.<br>Note: The h264 decoder will use these bits. |
| 16 | RW | 0x0 | Sw_idr_pic_e<br>IDR (instantaneous decoding refresh) picture flag.<br>Note: The h264 decoder will use these bits. |
| 15:0 | RW | 0x0000 | Sw_idr_pic_id<br>Idr_pic_id, identifies IDR (instantaneous decoding refresh) picture.<br>Note: The h264 decoder will use these bits. |

Rockchip Confidential

**VDPU_SWREG9**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | Sw_pps_id<br>Pic_parameter_set_id, identifies the picture parameter set that is referred to in the slice header.<br>Note: The h264 decoder will use these bits. |
| 23:19 | RW | 0x00 | Sw_refidx1_active<br>Pecifies the maximum reference index that can be used while decoding inter predicted macro blocks.<br>Note: The h264 decoder will use these bits. |
| 18:14 | RW | 0x00 | Sw_refidx0_active<br>Specifies the maximum reference index that can be used while decoding inter predicted macro blocks. This is same as in previous decoders (width increased with q bit).<br>Note: The h264 decoder will use these bits. |
| 13:8 | RO | 0x00 | Reserved |
| 7:0 | RW | 0x00 | Sw_poc_length<br>Length of picture order count field in stream.<br>Note: The h264 decoder will use these bits. |

**VDPU_SREG10_H264_RLC**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_diff_mv_base<br>For H264 and MPEG4, RLC mode: Differential motion vector base address. |

**VDPU_SREG10_H264**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | Reserved |
| 29:25 | RW | 0x00 | Sw_pinit_rlist_f9<br>Initial reference picture list for P forward picid 9 |
| 24:20 | RW | 0x00 | Sw_pinit_rlist_f8<br>Initial reference picture list for P forward picid 8 |
| 19:15 | RW | 0x00 | Sw_pinit_rlist_f7<br>Initial reference picture list for P forward picid 7 |
| 14:10 | RW | 0x00 | Sw_pinit_rlist_f6<br>Initial reference picture list for P forward picid 6 |
| 9:5 | RW | 0x00 | Sw_pinit_rlist_f5<br>Initial reference picture list for P forward picid 5 |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4:0 | RW | 0x00 | Sw_pinit_rlist_f4<br>Initial reference picture list for P forward picid 4 |

**VDPU_SWREG11_H264_RLC**

Address: Operational Base + offset (0x002c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_i4x4_or_dc_base<br>RLC mode: H.264: Intra prediction 4x4 mode base address.<br>RLC mode: MPEG-4: DC component base address. |

**VDPU_SWREG11_H264**

Address: Operational Base + offset (0x002c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | Reserved |
| 29:25 | RW | 0x00 | Sw_pinit_rlist_f15<br>Initial reference picture list for P forward picid 15 |
| 24:20 | RW | 0x00 | Sw_pinit_rlist_f14<br>Initial reference picture list for P forward picid 14 |
| 19:15 | RW | 0x00 | Sw_pinit_rlist_f13<br>Initial reference picture list for P forward picid 13 |
| 14:10 | RW | 0x00 | Sw_pint_rlist_f12<br>Initial reference picture list for P forward picid 12 |
| 9:5 | RW | 0x00 | Sw_pint_rlist_f11<br>Initial reference picture list for P forward picid 11 |
| 4:0 | RW | 0x00 | Sw_pint_rlist_f10<br>Initial reference picture list for P forward picid 10 |

**VDPU_SWREG12**

Address: Operational Base + offset (0x0030)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_rlc_vlc_base<br>RLC mode: Base address for RLC data (swreg3.sw_rlc_mode_e = 1).<br>VLC mode: Stream start address / end addr+I288ess with byte precision (swreg4.rlc_mode_en = 0), start bit number in swreg5. stream_start_bit. When sw_dec_buffer_int is high or sw_dec_e is low this register contains HW return value of last_byte_address (not valid for jpeg) where stream has been read (and used) in accuracy of byte. For debug purposes the last_byte_address is also written when stream error/ASO is detected even though it may not be accurate.<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG13**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_dec_out_base<br>Video: Base address for decoder output picture. Points directly to start of decoder output picture or field.<br>JPEG snapshot: Base address for decoder output luminance picture.<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG14**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_refer0_base<br>Base address for reference picture index 0. See picture index definition from toplevel_sp.<br>Note: The h264 decoder will use these bits. |
| 1 | RW | 0x0 | Sw_refer0_field_e<br>Refer picture consist of single fields or frame:<br>1'b0: Reference picture consists of frame<br>1'b1: Reference picture consists of fields<br>Note: The h264 decoder will use these bits. |
| 0 | RW | 0x0 | Sw_refer0_topc_e<br>Which field of reference picture is closer to current picture:<br>1'b0: Bottom field is closer to current picture<br>1'b1: Top field is closer to current picture<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG15_JPEG_ROI**

Address: Operational Base + offset (0x003c)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | Reserved |
| 19 | RW | 0x0 | Sw_jpegroi_in_endian<br>Sw_jpegroi_in_endian<br>1'b0: Big endian (0-1-2-3 order)<br>1'b1: Little endian (3-2-1-0 order) |
| 18 | RW | 0x0 | Sw_jpegroi_in_swap32<br>Sw_jpegroi_in_swap32<br>1'b0: No swapping of 32 bit words<br>1'b1: 32bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1 byte order (also little endian should be enabled). |
| 17:16 | RW | 0x0 | Sw_roi_sample_size<br>ROI MB num sample each time<br>2'b00: 1<br>2'b01: 8<br>2'b10: 16<br>2'b11: 8 |
| 15:12 | RW | 0x0 | Sw_roi_distance<br>The distance between the sample MB and ROI start MB |
| 11:10 | RW | 0x0 | Sw_roi_out_sel<br>ROI output selection<br>2'b00: Output offset/dc<br>2'b01: Output picture<br>2'b10: Output offset/dc and picture<br>2'b11: Output offset/dc |
| 9 | RW | 0x0 | Sw_roi_decode<br>JPEG ROI decode<br>1'b0: Build offset/dc table<br>1'b1: ROI decode |
| 8 | RW | 0x0 | Sw_roi_en<br>JPEG roi mode enable<br>1'b0: Normal jpeg decode mode<br>1'b1: JPEG roi mode |

**VDPU_SWREG15**

Address: Operational Base + offset (0x003c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_refer1_base<br>Base address for reference picture index 1. See picture index definition from toplevel_sp.<br>Note: The h264 decoder will use these bits. |
| 1 | RW | 0x0 | Sw_refer1_field_e<br>Refer picture consist of single fields or frame:<br>1'b0: Reference picture consists of frame<br>1'b1: Reference picture consists of fields |
| 0 | RW | 0x0 | Sw_refer1_topc_e<br>Which field of reference picture is closer to current picture:<br>1'b0: Bottom field is closer to current picture<br>1'b1: Top field is closer to current picture |

Rockchip Confidential

**VDPU_SWREG16**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_refer2_base<br>Base address for reference picture index 2. See picture index definition from toplevel_sp.<br>Note: The h264 decoder will use these bits. |
| 1 | RW | 0x0 | Sw_refer2_field_e<br>Refer picture consist of single fields or frame:<br>1'b0: Reference picture consists of frame<br>1'b1: Reference picture consists of fields<br>Note: The h264 decoder will use these bits. |
| 0 | RW | 0x0 | Sw_refer2_topc_e<br>Which field of reference picture is closer to current picture:<br>1'b0: Bottom field is closer to current picture<br>1'b1: Top field is closer to current picture<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG17**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_refer3_base<br>Base address for reference picture index 3. See picture index definition from toplevel_sp.<br>Note: The h264 decoder will use these bits. |
| 1 | RW | 0x0 | Sw_refer3_field_e<br>Refer picture consist of single fields or frame:<br>1'b0: Reference picture consists of frame<br>1'b1: Reference picture consists of fields<br>Note: The h264 decoder will use these bits. |
| 0 | RW | 0x0 | Sw_refer3_topc_e<br>Which field of reference picture is closer to current picture:<br>1'b0: Bottom field is closer to current picture<br>1'b1: Top field is closer to current picture<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG18**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_refer4_base<br>Base address for reference picture index 4. See picture index definition from toplevel_sp<br>Note: The h264 decoder will use these bits. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | Sw_refer4_field_e<br>Refer picture consist of single fields or frame:<br>1'b0: Teference picture consists of frame<br>1'b1: Teference picture consists of fields<br>Note: The h264 decoder will use these bits. |
| 0 | RW | 0x0 | Sw_refer4_topc_e<br>Which field of reference picture is closer to current picture:<br>1'b0: Bottom field is closer to current picture<br>1'b1: Top field is closer to current picture<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG19**

Address: Operational Base + offset (0x004c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_refer5_base<br>Base address for reference picture index 5. See picture index definition from toplevel_sp.<br>Note: The h264 decoder will use these bits. |
| 1 | RW | 0x0 | Sw_refer5_field_e<br>Refer picture consist of single fields or frame:<br>1'b0: Reference picture consists of frame<br>1'b1: Reference picture consists of fields<br>Note: The h264 decoder will use these bits. |
| 0 | RW | 0x0 | Sw_refer5_topc_e<br>Which field of reference picture is closer to current picture:<br>1'b0: Bottom field is closer to current picture<br>1'b1: Top field is closer to current picture<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG20**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_refer6_base<br>Base address for reference picture index 6. See picture index definition from toplevel_sp.<br>Note: The h264 decoder will use these bits. |
| 1 | RW | 0x0 | Sw_refer6_field_e<br>Refer picture consist of single fields or frame:<br>1'b0: Reference picture consists of frame<br>1'b1: Reference picture consists of fields<br>Note: The h264 decoder will use these bits. |
| 0 | RW | 0x0 | Sw_refer6_topc_e<br>Which field of reference picture is closer to current picture:<br>1'b0: Bottom field is closer to current picture<br>1'b1: Top field is closer to current picture<br>Note: The h264 decoder will use these bits. |

Rockchip Confidencial

**VDPU_SWREG21**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_refer7_base<br>Base address for reference picture index 7. See picture index definition from toplevel_sp<br>Note: The h264 decoder will use these bits. |
| 1 | RW | 0x0 | Sw_refer7_field_e<br>Refer picture consist of single fields or frame:<br>1'b0: Reference picture consists of frame<br>1'b1: Reference picture consists of fields<br>Note: The h264 decoder will use these bits. |
| 0 | RW | 0x0 | Sw_refer7_topc_e<br>Which field of reference picture is closer to current picture:<br>1'b0: Bottom field is closer to current picture<br>1'b1: Top field is closer to current picture<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG22**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_refer8_base<br>Base address for reference picture index 8. See picture index definition from toplevel_sp. |
| 1 | RW | 0x0 | Sw_refer8_field_e<br>Refer picture consist of single fields or frame:<br>1'b0: Reference picture consists of frame<br>1'b1: Reference picture consists of fields |
| 0 | RW | 0x0 | Sw_refer8_topc_e<br>Which field of reference picture is closer to current picture:<br>1'b0: Bottom field is closer to current picture<br>1'b1: Top field is closer to current picture |

**VDPU_SWREG23**

Address: Operational Base + offset (0x005c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_refer9_base<br>Base address for reference picture index 9. See picture index definition from toplevel_sp. |
| 1 | RW | 0x0 | Sw_refer9_field_e<br>Refer picture consist of single fields or frame:<br>1'b0: Reference picture consists of frame<br>1'b1: Reference picture consists of fields |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | Sw_refer9_topc_e<br>Which field of reference picture is closer to current picture:<br>1'b0: Bottom field is closer to current picture<br>1'b1: Top field is closer to current picture |

**VDPU_SWREG24**

Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_refer10_base<br>Base address for reference picture index 10. See picture index definition from toplevel_sp. |
| 1 | RW | 0x0 | Sw_refer10_field_e<br>Refer picture consist of single fields or frame:<br>1'b0: Reference picture consists of frame<br>1'b1: Reference picture consists of fields |
| 0 | RW | 0x0 | Sw_refer10_top_e<br>Which field of reference picture is closer to current picture:<br>1'b0: Bottom field is closer to current picture<br>1'b1: Top field is closer to current picture |

**VDPU_SWREG25**

Address: Operational Base + offset (0x0064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | Reserved |
| 2 | RW | 0x0 | Sw_refer11_base<br>Base address for reference picture index 11. See picture index definition from toplevel_sp. |
| 1 | RW | 0x0 | Sw_refer11_field_e<br>Refer picture consist of single fields or frame:<br>1'b0: Reference picture consists of frame<br>1'b1: Reference picture consists of fields |
| 0 | RW | 0x0 | Sw_refer11_topc_e<br>Which field of reference picture is closer to current picture:<br>1'b0: Bottom field is closer to current picture<br>1'b1: Top field is closer to current picture |

**VDPU_SWREG26**

Address: Operational Base + offset (0x0068)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_refer12_base<br>Base address for reference picture index 12. See picture index definition from toplevel_sp. |
| 1 | RW | 0x0 | Sw_refer12_field_e<br>Refer picture consist of single fields or frame:<br>1'b0: Reference picture consists of frame<br>1'b1: Reference picture consists of fields |
| 0 | RW | 0x0 | Sw_refer12_topc_e<br>Which field of reference picture is closer to current picture:<br>1'b0: Bottom field is closer to current picture<br>1'b1: Top field is closer to current picture |

**VDPU_SWREG27**

Address: Operational Base + offset (0x006c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_refer13_base<br>Base address for reference picture index 13. See picture index definition from toplevel_sp. |
| 1 | RW | 0x0 | Sw_refer13_field_e<br>Refer picture consist of single fields or frame:<br>1'b0: Reference picture consists of frame<br>1'b1: Reference picture consists of fields |
| 0 | RW | 0x0 | Sw_refer13_topc_e<br>Which field of reference picture is closer to current picture:<br>1'b0: Bottom field is closer to current picture<br>1'b1: Top field is closer to current picture |

**VDPU_SWREG28**

Address: Operational Base + offset (0x0070)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_refer14_base<br>Base address for reference picture index 14. See picture index definition from toplevel_sp. |
| 1 | RW | 0x0 | Sw_refer14_field_e<br>Refer picture consist of single fields or frame:<br>1'b0: Reference picture consists of frame<br>1'b1: Reference picture consists of fields |
| 0 | RW | 0x0 | Sw_refer14_topc_e<br>Which field of reference picture is closer to current picture:<br>1'b0: Bottom field is closer to current picture<br>1'b1: Top field is closer to current picture |

**VDPU_SWREG29**

Address: Operational Base + offset (0x0074)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_refer15_base<br>Base address for reference picture index 15. See picture index definition from toplevel_sp. |
| 1 | RW | 0x0 | Sw_refer15_field_e<br>Refer picture consist of single fields or frame:<br>1'b0: Reference picture consists of frame<br>1'b1: Reference picture consists of fields |
| 0 | RW | 0x0 | Sw_refer15_topc_e<br>Which field of reference picture is closer to current picture:<br>1'b0: Bottom field is closer to current picture<br>1'b1: Top field is closer to current picture |

**VDPU_SWREG30**

Address: Operational Base + offset (0x0078)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | Sw_refer1_nbr<br>Number for reference picture index 1. |
| 15:0 | RW | 0x0000 | Sw_refer0_nbr<br>Number for reference picture index 0. |

**VDPU_SWREG31**

Address: Operational Base + offset (0x007c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | Sw_refer3_nbr<br>Number for reference picture index 3. |
| 15:0 | RW | 0x0000 | Sw_refer2_nbr<br>Number for reference picture index 2. |

**VDPU_SWREG32**

Address: Operational Base + offset (0x0080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | Sw_refer5_nbr<br>Number for reference picture index 5. |
| 15:0 | RW | 0x0000 | Sw_refer4_nbr<br>Number for reference picture index 4. |

**VDPU_SWREG33**

Address: Operational Base + offset (0x0084)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | Sw_refer7_nbr<br>Number for reference picture index 7. |
| 15:0 | RW | 0x0000 | Sw_refer6_nbr<br>Number for reference picture index 6. |

**VDPU_SWREG34**

Address: Operational Base + offset (0x0088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | Sw_refer9_nbr<br>Number for reference picture index 9. |
| 15:0 | RW | 0x0000 | Sw_refer8_nbr<br>Number for reference picture index 8. |

**VDPU_SWREG35_JPEG_ROI**

Address: Operational Base + offset (0x008c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_jpegdcoff_base<br>JPEG roi offest/dc base address. |

**VDPU_SWREG35**

Address: Operational Base + offset (0x008c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | Sw_refer11_nbr<br>Number for reference picture index 11. |
| 15:0 | RW | 0x0000 | Sw_refer10_nbr<br>Number for reference picture index 10. |

**VDPU_SWREG36**

Address: Operational Base + offset (0x0090)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | Sw_refer13_nbr<br>Number for reference picture index 13. |
| 15:0 | RW | 0x0000 | Sw_refer12_nbr<br>Number for reference picture index 12. |

**VDPU_SWREG36_JPEG_ROI**

Rockchip Confidencial

Address: Operational Base + offset (0x0090)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | Reserved |
| 16:0 | RW | 0x00000 | Sw_jpegdcoff_len<br>The number of 64bit jpegdcoff, it can be used both when Sw_roi_decode is 1b0 or 1b1. |

**VDPU_SWREG37**

Address: Operational Base + offset (0x0094)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | Sw_refer15_nbr<br>Number for reference picture index 15. |
| 15:0 | RW | 0x0000 | Sw_refer14_nbr<br>Number for reference picture index 14. |

**VDPU_SWREG38**

Address: Operational Base + offset (0x0098)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RW | 0x000 | Sw_pred_bc_tap_3_3<br>Prediction filter set 3, tap 3 |
| 21:12 | RW | 0x000 | Sw_pred_bc_tap_4_0<br>Prediction filter set 4, tap 0 |
| 11:2 | RW | 0x000 | Sw_perd_bc_tap_4_1<br>Prediction filter set 4, tap 1 |

**VDPU_SWREG38_H264**

Address: Operational Base + offset (0x0098)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Sw_refer_lterm_e<br>Long term flag for reference picture index [31:0]. |

**VDPU_SWREG39**

Address: Operational Base + offset (0x009c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RW | 0x000 | Sw_pred_bc_tap_4_2<br>Prediction filter set 4, tap 2 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 21:12 | RW | 0x000 | Sw_pred_bc_tap_4_3<br>Prediction filter set 4, tap 3 |
| 11:2 | RW | 0x000 | Sw_pred_bc_tap_5_0<br>Prediction filter set 5, tap 0 |

**VDPU_SWREG39_H264**

Address: Operational Base + offset (0x009c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Sw_refer_valid_e<br>Valid flag for reference picture index [31:0] |

**VDPU_SWREG40**

Address: Operational Base + offset (0x00a0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_qtable_base<br>Base address for standard dependent tables:<br>JPEG= AC,DC, QP tables<br>MPEG4=QP table base address if type 1 quantization is used<br>MPEG2=QP table base address<br>H.264=base address for various tables<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG41**

Address: Operational Base + offset (0x00a4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_dir_mv_base<br>Direct mode motion vector write/read base address. For H264 this is used only for direct mode motion vector write base.<br>Progressive JPEG: ACDC coefficient read/write base address. If current round is for DC components this base address is pointing to luminance (separate base addresses for chrominance), for AC component rounds this base is used for current type |

**VDPU_SWREG42**

Address: Operational Base + offset (0x00a8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | Reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 29:25 | RW | 0x00 | Sw_binit_rlist_b2<br>Initial reference picture list for bi- direct backward picid 2. |
| 24:20 | RW | 0x00 | Sw_binit_rlist_f2<br>Initial reference picture list for bi- direct forward picid 2. |
| 19:15 | RW | 0x00 | Sw_binit_rlist_b1<br>Initial reference picture list for bi- direct backward picid 1. |
| 14:10 | RW | 0x00 | Sw_binit_rlist_f1<br>Initial reference picture list for bi- direct forward picid 1. |
| 9:5 | RW | 0x00 | Sw_binit_rlist_b0<br>Initial reference picture list for bi- direct backward picid 0. |
| 4:0 | RW | 0x00 | Sw_binit_rlist_f0<br>Initial reference picture list for bi- direct forward picid 0. |

**VDPU_SWREG43**

Address: Operational Base + offset (0x00ac)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | Reserved |
| 29:25 | RW | 0x00 | Sw_binit_rlist_b5<br>Initial reference picture list for bi- direct backward picid 5. |
| 24:20 | RW | 0x00 | Sw_binit_rlist_f5<br>Initial reference picture list for bi- direct forward picid 5. |
| 19:15 | RW | 0x00 | Sw_binit_rlist_b4<br>Initial reference picture list for bi- direct backward picid 4. |
| 14:10 | RW | 0x00 | Sw_binit_rlist_f4<br>Initial reference picture list for bi- direct forward picid 4. |
| 9:5 | RW | 0x00 | Sw_binit_rlist_b3<br>Initial reference picture list for bi- direct backward picid 3. |
| 4:0 | RW | 0x00 | Sw_binit_rlist_f3<br>Initial reference picture list for bi- direct forward picid 3. |

**VDPU_SWREG44**

Address: Operational Base + offset (0x00b0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | Reserved |
| 29:25 | RW | 0x00 | Sw_binit_rlist_b8<br>Initial reference picture list for bi- direct backward picid 8. |
| 24:20 | RW | 0x00 | Sw_binit_rlist_f8<br>Initial reference picture list for bi- direct forward picid 8. |
| 19:15 | RW | 0x00 | Sw_binit_rlist_b7<br>Initial reference picture list for bi- direct backward picid 7. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14:10 | RW | 0x00 | Sw_binit_rlist_f7<br>Initial reference picture list for bi- direct forward picid 7. |
| 9:5 | RW | 0x00 | Sw_binit_rlist_b6<br>Initial reference picture list for bi- direct backward picid 6. |
| 4:0 | RW | 0x00 | Sw_binit_rlist_f6<br>Initial reference picture list for bi- direct forward picid 6. |

**VDPU_SWREG45**

Address: Operational Base + offset (0x00b4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | Reserved |
| 29:25 | RW | 0x00 | Sw_binit_rlist_b11<br>Initial reference picture list for bi-direct backward picid 11. |
| 24:20 | RW | 0x00 | Sw_binit_rlist_f11<br>Initial reference picture list for bi-direct forward picid 11. |
| 19:15 | RW | 0x00 | Sw_binit_rlist_b10<br>Initial reference picture list for bi-direct backward picid 10. |
| 14:10 | RW | 0x00 | Sw_binit_rlist_f10<br>Initial reference picture list for bi-direct forward picid 10. |
| 9:5 | RW | 0x00 | Sw_binit_rlist_b9<br>Initial reference picture list for bi-direct backward picid 9. |
| 4:0 | RW | 0x00 | Sw_binit_rlist_f9<br>Initial reference picture list for bi-direct forward picid 9. |

**VDPU_SWREG46**

Address: Operational Base + offset (0x00b8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | Reserved |
| 29:25 | RW | 0x00 | Sw_binit_rlist_b14<br>Initial reference picture list for bi-direct backward picid 14. |
| 24:20 | RW | 0x00 | Sw_binit_rlist_f14<br>Initial reference picture list for bi-direct forward picid 14. |
| 19:15 | RW | 0x00 | Sw_binit_rlist_b13<br>Initial reference picture list for bi-direct backward picid 13. |
| 14:10 | RW | 0x00 | Sw_binit_rlist_f13<br>Initial reference picture list for bi-direct forward picid 13. |
| 9:5 | RW | 0x00 | Sw_binit_rlist_b12<br>Initial reference picture list for bi-direct backward picid 12. |
| 4:0 | RW | 0x00 | Sw_binit_rlist_f12<br>Initial reference picture list for bi-direct forward picid 12. |

Rockchip Confidencial

**VDPU_SWREG47**

Address: Operational Base + offset (0x00bc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | Reserved |
| 29:25 | RW | 0x00 | Sw_pinit_rlist_f3<br>Initial reference picture list for P forward picid 3. |
| 24:20 | RW | 0x00 | Sw_pinit_rlist_f2<br>Initial reference picture list for P forward picid 2. |
| 19:15 | RW | 0x00 | Sw_pinit_rlist_f1<br>Initial reference picture list for P forward picid 1. |
| 14:10 | RW | 0x00 | Sw_pinit_rlist_f0<br>Initial reference picture list for P forward picid 0. |
| 9:5 | RW | 0x00 | Sw_binit_rlist_b15<br>Initial reference picture list for bi-direct backward picid 15. |
| 4:0 | RW | 0x00 | Sw_binit_rlist_f15<br>Initial reference picture list for bi-direct forward picid 15. |

**VDPU_SWREG48**

Address: Operational Base + offset (0x00c0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RW | 0x000 | Sw_startmb_x<br>Start MB from SW for X dimension. Used in error concealment case.<br>Note: The h264 decoder will use these bits. |
| 22:15 | RW | 0x00 | Sw_startmb_y<br>Start MB from SW for Y dimension. Used in error concealment case.<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG49**

Address: Operational Base + offset (0x00c4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RW | 0x000 | Sw_pred_bc_tap_0_0<br>Prediction filter set 0, tap 0<br>Note: The h264 decoder will use these bits. |
| 21:12 | RW | 0x000 | Sw_pred_bc_tap_0_1<br>Prediction filter set 0, tap 1<br>Note: The h264 decoder will use these bits. |
| 11:2 | RW | 0x000 | Sw_pred_bc_tap_0_2<br>Prediction filter set 0, tap 2<br>Note: The h264 decoder will use these bits. |

Rockchip Confidencial

**VDPU_SWREG50**

Address: Operational Base + offset (0x00c8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x1 | Sw_DEC_MPEG2_PROF<br>Decoding format support, MPEG-2 / MPEG-1<br>1'b0: Not supported<br>1'b1: Supported |
| 30:29 | RO | 0x3 | Sw_DEC_VC1_PROF<br>Decoding format support, VC-1<br>2'd0: Not supported<br>2'd1: Supported up to simple profile<br>2'd2: Supported up to main profile<br>2'd3: Supported up to advanced profile |
| 28 | RO | 0x1 | Sw_DEC_JPEG_PROF<br>Decoding format support, JPEG<br>1'b0: Not supported<br>1'b1: Supported |
| 27:26 | RO | 0x2 | Sw_DEC_MPEG4_PROF<br>Decoding format support, MPEG-4 / H.263<br>2'd0: Not supported<br>2'd1: Supported up to simple profile<br>2'd2: Supported up to advanced simple profile |
| 25:24 | RO | 0x3 | Sw_DEC_H264_PROF<br>Decoding format support, H.264<br>2'd0: Not supported<br>2'd1: Supported up to baseline profile<br>2'd2: Supported up to high profile labeled stream with restricted high profile tools<br>Note: The h264 decoder will use these bits. |
| 22 | RO | 0x0 | Sw_DEC_PJEPEG_EXIT<br>Progressive JPEG support:<br>1'b0: Not supported<br>1'b1: Supported |
| 21 | RO | 0x1 | Sw_DEC_OBUFF_LEVEL<br>Decoder output buffer level:<br>1'b0: 1 MB buffering is used<br>1'b1: 4 MB buffering is used<br>Note: The h264 decoder will use these bits. |
| 20 | RO | 0x1 | Sw_REF_BUFF_EXIST<br>Note: The h264 decoder will use these bits. |
| 19:16 | RO | 0x5 | Sw_DEC_BUS_STRD<br>Note: The h264 decoder will use these bits. |
| 15:14 | RO | 0x1 | Sw_DEC_SYNTH_LAN<br>Note: The h264 decoder will use these bits. |
| 13:12 | RO | 0x2 | Sw_DEC_BUS_WIDTH<br>2'd0: Error<br>2'd1: 32 bit bus<br>2'd2: 64 bit bus<br>2'd3: 128 bit bus<br>Note: The h264 decoder will use these bits. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10:0 | RO | 0x780 | Sw_DEC_MAX_OWIDTH<br>Max configured decoder video resolution that can be decoded. Informed as width of the picture in pixels<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG51**

Address: Operational Base + offset (0x00cc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | Sw_refbu_e<br>Refer picture buffer enable:<br>1'b0: Refer picture buffer disabled<br>1'b1: Refer picture buffer enabled. Valid if picture size is QVGA or more<br>Note: The h264 decoder will use these bits. |
| 30:19 | RW | 0x000 | Sw_refbu_thr<br>Reference buffer disable threshold value (cache miss amount). Used to buffer shut down (if more misses than allowed).<br>Note: The h264 decoder will use these bits. |
| 18:14 | RW | 0x00 | Sw_refbu_picid<br>The used reference picture ID for reference buffer usage<br>Note: The h264 decoder will use these bits. |
| 13 | RW | 0x0 | Sw_refbu_eval_e<br>Enable for HW internal reference ID calculation. If given threshold level is reached by any picture_id after first MB row, that picture_id is used for reference buffer fill for rest of the picture.<br>Note: The h264 decoder will use these bits. |
| 12 | RW | 0x0 | Sw_refbu_fparmod_e<br>Field parity mode enable. Used in refbufferd evaluation mode<br>1'b0: Use the result field of the evaluation<br>1'b1: Use the parity mode field<br>Note: The h264 decoder will use these bits. |
| 11:9 | RO | 0x0 | Reserved |
| 8:0 | RW | 0x000 | Sw_refbu_y_offset<br>Y offset for refbufferd. This coordinate is used to compensate the global motion of the video for better buffer hit rate.<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG52**

Address: Operational Base + offset (0x00d0)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | Sw_refbu_hit_sum<br>The sum of the refbufferd hits of the picture. Determined for each 8x8 luminance partition of the picture. The proceeding of the HW calculation can be read during HW decoding.<br>Note: The h264 decoder will use these bits. |
| 15:0 | RW | 0x0000 | Sw_refbu_intra_sum<br>The sum of the luminance 8x8 intra partitons of the picture. The proceeding of the HW calculation can be read during HW decoding.<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG53**

Address: Operational Base + offset (0x00d4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | Reserved |
| 21:0 | RW | 0x000000 | Sw_refbu_y_mv_sum<br>The sum of the decoded motion vector y-components of the picture. The first luminance motion vector of each MB is used in calculation. Other motion vectors of the MB are discarded. Each motion vector is saturated between 256-255 before calculation. The proceeding of the HW calculation can be read during HW decoding.<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG54**

Address: Operational Base + offset (0x00d8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x1 | Sw_DEC_JPEG_EXTENS<br>JPEG sampling support extension for 411 and 444 samplings and support for bigger max resolution than 16 Mpix (up to 67Mpixels):<br>1'b0: Not supported<br>1'b1: Supported |
| 30 | RO | 0x1 | Sw_DEC_REFBU_ILACE<br>Refbufferd support for interlaced content:<br>1'b0: Not supported<br>1'b1: Supported<br>Note: The h264 decoder will use these bits. |
| 28 | RO | 0x0 | Sw_REF_BUFF2_EXIST<br>Reference picture buffer 2 usage:<br>1'b0: Not supported<br>1'b1: Reference buffer 2 is used<br>Note: The h264 decoder will use these bits. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 25 | RO | 0x0 | Sw_DEC_RTL_ROM<br>ROM implementation type (If design includes ROMs)<br>1'b0: ROMs are implemented from actual ROM units<br>1'b1: ROMs are impelemted from RTL |
| 22 | RO | 0x1 | Sw_DEC_AVS_PROF<br>Decoding format support, AVS<br>1'b0: Not supported<br>1'b1: Supported |
| 21:20 | RO | 0x1 | Sw_DEC_MVC_PROF<br>Decoding format support, MVC<br>1'b0: Not supported<br>1'b1: Supported |
| 18:17 | RO | 0x1 | Sw_DEC_TILED_L<br>Tiled mode support level<br>2'd0: Not supported<br>2'd1: Supported with 8x4 tile size<br>2'd2, 2'd3: Reserved<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG55**

Address: Operational Base + offset (0x00dc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | Sw_refbu2_buf_e<br>Refer picture buffer 2 enable:<br>1'b0: Refer picture buffer disabled<br>1'b1: Refer picture buffer enabled. Valid if picture size is QVGA or more (can be turned of by HW if threshold value reached).<br>Note: The h264 decoder will use these bits. |
| 30:19 | RW | 0x000 | Sw_refbu2_thr<br>Reference buffer disable threshold value (buffer miss amount). Used to buffer shut down (if more misses than allowed).<br>Note: The h264 decoder will use these bits. |
| 18:14 | RW | 0x00 | Sw_refbu2_picid<br>The used reference picture ID for reference buffer usage<br>Note: The h264 decoder will use these bits. |
| 13:0 | RW | 0x0000 | Sw_apf_threshold<br>Advanced prefetch threshold value. If current MB exceeds the threshold the advanced mode is not used. Value 0 disables threshold usage and advanced.<br>Refetch usage is restricted by internal memory limitation only.<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG56**

Address: Operational Base + offset (0x00e0)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | Sw_refbu_top_sum<br>The sum of the top partitions of the picture<br>Note: The h264 decoder will use these bits. |
| 15:0 | RW | 0x0000 | Sw_refbu_bot_sum<br>The sum of the bottom partitions of the picture<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG57_INTRA_INTER**

Address: Operational Base + offset (0x00e4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:15 | RO | 0x00000 | Reserved |
| 14:8 | RO | 0x00 | Debug_service<br>Service_wr[2:0], service_rd[3:0]. |
| 7 | RW | 0x0 | Sw_cache_en<br>1'b1: Cache enable<br>1'b0: Cache disable<br>When Sw_cache_en is 1'b1, Sw_pref_sigchan should also be 1'b1. |
| 6 | RW | 0x0 | Sw_pref_sigchan<br>1'b1: Prefetch single channel enable. |
| 5 | RW | 0x0 | Sw_axiwr_sel<br>1'b0: Auto sel encoder axi signals and decoder axi signals.<br>1'b1: Sel decoder axi signals (it only use to set bu_dec_e to 1'b0 in the middle of a frame). |
| 4 | RW | 0x0 | Sw_paral_bus<br>When it is set to 1'b1, the axi support read and write service parallel; when it is set to 1'b0, the axi only support read and write serial. |
| 3 | RW | 0x0 | Sw_intra_dbl3t<br>In chroma dc intra prediction, when this bit is enable, there will 3 cycle enhance for every block. |
| 2 | RW | 0x0 | Sw_intra_dblspeed<br>Intra double speed enable. |
| 1 | RW | 0x0 | Sw_inter_dblspeed<br>Inter double speed enable. |
| 0 | RW | 0x0 | Sw_stream_len_hi<br>The extension bit of Sw_stream_len. |

**VDPU_SWREG57**

Address: Operational Base + offset (0x00e4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | Fuse_dec_h264<br>1'b1: H.264 enabled |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 30 | RW | 0x0 | Fuse_dec_mpeg4<br>1'b1: MPEG-4/H.263 enabled |
| 29 | RW | 0x0 | Fuse_dec_mpeg2<br>1'b1: MPEG-2/MPEG-1 enabled N |
| 27 | RW | 0x0 | Fuse_dec_jpeg<br>1'b1: JPEG enabled |
| 25 | RW | 0x0 | Fuse_dec_vc1<br>1'b1: VC1 enabled |
| 24 | RW | 0x0 | Fuse_dec_pjpeg<br>1'b1: Progressive JPEG enabled (Requires also JPEG to be enabled |
| 19 | RW | 0x0 | Fuse_dec_avs<br>1'b1: AVS enabled |
| 18 | RW | 0x0 | Fuse_dec_mvc<br>Enabled (requires also H264 to be enabled) |
| 17:16 | RO | 0x0 | Reserved |
| 15 | RW | 0x0 | Fuse_dec_maxw_1920<br>1'b1: Max video width up to 1920 pixels enabled. Priority coded with priority 1. |
| 14 | RW | 0x0 | Fuse_dec_maxw_1280<br>1'b1: Max video width up to 1280 pixels enabled. Priority coded with priority 2. |
| 13 | RW | 0x0 | Fuse_dec_maxw_720<br>1'b1: Max video width up to 720 pixels enabled. Priority coded with priority 3. |
| 12 | RW | 0x0 | Fuse_dec_maxw_352<br>1'b1: Max video width up to 352 pixels enabled. Priority coded with priority 4 |
| 11:8 | RO | 0x0 | Reserved |
| 7 | RW | 0x0 | Fuse_dec_refbuffer<br>1'b1: Reference buffer used |

**VDPU_SWREG58**

Address: Operational Base + offset (0x00e8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | Reserved |
| 30 | RO | 0x0 | Debug_mv_req<br>Mvst_mv_req signal value |
| 29 | RO | 0x0 | Debug_rlc_req<br>Prtr_res_y_req signal value |
| 28 | RO | 0x0 | Debug_res_y_req<br>Prtr_res_y_req signal value |
| 27 | RO | 0x0 | Debug_res_c_req<br>Prtr_res_c_req signal value |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 26 | RO | 0x0 | Debug_strm_da_e<br>Strm_da_e signal value |
| 25 | RO | 0x0 | Debug_framerdy<br>Dfbu_framerdy signal value |
| 24 | RO | 0x0 | Debug_filter_req<br>Dfbu_req_e signal value |
| 23 | RO | 0x0 | Debug_referreq0<br>Drbu_referreq0 signal value |
| 22 | RO | 0x0 | Debug_referreq1<br>Prbu_referreq1 signal value |
| 21 | RO | 0x0 | Reserved |
| 20:0 | RO | 0x000000 | Debug_dec_mb_count<br>HW internal MB counter value |

**VDPU_SWREG59**

Address: Operational Base + offset (0x00ec)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_dec_ch8pix_base<br>Base address for additional chrominance data format where chrominance is interleaved in group of 8 pixels. The usage is enabled by Sw_ch_8pix_ileav_e.<br>Note: The h264 decoder will use these bits. |

**VDPU_SWREG60**

Address: Operational Base + offset (0x00f0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RO | 0x00000 | Reserved |
| 13 | RW | 0x0 | Sw_pp_bus_int<br>Interrupt status bit bus. Error response from bus. In pipeline mode this bit is not used. |
| 12 | RW | 0x0 | Sw_pp_rdy_int<br>Interrupt status bit pp. When this bit is high post processor has processed a picture in external mode. In pipeline mode this bit is not used. |
| 11:9 | RO | 0x0 | Reserved |
| 8 | RW | 0x0 | Sw_pp_irq<br>Post-processor IRQ. SW will reset this after interrupt is handled. HINTpp is not used for pp if IRQ disable pp is high (Sw_pp_irq_n_e = 1). In pipeline mode this bit is not used. |
| 7:5 | RO | 0x0 | Reserved |

Rockchip confidencial

Copyright 2022 © Rockchip Electronics Co., Ltd. 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | Sw_pp_irq_dis<br>Post-processor IRQ disable. When high, there are no interrupts from HW concerning post processing. Polling must be used to see the interrupt. |
| 3:2 | RO | 0x0 | Reserved |
| 1 | RW | 0x0 | Sw_pp_pipeline_e<br>Decoder C post-processing pipeline enable:<br>1'b0: Post-processing is processing different picture than decoder or is disabled<br>1'b1: Post-processing is performed in pipeline with decoder |
| 0 | RW | 0x0 | Sw_pp_e<br>External mode post-processing enable. This bit will start the post-processing operation. Not to be used if PP is in pipeline with decoder (Sw_pp_pipeline_e = 1). HW will reset this when picture is post-processed. |

**VDPU_SWREG61**

Address: Operational Base + offset (0x00f4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x01 | Sw_pp_axi_rd_id<br>Read ID used for AXI PP read services (if connected to AXI) |
| 23:16 | RW | 0x01 | Sw_pp_axi_wr_id<br>Write ID used for AXI PP write services (if connected to AXI) |
| 15 | RO | 0x0 | Reserved |
| 14 | RW | 0x0 | Sw_pp_scmd_dis<br>AXI Single Command Multiple Data disable. |
| 13 | RW | 0x0 | Sw_pp_in_a2_endsel<br>Endian/swap select for Alpha blend input source 2:<br>1'b0: Use PP in endian/swap definitions (Sw_pp_in_endian, Sw_pp_in_swap)<br>1'b1: Use Ablend source 1 endian/swap definitions |
| 12 | RW | 0x0 | Sw_pp_in_a1_swap32<br>Alpha blend source 1 input 32bit data swap (may be used for 64 bit environment):<br>1'b0: No swapping of 32 bit words<br>1'b1: 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order(also little endian should be enabled)) |
| 11 | RW | 0x0 | Sw_pp_in_a1_endian<br>Alpha blend source 1 input data byte endian mode.<br>1'b0: Big endian (0-1-2-3 order)<br>1'b1: Little endian (3-2-1-0 order) |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10 | RW | 0x0 | Sw_pp_in_swap32_e<br>PP input 32bit data swap (may be used for 64 bit environment):<br>1'b0: No swapping of 32 bit words<br>1'b1: 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order(also little endian should be enabled)) |
| 9 | RW | 0x0 | Sw_pp_data_disc_e<br>PP data discard enable. Precise burst lengths are used with reading services. Extra data is discarded internally. |
| 8 | RW | 0x1 | Sw_pp_clkgate_e<br>PP dynamic clock gating enable:<br>1'b1: Clock is gated from PP structures that are not used<br>1'b0: Clock is running for all PP structures<br>Note: Clock gating value can be changed only when PP is not enabled |
| 7 | RW | 0x0 | Sw_pp_in_endian<br>PP input picture byte endian mode. Used only if PP is in standalone mode. If PP is running pipelined with the decoder, this bit has no effect.<br>1'b0: Big endian (0-1-2-3 order)<br>1'b1: Little endian (3-2-1-0 order) |
| 6 | RW | 0x0 | Sw_pp_out_endian<br>PP output picture endian mode for YCbCr data or for any data if config value Sw_PP_OEN_VERSION=1<br>1'b0: Big endian (0-1-2-3 order)<br>1'b1: Little endian (3-2-1-0 order)<br>Note: For Sw_PP_OEN_VERSION=0, 16 bit RGB data this bit works as pixel swapping bit. For 32 bit RGB this bit has no meaning. |
| 5 | RW | 0x0 | Sw_pp_out_swap32_e<br>PP output data word swap (may be used for 64 bit environment):<br>1'b0: No swapping of 32 bit words<br>1'b1: 32 bit data words are swapped (needed in 64 bit environment to achieve 7-6-5-4-3-2-1-0 byte order (also little endian should be enabled)). |
| 4:0 | RW | 0x00 | Sw_pp_max_burst<br>Maximum burst length for PP bus transactions. 1-16 |

**VDPU_SWREG62**

Address: Operational Base + offset (0x00f8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | Sw_deint_e<br>De-interlace enable. Input data is in interlaced format and deinterlacing needs to be performed. |
| 30 | RO | 0x0 | Reserved |
| 29:16 | RW | 0x0000 | Sw_deint_threshold<br>Threshold value used in deinterlacing. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x0 | Sw_deint_blend_e<br>Blend enable for deinterlacing. |
| 14:0 | RW | 0x0000 | Sw_deint_edge_det<br>Edge detect value used for deinterlacing. |

**VDPU_SWREG63**

Address: Operational Base + offset (0x00fc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_pp_in_lu_base<br>Base address for post-processing input luminance picture. If PP input picture is fetched from fields this base address is used to point to topfield of the picture. Used in external mode only. |

**VDPU_SWREG64**

Address: Operational Base + offset (0x0100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_pp_in_cb_base<br>Base address for post-processing input Cb picture or for both chrominance pictures (if chrominances interleaved). If PP input picture is fetched from fields this base address is used to point to topfield of the picture. Used in external mode only. |

**VDPU_SWREG65**

Address: Operational Base + offset (0x0104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_pp_in_cr_base<br>Base address for post-processing input cr picture. Used in external mode only. |

**VDPU_SWREG66**

Address: Operational Base + offset (0x0108)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Sw_pp_out_lu_base<br>Base address for post-processing output picture (luminance/YUYV/RGB). |

**VDPU_SWREG67**

Rockchip Confidential

Address: Operational Base + offset (0x010c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Sw_pp_out_ch_base<br>Base address for post-processing output chrominance picture (interleaved chrominance). |

**VDPU_SWREG68**

Address: Operational Base + offset (0x0110)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | Sw_contrast_thr1<br>Threshold value 1, used with contrast adjusting. |
| 23:20 | RO | 0x0 | Reserved |
| 19:10 | RW | 0x000 | Sw_contrast_off2<br>Offset value 2, used with contrast adjusting. |
| 9:0 | RW | 0x000 | Sw_contrast_off1<br>Offset value 1, used with contrast adjusting. |

**VDPU_SWREG69**

Address: Operational Base + offset (0x0114)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | Sw_pp_in_start_ch<br>For YUYV 422 input format. Enable for start_with_chrominance.<br>1'b0: The order is Y0CbY0Cr or Y0CrY0Cb<br>1'b1: The order is CbY0CrY0 or CrY0CbY0 |
| 30 | RW | 0x0 | Sw_pp_in_cr_first<br>For YUYV 422 input format and YCbCr 420 semiplanar format. Enable for Cr first (before Cb)<br>1'b0: The order is Y0CbY0Cr or CbY0CrY0 (if 420 semiplanar chrominance: CbCrCbCr)<br>1'b1: The order is Y0CrY0Cb or CrY0CbY0 (if 420 semiplanar chrominance: CrCbCrCb) |
| 29 | RW | 0x0 | Sw_pp_out_start_ch<br>For YUYV 422 output format. Enable for start_with_chrominance.<br>1'b0: The order is Y0CbY0Cr or Y0CrY0Cb<br>1'b1: The order is CbY0CrY0 or CrY0CbY0 |
| 28 | RW | 0x0 | Sw_pp_out_cr_first<br>For YUYV 422 output format. Enable for Cr first (before Cb)<br>1'b0: The order is Y0CbY0Cr or CbY0CrY0<br>1'b1: The order is Y0CrY0Cb or CrY0CbY0 |
| 27:18 | RW | 0x000 | Sw_color_coeffa2<br>Coefficient a2, used with Y pixel to calculate all color components. |
| 17:8 | RW | 0x000 | Sw_color_coeffa1<br>Coefficient a1, used with Y pixel to calculate all color components. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:0 | RW | 0x00 | Sw_contrast_thr2<br>Threshold value 2, used with contrast adjusting. |

**VDPU_SWREG70**

Address: Operational Base + offset (0x0118)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | Reserved |
| 29:20 | RW | 0x000 | Sw_color_coeffd<br>Coefficient d, used with Cb to calculate green component value. |
| 19:10 | RW | 0x000 | Sw_color_coeffc<br>Coefficient c, used with Cr to calculate green component value. |
| 9:0 | RW | 0x000 | Sw_color_coeffb<br>Coefficient b, used with Cr to calculate red component value. |

**VDPU_SWREG71**

Address: Operational Base + offset (0x011c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | Reserved |
| 29:21 | RW | 0x000 | Sw_crop_startx<br>Start coordinate x for the cropped area in macroblocks. |
| 20:18 | RW | 0x0 | Sw_rotation_mode<br>Rotation mode:<br>3'b000: Rotation disabled<br>3'b001: Rotate + 90<br>3'b010: Rotate C 90<br>3'b011: Horizontal flip (mirror)<br>3'b100: Vertical flip<br>3'b101: Rotate 180 |
| 17:10 | RW | 0x00 | Sw_color_coefff<br>Coefficient f, used with Y to adjust brightness. |
| 9:0 | RW | 0x000 | Sw_color_coeffe<br>Coefficient e, used with Cb to calculate blue component value. |

**VDPU_SWREG72**

Address: Operational Base + offset (0x0120)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | Sw_crop_starty<br>Start coordinate y for the cropped area in macroblocks. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23 | RO | 0x0 | Reserved |
| 22:18 | RW | 0x00 | Sw_rangemap_coef_y<br>Range map value for Y component (RANGE_MAPY+9 in VC-1 standard). |
| 17 | RO | 0x0 | Reserved |
| 16:9 | RW | 0x00 | Sw_pp_in_height<br>PP input picture height in MBs. Can be cropped from a bigger input picture in external mode. |
| 8:0 | RW | 0x000 | Sw_pp_in_width<br>PP input picture width in MBs. Can be cropped from a bigger input picture in external mode. |

**VDPU_SWREG73**

Address: Operational Base + offset (0x0124)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_pp_bot_yin_base<br>PP input Y base for bottom field. |

**VDPU_SWREG74**

Address: Operational Base + offset (0x0128)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RW | 0x00000000 | Sw_pp_bot_cin_base<br>PP input C base for bottom field (mixed chrominance). |

**VDPU_SWREG79**

Address: Operational Base + offset (0x013c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | Sw_rangemap_y_e<br>Range map enable for Y component (RANGE_MAPY_FLAG in VC-1 standard). For VC1 main profile this bit is used as range expansion enable. |
| 30 | RW | 0x0 | Sw_rangemap_c_e<br>Range map enable for chrominance component (RANGE_MAPUV_FLAG in VC-1 standard). |
| 29 | RW | 0x0 | Sw_ycbcr_range<br>Defines the YCbCr range in RGB conversion:<br>1'b0: 16 --> 235 for Y, 16 --> 240 for Chrominance<br>1'b1: 0 --> 255 for all components |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 28 | RW | 0x0 | Sw_rgb_pix_in32<br>RGB pixel amount/ 32 bit word<br>1'b0: 1 RGB pixel/32 bit<br>1'b1: 2 RGB pixels/32 bit |
| 27:23 | RW | 0x00 | Sw_rgb_r_padd<br>Amount of ones that will be padded in front of the R-component. |
| 22:18 | RW | 0x00 | Sw_rgb_g_padd<br>Amount of ones that will be padded in front of the G-component. |
| 17:0 | RW | 0x00000 | Sw_scale_wratio<br>Scaling ratio for width (outputw-1/inputw-1) |

**VDPU_SWREG80**

Address: Operational Base + offset (0x0140)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | Reserved |
| 30 | RW | 0x0 | Sw_pp_fast_scale_e<br>1'b0: Fast downscaling is not enabled.<br>1'b1: Fast downscaling is enabled. The quality of the picture is decreased but performance is improved. |
| 29:27 | RW | 0x0 | Sw_pp_in_struct<br>PP input data picture structure:<br>3'd0: Top field / progressive frame structure: Read input data from top field base address /frame base address and read every line.<br>3'd1: Bottom field structure: Read input data from bottom field base address and read every line.<br>3'd2: Interlaced field structure: Read input data from both top and bottom field base address and take every line from each field.<br>3'd3: Interlaced frame structure: Read input data from both top and bottom field base address and take every second line from each field.<br>3'd4: Ripped top field structure: Read input data from top field base address and read every second line.<br>3'd5: Ripped bottom field structure: Read input data from bottom field base address and read every second line |
| 26:25 | RW | 0x0 | Sw_hor_scale_mode<br>Horizontal scaling mode:<br>2’b00: Off<br>2’b01: Upscale<br>2’b10: Downscale |
| 24:23 | RW | 0x0 | Sw_ver_scale_mode<br>Vertical scaling mode:<br>2’b00: Off<br>2’b01: Upscale<br>2’b10: Downscale |
| 22:18 | RW | 0x00 | Sw_rgb_b_padd<br>Amount of ones that will be padded in front of the B-component. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17:0 | RW | 0x00000 | Sw_scale_hratio<br>Scaling ratio for height (outputh-1/inputh-1) . |

**VDPU_SWREG81**

Address: Operational Base + offset (0x0144)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | Sw_wscale_invra<br>Inverse scaling ratio for width, or ch (inputw-1 / outputw-1) |
| 15:0 | RW | 0x0000 | Sw_hscale_invra<br>Inverse scaling ratio for height or cv (inputh-1 / outputh-1) |

**VDPU_SWREG82**

Address: Operational Base + offset (0x0148)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Sw_r_mask<br>Bit mask for R component (and alpha channel) |

**VDPU_SWREG83**

Address: Operational Base + offset (0x014c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Sw_g_mask<br>Bit mask for G component (and alpha channel) |

**VDPU_SWREG84**

Address: Operational Base + offset (0x0150)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Sw_b_mask<br>Bit mask for B component (and alpha channel) |

**VDPU_SWREG85**

Address: Operational Base + offset (0x0154)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RW | 0x0 | Sw_pp_in_format<br>PP input picture data format<br>3'd0: YUYV 4:2:2 interleaved (supported only in external mode)<br>3'd1: YCbCr 4:2:0 Semi-planar in linear raster-scan format<br>3'd2: YCbCr 4:2:0 planar (supported only in external mode)<br>3'd3: YCbCr 4:0:0 (supported only in pipelined mode)<br>3'd4: YCbCr 4:2:2 Semi-planar (supported only in pipelined mode)<br>3'd5: YCbCr 4:2:0 Semi-planar in tiled format (supported only in 3'dexternal mode (8170 decoder only)<br>3'd6: YCbCr 4:4:0 Semi-planar (supported only in pipelined mode, possible for jpeg only)<br>3'd7: Escape pp input data format. Defined in swreg86 |
| 28:26 | RW | 0x0 | Sw_pp_out_format<br>PP output picture data format:<br>3'd0: RGB<br>3'd1: YCbCr 4:2:0 planar (Not supported)<br>3'd2: YCbCr 4:2:2 planar (Not supported)<br>3'd3: YUYV 4:2:2 interleaved<br>3'd4: YCbCr 4:4:4 planar (Not supported)<br>3'd5: YCh 4:2:0 chrominance interleaved<br>3'd6: YCh 4:2:2 (Not supported)<br>3'd7: YCh 4:4:4 (Not supported) |
| 25:15 | RW | 0x000 | Sw_pp_out_height<br>Scaled picture height in pixels (Must be dividable by 2 or by any if Pixel Accurate PP output configuration is enabled) Max scaled picture height is 1920 pixels or maximum three times the input source height minus 8 pixels. |
| 14:4 | RW | 0x000 | Sw_pp_out_width<br>Scaled picture width in pixels. Must be dividable by 8 or by any if Pixel Accurate PP output configuration is enabled. Max scaled picture width is 1920 pixels or maximum three times the input source width minus 8 pixels. |
| 3 | RW | 0x0 | Sw_pp_out_tiled_e<br>Tiled mode enable for PP output. Can be used only for YCbYCr 422 output format. Can be used only if correponding configuration supports this feature. Tile size is 4x4 pixels. |
| 2 | RW | 0x0 | Sw_pp_out_swap16_e<br>PP output swap 16 swaps 16 bit halfs inside of 32 bit word. Can be used for 16 bit RGB to change pixel orders but is valid also for any output format.<br>Note: requires that configuration of Sw_PPD_OEN_VERSION=1. |
| 1 | RW | 0x0 | Sw_pp_crop8_r_e<br>PP input picture width is not 16 pixels multiple. Only 8 pixels of the most right MB of the un-rotated input picture is used for PP input. |
| 0 | RW | 0x0 | Sw_pp_crop8_d_e<br>PP input picture height is not 16 pixels multiple. Only 8 pixel rows of the most down MB of the un-rotated input picture is used for PP input. |

**VDPU_SWREG86**

Rockchip Confidential

Address: Operational Base + offset (0x0158)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RW | 0x0 | Sw_pp_in_format_es<br>Escape PP in format. Used if Sw_pp_in_format is defined to 7: 0<br>1'b0: YCbCr 4:4:4<br>1'b1: YCbCr 4:1:1 |
| 28 | RO | 0x0 | Reserved |
| 27:23 | RW | 0x00 | Sw_rangemap_coef_c<br>Range map value for chrominance component<br>(RANGE_MAPUV+9 in VC-1 standard). |
| 22 | RW | 0x0 | Sw_mask1_ablend_e<br>Mask 1 alpha blending enable. Instead of masking the output picture the alpha blending is performed. Alpha blending source can be found from alpha blend 1 base address. Alpha blending can be enabled only for RGB/ YUYV 422 data. |
| 21:11 | RW | 0x000 | Sw_mask1_starty<br>Vertical start pixel for mask area 1. Defines the y coordinate. Coordinate 0,0 means the up-left corner in PP output luminance picture. See Table 47 for restrictions. |
| 10:0 | RW | 0x000 | Sw_mask1_startix<br>Horizontal start pixel for mask area 1. Defines the x coordinate. Coordinate 0,0 means the up-left corner in PP output luminance picture. See Table 47 for restrictions. |

**VDPU_SWREG87**

Address: Operational Base + offset (0x015c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x000 | Reserved |
| 22 | RW | 0x0 | Sw_mask2_ablend_e<br>Mask 2 alpha blending enable. Instead of masking the output picture the alpha blending is performed. Alpha blending source can be found from alpha blend 2 base address. Alpha blending can be enabled only for RGB/YUYV 422 data. |
| 21:11 | RW | 0x000 | Sw_mask_starty<br>Verical start pixel for mask area 2. Defines the y coordinate. Coordinate 0,0 means the up-left corner in PP output Y picture. See Table 47 for restrictions. |
| 10:0 | RW | 0x000 | Sw_mask2_startx<br>Horizontal start pixel for mask area 2. Defines the x coordinate. Coordinate 0,0 means the up-left corner in PP output Y picture. See Table 47 for restrictions. |

**VDPU_SWREG88**

Address: Operational Base + offset (0x0160)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RW | 0x000 | Sw_ext_orig_width<br>PP input picture original width in macro blocks. |
| 22 | RW | 0x0 | Sw_mask1_e<br>Mask 1 enable. If mask 1 is used this bit is high. |
| 21:11 | RW | 0x000 | Sw_mask1_endy<br>Mask 1 end coordinate y in pixels (inside of PPD output picture).<br>Range must be between [Mask1StartCoordinateY, ScaledHeight]. |
| 10:0 | RW | 0x000 | Sw_mask1_endx<br>Mask 1 end coordinate x in pixels (inside of PPD output picture).<br>Range must be between [Mask1StartCoordinateX, ScaledWidth]. |

**VDPU_SWREG89**

Address: Operational Base + offset (0x0164)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x000 | Reserved |
| 22 | RW | 0x0 | Sw_mask2_e<br>Mask 2 enable. If mask 1 is used this bit is high. |
| 21:11 | RW | 0x000 | Sw_mask2_endy<br>Mask 2 end coordinate y in pixels (inside of PP output picture).<br>Range must be between [Mask2StartCoordinateY,ScaledHeight]. |
| 10:0 | RW | 0x000 | Sw_mask2_endx<br>Mask 2 end coordinate x in pixels (inside of PP output picture).<br>Range must be between [Mask2StartCoordinateX,ScaledWidth]. |

**VDPU_SWREG90**

Address: Operational Base + offset (0x0168)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | Reserved |
| 29 | RW | 0x0 | Sw_right_cross_e<br>Right side overcross enable.<br>1'b0: No right side overcross.<br>1'b1: Right side overcross. |
| 28 | RW | 0x0 | Sw_left_cross_e<br>Left side overcross enable.<br>1'b0: No left side overcross.<br>1'b1: Left side overcross. |
| 27 | RW | 0x0 | Sw_up_cross_e<br>Upward overcross enable.<br>1'b0: No upward overcross.<br>1'b1: Upward overcross. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 26 | RW | 0x0 | Sw_down_cross_e<br>Downward overcross enable.<br>1'b0: No downward overcross.<br>1'b1: Downward overcross. |
| 25:15 | RW | 0x000 | Sw_up_cross<br>Amount of upward overcross (vertical pixels outside of display from the upper side). Range must be between [0, ScaledHeight]. |
| 14:11 | RO | 0x0 | Reserved |
| 10:0 | RW | 0x000 | Sw_down_cross<br>Amount of downward overcross (vertical pixels outside of displayfrom the down side). Range must be between [0, ScaledHeight]. |

**VDPU_SWREG91**

Address: Operational Base + offset (0x016c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | Sw_dither_select_r<br>Dithering control for R channel:<br>2'b00: Dithering disabled<br>2'b01: Use four-bit dither matrix<br>2'b10: Use five-bit dither matrix<br>2'b11: Use six-bit dither matrix |
| 29:28 | RW | 0x0 | Sw_dither_select_g<br>Dithering control for G channel:<br>2'b00: Dithering disabled<br>2'b01: Use four-bit dither matrix<br>2'b10: Use five-bit dither matrix<br>2'b11: Use six-bit dither matrix |
| 27:26 | RW | 0x0 | Sw_dither_select_b<br>Dithering control for B channel:<br>2'b00: Dithering disabled<br>2'b01: Use four-bit dither matrix<br>2'b10: Use five-bit dither matrix<br>2'b11: Use six-bit dither matrix |
| 25:24 | RO | 0x0 | Reserved |
| 23:22 | RW | 0x0 | Sw_pp_tiled_mode<br>Input data is in tiled mode (at the moment valid only for YCbCr 420 data, pipeline or external mode):<br>2'b00: Tiled mode not used<br>2'b01: Tiled mode enabled for 8x4 sized tiles<br>2'b10, 2'b11: Reserved |
| 21:11 | RW | 0x000 | Sw_right_cross<br>Amount of right side overcross (Horizontal pixels outside of display from the right side). Range must be between [0, ScaledWidth]. |
| 10:0 | RW | 0x000 | Sw_left_cross<br>Amount of left side overcross (Horizontal pixels outside of display from the left side). Range must be between [0, ScaledWidth]. |

Rockchip Confidencial

**VDPU_SWREG92**

Address: Operational Base + offset (0x0170)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RW | 0x0 | Sw_pp_in_h_ext<br>Extended PP input height. Used with JPEG. |
| 28:26 | RW | 0x0 | Sw_pp_in_w_ext<br>Extended PP input width. Used with JPEG. |
| 25:23 | RW | 0x0 | Sw_crop_starty_ext<br>Extended PP input crop start coordinate x. Used with JPEG. |
| 22:20 | RW | 0x0 | Sw_crop_start_ext<br>Extended PP input crop start coordinate y. Used with JPEG. |
| 19:12 | RO | 0x00 | Reserved |
| 11:0 | RW | 0x000 | Sw_display_width<br>Width of the display in pixels. Max HDTV (1920). |

**VDPU_SWREG93**

Address: Operational Base + offset (0x0174)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Sw_abledn1_base<br>Base address for alpha blending input 1 (if mask1 is used in alpha blending mode). Format of data is 24 bit RGB/ YCbCr and endian/swap -mode is as in PP input. Amount of data is informed with mask 1 size or with ablend1_scanline if ablend cropping is supported in configuration. |

**VDPU_SWREG94**

Address: Operational Base + offset (0x0178)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Sw_ablend2_base<br>Base address for alpha blending input 2 (if mask2 is used in alpha blending mode). Format of data is 24 bit RGB/ YCbCr and endian/swap -mode is as in PP input. Amount of data is informed with mask 2 size or with ablend2_scanline if ablend cropping is supported in configuration. |

**VDPU_SWREG95**

Address: Operational Base + offset (0x017c)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | Reserved |
| 25:13 | RW | 0x0000 | Sw_ablend2_scan<br>Scanline width in pixels for Ablend 2. Usage enabled if corresponding configuration bit is enabled. |
| 12:0 | RW | 0x0000 | Sw_ablend1_scan<br>Scanline width in pixels for Ablend 1. Usage enabled if corresponding configuration bit is enabled. |

**VDPU_SWREG98**

Address: Operational Base + offset (0x0188)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | Reserved |
| 1 | RW | 0x0 | Sw_pp_out_h_ext<br>PP output heightextension. |
| 0 | RW | 0x0 | Sw_pp_out_w_ext<br>PP output widthextension. |

**VDPU_SWREG99**

Address: Operational Base + offset (0x018c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x1 | Fuse_pp_pp<br>1'b1: PP enabled. |
| 30 | RO | 0x1 | Fuse_pp_deint<br>1'b1: Deinterlacing enabled. |
| 29 | RO | 0x1 | Fuse_pp_ablend<br>1'b1: Alpha Blending enabled. |
| 28:16 | RO | 0x0000 | Reserved |
| 15 | RO | 0x1 | Fuse_pp_maxw_1920<br>1'b1: Max PP output width up to 1920 pixels enabled. Priority coded with priority 1. |
| 14 | RO | 0x1 | Fuse_pp_maxw_1280<br>1'b1: Max PP output width up to 1280 pixels enabled. Priority coded with priority 2. |
| 13 | RO | 0x1 | Fuse_pp_maxw_720<br>1'b1: Max PP output width up to 720 pixels enabled. Priority coded with priority 3. |
| 12 | RO | 0x1 | Fuse_pp_maxw_352<br>1'b1: Max PP output width up to 352 pixels enabled. Priority coded with priority 4. |

Rockchip Confidencial

**VDPU_SWREG100**

Address: Operational Base + offset (0x0190)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x1 | SW_ABLEND_CROP_E<br>Alpha blending support for input cropping:<br>1'b0: Not supported. External memory must include the exact image of the area being alpha blended.<br>1'b1: Supported. External memory can include a picture from blended area can be cropped. Requires usage of swreg95. |
| 30 | RO | 0x1 | SW_PPD_PIXAC_E<br>Pixel Accurate PP output mode exists:<br>1'b0: PIP, Scaling and masks can be adjusted by steps of 8 pixels (width) or 2 pixels (height).<br>1'b1: PIP, Scaling and masks can be adjusted by steps of 1 pixel for RGB and 2 pixels for subsampled chroma formats (by using bus specific write strobe functionality). |
| 29 | RO | 0x1 | SW_PPD_TILED_EXIST<br>PP output YCbYCr 422 tiled support (4x4 pixel tiles)<br>1'b0: Not supported<br>1'b1: Supported |
| 28 | RO | 0x1 | SW_PPD_DITH_EXIST<br>Dithering exists:<br>1'b0: No<br>1'b1: Yes |
| 27:26 | RO | 0x3 | SW_PPD_SCALE_LEVEL<br>Scaling support:<br>2'b00: No scaling<br>2'b01: Scaling with lo performance architecture<br>2'b10: Scaling with high performance architecture<br>2'b11: Scaling with high performance architecture + fast |
| 25 | RO | 0x1 | SW_PPD_DEINT_EXIST<br>De-interlacing exits:<br>1'b0: No<br>1'b1: Yes |
| 24 | RO | 0x1 | SW_PPD_BLEND_EXIST<br>Alpha blending exists:<br>1'b0: No<br>1'b1: Yes |
| 23 | RO | 0x1 | SW_PPD_IBUFF_LEVEL<br>PP input buffering level:<br>1'b0: 1 MB input buffering is used<br>1'b1: 4 MB input buffering is used |
| 22:19 | RO | 0x0 | Reserved |
| 18 | RO | 0x1 | SW_PPD_OEN_VERSION<br>PP output endian version:<br>1'b0: Endian mode supported for other than RGB<br>1'b1: Endian mode supported for any output format |
| 17 | RO | 0x1 | SW_PPD_OBUFF_LEVEL<br>PP output buffering level:<br>1'b0: 1 unit output buffering is used<br>1'b1: 4 unit output buffering is used |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 16 | RO | 0x1 | SW_PPD_PP_EXIST<br>PPD exists:<br>1'b0: No<br>1'b1: Yes |
| 15:14 | RO | 0x1 | SW_PPD_IN_TILED_L<br>PPD input tiled mode support level<br>1'b0: Not supported<br>1'b1: 8x4 tile size supported |
| 13:11 | RO | 0x0 | Reserved |
| 10:0 | RO | 0x780 | SW_PPD_MAX_OWIDTH<br>Max supported PP output width in pixels |

**VDPU_SWREG101**

Address: Operational Base + offset (0x0194)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | Reserved |
| 0 | RW | 0x0 | Sw_soft_reset<br>Softreset pulse signal<br>Write to 1'b1, valid;<br>Write to 1'b0, invalid; |

**VDPU_SWREG102**

Address: Operational Base + offset (0x0198)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Vpu_work_cycle<br>Write initial/reset value in the begin of frame start, then will auto count base this value. |

**VDPU_SWREG103**

Address: Operational Base + offset (0x019c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Sw_axi_ddr_rdata<br>Axi ddr rdata num, the unit is byte. |

**VDPU_SWREG104**

Address: Operational Base + offset (0x01a0)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | Reserved |
| 0 | RW | 0x0 | Sw_axi_ddr_wdata<br>Vdpu write data byte num |

**VDPU_SWREG105**

Address: Operational Base + offset (0x01a4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | Reserved |
| 19:16 | RW | 0x0 | Mon_sig_sel1<br>Select the counter be used for which to calculate cycle num<br>4'b0000: Don't work.<br>4'b0001: Mv buffer hold back stream decode working cycles<br>4'b0010: The output fifo of cabac keep full cycles.<br>4'b0011: The Code stream parsing block working cycles.<br>4'b0100: Scd block can't write data to scd buffer cycles.<br>4'b0101: The speed of reconsitution and interpolation fast than reference frames fetch cycles.<br>4'b0110: The speed of reconsitution and interpolation slow than reference frames fetch cycles.<br>4'b0111: The cycles filter block hold back pred block.<br>4'b1000: The cycles of pred block waiting for Residual data.<br>4'b1001: The cycles of bus Related modules working. |
| 15:4 | RO | 0x000 | Reserved |
| 3:0 | RW | 0x0 | Mon_sig_sel0<br>Select the counter be used for which to calculate cycle num<br>4'b0000: Don't work.<br>4'b0001: Mv buffer hold back stream decode working cycles.<br>4'b0010: The output fifo of cabac keep full cycles.<br>4'b0011: The Code stream parsing block working cycles.<br>4'b0100: Scd block can't write data to scd buffer cycles.<br>4'b0101: The speed of reconsitution and interpolation fast than reference frames fetch cycles.<br>4'b0110: The speed of reconsitution and interpolation slow than reference frames fetch cycles.<br>4'b0111: The cycles filter block hold back pred block.<br>4'b1000: The cycles of pred block waiting for Residual data.<br>4'b1001: The cycles of bus Related modules working. |

**VDPU_SWREG106**

Address: Operational Base + offset (0x01a8)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Performance_mon_cnt0<br>The counter for the selected signal valid cycles which describe in swreg105[3:0].<br>Write initial/reset value |

**VDPU_SWREG107**

Address: Operational Base + offset (0x01ac)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Performance_mon_cnt1<br>The counter for the selected signal valid cycles which describe in swreg105[19:16]<br>Write initial/reset value. |

### 5.5.4 VDPU121 CACHE Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PREF_CACHE_VERSION | 0x0000 | W | 0xcac20101 | VERSION register |
| PREF_CACHE_SIZE | 0x0004 | W | 0x06110206 | L2 cache SIZE |
| PREF_CACHE_STATUS | 0x0008 | W | 0x00000000 | Status register |
| PREF_CACHE_COMMAND | 0x0010 | W | 0x00000000 | Command setting register |
| PREF_CACHE_CLEAR_PAGE | 0x0014 | W | 0x00000000 | Clear page register |
| PREF_CACHE_MAX_READS | 0x0018 | W | 0x0000001c | Maximum read register |
| PREF_CACHE_PERFCNT_SRC0 | 0x0020 | W | 0x00000000 | Performance counter 0 source register |
| PREF_CACHE_PERFCNT_VAL0 | 0x0024 | W | 0x00000000 | Performance counter 0 value register |
| PREF_CACHE_PERFCNT_SRC1 | 0x0028 | W | 0x00000000 | This register holds all the possible source values for Performance Counter 00: total clock cycles1: active clock cycles2: read transactions, master3: word reads, master4: read transactions, slave5: word reads, slave6: read hit, slave7: read misses, slave8: read invalidates, slave9: cacheable read transactions, slave10: bad hit nmber, slave |
| PREF_CACHE_PERFCNT_VAL1 | 0x002c | W | 0x00000000 | Performance counter 1 value register |

Rockchip Confidential

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

## 5.5.5 VDPU121 CACHE Detail Register Description

**PREF_CACHE_VERSION**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0xcac2 | product_id<br>Product id |
| 15:8 | RO | 0x01 | version_major<br>Version major |
| 7:0 | RO | 0x01 | version_minor<br>Version minor |

**PREF_CACHE_SIZE**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x06 | external_bus_width<br>Log2 external bus width in bits |
| 23:16 | RO | 0x11 | cache_size<br>Log2 cache size in bytes |
| 15:8 | RO | 0x02 | associativity<br>Log2 associativity |
| 7:0 | RO | 0x06 | line_size<br>Log2 line size in bytes |

**PREF_CACHE_STATUS**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x0 | Reserved |
| 1 | RO | 0x0 | data_busy<br>Set when the cache is busy handling data |
| 0 | RO | 0x0 | cmd_busy<br>Set when the cache is busy handling commands |

**PREF_CACHE_COMMAND**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0 | Reserved |
| 5:4 | RW | 0x0 | sw_addrb_sel<br>2'b00: To sel b[14:6]<br>2'b01: To sel b[15:9], b[7:6]<br>2'b10: To sel b[16:10], b[7:6]<br>2'b11: To sel b[17:11], b[7:6] |
| 3 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2:0 | WO | 0x0 | command<br>The possible command is<br>1'b1: Clear entire cache |

**PREF_CACHE_CLEAR_PAGE**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | WO | 0x00000000 | clear_page<br>Writing an address, invlidates all lines in that page from the cache. |

**PREF_CACHE_MAX_READS**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0 | Reserved |
| 4:0 | RW | 0x1c | max_reads<br>Limit the number of outstanding read transactions to this amount. |

**PREF_CACHE_PERFCNT_SRC0**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0 | Reserved |
| 3:0 | RW | 0x0 | perfcnt_src0<br>This register holds all the possible source values for Performance Counter 0.<br>4'd0: Total clock cycles<br>4'd1: Active clock cycles<br>4'd2: Read transactions, master<br>4'd3: Word reads, master<br>4'd4: Read transactions, slave<br>4'd5: Word reads, slave<br>4'd6: Read hit, slave<br>4'd7: Read misses, slave<br>4'd8: Read invalidates, slave<br>4'd9: Cacheable read transactions, slave<br>4'd10: Bad hit nmber, slave |

**PREF_CACHE_PERFCNT_VAL0**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | perfcnt_val0<br>Performance counter 0 value. |

Rockchip Confidencial

**PREF_CACHE_PERFCNT_SRC1**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0 | reserved |
| 3:0 | RW | 0x0 | perfcnt_src1<br>This register holds all the possible source values for Performance Counter 1.<br>4'd0: Total clock cycles<br>4'd1: Active clock cycles<br>4'd2: Read transactions, master<br>4'd3: Word reads, master<br>4'd4: Read transactions, slave<br>4'd5: Word reads, slave<br>4'd6: Read hit, slave<br>4'd7: Read misses, slave<br>4'd8: Read invalidates, slave<br>4'd9: Cacheable read transactions, slave<br>4'd10: Bad hit nmber, slave |

**PREF_CACHE_PERFCNT_VAL1**

Address: Operational Base + offset (0x002c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | perfcnt_val1<br>Performance counter 1 value. |

## 5.5.6 VEPU121 MMU Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VCODEC_MMU_DTE_ADDR | 0x0000 | W | 0x00000000 | MMU current page Table address. It is only can be written when MMU state is disable or page fault or mmu enable stall state |
| VCODEC_MMU_STATUS | 0x0004 | W | 0x00000018 | MMU status register |
| VCODEC_MMU_COMMAND | 0x0008 | W | 0x00000000 | MMU command register |
| VCODEC_MMU_PAGE_FAULT_ADDR | 0x000c | W | 0x00000000 | MMU logical address of last page fault |
| VCODEC_MMU_ZAP_ONE_LINE | 0x0010 | W | 0x00000000 | MMU Zap cache line register |
| VCODEC_MMU_INT_RAWSTAT | 0x0014 | W | 0x00000000 | MMU raw interrupt status register |

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VCODEC_MMU_INT_CLEAR | 0x0018 | W | 0x00000000 | MMU raw interrupt status register |
| VCODEC_MMU_INT_MASK | 0x001c | W | 0x00000000 | MMU raw interrupt status register |
| VCODEC_MMU_INT_STATUS | 0x0020 | W | 0x00000000 | MMU raw interrupt status register |
| VCODEC_MMU_AUTO_GATING | 0x0024 | W | 0x00000001 | mmu auto gating |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

### 5.5.7 VDPU121 MMU Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VCODEC_MMU_DTE_ADDR | 0x0000 | W | 0x00000000 | MMU current page Table address. It is only can be written when MMU state is disable or page fault or mmu enable stall state |
| VCODEC_MMU_STATUS | 0x0004 | W | 0x00000018 | MMU status register |
| VCODEC_MMU_COMMAND | 0x0008 | W | 0x00000000 | MMU command register |
| VCODEC_MMU_PAGE_FAULT_ADDR | 0x000c | W | 0x00000000 | MMU logical address of last page fault |
| VCODEC_MMU_ZAP_ONE_LINE | 0x0010 | W | 0x00000000 | MMU Zap cache line register |
| VCODEC_MMU_INT_RAWSTAT | 0x0014 | W | 0x00000000 | MMU raw interrupt status register |
| VCODEC_MMU_INT_CLEAR | 0x0018 | W | 0x00000000 | MMU raw interrupt status register |
| VCODEC_MMU_INT_MASK | 0x001c | W | 0x00000000 | MMU raw interrupt status register |
| VCODEC_MMU_INT_STATUS | 0x0020 | W | 0x00000000 | MMU raw interrupt status register |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VCODEC_MMU_AUTO_GATING | 0x0024 | W | 0x00000001 | mmu auto gating |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

## 5.5.8 VDPU121 MMU Detail Registers Description

### VCODEC_MMU_DTE_ADDR

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | MMU_DTE_ADDR<br>MMU current page Table address |

### VCODEC_MMU_STATUS

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:11 | RO | 0x000000 | Reserved |
| 10:6 | RO | 0x00 | PAGE_FAULT_BUS_ID<br>Index of master responsible for last page fault |
| 5 | RO | 0x0 | PAGE_FAULT_IS_WRITE<br>The direction of access for last page fault:<br>1'b0: Read<br>1'b1: Write |
| 4 | RO | 0x1 | REPLAY_BUFFER_EMPTY<br>1'b1:The MMU replay buffer is empty |
| 3 | RO | 0x1 | MMU_IDLE<br>The MMU is idle when accesses are being translated and there are no unfinished translated accesses.<br>1'b1: MMU is idle |
| 2 | RO | 0x0 | STAIL_ACTIVE<br>MMU stall mode currently enabled. The mode is enabled by command<br>1'b1: MMU is in stall active status |
| 1 | RO | 0x0 | PAGE_FAULT_ACTIVE<br>MMU page fault mode currently enabled. The mode is enabled by command.<br>1'b1: Page fault is active |
| 0 | RO | 0x0 | PAGING_ENABLED<br>1'b0: Paging is disabled<br>1'b1: Paging is enabled |

### VCODEC_MMU_COMMAND

Rockchip Confidencial

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | Reserved |
| 2:0 | WO | 0x0 | MMU_CMD<br>MMU_CMD. This can be:<br>3'd0: MMU_ENABLE_PAGING<br>3'd1: MMU_DISABLE_PAGING<br>3'd2: MMU_ENABLE_STALL<br>3'd3: MMU_DISABLE_STALL<br>3'd4: MMU_ZAP_CACHE<br>3'd5: MMU_PAGE_FAULT_DONE<br>3'd6: MMU_FORCE_RESET |

**VCODEC_MMU_PAGE_FAULT_ADDR**

Address: Operational Base + offset (0x000c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | PAGE_FAULT_ADDR<br>Address of last page fault |

**VCODEC_MMU_ZAP_ONE_LINE**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | WO | 0x00000000 | MMU_ZAP_ONE_LINE<br>ddress to be invalidated from the page table cache |

**VCODEC_MMU_INT_RAWSTAT**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | Reserved |
| 1 | RW | 0x0 | READ_BUS_ERROR<br>Read bus error status |
| 0 | RW | 0x0 | PAGE_FAULT<br>Page fault status |

**VCODEC_MMU_INT_CLEAR**

Address: Operational Base + offset (0x0018)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | Reserved |
| 1 | WO | 0x0 | READ_BUS_ERROR<br>Write 1 to clear read bus error |
| 0 | WO | 0x0 | PAGE_FAULT<br>Write 1 to page fault clear |

**VCODEC_MMU_INT_MASK**

Address: Operational Base + offset (0x001c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | Reserved |
| 1 | RW | 0x0 | READ_BUS_ERROR<br>Enable the read bus interrupt source when this bit is set to 1'b1 |
| 0 | RW | 0x0 | PAGE_FAULT<br>Enable the page fault interrupt source when this bit is set to 1'b1 |

**VCODEC_MMU_INT_STATUS**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | Reserved |
| 1 | RO | 0x0 | READ_BUS_ERROR<br>1'b1: Read bus error status |
| 0 | RO | 0x0 | PAGE_FAULT<br>1'b1: Page fault |

**VCODEC_MMU_AUTO_GATING**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | Reserved |
| 0 | RW | 0x1 | Mmu_auto_clkgating<br>When it is 1'b1, the mmu will auto gating it self |

## 5.5.9 VDPU381 Registers Summary

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKVDEC_SWREG0_ID | 0x0000 | W | 0x00000000 | ID register (read only) |
| RKVDEC_SWREG8_IN_OUT | 0x0020 | W | 0x00000000 | Data input and output endian setting and sys ctrl. |
| RKVDEC_SWREG9_DEC_MODE | 0x0024 | W | 0x00000000 | Dec mode |
| RKVDEC_SWREG10_DEC_E | 0x0028 | W | 0x00000000 | Decoder enable |
| RKVDEC_SWREG11_IMPORTANT_EN | 0x002c | W | 0x00000000 | Interrupt and decoder enable register. |
| RKVDEC_SWREG12_SENCODARY_EN | 0x0030 | W | 0x00000000 | Sys ctrl |
| RKVDEC_SWREG13_EN_MODE_SET | 0x0034 | W | 0x00000000 | Enable register. |
| RKVDEC_SWREG14_FBC_PARAM_SET | 0x0038 | W | 0x00000000 | Fbc parem set. |
| RKVDEC_SWREG15_STREAM_PARAM_SET | 0x003c | W | 0x00000000 | Stream param set |
| RKVDEC_SWREG16_STREAM_LEN | 0x0040 | W | 0x00000000 | Amount of stream bytes in the input buffer or amount ot rlc bytes in the input buffer. |
| RKVDEC_SWREG17_SLICE_NUMBER | 0x0044 | W | 0x00000000 | The current frame slice number |
| RKVDEC_SWREG18_Y_HOR_STRIDE | 0x0048 | W | 0x00000000 | Picture horizontal virtual stride. |
| RKVDEC_SWREG19_UV_HOR_STRIDE | 0x004c | W | 0x00000000 | Picture parametes |
| RKVDEC_SWREG20_FBC_PAYLOAD_OFFSET | 0x0050 | W | 0x00000000 | Register0004 Description |
| RKVDEC_SWREG20_Y_STRIDE | 0x0050 | W | 0x00000000 | The output picture y fac virtual stride.Suggest this register to config to even for advance ddr performance. |
| RKVDEC_SWREG21_ERROR_CTRL_SET | 0x0054 | W | 0x00000000 | Error sys ctrl |
| RKVDEC_SWREG22_ERR_ROI_CTU_OFFSET_START | 0x0058 | W | 0x00000000 | It will cal the error ctu num in the roi.It will include the st ctu and end ctu. |
| RKVDEC_SWREG23_ERR_ROI_CTU_OFFSET_END | 0x005c | W | 0x00000000 | It will cal the error ctu num in the roi.It will include the st ctu and end ctu. |
| RKVDEC_SWREG24_CABAC_ERROR_EN_LOWBITS | 0x0060 | W | 0x00000000 | Cabac error enable config. |
| RKVDEC_SWREG25_CABAC_ERROR_EN_HIGHBITS | 0x0064 | W | 0x00000000 | Cabac error enable high bits config. |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKVDEC_SWREG26_BLOCK_GATING_EN | 0x0068 | W | 0x00000000 | Block gating enable ctrl flag. |
| RKVDEC_SWREG27_CORE_SAFE_PIXELS | 0x006c | W | 0x00000000 | Colmv and recon report coord should be protect by safe pixels |
| RKVDEC_SWRE28_MULTIPLY_CORE_CTRL | 0x0070 | W | 0x00000000 | Multiply core work ctrl |
| RKVDEC_SWRE29_SCALE_DOWN_CTRL | 0x0074 | W | 0x00000000 | Scale down ctrl |
| RKVDEC_SWREG30_Y_SCALE_DOWN_TILE8X8_HOR_STRIDE | 0x0078 | W | 0x00000000 | Picture horizontal virtual stride. |
| RKVDEC_SWREG31_UV_SCALE_DOWN_TILE8X8_HOR_STRIDE | 0x007c | W | 0x00000000 | Picture parametes |
| RKVDEC_SWREG32_TIMEOUT_THRESHOLD | 0x0080 | W | 0x00000000 | Timeout threshold |
| RKVDEC_SWREG64_VP9_SET | 0x0100 | W | 0x00000000 | Vp9 compressed header offset.2014.11.19 del this register, because we can decode out sw_vp9_cprheader_offset from the stream. |
| RKVDEC_SWREG64_H26X_SET | 0x0100 | W | 0x00000000 | For H26x use |
| RKVDEC_SWREG65_CUR_POC | 0x0104 | W | 0x00000000 | Hevc & h264 & avs2 :the poc of cur picture.add vp9. |
| RKVDEC_SWREG66_H264_CUR_POC1 | 0x0108 | W | 0x00000000 | When cur is field, h264 cur poc for bottom field. |
| RKVDEC_SWREG67_VP9_SEGID_GRP0 | 0x010c | W | 0x00000000 | Vp9 segid syntax grp0.When write it is for last frame.When read it is for cur frame. |
| RKVDEC_SWREG67_REF0_POC | 0x010c | W | 0x00000000 | Hevc & h264 & avs2: The poc of reference picture index 0. |
| RKVDEC_SWREG68_VP9_SEGID_GRP1 | 0x0110 | W | 0x00000000 | Vp9 segid syntax grp1.When write it is for last frame.When read it is for cur frame. |
| RKVDEC_SWREG68_REF1_POC | 0x0110 | W | 0x00000000 | Hevc & h264 & avs2: The poc of reference picture index 1. |
| RKVDEC_SWREG69_VP9_SEGID_GRP2 | 0x0114 | W | 0x00000000 | Vp9 segid syntax grp2.When write it is for last frame.When read it is for cur frame. |
| RKVDEC_SWREG69_REF2_POC | 0x0114 | W | 0x00000000 | Hevc & h264 & avs2: The poc of reference picture index 2. |

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKVDEC_SWREG70_VP9_SEGID_GRP3 | 0x0118 | W | 0x00000000 | Vp9 segid syntax grp3.When write it is for last frame.When read it is for cur frame. |
| RKVDEC_SWREG70_REF3_POC | 0x0118 | W | 0x00000000 | Hevc & h264 & avs2: The poc of reference picture index 3. |
| RKVDEC_SWREG71_VP9_SEGID_GRP4 | 0x011c | W | 0x00000000 | Vp9 segid syntax grp4.When write it is for last frame.When read it is for cur frame. |
| RKVDEC_SWREG71_REF4_POC | 0x011c | W | 0x00000000 | Hevc & h264 & avs2: The poc of reference picture index 4. |
| RKVDEC_SWREG72_VP9_SEGID_GRP5 | 0x0120 | W | 0x00000000 | Vp9 segid syntax grp5.When write it is for last frame.When read it is for cur frame. |
| RKVDEC_SWREG72_REF5_POC | 0x0120 | W | 0x00000000 | Hevc & h264 & avs2: The poc of reference picture index 5. |
| RKVDEC_SWREG73_VP9_SEGID_GRP6 | 0x0124 | W | 0x00000000 | Vp9 segid syntax grp6.When write it is for last frame.When read it is for cur frame. |
| RKVDEC_SWREG73_REF6_POC | 0x0124 | W | 0x00000000 | Hevc & h264 & avs2: The poc of reference picture index 6. |
| RKVDEC_SWREG74_VP9_SEGID_GRP7 | 0x0128 | W | 0x00000000 | Vp9 segid syntax grp7.When write it is for last frame.When read it is for cur frame. |
| RKVDEC_SWREG74_REF7_POC | 0x0128 | W | 0x00000000 | Hevc & h264 & avs2: The poc of reference picture index 7. |
| RKVDEC_SWREG75_VP9_INFO_LASTFRAME | 0x012c | W | 0x00000000 | Vp9 info for lastframe. |
| RKVDEC_SWREG75_REF8_POC | 0x012c | W | 0x00000000 | Hevc & h264: The poc of reference picture index 8. |
| RKVDEC_SWREG76_VP9_CPRHEADER_CONFIG | 0x0130 | W | 0x00000000 | Vp9 compressed header config info. |
| RKVDEC_SWREG76_REF9_POC | 0x0130 | W | 0x00000000 | Hevc & h264: The poc of reference picture index 9. |
| RKVDEC_SWREG77_VP9_INTERCMD_NUM | 0x0134 | W | 0x00000000 | Vp9 intercmd num. |
| RKVDEC_SWREG77_REF10_POC | 0x0134 | W | 0x00000000 | Hevc & h264: The poc of reference picture index 10. |
| RKVDEC_SWREG78_VP9_STREAM_SIZE | 0x0138 | W | 0x00000000 | Vp9 last tile size. |
| RKVDEC_SWREG78_REF11_POC | 0x0138 | W | 0x00000000 | Hevc & h264: The poc of reference picture index 11. |
| RKVDEC_SWREG79_VP9_LASTF_Y_HOR_VIRSTRIDE | 0x013c | W | 0x00000000 | Vp9 last frame y horizontal virstride. |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKVDEC_SWREG79_REF12_POC | 0x013c | W | 0x00000000 | Hevc & h264: The poc of reference picture index 12. |
| RKVDEC_SWREG80_VP9_LASTF_UV_HOR_VIRSTRIDE | 0x0140 | W | 0x00000000 | Vp9 last frame uv horizontal virstride. |
| RKVDEC_SWREG80_REF13_POC | 0x0140 | W | 0x00000000 | Hevc & h264: The poc of reference picture index 13. |
| RKVDEC_SWREG81_VP9_GOLDENF_Y_HOR_VIRSTRIDE | 0x0144 | W | 0x00000000 | Vp9 golden frame y horizontal virstride. |
| RKVDEC_SWREG81_REF14_POC | 0x0144 | W | 0x00000000 | Hevc & h264: The poc of reference picture index 14. |
| RKVDEC_SWREG82_VP9_GOLDEN_UV_HOR_VIRSTRIDE | 0x0148 | W | 0x00000000 | Vp9 golden uv horizontal virstirde. |
| RKVDEC_SWREG82_REF15_POC | 0x0148 | W | 0x00000000 | H264: The poc of reference picture index 15.Hevc: Used for mvc.Vp9: Now is no use. |
| RKVDEC_SWREG83_VP9_ALTREFF_Y_HOR_VIRSTRIDE | 0x014c | W | 0x00000000 | Vp9 altref frame y horizontal virstride. |
| RKVDEC_SWREG83_REF16_POC | 0x014c | W | 0x00000000 | H264: The poc of reference picture index 16.Hevc & vp9: Now is no use. |
| RKVDEC_SWREG84_VP9_ALTREFF_UV_HOR_VIRSTRIDE | 0x0150 | W | 0x00000000 | Vp9 altreff uv horizontal virstirde.2015.10.23, change from 9bits to 10bits. |
| RKVDEC_SWREG84_REF17_POC | 0x0150 | W | 0x00000000 | H264: The poc of reference picture index 17.Hevc & vp9: Now is no use. |
| RKVDEC_SWREG85_VP9_LASTF_Y_VIRSTRIDE | 0x0154 | W | 0x00000000 | Last ref ystride |
| RKVDEC_SWREG85_REF18_POC | 0x0154 | W | 0x00000000 | H264: The poc of reference picture index 18.Hevc & vp9: Now is no use. |
| RKVDEC_SWREG86_VP9_GOLDEN_Y_VIRSTRIDE | 0x0158 | W | 0x00000000 | Vp9 golden y stride |
| RKVDEC_SWREG86_REF19_POC | 0x0158 | W | 0x00000000 | H264: The poc of reference picture index 19.Hevc & vp9: Now is no use. |
| RKVDEC_SWREG87_VP9_ALTREF_Y_VIRSTRIDE | 0x015c | W | 0x00000000 | Altref ref ystride |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKVDEC_SWREG87_REF20_POC | 0x015c | W | 0x00000000 | H264: The poc of reference picture index 20.Hevc & vp9: Now is no use. |
| RKVDEC_SWREG88_VP9_LREF_HOR_SCALE | 0x0160 | W | 0x00000000 | Horizontal scaling factor for last reference picture. |
| RKVDEC_SWREG88_REF21_POC | 0x0160 | W | 0x00000000 | H264: The poc of reference picture index 21.Hevc & vp9: Now is no use. |
| RKVDEC_SWREG89_VP9_LREF_VER_SCALE | 0x0164 | W | 0x00000000 | Vertical scaling factor for last reference picture. |
| RKVDEC_SWREG89_REF22_POC | 0x0164 | W | 0x00000000 | H264: The poc of reference picture index 22.Hevc & vp9: Now is no use. |
| RKVDEC_SWREG90_VP9_GREF_HOR_SCALE | 0x0168 | W | 0x00000000 | Horizontal scaling factor for golden reference picture. |
| RKVDEC_SWREG90_REF23_POC | 0x0168 | W | 0x00000000 | H264: The poc of reference picture index 23.Hevc & vp9: Now is no use. |
| RKVDEC_SWREG91_VP9_GREF_VER_SCALE | 0x016c | W | 0x00000000 | Vertical scaling factor for golden reference picture. |
| RKVDEC_SWREG91_REF24_POC | 0x016c | W | 0x00000000 | H264: The poc of reference picture index 24.Hevc & vp9: Now is no use. |
| RKVDEC_SWREG92_VP9_AREF_HOR_SCALE | 0x0170 | W | 0x00000000 | Horizontal scaling factor for alfter reference picture. |
| RKVDEC_SWREG92_REF25_POC | 0x0170 | W | 0x00000000 | H264: The poc of reference picture index 25.Hevc & vp9: Now is no use. |
| RKVDEC_SWREG93_VP9_AREF_VER_SCALE | 0x0174 | W | 0x00000000 | Vertical scaling factor for alfter reference picture. |
| RKVDEC_SWREG93_REF26_POC | 0x0174 | W | 0x00000000 | H264: The poc of reference picture index 26.Hevc & vp9: Now is no use. |
| RKVDEC_SWREG94_VP9_REF_DELTAS_LASTFRAME | 0x0178 | W | 0x00000000 | Vp9 ref deltas |
| RKVDEC_SWREG94_REF27_POC | 0x0178 | W | 0x00000000 | H264: The poc of reference picture index 27.Hevc & vp9: Now is no use. |
| RKVDEC_SWREG95_VP9_LAST_POC | 0x017c | W | 0x00000000 | VP9: The poc of last reference |
| RKVDEC_SWREG95_REF28_POC | 0x017c | W | 0x00000000 | H264: The poc of reference picture index 28.Hevc & vp9: Now is no use. |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKVDEC_SWREG96_VP9_GOLDEN_POC | 0x0180 | W | 0x00000000 | VP9: The poc of golden reference |
| RKVDEC_SWREG96_REF29_POC | 0x0180 | W | 0x00000000 | H264: The poc of reference picture index 29.Hevc & vp9: Now is no use. |
| RKVDEC_SWREG97_VP9_ALTREF_POC | 0x0184 | W | 0x00000000 | VP9: The poc of altref reference |
| RKVDEC_SWREG97_REF30_POC | 0x0184 | W | 0x00000000 | H264: The poc of reference picture index 30.Hevc & vp9: Now is no use. |
| RKVDEC_SWREG98_VP9_COL_REF_POC | 0x0188 | W | 0x00000000 | VP9: The poc of colpic reference |
| RKVDEC_SWREG98_REF31_POC | 0x0188 | W | 0x00000000 | H264: The poc of reference picture index 31.Hevc & vp9: Now is no use. |
| RKVDEC_SWREG99_H264_REG0_3_INFO | 0x018c | W | 0x00000000 | Rreference picture index 0~3 |
| RKVDEC_SWREG99_AVS2_REG0_3_INFO | 0x018c | W | 0x00000000 | Rreference picture index 0~3 |
| RKVDEC_SWREG99_VP9_PROB_REF_POC | 0x018c | W | 0x00000000 | VP9: The poc of reference prob |
| RKVDEC_SWREG99_HEVC_REF_VALID | 0x018c | W | 0x00000000 | Valid flag for picture index 0 ~14. |
| RKVDEC_SWREG100_AVS2_REG4_7_INFO | 0x0190 | W | 0x00000000 | Rreference picture index 4~7 |
| RKVDEC_SWREG100_H264_REG4_7_INFO | 0x0190 | W | 0x00000000 | Rreference picture index 4~7 |
| RKVDEC_SWREG100_VP9_SEGID_REF_POC | 0x0190 | W | 0x00000000 | VP9: The poc of reference segmentid |
| RKVDEC_SWREG101_H264_REG8_11_INFO | 0x0194 | W | 0x00000000 | Rreference picture index 8~11 |
| RKVDEC_SWREG102_H264_REG12_15_INFO | 0x0198 | W | 0x00000000 | Rreference picture index 12~15 |
| RKVDEC_SWREG103_HEVC_MVC0 | 0x019c | W | 0x00000000 | Hevc mvc config register. |
| RKVDEC_SWREG103_AVS2_CTRL_EXTRA | 0x019c | W | 0x00000000 | Avs2 ctrl register |
| RKVDEC_SWREG103_VP9_PROB_EN | 0x019c | W | 0x00000000 | Vp9_prob_en config. |
| RKVDEC_SWREG104_HEVC_MVC1 | 0x01a0 | W | 0x00000000 | Hevc MVC ctrl register. |
| RKVDEC_SWREG105_VP9CNT_UPD_EN_AVS2_HEADLEN | 0x01a4 | W | 0x00000000 | Avs2_head_len and Vp9 count update en. |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKVDEC_SWREG106_VP9_FRAME_WIDTH_LAST | 0x01a8 | W | 0x00000000 | Last frame frame_size_width. |
| RKVDEC_SWREG107_VP9_FRAME_HEIGHT_LAST | 0x01ac | W | 0x00000000 | Last frame frame_size_height. |
| RKVDEC_SWREG108_VP9_FRAME_WIDTH_GOLDEN | 0x01b0 | W | 0x00000000 | Golden frame_size_width. |
| RKVDEC_SWREG109_VP9_FRAME_HEIGHT_GOLDEN | 0x01b4 | W | 0x00000000 | Golden frame_size_height. |
| RKVDEC_SWREG110_VP9_FRAME_WIDTH_ALTREF | 0x01b8 | W | 0x00000000 | Alfter frame_size_width. |
| RKVDEC_SWREG111_VP9_FRAME_HEIGHT_ALTREF | 0x01bc | W | 0x00000000 | Alfter frame_size_height. |
| RKVDEC_SWREG112_ERROR_REF_INFO | 0x01c0 | W | 0x00000000 | Refer error is top or bot field flag. |
| RKVDEC_SWREG128_STRM_RLC_BASE | 0x0200 | W | 0x00000000 | The stream or rlc data base address. |
| RKVDEC_SWREG129_ERROR_INFO_BASE | 0x0204 | W | 0x00000000 | The base address of error info |
| RKVDEC_SWREG129_RLCWRITE_BASE | 0x0204 | W | 0x00000000 | The base address of rlcwrite base address.When frame is ready, it is the address of the end of rlcwrite address. |
| RKVDEC_SWREG130_DECOUT_BASE | 0x0208 | W | 0x00000000 | Base address of decoder output picture.Suggest this register to config to even for advance ddr performance. |
| RKVDEC_SWREG131_COLMV_CUR_BASE | 0x020c | W | 0x00000000 | Cur frame colmv output addr. |
| RKVDEC_SWREG132_ERROR_REF_BASE | 0x0210 | W | 0x00000000 | Error reference frame base address. |
| RKVDEC_SWREG133_RCB_INTRAR_BASE | 0x0214 | W | 0x00000000 | Rcb intra row base address, unit: 64byts align. |
| RKVDEC_SWREG134_RCB_TRANSDR_BASE | 0x0218 | W | 0x00000000 | Rcb transd row base address, unit: 64byts align. |
| RKVDEC_SWREG135_RCB_TRANSDC_BASE | 0x021c | W | 0x00000000 | Rcb transd col base address, unit: 64byts align. |
| RKVDEC_SWREG136_RCB_STRMDR_BASE | 0x0220 | W | 0x00000000 | Rcb stream row base address, unit: 64byts align. |
| RKVDEC_SWREG137_RCB_INTERR_BASE | 0x0224 | W | 0x00000000 | Rcb inter row base address, unit: 64byts align. |
| RKVDEC_SWREG138_RCB_INTERC_BASE | 0x0228 | W | 0x00000000 | Rcb inter col base address, unit: 64byts align. |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKVDEC_SWREG139_RCB_DBLKR_BASE | 0x022c | W | 0x00000000 | Rcb dblock row base address, unit: 64byts align. |
| RKVDEC_SWREG140_RCB_SAOR_BASE | 0x0230 | W | 0x00000000 | Rcb sao row base address, unit: 64byts align. |
| RKVDEC_SWREG141_RCB_FBCR_BASE | 0x0234 | W | 0x00000000 | Rcb fbc row base address, unit: 64byts align. |
| RKVDEC_SWREG142_RCB_FILTC_COL_BASE | 0x0238 | W | 0x00000000 | Rcb filter col base address, unit: 64byts align. |
| RKVDEC_SWREG160_VP9_DELTA_PROB_BASE | 0x0280 | W | 0x00000000 | The base address of prob. |
| RKVDEC_SWREG161_PPS_BASE | 0x0284 | W | 0x00000000 | The base address of pps. |
| RKVDEC_SWREG161_AVS2_HEAD_BASE | 0x0284 | W | 0x00000000 | The base address of avs2 head. |
| RKVDEC_SWREG162_VP9_LAST_PROB_BASE | 0x0288 | W | 0x00000000 | It only used when hardware parse prob.This base addr is for last prob. |
| RKVDEC_SWREG163_RPS_BASE | 0x028c | W | 0x00000000 | The base address of rps. |
| RKVDEC_SWREG164_REF0_BASE | 0x0290 | W | 0x00000000 | Base address for reference picture index0. |
| RKVDEC_SWREG164_VP9_REFERLAST_BASE | 0x0290 | W | 0x00000000 | Base address for reference picture.Suggest this register to config to even for advance ddr performance. |
| RKVDEC_SWREG165_REF1_BASE | 0x0294 | W | 0x00000000 | Base address for reference picture index1. |
| RKVDEC_SWREG165_VP9_REFERGOLDEN_BASE | 0x0294 | W | 0x00000000 | Base address for golden picture.Suggest this register to config to even for advance ddr performance. |
| RKVDEC_SWREG166_REF2_BASE | 0x0298 | W | 0x00000000 | Base address for reference picture index2. |
| RKVDEC_SWREG166_VP9_REFERALFTER_BASE | 0x0298 | W | 0x00000000 | Base address for alfter picture.Suggest this register to config to even for advance ddr performance. |
| RKVDEC_SWREG167_VP9COUNT_BASE | 0x029c | W | 0x00000000 | Vp9 count base addr. |
| RKVDEC_SWREG167_REF3_BASE | 0x029c | W | 0x00000000 | Base address for reference picture index3. |
| RKVDEC_SWREG168_VP9_SEGIDLAST_BASE | 0x02a0 | W | 0x00000000 | Base address for last frame segment id. |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKVDEC_SWREG168_REF4_BASE | 0x02a0 | W | 0x00000000 | Base address for reference picture index4. |
| RKVDEC_SWREG169_AVP9_SEGIDCUR_BASE | 0x02a4 | W | 0x00000000 | Base address for cur frame segment id. |
| RKVDEC_SWREG169_REF5_BASE | 0x02a4 | W | 0x00000000 | Base address for reference picture index5. |
| RKVDEC_SWREG170_VP9_REFCOLMV_BASE | 0x02a8 | W | 0x00000000 | Vp9 refcolmv base addr. |
| RKVDEC_SWREG170_REF6_BASE | 0x02a8 | W | 0x00000000 | Base address for reference picture index6. |
| RKVDEC_SWREG171_VP9_INTERCMD_BASE | 0x02ac | W | 0x00000000 | Inter cmd base addr. |
| RKVDEC_SWREG171_REF7_BASE | 0x02ac | W | 0x00000000 | Base address for reference picture index7. |
| RKVDEC_SWREG172_VP9_UPDATE_PROB_WR_BASE | 0x02b0 | W | 0x00000000 | Hardware parse prob: Used as vp9 prob write base. |
| RKVDEC_SWREG172_H26X_REF8_BASE | 0x02b0 | W | 0x00000000 | Base address for reference picture index8. |
| RKVDEC_SWREG173_H26X_REF9_BASE | 0x02b4 | W | 0x00000000 | Base address for reference picture index9. |
| RKVDEC_SWREG174_H26X_REF10_BASE | 0x02b8 | W | 0x00000000 | Base address for reference picture index10. |
| RKVDEC_SWREG175_H26X_REF11_BASE | 0x02bc | W | 0x00000000 | Base address for reference picture index11. |
| RKVDEC_SWREG176_H26X_REF12_BASE | 0x02c0 | W | 0x00000000 | Base address for reference picture index12. |
| RKVDEC_SWREG177_H26X_REF13_BASE | 0x02c4 | W | 0x00000000 | Base address for reference picture index13. |
| RKVDEC_SWREG178_H26X_REF14_BASE | 0x02c8 | W | 0x00000000 | Base address for reference picture index14. |
| RKVDEC_SWREG179_H26X_REF15_BASE | 0x02cc | W | 0x00000000 | Base address for reference picture index15. |
| RKVDEC_SWREG180_SCANLIST_ADDR | 0x02d0 | W | 0x00000000 | The addr for scanlist table. |
| RKVDEC_SWREG181_COLMV_REF0_BASE | 0x02d4 | W | 0x00000000 | Ref0 frame colmv base addr. |
| RKVDEC_SWREG182_COLMV_REF1_BASE | 0x02d8 | W | 0x00000000 | Ref1 frame colmv base addr. |
| RKVDEC_SWREG183_COLMV_REF2_BASE | 0x02dc | W | 0x00000000 | Ref2 frame colmv base addr. |
| RKVDEC_SWREG184_COLMV_REF3_BASE | 0x02e0 | W | 0x00000000 | Ref3 frame colmv base addr. |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKVDEC_SWREG185_COLMV_REF4_BASE | 0x02e4 | W | 0x00000000 | Ref4 frame colmv base addr. |
| RKVDEC_SWREG186_COLMV_REF5_BASE | 0x02e8 | W | 0x00000000 | Ref5 frame colmv base addr. |
| RKVDEC_SWREG187_COLMV_REF6_BASE | 0x02ec | W | 0x00000000 | Ref6 frame colmv base addr. |
| RKVDEC_SWREG188_COLMV_REF7_BASE | 0x02f0 | W | 0x00000000 | Ref7 frame colmv base addr. |
| RKVDEC_SWREG189_COLMV_REF8_BASE | 0x02f4 | W | 0x00000000 | Ref8 frame colmv base addr. |
| RKVDEC_SWREG190_COLMV_REF9_BASE | 0x02f8 | W | 0x00000000 | Ref9 frame colmv base addr. |
| RKVDEC_SWREG191_COLMV_REF10_BASE | 0x02fc | W | 0x00000000 | Ref10 frame colmv base addr. |
| RKVDEC_SWREG192_COLMV_REF11_BASE | 0x0300 | W | 0x00000000 | Ref11 frame colmv base addr. |
| RKVDEC_SWREG193_COLMV_REF12_BASE | 0x0304 | W | 0x00000000 | Ref12 frame colmv base addr. |
| RKVDEC_SWREG194_COLMV_REF13_BASE | 0x0308 | W | 0x00000000 | Ref13 frame colmv base addr. |
| RKVDEC_SWREG195_COLMV_REF14_BASE | 0x030c | W | 0x00000000 | Ref14 frame colmv base addr. |
| RKVDEC_SWREG196_COLMV_REF15_BASE | 0x0310 | W | 0x00000000 | Ref15 frame colmv base addr. |
| RKVDEC_SWREG197_CABACTBL_BASE | 0x0314 | W | 0x00000000 | Hevc & H264: The base address of cabac table. |
| RKVDEC_SWREG198_SCALE_DOWN_LUMA_BASE | 0x0318 | W | 0x00000000 | Hevc & H264: The base address of cabac table. |
| RKVDEC_SWREG199_SCALE_DOWN_CHRO_BASE | 0x031c | W | 0x00000000 | The base address of scale down chro base |
| RKVDEC_SWREG200_REF_POC_HIGHBIT_P0 | 0x0320 | W | 0x00000000 | Sw_ref_poc_highbituse for separate top/bot field or multi-view stream in multi-core casevp9 not used |
| RKVDEC_SWREG201_REF_POC_HIGHBIT_P1 | 0x0324 | W | 0x00000000 | Sw_ref_poc_highbituse for separate top/bot field or multi-view stream in multi-core casevp9 not used |
| RKVDEC_SWREG202_REF_POC_HIGHBIT_P2 | 0x0328 | W | 0x00000000 | Sw_ref_poc_highbituse for separate top/bot field or multi-view stream in multi-core casevp9 not used |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKVDEC_SWREG203_REF_POC_HIGHBIT_P3 | 0x032c | W | 0x00000000 | Sw_ref_poc_highbituse for separate top/bot field or multi-view stream in multi-core casevp9 not used |
| RKVDEC_SWREG204_CUR_POC_HIGHBIT | 0x0330 | W | 0x00000000 | Sw_cur_poc_highbituse for separate top/bot field or multi-view stream in multi-core casevp9 not used |
| RKVDEC_SWREG224_STA_INT | 0x0380 | W | 0x00000000 | Decoder status |
| RKVDEC_SWREG225_STA_ERR_INFO | 0x0384 | W | 0x00000000 | Error info status. |
| RKVDEC_SWREG226_STA_CABAC_ERROR_STATUS | 0x0388 | W | 0x00000000 | Cabac error status. |
| RKVDEC_SWREG227_STA_COLMV_ERROR_REF_PICIDX | 0x038c | W | 0x00000000 | Colmv error ref picidx. |
| RKVDEC_SWREG228_STA_CABAC_ERROR_CTU_OFFSET | 0x0390 | W | 0x00000000 | Cabac error ctu offset. |
| RKVDEC_SWREG229_STA_SAOWR_CTU_OFFSET | 0x0394 | W | 0x00000000 | When there is any error, it is for the position of sao decode output to busifd. |
| RKVDEC_SWREG230_STA_SLICE_DEC_NUM | 0x0398 | W | 0x00000000 | Slice dec num |
| RKVDEC_SWREG231_STA_FRAME_ERROR_CTU_NUM | 0x039c | W | 0x00000000 | H264 and hevc error ctu number. |
| RKVDEC_SWREG232_STA_ERROR_PACKET_NUM | 0x03a0 | W | 0x00000000 | Error packet number |
| RKVDEC_SWREG233_STA_ERR_CTU_NUM_IN_ROI | 0x03a4 | W | 0x00000000 | The error ctu num in roi. |
| RKVDEC_SWREG256_DEBUG_PERF_LATENCY_CTRL0 | 0x0400 | W | 0x00000000 | Axi performance latency module contrl register. |
| RKVDEC_SWREG257_DEBUG_PERF_LATENCY_CTRL1 | 0x0404 | W | 0x00000000 | Debug perf latency ctrl. |
| RKVDEC_SWREG258_DEBUG_PERF_RD_MAX_LATENCY_NUM | 0x0408 | W | 0x00000000 | Read max latency number. |
| RKVDEC_SWREG259_PERF_RD_LATENCY_SAMP_NUM | 0x040c | W | 0x00000000 | The number of bigger than configed threshold value. |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKVDEC_SWREG260_DEBUG_PERF_RD_LATENCY_ACC_SUM | 0x0410 | W | 0x00000000 | Total sample number. |
| RKVDEC_SWREG261_DEBUG_PERF_RD_AXI_TOTAL_BYTE | 0x0414 | W | 0x00000000 | The bandwidth of total read bytes. |
| RKVDEC_SWREG262_DEBUG_PERF_WR_AXI_TOTAL_BYTE | 0x0418 | W | 0x00000000 | The bandwidth of total write bytes. |
| RKVDEC_SWREG263_DEBUG_PERF_WORKING_CNT | 0x041c | W | 0x00000000 | The total running cycle of current frame. |
| RKVDEC_SWREG265_DEBUG_PERF_SEL | 0x0424 | W | 0x00000000 | Performance montor ctrl. |
| RKVDEC_SWREG266_DEBUG_PERF_CNT0 | 0x0428 | W | 0x00000000 | Performance count value0. |
| RKVDEC_SWREG267_DEBUG_PERF_CNT1 | 0x042c | W | 0x00000000 | Performance count value1. |
| RKVDEC_SWREG268_DEBUG_PERF_CNT2 | 0x0430 | W | 0x00000000 | Performance count value2. |
| RKVDEC_SWREG269_VP9_ERROR_INFO | 0x0434 | W | 0x00000000 | Performance count value2. |
| RKVDEC_SWREG270_DEBUG_QOS_CTRL | 0x0438 | W | 0x00000000 | AXI bus hurry ctrl. |
| RKVDEC_SWREG271_DEBUG_WAIT_CYCLE_QOS | 0x043c | W | 0x00000000 | Hw find sw_wr_wait_cycle_qos cycle can't wr to ddr, it will give hurry. |
| RKVDEC_SWREG272_DEBUG_INT | 0x0440 | W | 0x00000000 | Debug info |
| RKVDEC_SWREG273_STA_B_FRAME_FLAG | 0x0444 | W | 0x00000000 | STA B Frame flag |
| RKVDEC_SWREG274_PIX_RANGE_Y | 0x0448 | W | 0x00000000 | It will montior current frame max or min pix value. |
| RKVDEC_SWREG275_PIX_RANGE_U | 0x044c | W | 0x00000000 | It will montior current frame max or min pix value. |
| RKVDEC_SWREG276_PIX_RANGE_V | 0x0450 | W | 0x00000000 | It will montior current frame max or min pix value. |
| RKVDEC_SWREG277_ERROR_SPREAD_NUM | 0x0454 | W | 0x00000000 | Error spread block numbers |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

### 5.5.10 VDPU381 Detail Register Description

**RKVDEC_SWREG0_ID**

Address: Operational Base + offset (0x0000)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | prod_num<br>Prod code |
| 15:8 | RO | 0x00 | major_ver<br>Major verision |
| 7:0 | RO | 0x00 | minor_ver<br>Minor version |

**RKVDEC_SWREG8_IN_OUT**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x0 | Reserved |
| 9 | RW | 0x0 | sw_out_swap64_e<br>May be used for 64 or 128 bit environment.<br>1'b0: No swapping of 64 bit words.<br>1'b1: 64 bit data words are swapped. |
| 8 | RW | 0x0 | sw_out_cbcr_swap<br>1'b0: Cb(u) is in the lower address, cr(v) is in the higher address.<br>1'b1: Cb(u) is in the higher address,cr(v) is in the lower address.<br>Sw_in_cbcr_swap is the same with sw_out_cbcr_swap. |
| 7 | RW | 0x0 | sw_out_swap32_e<br>May be used for 64 or 128 bit environment.<br>1'b0: No swapping of 32 bit words.<br>1'b1: 32 bit data words are swapped. |
| 6 | RW | 0x0 | sw_out_endian<br>1'b0: Little endian<br>1'b1: Big endian<br>For litter enadian, a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address. |
| 5 | RW | 0x0 | sw_str_swap64_e<br>May be used for 128 bit environment.<br>1'b0: No swapping of 64 bit words.<br>1'b1: 64 bit data words are swapped. |
| 4 | RW | 0x0 | sw_str_swap32_e<br>May be used for 64 or 128 bit environment.<br>1'b0: No swapping of 32 bit words<br>1'b1: 32 bit data words are swapped. |
| 3 | RW | 0x0 | sw_str_endian<br>1'b0: Little endian<br>1'b1: Big endian<br>For litter enadian, a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address. |
| 2 | RW | 0x0 | sw_in_swap64_e<br>May be used for 128 bit environment.<br>1'b0: No swapping of 64 bit words.<br>1'b1: 64 bit data words are swapped. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | sw_in_swap32_e<br>May be used for 64 or 128 bit environment.<br>1'b0: No swapping of 32 bit words.<br>1'b1: 32 bit data words are swapped. |
| 0 | RW | 0x0 | sw_in_endian<br>1'b0: Little endian<br>1'b1: Big endian<br>For litter enadian, a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address. |

**RKVDEC_SWREG9_DEC_MODE**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x0 | Reserved |
| 9:0 | RW | 0x000 | sw_dec_mode<br>10'd0: Hevc<br>10'd1: H264<br>10'd2: Vp9<br>10'd3: Avs2<br>Other: Reversed |

**RKVDEC_SWREG10_DEC_E**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x0 | Reserved |
| 0 | RW | 0x0 | sw_dec_e<br>Decoder enable. Setting this bit high will start the decoding operation. HW will reset this when the picture is decoded ready or bus error or time out interrupt is given for all decode format.<br>HW will reset this when picture is processed stream error for vp9 & hevc & (h264 when sw_h264_error_mode is 1'b0). |

**RKVDEC_SWREG11_IMPORTANT_EN**

Address: Operational Base + offset (0x002c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x0 | Reserved |
| 24 | RW | 0x0 | sw_pix_range_det_e<br>1'b0: Pix range detect disable<br>1'b1: Pix range detect enable |
| 23:22 | RO | 0x0 | Reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 21 | RW | 0x0 | sw_force_softreset_valid<br>When sw_force_softreset_valid is 1'b1, sw_softrst_en will always be valid to the system no matter that whether the axi bus is idle.<br>When sw_force_softreset_valid is 1'b0, sw_softrst_en will only be valid when the axi bus is idle.<br>We suggest such bit always be config to 0 except when soft want to force reset. |
| 20 | RW | 0x0 | sw_softrst_en_p<br>Softreset enable signal, write 1 to soft reset, write 0 invalid, puls register. |
| 19:11 | RO | 0x0 | Reserved |
| 10 | RW | 0x0 | sw_dec_e_rewrite_valid<br>Sw_dec_e rewrite valid signal, maybe for only when buffer empty, restart the decoder use. |
| 9:7 | RO | 0x0 | Reserved |
| 6 | RW | 0x0 | sw_buf_empty_en<br>Buffer empty interrupt enable. |
| 5 | RW | 0x0 | sw_dec_timeout_e<br>If enabled HW may return timeout interrupt in case HW gets stucked while decoding picture. |
| 4 | RW | 0x0 | sw_dec_irq_dis<br>When hight, there are no interrupts concerning decoder from HW. Polling must be used to see the interrupt status. |
| 3 | RO | 0x0 | Reserved |
| 2 | RW | 0x0 | sw_dec_e_strmd_clkgate_dis<br>In streamd module, there contains HEVC, H264, VP9, AVS2 modules, when it is 1'b1, these modules will no auto clkgate. |
| 1 | RW | 0x0 | sw_dec_clkgate_e<br>1'b0: Clock is running for all structures.<br>1'b1: Clock is gated for decoder structures that are not used. |
| 0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG12_SENCODARY_EN**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:11 | RO | 0x0 | Reserved |
| 10 | RW | 0x0 | sw_error_cfg_wr_disable<br>default is write ltb cfg to ddr when error occur<br>1'b0: Hardware will write ltb cfg to ddr when error occur.<br>1'b1: Hardware do not write ltb cfg to ddr when error occur. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RW | 0x0 | sw_scale_down_en<br>scale down used 8x8 tile mode output.<br>it support 1/2 scale down ratio for hor or vrz.<br>1'b0:Disable scale down function.<br>1'b1:Enable scale down function,scale down en can be enable only when fbc work mode be actived. |
| 8 | RW | 0x0 | sw_scanlist_addr_valid_en<br>1'b0 : Scanlsit addr get from pps table.<br>1'b1 : Scanlist addr get from config. |
| 7 | RW | 0x0 | sw_error_auto_rst_disable<br>default is auto reset<br>1'b0: Hardware will auto reset when error occur.<br>1'b1: Wait software process reset when error occur. |
| 6 | RW | 0x0 | sw_collect_info_en<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | sw_error_info_en<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | sw_buspr_slot_disable<br>1'b1: Bus prefetch slot manage disable. |
| 3 | RO | 0x0 | Reserved |
| 2 | RW | 0x0 | sw_fbc_e<br>1'b0: Fbc disable<br>1'b1: Fbc enable |
| 1 | RW | 0x0 | sw_colmv_compress_en<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG13_EN_MODE_SET**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | sw_filter_outbuf_mode<br>Active at sw_fbc_e=1<br>1'b0: Fbchead write ddr with 64byte align<br>1'b1: Fbchead write ddr not almost 64byte align |
| 30 | RO | 0x0 | Reserved |
| 29 | RW | 0x0 | sw_rd_ctrl_prior_mode<br>1'b0 : Rcb data prior higher than referance data<br>1'b1 : Rcb data prior lower than referance data |
| 28 | RW | 0x0 | sw_rd_prior_mode<br>1'b0 : Used default mode<br>1'b1 : Used ctrl mode |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 27 | RW | 0x0 | sw_frame_end_err_rst_flag<br>sw_error_mode should be 1 at first<br>1'b0: When there is stream/inter_ref error, and hardware decode frame end, will not be reset<br>1'b1: When there is stream/inter_ref error, and hardware decode frame end, will be reset |
| 26 | RW | 0x0 | sw_right_auto_rst_disable<br>Secoder each frame end with auto reset select, but mmu do not auto reset,default is auto reset<br>1'b0:Decoder each frame end with auto reset enable<br>1'b1:Decoder each frame end with auto reset disable |
| 25 | RO | 0x0 | Reserved |
| 24 | RW | 0x0 | sw_cur_pic_is_idr<br>All frame is I frame flag. |
| 23:22 | RO | 0x0 | Reserved |
| 21 | RW | 0x0 | sw_ycacherd_prior<br>1'b0: Y cacherd prior is higher than uv.<br>1'b1: Y cache prior is equal than uv.<br>Fbc mode: Sw_head_prior_high_en.<br>1'b0: Fbc head fetch data prior normal.<br>1'b1: Fbc head fetch data prior high. |
| 20:19 | RO | 0x0 | Reserved |
| 18 | RW | 0x0 | sw_error_mode<br>For H264/hevc/avs2:<br>1'b0: When there is any error, the hardware will stop the decoder and reset itself.<br>1'b1: When there is any error, the hardware will start error proc and wait frame end.<br>It is recommend that when vp9, it is configed to 1'b0. |
| 17:14 | RO | 0x0 | Reserved |
| 13 | RW | 0x0 | sw_fbc_output_wr_disable<br>1'b0 : Fbc output picture data will be write to ddr when sw_fbc_e=1<br>1'b1 : Fbc output picture data will not be write to ddr even if sw_fbc_e=1 |
| 12 | RW | 0x0 | sw_allow_not_wr_unref_bframe<br>1'b0: If dec not referance b frame, will write to ddr.<br>1'b1: If dec not referance b frame, will not write to ddr.<br>If wan't to set this bit to 1, should set sw_scl_down_en=1 also.<br>It only used in hevc and unsupport tile mode. |
| 11:7 | RO | 0x0 | Reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | sw_stmerror_waitdecfifo_empty<br>When it is 1'b0, the stream error process will no wait the ca2decfifo empty; when it is 1'b1, the stream error process will wait the ca2decfifo empty, when sw_dec_mode is HEVC and VP9.<br>It always take effect. When sw_dec_mode is H264.<br>It only take effect, when sw_h264_error_mode is 1'b0. |
| 5:4 | RO | 0x0 | Reserved |
| 3 | RW | 0x0 | sw_dec_commonirq_mode<br>1'b0: In H264 and vp9 mode, the interrrupt will wait strmd end pulse.<br>1'b1: In H264 and vp9 mode, the interrupt will not wait strmd end plus. |
| 2 | RO | 0x0 | Reserved |
| 1 | RW | 0x0 | sw_req_timeout_rst_sel<br>use for multicore pu/colmv offset req timeout reset enable select active when the counter is 16'hffff<br>1'b0: Req timeout reset enable<br>1'b1: Req timeout reset disable |
| 0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG14_FBC_PARAM_SET**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0 | Reserved |
| 6 | RW | 0x0 | sw_fbc_h264_exten_4or8_flag<br>It was h264 mbaff flag.<br>1'b0: Not mabff<br>1'b1: Mabff |
| 5:4 | RO | 0x0 | Reserved |
| 3 | RW | 0x0 | sw_allow_16x8_cp_flag<br>1'b0: Not allow<br>1'b1: Allow<br>The config value is depend on vop work mode. |
| 2:1 | RO | 0x0 | Reserved |
| 0 | RW | 0x0 | sw_fbc_force_uncompress<br>1'b0: Allow fbce compress yuv block.<br>1'b1: Force all yuv block use uncompress mode. |

**RKVDEC_SWREG15_STREAM_PARAM_SET**

Address: Operational Base + offset (0x003c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x0 | Reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:5 | RW | 0x00 | sw_strm_start_bit<br>Exact bit of streamd start word where decoding can be started (asosiates with sw_str_rlc_base). |
| 4:2 | RO | 0x0 | Reserved |
| 1 | RW | 0x0 | sw_rlc_mode<br>1'b0: Hw decodes video from bit stream.<br>1'b1: Hw decodes video from RLC input data. |
| 0 | RW | 0x0 | sw_rlc_mode_direct_write<br>Cabac decode output direct write enable.<br>When this bit is enable, all the module other than cabac and busifd are not work. |

**RKVDEC_SWREG16_STREAM_LEN**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_stream_len<br>Amount of stream 8bits in the input buffer, byte unitL.<br>The max of sw_stream_len: min(65536x65536x1.5x1.5,4G) = 4G. |

**RKVDEC_SWREG17_SLICE_NUMBER**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x0 | Reserved |
| 24:0 | RW | 0x0000000 | sw_slice_num<br>Hevc: Slice number in a frame (0~199, when it is 0, it real means 1 slice in a frame), just only used for rps read.<br>The meaning from count from 1, so it will be in 1~200.<br>H264: Slice number in a frame (0~4095, when it is 1, it real means 1 slice in a frame).<br>Vp9: No use. |

**RKVDEC_SWREG18_Y_HOR_STRIDE**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_y_hor_virstride<br>Picture horizontal virtual stride (the unit is 128bit).<br>The max is (4096x1.5 + 128) /16 = 0x188.<br>Suggest this register to config to even for advance ddr performance.<br>Fbc mode: Used for head hor virstirde. |

Rockchip Confidencial

**RKVDEC_SWREG19_UV_HOR_STRIDE**

Address: Operational Base + offset (0x004c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_uv_hor_virstride<br>Picture horizontal virtual stride (the unit is 128bit).<br>The max is (4096x1.5 + 128) /16 = 0x188.<br>Suggest this register to config to even for advance ddr performance. |

**RKVDEC_SWREG20_FBC_PAYLOAD_OFFSET**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_fbc_payload_base_addr<br>The offset should be 128bit align.<br>[Note]: The payload will be store in the base: Sw_decout_base + Sw_payload_st_offset. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG20_Y_STRIDE**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | Reserved |
| 27:0 | RW | 0x0000000 | sw_y_virstride<br>The output picture y virtual stride (the unit is 128bit).<br>The max:min( (65536x1.5 +128) x 65536,4G) = 4G.<br>We can know the sw_uvout_base = sw_decout_base + (sw_y_virstride <<4). |

**RKVDEC_SWREG21_ERROR_CTRL_SET**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x0 | Reserved |
| 24 | RW | 0x0 | sw_roi_error_ctu_cal_en<br>1'b0: Disable<br>1'b1: Enable |
| 23:13 | RO | 0x0 | Reserved |
| 12 | RW | 0x0 | sw_error_inter_pred_cross_slice<br>1'b0 : Inter mv pred can't cross slice boundary<br>1'b1 : Inter mv pred will cross slice boundary<br>it only be used when Sw_inter_error_prc_mode=0 |
| 11:9 | RO | 0x0 | Reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | sw_error_spread_e<br>1'b0: Error info spread disable.<br>1'b1: Error info spread enable.<br>error info spread unit is ctu size<br>H264/HEVC/AVS2 avaliable |
| 7:3 | RW | 0x00 | Sw_picidx_replace<br>Hevc:<br>[4:1]: Default pic idx<br>[0]: Invalid<br>H264:<br>[4:1]: Default pic idx<br>[0]: Field mode, 0 is top field. |
| 2 | RW | 0x0 | Sw_error_deb_en<br>1'b0: Disable<br>1'b1: Enable<br>Only valid when sw_error_prc_intra_mode_sel = 1'b1. |
| 1 | RW | 0x0 | Sw_error_intra_mode<br>1'b0: Use inter mode to proc error ctu.<br>1'b1: Use intra mode to proc error ctu. |
| 0 | RW | 0x0 | Sw_inter_error_prc_mode<br>1'b0: Mv used pred.<br>1'b1: Mv=0, and sw_error_ref_base will be used. |

**RKVDEC_SWREG22_ERR_ROI_CTU_OFFSET_START**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | Reserved |
| 27:16 | RW | 0x000 | sw_roi_y_ctu_offset_st<br>The start offset of ctu_y when roi check. |
| 15:12 | RO | 0x0 | Reserved |
| 11:0 | RW | 0x000 | sw_roi_x_ctu_offset_st<br>The start offset of ctu_x when roi check. |

**RKVDEC_SWREG23_ERR_ROI_CTU_OFFSET_END**

Address: Operational Base + offset (0x005c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | Reserved |
| 27:16 | RW | 0x000 | sw_roi_y_ctu_offset_end<br>The end offset of ctu_y when roi check. |
| 15:12 | RO | 0x0 | Reserved |
| 11:0 | RW | 0x000 | sw_roi_x_ctu_offset_end<br>The end offset of ctu_x when roi check. |

**RKVDEC_SWREG24_CABAC_ERROR_EN_LOWBITS**

Rockchip Confidencial

Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_cabac_error_en_lowbits<br>Cabac error enable config. |

**RKVDEC_SWREG25_CABAC_ERROR_EN_HIGHBITS**

Address: Operational Base + offset (0x0064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | Reserved |
| 29:0 | RW | 0x00000000 | sw_cabac_error_en_highbits<br>Cabac error enable high bits config. |

**RKVDEC_SWREG26_BLOCK_GATING_EN**

Address: Operational Base + offset (0x0068)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | sw_reg_cfg_gating_en<br>1'b0: Disable<br>1'b1: Enable auto gating |
| 30:18 | RO | 0x0 | Reserved |
| 17 | RW | 0x0 | sw_cru_auto_gating_e<br>1'b0: Disable<br>1'b1: Enable auto gating |
| 16 | RW | 0x0 | sw_sram_auto_gating_e<br>1'b0: Disable<br>1'b1: Enable auto gating |
| 15:12 | RO | 0x0 | Reserved |
| 11 | RW | 0x0 | sw_transd_auto_gating_e<br>1'b0: Disable<br>1'b1: Enable auto gating |
| 10 | RW | 0x0 | sw_mc_auto_gating_e<br>1'b0: Disable<br>1'b1: Enable auto gating |
| 9 | RW | 0x0 | sw_intra_auto_gating_e<br>1'b0: Disable<br>1'b1: Enable auto gating |
| 8 | RW | 0x0 | sw_dec_ctrl_auto_gating_e<br>1'b0: Disable<br>1'b1: Enable auto gating |
| 7:5 | RO | 0x0 | Reserved |
| 4 | RW | 0x0 | sw_busifd_auto_gating_e<br>1'b0: Disable<br>1'b1: Enable auto gating |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | sw_mcp_auto_gating_e<br>block access to ccu<br>1'b0: Disable<br>1'b1: Enable auto gating |
| 2 | RW | 0x0 | sw_strmd_auto_gating_e<br>1'b0: Disable<br>1'b1: Enable auto gating |
| 1 | RW | 0x0 | sw_filterd_auto_gating_e<br>1'b0: Disable<br>1'b1: Enable auto gating |
| 0 | RW | 0x0 | sw_inter_auto_gating_e<br>1'b0: Disable<br>1'b1: Enable auto gating |

**RKVDEC_SWREG27_CORE_SAFE_PIXELS**

Address: Operational Base + offset (0x006c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | sw_core_safe_y_pixles<br>Colmv and recon report coord y safe pixels |
| 15:0 | RW | 0x0000 | sw_core_safe_x_pixels<br>Colmv and recon report coord x safe pixels |

**RKVDEC_SWRE28_MULTIPLY_CORE_CTRL**

Address: Operational Base + offset (0x0070)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | Reserved |
| 29 | RW | 0x0 | sw_colmv_req_mismatch_dis<br>inter colmv set req flag care refpoc mismatch flag is 1 or not<br>1'b0: Inter colmv set req flag care mismatch flag<br>1'b1: Inter colmv set req flag not care mismatch flag |
| 28 | RW | 0x0 | sw_pu_req_mismatch_dis<br>inter pu set req flag care refpoc mismatch flag is 1 or not<br>1'b0: Inter pu set req flag care mismatch flag<br>1'b1: Inter pu set req flag not care mismatch flag |
| 27:26 | RO | 0x0 | Reserved |
| 25:16 | RW | 0x000 | sw_film_idx<br>Film index is separe from difference decode sequences |
| 15:12 | RO | 0x0 | Reserved |
| 11 | RW | 0x0 | sw_poc_arb_flag<br>multiply core use poc arb flag, without common 32bits poc ,<br>but not include vp9 format.<br>1'b0:Use common 32bits base addr flag;<br>1'b1:Use common 32bits poc or highbit poc flag; |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10 | RW | 0x0 | sw_poc_only_highbit_flag<br>multiply core use only highbit poc flag, without common 32bits poc ,but not include vp9 format.<br>1'b0:Use common 32bits poc and highbit poc flag;<br>1'b1:Only use highbit poc flag; |
| 9 | RW | 0x0 | sw_colmv_req_advance_flag<br>Inter colmv data reqire with advance 1/4 picture right and height flag<br>1'b0: Pixels offset not advance<br>1'b1: Pixels x and y offset both advance |
| 8 | RW | 0x0 | sw_ref_req_advance_flag<br>inter pu reference pred data reqire with advance 1/4 picture right and height flag<br>1'b0: Pixels offset not advance<br>1'b1: Pixels x and y offset both advance |
| 7 | RO | 0x0 | Reserved |
| 6:4 | RW | 0x0 | sw_vp9_rd_prob_idx<br>Reference prob index only vp9 used |
| 3 | RO | 0x0 | Reserved |
| 2:0 | RW | 0x0 | sw_vp9_wr_prob_idx<br>Current prob index only vp9 used |

**RKVDEC_SWRE29_SCALE_DOWN_CTRL**

Address: Operational Base + offset (0x0074)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x0 | Reserved |
| 9:8 | RW | 0x0 | sw_scale_down_vrz_ratio<br>2'd1 : vrz not scale down<br>2'd2 : vrz 2-ratio scale down<br>Other: Reserved |
| 7:2 | RO | 0x0 | Reserved |
| 1:0 | RW | 0x0 | sw_scale_down_hor_ratio<br>2'd1 : horization not scale down<br>2'd2 : horization 2-ratio scale down<br>Other: Reserved |

**RKVDEC_SWREG30_Y_SCALE_DOWN_TILE8X8_HOR_STRIDE**

Address: Operational Base + offset (0x0078)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x0 | Reserved |
| 19:0 | RW | 0x00000 | sw_y_scale_down_tile8x8_hor_stride<br>Picture horizontal virtual stride (the unit is 128bit). |

**RKVDEC_SWREG31_UV_SCALE_DOWN_TILE8X8_HOR_STRIDE**

Rockchip Confidencial

Address: Operational Base + offset (0x007c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x0 | Reserved |
| 19:0 | RW | 0x00000 | sw_uv_scale_down8x8_tile_hor_stride<br>Picture horizontal virtual stride (the unit is 128bit). |

**RKVDEC_SWREG32_TIMEOUT_THRESHOLD**

Address: Operational Base + offset (0x0080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_timeout_threshold<br>Aclk cnt if equal to sw_timeout_threshold,it will give timeout. |

**RKVDEC_SWREG64_VP9_SET**

Address: Operational Base + offset (0x0100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_vp9_cprheader_offset<br>Vp9 compressed header offset, at most 2000 probs, 10bit per prob, 20000 bit at most.<br>Now is for no use, because it can read from the last syntax of the uncompressed header. |

**RKVDEC_SWREG64_H26X_SET**

Address: Operational Base + offset (0x0100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0 | Reserved |
| 4 | RW | 0x0 | sw_h264_first_slice_flag<br>1'b0: No First packet in the frame<br>1'b1: First packet in the frame, for h264 decode to read rps/pps data,because the first_mb_in_slice may be wrong, so need this syntax. |
| 3 | RW | 0x0 | sw_h26x_stream_lastpacket<br>When sw_h26x_stream_mode is 1'b1,<br>sw_h26x_stream_lastpacket.<br>1'b0: This packet is not the last packet of frame.<br>1'b1: The packet is the last packet of frame. |
| 2 | RW | 0x0 | sw_h26x_stream_mode<br>1'b0: Stream packet is slice by slice or frame by frame, should use sw_h26x_frame_orslice.<br>1'b1: Stream packet is random, should use sw_h26x_stream_last. |
| 1 | RW | 0x0 | sw_h26x_rps_mode<br>1'b0: Hardware parse rps mode.<br>1'b1: Software parse rps mode. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | sw_h26x_frame_orslice<br>For H26x use<br>1'b0: Frame<br>1'b1: Slice<br>When sw_h26x_streamd_mode is 1'b0, this register is valid. |

**RKVDEC_SWREG65_CUR_POC**

Address: Operational Base + offset (0x0104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_cur_poc<br>The poc of the cur picture.<br>For H264, it may be cur frame poc or cur top field poc. |

**RKVDEC_SWREG66_H264_CUR_POC1**

Address: Operational Base + offset (0x0108)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_h264_cur_poc1<br>H264 cur poc for bottom field. |

**RKVDEC_SWREG67_VP9_SEGID_GRP0**

Address: Operational Base + offset (0x010c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x0 | Reserved |
| 22 | RW | 0x0 | sw_vp9segid0_frame_skip_en<br>Frame skip feature enable. |
| 21:20 | RW | 0x0 | sw_vp9segid0_referinfo<br>Specifies segment i's reference_info which is used to get ref_frame[0]. |
| 19 | RW | 0x0 | sw_vp9segid0_referinfo_en<br>Frame reference info enable. |
| 18:12 | RW | 0x00 | sw_vp9segid0_frame_loopfilter_value<br>Specifies segment i's loopfilter_delta value which is used to calculate filter level. |
| 11 | RW | 0x0 | sw_vp9segid0_frame_loopfitler_value_en<br>Frame_loopfilter_value feature enable. |
| 10:2 | RW | 0x000 | sw_vp9segid0_frame_qp_delta<br>Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant. |
| 1 | RW | 0x0 | sw_vp9segid0_frame_qp_delta_en<br>Frame_qp_delta feature enable. |
| 0 | RW | 0x0 | sw_vp9segid_abs_delta<br>Used to decide quant and loopfilter param. |

Rockchip Confidencial

**RKVDEC_SWREG67_REF0_POC**

Address: Operational Base + offset (0x010c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer0_poc<br>Hevc & h264 & avs2: The poc of reference picture index 0. |

**RKVDEC_SWREG68_VP9_SEGID_GRP1**

Address: Operational Base + offset (0x0110)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x0 | Reserved |
| 22 | RW | 0x0 | sw_vp9segid1_frame_skip_en<br>Frame skip feature enable. |
| 21:20 | RW | 0x0 | sw_vp9segid1_referinfo<br>Specifies segment i's reference_info which is used to get ref_frame[0]. |
| 19 | RW | 0x0 | sw_vp9segid1_referinfo_en<br>Frame reference info enable. |
| 18:12 | RW | 0x00 | sw_vp9segid1_frame_loopfilter_value<br>Specifies segment i's loopfilter_delta value which is used to calculate filter level. |
| 11 | RW | 0x0 | sw_vp9segid1_frame_loopfitler_value_en<br>Frame_loopfilter_value feature enable. |
| 10:2 | RW | 0x000 | sw_vp9segid1_frame_qp_delta<br>Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant. |
| 1 | RW | 0x0 | sw_vp9segid1_frame_qp_delta_en<br>Frame_qp_delta feature enable. |
| 0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG68_REF1_POC**

Address: Operational Base + offset (0x0110)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer1_poc<br>Hevc & h264 & avs2: The poc of reference picture index 1. |

**RKVDEC_SWREG69_VP9_SEGID_GRP2**

Address: Operational Base + offset (0x0114)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x0 | Reserved |
| 22 | RW | 0x0 | sw_vp9segid2_frame_skip_en<br>Frame skip feature enable. |
| 21:20 | RW | 0x0 | sw_vp9segid2_referinfo<br>Specifies segment i's reference_info which is used to get ref_frame[0]. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19 | RW | 0x0 | sw_vp9segid2_referinfo_en<br>Frame reference info enable. |
| 18:12 | RW | 0x00 | sw_vp9segid2_frame_loopfilter_value<br>Specifies segment i's loopfilter_delta value which is used to calculate filter level. |
| 11 | RW | 0x0 | sw_vp9segid2_frame_loopfitler_value_en<br>Frame_loopfilter_value feature enable. |
| 10:2 | RW | 0x000 | sw_vp9segid2_frame_qp_delta<br>Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant. |
| 1 | RW | 0x0 | sw_vp9segid2_frame_qp_delta_en<br>Frame_qp_delta feature enable. |
| 0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG69_REF2_POC**

Address: Operational Base + offset (0x0114)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer2_poc<br>Hevc & h264 & avs2: The poc of reference picture index 2. |

**RKVDEC_SWREG70_VP9_SEGID_GRP3**

Address: Operational Base + offset (0x0118)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x0 | Reserved |
| 22 | RW | 0x0 | sw_vp9segid3_frame_skip_en<br>Frame skip feature enable. |
| 21:20 | RW | 0x0 | sw_vp9segid3_referinfo<br>Specifies segment i's reference_info which is used to get ref_frame[0]. |
| 19 | RW | 0x0 | sw_vp9segid3_referinfo_en<br>Frame reference info enable. |
| 18:12 | RW | 0x00 | sw_vp9segid3_frame_loopfilter_value<br>Specifies segment i's loopfilter_delta value which is used to calculate filter level. |
| 11 | RW | 0x0 | sw_vp9segid3_frame_loopfitler_value_en<br>Frame_loopfilter_value feature enable. |
| 10:2 | RW | 0x000 | sw_vp9segid3_frame_qp_delta<br>Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant. |
| 1 | RW | 0x0 | sw_vp9segid3_frame_qp_delta_en<br>Frame_qp_delta feature enable. |
| 0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG70_REF3_POC**

Rockchip Confidencial

Address: Operational Base + offset (0x0118)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer3_poc<br>Hevc & h264 & avs2: The poc of reference picture index 3. |

**RKVDEC_SWREG71_VP9_SEGID_GRP4**

Address: Operational Base + offset (0x011c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x0 | Reserved |
| 22 | RW | 0x0 | sw_vp9segid4_frame_skip_en<br>Frame skip feature enable. |
| 21:20 | RW | 0x0 | sw_vp9segid4_referinfo<br>Specifies segment i's reference_info which is used to get ref_frame[0]. |
| 19 | RW | 0x0 | sw_vp9segid4_referinfo_en<br>Frame reference info enable. |
| 18:12 | RW | 0x00 | sw_vp9segid4_frame_loopfilter_value<br>Specifies segment i's loopfilter_delta value which is used to calculate filter level. |
| 11 | RW | 0x0 | sw_vp9segid4_frame_loopfitler_value_en<br>Frame_loopfilter_value feature enable. |
| 10:2 | RW | 0x000 | sw_vp9segid4_frame_qp_delta<br>Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant. |
| 1 | RW | 0x0 | sw_vp9segid4_frame_qp_delta_en<br>Frame_qp_delta feature enable. |
| 0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG71_REF4_POC**

Address: Operational Base + offset (0x011c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer4_poc<br>Hevc & h264 & avs2: The poc of reference picture index 4. |

**RKVDEC_SWREG72_VP9_SEGID_GRP5**

Address: Operational Base + offset (0x0120)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x0 | Reserved |
| 22 | RW | 0x0 | sw_vp9segid5_frame_skip_en<br>Frame skip feature enable. |
| 21:20 | RW | 0x0 | sw_vp9segid5_referinfo<br>Specifies segment i's reference_info which is used to get ref_frame[0]. |
| 19 | RW | 0x0 | Sw_vp9segid5_referinfo_en<br>Frame reference info enable. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 18:12 | RW | 0x00 | sw_vp9segid5_frame_loopfilter_value<br>Specifies segment i's loopfilter_delta value which is used to calculate filter level. |
| 11 | RW | 0x0 | sw_vp9segid5_frame_loopfitler_value_en<br>Frame_loopfilter_value feature enable. |
| 10:2 | RW | 0x000 | sw_vp9segid5_frame_qp_delta<br>Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant. |
| 1 | RW | 0x0 | sw_vp9segid5_frame_qp_delta_en<br>Frame_qp_delta feature enable. |
| 0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG72_REF5_POC**

Address: Operational Base + offset (0x0120)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer5_poc<br>Hevc & h264 & avs2: The poc of reference picture index 5. |

**RKVDEC_SWREG73_VP9_SEGID_GRP6**

Address: Operational Base + offset (0x0124)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x0 | Reserved |
| 22 | RW | 0x0 | sw_vp9segid6_frame_skip_en<br>Frame skip feature enable. |
| 21:20 | RW | 0x0 | sw_vp9segid6_referinfo<br>Specifies segment i's reference_info which is used to get ref_frame[0]. |
| 19 | RW | 0x0 | sw_vp9segid6_referinfo_en<br>Frame reference info enable. |
| 18:12 | RW | 0x00 | sw_vp9segid6_frame_loopfilter_value<br>Specifies segment i's loopfilter_delta value which is used to calculate filter level. |
| 11 | RW | 0x0 | sw_vp9segid6_frame_loopfitler_value_en<br>Frame_loopfilter_value feature enable. |
| 10:2 | RW | 0x000 | sw_vp9segid6_frame_qp_delta<br>Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant. |
| 1 | RW | 0x0 | sw_vp9segid6_frame_qp_delta_en<br>Frame_qp_delta feature enable. |
| 0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG73_REF6_POC**

Address: Operational Base + offset (0x0124)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer6_poc<br>Hevc & h264 & avs2: The poc of reference picture index 6. |

**RKVDEC_SWREG74_VP9_SEGID_GRP7**

Address: Operational Base + offset (0x0128)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x0 | Reserved |
| 22 | RW | 0x0 | sw_vp9segid7_frame_skip_en<br>Frame skip feature enable. |
| 21:20 | RW | 0x0 | sw_vp9segid7_referinfo<br>Specifies segment i's reference_info which is used to get ref_frame[0]. |
| 19 | RW | 0x0 | sw_vp9segid7_referinfo_en<br>Frame reference info enable. |
| 18:12 | RW | 0x00 | sw_vp9segid7_frame_loopfilter_value<br>Specifies segment i's loopfilter_delta value which is used to calculate filter level. |
| 11 | RW | 0x0 | sw_vp9segid7_frame_loopfitler_value_en<br>Frame_loopfilter_value feature enable. |
| 10:2 | RW | 0x000 | sw_vp9segid7_frame_qp_delta<br>Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant. |
| 1 | RW | 0x0 | sw_vp9segid7_frame_qp_delta_en<br>Frame_qp_delta feature enable. |
| 0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG74_REF7_POC**

Address: Operational Base + offset (0x0128)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer7_poc<br>Hevc & h264 & avs2: The poc of reference picture index 7. |

**RKVDEC_SWREG75_VP9_INFO_LASTFRAME**

Address: Operational Base + offset (0x012c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x0 | Reserved |
| 22:20 | RW | 0x0 | sw_vp9_color_space_lastkeyframe<br>Vp9 last keyframe color_space. |
| 19 | RW | 0x0 | sw_vp9_last_widhheight_eqcur<br>Last width and height equal cur frame. |
| 18 | RW | 0x0 | sw_vp9_last_intra_only<br>Vp9 last frame intra only flag, to give inter command use.<br>It is for last_dec_frame. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17 | RW | 0x0 | sw_vp9_last_showframe<br>For cal the flag use_prev_in_find_mv_refs which is to inter cmd.<br>It is for last_dec_frame. |
| 16 | RW | 0x0 | sw_segmentation_enable_lstframe<br>1'b0: Sw_segmentation_disable for last frame.<br>1'b1: Sw_segmentation_enable for last frame.<br>It is for last_dec_frame. |
| 15:14 | RO | 0x0 | Reserved |
| 13:0 | RW | 0x0000 | sw_vp9_mode_deltas_lastframe<br>Vp9 mode deltas<br>It is for last dec frame. |

**RKVDEC_SWREG75_REF8_POC**

Address: Operational Base + offset (0x012c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer8_poc<br>Hevc & h264: The poc of reference picture index 8. |

**RKVDEC_SWREG76_VP9_CPRHEADER_CONFIG**

Address: Operational Base + offset (0x0130)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0 | Reserved |
| 4:3 | RW | 0x0 | sw_vp9_frame_reference_mode<br>Frame_reference_mode specifies frame reference mode.<br>SINGLE_REFERENCE = 0,<br>COMPOUND_REFERENCE = 1,<br>REFERENCE_MODE_SELECT = 2,<br>REFERENCE_MODES = 3,<br>When frame_reference_mode_flag0 is not present ,it equal to 0 by default.<br>When frame_reference_mode_flag1 is not present ,it equal to 0 by default.<br>frame_reference_mode = frame_reference_mode_flag0 == 0 ?<br>frame_reference_mode_flag1 == 0 ?<br>REFERENCE_MODE_SELECT : COMPOUND_REFERENCE) :<br>SINGLE_REFERENCE |
| 2:0 | RW | 0x0 | sw_vp9_tx_mode<br>Tx_mode specifies frame transform mode.<br>ONLY_4X4 = 0, // only 4x4 transform used.<br>ALLOW_8X8 = 1, // allow block transform size up to 8x8.<br>ALLOW_16X16 = 2, // allow block transform size up to 16x16.<br>ALLOW_32X32 = 3, // allow block transform size up to 32x32.<br>TX_MODE_SELECT = 4, // transform specified for each block. |

Rockchip Confidencial

**RKVDEC_SWREG76_REF9_POC**

Address: Operational Base + offset (0x0130)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer9_poc<br>Hevc & h264: The poc of reference picture index 9. |

**RKVDEC_SWREG77_VP9_INTERCMD_NUM**

Address: Operational Base + offset (0x0134)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x0 | Reserved |
| 23:0 | RW | 0x000000 | sw_vp9_intercmd_num<br>When rlc_mode is 1'b1, for sw_vp9_intercmd_num.<br>It's unit is 128bit.<br>It count from 1. |

**RKVDEC_SWREG77_REF10_POC**

Address: Operational Base + offset (0x0134)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer10_poc<br>Hevc & h264: The poc of reference picture index 10. |

**RKVDEC_SWREG78_VP9_STREAM_SIZE**

Address: Operational Base + offset (0x0138)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_vp9_stream_size<br>The size of vp9 compressed header and compressed frame data.<br>Its unit is byte.<br>The real meaning the current frame size. |

**RKVDEC_SWREG78_REF11_POC**

Address: Operational Base + offset (0x0138)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer11_poc<br>Hevc & h264: The poc of reference picture index 11. |

**RKVDEC_SWREG79_VP9_LASTF_Y_HOR_VIRSTRIDE**

Address: Operational Base + offset (0x013c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_vp9_lastfy_hor_virstride<br>Vp9 last frame y horizontal virstride.<br>For fbc mode: Vp9 head hor stride of last frame. |

**RKVDEC_SWREG79_REF12_POC**

Rockchip Confidencial

Address: Operational Base + offset (0x013c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer12_poc<br>Hevc & h264: The poc of reference picture index 12. |

**RKVDEC_SWREG80_VP9_LASTF_UV_HOR_VIRSTRIDE**

Address: Operational Base + offset (0x0140)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_vp9_lastfuv_hor_virstride<br>Vp9 last frame uv horizontal virstride. |

**RKVDEC_SWREG80_REF13_POC**

Address: Operational Base + offset (0x0140)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer13_poc<br>Hevc & h264: The poc of reference picture index 13. |

**RKVDEC_SWREG81_VP9_GOLDENF_Y_HOR_VIRSTRIDE**

Address: Operational Base + offset (0x0144)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_vp9_goldenfy_hor_virstride<br>Vp9 golden frame y horizontal virstride.<br>For fbc mode: Vp9 head hor stride of golden frame. |

**RKVDEC_SWREG81_REF14_POC**

Address: Operational Base + offset (0x0144)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer14_poc<br>Hevc & h264: The poc of reference picture index 14. |

**RKVDEC_SWREG82_VP9_GOLDEN_UV_HOR_VIRSTRIDE**

Address: Operational Base + offset (0x0148)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_vp9_goldenuv_hor_virstride<br>Vp9 golden uv horizontal virstirde. |

**RKVDEC_SWREG82_REF15_POC**

Address: Operational Base + offset (0x0148)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer15_poc<br>The poc of reference picture index 15.<br>Used to hevc for mvc. |

**RKVDEC_SWREG83_VP9_ALTREFF_Y_HOR_VIRSTRIDE**

Address: Operational Base + offset (0x014c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_vp9_altreffy_hor_virstride<br>Vp9 altref frame y horizontal virstride.<br>For fbc mode: Vp9 head hor stride of after frame. |

**RKVDEC_SWREG83_REF16_POC**

Address: Operational Base + offset (0x014c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer16_poc<br>H264: The poc of reference picture index 16.<br>Hevc & vp9: Now is no use. |

**RKVDEC_SWREG84_VP9_ALTREFF_UV_HOR_VIRSTRIDE**

Address: Operational Base + offset (0x0150)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_vp9_altreffuv_hor_virstride<br>Vp9 altreff uv horizontal virstirde. |

**RKVDEC_SWREG84_REF17_POC**

Address: Operational Base + offset (0x0150)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer17_poc<br>H264: The poc of reference picture index 17.<br>Hevc & vp9: Now is no use. |

**RKVDEC_SWREG85_VP9_LASTF_Y_VIRSTRIDE**

Address: Operational Base + offset (0x0154)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | Reserved |
| 27:0 | RW | 0x0000000 | sw_vp9_lastfy_virstride<br>Vp9 last frame y stride. |

**RKVDEC_SWREG85_REF18_POC**

Address: Operational Base + offset (0x0154)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer18_poc<br>H264: The poc of reference picture index 18.<br>Hevc & vp9: Now is no use. |

**RKVDEC_SWREG86_VP9_GOLDEN_Y_VIRSTRIDE**

Address: Operational Base + offset (0x0158)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | Reserved |
| 27:0 | RW | 0x0000000 | sw_vp9_goldeny_virstride<br>Vp9 golden frame y stride. |

**RKVDEC_SWREG86_REF19_POC**

Address: Operational Base + offset (0x0158)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer19_poc<br>H264: The poc of reference picture index 19.<br>Hevc & vp9: Now is no use. |

**RKVDEC_SWREG87_VP9_ALTREF_Y_VIRSTRIDE**

Address: Operational Base + offset (0x015c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | Reserved |
| 27:0 | RW | 0x0000000 | sw_vp9_altrefy_virstride<br>Vp9 altref frame y stride. |

**RKVDEC_SWREG87_REF20_POC**

Address: Operational Base + offset (0x015c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer20_poc<br>H264: The poc of reference picture index 20.<br>Hevc & vp9: Now is no use. |

**RKVDEC_SWREG88_VP9_LREF_HOR_SCALE**

Address: Operational Base + offset (0x0160)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_vp9_lref_hor_scale<br>Horizontal scaling factor for last reference picture.<br>Sw_vp9_lref_hor_scale = (last_ref_width / cur_width) * 0x4000. |

**RKVDEC_SWREG88_REF21_POC**

Address: Operational Base + offset (0x0160)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer21_poc<br>H264: The poc of reference picture index 21.<br>Hevc & vp9: Now is no use. |

**RKVDEC_SWREG89_VP9_LREF_VER_SCALE**

Address: Operational Base + offset (0x0164)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_vp9_lref_ver_scale<br>Vertical scaling factor for last reference picture. |

**RKVDEC_SWREG89_REF22_POC**

Address: Operational Base + offset (0x0164)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer22_poc<br>H264: The poc of reference picture index 22.<br>Hevc & vp9: Now is no use. |

**RKVDEC_SWREG90_VP9_GREF_HOR_SCALE**

Address: Operational Base + offset (0x0168)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_vp9_gref_hor_scale<br>Horizontal scaling factor for golden reference picture.<br>Sw_vp9_gref_hor_scale = (golden_ref_width / cur_width) * 0x4000. |

**RKVDEC_SWREG90_REF23_POC**

Address: Operational Base + offset (0x0168)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer23_poc<br>H264: The poc of reference picture index 23.<br>Hevc & vp9: Now is no use. |

**RKVDEC_SWREG91_VP9_GREF_VER_SCALE**

Address: Operational Base + offset (0x016c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_vp9_gref_ver_scale<br>Vertical scaling factor for golden reference picture. |

**RKVDEC_SWREG91_REF24_POC**

Address: Operational Base + offset (0x016c)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Sw_refer24_poc<br>H264: The poc of reference picture index 24.<br>Hevc & vp9: Now is no use. |

**RKVDEC_SWREG92_VP9_AREF_HOR_SCALE**

Address: Operational Base + offset (0x0170)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_vp9_aref_hor_scale<br>Horizontal scaling factor for alfter reference picture.<br>Sw_vp9_gref_hor_scale = (alfter_ref_width / cur_width) * 0x4000. |

**RKVDEC_SWREG92_REF25_POC**

Address: Operational Base + offset (0x0170)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer25_poc<br>H264: The poc of reference picture index 25.<br>Hevc & vp9: Now is no use. |

**RKVDEC_SWREG93_VP9_AREF_VER_SCALE**

Address: Operational Base + offset (0x0174)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_vp9_aref_ver_scale<br>Vertical scaling factor for alfter reference picture. |

**RKVDEC_SWREG93_REF26_POC**

Address: Operational Base + offset (0x0174)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer26_poc<br>H264: The poc of reference picture index 26.<br>Hevc & vp9: Now is no use. |

**RKVDEC_SWREG94_VP9_REF_DELTAS_LASTFRAME**

Address: Operational Base + offset (0x0178)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | Reserved |
| 27:0 | RW | 0x0000000 | sw_vp9_ref_deltas_lastframe<br>Vp9 ref deltas of lastframe, for cal loopfilter filter type use. |

**RKVDEC_SWREG94_REF27_POC**

Address: Operational Base + offset (0x0178)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer27_poc<br>H264: The poc of reference picture index 27.<br>Hevc & vp9: Now is no use. |

**RKVDEC_SWREG95_VP9_LAST_POC**

Address: Operational Base + offset (0x017c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_vp9_last_poc<br>VP9: The poc of last reference |

**RKVDEC_SWREG95_REF28_POC**

Address: Operational Base + offset (0x017c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer28_poc<br>H264: The poc of reference picture index 28.<br>Hevc & vp9: Now is no use. |

**RKVDEC_SWREG96_VP9_GOLDEN_POC**

Address: Operational Base + offset (0x0180)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_vp9_golden_poc<br>VP9: The poc of golden reference |

**RKVDEC_SWREG96_REF29_POC**

Address: Operational Base + offset (0x0180)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer29_poc<br>H264: The poc of reference picture index 29.<br>Hevc & vp9: Now is no use. |

**RKVDEC_SWREG97_VP9_ALTREF_POC**

Address: Operational Base + offset (0x0184)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_vp9_altref_poc<br>VP9: The poc of altref reference |

**RKVDEC_SWREG97_REF30_POC**

Address: Operational Base + offset (0x0184)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer30_poc<br>H264: The poc of reference picture index 30.<br>Hevc & vp9: Now is no use. |

Rockchip Confidencial

**RKVDEC_SWREG98_VP9_COL_REF_POC**

Address: Operational Base + offset (0x0188)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_vp9_col_ref_poc<br>VP9: The poc of colpic reference |

**RKVDEC_SWREG98_REF31_POC**

Address: Operational Base + offset (0x0188)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_refer31_poc<br>H264: The poc of reference picture index 31.<br>Hevc & vp9: Now is no use. |

**RKVDEC_SWREG99_H264_REG0_3_INFO**

Address: Operational Base + offset (0x018c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | Reserved |
| 27 | RW | 0x0 | sw_ref3_colmv_use_flag<br>Ref3 colmv use flag. |
| 26 | RW | 0x0 | sw_ref3_botfield_used<br>Ref3 bottom field is used, the same meaning with ref_valid. |
| 25 | RW | 0x0 | sw_ref3_topfield_used<br>Ref3 top field is used, the same meaning with ref_valid. |
| 24 | RW | 0x0 | sw_ref3_field<br>1'b0: Frame<br>1'b1: Field |
| 23:20 | RO | 0x0 | Reserved |
| 19 | RW | 0x0 | sw_ref2_colmv_use_flag<br>Ref2 colmv use flag. |
| 18 | RW | 0x0 | sw_ref2_botfield_used<br>Ref2 bottom field is used, the same meaning with ref_valid. |
| 17 | RW | 0x0 | sw_ref2_topfield_used<br>Ref2 top field is used, the same meaning with ref_valid. |
| 16 | RW | 0x0 | sw_ref2_field<br>1'b0: Frame<br>1'b1: Field |
| 15:12 | RO | 0x0 | Reserved |
| 11 | RW | 0x0 | sw_ref1_colmv_use_flag<br>Ref1 colmv use flag. |
| 10 | RW | 0x0 | sw_ref1_botfield_used<br>Ref1 bottom field is used, the same meaning with ref_valid. |
| 9 | RW | 0x0 | sw_ref1_topfield_used<br>Ref1 top field is used, the same meaning with ref_valid. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | sw_ref1_field<br>1'b0: Frame<br>1'b1: Field |
| 7:4 | RO | 0x0 | Reserved |
| 3 | RW | 0x0 | sw_ref0_colmv_use_flag<br>Ref0 colmv use flag. |
| 2 | RW | 0x0 | sw_ref0_botfield_used<br>Ref0 bottom field is used, the same meaning with ref_valid. |
| 1 | RW | 0x0 | sw_ref0_topfield_used<br>Ref0 top field is used, the same meaning with ref_valid. |
| 0 | RW | 0x0 | sw_ref0_field<br>1'b0: Frame<br>1'b1: Field |

**RKVDEC_SWREG99_AVS2_REG0_3_INFO**

Address: Operational Base + offset (0x018c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | Reserved |
| 27 | RW | 0x0 | sw_ref3_valid_flag<br>Reference picture3 used flag.<br>1'b0: Not be valid<br>1'b1: Be valid |
| 26 | RW | 0x0 | sw_ref3_botfield_used<br>Refer3 is bottow field flag.<br>1'b0: Top field flag<br>1'b1: Bottom field flag |
| 25 | RO | 0x0 | Reserved |
| 24 | RW | 0x0 | sw_ref3_field<br>1'b0: Frame<br>1'b1: Field |
| 23:20 | RO | 0x0 | Reserved |
| 19 | RW | 0x0 | sw_ref2_valid_flag<br>Reference picture2 used flag.<br>1'b0: Not be valid<br>1'b1: Be valid |
| 18 | RW | 0x0 | sw_ref2_botfield_used<br>Refer2 is bottow field flag.<br>1'b0: Top field flag<br>1'b1: Bottom field flag |
| 17 | RO | 0x0 | Reserved |
| 16 | RW | 0x0 | sw_ref2_field<br>1'b0: Frame<br>1'b1: Field |
| 15:12 | RO | 0x0 | Reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11 | RW | 0x0 | sw_ref1_valid_flag<br>Reference picture1 used flag.<br>1'b0: Not be valid<br>1'b1: Be valid |
| 10 | RW | 0x0 | Sw_ref1_botfield_used<br>Refer1 is bottow field flag.<br>1'b0: Top field flag<br>1'b1: Bottom field flag |
| 9 | RO | 0x0 | Reserved |
| 8 | RW | 0x0 | sw_ref1_field<br>1'b0: Frame<br>1'b1: Field |
| 7:4 | RO | 0x0 | Reserved |
| 3 | RW | 0x0 | sw_ref0_valid_flag<br>Reference picture0 used flag.<br>1'b0: Not be valid<br>1'b1: Be valid |
| 2 | RW | 0x0 | sw_ref0_botfield_used<br>Refer0 is bottow field flag.<br>1'b0: Top field flag<br>1'b1: Bottom field flag |
| 1 | RO | 0x0 | Reserved |
| 0 | RW | 0x0 | sw_ref0_field<br>1'b0: Frame<br>1'b1: Field |

**RKVDEC_SWREG99_VP9_PROB_REF_POC**

Address: Operational Base + offset (0x018c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_vp9_prob_ref_poc<br>VP9: The poc of reference prob |

**RKVDEC_SWREG99_HEVC_REF_VALID**

Address: Operational Base + offset (0x018c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:27 | RO | 0x0 | Reserved |
| 26 | RW | 0x0 | sw_hevc_ref_valid_14<br>Valid flag for picture index 14. |
| 25 | RW | 0x0 | sw_hevc_ref_valid_13<br>Valid flag for picture index 13. |
| 24 | RW | 0x0 | sw_hevc_ref_valid_12<br>Valid flag for picture index 12. |
| 23:20 | RO | 0x0 | Reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19 | RW | 0x0 | sw_hevc_ref_valid_11<br>Valid flag for picture index 11. |
| 18 | RW | 0x0 | sw_hevc_ref_valid_10<br>Valid flag for picture index 10. |
| 17 | RW | 0x0 | sw_hevc_ref_valid_9<br>Valid flag for picture index 9. |
| 16 | RW | 0x0 | sw_hevc_ref_valid_8<br>Valid flag for picture index 8. |
| 15:12 | RO | 0x0 | Reserved |
| 11 | RW | 0x0 | sw_hevc_ref_valid_7<br>Valid flag for picture index 7. |
| 10 | RW | 0x0 | sw_hevc_ref_valid_6<br>Valid flag for picture index 6. |
| 9 | RW | 0x0 | sw_hevc_ref_valid_5<br>Valid flag for picture index 5. |
| 8 | RW | 0x0 | sw_hevc_ref_valid_4<br>Valid flag for picture index 4. |
| 7:4 | RO | 0x0 | Reserved |
| 3 | RW | 0x0 | sw_hevc_ref_valid_3<br>Valid flag for picture index 3. |
| 2 | RW | 0x0 | sw_hevc_ref_valid_2<br>Valid flag for picture index 2. |
| 1 | RW | 0x0 | sw_hevc_ref_valid_1<br>Valid flag for picture index 1. |
| 0 | RW | 0x0 | sw_hevc_ref_valid_0<br>Valid flag for picture index 0. |

**RKVDEC_SWREG100_AVS2_REG4_7_INFO**

Address: Operational Base + offset (0x0190)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | Reserved |
| 27 | RW | 0x0 | sw_ref7_valid_flag<br>Reference picture7 used flag.<br>1'b0: Not be valid<br>1'b1: Be valid |
| 26 | RW | 0x0 | sw_ref7_botfield_used<br>Refer7 is bottow field flag.<br>1'b0: Top field flag<br>1'b1: Bottom field flag |
| 25 | RO | 0x0 | Reserved |
| 24 | RW | 0x0 | sw_ref7_field<br>1'b0: Frame<br>1'b1: Field |
| 23:20 | RO | 0x0 | Reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19 | RW | 0x0 | sw_ref6_valid_flag<br>Reference picture6 used flag.<br>1'b0: Not be valid<br>1'b1: Be valid |
| 18 | RW | 0x0 | sw_ref6_botfield_used<br>Refer6 is bottow field flag.<br>1'b0: Top field flag<br>1'b1: Bottom field flag |
| 17 | RO | 0x0 | Reserved |
| 16 | RW | 0x0 | sw_ref6_field<br>1'b0: Frame<br>1'b1: Field |
| 15:12 | RO | 0x0 | Reserved |
| 11 | RW | 0x0 | sw_ref5_valid_flag<br>Reference picture5 used flag.<br>1'b0: Not be valid<br>1'b1: Be valid |
| 10 | RW | 0x0 | sw_ref5_botfield_used<br>Refer5 is bottow field flag.<br>1'b0: Top field flag<br>1'b1: Bottom field flag |
| 9 | RO | 0x0 | Reserved |
| 8 | RW | 0x0 | sw_ref5_field<br>1'b0: Frame<br>1'b1: Field |
| 7:4 | RO | 0x0 | Reserved |
| 3 | RW | 0x0 | sw_ref4_valid_flag<br>Reference picture4 used flag.<br>1'b0: Not be valid<br>1'b1: Be valid |
| 2 | RW | 0x0 | sw_ref4_botfield_used<br>Refer4 is bottow field flag.<br>1'b0: Top field flag<br>1'b1: Bottom field flag |
| 1 | RO | 0x0 | Reserved |
| 0 | RW | 0x0 | sw_ref4_field<br>1'b0: Frame<br>1'b1: Field |

**RKVDEC_SWREG100_H264_REG4_7_INFO**

Address: Operational Base + offset (0x0190)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | Reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 27 | RW | 0x0 | sw_ref7_colmv_use_flag<br>Ref7 colmv use flag. |
| 26 | RW | 0x0 | sw_ref7_botfield_used<br>Ref7 bottom field is used, the same meaning with ref_valid. |
| 25 | RW | 0x0 | sw_ref7_topfield_used<br>Ref7 top field is used, the same meaning with ref_valid. |
| 24 | RW | 0x0 | sw_ref7_field<br>1'b0: Frame<br>1'b1: Field |
| 23:20 | RO | 0x0 | Reserved |
| 19 | RW | 0x0 | sw_ref6_colmv_use_flag<br>Ref6 colmv use flag. |
| 18 | RW | 0x0 | sw_ref6_botfield_used<br>Ref6 bottom field is used, the same meaning with ref_valid. |
| 17 | RW | 0x0 | sw_ref6_topfield_used<br>Ref6 top field is used, the same meaning with ref_valid. |
| 16 | RW | 0x0 | sw_ref6_field<br>1'b0: Frame<br>1'b1: Field |
| 15:12 | RO | 0x0 | Reserved |
| 11 | RW | 0x0 | sw_ref5_colmv_use_flag<br>Ref5 colmv use flag. |
| 10 | RW | 0x0 | sw_ref5_botfield_used<br>Ref5 bottom field is used, the same meaning with ref_valid. |
| 9 | RW | 0x0 | sw_ref5_topfield_used<br>Ref5 top field is used, the same meaning with ref_valid. |
| 8 | RW | 0x0 | sw_ref5_field<br>1'b0: Frame<br>1'b1: Field |
| 7:4 | RO | 0x0 | Reserved |
| 3 | RW | 0x0 | sw_ref4_colmv_use_flag<br>Ref4 colmv use flag. |
| 2 | RW | 0x0 | sw_ref4_botfield_used<br>Ref4 bottom field is used, the same meaning with ref_valid. |
| 1 | RW | 0x0 | sw_ref4_topfield_used<br>Ref4 top field is used, the same meaning with ref_valid. |
| 0 | RW | 0x0 | sw_ref4_field<br>1'b0: Frame<br>1'b1: Field |

**RKVDEC_SWREG100_VP9_SEGID_REF_POC**

Address: Operational Base + offset (0x0190)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0000 | sw_vp9_segid_ref_poc<br>VP9: The poc of reference segmentid |

**RKVDEC_SWREG101_H264_REG8_11_INFO**

Address: Operational Base + offset (0x0194)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | Reserved |
| 27 | RW | 0x0 | sw_ref11_colmv_use_flag<br>Ref11 colmv use flag. |
| 26 | RW | 0x0 | sw_ref11_botfield_used<br>Ref11 bottom field is used, the same meaning with ref_valid. |
| 25 | RW | 0x0 | sw_ref11_topfield_used<br>Ref11 top field is used, the same meaning with ref_valid. |
| 24 | RW | 0x0 | sw_ref11_field<br>1'b0: Frame<br>1'b1: Field |
| 23:20 | RO | 0x0 | Reserved |
| 19 | RW | 0x0 | sw_ref10_colmv_use_flag<br>Ref10 colmv use flag. |
| 18 | RW | 0x0 | sw_ref10_botfield_used<br>Ref10 bottom field is used, the same meaning with ref_valid. |
| 17 | RW | 0x0 | sw_ref10_topfield_used<br>Ref10 top field is used, the same meaning with ref_valid. |
| 16 | RW | 0x0 | sw_ref10_field<br>1'b0: Frame<br>1'b1: Field |
| 15:12 | RO | 0x0 | Reserved |
| 11 | RW | 0x0 | sw_ref9_colmv_use_flag<br>Ref9 colmv use flag. |
| 10 | RW | 0x0 | sw_ref9_botfield_used<br>Ref9 bottom field is used, the same meaning with ref_valid. |
| 9 | RW | 0x0 | sw_ref9_topfield_used<br>Ref9 top field is used, the same meaning with ref_valid. |
| 8 | RW | 0x0 | sw_ref9_field<br>1'b0: Frame<br>1'b1: Field |
| 7:4 | RO | 0x0 | Reserved |
| 3 | RW | 0x0 | sw_ref8_colmv_use_flag<br>Ref8 colmv use flag. |
| 2 | RW | 0x0 | sw_ref8_botfield_used<br>Ref8 bottom field is used, the same meaning with ref_valid. |
| 1 | RW | 0x0 | sw_ref8_topfield_used<br>Ref8 top field is used, the same meaning with ref_valid. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | sw_ref8_field<br>1'b0: Frame<br>1'b1: Field |

**RKVDEC_SWREG102_H264_REG12_15_INFO**

Address: Operational Base + offset (0x0198)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | Reserved |
| 27 | RW | 0x0 | sw_ref15_colmv_use_flag<br>Ref15 colmv use flag. |
| 26 | RW | 0x0 | sw_ref15_botfield_used<br>Ref15 bottom field is used, the same meaning with ref_valid. |
| 25 | RW | 0x0 | sw_ref15_topfield_used<br>Ref15 top field is used, the same meaning with ref_valid. |
| 24 | RW | 0x0 | sw_ref15_field<br>1'b0: Frame<br>1'b1: Field |
| 23:20 | RO | 0x0 | Reserved |
| 19 | RW | 0x0 | sw_ref14_colmv_use_flag<br>Ref14 colmv use flag. |
| 18 | RW | 0x0 | sw_ref14_botfield_used<br>Ref14 bottom field is used, the same meaning with ref_valid. |
| 17 | RW | 0x0 | sw_ref14_topfield_used<br>Ref14 top field is used, the same meaning with ref_valid. |
| 16 | RW | 0x0 | sw_ref14_field<br>1'b0: Frame<br>1'b1: Field |
| 15:12 | RO | 0x0 | Reserved |
| 11 | RW | 0x0 | sw_ref13_colmv_use_flag<br>Ref13 colmv use flag. |
| 10 | RW | 0x0 | sw_ref13_botfield_used<br>Ref13 bottom field is used, the same meaning with ref_valid. |
| 9 | RW | 0x0 | sw_ref13_topfield_used<br>Ref13 top field is used, the same meaning with ref_valid. |
| 8 | RW | 0x0 | sw_ref13_field<br>1'b0: Frame<br>1'b1: Field |
| 7:4 | RO | 0x0 | Reserved |
| 3 | RW | 0x0 | sw_ref12_colmv_use_flag<br>Ref12 colmv use flag. |
| 2 | RW | 0x0 | sw_ref12_botfield_used<br>Ref12 bottom field is used, the same meaning with ref_valid. |
| 1 | RW | 0x0 | sw_ref12_topfield_used<br>Ref12 top field is used, the same meaning with ref_valid. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | sw_ref12_field<br>1'b0: Frame<br>1'b1: Field |

**RKVDEC_SWREG103_HEVC_MVC0**

Address: Operational Base + offset (0x019c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_ref_pic_layer_same_with_cur<br>Referance picture layer same with current picture. |

**RKVDEC_SWREG103_AVS2_CTRL_EXTRA**

Address: Operational Base + offset (0x019c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x0 | Reserved |
| 0 | RW | 0x0 | sw_avs2_slice_hor_pos_ctrl<br>1'b0: Use default 255.<br>1'b1: Use fixed 256. |

**RKVDEC_SWREG103_VP9_PROB_EN**

Address: Operational Base + offset (0x019c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | sw_vp9_inter_coef_rfsh_flag<br>1'b0: Inter coef unneed refresh in current intra frame.<br>1'b1: Inter coef should be refresh in current intra frame. |
| 30 | RW | 0x0 | sw_vp9_last_key_frame_flag<br>The flag of last frame is key frame.<br>1'b0: Not key frame.<br>1'b1: Key frame. |
| 29 | RW | 0x0 | sw_vp9_allow_high_precision_mv<br>The enable of high precision mv prob refresh update.<br>1'b0: Disable<br>1'b1: Enable |
| 28 | RW | 0x0 | sw_vp9_interp_filter_switch_en<br>The enable of interp filter prob refresh update.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_vp9_comp_ref_rfsh_en<br>The enable of comp reference prob refresh update.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 26 | RW | 0x0 | sw_vp9_single_ref_rfsh_en<br>The enable of single reference prob refresh update.<br>1'b0: Disable<br>1'b1: Enable |
| 25 | RW | 0x0 | sw_vp9_ref_mode_rfsh_en<br>The enable of reference mode prob refresh update.<br>1'b0: Disable<br>1'b1: Enable |
| 24 | RW | 0x0 | sw_vp9_txfmmode_rfsh_en<br>The enable of tx mode prob refresh update.<br>1'b0: Disable<br>1'b1: Enable |
| 23 | RW | 0x0 | sw_vp9_intra_only_flag<br>The flag of intra only.<br>1'b0: Inter frame.<br>1'b1: Intra only frame（include key frame）. |
| 22 | RW | 0x0 | sw_vp9_prob_save_en<br>The flag of write updated prob to DDR.<br>1'b0: Not need write updated prob to DDR.<br>1'b1: Will write updated prob to DDR. |
| 21 | RW | 0x0 | sw_vp9_refresh_en<br>The enbale of prob backward refresh.<br>1'b0: Disable refresh parse.<br>1'b1: Enable refresh parse. |
| 20 | RW | 0x0 | sw_vp9_prob_update_en<br>The enable of used hardware to parse prob.<br>1'b0: Software parse prob.<br>1'b1: Hardware parse prob. |
| 19:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG104_HEVC_MVC1**

Address: Operational Base + offset (0x01a0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:19 | RO | 0x0 | Reserved |
| 18 | RW | 0x0 | sw_mvc_poc15_valid_flag<br>Mvc poc15 valid flag. |
| 17 | RW | 0x0 | sw_rps_poc_lsb_aligned_flag<br>Rps POC lsb aligned flag. |
| 16 | RW | 0x0 | sw_poc_reset_info_present_flag<br>The flag of poc reset infomation. |
| 15 | RW | 0x0 | sw_max_one_active_ref_layer_flag<br>The flag of max referance referance layer be actived. |
| 14 | RW | 0x0 | sw_default_ref_layers_active_flag<br>The flag of default referance layers which be actived. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:8 | RW | 0x00 | sw_num_reflayer_pics<br>The number of referance layer pictures. |
| 7 | RO | 0x0 | Reserved |
| 6:1 | RW | 0x00 | sw_num_direct_ref_layers<br>The number of direct referance layers. |
| 0 | RW | 0x0 | sw_poc_lsb_not_present_flag<br>Poc lsb not present flag. |

**RKVDEC_SWREG105_VP9CNT_UPD_EN_AVS2_HEADLEN**

Address: Operational Base + offset (0x01a4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0 | Reserved |
| 4 | RW | 0x0 | sw_vp9count_update_en<br>When 1'b1, the hardware will always update count.<br>When 1'b0, the hardware will auto check whether update the count. |
| 3:0 | RW | 0x0 | sw_avs2_head_len<br>It's unit is 128bit.<br>4'd0: 128bit<br>4'd1: 2*128bit<br>4'd2: 3*128bit<br>.....<br>4'd15: 16*128bit |

**RKVDEC_SWREG106_VP9_FRAME_WIDTH_LAST**

Address: Operational Base + offset (0x01a8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_framewidth_last<br>Last frame frame_size_width. |

**RKVDEC_SWREG107_VP9_FRAME_HEIGHT_LAST**

Address: Operational Base + offset (0x01ac)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_frameheight_last<br>Last frame frame_size_height. |

**RKVDEC_SWREG108_VP9_FRAME_WIDTH_GOLDEN**

Address: Operational Base + offset (0x01b0)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_framewidth_golden<br>Golden frame_size_width |

**RKVDEC_SWREG109_VP9_FRAME_HEIGHT_GOLDEN**

Address: Operational Base + offset (0x01b4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_frameheight_golden<br>Golden frame_size_height. |

**RKVDEC_SWREG110_VP9_FRAME_WIDTH_ALTREF**

Address: Operational Base + offset (0x01b8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_framewidth_alfter<br>Alfter frame_size_width. |

**RKVDEC_SWREG111_VP9_FRAME_HEIGHT_ALTREF**

Address: Operational Base + offset (0x01bc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | sw_frameheight_alfter<br>Alfter frame_size_height. |

**RKVDEC_SWREG112_ERROR_REF_INFO**

Address: Operational Base + offset (0x01c0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0 | Reserved |
| 3 | RW | 0x0 | sw_ref_error_botfield_used<br>For inter,<br>1'b1: Botfield is no used.<br>1'b1: Botfield is used. |
| 2 | RW | 0x0 | sw_ref_error_topfield_used<br>For inter,<br>1'b1: Topfield is no used.<br>1'b1: Topfield is used. |
| 1 | RW | 0x0 | sw_avs2_ref_error_topfield<br>Refer error is top field flag.<br>1'b0: Bottom field flag.<br>1'b1: Top field flag. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | sw_avs2_ref_error_field<br>1'b0: Frame<br>1'b1: Field |

**RKVDEC_SWREG128_STRM_RLC_BASE**

Address: Operational Base + offset (0x0200)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_strm_rlc_base<br>When swreg2.sw_rlc_mode =1, it is base address for rlc data.<br>When swreg2.sw_rlc_mode =0, it is base address for stream, after a frame is decoded ready or error (stream error , time out , bus error) , it is the last address of the stream.<br>The address should 128bit align. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG129_ERROR_INFO_BASE**

Address: Operational Base + offset (0x0204)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RW | 0x00000000 | sw_error_info_base<br>The base address of error info |
| 2:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG129_RLCWRITE_BASE**

Address: Operational Base + offset (0x0204)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RW | 0x00000000 | sw_rlcwrite_base<br>The base address of rlcwrite(the address should 64bit align).<br>Cabac output write to this rlcwrite base address when sw_rlc_mode_direct_write in swreg2_sysctrl is valid. |
| 2:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG130_DECOUT_BASE**

Address: Operational Base + offset (0x0208)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_decout_base<br>Base address of decoder output picture, the address should be 128bit align.<br>In H264 decode format, the top field and bottom field are the same addr.<br>Fbc mode: Fbc_head_base_addr[27:0]: the head base of fbc wr. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG131_COLMV_CUR_BASE**

Rockchip Confidencial

Address: Operational Base + offset (0x020c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_colmv_cur_base<br>Only valid when sw_colmv_mode is 1'b1.<br>Cur frame colmv base addr, for HEVC,H264 and vp9. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG132_ERROR_REF_BASE**

Address: Operational Base + offset (0x0210)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_error_ref_base<br>Error reference frame base address. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG133_RCB_INTRAR_BASE**

Address: Operational Base + offset (0x0214)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RW | 0x0000000 | sw_rcb_intrar_base<br>Rcb intra row base address, unit: 64byts align. |
| 5:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG134_RCB_TRANSDR_BASE**

Address: Operational Base + offset (0x0218)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RW | 0x0000000 | sw_rcb_transdr_base<br>Rcb transd row base address, unit: 64byts align. |
| 5:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG135_RCB_TRANSDC_BASE**

Address: Operational Base + offset (0x021c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RW | 0x0000000 | sw_rcb_transdc_base<br>Rcb transd col base address, unit: 64byts align. |
| 5:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG136_RCB_STRMDR_BASE**

Address: Operational Base + offset (0x0220)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RW | 0x0000000 | sw_rcb_strmdr_base<br>Rcb stream row base address, unit: 64byts align. |
| 5:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG137_RCB_INTERR_BASE**

Address: Operational Base + offset (0x0224)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RW | 0x0000000 | sw_rcb_interr_base<br>Rcb inter row base address, unit: 64byts align. |
| 5:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG138_RCB_INTERC_BASE**

Address: Operational Base + offset (0x0228)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RW | 0x0000000 | sw_rcb_interc_base<br>Rcb inter col base address, unit: 64byts align. |
| 5:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG139_RCB_DBLKR_BASE**

Address: Operational Base + offset (0x022c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RW | 0x0000000 | sw_rcb_dblkr_base<br>Rcb dblock row base address, unit: 64byts align. |
| 5:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG140_RCB_SAOR_BASE**

Address: Operational Base + offset (0x0230)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RW | 0x0000000 | sw_rcb_saor_base<br>Rcb sao row base address, unit: 64byts align. |
| 5:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG141_RCB_FBCR_BASE**

Address: Operational Base + offset (0x0234)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RW | 0x0000000 | sw_rcb_fbcr_base<br>Rcb fbc row base address, unit: 64byts align. |
| 5:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG142_RCB_FILTC_COL_BASE**

Address: Operational Base + offset (0x0238)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RW | 0x0000000 | sw_rcb_filtc_base<br>Rcb filter col base address, unit: 64byts align. |
| 5:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG160_VP9_DELTA_PROB_BASE**

Address: Operational Base + offset (0x0280)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_vp9_delta_prob_base<br>The base address of prob. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG161_PPS_BASE**

Address: Operational Base + offset (0x0284)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_pps_base<br>The base address of pps (the address should 128bit align).<br>It is for storing sps(sequence parameter set) and pps(picture parameter set). |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG161_AVS2_HEAD_BASE**

Address: Operational Base + offset (0x0284)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_avs2_head_base<br>The base address of avs2 head ( the address should 128bit align ).<br>It will include sequence and picture level syntax. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG162_VP9_LAST_PROB_BASE**

Address: Operational Base + offset (0x0288)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_vp9_last_porb_base<br>The base address of last prob (the address should 128bit align). |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG163_RPS_BASE**

Address: Operational Base + offset (0x028c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_rps_base<br>Rps(reference picture set) base address (the address should 128bit align). |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG164_REF0_BASE**

Address: Operational Base + offset (0x0290)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_refer0_base<br>Base address for reference picture index0 (the address should be 128bit align)<br>Fbc mode: H264 & hevc & avs2 ref0 head base. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG164_VP9_REFERLAST_BASE**

Address: Operational Base + offset (0x0290)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_vp9_last_base<br>Base address for last (the address should be 128bit align).<br>Fbc mode: Vp9 last ref frame head base. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG165_REF1_BASE**

Address: Operational Base + offset (0x0294)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_refer1_base<br>Base address for reference picture index1 (the address should be 128bit align)<br>Fbc mode: H264 & hevc & avs2 ref1 head base. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG165_VP9_REFERGOLDEN_BASE**

Address: Operational Base + offset (0x0294)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_vp9golden_base<br>Base address for golden (the address should be 128bit align).<br>Fbc mode: Vp9 golden ref frame head base. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG166_REF2_BASE**

Address: Operational Base + offset (0x0298)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_refer2_base<br>Base address for reference picture index2 (the address should be 128bit align)<br>Fbc mode: H264 & hevc & avs2 ref2 head base. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG166_VP9_REFERALFTER_BASE**

Address: Operational Base + offset (0x0298)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_vp9alfter_base<br>Base address for alfter (the address should be 128bit align).<br>Fbc mode: Vp9 after ref frame head base. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG167_VP9COUNT_BASE**

Address: Operational Base + offset (0x029c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RW | 0x00000000 | sw_vp9_count_prob_base<br>Software parse prob: Used as vp9 count write base. |
| 2:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG167_REF3_BASE**

Address: Operational Base + offset (0x029c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_refer3_base<br>Base address for reference picture index3 (the address should be 128bit align)<br>Fbc mode: H264 & hevc & avs2 ref3 head base. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG168_VP9_SEGIDLAST_BASE**

Address: Operational Base + offset (0x02a0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_vp9segidlast_base<br>Base address for vp9 last frame segment id (the address should be 128bit align). |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG168_REF4_BASE**

Address: Operational Base + offset (0x02a0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_refer4_base<br>Base address for reference picture index4 (the address should be 128bit align)<br>Fbc mode: H264 & hevc & avs2 ref4 head base. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG169_AVP9_SEGIDCUR_BASE**

Address: Operational Base + offset (0x02a4)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_vp9segidcur_base<br>Base address for vp9 cur frame segment id (the address should be 128bit align). |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG169_REF5_BASE**

Address: Operational Base + offset (0x02a4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_refer5_base<br>Base address for reference picture index5 (the address should be 128bit align)<br>Fbc mode: H264 & hevc & avs2 ref5 head base. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG170_VP9_REFCOLMV_BASE**

Address: Operational Base + offset (0x02a8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_vp9_refcolmv_base<br>Vp9 refcolmv base addr. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG170_REF6_BASE**

Address: Operational Base + offset (0x02a8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_refer6_base<br>Base address for reference picture index6 (the address should be 128bit align)<br>Fbc mode: H264 & hevc & avs2 ref6 head base. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG171_VP9_INTERCMD_BASE**

Address: Operational Base + offset (0x02ac)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_vp9_intercmd_base<br>Vp9 inter command base addr, when sw_rlc_mode is 1'b1.<br>When sw_dec_mode is VP9 and sw_rlc_mode is 1'b1, when read this register, after a frame is decoded ready or error (stream error, time out, bus error), it is the end address of the intercmd. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG171_REF7_BASE**

Address: Operational Base + offset (0x02ac)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_refer7_base<br>Base address for reference picture index7 (the address should be 128bit align)<br>Fbc mode: H264 & hevc & avs2 ref7 head base. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG172_VP9_UPDATE_PROB_WR_BASE**

Address: Operational Base + offset (0x02b0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_vp9_update_prob_wr_base<br>Hardware parse prob: Used as vp9 prob write base. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG172_H26X_REF8_BASE**

Address: Operational Base + offset (0x02b0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_refer8_base<br>Base address for reference picture index8 (the address should be 128bit align)<br>Fbc mode: H264 & hevc & avs2 ref8 head base. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG173_H26X_REF9_BASE**

Address: Operational Base + offset (0x02b4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_refer9_base<br>Base address for reference picture index9 (the address should be 128bit align)<br>Fbc mode: H264 & hevc & avs2 ref9 head base. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG174_H26X_REF10_BASE**

Address: Operational Base + offset (0x02b8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_refer10_base<br>Base address for reference picture index10 (the address should be 128bit align)<br>Fbc mode: H264 & hevc & avs2 ref10 head base. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG175_H26X_REF11_BASE**

Address: Operational Base + offset (0x02bc)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_refer11_base<br>Base address for reference picture index11 (the address should be 128bit align)<br>Fbc mode: H264 & hevc & avs2 ref11 head base. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG176_H26X_REF12_BASE**

Address: Operational Base + offset (0x02c0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_refer12_base<br>Base address for reference picture index12 (the address should be 128bit align)<br>Fbc mode: H264 & hevc & avs2 ref12 head base. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG177_H26X_REF13_BASE**

Address: Operational Base + offset (0x02c4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_refer13_base<br>Base address for reference picture index13 (the address should be 128bit align)<br>Fbc mode: H264 & hevc & avs2 ref13 head base. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG178_H26X_REF14_BASE**

Address: Operational Base + offset (0x02c8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_refer14_base<br>Base address for reference picture index14 (the address should be 128bit align)<br>Fbc mode: H264 & hevc & avs2 ref14 head base. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG179_H26X_REF15_BASE**

Address: Operational Base + offset (0x02cc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_refer15_base<br>Base address for reference picture index15 (the address should be 128bit align)<br>Fbc mode: H264 & hevc & avs2 ref15 head base. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG180_SCANLIST_ADDR**

Rockchip Confidential

Address: Operational Base + offset (0x02d0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_scanlist_addr<br>Should be align to 16byte, and will be used for h264 and hevc. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG181_COLMV_REF0_BASE**

Address: Operational Base + offset (0x02d4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_colmv_ref0_base<br>Only valid when sw_colmv_mode is 1'b1.<br>Ref0 frame colmv base addr.<br>For H264 and HEVC. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG182_COLMV_REF1_BASE**

Address: Operational Base + offset (0x02d8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_colmv_ref1_base<br>Only valid when sw_colmv_mode is 1'b1.<br>Ref1 frame colmv base addr.<br>For H264 and HEVC. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG183_COLMV_REF2_BASE**

Address: Operational Base + offset (0x02dc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_colmv_ref2_base<br>Only valid when sw_colmv_mode is 1'b1.<br>Ref2 frame colmv base addr.<br>For H264 and HEVC. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG184_COLMV_REF3_BASE**

Address: Operational Base + offset (0x02e0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_colmv_ref3_base<br>Only valid when sw_colmv_mode is 1'b1.<br>Ref3 frame colmv base addr.<br>For H264 and HEVC. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG185_COLMV_REF4_BASE**

Address: Operational Base + offset (0x02e4)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_colmv_ref4_base<br>Only valid when sw_colmv_mode is 1'b1.<br>Ref4 frame colmv base addr.<br>For H264 and HEVC. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG186_COLMV_REF5_BASE**

Address: Operational Base + offset (0x02e8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_colmv_ref5_base<br>Only valid when sw_colmv_mode is 1'b1.<br>Ref5 frame colmv base addr.<br>For H264 and HEVC. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG187_COLMV_REF6_BASE**

Address: Operational Base + offset (0x02ec)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_colmv_ref6_base<br>Only valid when sw_colmv_mode is 1'b1.<br>Ref6 frame colmv base addr.<br>For H264 and HEVC. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG188_COLMV_REF7_BASE**

Address: Operational Base + offset (0x02f0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_colmv_ref7_base<br>Only valid when sw_colmv_mode is 1'b1.<br>Ref7 frame colmv base addr.<br>For H264 and HEVC. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG189_COLMV_REF8_BASE**

Address: Operational Base + offset (0x02f4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_colmv_ref8_base<br>Only valid when sw_colmv_mode is 1'b1.<br>Ref8 frame colmv base addr.<br>For H264 and HEVC. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG190_COLMV_REF9_BASE**

Rockchip Confidencial

Address: Operational Base + offset (0x02f8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_colmv_ref9_base<br>Only valid when sw_colmv_mode is 1'b1.<br>Ref9 frame colmv base addr.<br>For H264 and HEVC. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG191_COLMV_REF10_BASE**

Address: Operational Base + offset (0x02fc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_colmv_ref10_base<br>Only valid when sw_colmv_mode is 1'b1.<br>Ref10 frame colmv base addr.<br>For H264 and HEVC. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG192_COLMV_REF11_BASE**

Address: Operational Base + offset (0x0300)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_colmv_ref11_base<br>Only valid when sw_colmv_mode is 1'b1.<br>Ref11 frame colmv base addr.<br>For H264 and HEVC. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG193_COLMV_REF12_BASE**

Address: Operational Base + offset (0x0304)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_colmv_ref12_base<br>Only valid when sw_colmv_mode is 1'b1.<br>Ref12 frame colmv base addr.<br>For H264 and HEVC. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG194_COLMV_REF13_BASE**

Address: Operational Base + offset (0x0308)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_colmv_ref13_base<br>Only valid when sw_colmv_mode is 1'b1.<br>Ref13 frame colmv base addr.<br>For H264 and HEVC. |
| 3:0 | RO | 0x0 | Reserved |

Rockchip Confidencial

**RKVDEC_SWREG195_COLMV_REF14_BASE**

Address: Operational Base + offset (0x030c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_colmv_ref14_base<br>Only valid when sw_colmv_mode is 1'b1.<br>Ref14 frame colmv base addr.<br>For H264 and HEVC. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG196_COLMV_REF15_BASE**

Address: Operational Base + offset (0x0310)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_colmv_ref15_base<br>Only valid when sw_colmv_mode is 1'b1.<br>Ref15 frame colmv base addr.<br>For H264 and HEVC. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG197_CABACTBL_BASE**

Address: Operational Base + offset (0x0314)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_cabactbl_base<br>Hevc & H264: The base address of cabac table. |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG198_SCALE_DOWN_LUMA_BASE**

Address: Operational Base + offset (0x0318)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_scale_down_luma_base<br>The base address of luma base |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG199_SCALE_DOWN_CHRO_BASE**

Address: Operational Base + offset (0x031c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_scale_down_chro_base<br>The base address of scale down chro base |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_SWREG200_REF_POC_HIGHBIT_P0**

Address: Operational Base + offset (0x0320)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RW | 0x0 | sw_ref7_poc_highbit<br>Sw_ref7_poc_highbit |
| 27:24 | RW | 0x0 | sw_ref6_poc_highbit<br>Sw_ref6_poc_highbit |
| 23:20 | RW | 0x0 | sw_ref5_poc_highbit<br>Sw_ref5_poc_highbit |
| 19:16 | RW | 0x0 | sw_ref4_poc_highbit<br>Sw_ref4_poc_highbit |
| 15:12 | RW | 0x0 | sw_ref3_poc_highbit<br>Sw_ref3_poc_highbit |
| 11:8 | RW | 0x0 | sw_ref2_poc_highbit<br>Sw_ref2_poc_highbit |
| 7:4 | RW | 0x0 | sw_ref1_poc_highbit<br>Sw_ref1_poc_highbit |
| 3:0 | RW | 0x0 | sw_ref0_poc_highbit<br>Sw_ref0_poc_highbit |

**RKVDEC_SWREG201_REF_POC_HIGHBIT_P1**

Address: Operational Base + offset (0x0324)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RW | 0x0 | sw_ref15_poc_highbit<br>Sw_ref15_poc_highbit |
| 27:24 | RW | 0x0 | sw_ref14_poc_highbit<br>Sw_ref14_poc_highbit |
| 23:20 | RW | 0x0 | sw_ref13_poc_highbit<br>Sw_ref13_poc_highbit |
| 19:16 | RW | 0x0 | sw_ref12_poc_highbit<br>Sw_ref12_poc_highbit |
| 15:12 | RW | 0x0 | sw_ref11_poc_highbit<br>Sw_ref11_poc_highbit |
| 11:8 | RW | 0x0 | sw_ref10_poc_highbit<br>Sw_ref10_poc_highbit |
| 7:4 | RW | 0x0 | sw_ref9_poc_highbit<br>Sw_ref9_poc_highbit |
| 3:0 | RW | 0x0 | sw_ref8_poc_highbit<br>Sw_ref8_poc_highbit |

**RKVDEC_SWREG202_REF_POC_HIGHBIT_P2**

Address: Operational Base + offset (0x0328)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RW | 0x0 | sw_ref23_poc_highbit<br>Sw_ref23_poc_highbit |
| 27:24 | RW | 0x0 | sw_ref22_poc_highbit<br>Sw_ref22_poc_highbit |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:20 | RW | 0x0 | sw_ref21_poc_highbit<br>Sw_ref21_poc_highbit |
| 19:16 | RW | 0x0 | sw_ref20_poc_highbit<br>Sw_ref20_poc_highbit |
| 15:12 | RW | 0x0 | sw_ref19_poc_highbit<br>Sw_ref19_poc_highbit |
| 11:8 | RW | 0x0 | sw_ref18_poc_highbit<br>Sw_ref18_poc_highbit |
| 7:4 | RW | 0x0 | sw_ref17_poc_highbit<br>Sw_ref17_poc_highbit |
| 3:0 | RW | 0x0 | sw_ref16_poc_highbit<br>Sw_ref16_poc_highbit |

**RKVDEC_SWREG203_REF_POC_HIGHBIT_P3**

Address: Operational Base + offset (0x032c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RW | 0x0 | sw_ref31_poc_highbit<br>Sw_ref31_poc_highbit |
| 27:24 | RW | 0x0 | sw_ref30_poc_highbit<br>Sw_ref30_poc_highbit |
| 23:20 | RW | 0x0 | sw_ref29_poc_highbit<br>Sw_ref29_poc_highbit |
| 19:16 | RW | 0x0 | sw_ref28_poc_highbit<br>Sw_ref28_poc_highbit |
| 15:12 | RW | 0x0 | sw_ref27_poc_highbit<br>Sw_ref27_poc_highbit |
| 11:8 | RW | 0x0 | sw_ref26_poc_highbit<br>Sw_ref26_poc_highbit |
| 7:4 | RW | 0x0 | sw_ref25_poc_highbit<br>Sw_ref25_poc_highbit |
| 3:0 | RW | 0x0 | sw_ref24_poc_highbit<br>Sw_ref24_poc_highbit |

**RKVDEC_SWREG204_CUR_POC_HIGHBIT**

Address: Operational Base + offset (0x0330)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0 | Reserved |
| 3:0 | RW | 0x0 | sw_cur_poc_highbit<br>Sw_cur_poc_highbit |

**RKVDEC_SWREG224_STA_INT**

Address: Operational Base + offset (0x0380)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x0 | Reserved |
| 9 | RW | 0x0 | sw_softreset_rdy<br>When it is 1'b1, it says that softreset has been done. |
| 8 | RW | 0x0 | sw_cabu_end_sta<br>Hevc: Cabac decode end status.<br>H264 & vp9 : Streamd decode status. |
| 7 | RW | 0x0 | Sw_colmv_ref_error_sta<br>Hevc & vp9: When it is 1'b1, it means that inter module read the invalid dpb frame.<br>It will self reset the hardware.<br>H264: When it is 1'b1, it means that inter module read the invalid dpb frame. When sw_h264_error_mode is 1'b0, it will self reset the hardware, otherwise it will not. |
| 6 | RW | 0x0 | sw_buf_empty_sta<br>Buffer empty status, only when sw_buf_empty_en is 1'b1 , this bit is valid, now is for no valid. |
| 5 | RW | 0x0 | sw_dec_timeout_sta<br>When high the decoder has been idling for too long. It will self reset the hardware<br>only when sw_dec_timeout_e is 1'b1, this bit is valid. |
| 4 | RW | 0x0 | sw_dec_error_sta<br>Hevc & vp9: When high, an error is found in input data stream decoding. It will self reset the hardware.<br>H264: When high, an error is found in input data stream decoding. When sw_h264_error_mode is 1'b0, it will self reset the hardware, otherwise it will not. |
| 3 | RW | 0x0 | sw_dec_bus_sta<br>When this bit is high, there is error on the axi bus, it will self reset hardware. |
| 2 | RW | 0x0 | sw_dec_rdy_sta<br>When this bit is high, decoder has decoded a picture( the loop filter module send out a frame rdy). |
| 1 | RW | 0x0 | sw_dec_irq_raw<br>The raw status of sw_dec_irq,SW should reset this bit after interrupt is handled. |
| 0 | RW | 0x0 | sw_dec_irq<br>When high, decoder requests an interrrupt.<br>Sw_dec_irq = sw_dec_irq_raw && (sw_dec_irq_dis == 1'b0). |

**RKVDEC_SWREG225_STA_ERR_INFO**

Address: Operational Base + offset (0x0384)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x0 | Reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | sw_strmd_detect_error_sta<br>Streamd logic error detected, it will stop decode. |
| 0 | RW | 0x0 | sw_dec_frame_error_sta<br>1'b1: All frame ctu error. |

**RKVDEC_SWREG226_STA_CABAC_ERROR_STATUS**

Address: Operational Base + offset (0x0388)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | Reserved |
| 27:0 | RW | 0x0000000 | Sw_cabac_error_status<br>In HEVC & H264, it is called cabac error status. |

**RKVDEC_SWREG227_STA_COLMV_ERROR_REF_PICIDX**

Address: Operational Base + offset (0x038c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0 | Reserved |
| 3:0 | RW | 0x0 | sw_colmv_ref_picidx<br>When sw_colmv_ref_error_sta is 1'b1, these bits are used for tell which dpb frame is invalid but is read by inter module.<br>It is for H264 and HEVC. |

**RKVDEC_SWREG228_STA_CABAC_ERROR_CTU_OFFSET**

Address: Operational Base + offset (0x0390)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | Reserved |
| 27:16 | RW | 0x000 | sw_cabac_error_ctu_offset_y<br>For all HEVC and H264 and VP9.<br>For vp9, it is the value of stsw_vp9_error_ctu0_y,stsw_vp9_error_ctu0_x. |
| 15:12 | RO | 0x0 | Reserved |
| 11:0 | RW | 0x000 | sw_cabac_error_ctu_offset_x<br>For all HEVC and H264 and VP9.<br>For vp9, it is the value of stsw_vp9_error_ctu0_y,stsw_vp9_error_ctu0_x. |

**RKVDEC_SWREG229_STA_SAOWR_CTU_OFFSET**

Address: Operational Base + offset (0x0394)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | sw_saowr_yoffset<br>Saowr y offset , its unit is 4 line pixel.<br>16'd0: Sao begin to write 0~3 pic line.<br>16'd1: Sao begin to write 4-7 pic line.<br>.....<br>Only valid when ip has any error. |
| 15:0 | RW | 0x0000 | sw_saowr_xoffet<br>Saowr x address offset, its unit is 128bit.<br>16'd0: Sao begin to write cur line first 128bit.<br>16'd1: Sao begin to write cur line second 128bit.<br>.....<br>Only valid when ip has any error. |

**RKVDEC_SWREG230_STA_SLICE_DEC_NUM**

Address: Operational Base + offset (0x0398)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x0 | Reserved |
| 24:0 | RO | 0x0000000 | sw_slicedec_num<br>H264 decoded num, the max slice num for H264 is 4096. |

**RKVDEC_SWREG231_STA_FRAME_ERROR_CTU_NUM**

Address: Operational Base + offset (0x039c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x0 | Reserved |
| 23:0 | RW | 0x000000 | sw_frame_ctu_error_num<br>H264 and hevc error ctu number |

**RKVDEC_SWREG232_STA_ERROR_PACKET_NUM**

Address: Operational Base + offset (0x03a0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x0 | Reserved |
| 23:0 | RW | 0x000000 | Sw_error_packet_num<br>Error packet number. |

**RKVDEC_SWREG233_STA_ERR_CTU_NUM_IN_ROI**

Address: Operational Base + offset (0x03a4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x0 | Reserved |
| 23:0 | RO | 0x000000 | sw_error_ctu_num_in_roi<br>The error ctu num in roi. |

**RKVDEC_SWREG256_DEBUG_PERF_LATENCY_CTRL0**

Address: Operational Base + offset (0x0400)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | Reserved |
| 27:16 | RW | 0x000 | sw_rd_latency_thr<br>Rd channel latency threshold. |
| 15:12 | RO | 0x0 | Reserved |
| 11:4 | RW | 0x00 | sw_rd_latency_id<br>Rd channel id for performance test. |
| 3 | RW | 0x0 | sw_axi_cnt_type<br>1'b0: Axi transfer num count.<br>1'b1: Ddr align transfer num count. |
| 2 | RO | 0x0 | Reserved |
| 1 | RW | 0x0 | Sw_axi_perf_clr<br>1'b0: Software clear disable.<br>1'b1: Software clear enalbe.<br>Clear pulse. |
| 0 | RW | 0x0 | sw_axi_perf_work_e<br>1'b0: Disable<br>1'b1: Enable |

**RKVDEC_SWREG257_DEBUG_PERF_LATENCY_CTRL1**

Address: Operational Base + offset (0x0404)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x0 | Reserved |
| 24 | RW | 0x0 | sw_rd_band_width_mode<br>1'b0: Cal all id.<br>1'b1: Cal sw_ar_count_id. |
| 23:16 | RW | 0x00 | sw_aw_count_id<br>Sw_aw_count_id |
| 15:12 | RO | 0x0 | Reserved |
| 11:4 | RW | 0x00 | sw_ar_count_id<br>Sw_ar_count_id |
| 3 | RW | 0x0 | sw_aw_cnt_id_type<br>1'b0: Count all wr-channels.<br>1'b1: Count sw_wr_cont_id wr-channel only. |
| 2 | RW | 0x0 | sw_ar_cnt_id_type<br>1'b0: Count all rd-channels.<br>1'b1: Count sw_ar_cont_id rd-channel only. |
| 1:0 | RW | 0x0 | sw_addr_align_type<br>2'd0: 16 byte align.<br>2'd1: 32byte align.<br>2'd2: 64byte align.<br>2'd3: 128byte align. |

**RKVDEC_SWREG258_DEBUG_PERF_RD_MAX_LATENCY_NUM**

Address: Operational Base + offset (0x0408)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RO | 0x0000 | sw_rd_max_latency_num<br>Read max latency number. |

**RKVDEC_SWREG259_PERF_RD_LATENCY_SAMP_NUM**

Address: Operational Base + offset (0x040c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | sw_perf_rd_latency_samp_num<br>The number of bigger than configed threshold value. |

**RKVDEC_SWREG260_DEBUG_PERF_RD_LATENCY_ACC_SUM**

Address: Operational Base + offset (0x0410)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | sw_rd_latency_acc_sum<br>Total sample number. |

**RKVDEC_SWREG261_DEBUG_PERF_RD_AXI_TOTAL_BYTE**

Address: Operational Base + offset (0x0414)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | sw_perf_rd_axi_total_byte<br>The bandwidth of total read bytes. |

**RKVDEC_SWREG262_DEBUG_PERF_WR_AXI_TOTAL_BYTE**

Address: Operational Base + offset (0x0418)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | sw_perf_wr_axi_total_byte<br>The bandwidth of total write bytes. |

**RKVDEC_SWREG263_DEBUG_PERF_WORKING_CNT**

Address: Operational Base + offset (0x041c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | sw_perf_working_cnt<br>The total running cycle of current frame. |

**RKVDEC_SWREG265_DEBUG_PERF_SEL**

Address: Operational Base + offset (0x0424)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x0 | Reserved |

Rockchip Confidencial

| | | | |
|---|---|---|---|
| 21:16 | RW | 0x00 | sw_perf_cnt2_sel<br>6'd0: Don't work.<br>6'd1: Cycles counter for cabac in buffer empty.<br>6'd2: Cycles counter for cabac in buffer full;(may be alwasys will be 0).<br>6'd3: Cycles counter for cabac out buffer empty.<br>6'd4: Cycles counter for cabac out buffer full.<br>6'd5: Cycles counter for transd input data ready.<br>6'd6: Cycles counter for transd write data to recon allow.<br>6'd7: Cycles counter for dec2transd cmd empty.<br>6'd8: Cycles counter for dec2transd cmd full.<br>6'd9: Cycles counter for transd2dblk bs fifo empty.<br>6'd10: Cycles counter for transd2dblk bs fifo full.<br>6'd11: Cycles counter for dec2intra cmd fifo empty.<br>6'd12: Cycles counter for dec2intra cmd fifo full.<br>6'd13: Cycles counter for mc2recon cmd fifo empty.<br>6'd14: Cycles counter for mc2recon cmd fifo full.<br>6'd15: Cycles counter for mc2recon data fifo empty.<br>6'd16: Cycles counter for mc2recon data fifo full.<br>6'd17: Cycles counter for recon2filter data write allow.<br>6'd18: Cycles counter for inter2busifd cmd fifo empty.<br>6'd19: Cycles counter for inter2busifd cmd fifo full.<br>6'd20: Cycles counter for busifd2mc data fifo empty.<br>6'd21: Cycles counter for busifd2mc data fifo full.<br>6'd22: Cycles counter for bus un-working status(idle status).<br>6'd23: Cycles counter for dec2inter cmd fifo empty.<br>6'd24: Cycles counter for dec2inter cmd fifo full.<br>6'd25: Cycles counter for inter2mc cmd fifo empty.<br>6'd26: Cycles counter for inter2mc cmd fifo full.<br>6'd27: Cycles counter for inter2dblk bs fifo empty.<br>6'd28: Cycles counter for inter2dblk bs fifo full.<br>6'd29: Cycles counter for colmv_rbuf_empty.<br>6'd30: Cycles counter for colmv_rbuf_full.<br>6'd31: Cycles counter for colmv_wbuf_empty.<br>6'd32: Cycles counter for colmv_wbuf_da_full.<br>6'd33: Cycles counter for dblk work status.<br>6'd34: Cycles counter for dblk work status.<br>6'd35: Cycles counter for dec2loopfilter cmd fifo empty.<br>6'd36: Cycles counter for dec2loopfilter cmd fifo full.<br>6'd37: Cycles counter for sao input data valid.<br>6'd38: Cycles counter for busifd hold back sao write data.<br>6'd39: Cycles counter for bus process writing output buffer data.<br>6'd40: Counter for dec_ctrl read cmd num.<br>6'd41: Error ctu num when stream error happen.<br>6'd42: Inter reflist idx which be used flag.<br>6'd43: Pu num, 4*4 unit. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| | | | 6'd44: mv_y_min[15:0], mv_x_min[15:0].<br>6'd45: mv_y_max[15:0], mv_x_max[15:0].<br>6'd46: The sum value of mv_x lowbits,sum_mv_x[31:0].<br>6'd47: The sum value of mv_y lotbits, sum_mv_y[31:0].<br>6'd48: The sum value of \|mv_x\| lowbits, sum_abs_mv_x[31:0].<br>6'd49: The sum value of \|mv_y\| lowbits, sum_abs_mv_x[31:0].<br>6'd50: The sum value of mv high bits, sum_abs_mv_y[40:32], sum_abs_mv_x[40:32], sum_mv_y[40:32], sum_mv_x[40:32].<br>6'd51: The cu skip num, unit is 8*8.<br>6'd52: The tu skip num, unit is 4*4.<br>6'd53: The max qp of tu, 8'h0, cr_qp_max[7:0], cb_qp_max[7:0], luma_qp_max[7:0].<br>6'd54: The min qp of tu, 8'h0, cr_qp_min[7:0], cb_qp_min[7:0], luma_qp_min[7:0].<br>6'd55: The sum of luma qp, unit is 4*4.<br>6'd56: The sum of cb qp, unit is 4*4.<br>6'd57: The sum of cr qp, unit is 4*4.<br>6'd58: The count of mv_x.<br>6'd59: The count of mv_y. |
| 15:14 | RO | 0x0 | Reserved |

Rockchip Confidencial

| | | | |
|---|---|---|---|
| 13:8 | RW | 0x00 | sw_perf_cnt1_sel<br>6'd0: Don't work.<br>6'd1: Cycles counter for cabac in buffer empty.<br>6'd2: Cycles counter for cabac in buffer full;(may be alwasys will be 0).<br>6'd3: Cycles counter for cabac out buffer empty.<br>6'd4: Cycles counter for cabac out buffer full.<br>6'd5: Cycles counter for transd input data ready.<br>6'd6: Cycles counter for transd write data to recon allow.<br>6'd7: Cycles counter for dec2transd cmd empty.<br>6'd8: Cycles counter for dec2transd cmd full.<br>6'd9: Cycles counter for transd2dblk bs fifo empty.<br>6'd10: Cycles counter for transd2dblk bs fifo full.<br>6'd11: Cycles counter for dec2intra cmd fifo empty.<br>6'd12: Cycles counter for dec2intra cmd fifo full.<br>6'd13: Cycles counter for mc2recon cmd fifo empty.<br>6'd14: Cycles counter for mc2recon cmd fifo full.<br>6'd15: Cycles counter for mc2recon data fifo empty.<br>6'd16: Cycles counter for mc2recon data fifo full.<br>6'd17: Cycles counter for recon2filter data write allow.<br>6'd18: Cycles counter for inter2busifd cmd fifo empty.<br>6'd19: Cycles counter for inter2busifd cmd fifo full.<br>6'd20: Cycles counter for busifd2mc data fifo empty.<br>6'd21: Cycles counter for busifd2mc data fifo full.<br>6'd22: Cycles counter for bus un-working status(idle status).<br>6'd23: Cycles counter for dec2inter cmd fifo empty.<br>6'd24: Cycles counter for dec2inter cmd fifo full.<br>6'd25: Cycles counter for inter2mc cmd fifo empty.<br>6'd26: Cycles counter for inter2mc cmd fifo full.<br>6'd27: Cycles counter for inter2dblk bs fifo empty.<br>6'd28: Cycles counter for inter2dblk bs fifo full.<br>6'd29: Cycles counter for colmv_rbuf_empty.<br>6'd30: Cycles counter for colmv_rbuf_full.<br>6'd31: Cycles counter for colmv_wbuf_empty.<br>6'd32: Cycles counter for colmv_wbuf_da_full.<br>6'd33: Cycles counter for dblk work status.<br>6'd34: Cycles counter for dblk work status.<br>6'd35: Cycles counter for dec2loopfilter cmd fifo empty.<br>6'd36: Cycles counter for dec2loopfilter cmd fifo full.<br>6'd37: Cycles counter for sao input data valid.<br>6'd38: Cycles counter for busifd hold back sao write data.<br>6'd39: Cycles counter for bus process writing output buffer data.<br>6'd40: Counter for dec_ctrl read cmd num.<br>6'd41: Error ctu num when stream error happen.<br>6'd42: Inter reflist idx which be used flag.<br>6'd43: Pu num, 4*4 unit. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| | | | 6'd44: mv_y_min[15:0], mv_x_min[15:0].<br>6'd45: mv_y_max[15:0], mv_x_max[15:0].<br>6'd46: The sum value of mv_x lowbits,sum_mv_x[31:0].<br>6'd47: The sum value of mv_y lotbits, sum_mv_y[31:0].<br>6'd48: The sum value of \|mv_x\| lowbits, sum_abs_mv_x[31:0].<br>6'd49: The sum value of \|mv_y\| lowbits, sum_abs_mv_x[31:0].<br>6'd50: The sum value of mv high bits, sum_abs_mv_y[40:32], sum_abs_mv_x[40:32], sum_mv_y[40:32], sum_mv_x[40:32].<br>6'd51: The cu skip num, unit is 8*8.<br>6'd52: The tu skip num, unit is 4*4.<br>6'd53: The max qp of tu, 8'h0, cr_qp_max[7:0], cb_qp_max[7:0], luma_qp_max[7:0].<br>6'd54: The min qp of tu, 8'h0, cr_qp_min[7:0], cb_qp_min[7:0], luma_qp_min[7:0].<br>6'd55: The sum of luma qp, unit is 4*4.<br>6'd56: The sum of cb qp, unit is 4*4.<br>6'd57: The sum of cr qp, unit is 4*4.<br>6'd58: The count of mv_x.<br>6'd59: The count of mv_y. |
| 7:6 | RO | 0x0 | Reserved |

Rockchip Confidencial

| | | | |
|---|---|---|---|
| 5:0 | RW | 0x00 | sw_perf_cnt0_sel<br>6'd0: Don't work.<br>6'd1: Cycles counter for cabac in buffer empty.<br>6'd2: Cycles counter for cabac in buffer full;(may be alwasys will be 0).<br>6'd3: Cycles counter for cabac out buffer empty.<br>6'd4: Cycles counter for cabac out buffer full.<br>6'd5: Cycles counter for transd input data ready.<br>6'd6: Cycles counter for transd write data to recon allow.<br>6'd7: Cycles counter for dec2transd cmd empty.<br>6'd8: Cycles counter for dec2transd cmd full.<br>6'd9: Cycles counter for transd2dblk bs fifo empty.<br>6'd10: Cycles counter for transd2dblk bs fifo full.<br>6'd11: Cycles counter for dec2intra cmd fifo empty.<br>6'd12: Cycles counter for dec2intra cmd fifo full.<br>6'd13: Cycles counter for mc2recon cmd fifo empty.<br>6'd14: Cycles counter for mc2recon cmd fifo full.<br>6'd15: Cycles counter for mc2recon data fifo empty.<br>6'd16: Cycles counter for mc2recon data fifo full.<br>6'd17: Cycles counter for recon2filter data write allow.<br>6'd18: Cycles counter for inter2busifd cmd fifo empty.<br>6'd19: Cycles counter for inter2busifd cmd fifo full.<br>6'd20: Cycles counter for busifd2mc data fifo empty.<br>6'd21: Cycles counter for busifd2mc data fifo full.<br>6'd22: Cycles counter for bus un-working status(idle status).<br>6'd23: Cycles counter for dec2inter cmd fifo empty.<br>6'd24: Cycles counter for dec2inter cmd fifo full.<br>6'd25: Cycles counter for inter2mc cmd fifo empty.<br>6'd26: Cycles counter for inter2mc cmd fifo full.<br>6'd27: Cycles counter for inter2dblk bs fifo empty.<br>6'd28: Cycles counter for inter2dblk bs fifo full.<br>6'd29: Cycles counter for colmv_rbuf_empty.<br>6'd30: Cycles counter for colmv_rbuf_full.<br>6'd31: Cycles counter for colmv_wbuf_empty.<br>6'd32: Cycles counter for colmv_wbuf_da_full.<br>6'd33: Cycles counter for dblk work status.<br>6'd34: Cycles counter for dblk work status.<br>6'd35: Cycles counter for dec2loopfilter cmd fifo empty.<br>6'd36: Cycles counter for dec2loopfilter cmd fifo full.<br>6'd37: Cycles counter for sao input data valid.<br>6'd38: Cycles counter for busifd hold back sao write data.<br>6'd39: Cycles counter for bus process writing output buffer data.<br>6'd40: Counter for dec_ctrl read cmd num.<br>6'd41: Error ctu num when stream error happen.<br>6'd42: Inter reflist idx which be used flag.<br>6'd43: Pu num, 4*4 unit. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| | | | 6'd44: mv_y_min[15:0], mv_x_min[15:0].<br>6'd45: mv_y_max[15:0], mv_x_max[15:0].<br>6'd46: The sum value of mv_x lowbits,sum_mv_x[31:0].<br>6'd47: The sum value of mv_y lotbits, sum_mv_y[31:0].<br>6'd48: The sum value of \|mv_x\| lowbits, sum_abs_mv_x[31:0].<br>6'd49: The sum value of \|mv_y\| lowbits, sum_abs_mv_x[31:0].<br>6'd50: The sum value of mv high bits, sum_abs_mv_y[40:32], sum_abs_mv_x[40:32], sum_mv_y[40:32], sum_mv_x[40:32].<br>6'd51: The cu skip num, unit is 8*8.<br>6'd52: The tu skip num, unit is 4*4.<br>6'd53: The max qp of tu, 8'h0, cr_qp_max[7:0], cb_qp_max[7:0], luma_qp_max[7:0].<br>6'd54: The min qp of tu, 8'h0, cr_qp_min[7:0], cb_qp_min[7:0], luma_qp_min[7:0].<br>6'd55: The sum of luma qp, unit is 4*4.<br>6'd56: The sum of cb qp, unit is 4*4.<br>6'd57: The sum of cr qp, unit is 4*4.<br>6'd58: The count of mv_x.<br>6'd59: The count of mv_y. |

**RKVDEC_SWREG266_DEBUG_PERF_CNT0**

Address: Operational Base + offset (0x0428)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | sw_perf_cnt0<br>Performance count value0 |

**RKVDEC_SWREG267_DEBUG_PERF_CNT1**

Address: Operational Base + offset (0x042c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | sw_perf_cnt1<br>Performance count value1. |

**RKVDEC_SWREG268_DEBUG_PERF_CNT2**

Address: Operational Base + offset (0x0430)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | sw_perf_cnt2<br>Performance count value2. |

**RKVDEC_SWREG269_VP9_ERROR_INFO**

Address: Operational Base + offset (0x0434)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | sw_vp9_error_ctu1_en<br>If the error ctu offset be valid. |
| 30:26 | RO | 0x0 | Reserved |
| 25:16 | RW | 0x000 | Sw_vp9_error_ctu1_y<br>The error ctu offset y |
| 15:10 | RO | 0x0 | Reserved |
| 9:0 | RW | 0x000 | Sw_vp9_error_ctu1_x<br>The error ctu offset x |

**RKVDEC_SWREG270_DEBUG_QOS_CTRL**

Address: Operational Base + offset (0x0438)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | Reserved |
| 30:28 | RW | 0x0 | sw_axi_rd_qos<br>axi_rd_qos |
| 27 | RO | 0x0 | Reserved |
| 26:24 | RW | 0x0 | sw_axi_rd_hurry_level<br>2'b00: Hurry off.<br>2'b01~2'b11: Hurry level. |
| 23 | RO | 0x0 | Reserved |
| 22:20 | RW | 0x0 | sw_axi_wr_qos<br>axi wr qos |
| 19 | RO | 0x0 | Reserved |
| 18:16 | RW | 0x0 | sw_axi_wr_hurry_level<br>2'b00: Hurry off.<br>2'b01~2'b11: Hurry level. |
| 15:8 | RO | 0x0 | Reserved |
| 7:0 | RW | 0x00 | sw_bus2mc_buf_qos_level<br>Range is: 0~255.<br>The value is means that sw_bus2mc_buffer_qos_level <= left space, it will give hurry. |

**RKVDEC_SWREG271_DEBUG_WAIT_CYCLE_QOS**

Address: Operational Base + offset (0x043c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_wr_hurry_wait_cycle<br>Hw find sw_wr_wait_cycle_qos cycle can't wr to ddr,it will give hurry. |

**RKVDEC_SWREG272_DEBUG_INT**

Address: Operational Base + offset (0x0440)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x0 | Reserved |
| 22:16 | RO | 0x00 | sw_streamfifo_space2full<br>It is for debug use, to tell the stream fifo space to full.<br>For HEVC , H264 and VP9. |
| 15:12 | RO | 0x0 | Reserved |
| 11:6 | RO | 0x00 | sw_wr_tansfer_cnt<br>Sw_wr_tansfer_cnt |
| 5 | RO | 0x0 | sw_stream_rdburst_cnteq0_towr<br>Sw_wr_tansfer_cnt |
| 4 | RO | 0x0 | sw_cabu_rlcend_valid_real<br>Sw_colmvwr_frame_rdy_real |
| 3 | RO | 0x0 | sw_colmvwr_frame_rdy_real<br>Sw_colmvwr_frame_rdy_real |
| 2 | RO | 0x0 | sw_saobu_frame_rdy_valid<br>Sw_saobu_frame_rdy_valid |
| 1 | RO | 0x0 | sw_saowr_frame_rdy<br>Sw_saowr_frame_rdy |
| 0 | RO | 0x0 | sw_bu_rw_clean<br>1'b0: Bus busy.<br>1'b1: Bus idle. |

**RKVDEC_SWREG273_STA_B_FRAME_FLAG**

Address: Operational Base + offset (0x0444)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | Sw_pps_no_ref_bframe_dec_r<br>1'b1: Find this frame is not referace B frame. |
| 30:25 | RO | 0x0 | Reserved |
| 24:0 | RO | 0x0000000 | Sw_bus_status_flag<br>sw_bus_status_flag |

**RKVDEC_SWREG274_PIX_RANGE_Y**

Address: Operational Base + offset (0x0448)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x0 | Reserved |
| 25:16 | RO | 0x000 | Sw_y_max_value<br>The max value of luma |
| 15:10 | RO | 0x0 | Reserved |
| 9:0 | RW | 0x000 | Sw_y_min_value<br>The min value of luma |

**RKVDEC_SWREG275_PIX_RANGE_U**

Address: Operational Base + offset (0x044c)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x0 | Reserved |
| 25:16 | RO | 0x000 | sw_u_max_value<br>The max value of chroma u |
| 15:10 | RO | 0x0 | Reserved |
| 9:0 | RO | 0x000 | sw_u_min_value<br>The min value of chroma u |

**RKVDEC_SWREG276_PIX_RANGE_V**

Address: Operational Base + offset (0x0450)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x0 | Reserved |
| 25:16 | RW | 0x000 | sw_v_max_value<br>The max value of chroma v |
| 15:10 | RO | 0x0 | Reserved |
| 9:0 | RO | 0x000 | sw_v_min_value<br>The min value of chroma v |

**RKVDEC_SWREG277_ERROR_SPREAD_NUM**

Address: Operational Base + offset (0x0454)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x0 | Reserved |
| 23:0 | RW | 0x000000 | sw_err_spread_cnt_sum<br>current frame error counters at ctu unit<br>active when sw_error_spread_e is 1 |

## 5.5.11 VDPU381 CCU Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKVDEC_CCU_SWREG0_CCU_CTRL | 0x0000 | W | 0x00000000 | Ccu ctrl cfg |
| RKVDEC_CCU_SWREG1_CCU_CFG_START_ADDR | 0x0004 | W | 0x00000000 | The address of register data |
| RKVDEC_CCU_SWREG2_CCU_LINK_MODE | 0x0008 | W | 0x00000000 | The LLP table add ctrl |
| RKVDEC_CCU_SWREG3_CCU_CONFIG_DONE | 0x000c | W | 0x00000000 | Config finish ctrl register |
| RKVDEC_CCU_SWREG4_CCU_DECODERED_NUM | 0x0010 | W | 0x00000000 | The frame number which have been decodered |
| RKVDEC_CCU_SWREG5_CCU_DEC_TOTAL_NUM | 0x0014 | W | 0x00000000 | The total needed decoder number |
| RKVDEC_CCU_SWREG6_CCU_WORK_EN | 0x0018 | W | 0x00000000 | LLP enable flag |

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKVDEC_CCU_SWREG7_CCU_CURRENT_PRC_LLP_ADDR_BASE | 0x001c | W | 0x00000000 | The address of register data |
| RKVDEC_CCU_SWREG8_CCU_VERISION | 0x0020 | W | 0x00000000 | The num of dec core |
| RKVDEC_CCU_SWREG9_CCU_SEND_NUM | 0x0024 | W | 0x00000000 | Read only |
| RKVDEC_CCU_SWREG10_CCU_TIMECNT | 0x0028 | W | 0x00000000 | Read only |
| RKVDEC_CCU_SWREG16_CCU_WORK_MODE | 0x0040 | W | 0x00000000 | Ccu work mode |
| RKVDEC_CCU_SWREG17_CCU_CORE_WORK_MODE | 0x0044 | W | 0x00000000 | Work mode cfg |
| RKVDEC_CCU_SWREG18_CCU_CORE_WORK_STA | 0x0048 | W | 0x00000000 | Must set work sta as 1 while cpu mode |
| RKVDEC_CCU_SWREG19_CCU_CORE_FORCE_IDLE_E | 0x004c | W | 0x00000000 | Force idle cfg |
| RKVDEC_CCU_SWREG20_CCU_CORE_REQ_TIMEOUT_E | 0x0050 | W | 0x00000000 | Timeout enable cfg |
| RKVDEC_CCU_SWREG21_CCU_CORE_ERR_STA | 0x0054 | W | 0x00000000 | Error status |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

## 5.5.12 VDPU381 CCU Detail Register Description

**RKVDEC_CCU_SWREG0_CCU_CTRL**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | sw_ccu_autogating_e<br>1'b0: Ccu clock will not be auto gating(default)<br>1'b1: Ccu clock will autogating when clock not be required |

**RKVDEC_CCU_SWREG1_CCU_CFG_START_ADDR**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_ccu_llp_cfg_addr<br>It should be align to 64 byte |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_CCU_SWREG2_CCU_LINK_MODE**

Address: Operational Base + offset (0x0008)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | sw_link_mode<br>1'b0: Normal mode,the first to start link mode<br>1'b1: Add extra ready frame to decoder |
| 30 | RO | 0x0 | reserved |
| 29:0 | RW | 0x00000000 | sw_pre_frame_num<br>1'b1: Config 1 frame |

**RKVDEC_CCU_SWREG3_CCU_CONFIG_DONE**

Address: Operational Base + offset (0x000c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x0 | Reserved |
| 0 | W1C | 0x0 | sw_config_done<br>After config okay,config this bit to 1 |

**RKVDEC_CCU_SWREG4_CCU_DECODERED_NUM**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | Reserved |
| 29:0 | RO | 0x00000000 | sw_decoder_num<br>The frame number which have been decodered |

**RKVDEC_CCU_SWREG5_CCU_DEC_TOTAL_NUM**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | Reserved |
| 29:0 | RO | 0x00000000 | sw_dec_total_num<br>The total needed decoder number |

**RKVDEC_CCU_SWREG6_CCU_WORK_EN**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x0 | Reserved |
| 0 | RW | 0x0 | sw_ccu_work_en<br>The enable flag of ccu |

**RKVDEC_CCU_SWREG7_CCU_CURRENT_PRC_LLP_ADDR_BASE**

Address: Operational Base + offset (0x001c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_ccu_current_prc_llp_addr_base<br>Read only |
| 3:0 | RO | 0x0 | Reserved |

**RKVDEC_CCU_SWREG8_CCU_VERISION**

Rockchip Confidencial

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | verision<br>Reserve |
| 15:8 | RO | 0x0 | Reserved |
| 7:0 | RO | 0x00 | sw_ccu_core_num<br>read only<br>How many dec cores can be used.<br>That value n is n dec cores can be used. |

**RKVDEC_CCU_SWREG9_CCU_SEND_NUM**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | Reserved |
| 29:0 | RO | 0x00000000 | sw_ccu_send_num<br>The frame number which have been send |

**RKVDEC_CCU_SWREG10_CCU_TIMECNT**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | sw_ccu_timecnt<br>Read time cnt while work_sta is invalid |

**RKVDEC_CCU_SWREG16_CCU_WORK_MODE**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | sw_ccu_work_mode<br>1'b0: Ccu auto ctrl mode<br>1'b1: Cpu ctrl mode |

**RKVDEC_CCU_SWREG17_CCU_CORE_WORK_MODE**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0 | reserved |
| 17 | RW | 0x0 | sw_core1_work_mode_wmask<br>1'b0: No allow to cfg<br>1'b1: Be allow to cfg |
| 16 | RW | 0x0 | sw_core0_work_mode_wmask<br>1'b0: No allow to cfg<br>1'b1: Be allow to cfg |
| 15:2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | sw_core1_work_mode<br>1'b0: Dec core will be used separate<br>1'b1: Dec core will ctrl by ccu |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | sw_core0_work_mode<br>1'b0: Dec core will be used separate<br>1'b1: Dec core will ctrl by ccu |

**RKVDEC_CCU_SWREG18_CCU_CORE_WORK_STA**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0 | reserved |
| 17 | RW | 0x0 | sw_core1_work_sta_wmask<br>1'b0: No allow to cfg<br>1'b1: Be allow to cfg |
| 16 | RW | 0x0 | sw_core0_work_sta_wmask<br>1'b0: No allow to cfg<br>1'b1: Be allow to cfg |
| 15:2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | sw_core1_work_sta<br>1'b0: Dec core not be ctrled by ccu or it stay at waiting to be actived<br>1'b1: Dec core has been actived,that is it was on working status |
| 0 | RW | 0x0 | sw_core0_work_sta<br>1'b0: Dec core not be ctrled by ccu or it stay at waiting to be actived<br>1'b1: Dec core has been actived,that is it was on working status |

**RKVDEC_CCU_SWREG19_CCU_CORE_FORCE_IDLE_E**

Address: Operational Base + offset (0x004c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0 | reserved |
| 17 | RW | 0x0 | sw_core1_force_idle_wmask<br>1'b0: No allow to cfg<br>1'b1: Be allow to cfg |
| 16 | RW | 0x0 | sw_core0_force_idle_wmask<br>1'b0: No allow to cfg<br>1'b1: Be allow to cfg |
| 15:2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | sw_core1_force_idle_e<br>1'b0: Core can be used<br>1'b1: When core should be reset,should config this bit to 1,force ccu core1 controller on idle status; |
| 0 | RW | 0x0 | sw_core0_force_idle_e<br>1'b0: Core can be used<br>1'b1: When core should be reset,should config this bit to 1,force ccu core0 controller on idle status; |

Rockchip Confidencial

**RKVDEC_CCU_SWREG20_CCU_CORE_REQ_TIMEOUT_E**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0 | reserved |
| 17 | RW | 0x0 | sw_core1_req_timeout_e_wmask<br>1'b0: No allow to cfg<br>1'b1: Be allow to cfg |
| 16 | RW | 0x0 | sw_core0_req_timeout_e_wmask<br>1'b0: No allow to cfg<br>1'b1: Be allow to cfg |
| 15:2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | sw_core1_req_timeout_e<br>1'b0: Ccu core1 controller can't timeout<br>1'b1: When ccu start core to work,but too long to fetch ack,it will unload such core. |
| 0 | RW | 0x0 | sw_core0_req_timeout_e<br>1'b0: Ccu core0 controller can't timeout<br>1'b1: When ccu start core to work,but too long to fetch ack,it will unload such core. |

**RKVDEC_CCU_SWREG21_CCU_CORE_ERR_STA**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0 | reserved |
| 17 | RW | 0x0 | sw_core1_err_sta_clr_wmask<br>1'b0: No allow to cfg<br>1'b1: Be allow to cfg |
| 16 | RW | 0x0 | sw_core0_err_sta_clr_wmask<br>1'b0: No allow to cfg<br>1'b1: Be allow to cfg |
| 15:2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | sw_core1_err_sta<br>1'b0: Core dec correct<br>1'b1: Some error be checked in dec core |
| 0 | RW | 0x0 | sw_core0_err_sta<br>1'b0: Core dec correct<br>1'b1: Some error be checked in dec core |

## 5.5.13 VDPU381 CACHE Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PREF_CACHE_VERSION | 0x0000 | W | 0xcac20101 | VERSION register |
| PREF_CACHE_SIZE | 0x0004 | W | 0x07100206 | L2 cache SIZE |
| PREF_CACHE_STATUS | 0x0008 | W | 0x00000000 | Status register |
| PREF_CACHE_COMMAND | 0x0010 | W | 0x00000000 | Command setting register |
| PREF_CACHE_CLEAR_PAGE | 0x0014 | W | 0x00000000 | Clear page register |
| PREF_CACHE_MAX_READS | 0x0018 | W | 0x0000001c | Maximum read register |

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PREF_CACHE_ENABLE | 0x001c | W | 0x00000003 | Enables cacheable accesses and cache read allocation |
| PREF_CACHE_PERFCNT_SRC0 | 0x0020 | W | 0x00000000 | Performance counter 0 source register |
| PREF_CACHE_PERFCNT_VAL0 | 0x0024 | W | 0x00000000 | Performance counter 0 value register |
| PREF_CACHE_PERFCNT_SRC1 | 0x0028 | W | 0x00000000 | This register holds all the possible source values for Performance Counter 00: total clock cycles1: active clock cycles2: read transactions, master3: word reads, master4: read transactions, slave5: word reads, slave6: read hit, slave7: read misses, slave8: read invalidates, slave9: cacheable read transactions, slave10: Bad hit number, slave |
| PREF_CACHE_PERFCNT_VAL1 | 0x002c | W | 0x00000000 | Performance counter 1 value register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

## 5.5.14 VDPU381 CACHE Detail Registers Description

**PREF_CACHE_VERSION**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0xcac2 | product_id<br>Minor verision |
| 15:8 | RO | 0x01 | version_major<br>Major verision |
| 7:0 | RO | 0x01 | version_minor<br>The id of product |

**PREF_CACHE_SIZE**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x07 | external_bus_width<br>Log2 external bus width in bits |
| 23:16 | RO | 0x10 | cache_size<br>Log2 cache size in bytes<br>For Y channel, its value is 0x10<br>For UV channel, its value is 0xf |
| 15:8 | RO | 0x02 | associativity<br>Log2 associativity |
| 7:0 | RO | 0x06 | line_size<br>Log2 line size in bytes |

**PREF_CACHE_STATUS**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | Reserved |
| 1 | RW | 0x0 | data_busy<br>Set when the cache is busy handling data. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | cmd_busy<br>Set when the cache is busy handling commands. |

**PREF_CACHE_COMMAND**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | Reserved |
| 5:4 | RW | 0x0 | sw_addrb_sel<br>2'b00: To sel b[14:6]<br>2'b01: To sel b[15:9], b[7:6]<br>2'b10: To sel b[16:10], b[7:6]<br>2'b11: To sel b[17:11], b[7:6] |
| 3:0 | RW | 0x0 | command<br>1'b1: Clear entire cache |

**PREF_CACHE_CLEAR_PAGE**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | WO | 0x00000000 | clear_page<br>Writing an address, invilidates all lines in that page from the cache. |

**PREF_CACHE_MAX_READS**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | Reserved |
| 4:0 | RW | 0x1c | max_reads<br>Limit the number of outstanding read transactions to this amount. |

**PREF_CACHE_ENABLE**

Address: Operational Base + offset (0x001c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | Reserved |
| 4 | RW | 0x0 | sw_cache_linsize<br>1'b0: The cache line is 32bytes<br>1'b1: The cache line is 64bytes |
| 3 | RW | 0x0 | sw_cache_clk_disgate<br>Cache clk disgate<br>When it is 1'b0, enable cache clk auto clkgating<br>When it is 1'b1, disable cache clk auto clkgating |
| 2 | RW | 0x0 | sw_readbuffer_counter_reject_en<br>Default is 1'b0, for enhance cacheable read performnace in readbuffer.<br>1'b1: Normal origin counter reject |
| 1 | RW | 0x1 | permit_cache_read_allocate<br>1'b1: Permit cache read allocate |
| 0 | RW | 0x1 | permit_cacheable_access<br>1'b1: Permit cacheable access |

**PREF_CACHE_PERFCNT_SRC0**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | Reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6:0 | RW | 0x00 | perfcnt_src0<br>This register holds all the possible source values for Performance Counter 0<br>0: Disabled<br>1: Total clock cycles<br>2: Active clock cycles<br>3: Read transactions, master<br>4: Word reads, master<br>5: Read transactions, slave<br>6: Word reads, slave<br>7: Read hit, slave<br>8: Read misses, slave<br>9: Read invalidates, slave<br>10: Cacheable read transactions, slave<br>11: Bad hit number, slave |

**PREF_CACHE_PERFCNT_VAL0**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | perfcnt_val0<br>Performance counter 0 value |

**PREF_CACHE_PERFCNT_SRC1**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | Reserved |
| 6:0 | RW | 0x00 | perfcnt_src1<br>This register holds all the possible source values for Performance Counter 1<br>0: Disabled<br>1: Total clock cycles<br>2: Active clock cycles<br>3: Read transactions, master<br>4: Word reads, master<br>5: Read transactions, slave<br>6: Word reads, slave<br>7: Read hit, slave<br>8: Read misses, slave<br>9: Read invalidates, slave<br>10: Cacheable read transactions, slave<br>11: Bad hit nmber, slave |

**PREF_CACHE_PERFCNT_VAL1**

Address: Operational Base + offset (0x002c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | perfcnt_val1<br>Performance counter 1 value |

## 5.5.15 VDPU381 MMU Registers Summary

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKVDEC_MMU_DTE_ADDR | 0x0000 | W | 0x00000000 | MMU current page Table address. It is only can be written when MMU state is disable or page fault or mmu enable stall state |
| RKVDEC_MMU_STATUS | 0x0004 | W | 0x00000018 | MMU status register |
| RKVDEC_MMU_COMMAND | 0x0008 | W | 0x00000000 | MMU command register |
| RKVDEC_MMU_PAGE_FAULT_ADDR | 0x000c | W | 0x00000000 | MMU logical address of last page fault |
| RKVDEC_MMU_ZAP_ONE_LINE | 0x0010 | W | 0x00000000 | MMU Zap cache line register |
| RKVDEC_MMU_INT_RAWSTAT | 0x0014 | W | 0x00000000 | MMU raw interrupt status register |
| RKVDEC_MMU_INT_CLEAR | 0x0018 | W | 0x00000000 | MMU raw interrupt status register |
| RKVDEC_MMU_INT_MASK | 0x001c | W | 0x00000000 | MMU raw interrupt status register |
| RKVDEC_MMU_INT_STATUS | 0x0020 | W | 0x00000000 | MMU raw interrupt status register |
| RKVDEC_MMU_AUTO_GATING | 0x0024 | W | 0x00000001 | MMU auto gating |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

## 5.5.16 VDPU381 MMU Detail Registers Description

**RKVDEC_MMU_DTE_ADDR**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | mmu_dte_addr<br>Mmu dte base addr , the address must be 4kb aligned |

**RKVDEC_MMU_STATUS**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:11 | RO | 0x000000 | Reserved |
| 10:6 | RO | 0x00 | page_fault_bus_id<br>Index of master responsible for last page fault. |
| 5 | RO | 0x0 | page_fault_is_write<br>The direction of access for last page fault:<br>1'b0: Read<br>1'b1: Write |
| 4 | RO | 0x1 | replay_buffer_empty<br>The MMU replay buffer is empty. |
| 3 | RO | 0x1 | mmu_idle<br>The MMU is idle when accesses are being translated and there are no unfinished translated accesses. |
| 2 | RO | 0x0 | stail_active<br>MMU stall mode currently enabled. The mode is enabled by command. |
| 1 | RO | 0x0 | page_fault_active<br>MMU page fault mode currently enabled. The mode is enabled by command. |
| 0 | RO | 0x0 | paging_enabled<br>Paging is enabled. |

Rockchip Confidential

**RKVDEC_MMU_COMMAND**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | Reserved |
| 2:0 | WO | 0x0 | mmu_cmd<br>MMU_CMD. This can be:<br>3'd0: MMU_ENABLE_PAGING<br>3'd1: MMU_DISABLE_PAGING<br>3'd2: MMU_ENABLE_STALL<br>3'd3: MMU_DISABLE_STALL<br>3'd4: MMU_ZAP_CACHE<br>3'd5: MMU_PAGE_FAULT_DONE<br>3'd6: MMU_FORCE_RESET<br>3'd7: Reserved |

**RKVDEC_MMU_PAGE_FAULT_ADDR**

Address: Operational Base + offset (0x000c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | page_fault_addr<br>Address of last page fault |

**RKVDEC_MMU_ZAP_ONE_LINE**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | WO | 0x00000000 | mmu_zap_one_line<br>Address to be invalidated from the page table cache |

**RKVDEC_MMU_INT_RAWSTAT**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | Reserved |
| 1 | RW | 0x0 | read_bus_error<br>Read bus error |
| 0 | RW | 0x0 | page_fault<br>Page fault |

**RKVDEC_MMU_INT_CLEAR**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | Reserved |
| 1 | WO | 0x0 | read_bus_error<br>Read bus error |
| 0 | WO | 0x0 | page_fault<br>Page fault |

**RKVDEC_MMU_INT_MASK**

Address: Operational Base + offset (0x001c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | Reserved |
| 1 | RW | 0x0 | read_bus_error<br>Read bus error<br>Enable an interrupt source if the corresponding mask bit is set to 1. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | page_fault<br>Page fault<br>Enable an interrupt source if the corresponding mask bit is set to 1. |

**RKVDEC_MMU_INT_STATUS**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | Reserved |
| 1 | RO | 0x0 | read_bus_error<br>Read bus error |
| 0 | RO | 0x0 | page_fault<br>Page fault |

**RKVDEC_MMU_AUTO_GATING**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | Reserved |
| 0 | RW | 0x1 | mmu_auto_gating<br>When it is 1'b1, the mmu will auto gating itself. |

## 5.5.17 VDPU381 LLP Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKVDEC_LINK_SWREG0_LINK_MODE_IRQ | 0x0000 | W | 0x00000000 | The interript of LLP mode |
| RKVDEC_LINK_SWREG1_CFG_START_ADDR | 0x0004 | W | 0x00000000 | the address of register data |
| RKVDEC_LINK_SWREG2_LINK_MODE | 0x0008 | W | 0x00000000 | The LLP table add ctrl |
| RKVDEC_LINK_SWREG3_CONFIG_DONE | 0x000c | W | 0x00000000 | Config finish ctrl register |
| RKVDEC_LINK_SWREG4_DECODERED_NUM | 0x0010 | W | 0x00000000 | The frame number which have been decodered |
| RKVDEC_LINK_SWREG5_DEC_TOTAL_NUM | 0x0014 | W | 0x00000000 | The total needed decoder number |
| RKVDEC_LINK_SWREG6_LINK_MODE_EN | 0x0018 | W | 0x00000000 | LLP enable flag |
| RKVDEC_LINK_SWREG7_NXT_DEC_LTB_BASE | 0x001c | W | 0x00000000 | Register0000 Description |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

## 5.5.18 VDPU381 LLP Detail Register Description

**RKVDEC_LINK_SWREG0_LINK_MODE_IRQ**

Address: Operational Base + offset (0x0000)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x0 | reserved |
| 20 | RW | 0x0 | sw_rcb_buffer_base_fixed<br>1'b0 : rcb buffer base can be config by ltb table.<br>1'b1 : rcb buffer will not be changed when ltb table be read,so it need to be config by normal reigster in first. |
| 19:18 | RO | 0x0 | reserved |
| 17 | RW | 0x0 | sw_ccu_core_work_mode<br>1'b0 : dec core will be used separate<br>1'b1 : dec core will ctrl by ccu |
| 16 | RW | 0x0 | sw_core_work_mode<br>1'b0 : ccu auto ctrl and decision mode<br>1'b1 : cpu ctrl ccu decision mode |
| 15:10 | RO | 0x0 | reserved |
| 9 | RW | 0x0 | rkvdec_irq_raw<br>The irq of decodered |
| 8 | RW | 0x0 | link_table_irq<br>when high,  decoder requests an interrrupt.<br>link table irq = sw_dec_irq_raw && (sw_dec_irq_dis == 1'b0) |
| 7:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | sw_error_irq_dis<br>0: if there are any error ,not matter sw_dec_irq_dis ,it will give an interrept .<br>1:if it will give interrept ,it only according to sw_dec_irq_dis |
| 1:0 | RO | 0x0 | reserved |

**RKVDEC_LINK_SWREG1_CFG_START_ADDR**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | reg_cfg_addr<br>it should be align to 32 byte |
| 3:0 | RO | 0x0 | reserved |

**RKVDEC_LINK_SWREG2_LINK_MODE**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | link_mode<br>0: normal mode,the first to start link mode<br>1:add extra ready frame to decoder |
| 30 | RO | 0x0 | reserved |
| 29:0 | RW | 0x00000000 | pre_frame_num<br>1:config 1 frame |

**RKVDEC_LINK_SWREG3_CONFIG_DONE**

Address: Operational Base + offset (0x000c)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x0 | reserved |
| 0 | W1C | 0x0 | config_done<br>after config okay,config this bit to 1 |

**RKVDEC_LINK_SWREG4_DECODERED_NUM**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | decoder_error_flag<br>0:no error<br>1:error,you will need to see swreg1 to check error type |
| 30 | RO | 0x0 | reserved |
| 29:0 | RO | 0x00000000 | decoder_num<br>The frame number which have been decodered |

**RKVDEC_LINK_SWREG5_DEC_TOTAL_NUM**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:0 | RO | 0x00000000 | dec_total_num<br>The total needed decoder number |

**RKVDEC_LINK_SWREG6_LINK_MODE_EN**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | link_mode_en<br>when error see by hw,it will auto reset to 0 |

**RKVDEC_LINK_SWREG7_NXT_DEC_LTB_BASE**

Address: Operational Base + offset (0x001c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | nxt_dec_ltb_base<br>bytes unit |

## 5.5.19 VDPU720 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKDJPEG_SWREG0_ID | 0x0000 | W | 0x00000000 | ID register (read only) |
| RKDJPEG_SWREG1_INT | 0x0004 | W | 0x00000000 | Interrupt and decoder enable register |
| RKDJPEG_SWREG2_SYS | 0x0008 | W | 0x00000000 | Rk jpeg decoder system ctrl |

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKDJPEG_SWREG3_PIC_SIZE | 0x000c | W | 0x00000000 | Picture width and height size |
| RKDJPEG_SWREG4_PIC_FORMAT | 0x0010 | W | 0x00000000 | Jpeg picture format configurate |
| RKDJPEG_SWREG5_HOR_VIRSTRIDE | 0x0014 | W | 0x00000000 | Sw_y_hor_virstride and sw_uv_hor_virstride configurate |
| RKDJPEG_SWREG6_Y_VIRSTRIDE | 0x0018 | W | 0x00000000 | Sw_y_virstride configurate |
| RKDJPEG_SWREG7_TABLE_LEN | 0x001c | W | 0x00000000 | Dequant table and huffman table length Description |
| RKDJPEG_SWREG8_STRM_LEN | 0x0020 | W | 0x00000000 | Rk jpeg stream length and start byte info Description |
| RKDJPEG_SWREG9_QTBL_BASE | 0x0024 | W | 0x00000000 | Dequant table DDR base address Description |
| RKDJPEG_SWREG10_HTBL_MINCODE_BASE | 0x0028 | W | 0x00000000 | huffman mincode table DDR base address Description |
| RKDJPEG_SWREG11_HTBL_VALUE_BASE | 0x002c | W | 0x00000000 | Huffman value table DDR base address Description |
| RKDJPEG_SWREG12_STRM_BASE | 0x0030 | W | 0x00000000 | Stream data DDR base address Description |
| RKDJPEG_SWREG13_DEC_OUT_BASE | 0x0034 | W | 0x00000000 | Rk jpeg recon decoder output data DDR address Description |
| RKDJPEG_SWREG14_STRM_ERROR | 0x0038 | W | 0x00000000 | Rk jpeg decoder stream error process |
| RKDJPEG_SWREG15_STRM_MASK | 0x003c | W | 0x00000000 | Rk jpeg decoder special marker process |
| RKDJPEG_SWREG16_CLK_GATE | 0x0040 | W | 0x00000000 | Rk jpeg decoder clk gate enable |
| RKDJPEG_SWREG30_PERF_LATENCY_CTRL0 | 0x0078 | W | 0x00000000 | Rk jpeg decoder axi performance ctrl0 Description |
| RKDJPEG_SWREG31_PERF_LATENCY_CTRL1 | 0x007c | W | 0x00000000 | Rk jpeg decoder axi performance ctrl1 Description |
| RKDJPEG_SWREG32_DBG_MCU_POS | 0x0080 | W | 0x00000000 | Rk jpeg debug register with mcu position Description |
| RKDJPEG_SWREG33_DBG_ERROR_INFO | 0x0084 | W | 0x00000000 | Rk jpeg debug register with error info Description |
| RKDJPEG_SWREG34_PERF_RD_MAX_LATENCY_NUM0 | 0x0088 | W | 0x00000000 | Rd_max_latency_num Description |
| RKDJPEG_SWREG35_PERF_RD_LATENCY_SAMP_NUM | 0x008c | W | 0x00000000 | Rd_latency_thr_num Description |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKDJPEG_SWREG36_PERF_RD_LATENCY_ACC_SUM | 0x0090 | W | 0x00000000 | Rd_latency_acc_sum Description |
| RKDJPEG_SWREG37_PERF_RD_AXI_TOTAL_BYTE | 0x0094 | W | 0x00000000 | Perf_rd_axi_total_byte Description |
| RKDJPEG_SWREG38_PERF_WR_AXI_TOTAL_BYTE | 0x0098 | W | 0x00000000 | Perf_wr_axi_total_byte Description |
| RKDJPEG_SWREG39_PERF_WORKING_CNT | 0x009c | W | 0x00000000 | Perf_working_cnt Description |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

## 5.5.20 VDPU720 Detail Registers Description

**RKDJPEG_SWREG0_ID**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | prod_num<br>RKDJPEG verision |
| 15:9 | RO | 0x0 | Reserved |
| 8 | RO | 0x0 | bit_depth<br>Max bit_depth support<br>1'b0: 8bits<br>1'b1: 12bits |
| 7:0 | RO | 0x00 | minor_ver<br>8'd0: Default<br>8'd1: 8k |

**RKDJPEG_SWREG1_INT**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0 | Reserved |
| 16 | RW | 0x0 | sw_care_strm_error_e<br>Use for sw_error_prc_mode=1<br>1'b0: Not care stream error,when sw_care_strm_error_e=0,<br>sw_dec_error_sta will not valid,<br>Mmu will not be reset at frame end,<br>Link table mode will continue without care stream error,<br>Only active error info registers;<br>1'b1: Care stream error; |
| 15 | RW | 0x0 | sw_buf_empty_force_end_flag<br>1'b0: Invalid<br>1'b1: Valid<br>Buffer empty interrupt with stream real empty<br>So should force hardware decoder current frame end |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14 | RW | 0x0 | sw_softreset_rdy<br>When it is 1'b1, it says that softreset has been done |
| 13 | RW | 0x0 | sw_dec_buf_empty_sta<br>Buffer empty status, only when sw_buf_empty_e is 1'b1 , this bit is valid<br>Software should clean stream buffer empty state and set sw_buf_empty_reload_p enbale at the same time |
| 12 | RW | 0x0 | sw_dec_timeout_sta<br>When high the decoder has been idling for too long. it will self reset the hardware<br>Only when sw_dec_timeout_e is 1'b1, this bit is valid |
| 11 | RW | 0x0 | sw_dec_error_sta<br>When high, an error is found in input data stream decoding.When sw_error_prc_mode is 1'b0, it will self reset the hardware, otherwise it will not |
| 10 | RW | 0x0 | sw_dec_bus_sta<br>When this bit is high, there is error on the axi bus, it will self reset hardware |
| 9 | RW | 0x0 | sw_dec_rdy_sta<br>When this bit is high, decoder has decoded a picture (the output module send out a frame rdy) |
| 8 | RW | 0x0 | sw_dec_irq<br>When high,  decoder requests an interrrupt.<br>sw_dec_irq = sw_dec_irq_raw && (sw_dec_irq_dis == 1'b0) |
| 7 | RW | 0x0 | sw_wait_reset_e<br>The enable flag of wait software system to reset flag<br>1'b0: Hardware will auto reset when error occur<br>1'b1: Wait software process reset when error occur |
| 6 | RW | 0x0 | sw_dec_irq_raw<br>The raw status of sw_dec_irq,SW should reset this bit after interrupt is handled |
| 5 | RW | 0x0 | sw_softrst_en_p<br>Softreset enable signal<br>Write 1 to soft reset, write 0 invalid<br>Pluse register |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | sw_buf_empty_reload_p<br>Buffer empty stream reload enable signal<br>Write 1 to reload stream data ready<br>Pulse register with hardware auto clean valid at next cycle<br>Before reload enable,strm_len register should be reset and start_of_type is zero<br>sw_strm_base addr may be reset also.<br>Note:sw_error_prc_mode should be set to 1 when sw_buf_empty_e valid<br>Otherwise the hardware would be reset and not support buffer buffer empty reload |
| 3 | RW | 0x0 | sw_buf_empty_e<br>Buffer empty interrupt enable |
| 2 | RW | 0x0 | sw_dec_timeout_e<br>If enabled HW may return timeout interrupt in case HW gets stucked while decoding picture. |
| 1 | RW | 0x0 | sw_dec_irq_dis<br>When hight, there are no interrupts concerning decoder from HW. Polling must be used to see the interrupt status |
| 0 | RW | 0x0 | sw_dec_e<br>Decoder enable. Setting this bit high will start the decoding operation. HW will reset this when the picture is decoded ready or bus error or time out interrupt is given for all decode format. |

**RKDJPEG_SWREG2_SYS**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | sw_yuv2rgb_range<br>Jpeg decoder yuv2rgb range<br>1'b0: Range0 limit (Y[16:235],UV[16:240],RGB[0:255])<br>1'b1: Range1 full (YUV[0:255],RGB[0:255]) |
| 30 | RW | 0x0 | sw_yuv2rgb_rec<br>Jpeg decoder yuv2rgb rec<br>1'b0: BT601<br>1'b1: BT709 |
| 29:27 | RW | 0x0 | sw_yuv_out_format<br>Jpeg decoder yuv output transmit format<br>3'b000: Yuv out without transmit format<br>3'b001: Yuv2rgb888<br>3'b010: Yuv2rgb565<br>3'b011: Yuv2yuv420sp(not support yuv400 transmit to yuv420sp)<br>3'b100: Yuv2yuyv(only support yuv422 or yuv444, yuv444 should uv scaledown) |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 26 | RW | 0x0 | sw_dec_out_sequence<br>Recon data out format when afbc off<br>1'b0: Raster sequence out<br>1'b1: Tile sequence out |
| 25 | RW | 0x0 | sw_fill_right_e<br>When JPEG picture width pixels is not a multiple of 16 pixels.<br>1'b0: Not fill picture width to multiple of 16 pixels.<br>1'b1: Fill picture width to multiple of 16 pixels. HW must fill one block of zero pixel data to the right border of the picture. |
| 24 | RW | 0x0 | sw_fill_down_e<br>When JPEG picture height pixels is not a multiple of 16 pixels.<br>1'b0: Not fill picture height to multiple of 16 pixels.<br>1'b1: Fill picture height to multiple of 16 pixels. HW must fill one block row of zero pixel data for the last block row of picture. |
| 23 | RW | 0x0 | sw_bgr_sequence<br>Jpeg decoder rgb sequence<br>1'b0: Rgb565/rgb888<br>1'b1: Bgr565/bgr888<br>Default is be mode |
| 22 | RW | 0x0 | sw_fbc_force_uncompress<br>1'b0：Allow fbce compress yuv block；<br>1'b1：Force all yuv block use uncompress mode； |
| 21 | RW | 0x0 | sw_allow_16x8_cp_flag<br>1'b0: Not allow<br>1'b1: Allow<br>The configurate value is depend on vop work mode |
| 20 | RW | 0x0 | sw_fbc_e<br>1'b0: Disable<br>1'b1: Fbc enable |
| 19:18 | RO | 0x0 | Reserved |
| 17 | RW | 0x0 | sw_force_softreset_valid<br>When sw_force_softreset_valid is 1'b1, sw_softrst_en will always be valid to the system no matter that whether the axi bus is idle;<br>When sw_force_softreset_valid is 1'b0, sw_softrst_en will only be valid when the axi bus is idle. |
| 16 | RW | 0x0 | sw_timeout_mode<br>Timeout mode select<br>1'b0: TIMEOUT_CYCLES is 24 1'b1;<br>1'b1: TIMEOUT_CYCLES is 18 1'b1; |
| 15:14 | RO | 0x0 | Reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:12 | RW | 0x0 | sw_scaledown_mode<br>Jpeg decoder scaledown mode<br>2'b00: Not scaledown<br>2'b01: 1/2 scaledown<br>2'b10: 1/4 scaledown<br>2'b11: 1/8 scaledown |
| 11 | RO | 0x0 | Reserved |
| 10 | RW | 0x0 | sw_out_byte_swap<br>May be used for 16 bits sequence output info<br>1'b0: No swapping of 8 bits data, 0x1234<br>1'b1: 8 bits data are swapped, 0x3412 |
| 9 | RW | 0x0 | sw_out_cbcr_swap<br>1'b0: Cb(u) is in the lower address, cr(v) is in the higher address<br>1'b1: Cb(u) is in the higher address,cr(v) is in the lower address<br>sw_in_cbcr_swap is the same with sw_out_cbcr_swap<br>Jpeg decoder only support for yuv4xxsp |
| 8 | RW | 0x0 | sw_out_swap64_e<br>May be used for 128 bit environment<br>1'b0: No swapping of 64 bit words<br>1'b1: 64 bit data words are swapped |
| 7 | RW | 0x0 | sw_out_swap32_e<br>May be used for 64 or 128 bit environment<br>1'b0: No swapping of 32 bit words<br>1'b1: 32 bit data words are swapped |
| 6 | RW | 0x0 | sw_out_endian<br>1'b0: Little endian<br>1'b1: Big endian<br>For litter enadian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address |
| 5 | RW | 0x0 | sw_str_swap64_e<br>May be used for 128 bit environment<br>1'b0: No swapping of 64 bit words<br>1'b1: 64 bit data words are swapped |
| 4 | RW | 0x0 | sw_str_swap32_e<br>May be used for 64 or 128 bit environment<br>1'b0: No swapping of 32 bit words<br>1'b1: 32 bit data words are swapped |
| 3 | RW | 0x0 | sw_str_endian<br>1'b0: Little endian<br>1'b1: Big endian<br>For little endian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | sw_in_swap64_e<br>May be used for 128 bit environment<br>1'b0: Noswapping of 64 bit words<br>1'b1: 64 bit data words are swapped |
| 1 | RW | 0x0 | sw_in_swap32_e<br>My be used for 64 or 128 bit environment<br>1'b0: Noswapping of 32 bit words<br>1'b1: 32 bit data words are swapped |
| 0 | RW | 0x0 | sw_in_endian<br>1'b0: Little endian<br>1'b1: Big endian<br>For litter enadian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address |

**RKDJPEG_SWREG3_PIC_SIZE**

Address: Operational Base + offset (0x000c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | sw_pic_height_m1<br>Picture height in pixels unit minus1(should be mcu align by hardware) |
| 15:0 | RW | 0x0000 | sw_pic_width_m1<br>Picture width in pixels unit minus1(should be mcu align by hardware) |

**RKDJPEG_SWREG4_PIC_FORMAT**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | sw_dri_mcu_num_m1<br>Restart marker frequency. Tells the amount of coding units between restart markers Specifies the number of MCU in the restart.<br>The number is minus1 |
| 15 | RW | 0x0 | sw_dri_e<br>Define restart interval marker enable<br>1'b0: Restart interval marker disable<br>1'b1: Restart interval marker enable |
| 14 | RO | 0x0 | Reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:12 | RW | 0x0 | sw_htables_sel<br>Amount of Huffman tables in external memory:<br>2'd0: No Huffman tables.<br>2'd1: One Huffman table. Used when picture is single type<br>2'd2: Two Huffman tables. One for luminance and one for chominances<br>2'd3: Three Huffman tables. Each type (Lu, Cb, Cr) has own Huffman table |
| 11:10 | RO | 0x0 | Reserved |
| 9:8 | RW | 0x0 | sw_qtables_sel<br>Amount of Quantization tables in external memory:<br>2'd0: No quantization tables.<br>2'd1: One quantization table. Used when picture is single type<br>2'd2: Two quantization tables. One for luminance and one for chominances<br>2'd3: Three quantization tables. Each type (Lu, Cr, Cb) has own QP-table |
| 7 | RO | 0x0 | Reserved |
| 6:4 | RW | 0x0 | sw_pixel_depth<br>Picture luma pixel depth minus8.<br>3'd0: 8bits<br>3'd4: 12bits |
| 3 | RO | 0x0 | Reserved |
| 2:0 | RW | 0x0 | sw_jpeg_mode<br>Input picture sampling format:<br>3'd0: single type, MB 1 block (4:0:0)<br>3'd1: single type, MB 6 blocks (4:1:1)<br>3'd2: three types, MB 6 blocks (4:2:0)<br>3'd3: three types, MB 4 blocks (4:2:2)<br>3'd4: three types, MB 4 blocks (4:4:0)<br>3'd5: three types, MB 3 blocks (4:4:4) |

**RKDJPEG_SWREG5_HOR_VIRSTRIDE**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | sw_uv_hor_virstride<br>Picture horizontal virtual stride (the unit is 128bit)<br>The max is 65536x2/16 = 0x2000<br>Suggest this register to configuration to even for advance DDR performance<br>yuv444 tile mode ,uv_hor_virstride will use 16bits |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0000 | sw_y_hor_virstride<br>Picture horizontal virtual stride (the unit is 128bit)<br>The max is 65536x2/16 = 0x2000<br>Suggest this register to configuration to even for advance DDR performance<br>Fbc mode: used for head virtual stride<br>But rgb888 tile mode ,y_hor_virstride 16bits is not enought,will be use 17bits |

**RKDJPEG_SWREG6_Y_VIRSTRIDE**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_y_virstride<br>Base address with 16 byte precision for decoder output luminance picture virtual stride |
| 3:0 | RO | 0x0 | Reserved |

**RKDJPEG_SWREG7_TABLE_LEN**

Address: Operational Base + offset (0x001c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x0 | Reserved |
| 24 | RW | 0x0 | sw_y_hor_virstride_h<br>Picture horizontal virtual stride (the unit is 128bit)<br>High bit when rgb888 tile mode use ,y_hor_virstride 16bits is not enought,will be use 17bits |
| 23:22 | RO | 0x0 | Reserved |
| 21:16 | RW | 0x00 | sw_htbl_value_len<br>Huffman value tables length(minus 1) with 16 byte align(128bits) |
| 15:13 | RO | 0x0 | Reserved |
| 12:8 | RW | 0x00 | sw_htbl_mincode_len<br>Huffman maxcode mincode and accaddr length(minus 1) with 16 byte align(128bits) |
| 7:5 | RO | 0x0 | Reserved |
| 4:0 | RW | 0x00 | sw_qtbl_len<br>Quant table length(minus 1) with 16 byte align(128bits) |

**RKDJPEG_SWREG8_STRM_LEN**

Address: Operational Base + offset (0x0020)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_stream_len<br>Amount of stream data 16 bytes(minus 1) in input buffer. If the given buffer size is not enough for finishing the picture the corresponding interrupt is given and new stream buffer base address and stream buffer size information should be given (assosiates with sw_strm_in_base). |
| 3:0 | RW | 0x0 | sw_strm_start_byte<br>Input stream start byte offset:<br>4'd0: 0 type, of the base addr(16bytes) offset<br>4'd1: 1 type, of the base addr(16bytes) offset<br>4'd2: 2 type, of the base addr(16bytes) offset<br>4'd3: 3 type, of the base addr(16bytes) offset<br>4'd4: 4 type, of the base addr(16bytes) offset<br>4'd5: 5 type, of the base addr(16bytes) offset<br>4'd6: 6 type, of the base addr(16bytes) offset<br>4'd7: 7 type, of the base addr(16bytes) offset<br>… |

**RKDJPEG_SWREG9_QTBL_BASE**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RW | 0x0000000 | sw_qtbl_base<br>Base address for standard dependent tables:<br>AC,DC, QP tables 64 bytes align） |
| 5:0 | RO | 0x0 | Reserved |

**RKDJPEG_SWREG10_HTBL_MINCODE_BASE**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RW | 0x0000000 | sw_htbl_mincode_base<br>Base address for standard dependent tables:<br>Huffman mincode and accaddr tables 64 bytes align） |
| 5:0 | RO | 0x0 | Reserved |

**RKDJPEG_SWREG11_HTBL_VALUE_BASE**

Address: Operational Base + offset (0x002c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RW | 0x0000000 | sw_htbl_value_base<br>Base address for standard dependent tables:<br>Huffman value tables 64 bytes align） |
| 5:0 | RO | 0x0 | Reserved |

**RKDJPEG_SWREG12_STRM_BASE**

Address: Operational Base + offset (0x0030)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | sw_strm_in_base<br>Stream start address with 16 byte precision.<br>Actually, start byte number in stream_start_byte. |
| 3:0 | RO | 0x0 | Reserved |

**RKDJPEG_SWREG13_DEC_OUT_BASE**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RW | 0x0000000 | sw_dec_out_base<br>Base address with 64 byte precision for decoder output luminance picture |
| 5:0 | RO | 0x0 | Reserved |

**RKDJPEG_SWREG14_STRM_ERROR**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x0 | Reserved |
| 20:16 | RW | 0x00 | sw_hfm_force_stop<br>1'b0: Huffman decoder error and continue.<br>1'b1: Huffman decoder error force stop the decoder and wait soft reset.<br>[12]: AXI stream buffer empty, and without detect EOI marker stop or not(0:support fill coefficient)<br>[11]:Huffman get EOI marker without frame end stop or not(0:support fill coefficient)<br>[10]:Huffman coefficient overflow detect and stop or not(0:support decode next coefficient)<br>[9]:Huffman decode DRI stream stop or not, when MCU counter is not zero with DRI marker detect(0:support fill coefficient)<br>[8]:Huffman decode DRI stream stop or not, when MCU counter is zero without DRI marker detect(0:support skip dummy stream) |
| 15:10 | RO | 0x0 | Reserved |
| 9 | RW | 0x0 | sw_strm_dri_seq_err_mode<br>1'b0: Stream dri sequence error do not report error pos;<br>1'b1: Stream dri sequence error should be report error pos(if it's first error);<br>Note: error state should be report at all case |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8:7 | RW | 0x0 | sw_strm_other_mark_mode<br>2'b00: Stream detect other marker do skip process and not report error pos;<br>2'b01: Stream detect another marker stop the decoder and wait soft reset;<br>2'b10: Stream detect other marker do skip process<br>2'b11: Stream detect other marker do with normal stream<br>Note: error state should be report at all case |
| 6:5 | RW | 0x0 | sw_strm_ffff_err_mode<br>2'b00: Stream detect ffff marker do skip first 0xff process and not report error position;<br>2'b01: Stream detect another marker stop the decoder and wait soft reset;<br>2'b10: Stream detect ffff marker do skip first 0xff process;<br>2'b11: Stream detect ffff marker do with normal stream at first 0xff;<br>Note: error state should be report at all case |
| 4:3 | RW | 0x0 | sw_strm_r1_err_mode<br>Stream detect second select marker process mode configuration<br>2'b00: Ignore second select marker.<br>2'b01: Force stop decoder when meet the second select marker<br>2'b10: Do skip process when meet the second select marker<br>2'b11: Do with normal stream when meet the second select marker |
| 2:1 | RW | 0x0 | sw_strm_r0_err_mode<br>Stream detect first select marker process mode configuration<br>2'b00: Ignore first select marker.<br>2'b01: Force stop decoder when meet the first select marker<br>2'b10: Do skip process when meet the first select marker<br>2'b11: Do with normal stream when meet the first select marker |
| 0 | RW | 0x0 | sw_error_prc_mode<br>1'b0: When there is any stream error, the hardware will stop the decoder and reset itself;<br>1'b1: When there is any stream error, the hardware will wait the end signal of recon and then reset request; |

**RKDJPEG_SWREG15_STRM_MASK**

Address: Operational Base + offset (0x003c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | sw_strm_r1_mask<br>zmark the mask info<br>1'b1: Stream value[7-0] will mask and not care<br>1'b0: Stream value[7-0] shall match SW marker value |
| 23:16 | RW | 0x00 | sw_strm_r1_marker<br>0xffxx marker low 8bits value |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:8 | RW | 0x00 | sw_strm_r0_mask<br>Mark the mask info<br>1'b1: Stream value[7-0] will mask and not care<br>1'b0: Stream value[7-0] shall match SW marker value |
| 7:0 | RW | 0x00 | sw_strm_r0_marker<br>0xffxx marker low 8bits value |

**RKDJPEG_SWREG16_CLK_GATE**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0 | Reserved |
| 7:0 | RW | 0x0 | sw_dec_gate_e<br>Total 8 bits each with follow phase<br>1'b0: Clock gate is not enable<br>1'b1: Clock gate is enable when busifd block is not working |

**RKDJPEG_SWREG30_PERF_LATENCY_CTRL0**

Address: Operational Base + offset (0x0078)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x0 | Reserved |
| 19:8 | RW | 0x000 | sw_rd_latency_thr<br>Rd channel latency threshold |
| 7:4 | RW | 0x0 | sw_rd_latency_id<br>Rd channel id for performance test |
| 3 | RW | 0x0 | sw_axi_cnt_type<br>sw_axi_cnt_type<br>1'b0: AXI transfer num count<br>1'b1: DDR align transfer num count |
| 2 | RW | 0x0 | sw_axi_perf_frm_type<br>1'b0: Clear by frame end<br>1'b1: Clear by software configuration |
| 1 | RW | 0x0 | sw_axi_perf_clr_e<br>1'b0: Software clear disable<br>1'b1: Software clear enalbe<br>Clear pulse |
| 0 | RW | 0x0 | sw_axi_perf_work_e<br>1'b0: Disable<br>1'b1: Enable |

**RKDJPEG_SWREG31_PERF_LATENCY_CTRL1**

Address: Operational Base + offset (0x007c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x0 | Reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | sw_rd_total_bytes_mode<br>1'b0: Cal all id<br>1'b1: Cal sw_ar_count_id |
| 11:8 | RW | 0x0 | sw_aw_count_id<br>sw_aw_count_id |
| 7:4 | RW | 0x0 | sw_ar_count_id<br>sw_ar_count_id |
| 3 | RW | 0x0 | sw_aw_cnt_id_type<br>sw_aw_cnt_id_type<br>1'b0: Count all wr-channels<br>1'b1: Count sw_wr_cont_id wr-channel only |
| 2 | RW | 0x0 | sw_ar_cnt_id_type<br>sw_ar_cnt_id_type<br>1'b0: Count all rd-channels<br>1'b1: Count sw_ar_cont_id rd-channel only |
| 1:0 | RW | 0x0 | sw_addr_align_type<br>sw_addr_align_type<br>2'd0: 16 byte align<br>2'd1: 32byte align<br>2'd2: 64byte align<br>2'd3: 128byte align |

**RKDJPEG_SWREG32_DBG_MCU_POS**

Address: Operational Base + offset (0x0080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | mcu_pos_y<br>Decoder mcu position at x coordinal with first error detect, only for read enable |
| 15:0 | RO | 0x0000 | mcu_pos_x<br>Decoder mcu position at y coordinal with first error detect, only for read enable |

**RKDJPEG_SWREG33_DBG_ERROR_INFO**

Address: Operational Base + offset (0x0084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x0 | Reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19:16 | RW | 0x0 | jpeg_first_error_idx<br>Jpeg decoder first error index<br>4'd0: stream_dri_seq_err_sta<br>4'd1: stream_r0_err_sta<br>4'd2: stream_r1_err_sta<br>4'd3: stream_ffff_err_sta<br>4'd4: stream_other_mark_err_sta<br>4'd8: huffman_mcu_cnt_l<br>4'd9: huffman_mcu_cnt_m<br>4'd10: huffman_eoi_without_end<br>4'd11: huffman_end_without_eoi<br>4'd12: huffman_overflow<br>4'd13: huffman_buf_empty |
| 15:14 | RO | 0x0 | Reserved |
| 13 | RW | 0x0 | huffman_buf_empty<br>Decoder picture not complete, and not detect EOI with buffer empty<br>1'b0: Buffer not empty<br>1'b1: Buffer empty |
| 12 | RW | 0x0 | huffman_overflow<br>Decoder Huffman coefficient overflow |
| 11 | RW | 0x0 | huffman_end_without_eoi<br>Decoder Huffman frame end without get EOI marker |
| 10 | RW | 0x0 | huffman_eoi_without_end<br>Decoder Huffman get EOI marker without frame end |
| 9 | RW | 0x0 | huffman_mcu_cnt_m<br>Decoder dri stream mcu count more, mcu count 0 without restart mark |
| 8 | RW | 0x0 | huffman_mcu_cnt_l<br>Decoder dri stream mcu count low, restart mark is coming without mcu count 0 |
| 7:5 | RO | 0x0 | Reserved |
| 4 | RW | 0x0 | stream_other_mark_err_sta<br>Decoder stream other marker error detect flag, only for read enable<br>1'b0: Other marker not detect<br>1'b1: Other marker detect |
| 3 | RW | 0x0 | stream_ffff_err_sta<br>Decoder stream ffff error detect flag, only for read enable<br>1'b0: Other marker not detect<br>1'b1: Other marker detect |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | stream_r1_err_sta<br>Decoder stream special marker1 error detect flag, only for read enable<br>1'b0: Special marker1 not detect<br>1'b1: Special marker1 detect |
| 1 | RW | 0x0 | stream_r0_err_sta<br>Decoder stream special marker0 error detect flag, only for read enable<br>1'b0: Special marker0 not detect<br>1'b1: Special marker0 detect |
| 0 | RW | 0x0 | stream_dri_seq_err_sta<br>1'b0: Stream DRI at normal sequence<br>1'b1: Stream error with DRI not at normal sequence |

**RKDJPEG_SWREG34_PERF_RD_MAX_LATENCY_NUM0**

Address: Operational Base + offset (0x0088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | Reserved |
| 15:0 | RW | 0x0000 | rd_max_latency_num_ch0<br>rd_max_latency_num_ch0 |

**RKDJPEG_SWREG35_PERF_RD_LATENCY_SAMP_NUM**

Address: Operational Base + offset (0x008c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | rd_latency_thr_num_ch0<br>rd_latency_thr_num_ch0 |

**RKDJPEG_SWREG36_PERF_RD_LATENCY_ACC_SUM**

Address: Operational Base + offset (0x0090)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | rd_latency_acc_sum<br>rd_latency_acc_sum |

**RKDJPEG_SWREG37_PERF_RD_AXI_TOTAL_BYTE**

Address: Operational Base + offset (0x0094)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | perf_rd_axi_total_byte<br>perf_rd_axi_total_byte |

**RKDJPEG_SWREG38_PERF_WR_AXI_TOTAL_BYTE**

Address: Operational Base + offset (0x0098)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | perf_wr_axi_total_byte<br>perf_wr_axi_total_byte |

**RKDJPEG_SWREG39_PERF_WORKING_CNT**

Address: Operational Base + offset (0x009c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | perf_working_cnt<br>perf_working_cnt |

## 5.5.21 VDPU720 MMU Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKVDEC_MMU_DTE_ADDR | 0x0000 | W | 0x00000000 | MMU current page Table address. It is only can be written when MMU state is disable or page fault or mmu enable stall state |
| RKVDEC_MMU_STATUS | 0x0004 | W | 0x00000018 | MMU status register |
| RKVDEC_MMU_COMMAND | 0x0008 | W | 0x00000000 | MMU command register |
| RKVDEC_MMU_PAGE_FAULT_ADDR | 0x000c | W | 0x00000000 | MMU logical address of last page fault |
| RKVDEC_MMU_ZAP_ONE_LINE | 0x0010 | W | 0x00000000 | MMU Zap cache line register |
| RKVDEC_MMU_INT_RAWSTAT | 0x0014 | W | 0x00000000 | MMU raw interrupt status register |
| RKVDEC_MMU_INT_CLEAR | 0x0018 | W | 0x00000000 | MMU raw interrupt status register |
| RKVDEC_MMU_INT_MASK | 0x001c | W | 0x00000000 | MMU raw interrupt status register |
| RKVDEC_MMU_INT_STATUS | 0x0020 | W | 0x00000000 | MMU raw interrupt status register |
| RKVDEC_MMU_AUTO_GATING | 0x0024 | W | 0x00000001 | MMU auto gating |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

## 5.5.22 VDPU720 MMU Detail Registers Description

**RKVDEC_MMU_DTE_ADDR**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | mmu_dte_addr<br>Mmu dte base addr , the address must be 4kb aligned |

**RKVDEC_MMU_STATUS**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:11 | RO | 0x000000 | Reserved |
| 10:6 | RO | 0x00 | page_fault_bus_id<br>Index of master responsible for last page fault. |
| 5 | RO | 0x0 | page_fault_is_write<br>The direction of access for last page fault:<br>1'b0: Read<br>1'b1: Write |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RO | 0x1 | replay_buffer_empty<br>The MMU replay buffer is empty. |
| 3 | RO | 0x1 | mmu_idle<br>The MMU is idle when accesses are being translated and there are no unfinished translated accesses. |
| 2 | RO | 0x0 | stail_active<br>MMU stall mode currently enabled. The mode is enabled by command. |
| 1 | RO | 0x0 | page_fault_active<br>MMU page fault mode currently enabled. The mode is enabled by command. |
| 0 | RO | 0x0 | paging_enabled<br>Paging is enabled. |

**RKVDEC_MMU_COMMAND**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | Reserved |
| 2:0 | WO | 0x0 | mmu_cmd<br>MMU_CMD. This can be:<br>3'd0: MMU_ENABLE_PAGING<br>3'd1: MMU_DISABLE_PAGING<br>3'd2: MMU_ENABLE_STALL<br>3'd3: MMU_DISABLE_STALL<br>3'd4: MMU_ZAP_CACHE<br>3'd5: MMU_PAGE_FAULT_DONE<br>3'd6: MMU_FORCE_RESET<br>3'd7: Reserved |

**RKVDEC_MMU_PAGE_FAULT_ADDR**

Address: Operational Base + offset (0x000c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | page_fault_addr<br>Address of last page fault |

**RKVDEC_MMU_ZAP_ONE_LINE**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | WO | 0x00000000 | mmu_zap_one_line<br>Address to be invalidated from the page table cache |

**RKVDEC_MMU_INT_RAWSTAT**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | Reserved |
| 1 | RW | 0x0 | read_bus_error<br>Read bus error |
| 0 | RW | 0x0 | page_fault<br>Page fault |

**RKVDEC_MMU_INT_CLEAR**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | Reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | WO | 0x0 | read_bus_error<br>Read bus error |
| 0 | WO | 0x0 | page_fault<br>Page fault |

**RKVDEC_MMU_INT_MASK**

Address: Operational Base + offset (0x001c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | Reserved |
| 1 | RW | 0x0 | read_bus_error<br>Read bus error<br>Enable an interrupt source if the corresponding mask bit is set to 1. |
| 0 | RW | 0x0 | page_fault<br>Page fault<br>Enable an interrupt source if the corresponding mask bit is set to 1. |

**RKVDEC_MMU_INT_STATUS**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | Reserved |
| 1 | RO | 0x0 | read_bus_error<br>Read bus error |
| 0 | RO | 0x0 | page_fault<br>Page fault |

**RKVDEC_MMU_AUTO_GATING**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | Reserved |
| 0 | RW | 0x1 | mmu_auto_gating<br>When it is 1'b1, the mmu will auto gating itself. |

## 5.5.23 VDPU720 LLP Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKDJPEG_LINK_SWREG0_LINK_MODE_IRQ | 0x0000 | W | 0x00000000 | Register0000 Description |
| RKDJPEG_LINK_SWREG1_CFG_START_ADDR | 0x0004 | W | 0x00000000 | the address of register data |
| RKDJPEG_LINK_SWREG2_LINK_MODE | 0x0008 | W | 0x00000000 | Register0000 Description |
| RKDJPEG_LINK_SWREG3_CONFIG_DONE | 0x000c | W | 0x00000000 | Register0000 Description |
| RKDJPEG_LINK_SWREG4_DECODERED_NUM | 0x0010 | W | 0x00000000 | Register0000 Description |
| RKDJPEG_LINK_SWREG5_DEC_TOTAL_NUM | 0x0014 | W | 0x00000000 | Register0000 Description |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKDJPEG_LINK_SWREG6_LINK_MODE_EN | 0x0018 | W | 0x00000000 | Register0000 Description |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

## 5.5.24 VDPU720 LLP Registers Description

**RKDJPEG_LINK_SWREG0_LINK_MODE_IRQ**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:11 | RO | 0x0 | reserved |
| 10 | RW | 0x0 | sw_link_softreset_rdy<br>when it is 1'b1, it says that softreset has been done |
| 9 | RW | 0x0 | rkvdec_irq_raw<br>Rkvdec raw irq |
| 8 | RW | 0x0 | link_table_irq<br>when high, decoder requests an interrrupt.<br>link table irq = sw_dec_irq_raw && (sw_dec_irq_dis == 1'b0) |
| 7:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | sw_error_irq_dis<br>1'b0: if there are any error ,not matter sw_dec_irq_dis ,it will give an interrept .<br>1'b1: if it will give interrept ,it only according to sw_dec_irq_dis |
| 1 | RW | 0x0 | cache_cfg_mode_sel<br>1'b0: use rtl default value to config cache, ip will auto clr cache when it begin to start dec a frame.<br>1'b1: use config in ddr to config cache. |
| 0 | RO | 0x0 | reserved |

**RKDJPEG_LINK_SWREG1_CFG_START_ADDR**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | reg_cfg_addr<br>it should be align to 32 byte |
| 3:0 | RO | 0x0 | reserved |

**RKDJPEG_LINK_SWREG2_LINK_MODE**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | link_mode<br>1'b0: normal mode,the first to start link mode<br>1'b1: add extra ready frame to decoder |
| 30 | RO | 0x0 | reserved |
| 29:0 | RW | 0x00000000 | pre_frame_num<br>1'b1: config 1 frame |

Rockchip Confidencial

**RKDJPEG_LINK_SWREG3_CONFIG_DONE**

Address: Operational Base + offset (0x000c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x0 | reserved |
| 0 | W1C | 0x0 | config_done<br>after config okay,config this bit to 1 |

**RKDJPEG_LINK_SWREG4_DECODERED_NUM**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | decoder_error_flag<br>1'b0: no error<br>1'b1: error,you will need to see swreg1 to check error type |
| 30 | RO | 0x0 | reserved |
| 29:0 | RO | 0x00000000 | decoder_num<br>Decoder number |

**RKDJPEG_LINK_SWREG5_DEC_TOTAL_NUM**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:0 | RO | 0x00000000 | dec_total_num<br>Decoder total number |

**RKDJPEG_LINK_SWREG6_LINK_MODE_EN**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | sw_link_softrst_en_p<br>link mode software force hardware self reset enable signal<br>write 1 to soft reset, write 0 invalid<br>puls register |
| 3:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | link_mode_en<br>when error see by hw,it will auto reset to 0 |

## 5.5.25 VEPU121 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VEPU_SWREG_0 | 0x0000 | W | 0x00000000 | 1st quantization for jpeg lumin table |
| VEPU_SWREG_1 | 0x0004 | W | 0x00000000 | 2st quantization for jpeg lumin table |
| VEPU_SWREG_2 | 0x0008 | W | 0x00000000 | 3st quantization for jpeg lumin table |

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VEPU_SWREG_3 | 0x000c | W | 0x00000000 | 4st quantization for jpeg lumin table |
| VEPU_SWREG_4 | 0x0010 | W | 0x00000000 | 5st quantization for jpeg lumin table |
| VEPU_SWREG_5 | 0x0014 | W | 0x00000000 | 6st quantization for jpeg lumin table/part 1 for qp round |
| VEPU_SWREG_6 | 0x0018 | W | 0x00000000 | 7st quantization for jpeg lumin table |
| VEPU_SWREG_7 | 0x001c | W | 0x00000000 | 8st quantization for jpeg lumin table |
| VEPU_SWREG_8 | 0x0020 | W | 0x00000000 | 9st quantization for jpeg lumin table |
| VEPU_SWREG_9 | 0x0024 | W | 0x00000000 | 10st quantization for jpeg lumin table |
| VEPU_SWREG_10 | 0x0028 | W | 0x00000000 | 11st quantization for jpeg lumin table |
| VEPU_SWREG_11 | 0x002c | W | 0x00000000 | 12st quantization for jpeg lumin table |
| VEPU_SWREG_12 | 0x0030 | W | 0x00000000 | 13st quantization for jpeg lumin table |
| VEPU_SWREG_13 | 0x0034 | W | 0x00000000 | 14st quantization for jpeg lumin table |
| VEPU_SWREG_14 | 0x0038 | W | 0x00000000 | 15st quantization for jpeg lumin table |
| VEPU_SWREG_15 | 0x003c | W | 0x00000000 | 16st quantization for jpeg lumin table |
| VEPU_SWREG_16 | 0x0040 | W | 0x00000000 | 1st quantization for jpeg chroma table |
| VEPU_SWREG_17 | 0x0044 | W | 0x00000000 | 2st quantization for jpeg chroma table |
| VEPU_SWREG_18 | 0x0048 | W | 0x00000000 | 3st quantization for jpeg chroma table |
| VEPU_SWREG_19 | 0x004c | W | 0x00000000 | 4st quantization for jpeg chroma table |
| VEPU_SWREG_20 | 0x0050 | W | 0x00000000 | 5st quantization for jpeg chroma table |
| VEPU_SWREG_21 | 0x0054 | W | 0x00000000 | 6st quantization for jpeg chroma table |
| VEPU_SWREG_22 | 0x0058 | W | 0x00000000 | 7st quantization for jpeg chroma table |
| VEPU_SWREG_23 | 0x005c | W | 0x00000000 | 8st quantization for jpeg chroma table/part 3 for qp round |
| VEPU_SWREG_24 | 0x0060 | W | 0x00000000 | 9st quantization for jpeg chroma table |
| VEPU_SWREG_25 | 0x0064 | W | 0x00000000 | 10st quantization for jpeg chroma table |
| VEPU_SWREG_26 | 0x0068 | W | 0x00000000 | 11st quantization for jpeg chroma table |
| VEPU_SWREG_27 | 0x006c | W | 0x00000000 | 12st quantization for jpeg chroma |
| VEPU_SWREG_28 | 0x0070 | W | 0x00000000 | 13st quantization for jpeg chroma |
| VEPU_SWREG_29 | 0x0074 | W | 0x00000000 | 14st quantization for jpeg chroma |
| VEPU_SWREG_30 | 0x0078 | W | 0x00000000 | 15st quantization for jpeg chroma |
| VEPU_SWREG_31 | 0x007c | W | 0x00000000 | 16st quantization for jpeg chroma |
| VEPU_SWREG_44 | 0x00b0 | W | 0x00000000 | Intra slice bitmap |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VEPU_SWREG_45 | 0x00b4 | W | 0x00000000 | Intra slice bitmap1 |
| VEPU_SWREG_46 | 0x00b8 | W | 0x00000000 | Intra macro block select register |
| VEPU_SWREG_47 | 0x00bc | W | 0x00000000 | CIR intra control register |
| VEPU_SWREG_48 | 0x00c0 | W | 0x00000000 | Base addr for input luma |
| VEPU_SWREG_49 | 0x00c4 | W | 0x00000000 | Base address for input cb |
| VEPU_SWREG_50 | 0x00c8 | W | 0x00000000 | Input cr start address |
| VEPU_SWREG_51 | 0x00cc | W | 0x00000000 | Stream header bits left register |
| VEPU_SWREG_52 | 0x00d0 | W | 0x00000000 | Stream header bits left register |
| VEPU_SWREG_53 | 0x00d4 | W | 0x00000000 | Stream buffer register |
| VEPU_SWREG_54 | 0x00d8 | W | 0x01010000 | Axi control register |
| VEPU_SWREG_55 | 0x00dc | W | 0x00000000 | Qp related |
| VEPU_SWREG_56 | 0x00e0 | W | 0x00000000 | The luma reference frame start address |
| VEPU_SWREG_57 | 0x00e4 | W | 0x00000000 | The chroma reference frame start address |
| VEPU_SWREG_58 | 0x00e8 | W | 0x00000000 | The result of qp sum div2 |
| VEPU_SWREG_59 | 0x00ec | W | 0x00000000 | H264 slice ctrl |
| VEPU_SWREG_60 | 0x00f0 | W | 0x00000000 | Spill ctrl |
| VEPU_SWREG_61 | 0x00f4 | W | 0x00000000 | Input luminance information |
| VEPU_SWREG_62 | 0x00f8 | W | 0x00000000 | Rlc_sum |
| VEPU_SWREG_63 | 0x00fc | W | 0x00000000 | The reconstructed luma start address |
| VEPU_SWREG_64 | 0x0100 | W | 0x00000000 | The reconstructed chroma start address |
| VEPU_SWREG_65_REUSE | 0x0104 | W | 0x00000000 | Checkpoint 1 and 2 |
| VEPU_SWREG_66_REUSE | 0x0108 | W | 0x00000000 | Checkpoint 3 and 4 |
| VEPU_SWREG_67_REUSE | 0x010c | W | 0x00000000 | Checkpoint 5 and 6 |
| VEPU_SWREG_68_REUSE | 0x0110 | W | 0x00000000 | Checkpoint 7 and 8 |
| VEPU_SWREG_69_REUSE | 0x0114 | W | 0x00000000 | Checkpoint 9 and 10 |
| VEPU_SWREG_70_REUSE | 0x0118 | W | 0x00000000 | Checkpoint word error 1 and 2 |
| VEPU_SWREG_71_REUSE | 0x011c | W | 0x00000000 | Checkpoint word error 1 and 2 |
| VEPU_SWREG_72_REUSE | 0x0120 | W | 0x00000000 | Checkpoint word error 1 and 2 |
| VEPU_SWREG_73_REUSE | 0x0124 | W | 0x00000000 | Checkpoint delta QP register |
| VEPU_SWREG_74 | 0x0128 | W | 0x00000000 | Input image format |
| VEPU_SWREG_75 | 0x012c | W | 0x00000000 | Intra/inter mode |
| VEPU_SWREG_76_REUSE | 0x0130 | W | 0x00000000 | Encoder control register 0 |
| VEPU_SWREG_77 | 0x0134 | W | 0x00000000 | Output stream start address |
| VEPU_SWREG_78 | 0x0138 | W | 0x00000000 | Output control start address |
| VEPU_SWREG_79 | 0x013c | W | 0x00000000 | Next picture luminance start address |
| VEPU_SWREG_80 | 0x0140 | W | 0x00000000 | Base address for MV output |
| VEPU_SWREG_81 | 0x0144 | W | 0x00000000 | The cabac table start address |
| VEPU_SWREG_82 | 0x0148 | W | 0x00000000 | ROI area register |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VEPU_SWREG_83 | 0x014c | W | 0x00000000 | The second of ROI area register |
| VEPU_SWREG_84 | 0x0150 | W | 0x00000000 | Stabilization matrix1 |
| VEPU_SWREG_85 | 0x0154 | W | 0x00000000 | Stabilization matrix2 |
| VEPU_SWREG_86 | 0x0158 | W | 0x00000000 | Stabilization matrix3 |
| VEPU_SWREG_87 | 0x015c | W | 0x00000000 | Stabilization matrix4 |
| VEPU_SWREG_88 | 0x0160 | W | 0x00000000 | Stabilization matrix5 |
| VEPU_SWREG_89 | 0x0164 | W | 0x00000000 | Stabilization matrix6 |
| VEPU_SWREG_90 | 0x0168 | W | 0x00000000 | Stabilization matrix7 |
| VEPU_SWREG_91 | 0x016c | W | 0x00000000 | Stabilization matrix8 |
| VEPU_SWREG_92 | 0x0170 | W | 0x00000000 | Stabilization matrix9 |
| VEPU_SWREG_93 | 0x0174 | W | 0x00000000 | The output of Stabilization motion sum |
| VEPU_SWREG_94 | 0x0178 | W | 0x00000000 | Output of Stabilization |
| VEPU_SWREG_95 | 0x017c | W | 0x00000000 | RGB to YUV conversion coefficient register |
| VEPU_SWREG_96 | 0x0180 | W | 0x00000000 | RGB to YUV conversion coefficient register |
| VEPU_SWREG_97 | 0x0184 | W | 0x00000000 | RGB to YUV conversion coefficient register |
| VEPU_SWREG_98 | 0x0188 | W | 0x00000000 | RGA MASK |
| VEPU_SWREG_99 | 0x018c | W | 0x00000000 | Mv related |
| VEPU_SWREG_100_REUSE | 0x0190 | W | 0x00000000 | QP register |
| VEPU_SWREG_101_READ | 0x0194 | W | 0x1f522780 | Hw config reg |
| VEPU_SWREG_102 | 0x0198 | W | 0x00000000 | Mvc related |
| VEPU_SWREG_103 | 0x019c | W | 0x00000000 | Encoder start |
| VEPU_SWREG_104 | 0x01a0 | W | 0x00000000 | Mb control register |
| VEPU_SWREG_105 | 0x01a4 | W | 0x00000000 | Swap ctrl register |
| VEPU_SWREG_106_REUSE | 0x01a8 | W | 0x00000000 | Encoder control register 1 |
| VEPU_SWREG_107_REUSE | 0x01ac | W | 0x00000000 | JPEG control register |
| VEPU_SWREG_108_REUSE | 0x01b0 | W | 0x00000000 | Intra slice bmp2 |
| VEPU_SWREG_109 | 0x01b4 | W | 0x00001000 | Encoder status |
| VEPU_SWREG_110_READ | 0x01b8 | W | 0x48311220 | Product ID |
| VEPU_SWREG_120_183 | 0x01e0 | W | 0x00000000 | Addr range: 0x01e0~0x02dc<br>Swreg120: DMV 4p/1p penalty table values<br>Swreg121: DMV 4p/1p penalty table values<br>Swreg122: DMV 4p/1p penalty table values<br>Swreg123: DMV 4p/1p penalty table values<br>.....<br>Swreg183: DMV 4p/1p penalty table values |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

## 5.5.26 VEPU121 Detail Registers Description

Rockchip Confidential

**VEPU_SWREG_0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_luma_quant1<br>Jpeg luma quantization 1 |

**VEPU_SWREG_1**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_luma_quant2<br>Jpeg luma quantization 2 |

**VEPU_SWREG_2**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_luma_quant3<br>Jpeg luma quantization 3 |

**VEPU_SWREG_3**

Address: Operational Base + offset (0x000c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_luma_quant4<br>Jpeg luma quantization 4 |

**VEPU_SWREG_4**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_luma_quant5<br>Jpeg luma quantization 5 |

**VEPU_SWREG_5**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_luma_quant6<br>Jpeg luma quantization 6 |

**VEPU_SWREG_6**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Sw_jpeg_luma_quant7<br>Jpeg luma quantization 7 |

**VEPU_SWREG_7**

Address: Operational Base + offset (0x001c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_luma_quant8<br>Jpeg luma quantization 8 |

**VEPU_SWREG_8**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_luma_quant9<br>Jpeg luma quantization 9 |

**VEPU_SWREG_9**

Rockchip Confidencial

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Sw_jpeg_luma_quant10<br>Jpeg luma quantization 10 |

**VEPU_SWREG_10**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_luma_quant11<br>Jpeg luma quantization 11 |

**VEPU_SWREG_11**

Address: Operational Base + offset (0x002c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Sw_jpeg_luma_quant12<br>Jpeg luma quantization 12 |

**VEPU_SWREG_12**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_luma_quant13<br>Jpeg luma quantization 13 |

**VEPU_SWREG_13**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_luma_quant14<br>Jpeg luma quantization 14 |

**VEPU_SWREG_14**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_luma_quant15<br>Jpeg luma quantization 15 |

**VEPU_SWREG_15**

Address: Operational Base + offset (0x003c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | Reserved |
| 7:0 | RW | 0x00 | sw_jpeg_luma_quant16<br>Jpeg luma quantization 16 |

**VEPU_SWREG_16**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_chroma_quant1<br>Jpeg chroma quantization 1 |

**VEPU_SWREG_17**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Sw_jpeg_chroma_quant2<br>Jpeg chroma quantization 2 |

**VEPU_SWREG_18**

Rockchip Confidencial

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_chroma_quant3<br>Jpeg chroma quantization 3 |

**VEPU_SWREG_19**

Address: Operational Base + offset (0x004c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_chroma_quant4<br>Jpeg chroma quantization 4 |

**VEPU_SWREG_20**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_chroma_quant5<br>Jpeg chroma quantization 5 |

**VEPU_SWREG_21**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_chroma_quant6<br>Jpeg chroma quantization 6 |

**VEPU_SWREG_22**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_chroma_quant7<br>Jpeg chroma quantization 7 |

**VEPU_SWREG_23**

Address: Operational Base + offset (0x005c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_chroma_quant8<br>Jpeg chroma quantization 8 |

**VEPU_SWREG_24**

Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_chroma_quant9<br>Jpeg chroma quantization 9 |

**VEPU_SWREG_25**

Address: Operational Base + offset (0x0064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_chroma_quant10<br>Jpeg chroma quantization 10 |

**VEPU_SWREG_26**

Address: Operational Base + offset (0x0068)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:9 | RO | 0x000000 | Reserved |
| 8:0 | RW | 0x000 | sw_jpeg_chroma_quant11<br>Jpeg chroma quantization 11 |

**VEPU_SWREG_27**

Rockchip Confidencial

Address: Operational Base + offset (0x006c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_chroma_quant12<br>Jpeg chroma quantization 12 |

**VEPU_SWREG_28**

Address: Operational Base + offset (0x0070)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | Reserved |
| 11:0 | RW | 0x000 | sw_jpeg_chroma_quant13<br>Jpeg chroma quantization 13 |

**VEPU_SWREG_29**

Address: Operational Base + offset (0x0074)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_chroma_quant14<br>Jpeg chroma quantization 14 |

**VEPU_SWREG_30**

Address: Operational Base + offset (0x0078)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | Reserved |
| 11:0 | RW | 0x000 | sw_jpeg_chroma_quant15<br>Jpeg chroma quantization 15 |

**VEPU_SWREG_31**

Address: Operational Base + offset (0x007c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_jpeg_chroma_quant16<br>Jpeg chroma quantization 16 |

**VEPU_SWREG_44**

Address: Operational Base + offset (0x00b0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | intra_slice_bmp0<br>Bit0 : Slices0<br>Bit1 : Slices1<br>Bit2 : Slices2<br>.....<br>Bit31 : Slices31 |

**VEPU_SWREG_45**

Address: Operational Base + offset (0x00b4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | intra_slice_bmp1<br>Bit0 : Slices32<br>Bit1 : Slices33<br>Bit2 : Slices34<br>.....<br>Bit31 : Slices63 |

**VEPU_SWREG_46**

Address: Operational Base + offset (0x00b8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | intra_up_mb_area<br>The top intra macro block's area used in row. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:16 | RW | 0x00 | intra_down_mb_area<br>The bottom intra macro block's area used in row. |
| 15:8 | RW | 0x00 | intra_left_mb_area<br>The left intra macro block's area used in column. |
| 7:0 | RW | 0x00 | intra_right_mb_area<br>The right intra macro block's area used in column. |

**VEPU_SWREG_47**

Address: Operational Base + offset (0x00bc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | cir_first_intra<br>16'd0: Disable<br>Other: Enable and be set |
| 15:0 | RW | 0x0000 | cir_intra_mb_itvl<br>16'd0: Disable<br>Other: Enable and be set |

**VEPU_SWREG_48**

Address: Operational Base + offset (0x00c0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | luma_in_st_adr<br>Input luma start address |

**VEPU_SWREG_49**

Address: Operational Base + offset (0x00c4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | cb_in_st_adr<br>Input cb start address |

**VEPU_SWREG_50**

Address: Operational Base + offset (0x00c8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | cr_in_st_adr<br>Input cr start address |

**VEPU_SWREG_51**

Address: Operational Base + offset (0x00cc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | strm_header_left_hbits<br>The high 32 bit of stram header be left. |

**VEPU_SWREG_52**

Address: Operational Base + offset (0x00d0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | strm_header_left_lbits<br>The low 32 bit of stram header be left. |

**VEPU_SWREG_53**

Address: Operational Base + offset (0x00d4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | strm_bufsize_lmt<br>The limit  size of steam buffer. |

**VEPU_SWREG_54**

Rockchip Confidencial

Address: Operational Base + offset (0x00d8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x01 | axi_rd_id<br>If config 0,it will be modify as 1 by HW auto |
| 23:16 | RW | 0x01 | axi_wr_id<br>If config 0,it will be modify as 1 by HW auto |
| 15:14 | RO | 0x0 | Reserved |
| 13:8 | RW | 0x00 | burst_len<br>Burst length |
| 7:3 | RO | 0x00 | Reserved |
| 2 | RW | 0x0 | burst_incr_mod_sel<br>1'b0: Single burst selected<br>1'b1: Incr burst selected |
| 1 | RW | 0x0 | burst_discard<br>1'b0: Disable, off<br>1'b1: Enable, on |
| 0 | RW | 0x0 | burst_disable<br>1'b0: Enable<br>1'b1: Disable |

**VEPU_SWREG_55**

Address: Operational Base + offset (0x00dc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | Reserved |
| 15:12 | RW | 0x0 | roi_dlt_qp1<br>1st for delta qp for roi |
| 11:8 | RW | 0x0 | roi_dlt_qp2<br>2st for delta qp for roi |
| 7:4 | RO | 0x0 | Reserved |
| 3:0 | RW | 0x0 | qp_adjst<br>Signed register;<br>Range from -8 to 7 |

**VEPU_SWREG_56**

Address: Operational Base + offset (0x00e0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | luma_ref_st_adr<br>The luma reference frame start address |

**VEPU_SWREG_57**

Address: Operational Base + offset (0x00e4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | chroma_ref_st_adr<br>The chroma reference frame start address |

**VEPU_SWREG_58**

Address: Operational Base + offset (0x00e8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:11 | RW | 0x000000 | qp_sum_div2<br>The result of (qp sum)/2 |

**VEPU_SWREG_59**

Address: Operational Base + offset (0x00ec)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | Reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 28 | RW | 0x0 | h264_qurt_pixmv_dis<br>1'b1: Disable<br>1'b0: Default, enable |
| 27:26 | RO | 0x0 | Reserved |
| 25:24 | RW | 0x0 | dblking_flt_mode<br>2'd0: Enabled<br>2'd1: Disabled<br>2'd2: Disabled on slice |
| 23 | RO | 0x0 | Reserved |
| 22:21 | RW | 0x0 | h264_cabac_idc<br>2'd0,2'd1,2'd2: Used<br>2'd3: No use |
| 20 | RW | 0x0 | entry_code_fmt<br>H.264:<br>1'b0: Cavlc<br>1'b1: Cabac |
| 19:18 | RO | 0x0 | Reserved |
| 17 | RW | 0x0 | h264_trfmod_8x8<br>On-off for 8x8 transform used in h264 |
| 16 | RW | 0x0 | h264_res_intermod_4x4<br>The restriction inter mode selected in 4x4 block |
| 15 | RW | 0x0 | h264_strm_mod_sel<br>1'b0: NAL unit<br>1'b1: BYTE |
| 14:8 | RW | 0x00 | h264_slice_num<br>7'b0: One slice in currect picture<br>7'b1: Two slice in currect picture<br>..... |

**VEPU_SWREG_60**

Address: Operational Base + offset (0x00f0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | Reserved |
| 21:16 | RW | 0x00 | strm_st_offset |
| 15:8 | RW | 0x00 | skip_mb_mode<br>H264: SKIP macroblock mode |
| 7:6 | RO | 0x0 | Reserved |
| 5:4 | RW | 0x0 | right_spill<br>Div4 value<br>Range: 0~3 |
| 3:0 | RW | 0x0 | bot_spill<br>The bottom edge of image for spill pixels |

**VEPU_SWREG_61**

Address: Operational Base + offset (0x00f4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x000 | Reserved |
| 22:20 | RW | 0x0 | offset_in_chroma<br>Byte unit |
| 19 | RO | 0x0 | Reserved |
| 18:16 | RW | 0x0 | offset_in_luma<br>Byte unit |
| 15:14 | RO | 0x0 | Reserved |
| 13:0 | RW | 0x0000 | row_len_in_luma |

Rockchip Confidencial

**VEPU_SWREG_62**

Address: Operational Base + offset (0x00f8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | Reserved |
| 21:0 | RW | 0x000000 | rlc_sum<br>Rlc_sum |

**VEPU_SWREG_63**

Address: Operational Base + offset (0x00fc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | recon_luma_st_adr<br>The reconstructed luma start address |

**VEPU_SWREG_64**

Address: Operational Base + offset (0x0100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | recon_chroma_st_adr<br>The reconstructed chroma start address |

**VEPU_SWREG_65_REUSE**

Address: Operational Base + offset (0x0104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | h264_chkpt_1<br>1st word used for check point used in h.264 |
| 15:0 | RW | 0x0000 | h264_chkpt_2<br>2st word used for check point used in h.264 |

**VEPU_SWREG_66_REUSE**

Address: Operational Base + offset (0x0108)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | h264_chkpt_3<br>3st word used for check point used in h.264 |
| 15:0 | RW | 0x0000 | h264_chkpt_4<br>4st word used for check point used in h.264 |

**VEPU_SWREG_67_REUSE**

Address: Operational Base + offset (0x010c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | h264_chkpt_5<br>5st word used for check point used in h.264 |
| 15:0 | RW | 0x0000 | h264_chkpt_6<br>6st word used for check point used in h.264 |

**VEPU_SWREG_68_REUSE**

Address: Operational Base + offset (0x0110)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | h264_chkpt_7<br>7st word used for check point used in h.264 |
| 15:0 | RW | 0x0000 | h264_chkpt_8<br>8st word used for check point used in h.264 |

**VEPU_SWREG_69_REUSE**

Address: Operational Base + offset (0x0114)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | h264_chkpt_9<br>9st word used for check point used in h.264 |
| 15:0 | RW | 0x0000 | h264_chkpt_10<br>10st word used for check point used in h.264 |

**VEPU_SWREG_70_REUSE**

Address: Operational Base + offset (0x0118)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | h264_errchkpt_1<br>1st word error check point used in h.264 |
| 15:0 | RW | 0x0000 | h264_errchkpt_2<br>2st word error check point used in h.264 |

**VEPU_SWREG_71_REUSE**

Address: Operational Base + offset (0x011c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | h264_errchkpt_3<br>3st word error check point used in h.264 |
| 15:0 | RW | 0x0000 | h264_errchkpt_4<br>4st word error check point used in h.264 |

**VEPU_SWREG_72_REUSE**

Address: Operational Base + offset (0x0120)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | h264_errchkpt_5<br>5st word error check point used in h.264 |
| 15:0 | RW | 0x0000 | h264_errchkpt_6<br>6st word error check point used in h.264 |

**VEPU_SWREG_73_REUSE**

Address: Operational Base + offset (0x0124)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | Reserved |
| 27:24 | RW | 0x0 | chkqp_1<br>1st for delta qp check point |
| 23:20 | RW | 0x0 | chkqp_2<br>2st for delta qp check point |
| 19:16 | RW | 0x0 | chkqp_3<br>3st for delta qp check point |
| 15:12 | RW | 0x0 | chkqp_4<br>4st for delta qp check point |
| 11:8 | RW | 0x0 | chkqp_5<br>5st for delta qp check point |
| 7:4 | RW | 0x0 | chkqp_6<br>6st for delta qp check point |
| 3:0 | RW | 0x0 | chkqp_7<br>7st for delta qp check point |

**VEPU_SWREG_74**

Address: Operational Base + offset (0x0128)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | Reserved |
| 29:24 | RW | 0x00 | mad_thsld<br>Value = (MAD threshold)/256 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:16 | RW | 0x00 | encodered_slices<br>The number of encoder slices which used in h.264 |
| 15:8 | RO | 0x00 | Reserved |
| 7:4 | RW | 0x0 | img_fmt_in<br>YUV420P<br>YUV420SP<br>YUV422<br>UYVY422<br>RGB565<br>RGB444<br>RGB888<br>RGB101010 |
| 3:2 | RW | 0x0 | Img_in_rot<br>2'd0: No rotation<br>2'd1: Rotate right 90 degress<br>2'd2: Rotate left 90 degress |
| 1 | RO | 0x0 | Reserved |
| 0 | RW | 0x0 | nal_mode<br>The output of NAL size to base control |

**VEPU_SWREG_75**

Address: Operational Base + offset (0x012c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | intramod_16x16 |
| 15:0 | RW | 0x0000 | intermod<br>The intra/inter selection for inter macro block mode favor. |

**VEPU_SWREG_76_REUSE**

Address: Operational Base + offset (0x0130)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RW | 0x00 | pps_init_qp<br>Pps init qp in picture used in h264.<br>Range: 0~51 |
| 25:22 | RW | 0x0 | slice_flt_alpha<br>Offset div2<br>Range: -6~6 |
| 21:18 | RW | 0x0 | slice_flt_beta<br>Config value = (real value)/2<br>Signed register<br>Range: -6 ~6 |
| 17:13 | RW | 0x00 | qp_offset_ch<br>Signed register<br>Range: -12~12 |
| 12:9 | RO | 0x0 | Reserved |
| 8 | RW | 0x0 | sw_qpass |
| 7:5 | RO | 0x0 | Reserved |
| 4:1 | RW | 0x0 | idr_picid<br>IDR pic ID |
| 0 | RW | 0x0 | constr_intra_pred<br>Constrained intra prediction |

**VEPU_SWREG_77**

Address: Operational Base + offset (0x0134)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | output_strm_st_adr<br>Output stream start address |

**VEPU_SWREG_78**

Address: Operational Base + offset (0x0138)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | output_ctrl_st_adr<br>Output control start address |

**VEPU_SWREG_79**

Address: Operational Base + offset (0x013c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | next_luma_st_adr<br>Next picture luminance start address |

**VEPU_SWREG_80**

Address: Operational Base + offset (0x0140)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | mv_out_st_adr<br>Mv wr start address |

**VEPU_SWREG_81**

Address: Operational Base + offset (0x0144)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | cabac_table_st_adr<br>H264: Cabac table |

**VEPU_SWREG_82**

Address: Operational Base + offset (0x0148)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | first_roi_tmb<br>(Inside area) |
| 23:16 | RW | 0x00 | first_roi_bmb<br>(Outside area) |
| 15:8 | RW | 0x00 | first_roi_lmb<br>Qp=qp + roi1_Delta_Qp<br>(Inside area) |
| 7:0 | RW | 0x00 | first_roi_rmb<br>Qp=qp - roi1_Delta_Qp<br>(Outside area) |

**VEPU_SWREG_83**

Address: Operational Base + offset (0x014c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | second_roi_rmb<br>(Inside area) |
| 23:16 | RW | 0x00 | second_roi_bmb<br>(Outside area) |
| 15:8 | RW | 0x00 | second_roi_lmb<br>Qp=qp + roi1_Delta_Qp<br>(Inside area) |
| 7:0 | RW | 0x00 | second_roi_tmb<br>Qp=qp - roi1_Delta_Qp<br>(Outside area) |

Rockchip Confidencial

**VEPU_SWREG_84**

Address: Operational Base + offset (0x0150)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | Reserved |
| 23:0 | RW | 0x000000 | stab_matrix1<br>(Position@ up-left) |

**VEPU_SWREG_85**

Address: Operational Base + offset (0x0154)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | Reserved |
| 23:0 | RW | 0x000000 | stab_matrix2<br>(Position @ up) |

**VEPU_SWREG_86**

Address: Operational Base + offset (0x0158)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | Reserved |
| 23:0 | RW | 0x000000 | stab_matrix3<br>(Position @up-right) |

**VEPU_SWREG_87**

Address: Operational Base + offset (0x015c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23:0 | RW | 0x000000 | stab_matrix4<br>(Position @ left) |

**VEPU_SWREG_88**

Address: Operational Base + offset (0x0160)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23:0 | RW | 0x000000 | stab_matrix5<br>(Position @GMV ) |

**VEPU_SWREG_89**

Address: Operational Base + offset (0x0164)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | Reserved |
| 23:0 | RW | 0x000000 | stab_matrix6<br>(Position@right ) |

**VEPU_SWREG_90**

Address: Operational Base + offset (0x0168)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | Reserved |
| 23:0 | RW | 0x000000 | stab_matrix7<br>(Position@down-left) |

**VEPU_SWREG_91**

Address: Operational Base + offset (0x016c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | Reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:0 | RW | 0x000000 | stab_matrix8<br>(Position@down ) |

**VEPU_SWREG_92**

Address: Operational Base + offset (0x0170)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RW | 0x00 | stab_gmv_vrtl<br>Signed register<br>Range: -16~16 |
| 25:24 | RO | 0x0 | Reserved |
| 23:0 | RW | 0x000000 | stab_matrix9<br>(Position@down- right ) |

**VEPU_SWREG_93**

Address: Operational Base + offset (0x0174)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | stab_motion_sum<br>Read value = (real value)/8<br>Range: 0~1089*253*255*53/8 |

**VEPU_SWREG_94**

Address: Operational Base + offset (0x0178)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RW | 0x000000 | stab_min_value<br>Range: 0~255*253*253 |
| 7:6 | RW | 0x0 | stab_mod_sel<br>2'd0: Disabled<br>2'd1: Stab only<br>2'd2: Stab+encode<br>2'd3: Reservde |
| 5:0 | RW | 0x00 | stab_hor_gmv<br>Signed register<br>Range: -16~16 |

**VEPU_SWREG_95**

Address: Operational Base + offset (0x017c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | rgb2yuv_coe2<br>The 2st conversion coefficien for RGB to YUV |
| 15:0 | RW | 0x0000 | rgb2yuv_coe1<br>The 1st conversion coefficien for RGB to YUV |

**VEPU_SWREG_96**

Address: Operational Base + offset (0x0180)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | rgb2yuv_coe5<br>The 5st conversion coefficien for RGB to YUV |
| 15:0 | RW | 0x0000 | rgb2yuv_coe3<br>The 3st conversion coefficien for RGB to YUV |

**VEPU_SWREG_97**

Address: Operational Base + offset (0x0184)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | Reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0000 | rgb2yuv_coe6<br>The 6st conversion coefficien for RGB to YUV |

**VEPU_SWREG_98**

Address: Operational Base + offset (0x0188)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x000 | Reserved |
| 20:16 | RW | 0x00 | bcmpt_mask_postition<br>Range: 0~31 |
| 15:13 | RO | 0x0 | Reserved |
| 12:8 | RW | 0x00 | gcmpt_mask_postition<br>Range: 0~31 |
| 7:5 | RO | 0x0 | Reserved |
| 4:0 | RW | 0x00 | rcmpt_mask_postition<br>Range: 0~31 |

**VEPU_SWREG_99**

Address: Operational Base + offset (0x018c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | Reserved |
| 30:21 | RW | 0x000 | mv_1p_ply<br>Differential MV penalty for 1p |
| 20:11 | RW | 0x000 | mv_1p_4p_ply<br>ME. DMVPenaltyQp |
| 10:1 | RW | 0x000 | mv_4p_ply<br>4p of differential MV penalty |
| 0 | RW | 0x0 | mutimv_en<br>On-off flag for using exceed one mv every mb. |

**VEPU_SWREG_100_REUSE**

Address: Operational Base + offset (0x0190)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RW | 0x00 | h264_init_luma_qp<br>Range: 0~51 |
| 25:20 | RW | 0x00 | h264_max_qp<br>Range: 0~51 |
| 19:14 | RW | 0x00 | h264_min_qp<br>Range: 0~51 |
| 13 | RO | 0x0 | Reserved |
| 12:0 | RW | 0x0000 | h264_chkpt_distance<br>Checkpoint distance for macro block |

**VEPU_SWREG_101_READ**

Address: Operational Base + offset (0x0194)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x1f522 | hw_config<br>Hardware config |
| 11:0 | RO | 0x780 | max_vid_width<br>Max vid_width |

**VEPU_SWREG_102**

Address: Operational Base + offset (0x0198)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | Reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:20 | RW | 0x0 | mv_favor_16x16<br>Value = (real value)/2. |
| 19:11 | RW | 0x000 | mv_ply_4x4<br>4x4 Mv Penalty |
| 10:8 | RW | 0x0 | mvc_view_id<br>MVC view id |
| 7 | RW | 0x0 | mvc_anchor_pic_flag<br>To specifie picture is one part of anchor access unit |
| 6:4 | RW | 0x0 | mvc_priority_id<br>MVC priority id |
| 3:1 | RW | 0x0 | mvc_temporal_id<br>MVC temporal id |
| 0 | RW | 0x0 | mvc_inter_view_flag<br>MVC inter_view_flag. |

**VEPU_SWREG_103**

Address: Operational Base + offset (0x019c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | Rreserved |
| 28:20 | RW | 0x000 | enc_height<br>Lum height (macroblock unit)<br>H264: [6..255]<br>JPEG: [6..511] |
| 19:17 | RO | 0x0 | Reserved |
| 16:8 | RW | 0x000 | enc_width<br>Lum width (macroblock unit)<br>H264:<br>Range: 9~255<br>JPEG:<br>Range: 6~511 |
| 7:6 | RW | 0x0 | enc_frame_type<br>2'd0: INTER<br>2'd1: INTRA(IDR)<br>2'd2: MVC-INTER<br>2'd3: Reserved |
| 5:4 | RW | 0x0 | enc_fmt<br>2'd2: JPEG<br>2'd3: H264<br>Other: Reserved |
| 3:1 | RO | 0x0 | Reserved |
| 0 | RW | 0x0 | enc_en<br>Encoder enable |

**VEPU_SWREG_104**

Address: Operational Base + offset (0x01a0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | mb_count_out<br>Mb_count_out |
| 15:0 | RW | 0x0000 | mb_cnt<br>Macroblock_count |

**VEPU_SWREG_105**

Address: Operational Base + offset (0x01a4)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | swap8_in<br>1'b0: No swap<br>1'b1: Swap 8bit |
| 30 | RW | 0x0 | swap16_in<br>1'b0: No swap<br>1'b1: Swap 16bit |
| 29 | RW | 0x0 | swap32_in<br>1'b0: No swap<br>1'b1: Swap 32bit |
| 28 | RW | 0x0 | swap8_out<br>1'b0: No swap<br>1'b1: Swap 8bit |
| 27 | RW | 0x0 | swap16_out<br>1'b0: No swap<br>1'b1: Swap 16bit |
| 26 | RW | 0x0 | swap32_out<br>1'b0: No swap<br>1'b1: Swap 32bit |
| 25 | RO | 0x0 | Reserved |
| 24 | RW | 0x0 | test_irq<br>Test irq |
| 23:20 | RW | 0x0 | test_counter<br>Test counter |
| 19 | RW | 0x0 | coher_test_reg<br>Test register coherency |
| 18 | RW | 0x0 | coher_test_mem<br>Test memory coherency |
| 17:0 | RW | 0x00000 | test_len<br>Test data length |

**VEPU_SWREG_106_REUSE**

Address: Operational Base + offset (0x01a8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | pic_para_id<br>H.264 picture parameter id set |
| 23:16 | RW | 0x00 | intra_pred_mode<br>H.264 intra prediction previous 4x4 mode favor |
| 15:0 | RW | 0x0000 | frame_num<br>H.264 frame number |

**VEPU_SWREG_107_REUSE**

Address: Operational Base + offset (0x01ac)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | Reserved |
| 29:20 | RW | 0x000 | mv_ply_16x8_8x16<br>Penalty for using 16x8 or 8x16 MV |
| 19:10 | RW | 0x000 | mv_ply_8x8<br>Penalty for using 8x8 MV |
| 9:0 | RW | 0x000 | mv_ply_8x4_4x8<br>Penalty for using 8x4 or 4x8 MV. |

**VEPU_SWREG_108_REUSE**

Address: Operational Base + offset (0x01b0)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | intra_slice_bmp2<br>Bit0: Slices64<br>Bit1: Slices65<br>Bit2: Slices66<br>.....<br>Bit31: Slices95 |

**VEPU_SWREG_109**

Address: Operational Base + offset (0x01b4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x0 | Reserved |
| 24 | RW | 0x0 | mv_sad_wren<br>The each MB MV and SAD be writed to mv_wr_st_adr enable |
| 23:21 | RO | 0x0 | Reserved |
| 20 | RW | 0x0 | rocon_write_dis<br>Write reconstructed image disable flag |
| 19:17 | RO | 0x0 | Reserved |
| 16 | RW | 0x0 | slice_rdyint_en<br>Enable slice ready interruupt |
| 15:13 | RO | 0x0 | Reserved |
| 12 | RW | 0x1 | clk_gating_en<br>Default clk_gating_en =1'b1 |
| 11 | RO | 0x0 | Reserved |
| 10 | RW | 0x0 | int_timeout_en<br>Enable interrupt for timeout |
| 9 | RW | 0x0 | irq_clr<br>Irq clear |
| 8 | RW | 0x0 | irq_dis<br>Irq disable |
| 7 | RO | 0x0 | Reserved |
| 6 | RW | 0x0 | irq_timeout<br>HW wait timeout flag |
| 5 | RW | 0x0 | irq_buffer_full<br>Buffer full flag |
| 4 | RW | 0x0 | irq_bus_error<br>Bus error irq |
| 3 | RW | 0x0 | fuse_int<br>Fuse irq |
| 2 | RW | 0x0 | irq_slice_ready<br>Slice ready flag |
| 1 | RW | 0x0 | irq_frame_rdy<br>One frame encoder sucess flag |
| 0 | RW | 0x0 | enc_irq<br>Enc interrupt |

**VEPU_SWREG_110_READ**

Address: Operational Base + offset (0x01b8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x4831 | prod_id<br>Product ID |
| 15:12 | RO | 0x1 | major_num<br>Major number |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:4 | RO | 0x22 | minor_num<br>Minor number |
| 3:0 | RO | 0x0 | synthesis<br>{ASCII_ID_E,BUILDNUMBER} |

**VEPU_SWREG_120_183**

Address: Operational Base + offset (0x01e0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | WO | 0x00000000 | dmv_ply_table<br>Addr range: 0x01e0~0x02dc<br>Swreg120: DMV 4p/1p penalty table values<br>Swreg121: DMV 4p/1p penalty table values<br>Swreg122: DMV 4p/1p penalty table values<br>Swreg123: DMV 4p/1p penalty table values<br>.....<br>Swreg183: DMV 4p/1p penalty table values |

## 5.5.27 VEPU121 MMU Detail Registers Description

**VCODEC_MMU_DTE_ADDR**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | mmu_dte_addr<br>MMU current page Table address |

**VCODEC_MMU_STATUS**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:11 | RO | 0x000000 | Reserved |
| 10:6 | RO | 0x00 | page_fault_bus_id<br>Index of master responsible for last page fault |
| 5 | RO | 0x0 | page_fault_is_write<br>The direction of access for last page fault:<br>1'b0: Read<br>1'b1: Write |
| 4 | RO | 0x1 | replay_buffer_empty<br>1'b1:The MMU replay buffer is empty |
| 3 | RO | 0x1 | mmu_idle<br>The MMU is idle when accesses are being translated and there are no unfinished translated accesses.<br>1'b1: MMU is idle |
| 2 | RO | 0x0 | stail_active<br>MMU stall mode currently enabled. The mode is enabled by command<br>1'b1: MMU is in stall active status |
| 1 | RO | 0x0 | page_fault_active<br>MMU page fault mode currently enabled. The mode is enabled by command.<br>1'b1: Page fault is active |
| 0 | RO | 0x0 | paging_enabled<br>1'b0: Paging is disabled<br>1'b1: Paging is enabled |

**VCODEC_MMU_COMMAND**

Address: Operational Base + offset (0x0008)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | Reserved |
| 2:0 | WO | 0x0 | mmu_cmd<br>MMU_CMD. This can be:<br>3'd0: MMU_ENABLE_PAGING<br>3'd1: MMU_DISABLE_PAGING<br>3'd2: MMU_ENABLE_STALL<br>3'd3: MMU_DISABLE_STALL<br>3'd4: MMU_ZAP_CACHE<br>3'd5: MMU_PAGE_FAULT_DONE<br>3'd6: MMU_FORCE_RESET |

**VCODEC_MMU_PAGE_FAULT_ADDR**

Address: Operational Base + offset (0x000c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | page_fault_addr<br>Address of last page fault |

**VCODEC_MMU_ZAP_ONE_LINE**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | WO | 0x00000000 | mmu_zap_one_line<br>ddress to be invalidated from the page table cache |

**VCODEC_MMU_INT_RAWSTAT**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | Reserved |
| 1 | RW | 0x0 | read_bus_error<br>Read bus error status |
| 0 | RW | 0x0 | page_fault<br>Page fault status |

**VCODEC_MMU_INT_CLEAR**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | Reserved |
| 1 | WO | 0x0 | read_bus_error<br>Write 1 to clear read bus error |
| 0 | WO | 0x0 | page_fault<br>Write 1 to page fault clear |

**VCODEC_MMU_INT_MASK**

Address: Operational Base + offset (0x001c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | Reserved |
| 1 | RW | 0x0 | read_bus_error<br>Enable the read bus interrupt source when this bit is set to 1'b1 |
| 0 | RW | 0x0 | page_fault<br>Enable the page fault interrupt source when this bit is set to 1'b1 |

**VCODEC_MMU_INT_STATUS**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | Reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RO | 0x0 | read_bus_error<br>1'b1: Read bus error status |
| 0 | RO | 0x0 | page_fault<br>1'b1: Page fault |

**VCODEC_MMU_AUTO_GATING**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | Reserved |
| 0 | RW | 0x1 | mmu_auto_clkgating<br>When it is 1'b1, the mmu will auto gating it self |

## 5.5.28 VEPU580 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VEPU580_VERSION | 0x0000 | W | 0x5060030B | VEPU Version Register |
| VEPU580_ENC_STRT | 0x0010 | W | 0x00000000 | VEPU Start Command Register |
| VEPU580_ENC_CLR | 0x0014 | W | 0x00000000 | VEPU Clear Command Register |
| VEPU580_INT_EN | 0x0020 | W | 0x00000000 | Interrupt Enable Register |
| VEPU580_INT_MSK | 0x0024 | W | 0x00000000 | Interrupt Mask Register |
| VEPU580_INT_CLR | 0x0028 | W | 0x00000000 | Interrupt Clear Register |
| VEPU580_INT_STA | 0x002C | W | 0x00000000 | Interrupt Status Register |
| VEPU580_DBUS_ENDIAN | 0x0030 | W | 0x00000000 | Data Bus Endian |
| VEPU580_DBUS_CFG | 0x0034 | W | 0x00000000 | Data Bus Configuration |
| VEPU580_ENC_WDG | 0x0038 | W | 0x00000000 | VEPU Watch Dog |
| VEPU580_CORE_ID | 0x005C | W | 0x00000000 | Core ID |
| VEPU580_LKT_BASE_ADDR | 0x0070 | W | 0x00000000 | Link Table Base Address |
| VEPU580_NODE_ID | 0x0100 | W | 0x00000000 | Core ID of Link Table Node |
| VEPU580_NODE_ADR_FCFG | 0x0104 | W | 0x00000000 | Address of Frame Configuration Section in Link Table Node |
| VEPU580_NODE_ADR_RC | 0x0108 | W | 0x00000000 | Address of Rate Control Section in Link Table Node |
| VEPU580_NODE_ADR_PAR | 0x010C | W | 0x00000000 | Address of Parameter Section in Link Table Node |
| VEPU580_NODE_ADR_SA | 0x0110 | W | 0x00000000 | Address of Subjective Adjustment Section in Link Table Node |
| VEPU580_NODE_ADR_SCAL | 0x0114 | W | 0x00000000 | Address of Scaling List Section in Link Table Node |
| VEPU580_NODE_ADR_OSD | 0x0118 | W | 0x00000000 | Address of OSD Section in Link Table Node |
| VEPU580_NODE_ADR_INF | 0x011C | W | 0x00000000 | Encoding Information Section in Link Table Node |
| VEPU580_NODE_ADR_NXT | 0x0120 | W | 0x00000000 | Address of the next Link Table Node |
| VEPU580_ADR_SRC0 | 0x0280 | W | 0x00000000 | Address of Video Source Buffer0 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VEPU580_ADR_SRC1 | 0x0284 | W | 0x00000000 | Address of Video Source Buffer1 |
| VEPU580_ADR_SRC2 | 0x0288 | W | 0x00000000 | Address of Video Source Buffer2 |
| VEPU580_ADR_RECW_H | 0x028C | W | 0x00000000 | Write Address of Reconstruction Header Buffer |
| VEPU580_ADR_RFPW_B | 0x0290 | W | 0x00000000 | Write Address of Reconstruction Body Buffer |
| VEPU580_ADR_RFPR_H | 0x0294 | W | 0x00000000 | Read Address of Reconstruction Header Buffer |
| VEPU580_ADR_RFPR_B | 0x0298 | W | 0x00000000 | Read Address of Reconstruction Body Buffer |
| VEPU580_ADR_CMVW | 0x029C | W | 0x00000000 | Write Address of Col-Mv Buffer |
| VEPU580_ADR_CMVR | 0x02A0 | W | 0x00000000 | Read Address of Col-Mv Buffer |
| VEPU580_ADR_DSPW | 0x02A4 | W | 0x00000000 | Write Address of Down Sample Picture Buffer |
| VEPU580_ADR_DSPR | 0x02A8 | W | 0x00000000 | Read Address of Down Sample Picture Buffer |
| VEPU580_ADR_MEIW | 0x02AC | W | 0x00000000 | Write Address of ME Information Buffer |
| VEPU580_ADR_BSBT | 0x02B0 | W | 0x00000000 | Top Address of Bit Stream Buffer |
| VEPU580_ADR_BSBB | 0x02B4 | W | 0x00000000 | Bottom Address of Bit Stream Buffer |
| VEPU580_ADR_BSBR | 0x02B8 | W | 0x00000000 | Read Address of Bit Stream Buffer |
| VEPU580_ADR_BSBS | 0x02BC | W | 0x00000000 | Start Address of Bit Stream Buffer |
| VEPU580_ADR_TILEW | 0x02C0 | W | 0x00000000 | Write Address of TILE Buffer |
| VEPU580_ADR_TILER | 0x02C4 | W | 0x00000000 | Read Address of TILE Buffer |
| VEPU580_ADR_ROI_BASE | 0x02C8 | W | 0x00000000 | Address of ROI Base Buffer |
| VEPU580_ADR_ROI_QP | 0x02CC | W | 0x00000000 | Address of ROI QP buffer |
| VEPU580_ADR_ROI_AMV | 0x02D0 | W | 0x00000000 | Address of ROI AMV Buffer |
| VEPU580_ADR_ROI_FMV | 0x02D4 | W | 0x00000000 | Address of ROI Forced Mv Buffer |
| VEPU580_ADR_ELBT | 0x02D8 | W | 0x00000000 | Top Address of External Line Buffer |
| VEPU580_ADR_ELBB | 0x02DC | W | 0x00000000 | Bottom Address of External Line Buffer |
| VEPU580_CMN_CFG | 0x0300 | W | 0x00000000 | VEPU Common Configuration |
| VEPU580_ENC_RSL | 0x0310 | W | 0x00000000 | Video Resolution |
| VEPU580_SRC_EXT | 0x0314 | W | 0x00000000 | Video Source Extension For Alignment |
| VEPU580_SRC_FMT | 0x0318 | W | 0x00000000 | Video Source Format |
| VEPU580_SRC_UDFY | 0x031C | W | 0x00000000 | Weight of User Defined RGB to Y Conversion |
| VEPU580_SRC_UDFU | 0x0320 | W | 0x00000000 | Weight of User Defined RGB to U Conversion |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VEPU580_SRC_UDFV | 0x0324 | W | 0x00000000 | Weight of User Defined RGB to V Conversion |
| VEPU580_SRC_UDFO | 0x0328 | W | 0x00000000 | Offset of User Defined RGB to YUV Conversion |
| VEPU580_SRC_PROC | 0x032C | W | 0x00000000 | Video Source Process |
| VEPU580_SRC_OFST | 0x0330 | W | 0x00000000 | Video Source Offset |
| VEPU580_SRC_STRD0 | 0x0334 | W | 0x00000000 | Video Source Stride0 |
| VEPU580_SRC_STRD1 | 0x0338 | W | 0x00000000 | Video Source Stride1 |
| VEPU580_RC_CFG | 0x0350 | W | 0x00000000 | Rate Control Configuration |
| VEPU580_RC_QP | 0x0354 | W | 0x00000000 | Rate Control Qp Configuration |
| VEPU580_RC_TGT | 0x0358 | W | 0x00000000 | Rate Control Target |
| VEPU580_SLI_SPLT | 0x0360 | W | 0x00000000 | Slice Split Configuration |
| VEPU580_SLI_BYTE | 0x0364 | W | 0x00000000 | Byte Length of Slice Split |
| VEPU580_SLI_CNUM | 0x0368 | W | 0x00000000 | CTU/MB Num of Slice Split |
| VEPU580_ME_RNGE | 0x0370 | W | 0x00000000 | Motion Estimation Search Range |
| VEPU580_ME_CFG_HEVC | 0x0374 | W | 0x00080505 | Motion Estimation Configuration for HEVC |
| VEPU580_ME_CFG_H264 | 0x0374 | W | 0x00090505 | Motion Estimation Configuration for H.264 |
| VEPU580_ME_CACH | 0x0378 | W | 0x00000000 | ME Cache Configuration |
| VEPU580_GMV | 0x0380 | W | 0x00000000 | Global Mv |
| VEPU580_ROI_EN | 0x0390 | W | 0x00000000 | ROI enable |
| VEPU580_RDO_CFG_H264 | 0x03A0 | W | 0x00000000 | H.264 RDO Configuration, share address with HEVC |
| VEPU580_RDO_CFG_HEVC | 0x03A0 | W | 0x00000000 | HEVC RDO Configuration, share address with H.264 |
| VEPU580_IPRD_CSTS | 0x03A4 | W | 0x00000000 | Intra Prediction Cost Configuration |
| VEPU580_SYNT_NAL_H264 | 0x03B0 | W | 0x00000000 | NAL configuration for H.264, share address with HEVC |
| VEPU580_SYNT_NAL_HEVC | 0x03B0 | W | 0x00000000 | NAL configuration for HEVC, share address with H.264 |
| VEPU580_SYNT_SPS_H264 | 0x03B4 | W | 0x00000000 | Sequence Parameter Set syntax for H.264, share address with HEVC |
| VEPU580_SYNT_SPS_HEVC | 0x03B4 | W | 0x00000000 | Sequence Parameter Set syntax for HEVC, share address with H.264 |
| VEPU580_SYNT_PPS_H264 | 0x03B8 | W | 0x00000000 | Picture Parameter Set for H.264, share address with HEVC |
| VEPU580_SYNT_PPS_HEVC | 0x03B8 | W | 0x00000000 | Picture Parameter Set for HEVC, share address with H.264 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VEPU580_SYNT_SLI0_H264 | 0x03BC | W | 0x00000000 | Slice Header0 for H.264, share address with HEVC |
| VEPU580_SYNT_SLI0_HEVC | 0x03BC | W | 0x00000000 | Slice Header0 for HEVC, share address with H.264 |
| VEPU580_SYNT_SLI1_H264 | 0x03C0 | W | 0x00000000 | Slice Header1 for H.264, share address with HEVC |
| VEPU580_SYNT_SLI1_HEVC | 0x03C0 | W | 0x00000000 | Slice Header1 for HEVC, share address with H.264 |
| VEPU580_SYNT_SLI2_H264 | 0x03C4 | W | 0x00000000 | Slice Header2 for H.264, share address with HEVC |
| VEPU580_SYNT_SLI2_HEVC | 0x03C4 | W | 0x00000000 | Slice Header2 for HEVC, share address with H.264 |
| VEPU580_SYNT_REFM0_H264 | 0x03C8 | W | 0x00000000 | Reference Frame Mark0 for H.264, share address with HEVC |
| VEPU580_SYNT_REFM0_HEVC | 0x03C8 | W | 0x00000000 | Reference Frame Mark0 for HEVC, share address with H.264 |
| VEPU580_SYNT_REFM1_H264 | 0x03CC | W | 0x00000000 | Reference Frame Mark1 for H.264, share address with HEVC |
| VEPU580_SYNT_REFM1_HEVC | 0x03CC | W | 0x00000000 | Reference Frame Mark1 for HEVC, share address with H.264 |
| VEPU580_SYNT_REFM2_HEVC | 0x03D0 | W | 0x00000000 | Reference Frame Mark2 for HEVC |
| VEPU580_SYNT_REFM2_H264 | 0x03D0 | W | 0x00000000 | Reference Frame Mark2 for H264 |
| VEPU580_SYNT_REFM3_HEVC | 0x03D4 | W | 0x00000000 | Reference Frame Mark3 for HEVC |
| VEPU580_SYNT_LONG_REFM0 | 0x03D8 | W | 0x00000000 | Long term reference frame mark0 for HEVC |
| VEPU580_SYNT_LONG_REFM1 | 0x03DC | W | 0x00000000 | Long term reference frame mark1 for HEVC |
| VEPU580_LINE_SLICE_H264 | 0x03F0 | W | 0x00000000 | Line Slice Configuration, h264 only. |
| VEPU580_TILE_CFG_HEVC | 0x03F0 | W | 0x00000000 | TILE Configuration, HEVC only. |
| VEPU580_TILE_POS | 0x03F4 | W | 0x00000000 | TILE position |
| VEPU580_RC_ADJ0 | 0x1000 | W | 0x00000000 | QP adjust configuration for rate control |
| VEPU580_RC_ADJ1 | 0x1004 | W | 0x00000000 | QP adjust configuration for rate control |
| VEPU580_RC_DTHD0 | 0x1008 | W | 0x00000000 | Bits rate deviation threshold0 |
| VEPU580_RC_DTHD1 | 0x100C | W | 0x00000000 | Bits rate deviation threshold1 |
| VEPU580_RC_DTHD2 | 0x1010 | W | 0x00000000 | Bits rate deviation threshold2 |
| VEPU580_RC_DTHD3 | 0x1014 | W | 0x00000000 | Bits rate deviation threshold3 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VEPU580_RC_DTHD4 | 0x1018 | W | 0x00000000 | Bits rate deviation threshold4 |
| VEPU580_RC_DTHD5 | 0x101C | W | 0x00000000 | Bits rate deviation threshold5 |
| VEPU580_RC_DTHD6 | 0x1020 | W | 0x00000000 | Bits rate deviation threshold6 |
| VEPU580_RC_DTHD7 | 0x1024 | W | 0x00000000 | Bits rate deviation threshold7 |
| VEPU580_RC_DTHD8 | 0x1028 | W | 0x00000000 | Bits rate deviation threshold8 |
| VEPU580_ROI_QTHD0 | 0x1030 | W | 0x00000000 | ROI QP threshold configuration0 |
| VEPU580_ROI_QTHD1 | 0x1034 | W | 0x00000000 | ROI QP threshold configuration1 |
| VEPU580_ROI_QTHD2 | 0x1038 | W | 0x00000000 | ROI QP threshold configuration2 |
| VEPU580_ROI_QTHD3 | 0x103C | W | 0x00000000 | ROI QP threshold configuration3 |
| VEPU580_MADI_CFG | 0x1040 | W | 0x00000000 | MADI configuration. |
| VEPU580_AQ_TTHD0 | 0x1044 | W | 0x00000000 | Texture threshold configuration0 for adaptive QP adjustment. |
| VEPU580_AQ_TTHD1 | 0x1048 | W | 0x00000000 | Texture threshold configuration1 for adaptive QP adjustment. |
| VEPU580_AQ_TTHD2 | 0x104C | W | 0x00000000 | Texture threshold configuration2 for adaptive QP adjustment. |
| VEPU580_AQ_TTHD3 | 0x1050 | W | 0x00000000 | Texture threshold configuration3 for adaptive QP adjustment. |
| VEPU580_AQ_STP0 | 0x1054 | W | 0x00000000 | Adjustment step configuration0 for adaptive QP adjustment. |
| VEPU580_AQ_STP1 | 0x1058 | W | 0x00000000 | Adjustment step configuration1 for adaptive QP adjustment. |
| VEPU580_AQ_STP2 | 0x105C | W | 0x00000000 | Adjustment step configuration2 for adaptive QP adjustment. |
| VEPU580_AQ_STP3 | 0x1060 | W | 0x00000000 | Adjustment step configuration3 for adaptive QP adjustment. |
| VEPU580_MD_SAD_THD | 0x1070 | W | 0x00000000 | SAD thresholds of motion detection. |
| VEPU580_MADI_THD | 0x1074 | W | 0x00000000 | Spatial complexity(MADI) thresholds. |
| VEPU580_KLUT_OFST | 0x1080 | W | 0x00000000 | Offset of (RDO) chroma cost weight table |
| VEPU580_KLUT_WGT0 | 0x1084 | W | 0x00000000 | (RDO) Chroma weight table configure register0 |
| VEPU580_KLUT_WGT1 | 0x1088 | W | 0x00000000 | (RDO) Chroma weight table configure register1 |
| VEPU580_KLUT_WGT2 | 0x108C | W | 0x00000000 | (RDO) Chroma weight table configure register2 |
| VEPU580_KLUT_WGT3 | 0x1090 | W | 0x00000000 | (RDO) Chroma weight table configure register3 |
| VEPU580_KLUT_WGT4 | 0x1094 | W | 0x00000000 | (RDO) Chroma weight table configure register4 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VEPU580_KLUT_WGT5 | 0x1098 | W | 0x00000000 | (RDO) Chroma weight table configure register5 |
| VEPU580_KLUT_WGT6 | 0x109C | W | 0x00000000 | (RDO) Chroma weight table configure register6 |
| VEPU580_KLUT_WGT7 | 0x10A0 | W | 0x00000000 | (RDO) Chroma weight table configure register7 |
| VEPU580_KLUT_WGT8 | 0x10A4 | W | 0x00000000 | (RDO) Chroma weight table configure register8 |
| VEPU580_KLUT_WGT9 | 0x10A8 | W | 0x00000000 | (RDO) Chroma weight table configure register9 |
| VEPU580_KLUT_WGT10 | 0x10AC | W | 0x00000000 | (RDO) Chroma weight table configure register10 |
| VEPU580_KLUT_WGT11 | 0x10B0 | W | 0x00000000 | (RDO) Chroma weight table configure register11 |
| VEPU580_KLUT_WGT12 | 0x10B4 | W | 0x00000000 | (RDO) Chroma weight table configure register12 |
| VEPU580_KLUT_WGT13 | 0x10B8 | W | 0x00000000 | (RDO) Chroma weight table configure register13 |
| VEPU580_KLUT_WGT14 | 0x10BC | W | 0x00000000 | (RDO) Chroma weight table configure register14 |
| VEPU580_KLUT_WGT15 | 0x10C0 | W | 0x00000000 | (RDO) Chroma weight table configure register15 |
| VEPU580_KLUT_WGT16 | 0x10C4 | W | 0x00000000 | (RDO) Chroma weight table configure register16 |
| VEPU580_KLUT_WGT17 | 0x10C8 | W | 0x00000000 | (RDO) Chroma weight table configure register17 |
| VEPU580_KLUT_WGT18 | 0x10CC | W | 0x00000000 | (RDO) Chroma weight table configure register18 |
| VEPU580_KLUT_WGT19 | 0x10D0 | W | 0x00000000 | (RDO) Chroma weight table configure register19 |
| VEPU580_KLUT_WGT20 | 0x10D4 | W | 0x00000000 | (RDO) Chroma weight table configure register20 |
| VEPU580_KLUT_WGT21 | 0x10D8 | W | 0x00000000 | (RDO) Chroma weight table configure register21 |
| VEPU580_KLUT_WGT22 | 0x10DC | W | 0x00000000 | (RDO) Chroma weight table configure register22 |
| VEPU580_KLUT_WGT23 | 0x10E0 | W | 0x00000000 | (RDO) Chroma weight table configure register23 |
| VEPU580_QNT_BIAS_COMB | 0x1730 | W | 0x00000000 | Quantization Bias for H.264 and HEVC. |
| VEPU580_RDO_WGTA_QP15_COMB | 0x193C | W | 0x00000000 | Weight of group A for HEVC and H.264 RDO mode decision when QP is 15. |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VEPU580_OSD_INV_EN | 0x3000 | W | 0x00000000 | OSD color inverse configuration |
| VEPU580_OSD_INV_THD | 0x3004 | W | 0x00000000 | OSD color inverse threshold |
| VEPU580_OSD_CFG | 0x3008 | W | 0x00000000 | OSD configuration |
| VEPU580_OSD0_LT_POS | 0x3010 | W | 0x00000000 | OSD region0 left-top position |
| VEPU580_OSD0_RB_POS | 0x3014 | W | 0x00000000 | OSD region0 right-bottom position |
| VEPU580_OSD1_LT_POS | 0x3018 | W | 0x00000000 | OSD region1 left-top position |
| VEPU580_OSD1_RB_POS | 0x301C | W | 0x00000000 | OSD region1 right-bottom position |
| VEPU580_OSD2_LT_POS | 0x3020 | W | 0x00000000 | OSD region2 left-top position |
| VEPU580_OSD2_RB_POS | 0x3024 | W | 0x00000000 | OSD region2 right-bottom position |
| VEPU580_OSD3_LT_POS | 0x3028 | W | 0x00000000 | OSD region3 left-top position |
| VEPU580_OSD3_RB_POS | 0x302C | W | 0x00000000 | OSD region3 right-bottom position |
| VEPU580_OSD4_LT_POS | 0x3030 | W | 0x00000000 | OSD region4 left-top position |
| VEPU580_OSD4_RB_POS | 0x3034 | W | 0x00000000 | OSD region4 right-bottom position |
| VEPU580_OSD5_LT_POS | 0x3038 | W | 0x00000000 | OSD region5 left-top position |
| VEPU580_OSD5_RB_POS | 0x303C | W | 0x00000000 | OSD region5 right-bottom position |
| VEPU580_OSD6_LT_POS | 0x3040 | W | 0x00000000 | OSD region6 left-top position |
| VEPU580_OSD6_RB_POS | 0x3044 | W | 0x00000000 | OSD region6 right-bottom position |
| VEPU580_OSD7_LT_POS | 0x3048 | W | 0x00000000 | OSD region7 left-top position |
| VEPU580_OSD7_RB_POS | 0x304C | W | 0x00000000 | OSD region7 right-bottom position |
| VEPU580_ADR_OSD0 | 0x3050 | W | 0x00000000 | Base address of OSD region0 |
| VEPU580_ADR_OSD1 | 0x3054 | W | 0x00000000 | Base address for OSD region1, 16B aligned |
| VEPU580_ADR_OSD2 | 0x3058 | W | 0x00000000 | Base address for OSD region2, 16B aligned |
| VEPU580_ADR_OSD3 | 0x305C | W | 0x00000000 | Base address for OSD region3, 16B aligned |
| VEPU580_ADR_OSD4 | 0x3060 | W | 0x00000000 | Base address for OSD region4, 16B aligned |
| VEPU580_ADR_OSD5 | 0x3064 | W | 0x00000000 | Base address for OSD region5, 16B aligned |
| VEPU580_ADR_OSD6 | 0x3068 | W | 0x00000000 | Base address for OSD region6, 16B aligned |
| VEPU580_ADR_OSD7 | 0x306C | W | 0x00000000 | Base address for OSD region7, 16B aligned |
| VEPU580_OSD_PLT0 | 0x3080 | W | 0x00000000 | User defined OSD palette color0 |
| VEPU580_OSD_PLT1 | 0x3084 | W | 0x00000000 | User defined OSD palette color1 |
| VEPU580_OSD_PLT255 | 0x347C | W | 0x00000000 | OSD palette color255 |
| VEPU580_ST_BSL_L32 | 0x4000 | W | 0x00000000 | Low 32bits of bit stream length for current frame. |
| VEPU580_ST_SSE_BSL | 0x4004 | W | 0x00000000 | High 8 bits of bit stream length for current frame and low 16 bits of encoding distortion (SSE). |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VEPU580_ST_SSE_H32 | 0x4008 | W | 0x00000000 | High 32 bits of encoding distortion (SSE). |
| VEPU580_ST_SSE_QP | 0x400C | W | 0x00000000 | Sum of QP for the encoded frame. |
| VEPU580_ST_SAO | 0x4010 | W | 0x00000000 | Number of CTUs which adjusted by SAO |
| VEPU580_ST_HEAD_BL_L32 | 0x4014 | W | 0x00000000 | Low 32 bits of RDO HeaderBits length. |
| VEPU580_ST_HEAD_RES_BL | 0x4018 | W | 0x00000000 | High 8 bits of RDO HeaderBits length and low 16 bits of RDO ResidualBits length. |
| VEPU580_ST_RES_BL_H24 | 0x401C | W | 0x00000000 | High 24 bits of RDO ResidualBits length. |
| VEPU580_ST_ENC | 0x4020 | W | 0x00000000 | VEPU working status |
| VEPU580_ST_LKT | 0x4024 | W | 0x00000000 | Status of link table mode encoding |
| VEPU580_ST_NADR | 0x4028 | W | 0x00000000 | Address of the processing link table node |
| VEPU580_ST_BSB | 0x402C | W | 0x00000000 | Status of bit stream buffer |
| VEPU580_ST_BUS | 0x4030 | W | 0x00000000 | VEPU bus status |
| VEPU580_ST_SNUM | 0x4034 | W | 0x00000000 | Slice number status. |
| VEPU580_ST_SLEN | 0x4038 | W | 0x00000000 | Status of slice length |
| VEPU580_ST_PNUM_P64 | 0x4100 | W | 0x00000000 | Number of 64x64 inter predicted blocks |
| VEPU580_ST_PNUM_P32 | 0x4104 | W | 0x00000000 | Number of 32x32 inter predicted blocks |
| VEPU580_ST_PNUM_P16 | 0x4108 | W | 0x00000000 | Number of 16x16 inter predicted blocks |
| VEPU580_ST_PNUM_P8 | 0x410C | W | 0x00000000 | Number of 8x8 inter predicted blocks |
| VEPU580_ST_PNUM_I32 | 0x4110 | W | 0x00000000 | Number of 32x32 intra predicted blocks |
| VEPU580_ST_PNUM_I16 | 0x4114 | W | 0x00000000 | Number of 16x16 intra predicted blocks |
| VEPU580_ST_PNUM_I8 | 0x4118 | W | 0x00000000 | Number of 8x8 intra predicted blocks |
| VEPU580_ST_PNUM_I4 | 0x411C | W | 0x00000000 | Number of 4x4 intra predicted blocks |
| VEPU580_ST_CPLX_TMP | 0x4120 | W | 0x00000000 | Temporal complexity(MADP) for current encoding and reference frame |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VEPU580_ST_BNUM_CME | 0x4124 | W | 0x00000000 | Number of CME blocks in frame. H.264: number CME blocks (4 MBs) in 16x64 aligned extended frame, except for the CME blocks configured as force intra. HEVC: number CME blocks (CTU) in 64x64 aligned extended frame, except for the CME blocks configured as force intra. |
| VEPU580_ST_CPLX_SPT | 0x4128 | W | 0x00000000 | Spatial complexity(MADI) for current encoding frame |
| VEPU580_ST_BNUM_B16 | 0x412C | W | 0x00000000 | Number of 16x16 blocks in frame. H.264: number of macro-blocks in encoding frame. HEVC: number of 16x16 blocks in 16x16 aligned extended frame. |
| VEPU580_ST_CPLX_MAX_B16 | 0x4130 | W | 0x00000000 | Number of 16x16 blocks which the value is bigger than sw_aq_thd15. H.264: number of macro-blocks in encoding frame. HEVC: number of 16x16 blocks in 16x16 aligned extended frame. |
| VEPU580_ST_MD_SAD_NUM0 | 0x4134 | W | 0x00000000 | Number of 16x16 blocks with cime orginal sad < md_sad_thd0. |
| VEPU580_ST_MD_SAD_NUM1 | 0x4138 | W | 0x00000000 | Number of 16x16 blocks with md_sad_thd0 <= cime_orginal_sad < md_sad_thd1. |
| VEPU580_ST_MD_SAD_NUM2 | 0x413C | W | 0x00000000 | Number of 16x16 blocks with md_sad_thd1 <= cime_orginal_sad < md_sad_thd2. |
| VEPU580_ST_MD_SAD_NUM3 | 0x4140 | W | 0x00000000 | Number of 16x16 blocks with md_sad_thd2 <= cime_orginal_sad. |
| VEPU580_ST_MADI_NUM0 | 0x4144 | W | 0x00000000 | Number of 16x16 blocks with madi < madi_thd0. |
| VEPU580_ST_MADI_NUM1 | 0x4148 | W | 0x00000000 | Number of 16x16 blocks with madi_thd0 <= madi < madi_thd1. |
| VEPU580_ST_MADI_NUM2 | 0x414C | W | 0x00000000 | Number of 16x16 blocks with madi_thd1 <= madi < madi_thd2. |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VEPU580_ST_MADI_NUM3 | 0x4150 | W | 0x00000000 | Number of 16x16 blocks with madi_thd2 <= madi. |
| VEPU580_ST_B8_QP0 | 0x4200 | W | 0x00000000 | Number of block8x8s with QP=0 |
| VEPU580_ST_B8_QP1 | 0x4204 | W | 0x00000000 | Number of block8x8s with QP=1 |
| VEPU580_ST_B8_QP2 | 0x4208 | W | 0x00000000 | Number of block8x8s with QP=2 |
| VEPU580_ST_B8_QP3 | 0x420C | W | 0x00000000 | Number of block8x8s with QP=3 |
| VEPU580_ST_B8_QP4 | 0x4210 | W | 0x00000000 | Number of block8x8s with QP=4 |
| VEPU580_ST_B8_QP5 | 0x4214 | W | 0x00000000 | Number of block8x8s with QP=5 |
| VEPU580_ST_B8_QP6 | 0x4218 | W | 0x00000000 | Number of block8x8s with QP=6 |
| VEPU580_ST_B8_QP7 | 0x421C | W | 0x00000000 | Number of block8x8s with QP=7 |
| VEPU580_ST_B8_QP8 | 0x4220 | W | 0x00000000 | Number of block8x8s with QP=8 |
| VEPU580_ST_B8_QP9 | 0x4224 | W | 0x00000000 | Number of block8x8s with QP=9 |
| VEPU580_ST_B8_QP10 | 0x4228 | W | 0x00000000 | Number of block8x8s with QP=10 |
| VEPU580_ST_B8_QP11 | 0x422C | W | 0x00000000 | Number of block8x8s with QP=11 |
| VEPU580_ST_B8_QP12 | 0x4230 | W | 0x00000000 | Number of block8x8s with QP=12 |
| VEPU580_ST_B8_QP13 | 0x4234 | W | 0x00000000 | Number of block8x8s with QP=13 |
| VEPU580_ST_B8_QP14 | 0x4238 | W | 0x00000000 | Number of block8x8s with QP=14 |
| VEPU580_ST_B8_QP15 | 0x423C | W | 0x00000000 | Number of block8x8s with QP=15 |
| VEPU580_ST_B8_QP16 | 0x4240 | W | 0x00000000 | Number of block8x8s with QP=16 |
| VEPU580_ST_B8_QP17 | 0x4244 | W | 0x00000000 | Number of block8x8s with QP=17 |
| VEPU580_ST_B8_QP18 | 0x4248 | W | 0x00000000 | Number of block8x8s with QP=18 |
| VEPU580_ST_B8_QP19 | 0x424C | W | 0x00000000 | Number of block8x8s with QP=19 |
| VEPU580_ST_B8_QP20 | 0x4250 | W | 0x00000000 | Number of block8x8s with QP=20 |
| VEPU580_ST_B8_QP21 | 0x4254 | W | 0x00000000 | Number of block8x8s with QP=21 |
| VEPU580_ST_B8_QP22 | 0x4258 | W | 0x00000000 | Number of block8x8s with QP=22 |
| VEPU580_ST_B8_QP23 | 0x425C | W | 0x00000000 | Number of block8x8s with QP=23 |
| VEPU580_ST_B8_QP24 | 0x4260 | W | 0x00000000 | Number of block8x8s with QP=24 |
| VEPU580_ST_B8_QP25 | 0x4264 | W | 0x00000000 | Number of block8x8s with QP=25 |
| VEPU580_ST_B8_QP26 | 0x4268 | W | 0x00000000 | Number of block8x8s with QP=26 |
| VEPU580_ST_B8_QP27 | 0x426C | W | 0x00000000 | Number of block8x8s with QP=27 |
| VEPU580_ST_B8_QP28 | 0x4270 | W | 0x00000000 | Number of block8x8s with QP=28 |
| VEPU580_ST_B8_QP29 | 0x4274 | W | 0x00000000 | Number of block8x8s with QP=29 |
| VEPU580_ST_B8_QP30 | 0x4278 | W | 0x00000000 | Number of block8x8s with QP=30 |
| VEPU580_ST_B8_QP31 | 0x427C | W | 0x00000000 | Number of block8x8s with QP=31 |
| VEPU580_ST_B8_QP32 | 0x4280 | W | 0x00000000 | Number of block8x8s with QP=32 |
| VEPU580_ST_B8_QP33 | 0x4284 | W | 0x00000000 | Number of block8x8s with QP=33 |
| VEPU580_ST_B8_QP34 | 0x4288 | W | 0x00000000 | Number of block8x8s with QP=34 |
| VEPU580_ST_B8_QP35 | 0x428C | W | 0x00000000 | Number of block8x8s with QP=35 |
| VEPU580_ST_B8_QP36 | 0x4290 | W | 0x00000000 | Number of block8x8s with QP=36 |
| VEPU580_ST_B8_QP37 | 0x4294 | W | 0x00000000 | Number of block8x8s with QP=37 |
| VEPU580_ST_B8_QP38 | 0x4298 | W | 0x00000000 | Number of block8x8s with QP=38 |
| VEPU580_ST_B8_QP39 | 0x429C | W | 0x00000000 | Number of block8x8s with QP=39 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VEPU580_ST_B8_QP40 | 0x42A0 | W | 0x00000000 | Number of block8x8s with QP=40 |
| VEPU580_ST_B8_QP41 | 0x42A4 | W | 0x00000000 | Number of block8x8s with QP=41 |
| VEPU580_ST_B8_QP42 | 0x42A8 | W | 0x00000000 | Number of block8x8s with QP=42 |
| VEPU580_ST_B8_QP43 | 0x42AC | W | 0x00000000 | Number of block8x8s with QP=43 |
| VEPU580_ST_B8_QP44 | 0x42B0 | W | 0x00000000 | Number of block8x8s with QP=44 |
| VEPU580_ST_B8_QP45 | 0x42B4 | W | 0x00000000 | Number of block8x8s with QP=45 |
| VEPU580_ST_B8_QP46 | 0x42B8 | W | 0x00000000 | Number of block8x8s with QP=46 |
| VEPU580_ST_B8_QP47 | 0x42BC | W | 0x00000000 | Number of block8x8s with QP=47 |
| VEPU580_ST_B8_QP48 | 0x42C0 | W | 0x00000000 | Number of block8x8s with QP=48 |
| VEPU580_ST_B8_QP49 | 0x42C4 | W | 0x00000000 | Number of block8x8s with QP=49 |
| VEPU580_ST_B8_QP50 | 0x42C8 | W | 0x00000000 | Number of block8x8s with QP=50 |
| VEPU580_ST_B8_QP51 | 0x42CC | W | 0x00000000 | Number of block8x8s with QP=51 |
| VEPU580_ST_SLI_NUM | 0x5028 | W | 0x00000000 | Number of slices |
| VEPU580_ST_LKT_ERR | 0x502C | W | 0x00000000 | Link Table error status |
| VEPU580_MMU0_ADDR | 0xF000 | W | 0x00000000 | Page table address for AXI0 MMU |
| VEPU580_MMU0_ST | 0xF004 | W | 0x00000000 | Status of the MMU for AXI0 |
| VEPU580_MMU0_CMD | 0xF008 | W | 0x00000000 | MMU command for AXI0 |
| VEPU580_MMU0_PFA | 0xF00C | W | 0x00000000 | Address of the last page fault for MMU0 |
| VEPU580_MMU0_ZAP | 0xF010 | W | 0x00000000 | Zap address for MMU0 |
| VEPU580_MMU0_ERR | 0xF014 | W | 0x00000000 | MMU error |
| VEPU580_MMU0_INT_CLR | 0xF018 | W | 0x00000000 | Interrupt clear for MMU0 |
| VEPU580_MMU0_INT_MSK | 0xF01C | W | 0x00000000 | Interrupt mask for MMU0 |
| VEPU580_MMU0_INT_STA | 0xF020 | W | 0x00000000 | Interrupt status for MMU0 |
| VEPU580_MMU0_ACKG | 0xF024 | W | 0x00000001 | Auto clock gating for MMU0 |
| VEPU580_MMU1_ADDR | 0xF040 | W | 0x00000000 | Page table address for AXI1 MMU |
| VEPU580_MMU1_ST | 0xF044 | W | 0x00000000 | Status of the MMU for AXI1 |
| VEPU580_MMU1_CMD | 0xF048 | W | 0x00000000 | MMU command for AXI1 |
| VEPU580_MMU1_PFA | 0xF04C | W | 0x00000000 | Address of the last page fault for MMU1 |
| VEPU580_MMU1_ZAP | 0xF050 | W | 0x00000000 | Zap address for MMU1 |
| VEPU580_MMU1_ERR | 0xF054 | W | 0x00000000 | MMU error |
| VEPU580_MMU1_INT_CLR | 0xF058 | W | 0x00000000 | Interrupt clear for MMU1 |
| VEPU580_MMU1_INT_MSK | 0xF05C | W | 0x00000000 | Interrupt mask for MMU1 |
| VEPU580_MMU1_INT_STA | 0xF060 | W | 0x00000000 | Interrupt status for MMU1 |
| VEPU580_MMU1_ACKG | 0xF064 | W | 0x00000001 | Auto clock gating for MMU1 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

## 5.5.29 VEPU580 Detail Registers Description

**VEPU580_VERSION**

Rockchip Confidential

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x50 | ip_id<br>VEPU ID. |
| 23 | RO | 0x0 | reserved |
| 22:21 | RW | 0x3 | fbc_cap<br>FBC capability.<br>2'h0: No FBC<br>2'h3: Support AFBC for video source and FBC for reconstructed picture<br>Others: Reserved |
| 20 | RW | 0x0 | bfrm_cap<br>B frame encoding capability. 1 means VEPU supports B frame encoding while 0 means not. |
| 19:18 | RW | 0x0 | filtr_cap<br>Pre-process filter capability<br>2'h0: Basic pre-process filter<br>2'h3: No pre-process filter<br>Others: Reserved |
| 17:16 | RW | 0x0 | osd_cap<br>OSD capability.<br>2'h0: 8-area OSD with 256-color palette<br>2'h3: No OSD<br>Others: Reserved |
| 15:12 | RW | 0x0 | res_cap<br>Max resolution<br>4'h0: 4096x2304<br>4'h1: 1920x1088<br>4'h2: 8192x8192<br>4'h3: 16384x16384<br>Others: Reserved |
| 11:10 | RO | 0x0 | reserved |
| 9 | RW | 0x1 | hevc_cap<br>HEVC encoding capability. 1 means VEPU supports HEVC encoding while 0 means not |
| 8 | RW | 0x1 | h264_cap<br>H.264 encoding capability. 1 means VEPU supports H.264 encoding, while 0 means not. |
| 7:0 | RW | 0x0b | sub_ver<br>VEPU sub-version. |

**VEPU580_ENC_CLR**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | force_clr<br>Force clear. Clear all sub-modules besides Configuration Registers and AHB Data Path. |
| 0 | RW | 0x0 | safe_clr<br>Safe clear. It only clears DMA module to confirm AXI transaction integrity.<br>1'h0: Safe clear is not performing.<br>1'h1: Safe clear is performing. |

**VEPU580_INT_EN**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9 | RW | 0x0 | lkt_err_int_en |
| 8 | RW | 0x0 | wdg_en<br>Watch dog(time out) interrupt enable. |
| 7 | RW | 0x0 | rbus_err_en<br>AXI read channel error interrupt enable. |
| 6 | RW | 0x0 | wbus_err_en<br>AXI write channel error interrupt enable. |
| 5 | RW | 0x0 | brsp_otsd_en<br>AXI write response outstanding overflow interrupt enable. |
| 4 | RW | 0x0 | bsf_oflw_en<br>Bit stream buffer overflow enable. |
| 3 | RW | 0x0 | slc_done_en<br>One slice encoding finish interrupt enable. |
| 2 | RW | 0x0 | sclr_done_en<br>Safe clear finish interrupt enable. |
| 1 | RW | 0x0 | lkt_node_done_en<br>Link table one node finish interrupt enable. |
| 0 | RW | 0x0 | enc_done_en<br>One frame encoding finish interrupt enable. |

**VEPU580_INT_MSK**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9 | RW | 0x0 | lkt_err_msk |
| 8 | RW | 0x0 | wdg_msk<br>Watch dog(time out) interrupt mask. |
| 7 | RW | 0x0 | rbus_err_msk<br>AXI read channel error interrupt mask. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | wbus_err_msk<br>AXI write channel error interrupt mask. |
| 5 | RW | 0x0 | brsp_otsd_msk<br>AXI write response outstanding overflow interrupt mask. |
| 4 | RW | 0x0 | bsf_oflw_msk<br>Bit stream buffer overflow mask. |
| 3 | RW | 0x0 | slc_done_msk<br>One slice encoding finish interrupt mask. |
| 2 | RW | 0x0 | sclr_done_msk<br>Safe clear finish interrupt mask. |
| 1 | RW | 0x0 | lkt_node_done_msk<br>Link table one node finish interrupt mask. |
| 0 | RW | 0x0 | enc_done_msk<br>One frame encoding finish interrupt mask. |

**VEPU580_INT_CLR**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9 | RW | 0x0 | lkt_err_clr |
| 8 | RW | 0x0 | wdg_clr<br>Watch dog(time out) interrupt clear. |
| 7 | RW | 0x0 | rbus_err_clr<br>AXI read channel error interrupt clear. |
| 6 | RW | 0x0 | wbus_err_clr<br>AXI write channel error interrupt clear. |
| 5 | RW | 0x0 | brsp_otsd_clr<br>AXI write response outstanding overflow interrupt clear. |
| 4 | RW | 0x0 | bsf_oflw_clr<br>Bit stream buffer overflow clear. |
| 3 | RW | 0x0 | slc_done_clr<br>One slice encoding finish interrupt clear. |
| 2 | RW | 0x0 | sclr_done_clr<br>Safe clear finish interrupt clear. |
| 1 | RW | 0x0 | lkt_node_done_clr<br>Link table one node finish interrupt clear. |
| 0 | RW | 0x0 | enc_done_clr<br>One frame encoding finish interrupt clear. |

**VEPU580_INT_STA**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RW | 0x0 | lkt_err_sta |
| 8 | RW | 0x0 | wdg_sta<br>Watch dog(time out) interrupt status. |
| 7 | RW | 0x0 | rbus_err_sta<br>AXI read channel error interrupt status. |
| 6 | RW | 0x0 | wbus_err_sta<br>AXI write channel error interrupt status. |
| 5 | RW | 0x0 | brsp_otsd_sta<br>AXI write response outstanding overflow interrupt status. |
| 4 | RW | 0x0 | bsf_oflw_sta<br>Bit stream buffer overflow status. |
| 3 | RW | 0x0 | slc_done_sta<br>One slice encoding finish interrupt status. |
| 2 | RW | 0x0 | sclr_done_sta<br>Safe clear finish interrupt status. |
| 1 | RW | 0x0 | lkt_node_done_sta<br>Link table one node finish interrupt status. |
| 0 | RW | 0x0 | enc_done_sta<br>One frame encoding finish interrupt status. |

**VEPU580_DBUS_ENDIAN**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RW | 0x0 | rec_nfbc_bus_edin<br>Data swap for reference picture channel without fbc.<br>[2]: Swap 32 bits in 64 bits<br>[1]: Swap 16 bits in 32 bits<br>[0]: Swap 8 bits in 16 bits |
| 28 | RW | 0x0 | ebufw_bus_ordr<br>Swap the position of 64 bits in 128 bits for external linebuffer. |
| 27 | RW | 0x0 | afbc_bsize<br>AFBC video source loading burst size.<br>1'h0: 32 bytes<br>1'h1: 64 bytes |
| 26:23 | RW | 0x0 | lktw_bus_edin<br>Data swap for link table write channel.<br>[3]: Swap 64 bits in 128 bits<br>[2]: Swap 32 bits in 64 bits<br>[1]: Swap 16 bits in 32 bits<br>[0]: Swap 8 bits in 16 bits |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 22:19 | RW | 0x0 | roir_bus_edin<br>Data swap for ROI configuration read channel.<br>[3]: Swap 64 bits in 128 bits<br>[2]: Swap 32 bits in 64 bits<br>[1]: Swap 16 bits in 32 bits<br>[0]: Swap 8 bits in 16 bits |
| 18:15 | RW | 0x0 | lktr_bus_edin<br>Data swap for link table read channel.<br>[3]: Swap 64 bits in 128 bits<br>[2]: Swap 32 bits in 64 bits<br>[1]: Swap 16 bits in 32 bits<br>[0]: Swap 8 bits in 16 bits |
| 14:12 | RW | 0x0 | bsw_bus_edin<br>Data swap for bis stream write channel.<br>[2]: Swap 32 bits in 64 bits<br>[1]: Swap 16 bits in 32 bits<br>[0]: Swap 8 bits in 16 bits |
| 11:8 | RW | 0x0 | meiw_bus_edin<br>Data swap for ME information write channel.<br>[3]: Swap 64 bits in 128 bits<br>[2]: Swap 32 bits in 64 bits<br>[1]: Swap 16 bits in 32 bits<br>[0]: Swap 8 bits in 16 bits |
| 7:4 | RW | 0x0 | src_bus_edin<br>Data swap for video source loading channel.<br>[3]: Swap 64 bits in 128 bits<br>[2]: Swap 32 bits in 64 bits<br>[1]: Swap 16 bits in 32 bits<br>[0]: Swap 8 bits in 16 bits |
| 3 | RW | 0x0 | rfpw_bus_ordr<br>Swap the position of 64 bits in 128 bits for reference picture. |
| 2 | RW | 0x0 | dspw_bus_ordr<br>Swap the position of 64 bits in 128 bits for down-sampled picture. |
| 1 | RW | 0x0 | cmvw_bus_ordr<br>Swap the position of 64 bits in 128 bits for co-located Mv(HEVC only). |
| 0 | RW | 0x0 | lpfw_bus_ordr<br>Swap the position of 64 bits in 128 bits for loop-filter write-back data between tiles(HEVC only). |

**VEPU580_DBUS_CFG**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:16 | RW | 0x00 | axi_brsp_cke<br>AXI write response channel check enable.<br>[7]: Lpf write response check enable.<br>[6]: Reconstructed picture write response check enable.<br>[5]: ME information write response check enable.<br>[4]: CTU information write response check enable.<br>[3]: Down-sampled picture write response check enable.<br>[2]: Bit stream write response check enable.<br>[1]: Link table mode write reponse check enable.<br>[0]: External line buffer write response check enable. |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | dspr_otsd<br>Down sampled reference picture read outstanding enable.<br>1'h0: No outstanding<br>1'h1: Outstanding read, which improves data transaction efficiency, but core clock frequency should not lower than bus clock frequency. |
| 6:0 | RO | 0x00 | reserved |

**VEPU580_ENC_WDG**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | rfp_load_thd<br>Reference picture loading timeout threshold.<br>8'h0: No time limit<br>8'hx: x*256 core clock cycles |
| 23:0 | RW | 0x000000 | vs_load_thd<br>Video source loading timeout threshold.<br>24'h0: No time limit<br>24'hx: x*1024 core clock cycles |

**VEPU580_CORE_ID**

Address: Operational Base + offset (0x005C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1:0 | RW | 0x0 | core_id<br>ID idx of current encoder id for linktable mode.<br>2'b01: core0;<br>2'b10: core1; |

**VEPU580_LKT_BASE_ADDR**

Address: Operational Base + offset (0x0070)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | lkt_addr<br>High 28 bits of the address for the first node in link table. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RO | 0x0 | reserved |

**VEPU580_NODE_ID**

Address: Operational Base + offset (0x0100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2 | RW | 0x0 | node_int<br>Node interrupt enable (only for link table node configuration). |
| 1:0 | RW | 0x0 | node_core_id<br>Core id idx of current linktable node. |

**VEPU580_NODE_ADR_FCFG**

Address: Operational Base + offset (0x0104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | lkt_addr_pcfg<br>High 28 bits of the address of picture configuration for the current frame. |
| 3:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | pcfg_rd_en<br>Picture configuration read enable of current frame. |

**VEPU580_NODE_ADR_RC**

Address: Operational Base + offset (0x0108)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | lkt_addr_rc_cfg<br>High 28 bits of the address of parameter configuration for the current frame. |
| 3:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | rc_cfg_rd_en<br>Parameter configuration read enable of current frame. |

**VEPU580_NODE_ADR_PAR**

Address: Operational Base + offset (0x010C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | lkt_addr_par_cfg<br>High 28 bits of the address of parameter configuration for the current frame. |
| 3:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | par_cfg_rd_en<br>Parameter configuration read enable of current frame. |

**VEPU580_NODE_ADR_SA**

Address: Operational Base + offset (0x0110)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | lkt_addr_sqi_cfg<br>High 28 bits of the address of AFM configuration for the current frame. |
| 3:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | sqi_cfg_rd_en<br>AFM configuration read enable of current frame. |

**VEPU580_NODE_ADR_SCAL**

Address: Operational Base + offset (0x0114)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | lkt_addr_scal_cfg<br>High 28 bits of the address of scalist configuration for the current frame. |
| 3:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | scal_cfg_rd_en<br>Scalist configuration read enable of current frame. |

**VEPU580_NODE_ADR_OSD**

Address: Operational Base + offset (0x0118)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | lkt_addr_pp_cfg<br>High 28 bits of the address of pre-process configuration for the current frame. |
| 3:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | pp_cfg_rd_en<br>Pre-process configuration read enable of current frame. |

**VEPU580_NODE_ADR_INF**

Address: Operational Base + offset (0x011C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | lkt_addr_st<br>High 28 bits of the address of output state for the current frame. |
| 3:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | st_out_en<br>Output state write-back enable of current frame. |

**VEPU580_NODE_ADR_NXT**

Address: Operational Base + offset (0x0120)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | lkt_addr_nxt<br>High 28 bits of the address of next node. |
| 3:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | nxt_node_vld<br>Lkt_addr_nxt is a valid address. |

Rockchip Confidential

**VEPU580_ADR_SRC0**

Address: Operational Base + offset (0x0280)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | adr_src0<br>Base address of the 1st storage area for video source, based on byte.<br>ARGB8888, BGR888, RGB565, YUYV422 and UYUV422 have only one storage area, while adr_src0 is configured as the base address of video source frame buffer.<br>YUV422/420 semi-planar have 2 storage area, while adr_src0 is configured as the base address of Y frame buffer.<br>YUV422/420 planar have 3 storage area, while adr_src0 is configured as the base address of Y frame buffer.<br>Note that if the video source is compressed by AFBC, adr_src0 is configured as the base address of header buffer, and it is 16-byte aligned. |

**VEPU580_ADR_SRC1**

Address: Operational Base + offset (0x0284)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | adr_src1<br>Base address of the 2nd storage area for video source.<br>ARGB8888, BGR888, RGB565, YUYV422 and UYUV422 have only one storage area, while adr_src1 is reserved.<br>YUV422/420 semi-planar have 2 storage area, while adr_src1 is configured as the base address of CHROMA frame buffer.<br>YUV422/420 planar have 3 storage area, while adr_src1 is configured as the base address of U frame buffer.<br>Note that if the video source is compressed by AFBC, adr_src1 is configured as the base address of body buffer. |

**VEPU580_ADR_SRC2**

Address: Operational Base + offset (0x0288)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | adr_src2<br>Base address of V frame buffer when video source is uncompress and color format is YUV422/420 planar. |

**VEPU580_ADR_RECW_H**

Address: Operational Base + offset (0x028C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RW | 0x00000 | rfpw_h_addr<br>High 20 bits of the header_block base address for compressed reference frame write. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:0 | RO | 0x000 | reserved |

**VEPU580_ADR_RFPW_B**

Address: Operational Base + offset (0x0290)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RW | 0x00000 | rfpw_b_addr<br>High 20 bits of the body_block base address for compressed reference frame write. |
| 11:0 | RO | 0x000 | reserved |

**VEPU580_ADR_RFPR_H**

Address: Operational Base + offset (0x0294)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RW | 0x00000 | rfpr_h_addr<br>High 20 bits of the header_block base address for compressed reference frame read. |
| 11:0 | RO | 0x000 | reserved |

**VEPU580_ADR_RFPR_B**

Address: Operational Base + offset (0x0298)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RW | 0x00000 | rfpr_b_addr<br>High 20 bits of the body_block base address for compressed reference frame read. |
| 11:0 | RO | 0x000 | reserved |

**VEPU580_ADR_CMVW**

Address: Operational Base + offset (0x029C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RW | 0x000000 | cmvw_addr<br>High 22 bits of base address for col-located Mv write, HEVC only. |
| 9:0 | RO | 0x000 | reserved |

**VEPU580_ADR_CMVR**

Address: Operational Base + offset (0x02A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RW | 0x000000 | cmvr_addr<br>High 22 bits of base address for col-located Mv read, HEVC only. |
| 9:0 | RO | 0x000 | reserved |

**VEPU580_ADR_DSPW**

Address: Operational Base + offset (0x02A4)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RW | 0x000000 | dspw_addr<br>High 22 bits of base address for down-sampled reference frame write. |
| 9:0 | RO | 0x000 | reserved |

**VEPU580_ADR_DSPR**

Address: Operational Base + offset (0x02A8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RW | 0x000000 | dspr_addr<br>High 22 bits of base address for down-sampled reference frame read. |
| 9:0 | RO | 0x000 | reserved |

**VEPU580_ADR_MEIW**

Address: Operational Base + offset (0x02AC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RW | 0x000000 | meiw_addr<br>High 22 bits of base address for ME information write. |
| 9:0 | RO | 0x000 | reserved |

**VEPU580_ADR_BSBT**

Address: Operational Base + offset (0x02B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RW | 0x0000000 | bsbt_addr<br>High 25 bits of the top address of bit stream buffer. |
| 6:0 | RO | 0x00 | reserved |

**VEPU580_ADR_BSBB**

Address: Operational Base + offset (0x02B4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RW | 0x0000000 | bsbb_addr<br>High 25 bits of the bottom address of bit stream buffer. |
| 6:0 | RO | 0x00 | reserved |

**VEPU580_ADR_BSBR**

Address: Operational Base + offset (0x02B8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RW | 0x0000000 | bsbr_addr<br>Read address of bit stream buffer, 128B aligned. VEPU will pause when write address meets read address and then send an interrupt. SW should move some data out from bit stream buffer and change this register accordingly. After that VEPU will continue processing automatically. |
| 6:0 | RO | 0x00 | reserved |

Rockchip Confidencial

**VEPU580_ADR_BSBS**

Address: Operational Base + offset (0x02BC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | adr_bsbs<br>Start address of bit stream buffer. VEPU begins to write bit stream from this address and increase address automatically. Note that the VEPU's real-time write address is marked in BSB_STUS. |

**VEPU580_ADR_TILEW**

Address: Operational Base + offset (0x02C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RW | 0x000000 | lpfw_addr<br>High 22 bits of base address for loop-filter write-back data between tiles, hevc only. |
| 9:0 | RO | 0x000 | reserved |

**VEPU580_ADR_TILER**

Address: Operational Base + offset (0x02C4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RW | 0x000000 | lpfr_addr<br>High 22 bits of base address for loop-filter read data between tiles, hevc only. |
| 9:0 | RO | 0x000 | reserved |

**VEPU580_ADR_ROI_BASE**

Address: Operational Base + offset (0x02C8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | roi_addr<br>High 28 bits of base address for ROI configuration. |
| 3:0 | RO | 0x0 | reserved |

**VEPU580_ADR_ROI_QP**

Address: Operational Base + offset (0x02CC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | roi_qp_addr<br>High 28 bits of base address for ROI qp configuration. |
| 3:0 | RO | 0x0 | reserved |

**VEPU580_ADR_ROI_AMV**

Address: Operational Base + offset (0x02D0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | qoi_amv_addr<br>High 28 bits of base address for ROI amv configuration. |
| 3:0 | RO | 0x0 | reserved |

Rockchip Confidencial

**VEPU580_ADR_ROI_FMV**

Address: Operational Base + offset (0x02D4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | qoi_mv_addr<br>High 28 bits of base address for ROI mv configuration. |
| 3:0 | RO | 0x0 | reserved |

**VEPU580_ADR_ELBT**

Address: Operational Base + offset (0x02D8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RW | 0x000000 | ebuft_addr<br>High 24 bits of the top address for external line buffer. |
| 7:0 | RO | 0x00 | reserved |

**VEPU580_ADR_ELBB**

Address: Operational Base + offset (0x02DC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RW | 0x000000 | ebufb_addr<br>High 24 bits of the bottom address for external line buffer. |
| 7:0 | RO | 0x00 | reserved |

**VEPU580_CMN_CFG**

Address: Operational Base + offset (0x0300)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | rec_fbc_dis<br>Recon data fbc disable. |
| 30 | RW | 0x0 | slen_fifo<br>Slice length fifo enable. |
| 29:24 | RO | 0x00 | reserved |
| 23:19 | RW | 0x00 | log2_ctu_num<br>Logarithm of bit width to express ctu number in current picture, HEVC only. |
| 18:14 | RW | 0x00 | num_pic_tot_cur<br>NumPicTotalCurr for HEVC reference picture list modification. |
| 13:8 | RW | 0x00 | pic_qp<br>QP value for current frame encoding. |
| 7:5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | bs_scp<br>Output start code prefix. |
| 3 | RW | 0x0 | mei_stor<br>Output ME(motion estimation) information. |
| 2 | RW | 0x0 | cur_frm_ref<br>Current frame should be referenced in future. |
| 1 | RW | 0x0 | roi_en<br>ROI(region of interest) encoding enable. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | enc_stnd<br>Video standard.<br>1'h0: H.264 encoding<br>1'h1: HEVC encoding |

**VEPU580_ENC_RSL**

Address: Operational Base + offset (0x0310)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:27 | RO | 0x00 | reserved |
| 26:16 | RW | 0x000 | pic_hd8_m1<br>Ceil(encoding picture height/8) -1 |
| 15:11 | RO | 0x00 | reserved |
| 10:0 | RW | 0x000 | pic_wd8_m1<br>Ceil(encoding picture width/8) -1 |

**VEPU580_SRC_EXT**

Address: Operational Base + offset (0x0314)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:16 | RW | 0x00 | pic_hfill<br>Filling pixels to keep (encoding) picture height is 8 pixels aligned for HEVC and 16 pixels aligned for H.264. |
| 15:6 | RO | 0x000 | reserved |
| 5:0 | RW | 0x00 | pic_wfill<br>Filling pixels to keep (encoding) picture width is 8 pixels aligned for HEVC and 16 pixels aligned for H.264. |

**VEPU580_SRC_FMT**

Address: Operational Base + offset (0x0318)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RW | 0x0 | out_fmt<br>The color format of output from preprocess.<br>1'h0: YUV400;<br>1'h1: YUV420; |
| 6 | RW | 0x0 | src_range<br>Video source clip (low active).<br>1'h0: [16:235] for luma and [16:240] for chroma.<br>1'h1: [0:255] for both luma and chroma. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5:2 | RW | 0x0 | src_cfmt<br>Video source color format.<br>4'h0: BGRA8888<br>4'h1: RGB888<br>4'h2: RGB565<br>4'h4: YUV422SP<br>4'h5: YUV422P<br>4'h6: YUV420SP<br>4'h7: YUV420P<br>4'h8: YUYV422<br>4'h9: UYVY422<br>4'ha: YUV400<br>4'hc: YUV444SP<br>4'hd: YUV444P<br>Others: Reserved |
| 1 | RW | 0x0 | rbuv_swap<br>Swap the position of R and B for BGRA8888, RGB888, RGB 656 format; Swap the position of U and V for YUV422-SP, YUV420-SP, YUYV422 and UYUV422 format.<br>1'h0: RGB or YUYV or UYVY.<br>1'h1: BGR or YVYU or VYUY. |
| 0 | RW | 0x0 | alpha_swap<br>Swap the position of alpha and RGB for ARBG8888.<br>1'h0: BGRA8888 or RGBA8888.<br>1'h1: ABGR8888 or ARGB8888. |

**VEPU580_SRC_UDFY**

Address: Operational Base + offset (0x031C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:27 | RO | 0x00 | reserved |
| 26:18 | RW | 0x000 | csc_wgt_r2y<br>Weight of RED in RGB to Y conversion formula. |
| 17:9 | RW | 0x000 | csc_wgt_g2y<br>Weight of GREEN in RGB to Y conversion formula. |
| 8:0 | RW | 0x000 | csc_wgt_b2y<br>Weight of BLUE in RGB to Y conversion formula. |

**VEPU580_SRC_UDFU**

Address: Operational Base + offset (0x0320)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:27 | RO | 0x00 | reserved |
| 26:18 | RW | 0x000 | csc_wgt_r2u<br>Weight of RED in RGB to U conversion formula. |
| 17:9 | RW | 0x000 | csc_wgt_g2u<br>Weight of GREEN in RGB to U conversion formula. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8:0 | RW | 0x000 | csc_wgt_b2u<br>Weight of BLUE in RGB to U conversion formula. |

**VEPU580_SRC_UDFV**

Address: Operational Base + offset (0x0324)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:27 | RO | 0x00 | reserved |
| 26:18 | RW | 0x000 | csc_wgt_r2v<br>Weight of RED in RGB to V conversion formula. |
| 17:9 | RW | 0x000 | csc_wgt_g2v<br>Weight of GREEN in RGB to V conversion formula. |
| 8:0 | RW | 0x000 | csc_wgt_b2v<br>Weight of BLUE in RGB to V conversion formula. |

**VEPU580_SRC_UDFO**

Address: Operational Base + offset (0x0328)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x000 | reserved |
| 20:16 | RW | 0x00 | csc_ofst_y<br>Offset of RGB to Y conversion formula. |
| 15:8 | RW | 0x00 | csc_ofst_u<br>Offset of RGB to U conversion formula. |
| 7:0 | RW | 0x00 | csc_ofst_v<br>Offset of RGB to V conversion formula. |

**VEPU580_SRC_PROC**

Address: Operational Base + offset (0x032C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |
| 30 | RW | 0x0 | afbcd_en<br>AFBC decompress enable (for AFBC format video source). |
| 29 | RW | 0x0 | txa_en<br>Video source texture analysis enable. |
| 28:27 | RW | 0x0 | src_rot<br>Video source rotation mode.<br>2'h0: 0 degree<br>2'h1: Clockwise 90 degree<br>2'h2: Clockwise 180 degree<br>2'h3: Clockwise 270 degree |
| 26 | RW | 0x0 | src_mirr<br>Video source mirror mode enable. |
| 25:0 | RO | 0x0000000 | reserved |

**VEPU580_SRC_OFST**

Address: Operational Base + offset (0x0330)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | pic_ofst_y<br>Horizontal offset for encoding picture. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | pic_ofst_x<br>Vertical offset for encoding picture. |

**VEPU580_SRC_STRD0**

Address: Operational Base + offset (0x0334)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16:0 | RW | 0x00000 | src_strd0<br>Video source stride0, based on pixel (byte). Note that if the video format is YUYV/UYVY/RGB/ARGB, src_strd0 is the only one component stride, if the video format is YUV420P/YUV420SP/YUV422P/YUV422SP, src_strd0 is the LUMA component stride.<br>Note that if the video source is compressed by AFBC, src_strd0 is the header stride and it is 16-byte aligned. |

**VEPU580_SRC_STRD1**

Address: Operational Base + offset (0x0338)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | src_strd1<br>CHROMA stride of video source, only for YUV format. Note that U and V stride must be the same when color format is YUV planar. |

**VEPU580_RC_CFG**

Address: Operational Base + offset (0x0350)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RW | 0x00000 | rc_ctu_num<br>RC adjustment intervals, base on CTU number. |
| 11:3 | RO | 0x000 | reserved |
| 2 | RW | 0x0 | aq_mode<br>Mode of aq_delta calculation for CU32 and CU64.<br>1'b0: aq_delta of CU32/CU64 is calculated by corresponding MADI32/64;<br>1'b1: aq_delta of CU32/CU64 is calculated by corresponding 4/16 CU16 qp_deltas. |
| 1 | RW | 0x0 | aq_en<br>Adaptive quantization enable. |
| 0 | RW | 0x0 | rc_en<br>Rate control enable. |

Rockchip Confidential

**VEPU580_RC_QP**

Address: Operational Base + offset (0x0354)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RW | 0x00 | rc_min_qp<br>Min QP for rate control and AQ mode. |
| 25:20 | RW | 0x00 | rc_max_qp<br>Max QP for rate control and AQ mode. |
| 19:16 | RW | 0x0 | rc_qp_range<br>QP adjust range(delta_qp) in rate control. Delta_qp is constrained between -rc_qp_range to rc_qp_range. |
| 15:0 | RO | 0x0000 | reserved |

**VEPU580_RC_TGT**

Address: Operational Base + offset (0x0358)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | ctu_ebit<br>Target bit num for one 64x64 CTU(for HEVC) or one 16x16 MB(for H.264), with 1/16 precision. |

**VEPU580_SLI_SPLT**

Address: Operational Base + offset (0x0360)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |
| 30:16 | RW | 0x0000 | sli_max_num_m1<br>Max slice num in one frame. |
| 15 | RW | 0x0 | sli_flsh<br>Slice flush. Flush all the bit stream after each slice finished. |
| 14:3 | RO | 0x000 | reserved |
| 2 | RW | 0x0 | sli_splt_cpst<br>Slice split compensation when slice is splited by byte. Byte distortion of current slice will be compensated in the next slice. |
| 1 | RW | 0x0 | sli_splt_mode<br>Slice split mode.<br>1'h0: Slice splited by byte.<br>1'h1: Slice splited by number of MB(H.264)/CTU(HEVC). |
| 0 | RW | 0x0 | sli_splt<br>Slice split enable. |

**VEPU580_SLI_BYTE**

Address: Operational Base + offset (0x0364)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19:0 | RW | 0x00000 | sli_splt_byte<br>Byte number for each slice when slice is splited by byte. |

**VEPU580_SLI_CNUM**

Address: Operational Base + offset (0x0368)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sli_splt_cnum_m1<br>Number of CTU/MB for slice split. Valid when slice is splited by CTU/MB. |

**VEPU580_ME_RNGE**

Address: Operational Base + offset (0x0370)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | dlt_frm_num<br>Frame number difference value between current and reference frame, HEVC only. |
| 15:14 | RO | 0x0 | reserved |
| 13:11 | RW | 0x0 | rme_srch_v<br>RME vertical search range, values from 4 to 5. |
| 10:8 | RW | 0x0 | rme_srch_h<br>RME horizontal search range, values from 3 to 7. |
| 7:4 | RW | 0x0 | cme_srch_v<br>CME vertical search range, base on 16 pixel. |
| 3:0 | RW | 0x0 | cme_srch_h<br>CME horizontal search range, base on 16 pixels. |

**VEPU580_ME_CFG_HEVC**

Address: Operational Base + offset (0x0374)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RW | 0x0 | fme_dis<br>[3]: Disable 64x64 block FME.<br>[2]: Disable 32x32 block FME.<br>[1]: Disable 16x16 block FME.<br>[0]: Disable 8x8 block FME. |
| 27 | RO | 0x0 | reserved |
| 26:23 | RW | 0x0 | rme_dis<br>[3]: Disable 64x64 block RME.<br>[2]: Disable 32x32 block RME.<br>[1]: Disable 16x16 block RME.<br>[0]: Disable 8x8 block RME. |
| 22 | RO | 0x0 | reserved |
| 21 | RW | 0x0 | colmv_load<br>Load co-located Mvs as predicated Mv candidates, HEVC only. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 20 | RW | 0x0 | colmv_stor<br>Store col-Mv information to external memory, HEVC only. |
| 19:18 | RW | 0x2 | pmv_num<br>PMV number (should be constant2). |
| 17:16 | RO | 0x0 | reserved |
| 15:8 | RW | 0x05 | pmv_mdst_v<br>Min vertical distance for PMV selection. |
| 7:0 | RW | 0x05 | pmv_mdst_h<br>Min horizontal distance for PMV selection. |

**VEPU580_ME_CFG_H264**

Address: Operational Base + offset (0x0374)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | lvl4_ovrd_en<br>1'b1: Fme lvl4 int_mv override by the corresponding lvl8 int_mv;<br>1'b0: No operation. |
| 30 | RO | 0x0 | reserved |
| 29:27 | RW | 0x0 | fme_dis<br>[2]: Disable 16x16 block FME.<br>[1]: Disable 8x8 block FME.<br>[0]: Disable 4x4 block FME. |
| 26:25 | RO | 0x0 | reserved |
| 24:22 | RW | 0x0 | rme_dis<br>[2]: Disable 16x16 block RME.<br>[1]: Disable 8x8 block RME.<br>[0]: Disable 4x4 block RME. |
| 21 | RW | 0x0 | colmv_load<br>Load co-located Mvs as predicated Mv candidates, HEVC only. |
| 20 | RW | 0x0 | colmv_stor<br>Store col-Mv information to external memory, HEVC only. |
| 19:18 | RW | 0x2 | pmv_num<br>PMV number (should be constant2). |
| 17:16 | RW | 0x1 | mv_llmt<br>Motion vector limit ( by level), H.264 only.<br>2'h0: Mvy is limited to [-64,63].<br>Others: Mvy is limited to [-128,127]. |
| 15:8 | RW | 0x05 | pmv_mdst_v<br>Min vertical distance for PMV selection. |
| 7:0 | RW | 0x05 | pmv_mdst_h<br>Min horizontal distance for PMV selection. |

**VEPU580_ME_CACH**

Address: Operational Base + offset (0x0378)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:27 | RO | 0x00 | reserved |
| 26:18 | RW | 0x000 | cme_linebuf_w<br>The width of CIME down-sample recon data linebuf, based on 64 pixel. |
| 17:16 | RW | 0x0 | cach_l2_map<br>L2 cach mapping, base on pixels.<br>2'h0: 32x512<br>2'h1: 16x1024<br>2'h2: 8x2048<br>2'h3: 4x4096<br>To get better performance, the recommended configuration is as follow:<br>1) When picture width <= 3072, cach_l2_map = 1;<br>2) When picture width > 3072, cach_l2_map = 3; |
| 15:11 | RW | 0x00 | cme_rama_h<br>Height of CME RAMA district, base on 4 pixels. |
| 10:0 | RW | 0x000 | cme_rama_max<br>CME's max RAM address. |

**VEPU580_GMV**

Address: Operational Base + offset (0x0380)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:16 | RW | 0x0000 | gmv_y<br>Y ordinate of Global Motion Vector, base on 4 pixels. |
| 15:13 | RO | 0x0 | reserved |
| 12:0 | RW | 0x0000 | gmv_x<br>X ordinate of Global Motion Vector, base on 4 pixels. |

**VEPU580_ROI_EN**

Address: Operational Base + offset (0x0390)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2 | RW | 0x0 | roi_fmv_en<br>ROI Force Mv enable. |
| 1 | RW | 0x0 | roi_amv_en<br>ROI Area Mv enable. |
| 0 | RW | 0x0 | roi_qp_en<br>ROI QP enable. |

**VEPU580_RDO_CFG_H264**

Address: Operational Base + offset (0x03A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 21:20 | RW | 0x0 | scl_lst_sel<br>Scale list selection.<br>2'h0: Flat scale list.<br>2'h1: Default scale list.<br>2'h2: User defined.<br>2'h3: Reserved. |
| 19 | RW | 0x0 | atf_intra_e<br>Intra mode anti-flicker enable. |
| 18:16 | RO | 0x0 | reserved |
| 15 | RW | 0x0 | atr_e<br>Anti-ring enable. |
| 14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | ccwa_e<br>Chroma cost weight adjustment(KLUT) enable. |
| 12:5 | RW | 0x00 | rdo_mask<br>[7]: Disable intra4x4.<br>[6]: Disable intra8x8.<br>[5]: Disable intra16x16.<br>[4]: Disable inter8x8 with T4.<br>[3]: Disable inter8x8 with T8.<br>[2]: Disable inter16x16 with T4.<br>[1]: Disable inter16x16 with T8.<br>[0]: Disable skip mode. |
| 4 | RW | 0x0 | chrm_spcl<br>Chroma special candidates enable. |
| 3 | RW | 0x0 | vlc_lmt<br>CAVLC syntax limit. |
| 2 | RW | 0x0 | arb_sel<br>Reserved |
| 1 | RW | 0x0 | inter_4x4<br>4x4 sub MB enable. |
| 0 | RW | 0x0 | rect_size<br>Limit sub_mb_rect_size for low level. |

**VEPU580_RDO_CFG_HEVC**

Address: Operational Base + offset (0x03A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RW | 0x0 | satd_byps_flg<br>Rdo cost caculation expression for intra by using sad or satd.<br>[3]: pu32 satd bypass enable, 0--satd, 1--sad;<br>[2]: pu16 satd bypass enable, 0--satd, 1--sad;<br>[1]: pu8 satd bypass enable, 0--satd, 1--sad;<br>[0]: pu4 satd bypass enable, 0--satd, 1--sad; |
| 27:26 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 25:24 | RW | 0x0 | scl_lst_sel<br>Scale list selection.<br>2'h0: Flat scale list.<br>2'h1: Default scale list.<br>2'h2: User defined.<br>2'h3: Reserved. |
| 23 | RW | 0x0 | ccwa_e<br>Chroma cost weight adjustment(KLUT) enable. |
| 22:19 | RW | 0x0 | cu_intra_e<br>[3]: Intra 32x32 mode enable.<br>[2]: Intra 16x16 mode enable.<br>[1]: Intra 8x8 mode enable.<br>[0]: Intra 4x4 mode enable. |
| 18:15 | RO | 0x0 | reserved |
| 14:3 | RW | 0x000 | cu_inter_e<br>Number of CU interpolation, the value must not been bigger than sw_max_num_merge_cand+1.<br>[11:9]: Number of cu64 interpolation.<br>[8:6]: Number of cu32 interpolation.<br>[5:3]: Number of cu16 interpolation.<br>[2:0]: Number of cu8 interpolation. |
| 2 | RW | 0x0 | chrm_spcl<br>4 special chroma candidates enable. |
| 1 | RW | 0x0 | ltm_idx0l0<br>The 1st reference frame in ref-list0 is long term. |
| 0 | RW | 0x0 | ltm_col<br>Co-located picture is long term reference frame. |

**VEPU580_IPRD_CSTS**

Address: Operational Base + offset (0x03A4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27:16 | RW | 0x000 | vthd_c<br>CHROMA variance threshold to select intra prediction cost function. |
| 15:12 | RO | 0x0 | reserved |
| 11:0 | RW | 0x000 | vthd_y<br>LUMA variance threshold to select intra prediction cost function. |

**VEPU580_SYNT_NAL_H264**

Address: Operational Base + offset (0x03B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6:2 | RW | 0x00 | nal_unit_type<br>nal_unit_type |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1:0 | RW | 0x0 | nal_ref_idc<br>nal_ref_idc |

**VEPU580_SYNT_NAL_HEVC**

Address: Operational Base + offset (0x03B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5:0 | RW | 0x00 | nal_unit_type<br>nal_unit_type |

**VEPU580_SYNT_SPS_H264**

Address: Operational Base + offset (0x03B4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:9 | RO | 0x000000 | reserved |
| 8:5 | RW | 0x0 | mpoc_lm4<br>log2_max_pic_order_cnt_lsb_minus4 |
| 4 | RW | 0x0 | drct_8x8<br>direct_8x8_inference_flag |
| 3:0 | RW | 0x0 | max_fnum<br>log2_max_frame_num_minus4 |

**VEPU580_SYNT_SPS_HEVC**

Address: Operational Base + offset (0x03B4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x000 | reserved |
| 20 | RW | 0x0 | strg_intra_smth<br>strong_intra_smoothing_enabled_flag |
| 19:16 | RW | 0x0 | log2_max_poc_lsb<br>log2_max_pic_order_cnt_lsb_minus4 |
| 15 | RW | 0x0 | tmpl_mvp_e<br>sps_temporal_mvp_enabled_flag |
| 14:9 | RW | 0x00 | num_lt_ref_pic<br>num_long_term_ref_pics_sps |
| 8 | RW | 0x0 | lt_ref_pic_prsnt<br>long_term_ref_pics_present_flag |
| 7:1 | RW | 0x00 | num_st_ref_pic<br>num_short_term_ref_pic_sets |
| 0 | RW | 0x0 | smpl_adpt_ofst_e<br>sample_adaptive_offset_enabled_flag |

**VEPU580_SYNT_PPS_H264**

Address: Operational Base + offset (0x03B8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x00 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 24 | RW | 0x0 | dbf_cp_flg<br>deblocking_filter_control_present_flag |
| 23 | RW | 0x0 | wght_pred<br>weight_pred_flag |
| 22:18 | RW | 0x00 | cr_ofst<br>second_chroma_qp_index_offset |
| 17:13 | RW | 0x00 | cb_ofst<br>chroma_qp_index_offset |
| 12:7 | RW | 0x00 | pic_init_qp<br>pic_init_qp_minus26 + 26 |
| 6:5 | RW | 0x0 | num_ref1_idx<br>num_ref_idx_l1_active_minus1 |
| 4:3 | RW | 0x0 | num_ref0_idx<br>num_ref_idx_l0_active_minus1 |
| 2 | RW | 0x0 | csip_flag<br>constrained_intra_pred_flag |
| 1 | RW | 0x0 | trns_8x8<br>transform_8x8_mode_flag |
| 0 | RW | 0x0 | etpy_mode<br>entropy_coding_mode_flag |

**VEPU580_SYNT_PPS_HEVC**

Address: Operational Base + offset (0x03B8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21 | RW | 0x0 | lp_fltr_acrs_til<br>loop_filter_across_tiles_enabled_flag |
| 20:19 | RW | 0x0 | cu_qp_dlt_depth<br>diff_cu_qp_delta_depth |
| 18 | RW | 0x0 | sli_seg_hdr_extn<br>slice_segment_header_extension_present_flag |
| 17 | RW | 0x0 | lst_mdfy_prsnt_flg<br>lists_modification_present_flag |
| 16 | RW | 0x0 | dblk_fltr_ovrd_e<br>deblocking_filter_override_enabled_flag |
| 15 | RW | 0x0 | lp_fltr_acrs_sli<br>pps_loop_filter_across_slices_enabled_flag |
| 14 | RW | 0x0 | chrm_qp_ofst_prsnt<br>pps_slice_chroma_qp_offsets_present_flag. VEPU only supports PPS level chroma QP adjustmentso this field shoud be configured to 0. |
| 13 | RW | 0x0 | cu_qp_dlt_en<br>cu_qp_delta_enabled_flag |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12:7 | RW | 0x00 | pic_init_qp<br>init_qp_minus26+26 |
| 6 | RW | 0x0 | cbc_init_prsnt_flag<br>cabac_init_present_flag |
| 5 | RW | 0x0 | sgn_dat_hid_e<br>sign_data_hiding_enabled_flag |
| 4:2 | RW | 0x0 | num_extr_sli_hdr<br>num_extra_slice_header_bits |
| 1 | RW | 0x0 | out_flg_prsnt_flg<br>output_flag_present_flag |
| 0 | RW | 0x0 | dpdnt_sli_seg_en<br>dependent_slice_segments_enable_flag |

**VEPU580_SYNT_SLI0_H264**

Address: Operational Base + offset (0x03BC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | frm_num<br>frame_num |
| 15:14 | RO | 0x0 | reserved |
| 13:12 | RW | 0x0 | cbc_init_idc<br>cabac_init_idc |
| 11 | RW | 0x0 | num_ref_ovrd<br>num_ref_idx_active_override_flag |
| 10 | RW | 0x0 | drct_smvp<br>direct_spatial_mv_pred_flag |
| 9:2 | RW | 0x00 | pps_id<br>pic_parameter_set_id |
| 1:0 | RW | 0x0 | sli_type<br>slice_type: 0->P, 1->B, 2->I. |

**VEPU580_SYNT_SLI0_HEVC**

Address: Operational Base + offset (0x03BC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | no_out_pri_pic<br>no_output_of_prior_pics_flag |
| 30:25 | RW | 0x00 | sli_pps_id<br>slice_pic_parameter_set_id |
| 24 | RW | 0x0 | dpdnt_sli_seg_flg<br>dependent_slice_segment_flag |
| 23:17 | RW | 0x00 | sli_rsrv_flg<br>slice_served_flag |
| 16:15 | RW | 0x0 | sli_type<br>slice_type: 0->B, 1->P, 2->I. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14 | RW | 0x0 | pic_out_flg<br>pic_output_flag |
| 13 | RW | 0x0 | sli_tmprl_mvp_e<br>slice_temporal_mvp_enabled_flag |
| 12 | RW | 0x0 | sli_sao_luma_flg<br>slice_sao_luma_flag |
| 11 | RW | 0x0 | sli_sao_chrm_flg<br>slice_sao_chroma_flag |
| 10 | RW | 0x0 | num_refidx_act_ovrd<br>num_ref_idx_active_override_flag |
| 9:8 | RW | 0x0 | num_refidx_l0_act<br>num_ref_idx_l0_active_minus1 |
| 7:6 | RW | 0x0 | num_refidx_l1_act<br>num_ref_idx_l1_active_minus1 |
| 5 | RW | 0x0 | ref_pic_lst_mdf_l0<br>ref_pic_list_modification_flag_l0 |
| 4 | RO | 0x0 | reserved |
| 3 | RW | 0x0 | mrg_lft_flg<br>sao_merge_left_flag |
| 2 | RW | 0x0 | mrg_up_flg<br>sao_merge_up_flag |
| 1 | RW | 0x0 | mvd_l1_zero_flg<br>mvd_l1_zero_flag |
| 0 | RW | 0x0 | cbc_init_flg<br>cabac_init_flag |

**VEPU580_SYNT_SLI1_H264**

Address: Operational Base + offset (0x03C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | poc_lsb<br>pic_order_cnt_lsb |
| 15:0 | RW | 0x0000 | idr_pid<br>idr_pic_id |

**VEPU580_SYNT_SLI1_HEVC**

Address: Operational Base + offset (0x03C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |
| 30:27 | RW | 0x0 | lst_entry_l0<br>list_entry_l0 |
| 26 | RW | 0x0 | col_frm_l0_flg<br>collocated_from_l0_flag |
| 25 | RW | 0x0 | col_ref_idx<br>collocated_ref_idx |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 24 | RO | 0x0 | reserved |
| 23:22 | RW | 0x0 | max_mrg_cnd<br>5 - five_minus_max_num_merge_cand, values from 0 to 3 |
| 21:16 | RW | 0x00 | sli_qp<br>slice_qp |
| 15:11 | RW | 0x00 | sli_cb_qp_ofst<br>Actually this field should be configured as pps_cb_qp_offset. |
| 10 | RW | 0x0 | dblk_fltr_ovrd_flg<br>deblocking_filter_override_flag |
| 9 | RW | 0x0 | sp_dblk_fltr_dis<br>slice/pps_deblocking_filter_disabled_flag.<br>If VEPU_SYNT_PPS_HEVC.dblk_fltr_ovrd_e==1 and VEPU_SYNT_SLI1_HEVC.dblk_fltr_ovrd_flg==1, this field is considered as slice_deblocking_filter_disabled_flag. Otherwise it is pps_deblocking_filter_disabled_flag. |
| 8 | RW | 0x0 | sli_lp_fltr_acrs_sli<br>slice_loop_filter_across_slices_enabled_flag |
| 7:4 | RW | 0x0 | sp_beta_ofst_div2<br>slice/pps_beta_offset_div2.<br>If VEPU_SYNT_PPS_HEVC.dblk_fltr_ovrd_e==1 and VEPU_SYNT_SLI1_HEVC.dblk_fltr_ovrd_flg==1, this field is considered as slice_beta_offset_div2. Otherwise it is pps_beta_offset_div2. |
| 3:0 | RW | 0x0 | sp_tc_ofst_div2<br>slice/pps_tc_offset_div2.<br>If VEPU_SYNT_PPS_HEVC.dblk_fltr_ovrd_e==1 and VEPU_SYNT_SLI1_HEVC.dblk_fltr_ovrd_flg==1, this field is considered as slice_tc_offset_div2. Otherwise it is pps_tc_offset_div2. |

**VEPU580_SYNT_SLI2_H264**

Address: Operational Base + offset (0x03C4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | rodr_pic_num<br>abs_diff_pic_num_minus1/long_term_pic_num |
| 15:13 | RO | 0x0 | reserved |
| 12:11 | RW | 0x0 | dis_dblk_idc<br>disable_deblocking_filter_idc |
| 10:7 | RW | 0x0 | sli_alph_ofst<br>slice_alpha_c0_offset_div2 |
| 6:3 | RW | 0x0 | sli_beta_ofst<br>slice_beta_offset_div2 |
| 2 | RW | 0x0 | ref_list0_rodr<br>ref_pic_list_reordering_flag_l0 |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1:0 | RW | 0x0 | rodr_pic_idx<br>reordering_of_pic_nums_idc |

**VEPU580_SYNT_SLI2_HEVC**

Address: Operational Base + offset (0x03C4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x00 | reserved |
| 24:16 | RW | 0x000 | sli_hdr_ext_len<br>slice_segment_header_extension_length |
| 15:0 | RW | 0x0000 | sli_poc_lsb<br>slice_pic_order_cnt_lsb |

**VEPU580_SYNT_REFM0_H264**

Address: Operational Base + offset (0x03C8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:26 | RW | 0x0 | mmco_type2<br>memory_management_control_operation[2] |
| 25:23 | RW | 0x0 | mmco_type1<br>memory_management_control_operation[1] |
| 22:7 | RW | 0x0000 | mmco_parm0<br>MMCO parameters which have different meanings according to different mmco_parm0 valus.<br>difference_of_pic_nums_minus1 for mmco_parm0 equals 0 or 3.<br>long_term_pic_num for mmco_parm0 equals 2.<br>long_term_frame_idx for mmco_parm0 equals 6.<br>max_long_term_frame_idx_plus1 for mmco_parm0 equals 4. |
| 6:4 | RW | 0x0 | mmco_type0<br>memory_management_control_operation |
| 3 | RW | 0x0 | mmco4_pre<br>A No.4 MMCO should be executed firstly if mmo4_pre is 1 |
| 2 | RW | 0x0 | arpm_flg<br>adaptive_ref_pic_marking_mode_flag |
| 1 | RW | 0x0 | ltrf_flg<br>long_term_reference_flag |
| 0 | RW | 0x0 | nopp_flg<br>no_output_of_prior_pics_flag |

**VEPU580_SYNT_REFM0_HEVC**

Address: Operational Base + offset (0x03C8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | num_lt_sps<br>num_long_term_sps |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 29:24 | RW | 0x00 | st_ref_pic_idx<br>short_term_ref_pic_set_idx |
| 23:22 | RW | 0x0 | num_lt_pic<br>num_long_term_pics |
| 21:17 | RW | 0x00 | lt_idx_sps<br>lt_idx_sps |
| 16:1 | RW | 0x0000 | poc_lsb_lt0<br>poc_lsb_lt[0] |
| 0 | RW | 0x0 | st_ref_pic_flg<br>short_term_ref_pic_set_sps_flag |

**VEPU580_SYNT_REFM1_H264**

Address: Operational Base + offset (0x03CC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | mmco_parm2<br>MMCO parameters which have different meanings according to different mmco_parm2 valus.<br>difference_of_pic_nums_minus1 for mmco_parm2 equals 0 or 3.<br>long_term_pic_num for mmco_parm2 equals 2.<br>long_term_frame_idx for mmco_parm2 equals 6.<br>max_long_term_frame_idx_plus1 for mmco_parm2 equals 4. |
| 15:0 | RW | 0x0000 | mmco_parm1<br>MMCO parameters which have different meanings according to different mmco_parm1 valus.<br>difference_of_pic_nums_minus1 for mmco_parm1 equals 0 or 3.<br>long_term_pic_num for mmco_parm1 equals 2.<br>long_term_frame_idx for mmco_parm1 equals 6.<br>max_long_term_frame_idx_plus1 for mmco_parm1 equals 4. |

**VEPU580_SYNT_REFM1_HEVC**

Address: Operational Base + offset (0x03CC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | used_by_lt_flg2<br>used_by_curr_pic_lt_flag[2] |
| 30 | RW | 0x0 | used_by_lt_flg1<br>used_by_curr_pic_lt_flag[1] |
| 29 | RW | 0x0 | used_by_lt_flg0<br>used_by_curr_pic_lt_flag[0] |
| 28 | RW | 0x0 | dlt_poc_msb_prsnt2<br>delta_poc_msb_present_flag[2] |
| 27 | RW | 0x0 | dlt_poc_msb_prsnt1<br>delta_poc_msb_present_flag[1] |
| 26 | RW | 0x0 | dlt_poc_msb_prsnt0<br>delta_poc_msb_present_flag[0] |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 25:10 | RW | 0x0000 | dlt_poc_msb_cycl0<br>delta_poc_msb_cycle_lt[0] |
| 9:5 | RW | 0x00 | num_negative_pics<br>num_neg_pic |
| 4 | RW | 0x0 | num_pos_pic<br>num_positive_pics |
| 3:0 | RW | 0x0 | used_by_s0_flg<br>used_by_curr_pic_s0_flag |

**VEPU580_SYNT_REFM2_HEVC**

Address: Operational Base + offset (0x03D0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | dlt_poc_s0_m11<br>delta_poc_s0_minus1[1] |
| 15:0 | RW | 0x0000 | dlt_poc_s0_m10<br>delta_poc_s0_minus1[0] |

**VEPU580_SYNT_REFM2_H264**

Address: Operational Base + offset (0x03D0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:8 | RW | 0x0 | long_term_frame_idx2<br>long_term_frame_idx[2] (when mmco equal 3) |
| 7:4 | RW | 0x0 | long_term_frame_idx1<br>long_term_frame_idx[1] (when mmco equal 3) |
| 3:0 | RW | 0x0 | long_term_frame_idx0<br>long_term_frame_idx[0] (when mmco equal 3) |

**VEPU580_SYNT_REFM3_HEVC**

Address: Operational Base + offset (0x03D4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | dlt_poc_s0_m13<br>delta_poc_s0_minus1[3] |
| 15:0 | RW | 0x0000 | dlt_poc_s0_m12<br>delta_poc_s0_minus1[2] |

**VEPU580_SYNT_LONG_REFM0**

Address: Operational Base + offset (0x03D8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | poc_lsb_lt2<br>Poc_lsb_lt[2] |
| 15:0 | RW | 0x0000 | poc_lsb_lt1<br>Poc_lsb_lt[1] |

**VEPU580_SYNT_LONG_REFM1**

Rockchip Confidencial

Address: Operational Base + offset (0x03DC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | dlt_poc_msb_cycl2<br>Delta_poc_msb_cycle_lt[2] |
| 15:0 | RW | 0x0000 | dlt_poc_msb_cycl1<br>Delta_poc_msb_cycle_lt[1] |

**VEPU580_LINE_SLICE_H264**

Address: Operational Base + offset (0x03F0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | sli_crs_en<br>Slice cut cross lines enable, using for breaking the resolution limit, h264 only. |
| 30:16 | RO | 0x0000 | reserved |
| 15 | RW | 0x0 | mv_v_lmt_en<br>According the profile, motion vector limit enable. |
| 14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | mv_v_lmt_thd<br>According the profile, motion vector limit ( by level ) , H.264 only, based on 1 pixel. |

**VEPU580_TILE_CFG_HEVC**

Address: Operational Base + offset (0x03F0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | tile_en<br>Tile cut enable, hevc only. |
| 30:24 | RO | 0x00 | reserved |
| 23:16 | RW | 0x00 | tile_h_m1<br>The height of current tile minus 1, based on 64 pixel, hevc only. |
| 15:8 | RO | 0x00 | reserved |
| 7:0 | RW | 0x00 | tile_w_m1<br>The width of current tile minus 1, based on 64 pixel, hevc only. |

**VEPU580_TILE_POS**

Address: Operational Base + offset (0x03F4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23:16 | RW | 0x00 | tile_y<br>The top-left point of current tile in the vertical dirction, based on 64 pixel, hevc only. |
| 15:8 | RO | 0x00 | reserved |
| 7:0 | RW | 0x00 | tile_x<br>The top-left point of current tile in the horizontal dirction, based on 64 pixel, hevc only. |

**VEPU580_RC_ADJ0**

Rockchip Confidential

Address: Operational Base + offset (0x1000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x00 | reserved |
| 24:20 | RW | 0x00 | qp_adj4<br>QP adjust step4 for rate control. It's a signed number and the valid value is from -16 to 15. |
| 19:15 | RW | 0x00 | qp_adj3<br>QP adjust step3 for rate control. It's a signed number and the valid value is from -16 to 15. |
| 14:10 | RW | 0x00 | qp_adj2<br>QP adjust step2 for rate control. It's a signed number and the valid value is from -16 to 15. |
| 9:5 | RW | 0x00 | qp_adj1<br>QP adjust step1 for rate control. It's a signed number and the valid value is from -16 to 15. |
| 4:0 | RW | 0x00 | qp_adj0<br>QP adjust step0 for rate control. It's a signed number and the valid value is from -16 to 15. |

**VEPU580_RC_ADJ1**

Address: Operational Base + offset (0x1004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:15 | RW | 0x00 | qp_adj8<br>QP adjust step8 for rate control. It's a signed number and the valid value is from -16 to 15. |
| 14:10 | RW | 0x00 | qp_adj7<br>QP adjust step7 for rate control. It's a signed number and the valid value is from -16 to 15. |
| 9:5 | RW | 0x00 | qp_adj6<br>QP adjust step6 for rate control. It's a signed number and the valid value is from -16 to 15. |
| 4:0 | RW | 0x00 | qp_adj5<br>QP adjust step5 for rate control. It's a signed number and the valid value is from -16 to 15. |

**VEPU580_RC_DTHD0**

Address: Operational Base + offset (0x1008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | rc_dthd0<br>Bits rate deviation threshold0. |

**VEPU580_RC_DTHD1**

Address: Operational Base + offset (0x100C)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | rc_dthd1<br>Bits rate deviation threshold1. |

**VEPU580_RC_DTHD2**

Address: Operational Base + offset (0x1010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | rc_dthd2<br>Bits rate deviation threshold2. |

**VEPU580_RC_DTHD3**

Address: Operational Base + offset (0x1014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | rc_dthd3<br>Bits rate deviation threshold3. |

**VEPU580_RC_DTHD4**

Address: Operational Base + offset (0x1018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | rc_dthd4<br>Bits rate deviation threshold4. |

**VEPU580_RC_DTHD5**

Address: Operational Base + offset (0x101C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | rc_dthd5<br>Bits rate deviation threshold5. |

**VEPU580_RC_DTHD6**

Address: Operational Base + offset (0x1020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | rc_dthd6<br>Bits rate deviation threshold6. |

**VEPU580_RC_DTHD7**

Address: Operational Base + offset (0x1024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | rc_dthd7<br>Bits rate deviation threshold7. |

**VEPU580_RC_DTHD8**

Address: Operational Base + offset (0x1028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | rc_dthd8<br>Bits rate deviation threshold8. |

Rockchip Confidencial

**VEPU580_ROI_QTHD0**

Address: Operational Base + offset (0x1030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:24 | RW | 0x00 | qpmin_area2<br>Min QP for 16x16 CU inside ROI area2. |
| 23:18 | RW | 0x00 | qpmax_area1<br>Max QP for 16x16 CU inside ROI area1. |
| 17:12 | RW | 0x00 | qpmin_area1<br>Min QP for 16x16 CU inside ROI area1. |
| 11:6 | RW | 0x00 | qpmax_area0<br>Max QP for 16x16 CU inside ROI area0. |
| 5:0 | RW | 0x00 | qpmin_area0<br>Min QP for 16x16 CU inside ROI area0. |

**VEPU580_ROI_QTHD1**

Address: Operational Base + offset (0x1034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:24 | RW | 0x00 | qpmax_area4<br>Max QP for 16x16 CU inside ROI area4. |
| 23:18 | RW | 0x00 | qpmin_area4<br>Min QP for 16x16 CU inside ROI area4. |
| 17:12 | RW | 0x00 | qpmax_area3<br>Max QP for 16x16 CU inside ROI area3. |
| 11:6 | RW | 0x00 | qpmin_area3<br>Min QP for 16x16 CU inside ROI area3. |
| 5:0 | RW | 0x00 | qpmax_area2<br>Max QP for 16x16 CU inside ROI area2. |

**VEPU580_ROI_QTHD2**

Address: Operational Base + offset (0x1038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:24 | RW | 0x00 | qpmin_area7<br>Min QP for 16x16 CU inside ROI area7. |
| 23:18 | RW | 0x00 | qpmax_area6<br>Max QP for 16x16 CU inside ROI area6. |
| 17:12 | RW | 0x00 | qpmin_area6<br>Min QP for 16x16 CU inside ROI area6. |
| 11:6 | RW | 0x00 | qpmax_area5<br>Max QP for 16x16 CU inside ROI area5. |
| 5:0 | RW | 0x00 | qpmin_area5<br>Min QP for 16x16 CU inside ROI area5. |

**VEPU580_ROI_QTHD3**

Rockchip Confidencial

Address: Operational Base + offset (0x103C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | qpmap_mode<br>QP theshold generation for the CUs whose size is bigger than 16x16.<br>2'h0: Mean value of 16x16 CU QP thesholds<br>2'h1: Max value of 16x16 CU QP thesholds<br>2'h2: Min value of 16x16 CU QP thesholds<br>2'h3: Reserved |
| 29:6 | RO | 0x000000 | reserved |
| 5:0 | RW | 0x00 | qpmax_area7<br>Max QP for 16x16 CU inside ROI area7. |

**VEPU580_MADI_CFG**

Address: Operational Base + offset (0x1040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23:16 | RW | 0x00 | madi_thd<br>Texture threshold for madi statistics. |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | madi_mode<br>MADI generation mode for CU32 and CU64.<br>1'h0: Follow 32x32 and 64x64 MADI functions.<br>1'h1: Calculated by the mean of corresponding CU16 MADIs. |

**VEPU580_AQ_TTHD0**

Address: Operational Base + offset (0x1044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | aq_tthd3<br>Texture threshold3 for adaptive QP adjustment. |
| 23:16 | RW | 0x00 | aq_tthd2<br>Texture threshold2 for adaptive QP adjustment. |
| 15:8 | RW | 0x00 | aq_tthd1<br>Texture threshold1 for adaptive QP adjustment. |
| 7:0 | RW | 0x00 | aq_tthd0<br>Texture threshold0 for adaptive QP adjustment. |

**VEPU580_AQ_TTHD1**

Address: Operational Base + offset (0x1048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | aq_tthd7<br>Texture threshold7 for adaptive QP adjustment. |
| 23:16 | RW | 0x00 | aq_tthd6<br>Texture threshold6 for adaptive QP adjustment. |
| 15:8 | RW | 0x00 | aq_tthd5<br>Texture threshold5 for adaptive QP adjustment. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:0 | RW | 0x00 | aq_tthd4<br>Texture threshold4 for adaptive QP adjustment. |

**VEPU580_AQ_TTHD2**

Address: Operational Base + offset (0x104C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | aq_tthd11<br>Texture threshold11 for adaptive QP adjustment. |
| 23:16 | RW | 0x00 | aq_tthd10<br>Texture threshold10 for adaptive QP adjustment. |
| 15:8 | RW | 0x00 | aq_tthd9<br>Texture threshold9 for adaptive QP adjustment. |
| 7:0 | RW | 0x00 | aq_tthd8<br>Texture threshold8 for adaptive QP adjustment. |

**VEPU580_AQ_TTHD3**

Address: Operational Base + offset (0x1050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | aq_tthd15<br>Texture threshold15 for adaptive QP adjustment. |
| 23:16 | RW | 0x00 | aq_tthd14<br>Texture threshold14 for adaptive QP adjustment. |
| 15:8 | RW | 0x00 | aq_tthd13<br>Texture threshold13 for adaptive QP adjustment. |
| 7:0 | RW | 0x00 | aq_tthd12<br>Texture threshold12 for adaptive QP adjustment. |

**VEPU580_AQ_STP0**

Address: Operational Base + offset (0x1054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:24 | RW | 0x00 | aq_stp_2t3<br>QP adjust step when current texture strength >= aq_tthd2 and < aq_tthd3. It's a signed number and the valid value is from -32 to 31. |
| 23:22 | RO | 0x0 | reserved |
| 21:16 | RW | 0x00 | aq_stp_1t2<br>QP adjust step when current texture strength >= aq_tthd1 and < aq_tthd2. It's a signed number and the valid value is from -32 to 31. |
| 15:14 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:8 | RW | 0x00 | aq_stp_0t1<br>QP adjust step when current texture strength >= aq_tthd0 and < aq_tthd1. It's a signed number and the valid value is from -32 to 31. |
| 7:6 | RO | 0x0 | reserved |
| 5:0 | RW | 0x00 | aq_stp_s0<br>QP adjust step when current texture strength < aq_tthd0. It's a signed number and the valid value is from -32 to 31. |

**VEPU580_AQ_STP1**

Address: Operational Base + offset (0x1058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:24 | RW | 0x00 | aq_stp_6t7<br>QP adjust step when current texture strength >= aq_tthd6 and < aq_tthd7. It's a signed number and the valid value is from -32 to 31. |
| 23:22 | RO | 0x0 | reserved |
| 21:16 | RW | 0x00 | aq_stp_5t6<br>QP adjust step when current texture strength >= aq_tthd5 and < aq_tthd6. It's a signed number and the valid value is from -32 to 31. |
| 15:14 | RO | 0x0 | reserved |
| 13:8 | RW | 0x00 | aq_stp_4t5<br>QP adjust step when current texture strength >= aq_tthd4 and < aq_tthd5. It's a signed number and the valid value is from -32 to 31. |
| 7:6 | RO | 0x0 | reserved |
| 5:0 | RW | 0x00 | aq_stp_3t4<br>QP adjust step when current texture strength >= aq_tthd3 and < aq_tthd4. It's a signed number and the valid value is from -32 to 31. |

**VEPU580_AQ_STP2**

Address: Operational Base + offset (0x105C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:24 | RW | 0x00 | aq_stp_11t12<br>QP adjust step when current texture strength > aq_tthd11 and <= aq_tthd12. It's a signed number and the valid value is from -32 to 31. |
| 23:22 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 21:16 | RW | 0x00 | aq_stp_10t11<br>QP adjust step when current texture strength > aq_tthd10 and <= aq_tthd11. It's a signed number and the valid value is from -32 to 31. |
| 15:14 | RO | 0x0 | reserved |
| 13:8 | RW | 0x00 | aq_stp_9t10<br>QP adjust step when current texture strength > aq_tthd9 and <= aq_tthd10. It's a signed number and the valid value is from -32 to 31. |
| 7:6 | RO | 0x0 | reserved |
| 5:0 | RW | 0x00 | aq_stp_8t9<br>QP adjust step when current texture strength > aq_tthd8 and <= aq_tthd9. It's a signed number and the valid value is from -32 to 31. |

**VEPU580_AQ_STP3**

Address: Operational Base + offset (0x1060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:24 | RW | 0x00 | aq_stp_b15<br>QP adjust step when current texture strength > aq_tthd15. It's a signed number and the valid value is from -32 to 31. |
| 23:22 | RO | 0x0 | reserved |
| 21:16 | RW | 0x00 | aq_stp_14t15<br>QP adjust step when current texture strength > aq_tthd14 and <= aq_tthd15. It's a signed number and the valid value is from -32 to 31. |
| 15:14 | RO | 0x0 | reserved |
| 13:8 | RW | 0x00 | aq_stp_13t14<br>QP adjust step when current texture strength > aq_tthd13 and <= aq_tthd14. It's a signed number and the valid value is from -32 to 31. |
| 7:6 | RO | 0x0 | reserved |
| 5:0 | RW | 0x00 | aq_stp_12t13<br>QP adjust step when current texture strength > aq_tthd12 and <= aq_tthd13. It's a signed number and the valid value is from -32 to 31. |

**VEPU580_MD_SAD_THD**

Address: Operational Base + offset (0x1070)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23:16 | RW | 0x00 | md_sad_thd2<br>SAD threshold2 of motion detection. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:8 | RW | 0x00 | md_sad_thd1<br>SAD threshold1 of motion detection. |
| 7:0 | RW | 0x00 | md_sad_thd0<br>SAD threshold0 of motion detection. |

**VEPU580_MADI_THD**

Address: Operational Base + offset (0x1074)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23:16 | RW | 0x00 | madi_thd2<br>MADI threshold2. |
| 15:8 | RW | 0x00 | madi_thd1<br>MADI threshold1. |
| 7:0 | RW | 0x00 | madi_thd0<br>MADI threshold0. |

**VEPU580_KLUT_OFST**

Address: Operational Base + offset (0x1080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2:0 | RW | 0x0 | chrm_klut_ofst<br>Offset of (RDO) chroma cost weight table, values from 0 to 6. |

**VEPU580_KLUT_WGT0**

Address: Operational Base + offset (0x1084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RW | 0x000 | chrm_klut_wgt1_l9<br>Low 9 bits of data1 in chroma cost weight table. |
| 22:18 | RO | 0x00 | reserved |
| 17:0 | RW | 0x00000 | chrm_klut_wgt0<br>Data0 in chroma cost weight table. |

**VEPU580_KLUT_WGT1**

Address: Operational Base + offset (0x1088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RW | 0x00000 | chrm_klut_wgt2<br>Data2 in chroma cost weight table. |
| 13:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x000 | chrm_klut_wgt1_h9<br>High 9 bits of data1 in chroma cost weight table. |

**VEPU580_KLUT_WGT2**

Address: Operational Base + offset (0x108C)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RW | 0x000 | chrm_klut_wgt4_l9<br>Low 9 bits of data4 in chroma cost weight table. |
| 22:18 | RO | 0x00 | reserved |
| 17:0 | RW | 0x00000 | chrm_klut_wgt3<br>Data3 in chroma cost weight table. |

**VEPU580_KLUT_WGT3**

Address: Operational Base + offset (0x1090)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RW | 0x00000 | chrm_klut_wgt5<br>Data5 in chroma cost weight table. |
| 13:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x000 | chrm_klut_wgt4_h9<br>High 9 bits of data4 in chroma cost weight table. |

**VEPU580_KLUT_WGT4**

Address: Operational Base + offset (0x1094)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RW | 0x000 | chrm_klut_wgt7_l9<br>Low 9 bits of data7 in chroma cost weight table. |
| 22:18 | RO | 0x00 | reserved |
| 17:0 | RW | 0x00000 | chrm_klut_wgt6<br>Data6 in chroma cost weight table. |

**VEPU580_KLUT_WGT5**

Address: Operational Base + offset (0x1098)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RW | 0x00000 | chrm_klut_wgt8<br>Data8 in chroma cost weight table. |
| 13:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x000 | chrm_klut_wgt7_h9<br>High 9 bits of data7 in chroma cost weight table. |

**VEPU580_KLUT_WGT6**

Address: Operational Base + offset (0x109C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RW | 0x000 | chrm_klut_wgt10_l9<br>Low 9 bits of data10 in chroma cost weight table. |
| 22:18 | RO | 0x00 | reserved |
| 17:0 | RW | 0x00000 | chrm_klut_wgt9<br>Data9 in chroma cost weight table. |

**VEPU580_KLUT_WGT7**

Address: Operational Base + offset (0x10A0)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RW | 0x00000 | chrm_klut_wgt11<br>Data11 in chroma cost weight table. |
| 13:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x000 | chrm_klut_wgt10_h9<br>High 9 bits of data10 in chroma cost weight table. |

**VEPU580_KLUT_WGT8**

Address: Operational Base + offset (0x10A4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RW | 0x000 | chrm_klut_wgt13_l9<br>Low 9 bits of data13 in chroma cost weight table. |
| 22:18 | RO | 0x00 | reserved |
| 17:0 | RW | 0x00000 | chrm_klut_wgt12<br>Data12 in chroma cost weight table. |

**VEPU580_KLUT_WGT9**

Address: Operational Base + offset (0x10A8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RW | 0x00000 | chrm_klut_wgt14<br>Data14 in chroma cost weight table. |
| 13:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x000 | chrm_klut_wgt13_h9<br>High 9 bits of data13 in chroma cost weight table. |

**VEPU580_KLUT_WGT10**

Address: Operational Base + offset (0x10AC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RW | 0x000 | chrm_klut_wgt16_l9<br>Low 9 bits of data16 in chroma cost weight table. |
| 22:18 | RO | 0x00 | reserved |
| 17:0 | RW | 0x00000 | chrm_klut_wgt15<br>Data15 in chroma cost weight table. |

**VEPU580_KLUT_WGT11**

Address: Operational Base + offset (0x10B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RW | 0x00000 | chrm_klut_wgt17<br>Data17 in chroma cost weight table. |
| 13:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x000 | chrm_klut_wgt16_h9<br>High 9 bits of data16 in chroma cost weight table. |

**VEPU580_KLUT_WGT12**

Address: Operational Base + offset (0x10B4)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RW | 0x000 | chrm_klut_wgt19_l9<br>Low 9 bits of data19 in chroma cost weight table. |
| 22:18 | RO | 0x00 | reserved |
| 17:0 | RW | 0x00000 | chrm_klut_wgt18<br>Data18 in chroma cost weight table. |

**VEPU580_KLUT_WGT13**

Address: Operational Base + offset (0x10B8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RW | 0x00000 | chrm_klut_wgt20<br>Data20 in chroma cost weight table. |
| 13:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x000 | chrm_klut_wgt19_h9<br>High 9 bits of data19 in chroma cost weight table. |

**VEPU580_KLUT_WGT14**

Address: Operational Base + offset (0x10BC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RW | 0x000 | chrm_klut_wgt22_l9<br>Low 9 bits of data22 in chroma cost weight table. |
| 22:18 | RO | 0x00 | reserved |
| 17:0 | RW | 0x00000 | chrm_klut_wgt21<br>Data21 in chroma cost weight table. |

**VEPU580_KLUT_WGT15**

Address: Operational Base + offset (0x10C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RW | 0x00000 | chrm_klut_wgt23<br>Data23 in chroma cost weight table. |
| 13:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x000 | chrm_klut_wgt22_h9<br>High 9 bits of data22 in chroma cost weight table. |

**VEPU580_KLUT_WGT16**

Address: Operational Base + offset (0x10C4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RW | 0x000 | chrm_klut_wgt25_l9<br>Low 9 bits of data25 in chroma cost weight table. |
| 22:18 | RO | 0x00 | reserved |
| 17:0 | RW | 0x00000 | chrm_klut_wgt24<br>Data24 in chroma cost weight table. |

**VEPU580_KLUT_WGT17**

Address: Operational Base + offset (0x10C8)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RW | 0x00000 | chrm_klut_wgt26<br>Data26 in chroma cost weight table. |
| 13:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x000 | chrm_klut_wgt25_h9<br>High 9 bits of data25 in chroma cost weight table. |

**VEPU580_KLUT_WGT18**

Address: Operational Base + offset (0x10CC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RW | 0x000 | chrm_klut_wgt28_l9<br>Low 9 bits of data28 in chroma cost weight table. |
| 22:18 | RO | 0x00 | reserved |
| 17:0 | RW | 0x00000 | chrm_klut_wgt27<br>Data27 in chroma cost weight table. |

**VEPU580_KLUT_WGT19**

Address: Operational Base + offset (0x10D0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RW | 0x00000 | chrm_klut_wgt29<br>Data29 in chroma cost weight table. |
| 13:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x000 | chrm_klut_wgt28_h9<br>High 9 bits of data28 in chroma cost weight table. |

**VEPU580_KLUT_WGT20**

Address: Operational Base + offset (0x10D4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RW | 0x000 | chrm_klut_wgt31_l9<br>Low 9 bits of data31 in chroma cost weight table. |
| 22:18 | RO | 0x00 | reserved |
| 17:0 | RW | 0x00000 | chrm_klut_wgt30<br>Data30 in chroma cost weight table. |

**VEPU580_KLUT_WGT21**

Address: Operational Base + offset (0x10D8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RW | 0x00000 | chrm_klut_wgt32<br>Data32 in chroma cost weight table. |
| 13:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x000 | chrm_klut_wgt31_h9<br>High 9 bits of data31 in chroma cost weight table. |

**VEPU580_KLUT_WGT22**

Address: Operational Base + offset (0x10DC)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RW | 0x000 | chrm_klut_wgt34_l9<br>Low 9 bits of data34 in chroma cost weight table. |
| 22:18 | RO | 0x00 | reserved |
| 17:0 | RW | 0x00000 | chrm_klut_wgt33<br>Data33 in chroma cost weight table. |

**VEPU580_KLUT_WGT23**

Address: Operational Base + offset (0x10E0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:9 | RO | 0x000000 | reserved |
| 8:0 | RW | 0x000 | chrm_klut_wgt34_h9<br>High 9 bits of data34 in chroma cost weight table. |

**VEPU580_QNT_BIAS_COMB**

Address: Operational Base + offset (0x1730)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:10 | RW | 0x000 | qnt_bias_p<br>Quantization bias for HEVC and H.264 P frame. |
| 9:0 | RW | 0x000 | qnt_bias_i<br>Quantization bias for HEVC and H.264 I frame. |

**VEPU580_RDO_WGTA_QP15_COMB**

Address: Operational Base + offset (0x193C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23:0 | RW | 0x000000 | wgt_qp15_grpa<br>Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 15. |

**VEPU580_OSD_INV_EN**

Address: Operational Base + offset (0x3000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | osd_ch_inv_msk<br>OSD color inverse expression switch for chroma component, each bit controls corresponding region.<br>1'h0: Expression need to determine the condition;<br>1'h1: Expression don't need to determine the condition; |
| 23:16 | RW | 0x00 | osd_lu_inv_msk<br>OSD color inverse expression switch for luma component, each bit controls corresponding region.<br>1'h0: Expression need to determine the condition;<br>1'h1: Expression don't need to determine the condition; |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:8 | RW | 0x00 | osd_ch_inv_en<br>OSD color inverse enable of chroma component, each bit controls corresponding region. |
| 7:0 | RW | 0x00 | osd_lu_inv_en<br>OSD color inverse enable of luma component, each bit controls corresponding region. |

**VEPU580_OSD_INV_THD**

Address: Operational Base + offset (0x3004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RW | 0x0 | osd_ithd_r7<br>Color inverse theshold for OSD region7. |
| 27:24 | RW | 0x0 | osd_ithd_r6<br>Color inverse theshold for OSD region6. |
| 23:20 | RW | 0x0 | osd_ithd_r5<br>Color inverse theshold for OSD region5. |
| 19:16 | RW | 0x0 | osd_ithd_r4<br>Color inverse theshold for OSD region4. |
| 15:12 | RW | 0x0 | osd_ithd_r3<br>Color inverse theshold for OSD region3. |
| 11:8 | RW | 0x0 | osd_ithd_r2<br>Color inverse theshold for OSD region2. |
| 7:4 | RW | 0x0 | osd_ithd_r1<br>Color inverse theshold for OSD region1. |
| 3:0 | RW | 0x0 | osd_ithd_r0<br>Color inverse theshold for OSD region0. |

**VEPU580_OSD_CFG**

Address: Operational Base + offset (0x3008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17 | RW | 0x0 | osd_plt_typ<br>OSD palette type.<br>1'h1: Default type.<br>1'h0: User defined type. |
| 16 | RW | 0x0 | osd_plt_cks<br>OSD palette clock selection.<br>1'h0: Configure bus clock domain.<br>1'h1: Core clock domain. |
| 15:8 | RW | 0x00 | osd_itype<br>OSD color inverse expression type, each bit controls corresponding region.<br>1'h0: AND;<br>1'h1: OR; |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:0 | RW | 0x00 | osd_en<br>Each bit controls the corresponding OSD region.<br>1'b0: OSD region disable<br>1'b1: OSD region enable |

**VEPU580_OSD0_LT_POS**

Address: Operational Base + offset (0x3010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |
| 25:16 | RW | 0x000 | osd0_lt_y<br>Y coordinate/16 of OSD region0's left-top point. |
| 15:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | osd0_lt_x<br>X coordinate/16 of OSD region0's left-top point. |

**VEPU580_OSD0_RB_POS**

Address: Operational Base + offset (0x3014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |
| 25:16 | RW | 0x000 | osd0_rb_y<br>Y coordinate/16 of OSD region0's right-bottom point. |
| 15:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | osd0_rb_x<br>X coordinate/16 of OSD region0's right-bottom point. |

**VEPU580_OSD1_LT_POS**

Address: Operational Base + offset (0x3018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |
| 25:16 | RW | 0x000 | osd1_lt_y<br>Y coordinate/16 of OSD region1's left-top point. |
| 15:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | osd1_lt_x<br>X coordinate/16 of OSD region1's left-top point. |

**VEPU580_OSD1_RB_POS**

Address: Operational Base + offset (0x301C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |
| 25:16 | RW | 0x000 | osd1_rb_y<br>Y coordinate/16 of OSD region1's right-bottom point. |
| 15:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | osd1_rb_x<br>X coordinate/16 of OSD region1's right-bottom point. |

Rockchip Confidencial

**VEPU580_OSD2_LT_POS**

Address: Operational Base + offset (0x3020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |
| 25:16 | RW | 0x000 | osd2_lt_y<br>Y coordinate/16 of OSD region2's left-top point. |
| 15:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | osd2_lt_x<br>X coordinate/16 of OSD region2's left-top point. |

**VEPU580_OSD2_RB_POS**

Address: Operational Base + offset (0x3024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |
| 25:16 | RW | 0x000 | osd2_rb_y<br>Y coordinate/16 of OSD region2's right-bottom point. |
| 15:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | osd2_rb_x<br>X coordinate/16 of OSD region2's right-bottom point. |

**VEPU580_OSD3_LT_POS**

Address: Operational Base + offset (0x3028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |
| 25:16 | RW | 0x000 | osd3_lt_y<br>Y coordinate/16 of OSD region3's left-top point. |
| 15:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | osd3_lt_x<br>X coordinate/16 of OSD region3's left-top point. |

**VEPU580_OSD3_RB_POS**

Address: Operational Base + offset (0x302C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |
| 25:16 | RW | 0x000 | osd3_rb_y<br>Y coordinate/16 of OSD region3's right-bottom point. |
| 15:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | osd3_rb_x<br>X coordinate/16 of OSD region3's right-bottom point. |

**VEPU580_OSD4_LT_POS**

Address: Operational Base + offset (0x3030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 25:16 | RW | 0x000 | osd4_lt_y<br>Y coordinate/16 of OSD region4's left-top point. |
| 15:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | osd4_lt_x<br>X coordinate/16 of OSD region4's left-top point. |

**VEPU580_OSD4_RB_POS**

Address: Operational Base + offset (0x3034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |
| 25:16 | RW | 0x000 | osd4_rb_y<br>Y coordinate/16 of OSD region4's right-bottom point. |
| 15:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | osd4_rb_x<br>X coordinate/16 of OSD region4's right-bottom point. |

**VEPU580_OSD5_LT_POS**

Address: Operational Base + offset (0x3038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |
| 25:16 | RW | 0x000 | osd5_lt_y<br>Y coordinate/16 of OSD region5's left-top point. |
| 15:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | osd5_lt_x<br>X coordinate/16 of OSD region5's left-top point. |

**VEPU580_OSD5_RB_POS**

Address: Operational Base + offset (0x303C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |
| 25:16 | RW | 0x000 | osd5_rb_y<br>Y coordinate/16 of OSD region5's right-bottom point. |
| 15:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | osd5_rb_x<br>X coordinate/16 of OSD region5's right-bottom point. |

**VEPU580_OSD6_LT_POS**

Address: Operational Base + offset (0x3040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |
| 25:16 | RW | 0x000 | osd6_lt_y<br>Y coordinate/16 of OSD region6's left-top point. |
| 15:10 | RO | 0x00 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9:0 | RW | 0x000 | osd6_lt_x<br>X coordinate/16 of OSD region6's left-top point. |

**VEPU580_OSD6_RB_POS**

Address: Operational Base + offset (0x3044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |
| 25:16 | RW | 0x000 | osd6_rb_y<br>Y coordinate/16 of OSD region6's right-bottom point. |
| 15:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | osd6_rb_x<br>X coordinate/16 of OSD region6's right-bottom point. |

**VEPU580_OSD7_LT_POS**

Address: Operational Base + offset (0x3048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |
| 25:16 | RW | 0x000 | osd7_lt_y<br>Y coordinate/16 of OSD region7's left-top point. |
| 15:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | osd7_lt_x<br>X coordinate/16 of OSD region7's left-top point. |

**VEPU580_OSD7_RB_POS**

Address: Operational Base + offset (0x304C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |
| 25:16 | RW | 0x000 | osd7_rb_y<br>Y coordinate/16 of OSD region7's right-bottom point. |
| 15:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | osd7_rb_x<br>X coordinate/16 of OSD region7's right-bottom point. |

**VEPU580_ADR_OSD0**

Address: Operational Base + offset (0x3050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | osd0_addr<br>High 28 bits of base address for OSD region0, based on 16byte. |
| 3:0 | RO | 0x0 | reserved |

**VEPU580_ADR_OSD1**

Address: Operational Base + offset (0x3054)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | osd1_addr<br>High 28 bits of base address for OSD region1, based on 16byte. |
| 3:0 | RO | 0x0 | reserved |

**VEPU580_ADR_OSD2**

Address: Operational Base + offset (0x3058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | osd2_addr<br>High 28 bits of base address for OSD region2, based on 16byte. |
| 3:0 | RO | 0x0 | reserved |

**VEPU580_ADR_OSD3**

Address: Operational Base + offset (0x305C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | osd3_addr<br>High 28 bits of base address for OSD region3, based on 16byte. |
| 3:0 | RO | 0x0 | reserved |

**VEPU580_ADR_OSD4**

Address: Operational Base + offset (0x3060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | osd4_addr<br>High 28 bits of base address for OSD region4, based on 16byte. |
| 3:0 | RO | 0x0 | reserved |

**VEPU580_ADR_OSD5**

Address: Operational Base + offset (0x3064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | osd5_addr<br>High 28 bits of base address for OSD region5, based on 16byte. |
| 3:0 | RO | 0x0 | reserved |

**VEPU580_ADR_OSD6**

Address: Operational Base + offset (0x3068)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | osd6_addr<br>High 28 bits of base address for OSD region6, based on 16byte. |
| 3:0 | RO | 0x0 | reserved |

**VEPU580_ADR_OSD7**

Address: Operational Base + offset (0x306C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | osd7_addr<br>High 28 bits of base address for OSD region7, based on 16byte. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RO | 0x0 | reserved |

**VEPU580_OSD_PLT0**

Address: Operational Base + offset (0x3080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | alpha<br>Alpha |
| 23:16 | RW | 0x00 | v<br>V component |
| 15:8 | RW | 0x00 | u<br>U component |
| 7:0 | RW | 0x00 | y<br>Y component |

**VEPU580_OSD_PLT1**

Address: Operational Base + offset (0x3084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | alpha<br>Alpha |
| 23:16 | RW | 0x00 | v<br>V component |
| 15:8 | RW | 0x00 | u<br>U component |
| 7:0 | RW | 0x00 | y<br>Y component |

**VEPU580_OSD_PLT255**

Address: Operational Base + offset (0x347C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | alpha<br>Alpha |
| 23:16 | RW | 0x00 | v<br>V component |
| 15:8 | RW | 0x00 | u<br>U component |
| 7:0 | RW | 0x00 | y<br>Y component |

**VEPU580_ST_BSL_L32**

Address: Operational Base + offset (0x4000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | bs_lgth_l32<br>Low 32 bits of bit stream length for current frame. |

**VEPU580_ST_SSE_BSL**

Rockchip Confidencial

Address: Operational Base + offset (0x4004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | sse_l16<br>Low 16 bits of encoding distortion (SSE). |
| 15:8 | RO | 0x00 | reserved |
| 7:0 | RW | 0x00 | bs_lgth_h8<br>High 8 bits of bit stream length for current frame. |

**VEPU580_ST_SSE_H32**

Address: Operational Base + offset (0x4008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sse_h32<br>High 32 bits of encoding distortion (SSE). |

**VEPU580_ST_SSE_QP**

Address: Operational Base + offset (0x400C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | qp_sum<br>Sum of QP for the encoded frame. |

**VEPU580_ST_SAO**

Address: Operational Base + offset (0x4010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | sao_ynum<br>Number of CTUs whose LUMA component are adjusted by SAO. |
| 15:0 | RW | 0x0000 | sao_cnum<br>Number of CTUs whose CHROMA component are adjusted by SAO. |

**VEPU580_ST_HEAD_BL_L32**

Address: Operational Base + offset (0x4014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | rdo_head_bits<br>Low 32 bits of RDO HeaderBits length. |

**VEPU580_ST_HEAD_RES_BL**

Address: Operational Base + offset (0x4018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | rdo_res_bits_l16<br>Low 16 bits of RDO ResidualBits length. |
| 15:8 | RO | 0x00 | reserved |
| 7:0 | RW | 0x00 | rdo_head_bits_h8<br>High 8 bits of RDO HeaderBits length. |

**VEPU580_ST_RES_BL_H24**

Address: Operational Base + offset (0x401C)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | rdo_res_bits_h24<br>High 24 bits of RDO ResidualBits length. |

**VEPU580_ST_ENC**

Address: Operational Base + offset (0x4020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2 | RW | 0x0 | st_sclr<br>Status of safe clear.<br>1'h0: Safe clear is finished or not started.<br>1'h1: VEPU is performing safe clear. |
| 1:0 | RW | 0x0 | st_enc<br>VEPU working status.<br>2'h0: Idle.<br>2'h1: Working in register conifguration mode.<br>2'h2: Working in link table configuration mode. |

**VEPU580_ST_LKT**

Address: Operational Base + offset (0x4024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | fnum_enc_done<br>Number modulo 256 of frames has been encoded done since link table mode started. |
| 23:16 | RW | 0x00 | fnum_int<br>Number modulo 256 of frames has been encoded since link table mode started, updated only when corresponding link table node send interrupt (VEPU_ENC_PIC_node_int==1). |
| 15:8 | RW | 0x00 | fnum_cfg<br>Number modulo 256 of frames has been configured since link table mode started. |
| 7:0 | RW | 0x00 | fnum_cfg_done<br>Number modulo 256 of frames has been config done since link table mode started. |

**VEPU580_ST_NADR**

Address: Operational Base + offset (0x4028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | node_addr<br>High 28 bits of the address for the processing linke table node. |
| 3:0 | RO | 0x0 | reserved |

**VEPU580_ST_BSB**

Address: Operational Base + offset (0x402C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 30:3 | RW | 0x0000000 | bsbw_addr<br>High 28 bits of bit stream buffer write address. |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | bsbw_ovfl<br>Bit stream buffer full (overflow). |

**VEPU580_ST_BUS**

Address: Operational Base + offset (0x4030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |
| 30:24 | RW | 0x00 | axir_err<br>AXI read error.<br>[6]: LPF read data between tiles(AXI0_ARID==9)<br>[5]: ROI configuration (AXI0_ARID==7)<br>[4]: Down-sampled picture (AXI0_ARID==6)<br>[3]: Co-located Mv (AXI0_ARID==5)<br>[2]: Link table (AXI0_ARID==4)<br>[1]: Reference picture (AXI0_ARID==1,2,3,8)<br>[0]: Video source load (AXI1) |
| 23:16 | RW | 0x00 | axib_err<br>AXI write response error.<br>[7]: LPF write-back data between tiles channel(AXI0_WID==6)<br>[6]: Reconstructed picture channel (AXI0_WID==5)<br>[5]: ME information channel (AXI0_WID==4)<br>[4]: Co-located Mv channel (AXI0_WID==3)<br>[3]: Down-sampled picture channel (AXI0_WID==2)<br>[2]: Bit stream channel (AXI0_WID==1)<br>[1]: Link table node channel (AXI0_WID==0)<br>[0]: External line buffer channel (AXI0_WID==7). |
| 15:8 | RW | 0x00 | axib_ovfl<br>AXI write response outstanding overflow.<br>[7]: LPF write-back data between tiles channel(AXI0_WID==6)<br>[6]: Reconstructed picture channel (AXI0_WID==5)<br>[5]: ME information channel (AXI0_WID==4)<br>[4]: Co-located Mv channel (AXI0_WID==3)<br>[3]: Down-sampled picture channel (AXI0_WID==2)<br>[2]: Bit stream channel (AXI0_WID==1)<br>[1]: Link table node channel (AXI0_WID==0)<br>[0]: External line buffer channel (AXI0_WID==7). |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:0 | RW | 0x00 | axib_idl<br>AXI write response idle.<br>[7]: LPF write-back data between tiles channel(AXI0_WID==6)<br>[6]: Reconstructed picture channel (AXI0_WID==5)<br>[5]: ME information channel (AXI0_WID==4)<br>[4]: Co-located Mv channel (AXI0_WID==3)<br>[3]: Down-sampled picture channel (AXI0_WID==2)<br>[2]: Bit stream channel (AXI0_WID==1)<br>[1]: Link table node channel (AXI0_WID==0)<br>[0]: External line buffer channel (AXI0_WID==7). |

**VEPU580_ST_SNUM**

Address: Operational Base + offset (0x4034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5:0 | RW | 0x00 | sli_num<br>Number for slices has been encoded and not read out (by reading ST_SLEN). |

**VEPU580_ST_SLEN**

Address: Operational Base + offset (0x4038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x00 | reserved |
| 24:0 | RW | 0x0000000 | sli_len<br>Byte length for the earlist encoded slice which has not been read out( by reading VEPU_ST_SLEN). |

**VEPU580_ST_PNUM_P64**

Address: Operational Base + offset (0x4100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16:0 | RW | 0x00000 | pnum_p64<br>Number of 64x64 inter predicted blocks. |

**VEPU580_ST_PNUM_P32**

Address: Operational Base + offset (0x4104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:19 | RO | 0x0000 | reserved |
| 18:0 | RW | 0x00000 | pnum_p32<br>Number of 32x32 inter predicted blocks. |

**VEPU580_ST_PNUM_P16**

Address: Operational Base + offset (0x4108)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 20:0 | RW | 0x000000 | pnum_p16<br>Number of 16x16 inter predicted blocks. |

**VEPU580_ST_PNUM_P8**

Address: Operational Base + offset (0x410C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x000 | reserved |
| 22:0 | RW | 0x000000 | pnum_p8<br>Number of 8x8 inter predicted blocks. |

**VEPU580_ST_PNUM_I32**

Address: Operational Base + offset (0x4110)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:19 | RO | 0x0000 | reserved |
| 18:0 | RW | 0x00000 | pnum_i32<br>Number of 32x32 intra predicted blocks. |

**VEPU580_ST_PNUM_I16**

Address: Operational Base + offset (0x4114)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x000 | reserved |
| 20:0 | RW | 0x000000 | pnum_i16<br>Number of 16x16 intra predicted blocks. |

**VEPU580_ST_PNUM_I8**

Address: Operational Base + offset (0x4118)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x000 | reserved |
| 22:0 | RW | 0x000000 | pnum_i8<br>Number of 8x8 intra predicted blocks. |

**VEPU580_ST_PNUM_I4**

Address: Operational Base + offset (0x411C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x000 | reserved |
| 22:0 | RW | 0x000000 | pnum_i4<br>Number of 4x4 intra predicted blocks. |

**VEPU580_ST_CPLX_TMP**

Address: Operational Base + offset (0x4120)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | madp<br>Mean absolute differences between current encoding and reference frame. |

Rockchip Confidencial

**VEPU580_ST_BNUM_CME**

Address: Operational Base + offset (0x4124)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x000 | reserved |
| 20:0 | RW | 0x000000 | num_ctu<br>Number of CTU (HEVC: 64x64; H.264: 64x16) for CME inter-frame prediction. |

**VEPU580_ST_CPLX_SPT**

Address: Operational Base + offset (0x4128)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | madi<br>Mean absolute differences for current encoding frame. |

**VEPU580_ST_BNUM_B16**

Address: Operational Base + offset (0x412C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x000 | reserved |
| 22:0 | RW | 0x000000 | num_b16<br>Number of valid 16x16 blocks for one frame. |

**VEPU580_ST_CPLX_MAX_B16**

Address: Operational Base + offset (0x4130)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | num_madi_max_b16<br>Number of 16x16 blocks which the value is bigger than sw_aq_thd15. |

**VEPU580_ST_MD_SAD_NUM0**

Address: Operational Base + offset (0x4134)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | md_sad_b16num0<br>Number of 16x16 blocks with cime orginal sad < md_sad_thd0. |

**VEPU580_ST_MD_SAD_NUM1**

Address: Operational Base + offset (0x4138)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | md_sad_b16num1<br>Number of 16x16 blocks with md_sad_thd0 <= cime_orginal_sad < md_sad_thd1. |

**VEPU580_ST_MD_SAD_NUM2**

Address: Operational Base + offset (0x413C)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | md_sad_b16num2<br>Number of 16x16 blocks with md_sad_thd1 <= cime_orginal_sad < md_sad_thd2. |

**VEPU580_ST_MD_SAD_NUM3**

Address: Operational Base + offset (0x4140)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | md_sad_b16num3<br>Number of 16x16 blocks with md_sad_thd2 <= cime_orginal_sad. |

**VEPU580_ST_MADI_NUM0**

Address: Operational Base + offset (0x4144)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | madi_b16num0<br>Number of 16x16 blocks with madi < madi_thd0. |

**VEPU580_ST_MADI_NUM1**

Address: Operational Base + offset (0x4148)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | madi_b16num1<br>Number of 16x16 blocks with madi_thd0 <= madi < madi_thd1. |

**VEPU580_ST_MADI_NUM2**

Address: Operational Base + offset (0x414C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | madi_b16num2<br>Number of 16x16 blocks with madi_thd1 <= madi < madi_thd2. |

**VEPU580_ST_MADI_NUM3**

Address: Operational Base + offset (0x4150)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | madi_b16num3<br>Number of 16x16 blocks with madi_thd2 <= madi. |

**VEPU580_ST_B8_QP0**

Address: Operational Base + offset (0x4200)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp0<br>Number of block8x8s with QP=0. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP1**

Rockchip Confidencial

Address: Operational Base + offset (0x4204)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp1<br>Number of block8x8s with QP=1. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP2**

Address: Operational Base + offset (0x4208)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp2<br>Number of block8x8s with QP=2. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP3**

Address: Operational Base + offset (0x420C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp3<br>Number of block8x8s with QP=3. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP4**

Address: Operational Base + offset (0x4210)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp4<br>Number of block8x8s with QP=4. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP5**

Address: Operational Base + offset (0x4214)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp5<br>Number of block8x8s with QP=5. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP6**

Address: Operational Base + offset (0x4218)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp6<br>Number of block8x8s with QP=6. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP7**

Address: Operational Base + offset (0x421C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp7<br>Number of block8x8s with QP=7. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP8**

Address: Operational Base + offset (0x4220)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp8<br>Number of block8x8s with QP=8. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP9**

Address: Operational Base + offset (0x4224)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp9<br>Number of block8x8s with QP=9. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP10**

Address: Operational Base + offset (0x4228)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp10<br>Number of block8x8s with QP=10. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP11**

Address: Operational Base + offset (0x422C)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp11<br>Number of block8x8s with QP=11. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP12**

Address: Operational Base + offset (0x4230)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp12<br>Number of block8x8s with QP=12. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP13**

Address: Operational Base + offset (0x4234)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp13<br>Number of block8x8s with QP=13. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP14**

Address: Operational Base + offset (0x4238)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp14<br>Number of block8x8s with QP=14. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP15**

Address: Operational Base + offset (0x423C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp15<br>Number of block8x8s with QP=15. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP16**

Address: Operational Base + offset (0x4240)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp16<br>Number of block8x8s with QP=16. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP17**

Address: Operational Base + offset (0x4244)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp17<br>Number of block8x8s with QP=17. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP18**

Address: Operational Base + offset (0x4248)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp18<br>Number of block8x8s with QP=18. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP19**

Address: Operational Base + offset (0x424C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp19<br>Number of block8x8s with QP=19. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP20**

Address: Operational Base + offset (0x4250)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp20<br>Number of block8x8s with QP=20. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP21**

Address: Operational Base + offset (0x4254)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp21<br>Number of block8x8s with QP=21. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP22**

Address: Operational Base + offset (0x4258)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp22<br>Number of block8x8s with QP=22. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP23**

Address: Operational Base + offset (0x425C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp23<br>Number of block8x8s with QP=23. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP24**

Address: Operational Base + offset (0x4260)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp24<br>Number of block8x8s with QP=24. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP25**

Address: Operational Base + offset (0x4264)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp25<br>Number of block8x8s with QP=25. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP26**

Address: Operational Base + offset (0x4268)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp26<br>Number of block8x8s with QP=26. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP27**

Address: Operational Base + offset (0x426C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp27<br>Number of block8x8s with QP=27. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP28**

Address: Operational Base + offset (0x4270)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp28<br>Number of block8x8s with QP=28. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP29**

Address: Operational Base + offset (0x4274)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp29<br>Number of block8x8s with QP=29. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP30**

Address: Operational Base + offset (0x4278)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp30<br>Number of block8x8s with QP=30. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP31**

Address: Operational Base + offset (0x427C)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp31<br>Number of block8x8s with QP=31. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP32**

Address: Operational Base + offset (0x4280)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp32<br>Number of block8x8s with QP=32. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP33**

Address: Operational Base + offset (0x4284)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp33<br>Number of block8x8s with QP=33. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP34**

Address: Operational Base + offset (0x4288)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp34<br>Number of block8x8s with QP=34. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP35**

Address: Operational Base + offset (0x428C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp35<br>Number of block8x8s with QP=35. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP36**

Address: Operational Base + offset (0x4290)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp36<br>Number of block8x8s with QP=36. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP37**

Address: Operational Base + offset (0x4294)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp37<br>Number of block8x8s with QP=37. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP38**

Address: Operational Base + offset (0x4298)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp38<br>Number of block8x8s with QP=38. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP39**

Address: Operational Base + offset (0x429C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp39<br>Number of block8x8s with QP=39. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP40**

Address: Operational Base + offset (0x42A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp40<br>Number of block8x8s with QP=40. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP41**

Address: Operational Base + offset (0x42A4)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp41<br>Number of block8x8s with QP=41. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP42**

Address: Operational Base + offset (0x42A8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp42<br>Number of block8x8s with QP=42. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP43**

Address: Operational Base + offset (0x42AC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp43<br>Number of block8x8s with QP=43. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP44**

Address: Operational Base + offset (0x42B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp44<br>Number of block8x8s with QP=44. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP45**

Address: Operational Base + offset (0x42B4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp45<br>Number of block8x8s with QP=45. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP46**

Address: Operational Base + offset (0x42B8)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp46<br>Number of block8x8s with QP=46. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP47**

Address: Operational Base + offset (0x42BC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp47<br>Number of block8x8s with QP=47. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP48**

Address: Operational Base + offset (0x42C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp48<br>Number of block8x8s with QP=48. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP49**

Address: Operational Base + offset (0x42C4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp49<br>Number of block8x8s with QP=49. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP50**

Address: Operational Base + offset (0x42C8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp50<br>Number of block8x8s with QP=50. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_B8_QP51**

Address: Operational Base + offset (0x42CC)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | b8num_qp51<br>Number of block8x8s with QP=51. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s. |

**VEPU580_ST_SLI_NUM**

Address: Operational Base + offset (0x5028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:15 | RO | 0x00000 | reserved |
| 14:0 | RW | 0x0000 | sli_num<br>Number of slices. |

**VEPU580_ST_LKT_ERR**

Address: Operational Base + offset (0x502C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2:0 | RW | 0x0 | lkt_err<br>Linktable mode error interrupt info:<br>[0]: lkt node error;<br>[1]: lkt command error;<br>[2]: lkt fifo full. |

**VEPU580_MMU0_ADDR**

Address: Operational Base + offset (0xF000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | mmu0_dte_addr<br>DTE address for AXI0 MMU. |

**VEPU580_MMU0_ST**

Address: Operational Base + offset (0xF004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:11 | RO | 0x000000 | reserved |
| 10:6 | RW | 0x00 | mmu_flt_id<br>ID for the last MMU0 fault. |
| 5 | RW | 0x0 | mmu_flt_typ<br>Type of MMU0 fault.<br>1'h0: Read fault.<br>1'h1: Write fault. |
| 4 | RW | 0x0 | mmu_rbly_epty<br>MMU0 replay buffer is empty. |
| 3 | RW | 0x0 | mmu_idl<br>MMU0 idle. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | mmu_stl<br>MMU0 stall. |
| 1 | RW | 0x0 | mmu_flt<br>MMU0 page fault. |
| 0 | RW | 0x0 | mmu_e<br>MMU0 is enabled. |

**VEPU580_MMU0_CMD**

Address: Operational Base + offset (0xF008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2:0 | RW | 0x0 | mmu_cmd<br>MMU0 command.<br>3'h0: MMU mapping enable.<br>3'h1: MMU mapping disable.<br>3'h2: MMU stall enable.<br>3'h3: MMU stall disable.<br>3'h4: Zap(disable) page table cache line.<br>3'h5: Leave fault mode.<br>3'h6: MMU reset. |

**VEPU580_MMU0_PFA**

Address: Operational Base + offset (0xF00C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | mmu_pfa<br>Address of the last page fault. |

**VEPU580_MMU0_ZAP**

Address: Operational Base + offset (0xF010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | mmu_zpa<br>Invalid address for page table cache mapping. |

**VEPU580_MMU0_ERR**

Address: Operational Base + offset (0xF014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | rb_err<br>Read bus error. |
| 0 | RW | 0x0 | pf_err<br>Page fault error. |

**VEPU580_MMU0_INT_CLR**

Address: Operational Base + offset (0xF018)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | rbe_clr<br>Read bus error interrupt clear. |
| 0 | RW | 0x0 | pfe_clr<br>Page fault error interrupt clear. |

**VEPU580_MMU0_INT_MSK**

Address: Operational Base + offset (0xF01C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | rbe_msk<br>Read bus error interrupt mask. |
| 0 | RW | 0x0 | pfe_msk<br>Page fault error interrupt mask. |

**VEPU580_MMU0_INT_STA**

Address: Operational Base + offset (0xF020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | rbe_sta<br>Read bus error interrupt status. |
| 0 | RW | 0x0 | pfe_sta<br>Page fault error interrupt status. |

**VEPU580_MMU0_ACKG**

Address: Operational Base + offset (0xF024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x1 | mmu_ackg<br>Auto clock gating enable. |

**VEPU580_MMU1_ADDR**

Address: Operational Base + offset (0xF040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | mmu1_dte_addr<br>DTE address for AXI1 MMU1. |

**VEPU580_MMU1_ST**

Address: Operational Base + offset (0xF044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:11 | RO | 0x000000 | reserved |
| 10:6 | RW | 0x00 | mmu_flt_id<br>ID for the last MMU fault. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | mmu_flt_typ<br>Type of MMU1 fault.<br>1'h0: Read fault.<br>1'h1: Write fault. |
| 4 | RW | 0x0 | mmu_rbly_epty<br>MMU1 replay buffer is empty. |
| 3 | RW | 0x0 | mmu_idl<br>MMU1 idle. |
| 2 | RW | 0x0 | mmu_stl<br>MMU1 stall. |
| 1 | RW | 0x0 | mmu_flt<br>MMU1 page fault. |
| 0 | RW | 0x0 | mmu_e<br>MMU1 is enabled. |

**VEPU580_MMU1_CMD**

Address: Operational Base + offset (0xF048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2:0 | RW | 0x0 | mmu_cmd<br>MMU1 command.<br>3'h0: MMU mapping enable.<br>3'h1: MMU mapping disable.<br>3'h2: MMU stall enable.<br>3'h3: MMU stall disable.<br>3'h4: Zap(disable) page table cache line.<br>3'h5: Leave fault mode.<br>3'h6: MMU reset. |

**VEPU580_MMU1_PFA**

Address: Operational Base + offset (0xF04C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | mmu_pfa<br>Address of the last page fault. |

**VEPU580_MMU1_ZAP**

Address: Operational Base + offset (0xF050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | mmu_zpa<br>Invalid address for page table cache mapping. |

**VEPU580_MMU1_ERR**

Address: Operational Base + offset (0xF054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | pf_err<br>Page fault error. |

**VEPU580_MMU1_INT_CLR**

Address: Operational Base + offset (0xF058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | rbe_clr<br>Read bus error interrupt clear. |
| 0 | RW | 0x0 | pfe_clr<br>Page fault error interrupt clear. |

**VEPU580_MMU1_INT_MSK**

Address: Operational Base + offset (0xF05C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | rbe_msk<br>Read bus error interrupt mask. |
| 0 | RW | 0x0 | pfe_msk<br>Page fault error interrupt mask. |

**VEPU580_MMU1_INT_STA**

Address: Operational Base + offset (0xF060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | rbe_sta<br>Read bus error interrupt status. |
| 0 | RW | 0x0 | pfe_sta<br>Page fault error interrupt status. |

**VEPU580_MMU1_ACKG**

Address: Operational Base + offset (0xF064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x1 | mmu_ackg<br>Auto clock gating enable. |

Rockchip Confidencial

# 5.6 Application Notes

## 5.6.1 MMU Config Flow

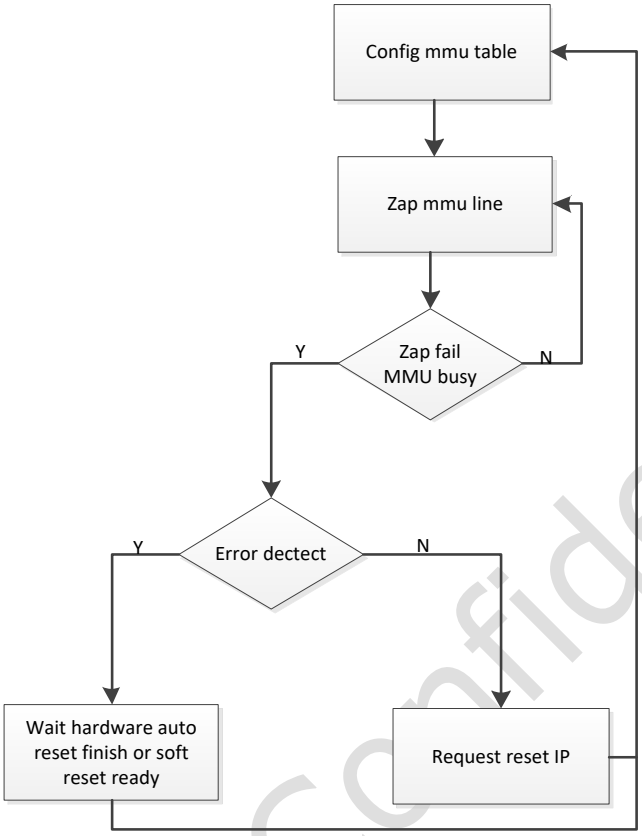



Fig. 5-13 MMU config flow

1. Prepare mmu table to ddr and config DTE address before begin to decoder.
2. If the mmu table have been changed, you will zap one mmu line.
3. If you zap successed, you can continus to zap next line.
4. If you zap fail, maybe some error happened, then you should check if there any error happen when decoding.
5. If some error happen, you should wait reset finish, and then re-start mmu config.
6. If don't have any error find, it will still need to reset, and then re-start mmu config.

## 5.6.2 VDPU121 decoder Configuration flow

1. Prepare the decoder data in the DDR memory, and in decoder other than JPEG decoder, the input stream buffer should at least contain a slice or a frame data, otherwise the decoder will produce an interrupt and show error and then reset itself.
2. Config all the registers will be used. The decoder can support ref buffer mode or cacheable mode, but they can't be both enabled. We can config the swreg57[28], swreg57[29] to enable cache and config the swreg65 to control the ref buffer.
3. You should config VDPU_SWREG57[0] as 1'b1 to enable video decoder. And config VDPU_SWREG41[0] as 1'b1 to enable pp. If pp performed in pipeline with decoder, you should config VDPU_SWREG41[4] as 1'b1 and then config VDPU_SWREG57[0] as 1'b1 to enable decoder and pp.
4. Wait for the frame interrupt, and then check if the frame decoder ready interrupt is right or not, after that, you can get the processed results in the target DDR.
5. Clear all the interrupts, repeat step 2~4 to start a new frame decoder or encoder.

Rockchip Confidencial

### 5.6.3 VDPU381 decoder Configuration Flow

1. Prepare the data in the DDR.
2. Set the H265 general system configuration. such as working mode in RKVDEC.swreg9, in/out endian in RKVDEC.swreg8.
3. Set the picture parameters with RKVDEC.swreg0~ RKVDEC.swreg63.
4. Set the input and output data base address and H265 reference configuration with RKVDEC.swreg64~ RKVDEC.swreg127.
5. If CABAC error detection is desired, set the RKVDEC.swreg21 to enable the corresponding error detection.
6. Set the interrupt configuration with RKVDEC.swreg11 and start the H265 with RKVDEC.swreg10.
7. Wait for the frame interrupt, and then get the processed results in the target DDR.
8. Clear all the interrupts, and repeat Process2~Process8 to start a new frame decoding if the decoding is not finished yet.

### 5.6.4 VDPU381 Link table Pointer mode configuration flow

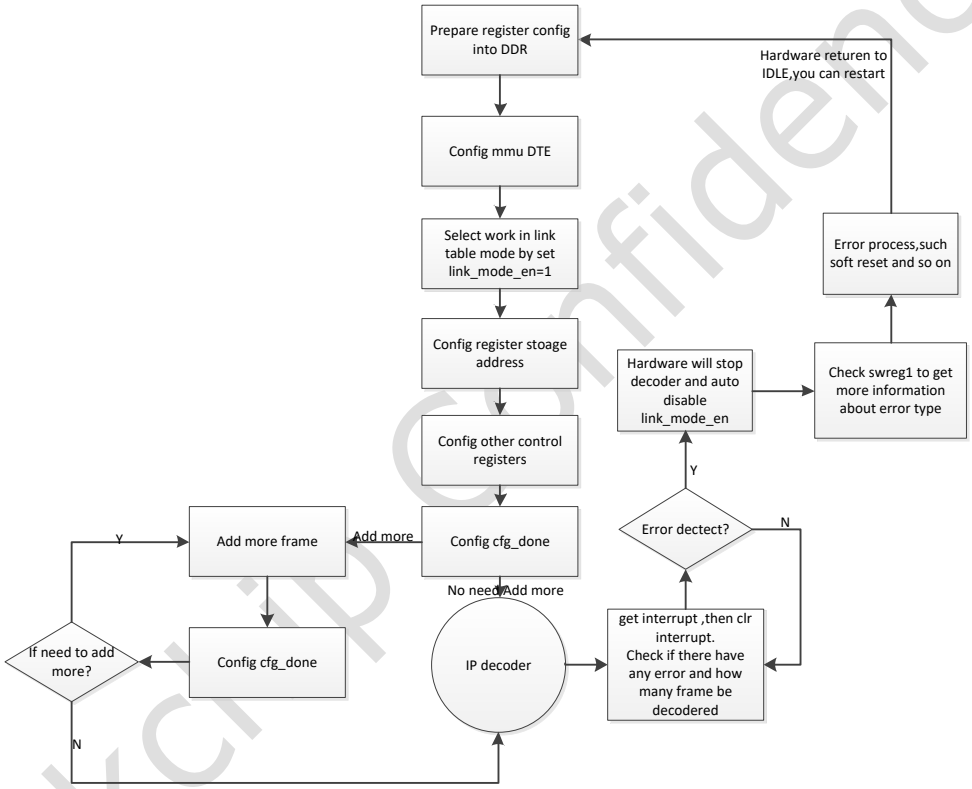



Fig. 5-14 Link table mode work flow

1. Prepare all the register config value into DDR.
2. Config mmu DTE and enable mmu before config link table mode.
3. Config link_mode_irq and other link table mode register. The register is from link_tale_swreg0~link_table_swreg2.
4. Config config_done(set link_table_swreg3[0]=1'b1) to make the link table register configuration effect, after that, hardware will begin to decoder frame by frame.
5. If you need to add more frame, you can use superaddition mode, you can add more frame when decoder at any status.
6. If all config be rdy, you should enable the working flag by config link_mode_en (link_table_swreg6[0]) to 1.
7. If all the frame be decodered, the hardware will hold the working status wait user to process, you can add more frame or set link_mode_en=0(need to set config_done=1'b1) to finish link table mode.
8. When you get interrupt, at first, you should clear the irq, and then, goto check if there

Rockchip Confidencial

have any error by check link_table_swreg4[31]=1'b1 or not. If any error found by hardware, the hardware will disable link table mode and stop decoder until user restart next link table mode. And then you can get more information about error type from normal register swreg225.
9. When you get interrupt, if there doesn't have any error, you may be to check the frame number which have been decoded.
10. Please note that: Any link table register be config, you need to config swreg3[0]=1'b1 to make it effective.

### 5.6.5 VDPU381 CCU configuration flow

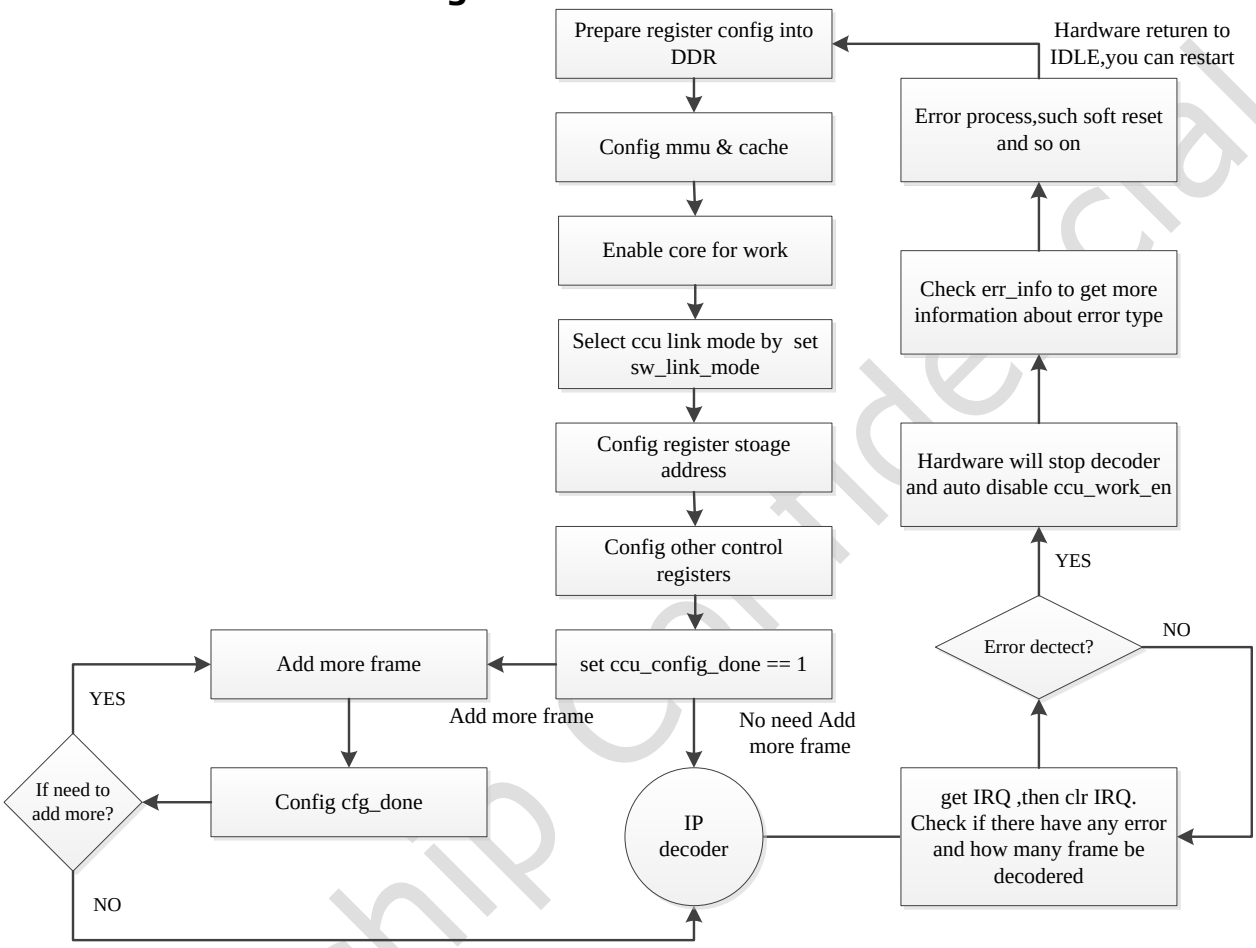



Fig. 5-15 Ccu mode work flow

1. Prepare all the register config value into DDR.
2. Config mmu&cache and enable mmu&cache before config sw_link_mode.
3. Select which cores work control by CCU, and enable these core by set resister (RKVDEC_BASE+0x0000
4. Config ccu_link_mode, ccu_cfg_start_addr and other ccu config resister
5. If all config be rdy, you should enable the working flag by config ccu_work_en set swreg6_ccu_work_en[0]=1'b1
6. Config ccu_config_done(set swreg3_ccu_config_down[0]=1'b1) to enble ccu configuration effect, after that, hardware will begin to decoder frame by frame.
7. If you need to add more frame, you can use superaddition mode, you can add more frame when decoder at any status.
8. If all the frame be decodered, the hardware will hold the working status wait user to process, you can add more frame or set sw_link_mode =0 to finish link table mode.
9.When you get interrupt, at first, you should clear the irq, and then, goto check if there have any error by check swreg21_ccu_core_err_sta[1:0]=2'b0 or not. If any error found by hardware core, the error hardware core will disable itself, and if all selection hareward core error, ccu stop decoder until user restart next ccu_mode.
10. When you get interrupt, if there doesn't have any error, you may be to check the frame

Rockchip Confidential

number which have been decoded.
11. Please note that: Any link table register be config, you need to config ccu_config_done =1'b1 to make it effective.

### 5.6.6 VDPU720 JPEG decoder Configuration flow

1. Prepare the decoder data in the DDR memory, and in decoder other than JPEG decoder, the input stream buffer should at least contain a slice or a frame data, otherwise the decoder will produce an interrupt and show error and then reset itself.
2. Config all the registers will be used.
3. You should config VDPU720_SWREG1[0] as 1'b1 to enable JPEG decoder.
4. Wait for the frame interrupt, and then check if the frame decoder ready interrupt is right or not, after that, you can get the processed results in the target DDR.
5. Clear all the interrupts, repeat step 2~4 to start a new frame decoder or encoder.

### 5.6.7 VEPU121 JPEG encoder Configuration flow

1. Prepare the encoder data in the DDR memory
2. Config all the registers will be used. And please notice that which be list as follows:
   - For encoder: We can configure the registers to control the input picture data format (such as endian and swap), but some input data format are fixed, such as cabac_table data. And the register VEPU_SWREG0~31 are JPEG quantization registers. They are write only registers. When you want to write these registers, you should first set VEPU_SWREG103[0] to 1'b0 and VEPU_SWREG103[5:4] to 2'b10( select JPEG mode).
3. VEPU_SWREG103[0] set to 1'b1 to enable encoder.
4. Wait for the frame interrupt, and then check if the frame decoder ready interrupt is right or not, after that, you can get the processed results in the target DDR.
5. Clear all the interrupts, repeat step 2~5 to start a new frame decoder or encoder.

### 5.6.8 VEPU580 Application Notes

## 5.6.8.1 VEPU Working Mode

VEPU supports two working modes: Register Configuration Mode and Link Table Mode.

In Register Configuration Mode, encoding a frame needs to be divided into three steps: Configure encoding parameters, start encoding, and then wait for enocoding finish. Configuration register and interrupt response time will reduce the encoding speed, but software can adjust the configuration of the next frame in real time accoding to the encoding result of the previous frame.

In Link Table Mode, User can store several frames' configurations in DDR before encoding or add new frames to be encoded while VEPU is processing the previous one. This will save the time of interrupt response and register configuration and let VEPU and software process in parallel.

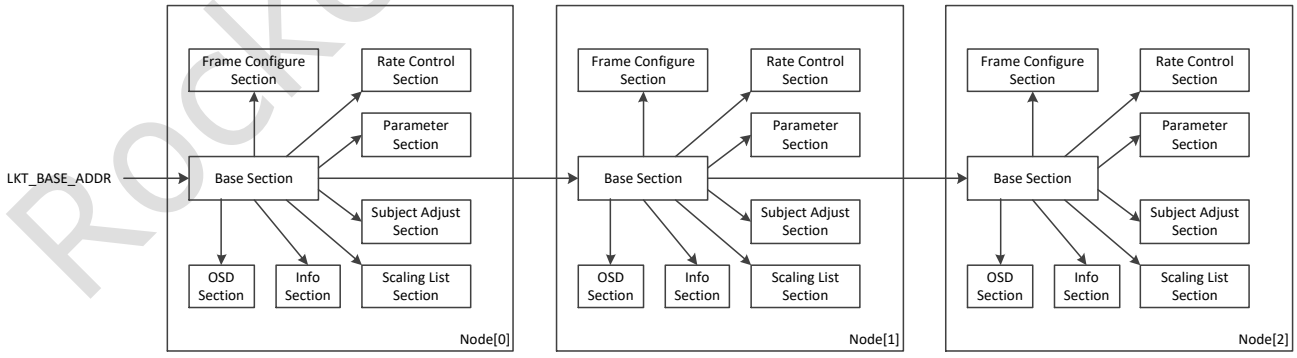



Fig. 5-16 VEPU mode mode

All the configurations for each frame encoding are organized into a Node, and the configurations in each Node are classified into different sections. There're 7 sections for each Nodes:

- Base Section: Contains the information of other sections for current Node and Base Section of the next node, including whether it is valid and the starting address.
- Frame Configure Section: Contains the base frame configurations.

Rockchip Confidential

- Rate Control Section: Contains the configurations for Rate Control.
- Parameter Section: Contains the configurations of optional parameters.
- Subjective Adjust Section: Contains the configurations for subjective Quality Adjustment.
- Scaling List Section: Contains the configurations for User Defined Scaling List.
- OSD Section: Contains the configurations for OSD application.
- Info Section: Contains the encoding informations sent out by VEPU.

Table 5-20 Link Table Node Section mapping and size

| Section | Size | Corresponding Register Address Offset |
|---|---|---|
| Base Section | 48 bytes | 0x0030~0x0058 |
| Frame Configure Section | 384 bytes | 0x0280~0x03f8 |
| Rate Control Section | 224 bytes | 0x1000~0x10e0 |
| Parameter Section | 1504 bytes | 0x1700~0x1cd4 |
| Subjective Adjust Section | 496 bytes | 0x2000~0x21e4 |
| Scaling List Section | 2720 bytes | 0x2200~0x2c98 |
| OSD Section | 1152 bytes | 0x3000~0x347c |
| Info Section | 32 bytes | 0x4000~0x401c |

## 5.6.8.2 VEPU Buffer Allocation

User should allocate the following buffers and informs VEPU before the corresponding frame encoding starts.

- Video Source Buffers: They store the encoded frame data and contain 1 to 3 buffers accoding to different color formats.
- Down Sampled Frame buffers: They store the Down Sampled Frame data for coarse ME, one for current frame if it will be referred while another for the reference frame if current frame contains P slice.
- Reconstruction Frame Buffers: One for current frame if it will be referred by other frames, and another for the reference frame if current frame contains P slice.
- Collocated MV buffers: One for current frame if it will be referred as col-Pic, and another for collocated picture if current frame contains P slice.
- Line Buffer: VEPU uses external space as linebuffer when the width of encoded frame or TILE is greater than 4K.
- TILE Buffer: It contains TILE boundary informations for cross TILE loop filter and frame buffer compression.
- Bitstream Buffer: VEPU stores encoded bitstreams in Bitstream Buffer.
- Motion Information Buffer: VEPU can output ME results for user expanded application.
- Link Table Buffers and ROI Buffers: described in corresponding function chapers.

### 5.6.8.2.1 Video Srouce Buffers

Depending on different video source format, there're up to 3 buffers should be allocated:

- VSBUF0: start address is configured by VEPU_ADR_SRC0
- VSBUF1: start address is configured by VEPU_ADR_SRC1
- VSBUF2: start address is configured by VEPU_ADR_SRC2

Table 5-21 Video Source Buffer allocation

| Color format | Data format | VSBUF0 | VSBUF1 | VSBUF2 |
|---|---|---|---|---|
| YUV444 8bit | YUV444 | ALL | | |
| YUV422 8bit | YUYV | ALL | | |
| | YUV422 Planar | Y | U | V |
| | YUV422 Semi-Planar | Y | U+V | |
| | Frame Buffer Compression | Header | Body | |
| YUV420 8bit | YUV420 Planar | Y | U | V |
| | YUV420 Semi-Planar | Y | U+V | |
| | Frame Buffer Compression | Header | Body | |
| YUV400 8bit | YUV400 | Y | | |
| RGB | ARGB8888 | ALL | | |

Rockchip Confidencial

| Color format | Data format | VSBUF0 | VSBUF1 | VSBUF2 |
|---|---|---|---|---|
| | RGB888 | ALL | | |
| | RGB565 | ALL | | |

#### 5.6.8.2.2 Down Sampled Frame Buffers

Down-sampled frame buffer is for VEPU coarse motion estimation. If current frame will be referred in subsequent encoding, the down-sampled current frame buffer should be allocated with the start address of VEPU_ADR_DSPW. If current frame is P frame, a reference frame buffer should be selected and set the start address to VEPU_ADR_DSPR.
The size of Down Sampled Frame Buffer is:
((VEPU_ENC_RSL.pic_wd8_m1+8)/8) x (VEPU_ENC_RSL.pic_hd8_m1+2)/2) x 64Bytes.
Note that the start address of Down Sampled Frame Buffer should be 1KB aligned.

#### 5.6.8.2.3 Reconstruction Frame Buffers

Reconstruction Frame Buffer store the reconstructed frame data for motion estimation. Because Frame Buffer Compression is implemented, each frame buffer has a head portion and a body portion. VEPU_ADR_RFPW_H and VEPU_ADR_RFPW_B should be set to the head portion and body portion start address of current frame buffer separately.
VEPU_ADR_RFPR_H and VEPU_ADR_RFPR_B should be set to the header portion and body portion start address of reference frame buffer.
The size of head portion of current and reference frame buffer is:
(((VEPU_ENC_RSL.pic_wd8_m1+2)/2) x ((VEPU_ENC_RSL.pic_hd8_m1+1)x2) +15)/16 x 16Bytes.
The size of body portion of current and reference frame buffer is:
((VEPU_ENC_RSL.pic_wd8_m1+2)/2) x ((VEPU_ENC_RSL.pic_hd8_m1+1)x2) x 96Bytes.
Note that the head and body start address should be 4K bytes aligned.

#### 5.6.8.2.4 Collocated Mv Buffers

Collocated Mv Buffers store the col-mv information for HEVC encoding.
When VEPU_ME_CFG.colmv_stor is 1, VEPU will store the col-mv information of current encoding frame into the Collocated Mv Buffer with the start address of VEPU_ADR_CMVW.
When VEPU_ME_CFG.colmv_load is 1, VEPU will load the col-mv information from the Collocated Mv Bufffer with the start address of VEPU_ADR_CMVR.
The size of Collocated Mv Buffer is calculated by the following function:
((VEPU_ENC_RSL.pic_wd8_m1+8)/8) x ((VEPU_ENC_RSL.pic_hd8_m1+8)/8) x 32Bytes.
Note that the start address should be 1K bytes aligned.

#### 5.6.8.2.5 Line Buffer

VEPU uses external memory space as line buffer when the width of encoded TILE or frame is bigger than 4K. The size of Line Buffer is: (VEPU_ENC_RSL.pic_wd8_m1+8)/8) x 480 Bytes.

#### 5.6.8.2.6 TILE Buffer

VEPU stores the Loop Filter and Frame Buffer Compression Information of the right TILE boundary and load it of the left side. Note that VEPU does not store if current TILE is the rightmost one of the frame, and does not load if current TILE is the leftmost one.
The size of TILE Buffer is: (VEPU_TLIE_CFG_HEVC.tile_h_m+1) x 128 x 16 Bytes

#### 5.6.8.2.7 Bitstream Buffer

VEPU stores the encoding result (bit stream) into bit stream buffer.
There are 4 address pointers for one bit stream buffer management:

- VEPU_ADR_BSBT: top address, not included.
- VEPU_ADR_BSBB: bottom address, included.
- VEPU_ADR_BSBR: read address to avoid overlap.
- VEPU_ADR_BSBW: write start address.

Two types of buffer management strategy can be implemented by configuring the four address pointers: single buffer and cyclic buffer management.
Single buffer management allocates a new buffer for each frame while cyclic buffer management allocates a shared cyclic buffer for all encoding frames.
Interrupt VEPU_INT_STUS.bs_ovflr will assert when write address meets read address

Rockchip Confidential

(which indicates buffer is full) and encoding process is paused. Driver should allocated a new buffer to continue current frame encoding by setting new values to the four address pointers or change buffer read address (read out the bitstream before that), and then the encoding process will continue.
Note that VEPU_ADR_BSBW must be configured after the other 3 address pointers.

#### 5.6.8.2.8 Motion Information Buffer

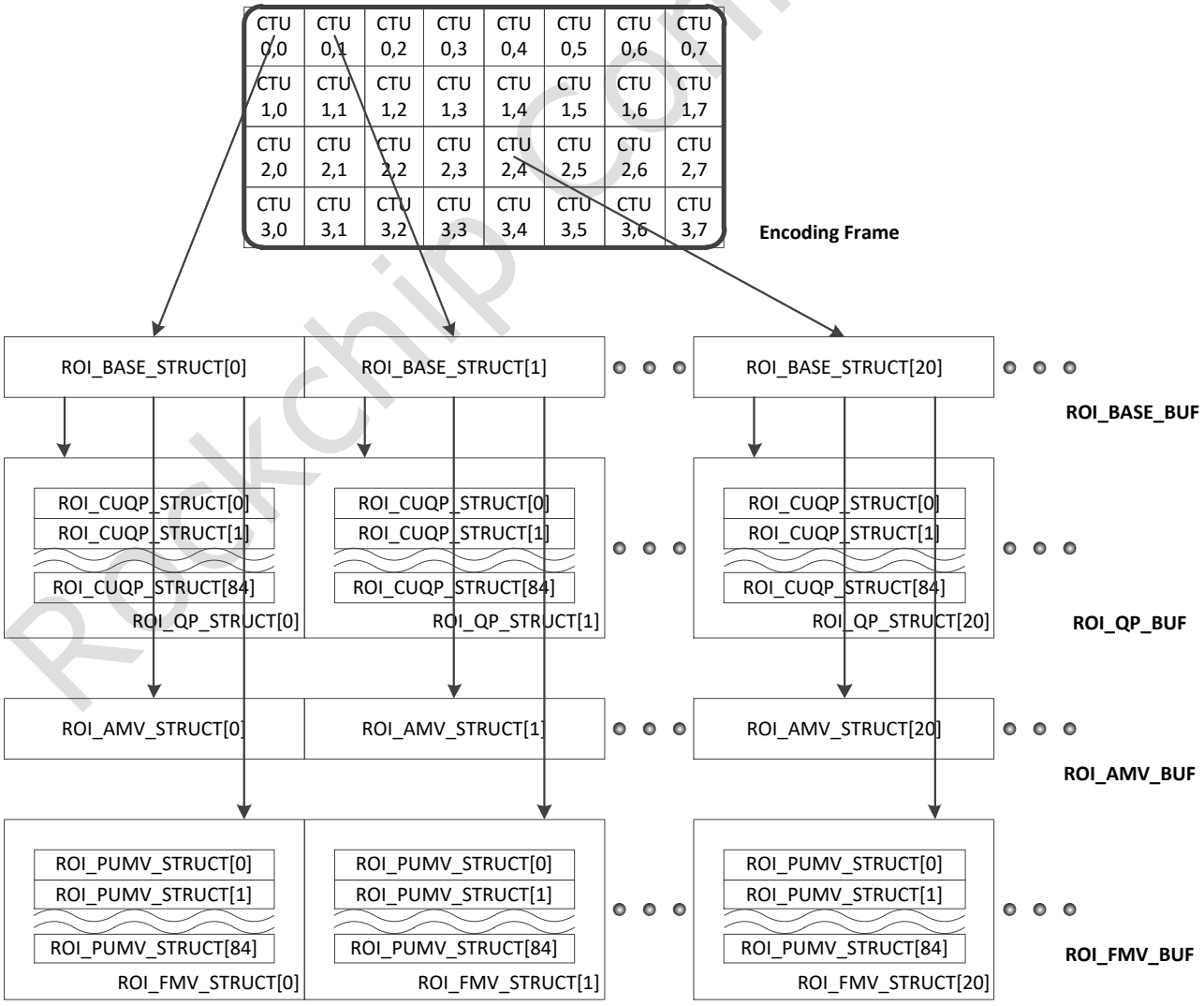
When VEPU_ENC_PIC.mei_stor is 1, the Motion Information Buffer should be allocated with the start address of VEPU_ADR_MEIW. VEPU stores best motion vector and corresponding SAD into this buffer just for user extended extraction.
The size of Motion Information Buffer is:
((VEPU_ENC_RSL.pic_wd8_m1+32)/32) x (VEPU_ENC_RSL.pic_hd8_m1+1)x2) x 64Bytes.

### 5.6.8.3 VEPU ROI Application

VEPU supports block mapping ROI configuration. Each CTU(for HEVC) or MB(for H.264) can be configured by the corresponding structs stored in ROI_BASE_BUF, which is called ROI_BASE_STRUCT.
The ROI_BASE_STRUCT contains the base configuration for each CTU or MB, and the switches for 3 extended ROI configuration structs: ROI_QP_STRUCT, ROI_AMV_STRUCT and ROI_FMV_STRUCT.

#### 5.6.8.3.1 ROI configuration for HEVC

User can specify partition, prediction mode, QP, and Mvs of each CTU though HEVC ROI configuration. The ROI configuration stucts and mapping relations are shown in the figure below.




Rockchip Confidential

Fig. 5-17 HEVC ROI configuration summary

Each CTU has its corresponding ROI_BASE_STRUCT stored in ROI_BASE_BUF, it contains the basic ROI configurations as listed in the table below.

Table 5-22 ROI_BASE_STRUCT for HEVC

| Bit | Field | Description |
|---|---|---|
| 511 | amv_en | Area Mv enable. VEPU will get AMV from ROI_AMV STRUCT if this field is 1. |
| 510 | Reserved | |
| 509:425 | qp_adj[85] | QP adjustment enable. VEPU will get the QP adjustment from ROI_QP_STRUCT if the corresponding bit is 1.<br>qp_adj[85]: adjust the QP of CU64<br>qp_adj[83:80]: adjust the QP of CU32[3~0]<br>qp_adj[79:64]: adjust the QP of CU16[15~0]<br>qp_adj[63:0] : adjust the QP of CU8[63~0] |
| 424:340 | force_split[85] | Force CU split if the corresponding bit is 1.<br>force_split[85]: force split of CU64<br>force_split[83:80]: force split of CU32[3~0]<br>force_split[79:64]: force split of CU16[15~0]<br>force_split[63:0]: reserved |
| 339:170 | force_intra[85][1:0] | CU will be encoded as INTRA if the corresponding section is 1. (each section has 2 bits, values of 2 and 3 are reserved)<br>force_intra[85][1:0]: force intra of CU64<br>force_intra[83:80][1:0]: force intra of CU32[3~0]<br>force_intra[79:64][1:0]: force intra of CU16[15~0]<br>force_intra[63:0][1:0]: force itnra of CU8[63:0] |
| 169:0 | force_inter[85][1:0] | CU will be encoded as INTER with Mv(0,0) if corresponding section is 2; with the Mv assigned by ROI_FMV_STRUCT if corresponding section is 3. (value of 1 is reserved).<br>force_inter[85][1:0]: force inter of CU64<br>force_inter[83:80][1:0]: force inter of CU32[3~0]<br>force_inter[79:64][1:0]: force inter of CU16[15~0]<br>force_inter[63:0][1:0]: force inter of CU8[63~0] |

Each CTU has its corresponding ROI_QP_STRUCT stored in ROI_QP_BUF, it contains 85 CUs' QP configurations which are called ROI_CUQP_STRUCT. Considering address alignment, spaces of 96 ROI_CUQP_STRUCT are allocated for each ROI_QP_STRUCT, and the high 11 of them are reserved. The definition of ROI_CUQP_STRUCT is listed in the table below.

Table 5-23 ROI_CUQP_SRUCT for HEVC

| Bit | Field | Description |
|---|---|---|
| 15 | adj_mode | QP adjustment mode.<br>0: relative QP adjuctment<br>1: absolute QP adjustment |
| 14:8 | qp_value | QP adjustment value. Two's complement. |
| 7:4 | qp_clip | The index of QP clipping, values from 0 to 7. |

Rockchip Confidential

| Bit | Field | Description |
|---|---|---|
| 3:0 | reserved | |

Each CTU has 1 ROI_AMV_STRUCT. It specifies a searh area for Motion Estimation.

Table 5-24 ROI ROI_AMV_STRUCT for HEVC

| Bit | Field | Description |
|---|---|---|
| 31:16 | amv_y | The vertical component of area Mv, with 1 pixel accuracy. |
| 15:0 | amv_x | The horizontal component of area Mv, with 1 pixel accuracy. |

Each CTU has 85 PUs and each PU has its own forced Mv configurations called ROI_PUMV_STRUCT. Considering address alignment, spaces of 96 ROI_PUMV_STRUCT are allocated for each ROI_FMV_STRUCT, and the high 11 of them are reserved. The definition of ROI_PUMV_STRUCT is listed in the table below.

Table 5-25 ROI ROI_PUMV_STRUCT for HEVC

| Bit | Field | Description |
|---|---|---|
| 31:16 | fmv_y | The vertical component of forced Mv, with 1/4 pixel accuracy. |
| 15:0 | fmv_x | The horizontal component of forced Mv, with 1/4 pixel accuracy. |

#### 5.6.8.3.2 ROI configuration for H.264

User can specify partition, encoding mode, QP, and Mvs of each MB though H.264 ROI configuration. The ROI configuration stucts and mapping relations are shown in the figure below. In particular, every 4 MBs share one ROI_AMV_STRUCT and one ROI_FMV_STRUCT.

Rockchip Confidential

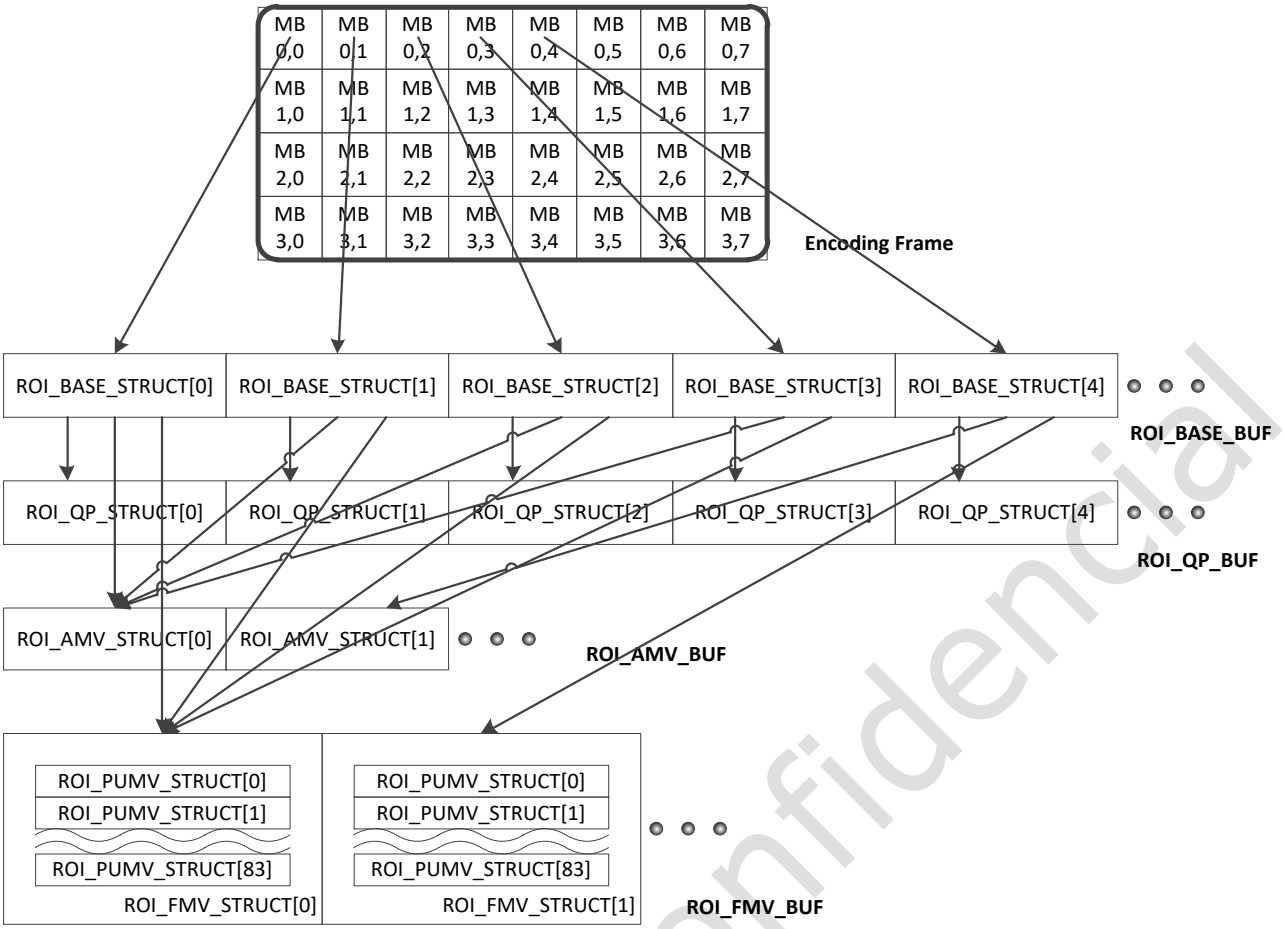



Fig. 5-18 H.264 ROI configuration summary

Each MB has its corresponding ROI_BASE_STRUCT stored in ROI_BASE_BUF, it contains the basic ROI configurations as listed in the table below.

Table 5-26 ROI_BASE_STRUCT for H.264

| Bit | Field | Description |
|---|---|---|
| 63 | amv_en | Area Mv enable. VEPU will get AMV from ROI_AMV_STRUCT if this field is 1. |
| 62 | qp_adj_en | QP adjustment enable. VEPU will load ROI_QP_STRUCT to get the QP adjustment configurations if ithis field is 1. |
| 61 | force_intra | Force Intra. MB will be encoded as INTRA if this field is 1. |
| 60:51 | reserved | |
| 50:42 | mode_mask[8:0] | Mode Mask. Disable the encoding mode if corresponding bit is 1.<br>mode_mask[8]: disable inter4x4<br>mode_mask[7]: disable intra4x4<br>mode_mask[6]: disable intra8x8<br>mode_mask[5]: disable intra16x16<br>mode_mask[4]: disable inter8x8 with T4<br>mode_mask[3]: disable inter8x8 with T8<br>mode_mask[2]: disable inter16x16 with T4<br>mode_mask[1]: disable inter16x16 with T8<br>mode_mask[0]: disable skip mode |

Rockchip Confidencial

| Bit | Field | Description |
|---|---|---|
| 41:0 | force_inter[21][1:0] | Partition will be encoded as INTER with Mv(0,0) if corresponding section is 2; with the Mv assigned by ROI_FMV_STRUCT if corresponding section is 3. (value of 1 is reserved).<br>force_inter[21][1:0]: force inter of 16x16 partition<br>force_inter[20:16][1:0]: force inter of 8x8 partition[3~0]<br>force_inter[15:0][1:0]: force inter of 4x4 partition[15~0] |

Each MB has its corresponding ROI_QP_STRUCT stored in ROI_QP_BUF, it contains the QP Adjustment Configurations as listed in the table below.

Table 5-27 ROI_QP_SRUCT for H.264

| Bit | Field | Description |
|---|---|---|
| 15 | adj_mode | QP adjustment mode.<br>0: relative QP adjuctment<br>1: absolute QP adjustment |
| 14:8 | qp_value | QP adjustment value. Two's complement. |
| 7:4 | qp_clip | The index of QP clipping, values from 0 to 7. |
| 3:0 | reserved | |

Every 4 MBs share one ROI_AMV_STRUCT. It specifies a searh area for Motion Estimation.

Table 5-28 ROI ROI_AMV_STRUCT for H.264

| Bit | Field | Description |
|---|---|---|
| 31:16 | amv_y | The vertical component of area Mv, with 1 pixel accuracy. |
| 15:0 | amv_x | The horizontal component of area Mv, with 1 pixel accuracy. |

Each 4 MBs have 84 PU Forced Mv configurations(each MB has 21 Mvs) called ROI_PUMV_STRUCT. Considering address alignment, spaces of 96 ROI_PUMV_STRUCT are allocated for each ROI_FMV_STRUCT, and the high 12 of them are reserved. The definition of ROI_PUMV_STRUCT is listed in the table below.

Table 5-29 ROI ROI_PUMV_STRUCT for H.264

| Bit | Field | Description |
|---|---|---|
| 31:16 | fmv_y | The vertical component of forced Mv, with 1/4 pixel accuracy. |
| 15:0 | fmv_x | The horizontal component of forced Mv, with 1/4 pixel accuracy. |

Rockchip Confidential

# Chapter 6 General Register Files (GRF)

## 6.1 Overview

The general register file will be used to do static setting by software, which is composed of many registers for system control. The GRF is located at several addresses.

## 6.2 Function Description

The function of general register file is:

- GPIO IOMUX control
- GPIO PAD control
- Common system control
- Record the system state

Table 6-1 GRF Address Mapping Table

| Name | Address Base |
|---|---|
| PMU0_GRF | 0xFD588000 |
| PMU1_GRF | 0xFD58A000 |
| SYS_GRF | 0xFD58C000 |
| BIGCORE0_GRF | 0xFD590000 |
| BIGCORE1_GRF | 0xFD592000 |
| LITCORE_GRF | 0xFD594000 |
| DSU_GRF | 0xFD598000 |
| DDR01_GRF | 0xFD59C000 |
| DDR23_GRF | 0xFD59D000 |
| CENTER_GRF | 0xFD59E000 |
| GPU_GRF | 0xFD5A0000 |
| NPU_GRF | 0xFD5A2000 |
| VOP_GRF | 0xFD5A4000 |
| VO0_GRF | 0xFD5A6000 |
| VO1_GRF | 0xFD5A8000 |
| USB_GRF | 0xFD5AC000 |
| PHP_GRF | 0xFD5B0000 |
| CSIDPHY0_GRF | 0xFD5B4000 |
| CSIDPHY1_GRF | 0xFD5B5000 |
| PCIe3PHY_GRF | 0xFD5B8000 |
| PIPE_PHY0_GRF | 0xFD5BC000 |
| PIPE_PHY1_GRF | 0xFD5C0000 |
| PIPE_PHY2_GRF | 0xFD5C4000 |
| USBDPPHY0_GRF | 0xFD5C8000 |
| USBDPPHY1_GRF | 0xFD5CC000 |
| USB2PHY0_GRF | 0xFD5D0000 |
| USB2PHY1_GRF | 0xFD5D4000 |
| USB2PHY2_GRF | 0xFD5D8000 |
| USB2PHY3_GRF | 0xFD5DC000 |
| HDPTXPHY0_GRF | 0xFD5E0000 |
| HDPTXPHY1_GRF | 0xFD5E4000 |
| MIPICDPHY0_GRF | 0xFD5E8000 |
| MIPICDPHY1_GRF | 0xFD5EC000 |
| PMU1_IOC | 0xFD5F0000 |
| PMU2_IOC | 0xFD5F4000 |
| BUS_IOC | 0xFD5F8000 |
| VCCIO1_4_IOC | 0xFD5F9000 |
| VCCIO3_5_IOC | 0xFD5FA000 |
| VCCIO2_IOC | 0xFD5FB000 |

Rockchip Confidential

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Address Base |
|---|---|
| VCCIO6_IOC | 0xFD5FC000 |
| EMMC_IOC | 0xFD5FD000 |

# 6.3 PMU0_GRF Register Description

## 6.3.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PMU0_GRF_SOC_CON0 | 0x0000 | W | 0x00000001 | System control register 0 |
| PMU0_GRF_SOC_CON1 | 0x0004 | W | 0x00000000 | System control register 1 |
| PMU0_GRF_SOC_CON2 | 0x0008 | W | 0x00001410 | System control register 2 |
| PMU0_GRF_SOC_CON3 | 0x000C | W | 0x00000000 | System control register 3 |
| PMU0_GRF_IO_RET_CON0 | 0x0020 | W | 0x00000000 | IO retention control register 0 |
| PMU0_GRF_IO_RET_CON1 | 0x0024 | W | 0x00000000 | IO retention control register 1 |
| PMU0_GRF_OS_REG8 | 0x0080 | W | 0x00000000 | Operation system register 8 |
| PMU0_GRF_OS_REG9 | 0x0084 | W | 0x00000000 | Operation system register 9 |
| PMU0_GRF_OS_REG10 | 0x0088 | W | 0x00000000 | Operation system register 10 |
| PMU0_GRF_OS_REG11 | 0x008C | W | 0x00000000 | Operation system register 11 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.3.2 Detail Registers Description

**PMU0_GRF_SOC_CON0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | clk_ref_mipi_dcphy0_sel<br>Clock source selection for clk_ref_mipi_dcphy0.<br>1'b0: Select from generated clock<br>1'b1: Select from oscillator |
| 14 | RW | 0x0 | clk_cr_para_sel<br>Clock source selection for clk_cr_para.<br>1'b0: Select from inverter of oscillator<br>1'b1: Select from generated clock |
| 13:11 | RO | 0x0 | reserved |
| 10 | RW | 0x0 | clk_battery_pwrup_gate_en<br>Enable clock gating for battery power up logic.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | resetn_battery_pwrup_hold_ena<br>Enable reset hold for battery power up logic.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | dbclk_gpio0_sel<br>Clock source selection for dbclk_gpio0.<br>1'b0: Select from oscillator<br>1'b1: Select from clk_deepslow |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RO | 0x0 | reserved |
| 6:5 | RW | 0x0 | clk_deepslow_sel<br>Clock source selection for clk_deepslow.<br>2'h0: Select from divider output of oscillator<br>2'h1: Select from external IO clock<br>2'h2: Select from divider output of PMU_PVTM<br>Others: Reserved |
| 4:1 | RO | 0x0 | reserved |
| 0 | RW | 0x1 | pd_pmu1_repair_enable<br>Enable memory repair for PD_PMU1.<br>1'b0: Disable<br>1'b1: Enable |

**PMU0_GRF_SOC_CON1**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | presetn_pmu0_ioc_hold_ena<br>Enable reset hold for presetn_pmu0_ioc.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | presetn_pmu0_grf_hold_ena<br>Enable reset hold for presetn_pmu0_grf.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | presetn_gpio0_hold_ena<br>Enable reset hold for presetn_gpio0.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | dbresetn_gpio0_hold_ena<br>Enable reset hold for dbresetn_gpio0.<br>1'b0: Disable<br>1'b1: Enable |
| 11:0 | RW | 0x000 | pmupvtm_clkout_div<br>Clock divide factor for clock generated by PMU_PVTM |

**PMU0_GRF_SOC_CON2**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:0 | RW | 0x1410 | pmu0_mem_cfg_hdsprf<br>Interface configuration for HDSPRF type memory in PD_PMU0.<br>Bit[0]: TEST1<br>Bit[1]: TEST_RNM<br>Bit[4:2]: RM<br>Bit[5]: WMD<br>Bit[7]: LS<br>Bit[11:10]: WPULSE<br>Bit[13:12]: RA<br>Other bits: Reserved |

**PMU0_GRF_SOC_CON3**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | pmic_int_pol<br>Polarity of PMIC int.<br>1'b0: High active<br>1'b1: Low active |
| 9 | RW | 0x0 | pmic1_sleep_pol<br>Polarity of pmic1_sleep.<br>1'b0: High active<br>1'b1: Low active |
| 8 | RW | 0x0 | pmic0_sleep_pol<br>Polarity of pmic0_sleep.<br>1'b0: High active<br>1'b1: Low active |
| 7:4 | RW | 0x0 | pmic1_sleep_iout_sel<br>Source selection for pmic1_sleep.<br>4'h1: VD_NPU power off request<br>4'h2: VD_GPU power off request<br>4'h3: VD_BIGCORE0 power off request<br>4'h4: VD_BIGCORE1 power off request<br>4'h5: VD_DSU power off request<br>4'h6: VD_VCODEC power off request<br>4'h7: VD_DDR power off request<br>4'h8: Low power mode or deep low power mode<br>4'h9: Chip reset output<br>4'ha: Deep low power mode<br>4'hb: Low power mode<br>Default: Reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RW | 0x0 | pmic0_sleep_iout_sel<br>Source selection for pmic0_sleep.<br>4'h1: VD_NPU power off request<br>4'h2: VD_GPU power off request<br>4'h3: VD_BIGCORE0 power off request<br>4'h4: VD_BIGCORE1 power off request<br>4'h5: VD_DSU power off request<br>4'h6: VD_VCODEC power off request<br>4'h7: VD_DDR power off request<br>4'h8: Low power mode or deep low power mode<br>4'h9: Chip reset output<br>4'ha: Deep low power mode<br>4'hb: Low power mode<br>Default: Reserved |

**PMU0_GRF_IO_RET_CON0**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | pmuio2_ret_ena<br>Enable PMUIO2 retention mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | vccio6_ret_ena<br>Enable VCCIO6 retention mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | vccio5_ret_ena<br>Enable VCCIO5 retention mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | vccio4_ret_ena<br>Enable VCCIO4 retention mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | vccio3_ret_ena<br>Enable VCCIO3 retention mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | vccio2_ret_ena<br>Enable VCCIO2 retention mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | vccio1_ret_ena<br>Enable VCCIO1 retention mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | emmcio_ret_ena<br>Enable EMMCIO retention mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

**PMU0_GRF_IO_RET_CON1**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | pmuio2_ret_sftena<br>Enable PMUIO2 retention mode by software.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | vccio6_ret_sftena<br>Enable VCCIO1 retention mode by software.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | vccio5_ret_sftena<br>Enable VCCIO5 retention mode by software.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | vccio4_ret_sftena<br>Enable VCCIO4 retention mode by software.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | vccio3_ret_sftena<br>Enable VCCIO3 retention mode by software.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | vccio2_ret_sftena<br>Enable VCCIO2 retention mode by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | vccio1_ret_sftena<br>Enable VCCIO1 retention mode by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | emmcio_ret_sftena<br>Enable EMMCIO retention mode by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU0_GRF_OS_REG8**

Address: Operational Base + offset (0x0080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | os_reg<br>Operation system register |

**PMU0_GRF_OS_REG9**

Address: Operational Base + offset (0x0084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | os_reg<br>Operation system register |

**PMU0_GRF_OS_REG10**

Address: Operational Base + offset (0x0088)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | os_reg<br>Operation system register |

**PMU0_GRF_OS_REG11**

Address: Operational Base + offset (0x008C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | os_reg<br>Operation system register |

# 6.4 PMU1_GRF Register Description

## 6.4.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PMU1GRF_SOC_CON0 | 0x0000 | W | 0x00000210 | System control register 0 |
| PMU1GRF_SOC_CON1 | 0x0004 | W | 0x00000000 | System control register 1 |
| PMU1GRF_SOC_CON2 | 0x0008 | W | 0x00000000 | System control register 2 |
| PMU1GRF_SOC_CON3 | 0x000C | W | 0x00000000 | System control register 3 |
| PMU1GRF_SOC_CON4 | 0x0010 | W | 0x0000000F | System control register 4 |
| PMU1GRF_SOC_CON5 | 0x0014 | W | 0x00000000 | System control register 5 |
| PMU1GRF_SOC_CON6 | 0x0018 | W | 0x00000FF0 | System control register 6 |
| PMU1GRF_SOC_CON7 | 0x001C | W | 0x00000000 | System control register 7 |
| PMU1GRF_SOC_CON8 | 0x0020 | W | 0x00000000 | System control register 8 |
| PMU1GRF_SOC_CON9 | 0x0024 | W | 0x00000000 | System control register 9 |
| PMU1GRF_SOC_CON10 | 0x0028 | W | 0x00000FF0 | System control register 10 |
| PMU1GRF_SOC_CON11 | 0x002C | W | 0xFFFFFFFF | System control register 11 |
| PMU1GRF_BIU_CON | 0x0050 | W | 0x00000000 | BIU interface control register |
| PMU1GRF_BIU_STS | 0x0054 | W | 0x00000000 | BIU interface status register |
| PMU1GRF_SOC_STS | 0x0060 | W | 0x00000000 | System status register |
| PMU1GRF_MEM_CON0 | 0x0080 | W | 0x00001410 | Memory interface control register 0 |
| PMU1GRF_MEM_CON1 | 0x0084 | W | 0x00001410 | Memory interface control register 1 |
| PMU1GRF_MEM_CON2 | 0x0088 | W | 0x00008010 | Memory interface control register 2 |
| PMU1GRF_MEM_CON3 | 0x008C | W | 0x00000010 | Memory interface control register 3 |
| PMU1GRF_OS_REG0 | 0x0200 | W | 0x00000000 | Operation system register 0 |
| PMU1GRF_OS_REG1 | 0x0204 | W | 0x00000000 | Operation system register 1 |
| PMU1GRF_OS_REG2 | 0x0208 | W | 0x00000000 | Operation system register 2 |
| PMU1GRF_OS_REG3 | 0x020C | W | 0x00000000 | Operation system register 3 |
| PMU1GRF_OS_REG4 | 0x0210 | W | 0x00000000 | Operation system register 4 |
| PMU1GRF_OS_REG5 | 0x0214 | W | 0x00000000 | Operation system register 5 |
| PMU1GRF_OS_REG6 | 0x0218 | W | 0x00000000 | Operation system register 6 |
| PMU1GRF_OS_REG7 | 0x021C | W | 0x00000000 | Operation system register 7 |
| PMU1GRF_RST_STS | 0x0230 | W | 0x00000000 | System reset status register |
| PMU1GRF_RST_CLR | 0x0234 | W | 0x00000000 | System reset status clear register |
| PMU1GRF_SD_DETECT_CON | 0x0380 | W | 0x00000000 | SDMMC detect control register |
| PMU1GRF_SD_DETECT_STS | 0x0390 | W | 0x00000000 | SDMMC detect status register |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PMU1GRF_SD_DETECT_CLR | 0x03A0 | W | 0x00000000 | SDMMC detect clear register |
| PMU1GRF_SD_DETECT_CNT | 0x03B0 | W | 0x000003E8 | SDMMC detect count register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.4.2 Detail Registers Description

**PMU1GRF_SOC_CON0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | force_jtag_uart<br>Enable GPIO0b5 and GPIO0b6 switch to JTAG function if uart2_rx low last for a specified period of time.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RO | 0x0 | reserved |
| 9 | RW | 0x1 | clk_spll_ls_sel<br>Path selection for SPLL clock output.<br>1'b0: Normal<br>1'b1: Through level-shift cell |
| 8 | RW | 0x0 | sdmmc_det_masked_pin_sel<br>Polarity selection for sdmmc_det_masked_pin.<br>1'b0: Low active<br>1'b1: High active |
| 7 | RO | 0x0 | reserved |
| 6 | RW | 0x0 | i2s1_8ch_mclkout_oe<br>Output enable for i2s1_8ch_mclkout.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | wakeup_timer_sel<br>Select PMU_TIMER interrupt as PMU wake up source.<br>1'b0: PMU_TIMER interrupt 0 selected<br>1'b1: PMU_TIMER interrupt 1 selected |
| 4 | RW | 0x1 | clk_cpll_ls_sel<br>Path selection for CPLL clock output.<br>1'b0: Normal<br>1'b1: Through level-shift cell |
| 3 | RW | 0x0 | pmu_pwr_idlereq<br>Enable PD_PMU1 idle request by software.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | pmuwdt_pause<br>PMU_WDT wdt pause enable. It is used to freeze the watchdog counter during pause mode<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | uart0_cts_inv<br>Polarity selection for uart0_cts.<br>1'b0: Low active<br>1'b1: High active |
| 0 | RW | 0x0 | uart0_rts_inv<br>Polarity selection for uart0_rts.<br>1'b0: Low active<br>1'b1: High active |

**PMU1GRF_SOC_CON1**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | reset_width<br>The chip output reset width, equals to reset_width*256. |

**PMU1GRF_SOC_CON2**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pwr3_sleep_sftena<br>Enable pwr3_sleep by software.<br>1'b0: Disable<br>1'b1: Enable |
| 14:12 | RW | 0x0 | pwr3_sleep_iout_sel<br>Source selection for pwr3_sleep.<br>3'h1: VD_NPU power off request<br>3'h2: VD_GPU power off request<br>3'h3: VD_BIGCORE0 power off request<br>3'h4: VD_BIGCORE1 power off request<br>3'h5: VD_DSU power off request<br>3'h6: VD_VCODEC power off request<br>3'h7: VD_DDR power off request<br>Default: Controlled by pwr3_sleep_sftena |
| 11 | RW | 0x0 | pwr2_sleep_sftena<br>Enable pwr2_sleep by software.<br>1'b0: Disable<br>1'b1: Enable |
| 10:8 | RW | 0x0 | pwr2_sleep_iout_sel<br>Source selection for pwr2_sleep.<br>3'h1: VD_NPU power off request<br>3'h2: VD_GPU power off request<br>3'h3: VD_BIGCORE0 power off request<br>3'h4: VD_BIGCORE1 power off request<br>3'h5: VD_DSU power off request<br>3'h6: VD_VCODEC power off request<br>3'h7: VD_DDR power off request<br>Default: Controlled by pwr2_sleep_sftena |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x0 | pwr1_sleep_sftena<br>Enable pwr1_sleep by software.<br>1'b0: Disable<br>1'b1: Enable |
| 6:4 | RW | 0x0 | pwr1_sleep_iout_sel<br>Source selection for pwr1_sleep.<br>3'h1: VD_NPU power off request<br>3'h2: VD_GPU power off request<br>3'h3: VD_BIGCORE0 power off request<br>3'h4: VD_BIGCORE1 power off request<br>3'h5: VD_DSU power off request<br>3'h6: VD_VCODEC power off request<br>3'h7: VD_DDR power off request<br>Default: Controlled by pwr1_sleep_sftena |
| 3 | RW | 0x0 | pwr0_sleep_sftena<br>Enable pwr0_sleep by software.<br>1'b0: Disable<br>1'b1: Enable |
| 2:0 | RW | 0x0 | pwr0_sleep_iout_sel<br>Source selection for pwr0_sleep.<br>3'h1: VD_NPU power off request<br>3'h2: VD_GPU power off request<br>3'h3: VD_BIGCORE0 power off request<br>3'h4: VD_BIGCORE1 power off request<br>3'h5: VD_DSU power off request<br>3'h6: VD_VCODEC power off request<br>3'h7: VD_DDR power off request<br>Default: Controlled by pwr0_sleep_sftena |

**PMU1GRF_SOC_CON3**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:5 | RO | 0x000 | reserved |
| 4 | RW | 0x0 | wdt_reset_trigger_en<br>Enable WDT reset trigger for DDR fail safe.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | tsadc_shut_reset_trigger_en<br>Enable TSADC shut reset trigger for DDR fail safe.<br>1'b0: Disable<br>1'b1: Enable |

**PMU1GRF_SOC_CON4**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:12 | RW | 0x0 | ddrio_rstiov_enter_ena<br>Enable DDR IO enter retention mode through RSTIOV by hardware for DDR fail safe.<br>1'b0: Disable<br>1'b1: Enable<br>Bit[12] used for DDR channel 0.<br>Bit[13] used for DDR channel 1.<br>Bit[14] used for DDR channel 2.<br>Bit[15] used for DDR channel 3.<br>When RSTIOV mode selected, the corresponding bit of ddrio_ret_enter_ena should be set to 1. |
| 11:4 | RO | 0x00 | reserved |
| 3:0 | RW | 0xf | ddrio_ret_enter_ena<br>Enable DDR IO enter retention mode through RETON/RETOFF or RSTIOV by hardware for DDR fail safe.<br>1'b0: Disable<br>1'b1: Enable<br>Bit[0] used for DDR channel 0.<br>Bit[1] used for DDR channel 1.<br>Bit[2] used for DDR channel 2.<br>Bit[3] used for DDR channel 3. |

**PMU1GRF_SOC_CON5**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | ddrio_rstiov_enter_sftena<br>Enable DDR IO enter retention mode through RSTIOV by software for DDR fail safe.<br>1'b0: Disable<br>1'b1: Enable<br>Bit[12] used for DDR channel 0.<br>Bit[13] used for DDR channel 1.<br>Bit[14] used for DDR channel 2.<br>Bit[15] used for DDR channel 3. |
| 11:4 | RO | 0x00 | reserved |
| 3:0 | RW | 0x0 | ddrio_reton_enter_sftena<br>Enable DDR IO enter retention mode through RETON/RETOFF by software for DDR fail safe.<br>1'b0: Disable<br>1'b1: Enable<br>Bit[0] used for DDR channel 0.<br>Bit[1] used for DDR channel 1.<br>Bit[2] used for DDR channel 2.<br>Bit[3] used for DDR channel 3. |

**PMU1GRF_SOC_CON6**

Address: Operational Base + offset (0x0018)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | upctl_c_sysreq_sftena<br>Enable for DDRC hardware low-power clock request by software.<br>1'b0: Disable<br>1'b1: Enable<br>Bit[11] used for DDR channel 0.<br>Bit[12] used for DDR channel 1.<br>Bit[13] used for DDR channel 2.<br>Bit[14] used for DDR channel 3. |
| 11:8 | RW | 0xf | ddrc_c_gating_en<br>Enable DDRCTRL's core-clock auto clock gating for DDR fail safe.<br>1'b0: Disable<br>1'b1: Enable<br>Bit[8] used for DDR channel 0.<br>Bit[9] used for DDR channel 1.<br>Bit[10] used for DDR channel 2.<br>Bit[11] used for DDR channel 3. |
| 7:4 | RW | 0xf | sref_c_enter_en<br>Enable DDR self-refresh mode for core-clock domain by hardware for DDR fail safe.<br>1'b0: Disable<br>1'b1: Enable<br>Bit[4] used for DDR channel 0.<br>Bit[5] used for DDR channel 1.<br>Bit[6] used for DDR channel 2.<br>Bit[7] used for DDR channel 3. |
| 3:0 | RW | 0x0 | ddrio_ret_exit_ena<br>Enable DDR IO exit retention mode through RETON/RETOFF or RSTIOV by hardware for DDR fail safe.<br>1'b0: Disable<br>1'b1: Enable<br>Bit[0] used for DDR channel 0.<br>Bit[1] used for DDR channel 1.<br>Bit[2] used for DDR channel 2.<br>Bit[3] used for DDR channel 3. |

**PMU1GRF_SOC_CON7**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | presetn_pmu_pwm_hold_ena<br>Enable reset hold for presetn_pmu_pwm.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | presetn_pmu1_biu_hold_ena<br>Enable reset hold for presetn_pmu1_biu.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | presetn_pmu1_ioc_hold_ena<br>Enable reset hold for presetn_pmu1_ioc.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | presetn_pmu1_grf_hold_ena<br>Enable reset hold for presetn_pmu1_grf.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | presetn_i2c0_hold_ena<br>Enable reset hold for presetn_i2c0.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | presetn_pmu1_cru_hold_ena<br>Enable reset hold for presetn_pmu1_cru.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | mresetn_mipi_dcphy1_hold_ena<br>Enable reset hold for mresetn_mipi_dcphy1.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | mresetn_mipi_dcphy0_hold_ena<br>Enable reset hold for mresetn_mipi_dcphy0.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | mresetn_i2s1_8ch_tx_hold_ena<br>Enable reset hold for mresetn_i2s1_8ch_tx.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | mresetn_i2s1_8ch_rx_hold_ena<br>Enable reset hold for mresetn_i2s1_8ch_rx.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | hresetn_vad_hold_ena<br>Enable reset hold for hresetn_vad.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | hresetn_pmu_mcu_biu_hold_ena<br>Enable reset hold for hresetn_pmu_mcu_biu.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | hresetn_pmu_biu_hold_ena<br>Enable reset hold for hresetn_pmu_biu.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | hresetn_pdm0_hold_ena<br>Enable reset hold for hresetn_pdm0.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | hresetn_i2s1_8ch_hold_ena<br>Enable reset hold for hresetn_i2s1_8ch.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | fresetn_pmu_mcu_hold_ena<br>Enable reset hold for fresetn_pmu_mcu.<br>1'b0: Disable<br>1'b1: Enable |

**PMU1GRF_SOC_CON8**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | resetn_pdm0_hold_ena<br>Enable reset hold for resetn_pdm0.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | resetn_otgphy_u3_1_hold_ena<br>Enable reset hold for resetn_otgphy_u3_1.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | resetn_otgphy_u3_0_hold_ena<br>Enable reset hold for resetn_otgphy_u3_0.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | resetn_otgphy_u2_1_hold_ena<br>Enable reset hold for resetn_otgphy_u2_1.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | resetn_otgphy_u2_0_hold_ena<br>Enable reset hold for resetn_otgphy_u2_0.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | resetn_i2c0_hold_ena<br>Enable reset hold for resetn_i2c0.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | resetn_hdptx1_lane_hold_ena<br>Enable reset hold for resetn_hdptx1_lane.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | resetn_hdptx1_init_hold_ena<br>Enable reset hold for resetn_hdptx1_init.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | resetn_hdptx1_cmn_hold_ena<br>Enable reset hold for resetn_hdptx1_cmn.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | resetn_hdptx0_lane_hold_ena<br>Enable reset hold for resetn_hdptx0_lane.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | resetn_hdptx0_init_hold_ena<br>Enable reset hold for resetn_hdptx0_init.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | resetn_hdptx0_cmn_hold_ena<br>Enable reset hold for resetn_hdptx0_cmn.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | resetn_ddr_fail_safe_hold_ena<br>Enable reset hold for resetn_ddr_fail_safe.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | presetn_uart0_hold_ena<br>Enable reset hold for presetn_uart0.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | presetn_pmu_wdt_hold_ena<br>Enable reset hold for presetn_pmu_wdt.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | presetn_pmu_timer_hold_ena<br>Enable reset hold for presetn_pmu_timer.<br>1'b0: Disable<br>1'b1: Enable |

**PMU1GRF_SOC_CON9**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | tresetn_pmu_wdt_hold_ena<br>Enable reset hold for tresetn_pmu_wdt.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | tresetn_pmu_mcu_jtag_hold_ena<br>Enable reset hold for tresetn_pmu_mcu_jtag.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | sresetn_uart0_hold_ena<br>Enable reset hold for sresetn_uart0.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | sresetn_mipi_dcphy1_hold_ena<br>Enable reset hold for sresetn_mipi_dcphy1.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | sresetn_mipi_dcphy0_hold_ena<br>Enable reset hold for sresetn_mipi_dcphy0.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | resetn_pmu_timer1_hold_ena<br>Enable reset hold for resetn_pmu_timer1.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | resetn_pmu_timer0_hold_ena<br>Enable reset hold for resetn_pmu_timer0.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | resetn_pmu_pwm_hold_ena<br>Enable reset hold for resetn_pmu_pwm.<br>1'b0: Disable<br>1'b1: Enable |

**PMU1GRF_SOC_CON10**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | upctl_a_sysreq_sftena<br>Enable for AXI hardware low-power clock request by software.<br>1'b0: Disable<br>1'b1: Enable |
| 11:8 | RW | 0xf | ddrc_a_gating_en<br>Enable DDRCTRL's AXI-clock auto clock gating for DDR fail safe.<br>1'b0: Disable<br>1'b1: Enable |
| 7:4 | RW | 0xf | sref_a_enter_en<br>Enable DDR self-refresh mode for AXI-clock domain by hardware for DDR fail safe.<br>1'b0: Disable<br>1'b1: Enable |
| 3:0 | RO | 0x0 | reserved |

**PMU1GRF_SOC_CON11**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0xffffffff | uart2rx_low_dly<br>uart2_rx low count. |

**PMU1GRF_BIU_CON**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | idle_req_top_sftena<br>Enable sending idle request to BIU_TOP by software.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | idle_req_bus_sftena<br>Enable sending idle request to BIU_BUS by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1:0 | RO | 0x0 | reserved |

**PMU1GRF_BIU_STS**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6 | RO | 0x0 | idle_ack_top<br>BIU_TOP idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 5 | RO | 0x0 | idle_top<br>BIU_TOP idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 4 | RO | 0x0 | idle_ack_bus<br>BIU_BUS idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 3 | RO | 0x0 | idle_bus<br>BIU_BUS idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 2 | RO | 0x0 | pmu_biu_pwractive<br>Power active status for BIU_PMU.<br>1'b0: Inactive<br>1'b1: Active |
| 1 | RO | 0x0 | vad_nopendingtrans<br>No pending transfer status for VAD.<br>1'b0: Inactive<br>1'b1: Active |
| 0 | RO | 0x0 | pmu_mcu_nopendingtrans<br>No pending transfer status for PMU_MCU.<br>1'b0: Inactive<br>1'b1: Active |

**PMU1GRF_SOC_STS**

Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RO | 0x00000 | reserved |
| 13 | RO | 0x0 | pmic_int<br>PMIC interrupt status.<br>1'b0: Inactive<br>1'b1: Active |
| 12 | RO | 0x0 | pmu1sgrf_crc_chk_rst_req<br>PMU1SGRF CRC check reset status. It is set to 1 if CRC check error.<br>1'b0: Inactive<br>1'b1: Active |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11 | RO | 0x0 | pmu0sgrf_crc_chk_rst_req<br>PMU0SGRF CRC check reset status. It is set to 1 if CRC check error.<br>1'b0: Inactive<br>1'b1: Active |
| 10 | RO | 0x0 | pmu_mcu_deepsleep<br>PMU_MCU deep sleep status.<br>1'b0: Inactive<br>1'b1: Active |
| 9 | RO | 0x0 | pmu_mcu_sleeping<br>PMU_MCU sleeping status.<br>1'b0: Inactive<br>1'b1: Active |
| 8 | RO | 0x0 | pmu_mcu_lockup<br>PMU_MCU lock up status.<br>1'b0: Inactive<br>1'b1: Active |
| 7 | RO | 0x0 | pmu_mcu_halted<br>PMU_MCU halt status.<br>1'b0: Inactive<br>1'b1: Active |
| 6 | RO | 0x0 | pmu_mcu_cache_flush_ack<br>PMU_MCU cache flush acknowledge.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 5 | RO | 0x0 | pmu_mcu_txev<br>PMU_MCU TXEV status.<br>1'b0: Inactive<br>1'b1: Active |
| 4 | RO | 0x0 | vad_dig_mic_sts<br>VAD digital mic status.<br>1'b0: Inactive<br>1'b1: Active |
| 3 | RO | 0x0 | pmu_timer1_en_status<br>PMU_TIMER1 enable status.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RO | 0x0 | pmu_timer0_en_status<br>PMU_TIMER0 enable status.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RO | 0x0 | pmu_wdt_sys_rstn<br>PMU_WDT reset request status.<br>1'b0: Active<br>1'b1: Inactive |
| 0 | RO | 0x0 | osc_chk_rst_req<br>OSC_CHK reset request status.<br>1'b0: Inactive<br>1'b1: Active |

**PMU1GRF_MEM_CON0**

Address: Operational Base + offset (0x0080)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x1410 | pmu1_mem_cfg_hdspra<br>Interface configuration for HDSPRA type memory in PD_PMU1.<br>Bit[0]: TEST1<br>Bit[1]: TEST_RNM<br>Bit[4:2]: RM<br>Bit[5]: WMD<br>Bit[7]: LS<br>Bit[11:10]: WPULSE<br>Bit[13:12]: RA<br>Other bits: Reserved |

**PMU1GRF_MEM_CON1**

Address: Operational Base + offset (0x0084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x1410 | mem_cfg_hdsprf<br>Interface configuration for HDSPRF type memory in PD_PMU1.<br>Bit[0]: TEST1<br>Bit[1]: TEST_RNM<br>Bit[4:2]: RM<br>Bit[5]: WMD<br>Bit[7]: LS<br>Bit[11:10]: WPULSE<br>Bit[13:12]: RA<br>Other bits: Reserved |

**PMU1GRF_MEM_CON2**

Address: Operational Base + offset (0x0088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x8010 | mem_cfg_hsdpra_l16<br>Lower 16 bits of interface configuration for HSDPRA type memory.<br>Bit[0]: TEST1A<br>Bit[1]: TEST_RNMA<br>Bit[4:2]: RMA<br>Bit[5]: WMDA<br>Bit[7]: LS<br>Bit[11:10]: WPULSE<br>Bit[13:12]: RA<br>Bit[15:14]: WA |

**PMU1GRF_MEM_CON3**

Address: Operational Base + offset (0x008C)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x010 | mem_cfg_hsdpra_h9<br>Higher 9 bits of interface configuration for HSDPRA type memory.<br>Bit[0]: TEST1B<br>Bit[1]: TEST_RNMB<br>Bit[4:2]: RMB<br>Bit[5]: WMDB<br>Other bits: Reserved |

**PMU1GRF_OS_REG0**

Address: Operational Base + offset (0x0200)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | os_reg<br>Operation system register |

**PMU1GRF_OS_REG1**

Address: Operational Base + offset (0x0204)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | os_reg<br>Operation system register |

**PMU1GRF_OS_REG2**

Address: Operational Base + offset (0x0208)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | os_reg<br>Operation system register |

**PMU1GRF_OS_REG3**

Address: Operational Base + offset (0x020C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | os_reg<br>Operation system register |

**PMU1GRF_OS_REG4**

Address: Operational Base + offset (0x0210)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | os_reg<br>Operation system register |

**PMU1GRF_OS_REG5**

Address: Operational Base + offset (0x0214)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | os_reg<br>Operation system register |

**PMU1GRF_OS_REG6**

Address: Operational Base + offset (0x0218)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | os_reg<br>Operation system register |

Rockchip Confidencial

**PMU1GRF_OS_REG7**

Address: Operational Base + offset (0x021C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | os_reg<br>Operation system register |

**PMU1GRF_RST_STS**

Address: Operational Base + offset (0x0230)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6 | RO | 0x0 | ddrio_ch3_ret_failsafe_sts<br>DDRIO channel 3 retention status under DDR fail safe condition.<br>1'b0: Inactive<br>1'b1: Active |
| 5 | RO | 0x0 | ddrio_ch2_ret_failsafe_sts<br>DDRIO channel 2 retention status under DDR fail safe condition.<br>1'b0: Inactive<br>1'b1: Active |
| 4 | RO | 0x0 | ddrio_ch1_ret_failsafe_sts<br>DDRIO channel 1 retention status under DDR fail safe condition.<br>1'b0: Inactive<br>1'b1: Active |
| 3 | RO | 0x0 | ddrio_ch0_ret_failsafe_sts<br>DDRIO channel 0 retention status under DDR fail safe condition.<br>1'b0: Inactive<br>1'b1: Active |
| 2 | RO | 0x0 | tsadc_shut_sts<br>TSADC shut status.<br>1'b0: Inactive<br>1'b1: Active |
| 1 | RO | 0x0 | wdt_reset_sts<br>WDT reset status.<br>1'b0: Inactive<br>1'b1: Active |
| 0 | RO | 0x0 | first_reset_sts<br>First reset status.<br>1'b0: Inactive<br>1'b1: Active |

**PMU1GRF_RST_CLR**

Address: Operational Base + offset (0x0234)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6 | WO | 0x0 | ddrio_ch3_ret_failsafe_clr<br>Enable clear for DDRIO channel 3 retention status under DDR fail safe condition.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | WO | 0x0 | ddrio_ch2_ret_failsafe_clr<br>Enable clear for DDRIO channel 2 retention status under DDR fail safe condition.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | WO | 0x0 | ddrio_ch1_ret_failsafe_clr<br>Enable clear for DDRIO channel 1 retention status under DDR fail safe condition.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | WO | 0x0 | ddrio_ch0_ret_failsafe_clr<br>Enable clear for DDRIO channel 0 retention status under DDR fail safe condition.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | WO | 0x0 | tsadc_reset_clr<br>Enable clear for TSADC shut status.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | WO | 0x0 | wdt_reset_clr<br>Enable clear for WDT reset status.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | WO | 0x0 | first_reset_clr<br>Enable clear for first reset status.<br>1'b0: Disable<br>1'b1: Enable |

**PMU1GRF_SD_DETECT_CON**

Address: Operational Base + offset (0x0380)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | sd_detect_fall_en<br>Enable SDMMC detect pin falling edge interrupt.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | sd_detect_rise_en<br>Enable SDMMC detect pin rising edge interrupt.<br>1'b0: Disable<br>1'b1: Enable |

**PMU1GRF_SD_DETECT_STS**

Address: Operational Base + offset (0x0390)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RO | 0x0 | sd_detect_fall_sts<br>SDMMC detect pin falling edge status.<br>1'b0: Inactive<br>1'b1: Active |
| 0 | RO | 0x0 | sd_detect_rise_sts<br>SDMMC detect pin rising edge status.<br>1'b0: Inactive<br>1'b1: Active |

**PMU1GRF_SD_DETECT_CLR**

Address: Operational Base + offset (0x03A0)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | WO | 0x0 | sd_detect_fall_clr<br>Enable clear for SDMMC detect pin falling edge interrupt.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | WO | 0x0 | sd_detect_rise_clr<br>Enable clear for SDMMC detect pin rising edge interrupt.<br>1'b0: Disable<br>1'b1: Enable |

**PMU1GRF_SD_DETECT_CNT**

Address: Operational Base + offset (0x03B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x0003e8 | sd_det_cnt<br>SDMMC detect count |

# 6.5 SYS_GRF Register Description

## 6.5.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| SYS_GRF_WDT_CON0 | 0x0000 | W | 0x00000000 | WDT Control Register |
| SYS_GRF_UART_CON0 | 0x0010 | W | 0x00000000 | UART Control Register 0 |
| SYS_GRF_UART_CON1 | 0x0014 | W | 0x00000000 | UART Control Register 1 |
| SYS_GRF_GIC_CON0 | 0x00C0 | W | 0x00000002 | GIC Control Register |
| SYS_GRF_MEMCFG_CON0 | 0x0200 | W | 0x00001410 | Memory Configuration Register 0 |
| SYS_GRF_MEMCFG_CON1 | 0x0204 | W | 0x00008010 | Memory Configuration Register 1 |
| SYS_GRF_MEMCFG_CON2 | 0x0208 | W | 0x00000000 | Memory Configuration Register 2 |
| SYS_GRF_MEMCFG_CON3 | 0x020C | W | 0x00000010 | Memory Configuration Register 3 |
| SYS_GRF_MEMCFG_CON4 | 0x0210 | W | 0x00000011 | Memory Configuration Register 4 |
| SYS_GRF_MEMCFG_CON5 | 0x0214 | W | 0x00001410 | Memory Configuration Register 5 |
| SYS_GRF_MEMCFG_CON6 | 0x0218 | W | 0x00008010 | Memory Configuration Register 6 |
| SYS_GRF_MEMCFG_CON7 | 0x021C | W | 0x00000000 | Memory Configuration Register 7 |
| SYS_GRF_MEMCFG_CON8 | 0x0220 | W | 0x00000010 | Memory Configuration Register 8 |
| SYS_GRF_MEMCFG_CON9 | 0x0224 | W | 0x00000011 | Memory Configuration Register 9 |
| SYS_GRF_MEMCFG_CON10 | 0x0228 | W | 0x00001410 | Memory Configuration Register 10 |
| SYS_GRF_MEMCFG_CON11 | 0x022C | W | 0x00008010 | Memory Configuration Register 11 |
| SYS_GRF_MEMCFG_CON12 | 0x0230 | W | 0x00000000 | Memory Configuration Register 12 |
| SYS_GRF_MEMCFG_CON13 | 0x0234 | W | 0x00000010 | Memory Configuration Register 13 |
| SYS_GRF_MEMCFG_CON14 | 0x0238 | W | 0x00000011 | Memory Configuration Register 14 |
| SYS_GRF_MEMCFG_CON15 | 0x023C | W | 0x00000008 | Memory Configuration Register 15 |

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| SYS_GRF_MEMCFG_CON16 | 0x0240 | W | 0x00000010 | Memory Configuration Register 16 |
| SYS_GRF_MEMCFG_CON17 | 0x0244 | W | 0x00000011 | Memory Configuration Register 17 |
| SYS_GRF_MEMCFG_CON18 | 0x0248 | W | 0x00008010 | Memory Configuration Register 18 |
| SYS_GRF_MEMCFG_CON19 | 0x024C | W | 0x00001410 | Memory Configuration Register 19 |
| SYS_GRF_MEMCFG_CON20 | 0x0250 | W | 0x00000008 | Memory Configuration Register 20 |
| SYS_GRF_MEMCFG_CON21 | 0x0254 | W | 0x00001410 | Memory Configuration Register 21 |
| SYS_GRF_MEMCFG_CON22 | 0x0258 | W | 0x00000010 | Memory Configuration Register 22 |
| SYS_GRF_MEMCFG_CON23 | 0x025C | W | 0x00000011 | Memory Configuration Register 23 |
| SYS_GRF_MEMCFG_CON24 | 0x0260 | W | 0x00002010 | Memory Configuration Register 24 |
| SYS_GRF_MEMCFG_CON26 | 0x0268 | W | 0x00008010 | Memory Configuration Register 26 |
| SYS_GRF_MEMCFG_CON27 | 0x026C | W | 0x00000010 | Memory Configuration Register 27 |
| SYS_GRF_MEMCFG_CON28 | 0x0270 | W | 0x00001410 | Memory Configuration Register 28 |
| SYS_GRF_MEMCFG_CON29 | 0x0274 | W | 0x00000010 | Memory Configuration Register 29 |
| SYS_GRF_MEMCFG_CON30 | 0x0278 | W | 0x00000011 | Memory Configuration Register 30 |
| SYS_GRF_MEMCFG_CON31 | 0x027C | W | 0x00002010 | Memory Configuration Register 31 |
| SYS_GRF_SOC_CON1 | 0x0304 | W | 0x00000000 | System Control Register 1 |
| SYS_GRF_SOC_CON2 | 0x0308 | W | 0x00008000 | System Control Register 2 |
| SYS_GRF_SOC_CON3 | 0x030C | W | 0x00000000 | System Control Register 3 |
| SYS_GRF_SOC_CON6 | 0x0318 | W | 0x00004600 | System Control Register 6 |
| SYS_GRF_SOC_CON7 | 0x031C | W | 0x00000A00 | System Control Register 7 |
| SYS_GRF_SOC_CON8 | 0x0320 | W | 0x00000000 | System Control Register 8 |
| SYS_GRF_SOC_CON9 | 0x0324 | W | 0x00000000 | System Control Register 9 |
| SYS_GRF_SOC_CON10 | 0x0328 | W | 0x00000300 | System Control Register 10 |
| SYS_GRF_SOC_CON11 | 0x032C | W | 0x00092820 | System Control Register 11 |
| SYS_GRF_SOC_CON12 | 0x0330 | W | 0x00000000 | System Control Register 12 |
| SYS_GRF_SOC_CON13 | 0x0334 | W | 0x00000000 | System Control Register 13 |
| SYS_GRF_SOC_STATUS0 | 0x0380 | W | 0x00000000 | System Status Register 0 |
| SYS_GRF_SOC_STATUS1 | 0x0384 | W | 0x00000000 | System Status Register 1 |
| SYS_GRF_SOC_STATUS2 | 0x0388 | W | 0x00000000 | System Status Register 2 |
| SYS_GRF_SOC_STATUS3 | 0x038C | W | 0x00000000 | System Status Register 3 |
| SYS_GRF_OTP_KEY08 | 0x0500 | W | 0x00000000 | OTP Status Register 8 |
| SYS_GRF_OTP_KEY0D | 0x0504 | W | 0x00000000 | OTP Status Register 13 |
| SYS_GRF_OTP_KEY0E | 0x0508 | W | 0x00000000 | OTP Status Register 14 |
| SYS_GRF_CHIP_ID | 0x0600 | W | 0x00003588 | Chip ID Register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

### 6.5.2 Detail Registers Description

Rockchip Confidential

**SYS_GRF_WDT_CON0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | wdtns_pause_en<br>wdt pause enable.<br>Used to freeze the watchdog counter during pause mode.<br>High active. |

**SYS_GRF_UART_CON0**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | uart9_cts_inv<br>Polarity selection for uart9_cts.<br>1'b0: Low active<br>1'b1: High active |
| 7 | RW | 0x0 | uart8_cts_inv<br>Polarity selection for uart8_cts.<br>1'b0: Low active<br>1'b1: High active |
| 6 | RW | 0x0 | uart7_cts_inv<br>Polarity selection for uart7_cts.<br>1'b0: Low active<br>1'b1: High active |
| 5 | RW | 0x0 | uart6_cts_inv<br>Polarity selection for uart6_cts.<br>1'b0: Low active<br>1'b1: High active |
| 4 | RW | 0x0 | uart5_cts_inv<br>Polarity selection for uart5_cts.<br>1'b0: Low active<br>1'b1: High active |
| 3 | RW | 0x0 | uart4_cts_inv<br>Polarity selection for uart4_cts.<br>1'b0: Low active<br>1'b1: High active |
| 2 | RW | 0x0 | uart3_cts_inv<br>Polarity selection for uart3_cts.<br>1'b0: Low active<br>1'b1: High active |
| 1 | RW | 0x0 | uart2_cts_inv<br>Polarity selection for uart2_cts.<br>1'b0: Low active<br>1'b1: High active |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | uart1_cts_inv<br>Polarity selection for uart1_cts.<br>1'b0: Low active<br>1'b1: High active |

**SYS_GRF_UART_CON1**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | uart9_rts_inv<br>Polarity selection for uart9_rts.<br>1'b0: Low active<br>1'b1: High active |
| 7 | RW | 0x0 | uart8_rts_inv<br>Polarity selection for uart8_rts.<br>1'b0: Low active<br>1'b1: High active |
| 6 | RW | 0x0 | uart7_rts_inv<br>Polarity selection for uart7_rts.<br>1'b0: Low active<br>1'b1: High active |
| 5 | RW | 0x0 | uart6_rts_inv<br>Polarity selection for uart6_rts.<br>1'b0: Low active<br>1'b1: High active |
| 4 | RW | 0x0 | uart5_rts_inv<br>Polarity selection for uart5_rts.<br>1'b0: Low active<br>1'b1: High active |
| 3 | RW | 0x0 | uart4_rts_inv<br>Polarity selection for uart4_rts.<br>1'b0: Low active<br>1'b1: High active |
| 2 | RW | 0x0 | uart3_rts_inv<br>Polarity selection for uart3_rts.<br>1'b0: Low active<br>1'b1: High active |
| 1 | RW | 0x0 | uart2_rts_inv<br>Polarity selection for uart2_rts.<br>1'b0: Low active<br>1'b1: High active |
| 0 | RW | 0x0 | uart1_rts_inv<br>Polarity selection for uart1_rts.<br>1'b0: Low active<br>1'b1: High active |

**SYS_GRF_GIC_CON0**

Address: Operational Base + offset (0x00C0)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RW | 0x00 | cpu_active<br>CPU active status<br>Indicates if the core is active and not in a low-power state such as retention. The GIC can decide to target only active cores for 1 of N SPIs. |
| 7:2 | RO | 0x00 | reserved |
| 1 | RW | 0x1 | gic_sample_req<br>GIC sample request<br>This 4-phase handshake provides a hardware mechanism to snapshot the PMU counters and has the same effect as writing to the GICP_CAPR register. |
| 0 | RO | 0x0 | reserved |

**SYS_GRF_MEMCFG_CON0**

Address: Operational Base + offset (0x0200)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x1410 | rkvdec_mem_cfg_hdpsprf<br>RKVDEC HDSPRF memory configuration<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMD<br>bit 7: LS<br>bit 11~10: WPULSE<br>bit 13~12: RA |

**SYS_GRF_MEMCFG_CON1**

Address: Operational Base + offset (0x0204)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x8010 | rkvdec_mem_cfg_uhdpdprf<br>RKVDEC UHDPDPRF memory configuration low bits<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMDA<br>bit 7: LS |

**SYS_GRF_MEMCFG_CON2**

Address: Operational Base + offset (0x0208)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:3 | RO | 0x0000 | reserved |
| 2:0 | RW | 0x0 | rkvdec_mem_cfg_uhdpdprf<br>RKVDEC UHDPDPRF memory configuration high bits<br>bit 0: TESTRWM |

**SYS_GRF_MEMCFG_CON3**

Address: Operational Base + offset (0x020C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0010 | rkvdec_mem_cfg_hsdprf<br>RKVDEC HSDPRF memory configuration low bits<br>bit 0: TEST1A<br>bit 1: TEST_RNMA<br>bit 5~2: RMA<br>bit 6: WMDA<br>bit 8: LS |

**SYS_GRF_MEMCFG_CON4**

Address: Operational Base + offset (0x0210)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7:0 | RW | 0x11 | rkvdec_mem_cfg_hsdprf<br>RKVDEC HSDPRF memory configuration high bits<br>bit 1: TEST1B<br>bit 5~2: RMB |

**SYS_GRF_MEMCFG_CON5**

Address: Operational Base + offset (0x0214)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x1410 | rkvenc_mem_cfg_hdsprf<br>RKVENC HDSPRF memory configuration<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMD<br>bit 7: LS<br>bit 11~10: WPULSE<br>bit 13~12: RA |

**SYS_GRF_MEMCFG_CON6**

Rockchip Confidencial

Address: Operational Base + offset (0x0218)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x8010 | rkvenc_mem_cfg_uhdpdprf<br>RKVENC UHDPDPRF memory configuration low bits<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMDA<br>bit 7: LS |

**SYS_GRF_MEMCFG_CON7**

Address: Operational Base + offset (0x021C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:3 | RO | 0x0000 | reserved |
| 2:0 | RW | 0x0 | rkvenc_mem_cfg_uhdpdprf<br>RKVENC UHDPDPRF memory configuration high bits<br>bit 0: TESTRWM |

**SYS_GRF_MEMCFG_CON8**

Address: Operational Base + offset (0x0220)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0010 | rkvenc_mem_cfg_hsdprf<br>RKVENC HSDPRF memory configuration low bits<br>bit 0: TEST1A<br>bit 1: TEST_RNMA<br>bit 5~2: RMA<br>bit 6: WMDA<br>bit 8: LS |

**SYS_GRF_MEMCFG_CON9**

Address: Operational Base + offset (0x0224)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7:0 | RW | 0x11 | rkvenc_mem_cfg_hsdprf<br>RKVENC HSDPRF memory configuration high bits<br>bit 1: TEST1B<br>bit 5~2: RMB |

**SYS_GRF_MEMCFG_CON10**

Address: Operational Base + offset (0x0228)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x1410 | vdpu_mem_cfg_hdsprf<br>VDPU HDSPRF memory configuration<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMD<br>bit 7: LS<br>bit 11~10: WPULSE<br>bit 13~12: RA |

**SYS_GRF_MEMCFG_CON11**

Address: Operational Base + offset (0x022C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x8010 | vdpu_mem_cfg_uhdpdprf<br>VDPU UHDPDPRF memory configuration low bits<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMDA<br>bit 7: LS |

**SYS_GRF_MEMCFG_CON12**

Address: Operational Base + offset (0x0230)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:3 | RO | 0x0000 | reserved |
| 2:0 | RW | 0x0 | vdpu_mem_cfg_uhdpdprf<br>VDPU UHDPDPRF memory configuration high bits<br>bit 0: TESTRWM |

**SYS_GRF_MEMCFG_CON13**

Address: Operational Base + offset (0x0234)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0010 | vdpu_mem_cfg_hsdprf<br>VDPU HSDPRF memory configuration low bits<br>bit 0: TEST1A<br>bit 1: TEST_RNMA<br>bit 5~2: RMA<br>bit 6: WMDA<br>bit 8: LS |

Rockchip Confidencial

**SYS_GRF_MEMCFG_CON14**

Address: Operational Base + offset (0x0238)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7:0 | RW | 0x11 | vdpu_mem_cfg_hsdprf<br>VDPU HSDPRF memory configuration high bits<br>bit 1: TEST1B<br>bit 5~2: RMB |

**SYS_GRF_MEMCFG_CON15**

Address: Operational Base + offset (0x023C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7:0 | RW | 0x08 | vdpu_mem_cfg_rom<br>VDPU ROM memory configuration<br>bit 0: TEST1<br>bit 4~1: RM<br>bit 5: LS |

**SYS_GRF_MEMCFG_CON16**

Address: Operational Base + offset (0x0240)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0010 | av1_mem_cfg_hsdprf<br>AV1 HSDPRF memory configuration low bits<br>bit 0: TEST1A<br>bit 1: TEST_RNMA<br>bit 5~2: RMA<br>bit 6: WMDA<br>bit 8: LS |

**SYS_GRF_MEMCFG_CON17**

Address: Operational Base + offset (0x0244)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10:8 | RW | 0x0 | av1_mem_cfg_uhdpdprf<br>AV1 UHDPDPRF memory configuration high bits<br>bit 8: TESTRWM |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:0 | RW | 0x11 | av1_mem_cfg_hsdprf<br>AV1 HSDPRF memory configuration high bits<br>bit 1: TEST1B<br>bit 5~2: RMB |

**SYS_GRF_MEMCFG_CON18**

Address: Operational Base + offset (0x0248)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x8010 | av1_mem_cfg_uhdpdprf<br>AV1 UHDPDPRF memory configuration low bits<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMDA<br>bit 7: LS |

**SYS_GRF_MEMCFG_CON19**

Address: Operational Base + offset (0x024C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x1410 | av1_mem_cfg_hdsprf<br>AV1 HDSPRF memory configuration<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMD<br>bit 7: LS<br>bit 11~10: WPULSE<br>bit 13~12: RA |

**SYS_GRF_MEMCFG_CON20**

Address: Operational Base + offset (0x0250)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7:0 | RW | 0x08 | sys_mem_cfg_rom<br>ROM memory configuration<br>bit 0: TEST1<br>bit 4~1: RM<br>bit 5: LS |

**SYS_GRF_MEMCFG_CON21**

Address: Operational Base + offset (0x0254)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x1410 | sys_mem_cfg_hdsprf<br>system HDSPRF memory configuration<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMD<br>bit 7: LS<br>bit 11~10: WPULSE<br>bit 13~12: RA |

**SYS_GRF_MEMCFG_CON22**

Address: Operational Base + offset (0x0258)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0010 | sys_mem_cfg_hsdprf<br>system HSDPRF memory configuration low bits<br>bit 0: TEST1A<br>bit 1: TEST_RNMA<br>bit 5~2: RMA<br>bit 6: WMDA<br>bit 8: LS |

**SYS_GRF_MEMCFG_CON23**

Address: Operational Base + offset (0x025C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7:0 | RW | 0x11 | sys_mem_cfg_hsdprf<br>system HSDPRF memory configuration high bits<br>bit 1: TEST1B<br>bit 5~2: RMB |

**SYS_GRF_MEMCFG_CON24**

Address: Operational Base + offset (0x0260)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x2010 | sys_mem_cfg_hsspra<br>system HSSPRA memory configuration<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMD<br>bit 7: LS |

**SYS_GRF_MEMCFG_CON26**

Address: Operational Base + offset (0x0268)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x8010 | sys_mem_cfg_hsdpra<br>system HSDPRA memory configuration low bits<br>bit 0: TEST1A<br>bit 1: TEST_RNMA<br>bit 4~2: RMA<br>bit 5: WMDA<br>bit 7: LS<br>bit 11~10: WPULSE<br>bit 13~12: RA<br>bit 15~14: WA |

**SYS_GRF_MEMCFG_CON27**

Address: Operational Base + offset (0x026C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x010 | sys_mem_cfg_hsdpra<br>system HSDPRA memory configuration high bits<br>bit 0: TEST1B<br>bit 1: TEST_RNMB<br>bit 4~2: RMB<br>bit 5: WMDB |

**SYS_GRF_MEMCFG_CON28**

Address: Operational Base + offset (0x0270)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x1410 | vi_mem_cfg_hdsprf<br>VI subsystem HDSPRF memory configuration<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMD<br>bit 7: LS<br>bit 11~10: WPULSE<br>bit 13~12: RA |

**SYS_GRF_MEMCFG_CON29**

Address: Operational Base + offset (0x0274)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0010 | vi_mem_cfg_hsdprf<br>VI subsystem HSDPRF memory configuration low bits<br>bit 0: TEST1A<br>bit 1: TEST_RNMA<br>bit 5~2: RMA<br>bit 6: WMDA<br>bit 8: LS |

**SYS_GRF_MEMCFG_CON30**

Address: Operational Base + offset (0x0278)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7:0 | RW | 0x11 | vi_mem_cfg_hsdprf<br>VI subsystem HSDPRF memory configuration high bits<br>bit 1: TEST1B<br>bit 5~2: RMB |

**SYS_GRF_MEMCFG_CON31**

Address: Operational Base + offset (0x027C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x2010 | vi_mem_cfg_hsspra<br>VI subsystem HSSPRA memory configuration<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMD<br>bit 7: LS |

**SYS_GRF_SOC_CON1**

Address: Operational Base + offset (0x0304)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | spdif0_txm1_inv_sel<br>Select SPDIF0_TXM1 to IO invert or not<br>1'b0: Do not invert spdif0_txm1<br>1'b1: Invert spdif0_txm1 |
| 14 | RW | 0x0 | vop_dclk_inv_sel<br>1'b0: Do not invert VOP DCLK to IO<br>1'b1: Invert VOP DCLK to IO |
| 13 | RW | 0x0 | isp1_shutter_trig<br>ISP1 shutter trigger.<br>High valid. |
| 12 | RW | 0x0 | isp1_disable_isp<br>disable ISP1 function.<br>High valid. |
| 11 | RW | 0x0 | isp0_shutter_trig<br>ISP0 shutter trigger.<br>High valid. |
| 10 | RW | 0x0 | isp0_disable_isp<br>disable ISP0 function.<br>High valid. |
| 9:2 | RO | 0x00 | reserved |
| 1 | RW | 0x0 | hdmirxphy_sram_ext_ld_done<br>HDMIRX PHY SRAM external load done<br>This signal asserted by user after any updates to the SRAM have been loaded. |
| 0 | RW | 0x0 | hdmirxphy_sram_bypass<br>HDMI RXPHY SRAM bypass control<br>when sram bypass control signal asserted, bypasses the SRAM interface. In this case, the adaptation and calibration algorithms are executed from the hard wired values within the Raw PCS. If SRAM is not bypassed, the internal algorithms are first loaded by Raw PCS into the SRAM at which point user can change the contents of the SRAM. The updated SRAM contents are used for the adaptation and calibration routines.<br>This signal is meant to be used only for debugging purposes and must not change after phy_reset is negated. |

**SYS_GRF_SOC_CON2**

Address: Operational Base + offset (0x0308)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | hdmitx1_hpd_int_msk<br>HDMI TX1 HPD interrupt mask<br>1'b0: Interrupt enable<br>1'b1: Interrupt disable |
| 14 | RW | 0x0 | hdmitx1_hpd_int_clr<br>A posedge of hdmitx1_hpd_int_clr will clear the HDMI TX1 HPD interrupt. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | hdmitx0_hpd_int_msk<br>HDMI TX0 HPD interrupt mask<br>1'b0: Interrupt enable<br>1'b1: Interrupt disable |
| 12 | RW | 0x0 | hdmitx0_hpd_int_clr<br>A posedge of hdmitx0_hpd_int_clr will clear the HDMI TX0 HPD interrupt. |
| 11 | RW | 0x0 | csihost5_sel<br>CSIHOST5 mode select<br>1'b0: Connect to D-PHY lane 0/1<br>1'b1: Connect to D-PHY lane 2/3<br>This bit is valid only in D-PHY split mode. |
| 10 | RW | 0x0 | csihost4_sel<br>CSIHOST4 mode select<br>1'b0: Connect to D-PHY lane 0/1<br>1'b1: Connect to D-PHY lane 2/3<br>This bit is valid only in D-PHY split mode. |
| 9 | RW | 0x0 | csihost3_sel<br>CSIHOST3 mode select<br>1'b0: Connect to D-PHY lane 0/1<br>1'b1: Connect to D-PHY lane 2/3<br>This bit is valid only in D-PHY split mode. |
| 8 | RW | 0x0 | csihost2_sel<br>CSIHOST2 mode select<br>1'b0: Connect to D-PHY lane 0/1<br>1'b1: Connect to D-PHY lane 2/3<br>This bit is valid only in D-PHY split mode. |
| 7 | RW | 0x0 | csidphy1_lane_sel<br>CSIDPHY 1 pipe clock select<br>1'b0: Select clock lane 0 to pipe CSIDPHY data[31:16]<br>1'b1: Select clock lane 1 to pipe CSIDPHY data[31:16]<br>If CSIDPHY works as full mode, set this bit to 1'b0.<br>If CSIDPHY works as split mode, set this bit to 1'b1. |
| 6 | RW | 0x0 | csidphy0_lane_sel<br>CSIDPHY 0 pipe clock select<br>1'b0: Select clock lane 0 to pipe CSIDPHY data[31:16]<br>1'b1: Select clock lane 1 to pipe CSIDPHY data[31:16]<br>If CSIDPHY works as full mode, set this bit to 1'b0.<br>If CSIDPHY works as split mode, set this bit to 1'b1. |
| 5 | RW | 0x0 | vicap_datapath<br>1'b0: Select single edge mode<br>1'b1: Select dual edge mode |
| 4 | RW | 0x0 | vicap_clk_inv_sel<br>VICAP clock invert select<br>1'b0: Do not invert VICAP clock in<br>1'b1: Invert VICAP clock in |
| 3:0 | RO | 0x0 | reserved |

**SYS_GRF_SOC_CON3**

Address: Operational Base + offset (0x030C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:8 | RW | 0x00 | vop_clk_delay_num<br>VOP clock delayline length control |
| 7:0 | RW | 0x00 | vicap_clk_delay_num<br>VIP clock delayline length control |

**SYS_GRF_SOC_CON6**

Address: Operational Base + offset (0x0318)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pciephy_dtb_sel<br>PCIEPHY DTB select<br>1'b0: Select PCIE0 PHY DTB output to IO<br>1'b1: Select PCIE1 PHY DTB output to IO |
| 14 | RW | 0x1 | force_jtag<br>Force SDMMC IO to JTAG function enable<br>When force_jtag is high , gpio4_d2_sel is 0x1 , gpio4_d3_sel is 0x1, and SDMMC_DETECTN is inactive, switch the SDMMC IO to CPU JTAG function. |
| 13:12 | RW | 0x0 | hdcp_uart2_en<br>HDCP uart enable<br>2'b01: UART2 IO is used for HDCP 0<br>2'b10: UART2 IO is used for HDCP 1 |
| 11 | RW | 0x0 | acdcdig_sel<br>ACDC path select<br>1'b0: I2S3 connect to IO<br>1'b1: I2S3 connect to DSM_PWM |
| 10 | RW | 0x1 | hdmirx_phy_gating_en<br>HDMI RXPHY memory clock gating enable<br>1'b0: HDMIRX PHY memory clock auto gating disable<br>1'b1: HDMIRX PHY memory clock auto gating enable |
| 9 | RW | 0x1 | i2s3_txrxlrck_sel<br>I2S3 lrck select<br>1'b0: Select i2s3_rx_lrck as lrck<br>1'b1: Select i2s3_tx_lrck as lrck |
| 8 | RW | 0x0 | i2s3_sclk_sel<br>I2S3 sclk select<br>1'b0: Select i2s3_sclk_in_rx as sclk<br>1'b1: Select i2s3_sclk_in_tx as sclk |
| 7 | RW | 0x0 | i2s3_mclk_ioe_<br>I2S3_MCLK output enable<br>1'b0: Output enable<br>1'b1: Output disable |
| 6 | RW | 0x0 | i2s2_sclk_sel<br>I2S2 sclk select<br>1'b0: Select i2s2_sclk_in_rx as sclk<br>1'b1: Select i2s2_sclk_in_tx as sclk |
| 5:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | i2s2_mclk_ioe_<br>I2S2_MCLK output enable<br>1'b0: Output enable<br>1'b1: Output disable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | i2s1_mclk_ioe_<br>I2S1_MCLK output enable<br>1'b0: Output enable<br>1'b1: Output disable |
| 0 | RW | 0x0 | i2s0_mclk_ioe_<br>I2S0_MCLK output enable<br>1'b0: Output enable<br>1'b1: Output disable |

**SYS_GRF_SOC_CON7**

Address: Operational Base + offset (0x031C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | edp1_hpd_sel<br>1'b0: Tie EDP1 hpd to 1'b1<br>1'b1: Connect EDP1 hpd to IO |
| 14 | RW | 0x0 | edp0_hpd_sel<br>1'b0: Tie EDP0 hpd to 1'b1<br>1'b1: Connect EDP0 hpd to IO |
| 13 | RW | 0x0 | hdmitx1hpd_io_sel<br>1'b0: Tie HDMITX1 hpd to 1'b0<br>1'b1: Connect HDMITX1 hpd to IO |
| 12 | RW | 0x0 | hdmitx0hpd_io_sel<br>1'b0: Tie HDMITX0 hpd to 1'b0<br>1'b1: Connect HDMITX0 hpd to IO |
| 11 | RW | 0x1 | emmc_ram_clkgat_disable<br>1'b0: Gate EMMC memory clock when idle<br>1'b1: EMMC memory clock is always on |
| 10 | RW | 0x0 | sdio_ram_clkgat_disable<br>1'b0: Gate SDIO memory clock when idle<br>1'b1: SDIO memory clock is always on |
| 9 | RW | 0x1 | sdmmc_ram_clkgat_disable<br>1'b0: Gate SDMMC memory clock when idle<br>1'b1: SDMMC memory clock is always on |
| 8 | RW | 0x0 | trng_ns_i_rst_sync_bypass<br>when high, bypass the reset synchronization logic. |
| 7 | RW | 0x0 | trng_ns_i_ctrl_reseed<br>control the non-secure TRNG to regenerate the random seed. |
| 6 | RW | 0x0 | trng_ns_i_ctrl_zeroize<br>used to clear the state and seed of non-secure TRNG. |
| 5 | RW | 0x0 | gmac1_rxclk_dly_ena<br>RGMII RX clock delayline enable<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | gmac1_txclk_dly_ena<br>RGMII TX clock delayline enable<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | gmac0_rxclk_dly_ena<br>RGMII RX clock delayline enable<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | gmac0_txclk_dly_ena<br>RGMII TX clock delayline enable<br>1'b0: Disable<br>1'b1: Enable |
| 1:0 | RW | 0x0 | sata_io_sel<br>SATA IO select<br>2'b00: Select SATA0 cp_det / mp_switch / cp_pod to IO<br>2'b01: Select SATA1 cp_det / mp_switch / cp_pod to IO<br>2'b10: Select SATA2 cp_det / mp_switch / cp_pod to IO |

**SYS_GRF_SOC_CON8**

Address: Operational Base + offset (0x0320)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RW | 0x00 | gmac0_clk_rx_dl_cfg<br>GMAC0 RX clock delayline configuration<br>MAC recept clock delay length configuration |
| 7:0 | RW | 0x00 | gmac0_clk_tx_dl_cfg<br>GMAC0 TX clock delayline configuration<br>MAC transmit clock delay length configuration |

**SYS_GRF_SOC_CON9**

Address: Operational Base + offset (0x0324)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RW | 0x00 | gmac1_clk_rx_dl_cfg<br>GMAC1 RX clock delayline configuration<br>MAC recept clock delay length configuration |
| 7:0 | RW | 0x00 | gmac1_clk_tx_dl_cfg<br>GMAC1 TX clock delayline configuration<br>MAC transmit clock delay length configuration |

**SYS_GRF_SOC_CON10**

Address: Operational Base + offset (0x0328)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | hdmi_debug_sel<br>HDMI DEBUG IO select<br>select different debug signals to IO. |
| 11:10 | RW | 0x0 | mcujtag_sel<br>2'b00: JTAG IO select PMU MCU<br>2'b01: JTAG IO select DDR MCU<br>2'b10: JTAG IO select GPU MCU<br>2'b11: JTAG IO select NPU MCU |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RW | 0x1 | clkbypass_emmc<br>clock gate bypass<br>1'b0: Enable clock gate of EMMC<br>1'b1: Disable clock gate of EMMC |
| 8 | RW | 0x1 | clkstable_emmc<br>card clock stable<br>When asserted it indicates that the card clock is stable.<br>Active State: High |
| 7:3 | RW | 0x00 | sdmmc_fifo_wr_thresh<br>SDMMC BUFFER FIFO threshold control<br>When the space of SDMMC BUFFER FIFO is more than the threshold, SDMMC BUFFER module will send the dma request signal. |
| 2 | RW | 0x0 | sdmmc_buf_clk_inv_sel<br>SDMMC BUFFER clock invert select<br>1'b0: Do not invert SDMMC BUFFER clock output<br>1'b1: Invert SDMMC BUFFER clock output |
| 1 | RW | 0x0 | sdmmc_buffer_en<br>SDMMC BUFFER enable<br>1'b0: SDMMC BUFFER module disable<br>1'b1: SDMMC BUFFER module enable |
| 0 | RW | 0x0 | sdmmc_buffer_io_en<br>SDMMC BUFFER IO select<br>1'b0: Select SDMMC to SDMMC IO<br>1'b1: Select SDMMC BUFFER to SDMMC IO |

**SYS_GRF_SOC_CON11**

Address: Operational Base + offset (0x032C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00092820 | sdcard_dectn_dly<br>Delay counter setting after sdcard plug out. Counted by 24M clock |

**SYS_GRF_SOC_CON12**

Address: Operational Base + offset (0x0330)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | hdmitx0_hpd_port_from_ff<br>1'b1: Active the register as the input hpd port<br>1'b0: Inactive the register as the input hpd port |
| 14 | RW | 0x0 | hdmitx0_hpd_port_from_top<br>1'b1: Active the top level's hpd port as the input hpd port<br>1'b0: Inactive the top level's hpd port as the input hpd port |
| 13:8 | RW | 0x00 | hdmitx0_setdly_en<br>6'h0: Inactive SET_LNUM_MS value<br>Others not 6'h0: Active SET_LNUM_MS value |
| 7:0 | RW | 0x00 | hdmitx0_set_lnum_ms<br>The low level count threshold value. For example: 20 means low level stable 20ms. |

**SYS_GRF_SOC_CON13**

Address: Operational Base + offset (0x0334)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | hdmitx1_hpd_port_from_ff<br>1'b1: Active the register as the input hpd port<br>1'b0: Inactive the register as the input hpd port |
| 14 | RW | 0x0 | hdmitx1_hpd_port_from_top<br>1'b1: Active the top level's hpd port as the input hpd port<br>1'b0: Inactive the top level's hpd port as the input hpd port |
| 13:8 | RW | 0x00 | hdmitx1_setdly_en<br>6'h0: Inactive SET_LNUM_MS value<br>Others not 6'h0: Active SET_LNUM_MS value |
| 7:0 | RW | 0x00 | hdmitx1_set_lnum_ms<br>The low level count threshold value. For example: 20 means low level stable 20ms. |

**SYS_GRF_SOC_STATUS0**

Address: Operational Base + offset (0x0380)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |
| 12 | RO | 0x0 | gic_sample_ack<br>Used with gic_sample_req. This 4-phase handshake provides a mechanism to snapshot the PMU counters and has the same effects as writting to the GICP_CAPR register. |
| 11:0 | RO | 0x000 | timer_ns_en_status<br>TIMER_NS enable status |

**SYS_GRF_SOC_STATUS1**

Address: Operational Base + offset (0x0384)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28 | RO | 0x0 | hdmitx1_low_morethan100ms<br>1'b0: Low more than 100 ms (Internal signal of the HPD module) signal is low level<br>1'b1: Low more than 100 ms (Internal signal of the HPD module) signal is high level |
| 27 | RO | 0x0 | hdmitx1_port_level<br>1'b0: HPD_PORT_LEVEL (Internal signal of the HPD module) signal is low level<br>1'b1: HPD_PORT_LEVEL (Internal signal of the HPD module) signal is high level |
| 26 | RO | 0x0 | hdmitx1_ihpd_port<br>1'b0: IHPD_PORT (Input signal of the HPD module) signal is low level<br>1'b1: IHPD_PORT (Input signal of the HPD module) signal is high level |
| 25 | RO | 0x0 | hdmitx1_ohpd_int<br>1'b0: Ohpd_int (Output signal of the HPD module) signal is low level<br>1'b1: Ohpd_int (Output signal of the HPD module) signal is high level |
| 24 | RO | 0x0 | hdmitx1_level_int<br>1'b0: Level Interrupt signal is low level<br>1'b1: Level Interrupt signal is high level |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:21 | RO | 0x0 | hdmitx1_int_change_cnt<br>Store the interrupt change times. |
| 20 | RO | 0x0 | hdmitx0_low_morethan100ms<br>1'b0: Low more than 100 ms (Internal signal of the HPD module) signal is low level<br>1'b1: Low more than 100 ms (Internal signal of the HPD module) signal is high level |
| 19 | RO | 0x0 | hdmitx0_port_level<br>1'b0: HPD_PORT_LEVEL (Internal signal of the HPD module) signal is low level<br>1'b1: HPD_PORT_LEVEL (Internal signal of the HPD module) signal is high level |
| 18 | RO | 0x0 | hdmitx0_ihpd_port<br>1'b0: IHPD_PORT (Input signal of the HPD module) signal is low level<br>1'b1: IHPD_PORT (Input signal of the HPD module) signal is high level |
| 17 | RO | 0x0 | hdmitx0_ohpd_int<br>1'b0: Ohpd_int (Output signal of the HPD module) signal is low level<br>1'b1: Ohpd_int (Output signal of the HPD module) signal is high level |
| 16 | RO | 0x0 | hdmitx0_level_int<br>1'b0: Level Interrupt signal is low level<br>1'b1: Level Interrupt signal is high level |
| 15:13 | RO | 0x0 | hdmitx0_int_change_cnt<br>Store the interrupt change times. |
| 12 | RO | 0x0 | isp1_shutter_open<br>ISP1 shutter open<br>High valid. |
| 11 | RO | 0x0 | isp0_shutter_open<br>ISP0 shutter open<br>High valid |
| 10 | RO | 0x0 | hdmirxphy_sram_init_done<br>HDMIRX PHY SRAM initialization done status<br>The bit indicates that the SRAM has been initialized by the boot loader in the Raw PCS. |
| 9 | RO | 0x0 | trng_ns_o_ctrl_secure<br>Non-Secure TRNG status<br>Secure mode output, high valid. |
| 8 | RO | 0x0 | trng_ns_o_ctrl_reminder<br>Non-Secure TRNG status<br>Reseed reminder output, high pulse valid. |
| 7 | RO | 0x0 | trng_ns_o_ctrl_reseeding<br>Non-Secure TRNG status<br>Reseeding activity output, high valid. |
| 6 | RO | 0x0 | trng_ns_o_ctrl_seeded<br>Non-Secure TRNG status<br>(Re)Seeding completion output, high valid. |
| 5 | RO | 0x0 | trng_ns_o_ctrl_rand_bit<br>Non-Secure TRNG status<br>Serial random bit output. |
| 4 | RO | 0x0 | trng_ns_o_ctrl_rand_vld<br>Non-Secure TRNG status<br>Serial random bit valid output, high valid. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RO | 0x0 | dfi_scramble_ready<br>DFI scramble key is ready, high valid. |

**SYS_GRF_SOC_STATUS2**

Address: Operational Base + offset (0x0388)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5 | RO | 0x0 | rkvenc1_idle_enc_core<br>RKVENC1 idle status |
| 4 | RO | 0x0 | rkvenc1_idle_enc_axi<br>RKVENC1 idle status |
| 3 | RO | 0x0 | rkvenc1_idle_enc_ahb<br>RKVENC1 idle status |
| 2 | RO | 0x0 | rkvenc0_idle_enc_core<br>RKVENC0 idle status |
| 1 | RO | 0x0 | rkvenc0_idle_enc_axi<br>RKVENC0 idle status |
| 0 | RO | 0x0 | rkvenc0_idle_enc_ahb<br>RKVENC0 idle status |

**SYS_GRF_SOC_STATUS3**

Address: Operational Base + offset (0x038C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19 | RO | 0x0 | osc_chk_rst_req<br>OSC frequency check error |
| 18 | RO | 0x0 | crc_chk_rst_req_sgrf<br>SGRF in pd_bus crc check error |
| 17 | RO | 0x0 | crc_chk_rst_req_dsusgrf<br>SGRF in pd_core crc check error |
| 16 | RO | 0x0 | crc_chk_rst_req_pmusgrf<br>SGRF in pd_pmu crc check error |
| 15:8 | RO | 0x00 | cpu_wfi<br>CPU WFI status |
| 7:0 | RO | 0x00 | cpu_wfe<br>CPU WFE status |

**SYS_GRF_OTP_KEY08**

Address: Operational Base + offset (0x0500)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RO | 0x0 | key08<br>The value of OTP address 0x8 |

**SYS_GRF_OTP_KEY0D**

Address: Operational Base + offset (0x0504)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RO | 0x0 | key0d<br>The value of OTP address 0xd |

**SYS_GRF_OTP_KEY0E**

Address: Operational Base + offset (0x0508)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RO | 0x0 | key0e<br>The value of OTP address 0xe |

**SYS_GRF_CHIP_ID**

Address: Operational Base + offset (0x0600)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00003588 | chip_id<br>The Chip ID status<br>Reads as 0x3588 |

# 6.6 BIGCORE_GRF Register Description

There are two BIGCORE_GRF modules in RK3588.They have different base address.

## 6.6.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| BIGCORE_GRF_PVTPLL_CON0_L | 0x0000 | W | 0x00000000 | PVTPLL Control Register 0 Low |
| BIGCORE_GRF_PVTPLL_CON0_H | 0x0004 | W | 0x00000000 | PVTPLL Control Register 0 High |
| BIGCORE_GRF_PVTPLL_CON1 | 0x0008 | W | 0x00000018 | PVTPLL Control Register 1 |
| BIGCORE_GRF_PVTPLL_CON2 | 0x000C | W | 0x00040000 | PVTPLL Control Register 2 |
| BIGCORE_GRF_PVTPLL_CON3 | 0x0010 | W | 0x00000000 | PVTPLL Control Register 3 |
| BIGCORE_GRF_MEM_CFG_HSSPRF_L | 0x0020 | W | 0x00008010 | Memory Configuration Register For HSSPRF Low |
| BIGCORE_GRF_MEM_CFG_HSDPRF_L | 0x0028 | W | 0x00000010 | Memory Configuration Register For HSDPRF |
| BIGCORE_GRF_MEM_CFG_HSDPRF_H | 0x002C | W | 0x00000011 | Memory Configuration Register For HSSPRF High |
| BIGCORE_GRF_CPU_CON0 | 0x0030 | W | 0x00000000 | CPU Control Register 0 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.6.2 Detail Registers Description

**BIGCORE_GRF_PVTPLL_CON0_L**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | bypass<br>1'b0: Support glitch-free frequency conversion.<br>1'b1: Not support. |
| 14:13 | RW | 0x0 | clk_div_osc<br>Frequency division factor for osc_clk. |
| 12:11 | RW | 0x0 | clk_div_ref<br>Frequency division factor for ref_clk. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10:8 | RW | 0x0 | osc_ring_sel<br>Oscillator ring channel select. |
| 7:3 | RO | 0x00 | reserved |
| 2 | RW | 0x0 | out_polar<br>1'b0: Out=1 when need to increase volt.<br>1'b1: Out=0 when need to increase volt. |
| 1 | RW | 0x0 | osc_en<br>Oscillator ring enable. |
| 0 | RW | 0x0 | start<br>1'b1: PVTPLL monitor start. |

**BIGCORE_GRF_PVTPLL_CON0_H**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5:0 | RW | 0x00 | ring_length_sel<br>Oscillator ring inverter length select. |

**BIGCORE_GRF_PVTPLL_CON1**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000018 | cal_cnt<br>Target frequency value. |

**BIGCORE_GRF_PVTPLL_CON2**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0004 | ckg_val<br>Clock gating interval control count value. |
| 15:0 | RW | 0x0000 | threshold<br>Count difference threshold value. |

**BIGCORE_GRF_PVTPLL_CON3**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ref_cnt<br>Frequency measurement period setting value. |

**BIGCORE_GRF_MEM_CFG_HSSPRF_L**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x8010 | grf_bigcore_mem_cfg_hssprf_l<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMD<br>bit 7: LS<br>bit 13~12: RA |

**BIGCORE_GRF_MEM_CFG_HSDPRF_L**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0010 | grf_bigcore_mem_cfg_hsdprf_l<br>bit 0: TEST1A<br>bit 1: TEST_RNMA<br>bit 5~2: RMA<br>bit 6: WMDA<br>bit 8: LS<br>bit 14~13: RA |

**BIGCORE_GRF_MEM_CFG_HSDPRF_H**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0011 | grf_bigcore_mem_cfg_hsdprf_h<br>bit 1: TEST1B<br>bit 5~2: RMB |

**BIGCORE_GRF_CPU_CON0**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x0 | grf_con_bigcore_mem_cfg_idle_trig<br>A 0 to 1 trigger of grf_con_bigcore_mem_cfg_idle_trig will cause a mem_cfg change when grf_con_bigcore_mem_cfg_idle_en equals to 1. |
| 4 | RW | 0x0 | grf_con_bigcore_mem_cfg_idle_en<br>1'b0: Mem_cfg is changed by software immediately<br>1'b1: Mem_cfg is changed when all cpu in wfi |
| 3:0 | RW | 0x0 | bigcore_grf_con_mem_ctrl_from_pmu<br>1'b0: Mem_cfg is driven by grf<br>1'b1: Mem_cfg is driven by pmu<br>Each bit for one cpu core |

Rockchip Confidencial

# 6.7 LITCORE_GRF Register Description

## 6.7.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| LITCORE_GRF_MEM_CFG_HSSPRF_L | 0x0020 | W | 0x00008010 | Memory Configuration Register For HSSPRF |
| LITCORE_GRF_MEM_CFG_HSDPRF_L | 0x0028 | W | 0x00000010 | Memory Configuration Register For HSDPRF Low |
| LITCORE_GRF_MEM_CFG_HSDPRF_H | 0x002C | W | 0x0000000B | Memory Configuration Register For HSDPRF Low |
| LITCORE_GRF_CPU_CON0 | 0x0030 | W | 0x00000000 | CPU Control Register 0 |
| LITCORE_GRF_PVTPLL_CON0_L | 0x0040 | W | 0x00000000 | PVTPLL Control Register 0 Low |
| LITCORE_GRF_PVTPLL_CON0_H | 0x0044 | W | 0x00000000 | PVTPLL Control Register 0 High |
| LITCORE_GRF_PVTPLL_CON1 | 0x0048 | W | 0x00000018 | PVTPLL Control Register 1 |
| LITCORE_GRF_PVTPLL_CON2 | 0x004C | W | 0x00040000 | PVTPLL Control Register 2 |
| LITCORE_GRF_PVTPLL_CON3 | 0x0050 | W | 0x00000000 | PVTPLL Control Register 3 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.7.2 Detail Registers Description

**LITCORE_GRF_MEM_CFG_HSSPRF_L**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x8010 | grf_litcore_mem_cfg_hssprf_l<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMD<br>bit 7: LS<br>bit 13~12: RA |

**LITCORE_GRF_MEM_CFG_HSDPRF_L**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0010 | grf_litcore_mem_cfg_hsdprf_l<br>bit 0: TEST1A<br>bit 1: TEST_RNMA<br>bit 5~2: RMA<br>bit 6: WMDA<br>bit 8: LS<br>bit 14~13: RA |

Rockchip Confidential

**LITCORE_GRF_MEM_CFG_HSDPRF_H**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x000b | grf_litcore_mem_cfg_hsdprf_h<br>bit 1: TEST1B<br>bit 5~2: RMB |

**LITCORE_GRF_CPU_CON0**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x0 | grf_con_litcore_mem_cfg_idle_trig<br>A 0 to 1 trigger of grf_con_litcore_mem_cfg_idle_trig will cause a mem_cfg change when grf_con_litcore_mem_cfg_idle_en equals to 1. |
| 4 | RW | 0x0 | grf_con_litcore_mem_cfg_idle_en<br>1'b0: Mem_cfg is changed by software immediately<br>1'b1: Mem_cfg is changed when all cpu in wfi |
| 3:0 | RW | 0x0 | litcore_grf_con_mem_ctrl_from_pmu<br>1'b0: Mem_cfg is driven by grf<br>1'b1: Mem_cfg is driven by pmu<br>Each bit for one cpu core |

**LITCORE_GRF_PVTPLL_CON0_L**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | bypass<br>1'b0: Support glitch-free frequency conversion.<br>1'b1: Not support. |
| 14:13 | RW | 0x0 | clk_div_osc<br>Frequency division factor for osc_clk. |
| 12:11 | RW | 0x0 | clk_div_ref<br>Frequency division factor for ref_clk. |
| 10:8 | RW | 0x0 | osc_ring_sel<br>Oscillator ring channel select. |
| 7:3 | RO | 0x00 | reserved |
| 2 | RW | 0x0 | out_polar<br>1'b0: Out=1 when need to increase volt.<br>1'b1: Out=0 when need to increase volt. |
| 1 | RW | 0x0 | osc_en<br>Oscillator ring enable. |
| 0 | RW | 0x0 | start<br>1'b1: PVTPLL monitor start. |

Rockchip Confidential

**LITCORE_GRF_PVTPLL_CON0_H**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5:0 | RW | 0x00 | ring_length_sel<br>Oscillator ring inverter length select. |

**LITCORE_GRF_PVTPLL_CON1**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000018 | cal_cnt<br>Target frequency value. |

**LITCORE_GRF_PVTPLL_CON2**

Address: Operational Base + offset (0x004C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0004 | ckg_val<br>Clock gating interval control count value. |
| 15:0 | RW | 0x0000 | threshold<br>Count difference threshold value. |

**LITCORE_GRF_PVTPLL_CON3**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ref_cnt<br>Frequency measurement period setting value. |

# 6.8 DSU_GRF Register Description

## 6.8.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| DSU_GRF_CON0 | 0x0000 | W | 0x0000FFFF | DSU Control Register 0 |
| DSU_GRF_CON1 | 0x0004 | W | 0x0000FFFF | DSU Control Register 1 |
| DSU_GRF_CON2 | 0x0008 | W | 0x00000000 | DSU Control Register 2 |
| DSU_GRF_CON3 | 0x000C | W | 0x0000FF00 | DSU Control Register 3 |
| DSU_GRF_CON4 | 0x0010 | W | 0x00000F00 | DSU Control Register 4 |
| DSU_GRF_CON5 | 0x0014 | W | 0x00000FF0 | DSU Control Register 5 |
| DSU_GRF_CON6 | 0x0018 | W | 0x00000000 | DSU Control Register 6 |
| DSU_GRF_MEM_CFG_HSSPRF_L | 0x0020 | W | 0x00008010 | Memory Configuration Register For HSSPRF |
| DSU_GRF_MEM_CFG_HSDPRF_L | 0x0028 | W | 0x00000010 | Memory Configuration Register For HSDPRF Low |
| DSU_GRF_MEM_CFG_HSDPRF_H | 0x002C | W | 0x00000011 | Memory Configuration Register For HSDPRF High |
| DSU_GRF_MEM_CFG_HDSPRA_L | 0x0030 | W | 0x00001410 | Memory Configuration Register For HDSPRA |
| DSU_GRF_MEM_CFG_UHDDPRF_L | 0x0038 | W | 0x00008010 | Memory Configuration Register For UHDDPRF |

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| DSU_GRF_STATUS0 | 0x0040 | W | 0x00000000 | DSU Status Register 0 |
| DSU_GRF_STATUS1 | 0x0044 | W | 0x00000000 | DSU Status Register 1 |
| DSU_GRF_PVTPLL_CON0_L | 0x0060 | W | 0x00000000 | PVTPLL Control Register 0 Low |
| DSU_GRF_PVTPLL_CON0_H | 0x0064 | W | 0x00000000 | PVTPLL Control Register 0 High |
| DSU_GRF_PVTPLL_CON1 | 0x0070 | W | 0x00000018 | PVTPLL Control Register 1 |
| DSU_GRF_PVTPLL_CON2 | 0x0074 | W | 0x00040000 | PVTPLL Control Register 2 |
| DSU_GRF_PVTPLL_CON3 | 0x0078 | W | 0x00000000 | PVTPLL Control Register 3 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.8.2 Detail Registers Description

**DSU_GRF_CON0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RW | 0xff | dsu_grf_con_nirq<br>GRF generate a nirq for each core, for debug usage only |
| 7:0 | RW | 0xff | dsu_grf_con_nfiq<br>GRF generate a nifq for each core, for debug usage only |

**DSU_GRF_CON1**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RW | 0xff | dsu_grf_con_nvirq<br>GRF generate a nvirq for each core, for debug usage only |
| 7:0 | RW | 0xff | dsu_grf_con_nvfiq<br>GRF generate a nvifq for each core, for debug usage only |

**DSU_GRF_CON2**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | dsu_grf_mem_ctrl_from_pmu<br>1'b1: Dsu mem cfg driven by pmu<br>1'b0: Dsu mem cfg driven by grf |
| 8 | RW | 0x0 | dsu_grf_con_awakeups<br>1'b1: Wake acp slave interface<br>1'b0: Not wake acp |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:4 | RW | 0x0 | dsu_grf_con_mpmmen<br>1'b1: Enable max power control for A76<br>1'b0: Diable<br>Each bit for a core |
| 3 | RW | 0x0 | dsu_grf_con_pwrq_permit_deny_sar_i<br>1'b1: Stream adb400 will deny a power request<br>1'b0: Stream adb400 will accept a power request |
| 2 | RW | 0x0 | dsu_grf_con_pmusnapshotreq<br>1'b1: Send a pmu snapshot request to DSU<br>1'b0: Not send |
| 1 | RW | 0x0 | dsu_grf_con_eventoack<br>1'b1: Send evento acknowledge to DSU<br>1'b0: Not send |
| 0 | RW | 0x0 | dsu_grf_con_eventireq<br>1'b1: Send eventi request to DSU<br>1'b0: Not send |

**DSU_GRF_CON3**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0xf | grf_con_acp_awcache<br>Awcache control bit for acp |
| 11:8 | RW | 0xf | grf_con_acp_arcache<br>Arcache ctrl bit for acp |
| 7:6 | RO | 0x0 | reserved |
| 5 | RW | 0x0 | grf_con_interconnect_cgen<br>1'b1: Interconnect clock gate enable<br>1'b0: Disable |
| 4:0 | RW | 0x0 | reserved |

**DSU_GRF_CON4**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0f00 | sys_grf_con_astartmp<br>Start address of MP master |

**DSU_GRF_CON5**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0ff0 | sys_grf_con_aendmp<br>End address for MP master |

Rockchip Confidencial

**DSU_GRF_CON6**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | grf_con_dsu_mem_cfg_idle_trig<br>A 0 to 1 trigger of grf_con_dsu_mem_cfg_idle_trig will cause a mem_cfg change when grf_con_dsu_mem_cfg_idle_en equals to 1. |
| 13 | RW | 0x0 | grf_con_dsu_mem_cfg_idle_en<br>1'b0: Mem_cfg is changed by software immediately<br>1'b1: Mem_cfg is changed when all cpu in wfi |
| 12:11 | RW | 0x0 | grf_con_ardomains<br>Ardomain control for ACP |
| 10:9 | RW | 0x0 | grf_con_awdomains<br>Awdomain control for ACP |
| 8:5 | RW | 0x0 | grf_con_awsnoops<br>Awsnoop ctrl for ACP |
| 4 | RW | 0x0 | grf_con_awstashlpidens<br>AW stashlpiden for ACP |
| 3:0 | RW | 0x0 | grf_con_awstashlpids<br>AW stashlpid for ACP |

**DSU_GRF_MEM_CFG_HSSPRF_L**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x8010 | grf_dsu_mem_cfg_hssprf_l<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMD<br>bit 7: LS<br>bit 13~12: RA |

**DSU_GRF_MEM_CFG_HSDPRF_L**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0010 | grf_dsu_mem_cfg_hssprf_l<br>bit 0: TEST1A<br>bit 1: TEST_RNMA<br>bit 5~2: RMA<br>bit 6: WMDA<br>bit 8: LS<br>bit 14~13: RA |

Rockchip Confidential

**DSU_GRF_MEM_CFG_HSDPRF_H**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0011 | grf_dsu_mem_cfg_hssprf_h<br>bit 1:TEST1B<br>bit 5~2: RMB |

**DSU_GRF_MEM_CFG_HDSPRA_L**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x1410 | grf_dsu_mem_cfg_hdspra_l<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMD<br>bit 7: LS<br>bit 11~10: WPULSE<br>bit 13~12: RA |

**DSU_GRF_MEM_CFG_UHDDPRF_L**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x8010 | grf_dsu_mem_cfg_uhddprf_l<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMDA<br>bit 7: LS |

**DSU_GRF_STATUS0**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23 | RO | 0x0 | dsu_grf_st_jtagactive<br>JTAG active status. |
| 22 | RO | 0x0 | dsu_grf_st_swactive<br>JTAG sw active status. |
| 21:19 | RO | 0x0 | reserved |
| 18 | RO | 0x0 | dsu_grf_st_pmusnapshotack<br>PMU snapshot acknowledge |
| 17 | RO | 0x0 | dsu_grf_st_eventoreq<br>EVENTO request. |
| 16 | RO | 0x0 | dsu_grf_st_eventiack<br>EVENTI acknowledge status |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:8 | RO | 0x00 | dsu_grf_st_coreinstrret<br>Cpu in retention status<br>Each bit for one core |
| 7:0 | RO | 0x00 | dsu_grf_st_coreinstrrun<br>Core running status, each bit for one core |

**DSU_GRF_STATUS1**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RW | 0x0 | dsu_Probe3_mainStatAlarm<br>Interconnect probe3 alarm |
| 6 | RW | 0x0 | dsu_Probe2_mainStatAlarm<br>Interconnect probe 2 alarm |
| 5 | RW | 0x0 | dsu_Probe1_mainStatAlarm<br>Interconnect probe1 alarm |
| 4 | RW | 0x0 | dsu_Probe0_mainStatAlarm<br>Interconnect probe0 alarm |
| 3 | RO | 0x0 | sys_grf_st_debug_m_i_mainnopendingtrans<br>Interconnect debug_m no pending translation |
| 2 | RO | 0x0 | sys_grf_st_nsp_dsu2main_T_mainNoPendingTrans<br>Interconnect dsu2main no pending translation |
| 1:0 | RO | 0x0 | reserved |

**DSU_GRF_PVTPLL_CON0_L**

Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | bypass<br>1'b0: Support glitch-free frequency conversion.<br>1'b1: Not support. |
| 14:13 | RW | 0x0 | clk_div_osc<br>Frequency division factor for osc_clk. |
| 12:11 | RW | 0x0 | clk_div_ref<br>Frequency division factor for ref_clk. |
| 10:8 | RW | 0x0 | osc_ring_sel<br>Oscillator ring channel select. |
| 7:3 | RO | 0x00 | reserved |
| 2 | RW | 0x0 | out_polar<br>1'b0: Out=1 when need to increase volt.<br>1'b1: Out=0 when need to increase volt. |
| 1 | RW | 0x0 | osc_en<br>Oscillator ring enable. |
| 0 | RW | 0x0 | start<br>1'b1: PVTPLL monitor start. |

**DSU_GRF_PVTPLL_CON0_H**

Address: Operational Base + offset (0x0064)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5:0 | RW | 0x00 | ring_length_sel<br>Oscillator ring inverter length select. |

**DSU_GRF_PVTPLL_CON1**

Address: Operational Base + offset (0x0070)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000018 | cal_cnt<br>Target frequency value. |

**DSU_GRF_PVTPLL_CON2**

Address: Operational Base + offset (0x0074)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0004 | ckg_val<br>Clock gating interval control count value. |
| 15:0 | RW | 0x0000 | threshold<br>Count difference threshold value. |

**DSU_GRF_PVTPLL_CON3**

Address: Operational Base + offset (0x0078)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ref_cnt<br>Frequency measurement period setting value. |

# 6.9 DDR_GRF Register Description

There are two DDR_GRF modules in RK3588, DDR01_GRF and DDR23_GRF. DDR01_GRF is for DDR channel 0 and 1. DDR23_GRF is for DDR channel 2 and 3. They have different base address. For DDR01_GRF, DDR_GRF_CHA_* refers to the registers that correspond to DDR channel 0, while DDR_GRF_CHB_* refers to the registers that correspond to DDR channel 1. For DDR23_GRF, DDR_GRF_CHA_* refers to the registers that correspond to DDR channel 2, while DDR_GRF_CHB_* refers to the registers that correspond to DDR channel 3. Register that doesn't have prefix DDR_GRF_CHA or DDR_GRF_CHB is shared by channel 0 and 1 or channel 2 and 3 separately.

## 6.9.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| DDR_GRF_CHA_CON0 | 0x0000 | W | 0x00000040 | DDR CHA Control Register 0 |
| DDR_GRF_CHA_CON1 | 0x0004 | W | 0x00000080 | DDR CHA Control Register 1 |
| DDR_GRF_CHA_CON2 | 0x0008 | W | 0x00000000 | DDR CHA Control Register 2 |
| DDR_GRF_CHA_CON3 | 0x000C | W | 0x00000000 | DDR CHA Control Register 3 |
| DDR_GRF_CHA_CON4 | 0x0010 | W | 0x00000000 | DDR CHA Control Register 4 |
| DDR_GRF_CHA_CON5 | 0x0014 | W | 0x00000000 | DDR CHA Control Register 5 |
| DDR_GRF_CHA_CON6 | 0x0018 | W | 0x00000000 | DDR CHA Control Register 6 |
| DDR_GRF_CHA_CON7 | 0x001C | W | 0x00000010 | DDR CHA Control Register 7 |
| DDR_GRF_CHA_CON8 | 0x0020 | W | 0x00001F4A | DDR CHA Control Register 8 |
| DDR_GRF_CHA_CON9 | 0x0024 | W | 0x000003FF | DDR CHA Control Register 9 |
| DDR_GRF_CHB_CON0 | 0x0030 | W | 0x00000040 | DDR CHB Control Register 0 |
| DDR_GRF_CHB_CON1 | 0x0034 | W | 0x00000080 | DDR CHB Control Register 1 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| DDR_GRF_CHB_CON2 | 0x0038 | W | 0x00000000 | DDR CHB Control Register 2 |
| DDR_GRF_CHB_CON3 | 0x003C | W | 0x00000000 | DDR CHB Control Register 3 |
| DDR_GRF_CHB_CON4 | 0x0040 | W | 0x00000000 | DDR CHB Control Register 4 |
| DDR_GRF_CHB_CON5 | 0x0044 | W | 0x00000000 | DDR CHB Control Register 5 |
| DDR_GRF_CHB_CON6 | 0x0048 | W | 0x00000000 | DDR CHB Control Register 6 |
| DDR_GRF_CHB_CON7 | 0x004C | W | 0x00000010 | DDR CHB Control Register 7 |
| DDR_GRF_CHB_CON8 | 0x0050 | W | 0x00008010 | DDR CHB Control Register 8 |
| DDR_GRF_CHB_CON9 | 0x0054 | W | 0x000003FF | DDR CHB Control Register 9 |
| DDR_GRF_CHA_STATUS0 | 0x0060 | W | 0x00000000 | DDR CHA Status Register 0 |
| DDR_GRF_CHA_STATUS16 | 0x00A0 | W | 0x00000000 | DDR CHA Status Register 16 |
| DDR_GRF_CHA_STATUS17 | 0x00A4 | W | 0x00000000 | DDR CHA Status Register 17 |
| DDR_GRF_CHA_STATUS19 | 0x00AC | W | 0x00000000 | DDR CHA Status Register 19 |
| DDR_GRF_CHB_STATUS0 | 0x00B0 | W | 0x00000000 | DDR CHB Status Register 0 |
| DDR_GRF_CHB_STATUS16 | 0x00F0 | W | 0x00000000 | DDR CHB Status Register 16 |
| DDR_GRF_CHB_STATUS17 | 0x00F4 | W | 0x00000000 | DDR CHB Status Register 17 |
| DDR_GRF_CHB_STATUS19 | 0x00FC | W | 0x00000000 | DDR CHB Status Register 19 |
| DDR_GRF_CHA_PHY_CON0 | 0x0130 | W | 0x00000400 | DDRPHY CHA Control Register 0 |
| DDR_GRF_CHB_PHY_CON0 | 0x0134 | W | 0x00000400 | DDRPHY CHB Control Register 0 |
| DDR_GRF_CHA_PHY_STATUS0 | 0x0138 | W | 0x00000000 | DDRPHY CHA Status Register 0 |
| DDR_GRF_CHB_PHY_STATUS0 | 0x013C | W | 0x00000000 | DDRPHY CHB Status Register 1 |
| DDR_GRF_CON0 | 0x0140 | W | 0x0001ADBA | DDR Control Register 0 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.9.2 Detail Registers Description

**DDR_GRF_CHA_CON0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | awpoison_0<br>DDRCTL AXI write address poison<br>1'b1: Enable poison on write command<br>1'b0: Disable |
| 14 | RW | 0x0 | arpoison_0<br>DDRCTL AXI read address poison<br>1'b1: Enable poison on read command<br>1'b0: Disable |
| 13 | RW | 0x0 | awurgent_0<br>DDRCTL AXI write address urgent<br>1'b1: Current aw command is urgent<br>1'b0: Not urgent |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | arurgent_0<br>DDRCTL AXI read address urgent<br>1'b1: Current ar command is urgent<br>1'b0: Not urgent |
| 11:9 | RO | 0x0 | reserved |
| 8 | RW | 0x0 | dis_regs_ecc_syndrome<br>Value of dis_regs_ecc_syndrome.<br>Signal used to hide the value of ECCCSYN* and ECCUSYN* registers for security purposes. When this value is set to 1, reading registers ECCCSYN*/ECCUSYN* returns value 0 always, otherwise it returns appropriate value. If this feature is not used, this port can be tied to 0.<br>The value of dis_regs_ecc_syndrome signal cannot change outside of reset(presetn=0 && core_ddrc_core_rstn=0). |
| 7 | RO | 0x0 | reserved |
| 6 | RW | 0x1 | axi_order_en<br>Enable preserve DDRCTL AXI cmd order counter<br>1'b1: Enable<br>1'b0: Disable<br>Please keep default 1'b1 all the time. |
| 5 | RW | 0x0 | ddrctl_a_sysreq_sel<br>DDRCTL AXI hardware low power request by PMU<br>1'b1: DDRCTL AXI hardware low power request is driven by PMU.<br>1'b0: DDRCTL AXI hardware low power request is not driven by PMU. |
| 4 | RW | 0x0 | ddrctl_slverr_enable<br>DDRCTL slave APB error response enable<br>1'b0: Disable DDRCTL from responding error<br>1'b1: Enable DDRCTL from responding error |
| 3:0 | RO | 0x0 | reserved |

**DDR_GRF_CHA_CON1**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:13 | RW | 0x0 | dfi_phyupd_type<br>This signal is the DFI PHY-initiated update. This signal indicates which one of the four types of PHY update times is being requested by the dfi_phyupd_req signal.<br>The valid values are as follows:<br>2'b00: Tphyupd_type0<br>2'b01: Tphyupd_type1<br>2'b10: Tphyupd_type2<br>2'b11: Tphyupd_type3 |
| 12:8 | RO | 0x00 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x1 | cg_en_ddrphy_mode<br>DDRPHY ctrl_phy_cg_en gate control mode<br>1'b1: Ctrl_phy_cg_en is set to 1'b1 to gate DDRPHY internal clock according to the status of DDRPHY dfi_phyupd_req or dfi_phymstr_active or when DDRCTL AXI aclk and core clk are both gated.<br>1'b0: Ctrl_phy_cg_en is set to 1'b1 to gate DDRPHY internal clock according to the status of DDRPHY dfi_phyupd_req or dfi_phymstr_active. |
| 6 | RW | 0x0 | pmu_ddrphy_gate_en<br>Enable PMU auto gate DDRPHY clock function<br>If it is set 1'b1, ctrl_phy_cg_en of DDRPHY will be controlled by PMU.<br>1'b1: Enable<br>1'b0: Disable |
| 5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | ddrctl_syscreq_cg_en<br>DDRCTL core clk gate enable during SR-PD<br>1'b1: Enable<br>1'b0: Disable |
| 3 | RW | 0x0 | selfref_type2_en<br>DDRCTL selfrefresh type for auto gate<br>1'b0: SDRAM is in SR-Powerdown (LPDDR4/5), which was caused by automatic self refresh only. If retry is enabled, this guarantees SRE command is executed correctly without parity error.<br>1'b1: SDRAM is in SR-Powerdown (LPDDR4/5), which was not caused solely under automatic self refresh control. It could have been caused by hardware low power interface and/or software (PWRCTL.selfref_sw). If retry is enabled, this guarantees SRE command is executed correctly without parity error. |
| 2 | RW | 0x0 | ddrctl_core_cg_en<br>DDRCTL core clk gate enable<br>1'b1: Enable DDRCTL core clk auto gate<br>1'b0: Disable |
| 1 | RW | 0x0 | ddrctl_apb_cg_en<br>DDRCTL APB pclk gate enable<br>1'b1: Enable DDRCTL pclk auto gate<br>1'b0: Disable |
| 0 | RW | 0x0 | ddrctl_axi_cg_en<br>DDRCTL AXI aclk gate enable<br>1'b1: Enable DDRCTL AXI auto gate<br>1'b0: Disable |

**DDR_GRF_CHA_CON2**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x0 | csysreq_ddrctl_ddr_gate<br>DDRCTL core hardware low power request by hardware gate control logic<br>1'b1: DDRCTL core hardware low power request is driven by hardware gate control logic.<br>1'b0: DDRCTL core hardware low power request is not driven by hardware gate control logic. |
| 14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | csysreq_ddrctl_pmu<br>DDRCTL core hardware low power request by PMU<br>1'b1: DDRCTL core hardware low power request is driven by PMU.<br>1'b0: DDRCTL core hardware low power request is not driven by PMU. |
| 12 | RW | 0x0 | csysreq_aclk_ddr_gate<br>DDRCTL AXI hardware low power request by hardware gate control logic<br>1'b1: DDRCTL AXI hardware low power request is driven by hardware gate control logic.<br>1'b0: DDRCTL AXI hardware low power request is not driven by hardware gate control logic. |
| 11 | RW | 0x0 | csysreq_aclk<br>DDRCTL AXI hardware low power request by GRF<br>1'b1: DDRCTL AXI hardware low power request is driven by DDR01_GRF or DDR23_GRF.<br>1'b0: DDRCTL AXI hardware low power request is not driven by DDR01_GRF or DDR23_GRF. |
| 10 | RW | 0x0 | cg_en_ddrphy<br>Enable DDRPHY ctrl_phy_cg_en auto gate function<br>1'b1: Enable<br>1'b0: Disable |
| 9 | RW | 0x0 | cg_en_axi<br>Enable DDRCTL hardware mode AXI aclk auto gate function<br>1'b1: Enable<br>1'b0: Disable |
| 8 | RW | 0x0 | cg_en_core<br>Enable DDRCTL hardware mode core clk auto gate function<br>1'b1: Enable<br>1'b0: Disable |
| 7:6 | RW | 0x0 | pre_dfi0_cs_combo_P3<br>These grf bits drive dfi_cs_P3 |
| 5:4 | RW | 0x0 | pre_dfi0_cs_combo_P2<br>These grf bits drive dfi_cs_P2 |
| 3:2 | RW | 0x0 | pre_dfi0_cs_combo_P1<br>These grf bits drive dfi_cs_P1 |
| 1:0 | RW | 0x0 | pre_dfi0_cs_combo_P0<br>These grf bits drive dfi_cs_P0 |

**DDR_GRF_CHA_CON3**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:8 | RW | 0x00 | silent_threshold_axi<br>Control after how many silent cycles, auto gate will gate DDRCTL aclk |
| 7:0 | RW | 0x00 | silent_threshold_core<br>Control after how many silent cycles, auto gate will gate DDRCTL core clk. |

**DDR_GRF_CHA_CON4**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RW | 0x00 | exit_threshold_axi<br>Exit time from gating DDRCTL aclk |
| 7:0 | RW | 0x00 | silent_threshold_ddrphy<br>Control after how many silent cycles, auto gate will enable ctrl_phy_cg_en to gate DDRPHY clock. |

**DDR_GRF_CHA_CON5**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RW | 0x00 | silent_threshold_rs<br>Control after how many silent cycles, auto gate will gate rs bridge clock<br>Rs bridge is a module to add one pipeline for AXI bus. |
| 7:0 | RW | 0x00 | exit_threshold_core<br>Exit time from gating DDRCTL core clk |

**DDR_GRF_CHA_CON6**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RW | 0x00 | wr_lat_delay<br>Control dfi_lp_data_req high level time during write |
| 7:0 | RW | 0x00 | rd_lat_delay<br>Control dfi_lp_data_req high level time during read |

**DDR_GRF_CHA_CON7**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:13 | RW | 0x0 | mem_cfg_uhdpdprf_interconnect_i_16_18<br>Control the mem_cfg bit 16-18 for uhdpdprf for interconnect.<br>bit 0: TESTRWM |
| 12:5 | RO | 0x00 | reserved |
| 4 | RW | 0x1 | ddr_axi_order_en<br>Enable preserve DDR scheduler AXI cmd order counter<br>1'b1: Enable<br>1'b0: Disable<br>Please keep default 1'b1 all the time. |
| 3 | RW | 0x0 | ddr_scramble_gate_en<br>Enable auto gate ddr scramble clock between DDR scheduler and DDRCTL<br>1'b1: Enable<br>1'b0: Disable |
| 2 | RW | 0x0 | ddr_frs_scramble_gate_en<br>Enable auto gate ddr scramble frs clock between DDR scheduler and DDRCTL<br>1'b1: Enable<br>1'b0: Disable |
| 1 | RW | 0x0 | ddr_frs_gate_en<br>Enable auto gate ddr frs clock between DDR scheduler and DDRCTL<br>1'b1: Enable<br>1'b0: Disable |
| 0 | RW | 0x0 | ddr_rs_gate_en<br>Enable auto gate ddr rs clock between DDR scheduler and DDRCTL<br>1'b1: Enable<br>1'b0: Disable |

**DDR_GRF_CHA_CON8**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x1f4a | mem_cfg_uhdpdprf_interconnect_i_0_15<br>Control the mem_cfg bit 0-15 for uhdpdprf for interconnect.<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMDA<br>bit 7: LS |

**DDR_GRF_CHA_CON9**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x0 | ddrctl_a_auto_gate_en<br>Enable DDRCTL core hardware low power gate control logic<br>1'b1: Enable<br>1'b0: Disable |
| 14 | RW | 0x0 | ddrctl_auto_gate_en<br>Enable DDRCTL AXI hardware low power gate control logic<br>1'b1: Enable<br>1'b0: Disable |
| 13 | RW | 0x0 | ddrctl_bsm_cg_en<br>Enable DDRCTL bsm clock gate function<br>1'b1: Enable<br>1'b0: Disable |
| 12:10 | RO | 0x0 | reserved |
| 9:0 | RW | 0x3ff | ddrctl_clk_gate<br>Each bit will enable an internal auto gate function in DDRCTL<br>1'b1: Enable<br>1'b0: Disable |

**DDR_GRF_CHB_CON0**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | awpoison_0<br>DDRCTL AXI write address poison<br>1'b1: Enable poison on write command<br>1'b0: Disable |
| 14 | RW | 0x0 | arpoison_0<br>DDRCTL AXI read address poison<br>1'b1: Enable poison on read command<br>1'b0: Disable |
| 13 | RW | 0x0 | awurgent_0<br>DDRCTL AXI write address urgent<br>1'b1: Current aw command is urgent<br>1'b0: Not urgent |
| 12 | RW | 0x0 | arurgent_0<br>DDRCTL AXI read address urgent<br>1'b1: Current ar command is urgent<br>1'b0: Not urgent |
| 11:9 | RO | 0x0 | reserved |
| 8 | RW | 0x0 | dis_regs_ecc_syndrome<br>Value of dis_regs_ecc_syndrome.<br>Signal used to hide the value of ECCCSYN* and ECCUSYN* registers for security purposes. When this value is set to 1, reading registers ECCCSYN*/ECCUSYN* returns value 0 always, otherwise it returns appropriate value. If this feature is not used, this port can be tied to 0.<br>The value of dis_regs_ecc_syndrome signal cannot change outside of reset(presetn=0 && core_ddrc_core_rstn=0). |
| 7 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x1 | axi_order_en<br>Enable preserve DDRCTL AXI cmd order counter<br>1'b1: Enable<br>1'b0: Disable<br>Please keep default 1'b1 all the time. |
| 5 | RW | 0x0 | ddrctl_a_sysreq_sel<br>DDRCTL AXI hardware low power request by PMU<br>1'b1: DDRCTL AXI hardware low power request is driven by PMU.<br>1'b0: DDRCTL AXI hardware low power request is not driven by PMU. |
| 4 | RW | 0x0 | ddrctl_slverr_enable<br>DDRCTL slave APB error response enable<br>1'b0: Disable DDRCTL from responding error<br>1'b1: Enable DDRCTL from responding error |
| 3:0 | RO | 0x0 | reserved |

**DDR_GRF_CHB_CON1**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:13 | RW | 0x0 | dfi_phyupd_type<br>This signal is the DFI PHY-initiated update. This signal indicates which one of the four types of PHY update times is being requested by the dfi_phyupd_req signal.<br>The valid values are as follows:<br>2'b00: Tphyupd_type0<br>2'b01: Tphyupd_type1<br>2'b10: Tphyupd_type2<br>2'b11: Tphyupd_type3 |
| 12:8 | RO | 0x00 | reserved |
| 7 | RW | 0x1 | cg_en_ddrphy_mode<br>DDRPHY ctrl_phy_cg_en gate control mode<br>1'b1: Ctrl_phy_cg_en is set to 1'b1 to gate DDRPHY internal clock according to the status of DDRPHY dfi_phyupd_req or dfi_phymstr_active or when DDRCTL AXI aclk and core clk are both gated.<br>1'b0: Ctrl_phy_cg_en is set to 1'b1 to gate DDRPHY internal clock according to the status of DDRPHY dfi_phyupd_req or dfi_phymstr_active. |
| 6 | RW | 0x0 | pmu_ddrphy_gate_en<br>Enable PMU auto gate DDRPHY clock function<br>If it is set 1'b1, ctrl_phy_cg_en of DDRPHY will be controlled by PMU.<br>1'b1: Enable<br>1'b0: Disable |
| 5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | ddrctl_syscreq_cg_en<br>DDRCTL core clk gate enable during SR-PD<br>1'b1: Enable<br>1'b0: Disable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | selfref_type2_en<br>DDRCTL selfrefresh type for auto gate<br>1'b0: SDRAM is in SR-Powerdown (LPDDR4/5), which was caused by automatic self refresh only. If retry is enabled, this guarantees SRE command is executed correctly without parity error.<br>1'b1: SDRAM is in SR-Powerdown (LPDDR4/5), which was not caused solely under automatic self refresh control. It could have been caused by hardware low power interface and/or software (PWRCTL.selfref_sw). If retry is enabled, this guarantees SRE command is executed correctly without parity error. |
| 2 | RW | 0x0 | ddrctl_core_cg_en<br>DDRCTL core clk gate enable<br>1'b1: Enable DDRCTL core clk auto gate<br>1'b0: Disable |
| 1 | RW | 0x0 | ddrctl_apb_cg_en<br>DDRCTL APB pclk gate enable<br>1'b1: Enable DDRCTL pclk auto gate<br>1'b0: Disable |
| 0 | RW | 0x0 | ddrctl_axi_cg_en<br>DDRCTL AXI aclk gate enable<br>1'b1: Enable DDRCTL AXI auto gate<br>1'b0: Disable |

**DDR_GRF_CHB_CON2**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | csysreq_upctl_ddr_gate<br>DDRCTL core hardware low power request by hardware gate control logic<br>1'b1: DDRCTL core hardware low power request is driven by hardware gate control logic.<br>1'b0: DDRCTL core hardware low power request is not driven by hardware gate control logic. |
| 14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | csysreq_upctl_pmu<br>DDRCTL core hardware low power request by PMU<br>1'b1: DDRCTL core hardware low power request is driven by PMU.<br>1'b0: DDRCTL core hardware low power request is not driven by PMU. |
| 12 | RW | 0x0 | csysreq_aclk_ddr_gate<br>DDRCTL AXI hardware low power request by hardware gate control logic<br>1'b1: DDRCTL AXI hardware low power request is driven by hardware gate control logic.<br>1'b0: DDRCTL AXI hardware low power request is not driven by hardware gate control logic. |

Rockchip Confidencial

Copyright 2022 © Rockchip Electronics Co., Ltd. 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11 | RW | 0x0 | csysreq_aclk<br>DDRCTL AXI hardware low power request by GRF<br>1'b1: DDRCTL AXI hardware low power request is driven by DDR01_GRF or DDR23_GRF.<br>1'b0: DDRCTL AXI hardware low power request is not driven by DDR01_GRF or DDR23_GRF. |
| 10 | RW | 0x0 | cg_en_ddrphy<br>Enable DDRPHY ctrl_phy_cg_en auto gate function<br>1'b1: Enable<br>1'b0: Disable |
| 9 | RW | 0x0 | cg_en_axi<br>Enable DDRCTL hardware mode AXI aclk auto gate function<br>1'b1: Enable<br>1'b0: Disable |
| 8 | RW | 0x0 | cg_en_core<br>Enable DDRCTL hardware mode core clk auto gate function<br>1'b1: Enable<br>1'b0: Disable |
| 7:6 | RW | 0x0 | pre_dfi0_cs_combo_P3<br>These grf bits drive dfi_cs_P3 |
| 5:4 | RW | 0x0 | pre_dfi0_cs_combo_P2<br>These grf bits drive dfi_cs_P2 |
| 3:2 | RW | 0x0 | pre_dfi0_cs_combo_P1<br>These grf bits drive dfi_cs_P1 |
| 1:0 | RW | 0x0 | pre_dfi0_cs_combo_P0<br>These grf bits drive dfi_cs_P0 |

**DDR_GRF_CHB_CON3**

Address: Operational Base + offset (0x003C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RW | 0x00 | silent_threshold_axi<br>Control after how many silent cycles, auto gate will gate DDRCTL aclk |
| 7:0 | RW | 0x00 | silent_threshold_core<br>Control after how many silent cycles, auto gate will gate DDRCTL core clk. |

**DDR_GRF_CHB_CON4**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RW | 0x00 | exit_threshold_axi<br>Exit time from gating DDRCTL aclk |
| 7:0 | RW | 0x00 | silent_threshold_ddrphy<br>Control after how many silent cycles, auto gate will enable ctrl_phy_cg_en to gate DDRPHY clock. |

**DDR_GRF_CHB_CON5**

Rockchip Confidential

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | silent_threshold_rs<br>Control after how many silent cycles, auto gate will gate rs bridge clock<br>Rs bridge is a module to add one pipeline for AXI bus. |
| 0 | RW | 0x0 | exit_threshold_ddrc<br>Exit time from gating DDRCTL core clk |

**DDR_GRF_CHB_CON6**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RW | 0x00 | wr_lat_delay<br>Control dfi_lp_data_req high level time during write |
| 7:0 | RW | 0x00 | rd_lat_delay<br>Control dfi_lp_data_req high level time during read |

**DDR_GRF_CHB_CON7**

Address: Operational Base + offset (0x004C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RW | 0x0 | mem_cfg_uhdpdprf_interconnect_i_16_18<br>Control the mem_cfg bit 16-18 for uhdpdprf for interconnect.<br>bit 0: TESTRWM |
| 12:5 | RO | 0x00 | reserved |
| 4 | RW | 0x1 | ddr_axi_order_en<br>Enable preserve DDR scheduler AXI cmd order counter<br>1'b1: Enable<br>1'b0: Disable<br>Please keep default 1'b1 all the time. |
| 3 | RW | 0x0 | ddr_scramble_gate_en<br>Enable auto gate ddr scramble clock between DDR scheduler and DDRCTL<br>1'b1: Enable<br>1'b0: Disable |
| 2 | RW | 0x0 | ddr_frs_scramble_gate_en<br>Enable auto gate ddr scramble frs clock between DDR scheduler and DDRCTL<br>1'b1: Enable<br>1'b0: Disable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | ddr_frs_gate_en<br>Enable auto gate ddr frs clock between DDR scheduler and DDRCTL<br>1'b1: Enable<br>1'b0: Disable |
| 0 | RW | 0x0 | ddr_rs_gate_en<br>Enable auto gate ddr rs clock between DDR scheduler and DDRCTL<br>1'b1: Enable<br>1'b0: Disable |

**DDR_GRF_CHB_CON8**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x8010 | mem_cfg_uhdpdprf_interconnect_i_0_15<br>Control the mem_cfg bit 0-15 for uhdpdprf for interconnect.<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMDA<br>bit 7: LS |

**DDR_GRF_CHB_CON9**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | upctl_a_auto_gate_en<br>Enable DDRCTL core hardware low power gate control logic<br>1'b1: Enable<br>1'b0: Disable |
| 14 | RW | 0x0 | upctl_auto_gate_en<br>Enable DDRCTL AXI hardware low power gate control logic<br>1'b1: Enable<br>1'b0: Disable |
| 13 | RW | 0x0 | ddrc_bsm_cg_en<br>Enable DDRCTL bsm clock gate function<br>1'b1: Enable<br>1'b0: Disable |
| 12:10 | RO | 0x0 | reserved |
| 9:0 | RW | 0x3ff | ddr_clk_gate<br>Each bit will enable an internal auto gate function in DDRCTL<br>1'b1: Enable<br>1'b0: Disable |

**DDR_GRF_CHA_STATUS0**

Address: Operational Base + offset (0x0060)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | st_mrr_data0<br>MRR data from DDRCTL |

**DDR_GRF_CHA_STATUS16**

Address: Operational Base + offset (0x00A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:11 | RO | 0x000000 | reserved |
| 10 | RO | 0x0 | st_write_overflow<br>DDR scramble write overflow status<br>1'b0: Not overflow<br>1'b1: Overflow |
| 9 | RO | 0x0 | st_read_overflow<br>DDR scramble read overflow status<br>1'b0: Not overflow<br>1'b1: Overflow |
| 8 | RO | 0x0 | scramble_shift_ready<br>Scramble shift ready status<br>1'b0: Not ready<br>1'b1: Ready |
| 7:6 | RO | 0x0 | st_stat_ddrc_reg_selfref_type<br>DDRCTL selfrefresh type status<br>Flags if SR-Powerdown is entered and if it was under automatic self<br>refresh control only or not.<br>2'b00: SDRAM is not in SR-Powerdown.<br>2'b01: SDRAM is in self refresh, which was caused by PHY master request.<br>2'b10: SDRAM is in SR-Powerdown, which was not caused solely under automatic self refresh control.<br>2'b11: SDRAM is in SR-Powerdown, which was caused by automatic self refresh only. |
| 5 | RO | 0x0 | st_cactive_aclk<br>DDRCTL aclk cactive status<br>1'b0: Not active<br>1'b1: Active |
| 4 | RO | 0x0 | st_csysack_aclk<br>DDRCTL aclk csysack status<br>1'b0: Low power request is acknowledged.<br>1'b0: Low power request is not acknowledged. |
| 3 | RO | 0x0 | st_csysreq_aclk<br>DDRCTL aclk csysreq status<br>1'b0: Low power request<br>1'b1: No low power request |
| 2 | RO | 0x0 | st_cactive_ddrc<br>DDRCTL core cactive status<br>1'b0: Not active<br>1'b1: Active |
| 1 | RO | 0x0 | st_csysack_ddrc<br>DDRCTL core low power ack status<br>1'b0: Low power request is acknowledged.<br>1'b0: Low power request is not acknowledged. |
| 0 | RO | 0x0 | st_csysreq_ddrc<br>DDRCTL core low power request status<br>1'b0: Low power request.<br>1'b1: No low power request. |

Rockchip Confidencial

**DDR_GRF_CHA_STATUS17**

Address: Operational Base + offset (0x00A4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |
| 30:24 | RO | 0x00 | st_wrecc_credit_cnt<br>DDRCTL wrecc credit count |
| 23 | RO | 0x0 | reserved |
| 22:16 | RO | 0x00 | st_wr_credit_cnt<br>DDRCTL wr credit count |
| 15 | RO | 0x0 | reserved |
| 14:8 | RO | 0x00 | st_hpr_credit_cnt<br>DDRCTL hpr credit count |
| 7 | RO | 0x0 | reserved |
| 6:0 | RO | 0x00 | st_lpr_credit_cnt<br>DDRCTL lpr credit count |

**DDR_GRF_CHA_STATUS19**

Address: Operational Base + offset (0x00AC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:18 | RO | 0x0 | st_derate_temp_limit_intr_fault<br>This signal is the derate temperature limit fault. This is a version of derate_temp_limit_intr, which can not be disabled or forced via a register. It is a 2-bit antivalent signal with encoding as follows:<br>2'b01: No Fault<br>2'b10: Fault Detected |
| 17:16 | RO | 0x0 | st_rd_linkecc_corr_err_intr_fault<br>This signal is the read Link-ECC corrected error fault. This is a version of rd_linkecc_corr_err_intr which can not be disabled or forced through a register. It is a 2-bit antivalent signal with encoding of<br>2'b01: No Fault<br>2'b10: Fault Detected |
| 15:14 | RO | 0x0 | st_rd_linkecc_uncorr_err_intr_fault<br>This signal is the read Link-ECC uncorrected error fault. This is a version of rd_linkecc_uncorr_err_intr, which can not be disabled or forced through a register. It is a 2-bit antivalent signal with encoding as follows:<br>2'b01: No Fault<br>2'b10: Fault Detected |
| 13:12 | RO | 0x0 | st_ecc_ap_err_intr_fault<br>This signal is the ECC address protection fault. This is a version of ecc_ap_err_intr which can not be disabled or forced through a register.<br>It is a 2-bit antivalent signal with encoding as follows:<br>2'b01: No Fault<br>2'b10: Fault Detected |
| 11:10 | RO | 0x0 | st_ecc_uncorrected_err_intr_fault<br>This signal is the ECC uncorrected error fault. This is a version of ecc_uncorrected_err_intr which can not be disabled or forced through a register. It is a 2-bit antivalent signal with encoding as follows:<br>2'b01: No Fault<br>2'b10: Fault Detected |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9:8 | RO | 0x0 | st_ecc_corrected_err_intr_fault<br>This signal is the ECC corrected error fault. This is a version of ecc_corrected_err_intr which can not be disabled or forced through register. It is a 2-bit antivalent signal with encoding as follows:<br>2'b01: No Fault<br>2'b10: Fault Detected |
| 7:6 | RO | 0x0 | reserved |
| 5:0 | RO | 0x00 | st_hif_refresh_req_bank<br>This signal indicates the next bank that is refreshed (channel 1); for multi-rank configurations, the bank number is reported independently for each rank, and the information for all ranks is concatenated to form this signal. |

**DDR_GRF_CHB_STATUS0**

Address: Operational Base + offset (0x00B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | st_mrr_data0<br>MRR data from DDRCTL |

**DDR_GRF_CHB_STATUS16**

Address: Operational Base + offset (0x00F0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:11 | RO | 0x000000 | reserved |
| 10 | RO | 0x0 | st_write_overflow<br>DDR scramble write overflow status<br>1'b0: Not overflow<br>1'b1: Overflow |
| 9 | RO | 0x0 | st_read_overflow<br>DDR scramble read overflow status<br>1'b0: Not overflow<br>1'b1: Overflow |
| 8 | RO | 0x0 | scramble_shift_ready<br>Scramble shift ready status<br>1'b0: Not ready<br>1'b1: Ready |
| 7:6 | RO | 0x0 | st_ddrc_reg_selfref_type<br>DDRCTL selfrefresh type status<br>Flags if SR-Powerdown is entered and if it was under automatic self<br>refresh control only or not.<br>2'b00: SDRAM is not in SR-Powerdown.<br>2'b01: SDRAM is in self refresh, which was caused by PHY master request.<br>2'b10: SDRAM is in SR-Powerdown, which was not caused solely under automatic self refresh control.<br>2'b11: SDRAM is in SR-Powerdown, which was caused by automatic self refresh only. |
| 5 | RO | 0x0 | st_cactive_aclk<br>DDRCTL aclk cactive status<br>1'b0: Not active<br>1'b1: Active |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RO | 0x0 | st_csysack_aclk<br>DDRCTL aclk csysack status<br>1'b0: Low power request is acknowledged.<br>1'b0: Low power request is not acknowledged. |
| 3 | RO | 0x0 | st_csysreq_aclk<br>DDRCTL aclk csysreq status<br>1'b0: Low power request<br>1'b1: No low power request |
| 2 | RO | 0x0 | st_cactive_ddrc<br>DDRCTL core cactive status<br>1'b0: Not active<br>1'b1: Active |
| 1 | RO | 0x0 | st_csysack_ddrc<br>DDRCTL core low power ack status<br>1'b0: Low power request is acknowledged.<br>1'b0: Low power request is not acknowledged. |
| 0 | RO | 0x0 | st_csysreq_ddrc<br>DDRCTL core low power request status<br>1'b0: Low power request.<br>1'b1: No low power request. |

**DDR_GRF_CHB_STATUS17**

Address: Operational Base + offset (0x00F4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |
| 30:24 | RO | 0x00 | st_wrecc_credit_cnt<br>DDRCTL wrecc credit count |
| 23 | RO | 0x0 | reserved |
| 22:16 | RO | 0x00 | st_wr_credit_cnt<br>DDRCTL wr credit count |
| 15 | RO | 0x0 | reserved |
| 14:8 | RO | 0x00 | st_hpr_credit_cnt<br>DDRCTL hpr credit count |
| 7 | RO | 0x0 | reserved |
| 6:0 | RO | 0x00 | st_lpr_credit_cnt<br>DDRCTL lpr credit count |

**DDR_GRF_CHB_STATUS19**

Address: Operational Base + offset (0x00FC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:18 | RO | 0x0 | st_derate_temp_limit_intr_fault<br>This signal is the derate temperature limit fault. This is a version of derate_temp_limit_intr, which can not be disabled or forced via a register. It is a 2-bit antivalent signal with encoding as follows:<br>2'b01: No Fault<br>2'b10: Fault Detected |
| 17:16 | RO | 0x0 | st_rd_linkecc_corr_err_intr_fault<br>This signal is the read Link-ECC corrected error fault. This is a version of rd_linkecc_corr_err_intr which can not be disabled or forced through a register. It is a 2-bit antivalent signal with encoding of<br>2'b01: No Fault<br>2'b10: Fault Detected |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:14 | RO | 0x0 | st_rd_linkecc_uncorr_err_intr_fault<br>This signal is the read Link-ECC uncorrected error fault. This is a version of rd_linkecc_uncorr_err_intr, which can not be disabled or forced through a register. It is a 2-bit antivalent signal with encoding as follows:<br>2'b01: No Fault<br>2'b10: Fault Detected |
| 13:12 | RO | 0x0 | st_ecc_ap_err_intr_fault<br>This signal is the ECC address protection fault. This is a version of ecc_ap_err_intr which can not be disabled or forced through a register.<br>It is a 2-bit antivalent signal with encoding as follows:<br>2'b01: No Fault<br>2'b10: Fault Detected |
| 11:10 | RO | 0x0 | st_ecc_uncorrected_err_intr_fault<br>This signal is the ECC uncorrected error fault. This is a version of ecc_uncorrected_err_intr which can not be disabled or forced through a register. It is a 2-bit antivalent signal with encoding as follows:<br>2'b01: No Fault<br>2'b10: Fault Detected |
| 9:8 | RO | 0x0 | st_ecc_corrected_err_intr_fault<br>This signal is the ECC corrected error fault. This is a version of ecc_corrected_err_intr which can not be disabled or forced through register. It is a 2-bit antivalent signal with encoding as follows:<br>2'b01: No Fault<br>2'b10: Fault Detected |
| 7:6 | RO | 0x0 | reserved |
| 5:0 | RO | 0x00 | st_hif_refresh_req_bank<br>This signal indicates the next bank that is refreshed (channel 1); for multi-rank configurations, the bank number is reported independently for each rank, and the information for all ranks is concatenated to form this signal. |

**DDR_GRF_CHA_PHY_CON0**

Address: Operational Base + offset (0x0130)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | ddrphy_pclk_cg_en<br>DDRPHY APB pclk clock gate enable<br>1'b1: Enable<br>1'b0: Disable |
| 13 | RW | 0x0 | ctrl_clkm_cg_en<br>DDRPHY master DLL clock gating enable.<br>1'b0: DDRPHY master DLL clock gating is disabled.<br>1'b1: DDRPHY master DLL clock gating is enabled. |
| 12:11 | RW | 0x0 | dfi_phymstr_type<br>Value of dfi_phymstr_type |
| 10 | RW | 0x1 | dfi_phymstr_state_sel<br>Value of dfi_phymastr_state_sel |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9:8 | RW | 0x0 | dfi_phymstr_cs_state<br>Value of dfi_phymstr_cs_state |
| 7 | RW | 0x0 | dfi_init_start<br>Value of dfi_init_start |
| 6 | RW | 0x0 | dfi_init_start_sel<br>DDRPHY dfi_init_start select<br>1'b0: DDRPHY dfi_init_start is driven by DDRCTL<br>1'b1: DDRPHY dfi_init_start is driven by DDR01_GRF or DDR23_GRF |
| 5 | RW | 0x0 | dfi_init_complete<br>Value of dfi_init_complete |
| 4 | RW | 0x0 | dfi_init_complete_sel<br>DDRCTL dfi_init_complete select<br>1'b0: DDRCTL dfi_init_complete is driven by DDRPHY<br>1'b1: DDRCTL dfi_init_complete is driven by DDR01_GRF or DDR23_GRF |
| 3 | RW | 0x0 | ddrphy2xclkgate_enable<br>Root clock gating control of DDRPHY. It controls clock gating of clk_phy2x. Set this pin to low to enable clock gating for clk_phy2x. For normal operation and DDRPHY test mode, this pin should be high. Root clock gating should be enabled while dfi_dram_clk_disable=1'b1. |
| 2 | RW | 0x0 | i_g_drcg_en<br>Dynamic regional clock gating control for DDRPHY. DRCG refers to clock gating controlled by pcl_pd field in LP_CON0 register.<br>1'b1: DRCG is enabled regardless of pcl_pd field<br>1'b0: DRCG will be controlled by pcl_pd field in LP_CON0 |
| 1:0 | RW | 0x0 | dvfs_clk_mode<br>DVFS mode select for clock mode between DFI clock and DFI PHY clock. This signal controls which DVFS register sets will be used after frequency change.<br>2'b00: Normal mode<br>2'b01: DVFS0 mode<br>2'b10: DVFS1 mode |

**DDR_GRF_CHB_PHY_CON0**

Address: Operational Base + offset (0x0134)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | ddrphy_pclk_cg_en<br>DDRPHY APB pclk clock gate enable<br>1'b1: Enable<br>1'b0: Disable |
| 13 | RW | 0x0 | ctrl_clkm_cg_en<br>DDRPHY master DLL clock gating enable.<br>1'b0: DDRPHY master DLL clock gating is disabled.<br>1'b1: DDRPHY master DLL clock gating is enabled. |
| 12:11 | RW | 0x0 | dfi_phymstr_type<br>Value of dfi_phymstr_type |
| 10 | RW | 0x1 | dfi_phymstr_state_sel<br>Value of dfi_phymastr_state_sel |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9:8 | RW | 0x0 | dfi_phymstr_cs_state<br>Value of dfi_phymstr_cs_state |
| 7 | RW | 0x0 | dfi_init_start<br>Value of dfi_init_start |
| 6 | RW | 0x0 | dfi_init_start_sel<br>DDRPHY dfi_init_start select<br>1'b0: DDRPHY dfi_init_start is driven by DDRCTL<br>1'b1: DDRPHY dfi_init_start is driven by DDR01_GRF or DDR23_GRF |
| 5 | RW | 0x0 | dfi_init_complete<br>Value of dfi_init_complete |
| 4 | RW | 0x0 | dfi_init_complete_sel<br>DDRCTL dfi_init_complete select<br>1'b0: DDRCTL dfi_init_complete is driven by DDRPHY<br>1'b1: DDRCTL dfi_init_complete is driven by DDR01_GRF or DDR23_GRF |
| 3 | RW | 0x0 | ddrphy2xclkgate_enable<br>Root clock gating control of DDRPHY. It controls clock gating of clk_phy2x. Set this pin to low to enable clock gating for clk_phy2x. For normal operation and DDRPHY test mode, this pin should be high. Root clock gating should be enabled while dfi_dram_clk_disable=1'b1. |
| 2 | RW | 0x0 | i_g_drcg_en<br>Dynamic regional clock gating control for DDRPHY. DRCG refers to clock gating controlled by pcl_pd field in LP_CON0 register.<br>1'b1: DRCG is enabled regardless of pcl_pd field<br>1'b0: DRCG will be controlled by pcl_pd field in LP_CON0 |
| 1:0 | RW | 0x0 | dvfs_clk_mode<br>DVFS mode select for clock mode between DFI clock and DFI PHY clock. This signal controls which DVFS register sets will be used after frequency change.<br>2'b00: Normal mode<br>2'b01: DVFS0 mode<br>2'b10: DVFS1 mode |

**DDR_GRF_CHA_PHY_STATUS0**

Address: Operational Base + offset (0x0138)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4 | RO | 0x0 | st_dfi_init_complete<br>Dfi_init_complete status |
| 3 | RO | 0x0 | st_dfi_init_start<br>Dfi_init_start status |
| 2 | RO | 0x0 | st_ddrphy2xclkgate_enout<br>Status of ddrphy2xclkgate_enout signal. This is a feed-through signal of ddrphy2xclkgate_enable. This signal can be monitored to get the status of ddrphy2xclkgate_enable signal. |
| 1 | RO | 0x0 | st_dfi_phymstr_active<br>DDRPHY phymstr_active status |
| 0 | RO | 0x0 | st_dfi_error<br>DDRPHY dfi error status<br>Indicates that the DDRPHY has detected an error condition such as read FIFO pointer error, conflict DLL update and wrdata and conflict DLL update and rddata. |

Rockchip Confidential

**DDR_GRF_CHB_PHY_STATUS0**

Address: Operational Base + offset (0x013C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4 | RO | 0x0 | st_dfi_init_complete<br>Dfi_init_complete status |
| 3 | RO | 0x0 | st_dfi_init_start<br>Dfi_init_start status |
| 2 | RO | 0x0 | st_ddrphy2xclkgate_enout<br>Status of ddrphy2xclkgate_enout signal. This is a feed-through signal of ddrphy2xclkgate_enable. This signal can be monitored to get the status of ddrphy2xclkgate_enable signal. |
| 1 | RO | 0x0 | st_dfi_phymstr_active<br>DDRPHY phymstr_active status |
| 0 | RO | 0x0 | st_dfi_error<br>DDRPHY dfi error status<br>Indicates that the DDRPHY has detected an error condition such as read FIFO pointer error, conflict DLL update and wrdata and conflict DLL update and rddata. |

**DDR_GRF_CON0**

Address: Operational Base + offset (0x0140)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23:0 | RW | 0x01adba | mem_cfg_hsdprf_ddrctl<br>Control the mem_cfg bit 0-21 for hsdprf for DDRCTL.<br>bit 0: TEST1A<br>bit 1: TEST_RNMA<br>bit 5~2: RMA<br>bit 6: WMDA<br>bit 8: LS<br>bit 14~13: RA<br>bit 17: TEST1B<br>bit 21~18: RMB |

# 6.10 CENTER_GRF Register Description

## 6.10.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CENTER_GRF_SOC_CON0 | 0x0000 | W | 0x00008010 | CENTER GRF Control Register 0 |
| CENTER_GRF_SOC_CON1 | 0x0004 | W | 0x00001410 | CENTER GRF Control Register 1 |
| CENTER_GRF_SOC_CON2 | 0x0008 | W | 0x00008010 | CENTER GRF Control Register 2 |
| CENTER_GRF_SOC_CON3 | 0x000C | W | 0x00001410 | CENTER GRF Control Register 3 |
| CENTER_GRF_SOC_CON4 | 0x0010 | W | 0x0000C000 | CENTER GRF Control Register 4 |
| CENTER_GRF_SOC_CON7 | 0x001C | W | 0x00000000 | CENTER GRF Control Register 7 |
| CENTER_GRF_SOC_CON8 | 0x0020 | W | 0x00000000 | CENTER GRF Control Register 8 |
| CENTER_GRF_SOC_STATUS1 | 0x0044 | W | 0x00000000 | CENTER GRF Status Register 1 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.10.2 Detail Registers Description

**CENTER_GRF_SOC_CON0**

Rockchip Confidential

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:19 | RO | 0x0000 | reserved |
| 18:0 | RW | 0x08010 | mem_cfg_uhdpdprf_dma2ddr_i<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMDA<br>bit 7: LS |

**CENTER_GRF_SOC_CON1**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x1410 | mem_cfg_hdspra_shrm_i<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMD<br>bit 7: LS<br>bit 11~10: WPULSE<br>bit 13~12: RA |

**CENTER_GRF_SOC_CON2**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:19 | RO | 0x0000 | reserved |
| 18:0 | RW | 0x08010 | mem_cfg_uhdpdprf_interconnect_i<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMDA<br>bit 7: LS |

**CENTER_GRF_SOC_CON3**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x1410 | mem_cfg_hdsprf_ddrtcm_i<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMDA<br>bit 7: LS |

**CENTER_GRF_SOC_CON4**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | grf_con_ddrch23_ena<br>1'b1: Enable simultaneously configure ddr ch2 and ddr ch3 function.<br>1'b0: Disable. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14 | RW | 0x1 | grf_con_ddrch01_ena<br>1'b1: Enable simultaneously configure ddr ch0 and ddr ch1 function.<br>1'b0: Disable. |
| 13:10 | RO | 0x0 | reserved |
| 9 | RW | 0x0 | grf_mcu_ddrcfg_mode_sel<br>1'b1: Enable mcu configure ddr mode.<br>1'b0: Disable. |
| 8:0 | RO | 0x0 | reserved |

**CENTER_GRF_SOC_CON7**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | grf_con_ddr_mcu_stcalib<br>Bit 0-23 provides an integer value to compute a 10ms delay from the reference clock is not implemented.<br>Bit 24<br>1'b0: If the system timer clock or SCLK , can guarantee an exact multiple of 10ms.<br>1'b1: System timer clock of SCLK can not guarantee an exact multiple of 10ms.<br>Bit 25 indicate no alternative reference clock source has been integrated. 1 means STCLKEN has been tie off. |

**CENTER_GRF_SOC_CON8**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:9 | RO | 0x000000 | reserved |
| 8 | RW | 0x0 | grf_con_wdt_pause_en<br>Center wdt pause enable.<br>Used to freeze the watchdog counter during pause mode.<br>High active. |
| 7:0 | RW | 0x00 | grf_con_ddr_mcu_irqlatency<br>Irqlatency specifies the minimum number of cycles between an interrupt that becomes pended in the NVIC, and the vector fetch for that interrupt being issued on the AHB-Lite interface. |

**CENTER_GRF_SOC_STATUS1**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | st_timer1_en<br>System timer 1 enable status. |
| 30 | RO | 0x0 | st_timer0_en<br>System timer 0 enable status. |
| 29 | RO | 0x0 | grf_st_ddr_mcu_deepsleep<br>Active only when SLEEPING is HIGH. Indicates that the SLEEPDEEP bit in the NVIC is set to 1. |
| 28 | RO | 0x0 | grf_st_ddr_mcu_sleeping<br>Indicates the processor is idle, waiting for an interrupt on either the IRQ, NMI, or internal SysTick, or HIGH level on RXEV. |
| 27 | RO | 0x0 | reserved |
| 26 | RO | 0x0 | grf_st_ddr_mcu_lockup<br>Indicates that the processor is in the architected lock-up state, as the result of an unrecoverable exception. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 25 | RO | 0x0 | grf_st_ddr_mcu_halted<br>Indicates that the processor is in debug state. HALTED remains asserted for as long as the processor remains in debug state. |
| 24 | RO | 0x0 | grf_st_ddr_mcu_txev<br>A single SCLK cycle HIGH level is generated on this output every time an SEV instruction is executed. |
| 23:0 | RO | 0x000000 | reserved |

# 6.11 GPU_GRF Register Description

## 6.11.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| GPU_GRF_PVTPLL_CON0_L | 0x0000 | W | 0x00000000 | PVTPLL Control Register 0 |
| GPU_GRF_PVTPLL_CON0_H | 0x0004 | W | 0x00000000 | PVTPLL Control Register 0 |
| GPU_GRF_PVTPLL_CON1 | 0x0008 | W | 0x00000018 | PVTPLL Control Register 1 |
| GPU_GRF_PVTPLL_CON2 | 0x000C | W | 0x00040000 | PVTPLL Control Register 2 |
| GPU_GRF_PVTPLL_CON3 | 0x0010 | W | 0x00000000 | PVTPLL Control Register 3 |
| GPU_GRF_MEMCFG_CON0 | 0x0024 | W | 0x00001410 | Memory Configuration Control Register 0 |
| GPU_GRF_MEMCFG_CON1 | 0x0028 | W | 0x00000010 | Memory Configuration Control Register 1 |
| GPU_GRF_CON0 | 0x0040 | W | 0x00000000 | GPU Control Register 0 |
| GPU_GRF_STATUS0 | 0x0044 | W | 0x00000000 | GPU Status Register 0 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.11.2 Detail Registers Description

**GPU_GRF_PVTPLL_CON0_L**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | bypass<br>1'b0: Support glitch-free frequency conversion.<br>1'b1: Not support. |
| 14:13 | RW | 0x0 | clk_div_osc<br>Frequency division factor for osc_clk. |
| 12:11 | RW | 0x0 | clk_div_ref<br>Frequency division factor for ref_clk. |
| 10:8 | RW | 0x0 | osc_ring_sel<br>Oscillator ring channel select. |
| 7:3 | RO | 0x00 | reserved |
| 2 | RW | 0x0 | out_polar<br>1'b0: Out=1 when need to increase voltage.<br>1'b1: Out=0 when need to increase voltage. |
| 1 | RW | 0x0 | osc_en<br>Oscillator ring enable. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | start<br>1'b1: PVTPLL monitor start. |

**GPU_GRF_PVTPLL_CON0_H**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5:0 | RW | 0x00 | ring_length_sel<br>Oscillator ring inverter length select. |

**GPU_GRF_PVTPLL_CON1**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000018 | cal_cnt<br>Target frequency value. |

**GPU_GRF_PVTPLL_CON2**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0004 | ckg_val<br>Clock gating interval control count value. |
| 15:0 | RW | 0x0000 | threshold<br>Count difference threshold value. |

**GPU_GRF_PVTPLL_CON3**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ref_cnt<br>Frequency measurement period setting value. |

**GPU_GRF_MEMCFG_CON0**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00001410 | memcfg_hdsprf<br>memory configuration of hdsprf type<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMD<br>bit 7: LS<br>bit 11~10: WPULSE<br>bit 13~12: RA |

**GPU_GRF_MEMCFG_CON1**

Address: Operational Base + offset (0x0028)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000010 | memcfg_uhdpdprf<br>memory configuration of uhdpdprf type.<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMDA<br>bit 7: LS |

**GPU_GRF_CON0**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x0 | protmode_en<br>gpu protected mode enable. |
| 5 | RW | 0x0 | halted_en<br>daplite2m halted enable. |
| 4 | RW | 0x0 | gpu_ckg_en<br>Clock gate enable. |
| 3:0 | RW | 0x0 | striping_granule<br>Memory striping control. This signal must be set during the GPU reset and remain static during operation. |

**GPU_GRF_STATUS0**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RO | 0x0 | swactive<br>Serial wire active. high when the debug port is operating using the serial wire protocol. |
| 0 | RO | 0x0 | dormantstate<br>Active-high status to indicate that none of the protocol engines are selected and that the DP is in dormant state. |

# 6.12 NPU_GRF Register Description

## 6.12.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| NPU_GRF_MEM_CON0 | 0x0000 | W | 0x00008010 | NPU memory configuration signal for uhdpdprf |
| NPU_GRF_MEM_CON1 | 0x0004 | W | 0x00001410 | NPU memory configuration signal for hdsprf |
| NPU_GRF_MEM_CON2 | 0x0008 | W | 0x00002010 | NPU memory configuration signal for hssprf |
| NPU_GRF_PVTPLL_CON0_L | 0x000C | W | 0x00000000 | Configure NPU PVTPLL Control 0 |
| NPU_GRF_PVTPLL_CON_H | 0x0010 | W | 0x00000000 | Configure NPU PVTPLL Control 0 |
| NPU_GRF_PVTPLL_CON1 | 0x0014 | W | 0x00000018 | Configure NPU PVTPLL Control 1 |

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| NPU_GRF_PVTPLL_CON2 | 0x0018 | W | 0x00000000 | Configure NPU PVTPLL Control 2 |
| NPU_GRF_PVTPLL_CON3 | 0x001C | W | 0x00000000 | Configure NPU PVTPLL Control 3 |
| NPU_GRF_NPUTOP_CON | 0x0024 | W | 0x00000000 | NPU power domain configure register |
| NPU_GRF_NPU_STS | 0x0028 | W | 0x00000000 | NPU power domain configure register |
| NPU_GRF_STCALIB_CON | 0x002C | W | 0x00000000 | NPU mcu stcalib control |
| NPU_GRF_CACHE_START | 0x0030 | W | 0x000F0000 | NPU mcu cache peripheral start address |
| NPU_GRF_CACHE_END | 0x0034 | W | 0x000FEFFF | NPU mcu cache peripheral end address |
| NPU_GRF_NPU_WQOS_CON | 0x0048 | W | 0x00000000 | NPU core AXI WQOS Control |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.12.2 Detail Registers Description

**NPU_GRF_MEM_CON0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16:0 | RW | 0x08010 | mem_cfg_uhddprf<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMDA<br>bit 7: LS<br>bit 16: TESTRWM |

**NPU_GRF_MEM_CON1**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x1410 | mem_cfg_hdsprf<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMD<br>bit 7: LS<br>bit 11~10: WPULSE<br>bit 13~12: RA |

**NPU_GRF_MEM_CON2**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:15 | RO | 0x00000 | reserved |
| 14:0 | RW | 0x2010 | npu_mem_hssprf<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMD<br>bit 7: LS |

**NPU_GRF_PVTPLL_CON0_L**

Rockchip Confidential

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | bypass<br>1'b0: Support glitch-free frequency conversion.<br>1'b1: Not support. |
| 14:13 | RW | 0x0 | clk_div_osc<br>Frequency division factor for osc_clk. |
| 12:11 | RW | 0x0 | clk_div_ref<br>Frequency division factor for ref_clk. |
| 10:8 | RW | 0x0 | osc_ring_sel<br>Oscillator ring channel select. |
| 7:3 | RO | 0x00 | reserved |
| 2 | RW | 0x0 | out_polar<br>1'b0: Out=1 when need to increase voltage.<br>1'b1: Out=0 when need to increase voltage. |
| 1 | RW | 0x0 | osc_en<br>Oscillator ring enable. |
| 0 | RW | 0x0 | start<br>PVTPLL monitor start control. |

**NPU_GRF_PVTPLL_CON_H**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:5 | RO | 0x000 | reserved |
| 5:0 | RW | 0x00 | ring_length_sel<br>Oscillator ring inverter length select. |

**NPU_GRF_PVTPLL_CON1**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |
| 30:0 | RW | 0x00000018 | cal_cnt<br>Target frequency value |

**NPU_GRF_PVTPLL_CON2**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | ckg_val<br>Clock gating interval control count value |
| 15:0 | RW | 0x0000 | threshold<br>Count difference threshold value |

**NPU_GRF_PVTPLL_CON3**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ref_cnt<br>Frequency measurement period setting value |

Rockchip Confidencial

**NPU_GRF_NPUTOP_CON**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11:10 | RW | 0x0 | cache_slv_memattr<br>Transaction memory attribute<br>When support mpu mode, the cache controller will cache the request if both the hprot[3] and memattr[0] is high on AHB slave bus, or will bypass the request. |
| 9 | RW | 0x0 | npu_mcu_cache_flush_req<br>Npu mcu cache memory flush request. |
| 8:1 | RW | 0x00 | npu_mcu_irqlatency<br>The processor supports zero jitter interrupt latency for zero wait-state memory.<br>IRQLATENCY specifies the minimum number of cycles between an interrupt that becomes pended in the NVIC, and the vector fetch for that interrupt being issued on the AHB-Lite interface. |
| 0 | RW | 0x0 | npu_wdt_pause<br>npu wdt pause enable.<br>Used to freeze the watchdog counter during pause mode.<br>High active |

**NPU_GRF_NPU_STS**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RO | 0x0 | npu_mcu_deepsleep<br>Active only when SLEEPING is HIGH. Indicates that the SLEEPDEEP bit in the NVIC is set to 1. |
| 6 | RO | 0x0 | npu_mcu_sleeping<br>Indicates the processor is idle, waiting for an interrupt on either the IRQ, NMI, or internal SysTick, or HIGH level on RXEV. |
| 5 | RO | 0x0 | npu_mcu_lockup<br>Indicates that the processor is in the architect lock-up state, as the result of an unrecoverable exception. |
| 4 | RO | 0x0 | npu_mcu_halted<br>Indicates that the processor is in debug state. HALTED remains asserted for as long as the processor remains in debug state. |
| 3 | RO | 0x0 | npu_mcu_cache_flush_ack<br>NPU MCU cache memory flush acknowledge. |
| 2 | RO | 0x0 | mcu_txev<br>A single SCLK cycle HIGH level is generated on this output every time an SEV instruction is executed on the MCU processor. |
| 1 | RO | 0x0 | npu_timer0_en<br>NPU timer0 clock enable state. If this signal is high, timer clock is enable. |
| 0 | RO | 0x0 | npu_timer1_en<br>NPU timer1 clock enable state. If this signal is high, timer clock is enable. |

**NPU_GRF_STCALIB_CON**

Rockchip Confidential

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |
| 25:0 | RW | 0x0000000 | npu_mcu_stcalib<br>Systick timer counter.<br>Stcalib[25]: Indicates that no alternative reference clock source has been integrated.<br>Stcalib[24]: Tie this LOW if the system timer clock, the external reference clock, or SCLK as indicated by STCALIB[25], can guarantee an exact multiple of 10ms.<br>Stcalib[23:0]: Indicates the processor is idle, waiting for an interrupt on either the IRQ, NMI, or internal SysTick, or HIGH level on RXEV. |

**NPU_GRF_CACHE_START**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xf0000 | cache_periphral_addr_start<br>NPU MCU cache peripheral start address. |

**NPU_GRF_CACHE_END**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfefff | cache_periphral_addr_start<br>NPU MCU cache peripheral end address. |

**NPU_GRF_NPU_WQOS_CON**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8:6 | RW | 0x0 | npu_core2_wqos<br>WQoS for NPU core2. |
| 5:3 | RW | 0x0 | npu_core1_wqos<br>WQoS for NPU core1. |
| 2:0 | RW | 0x0 | npu_core0_wqos<br>WQoS for NPU core0. |

# 6.13 VOP_GRF Register Description

## 6.13.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VOP_GRF_VOP_CON0 | 0x0000 | W | 0x00000000 | Video output system control register 0 |
| VOP_GRF_VOP_CON1 | 0x0004 | W | 0x00000000 | Video output system control register 1 |
| VOP_GRF_VOP_CON2 | 0x0008 | W | 0x00000000 | Video output system control register 2 |

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VOP_GRF_MEM_CON0 | 0x0010 | W | 0x00001410 | Video output system memory interface control register 0 |
| VOP_GRF_MEM_CON1 | 0x0014 | W | 0x00008010 | Video output system memory interface control register 1 |
| VOP_GRF_MEM_CON2 | 0x0018 | W | 0x00000010 | Video output system memory interface control register 2 |
| VOP_GRF_MEM_CON3 | 0x001C | W | 0x00008010 | Video output system memory interface control register 3 |
| VOP_GRF_MEM_CON4 | 0x0020 | W | 0x00000000 | Video output system memory interface control register 4 |
| VOP_GRF_MEM_CON5 | 0x0024 | W | 0x00000008 | Video output system memory interface control register 5 |
| VOP_GRF_MEM_CON6 | 0x0028 | W | 0x00000010 | Video output system memory interface control register 6 |
| VOP_GRF_MEM_CON7 | 0x002C | W | 0x00000011 | Video output system memory interface control register 7 |
| VOP_GRF_VOP_STS | 0x0030 | W | 0x00000000 | Video output system status register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.13.2 Detail Registers Description

**VOP_GRF_VOP_CON0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | dsihost0_txreqclkhs_ena<br>Enable phy_txskewcalhs condition for DSIHOST0 txrequestclkhs signal.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | dsihost0_gating_en<br>Enable clock gating for DSIHOST0.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | dsihost0_ipi_shutdn<br>Image pixel interface shutdown command for DSIHOST0.<br>1'b0: Shut down peripheral command request<br>1'b1: Turn on peripheral command request |
| 8 | RW | 0x0 | dsihost0_ipi_colorm<br>Image pixel interface color mode command for DSIHOST0.<br>1'b0: Color mode off command request<br>1'b1: Color mode on command request |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:4 | RW | 0x0 | dsihost0_ipi_color_depth<br>Image pixel interface color depth, only used when DSIHOST0 operates in auto mode.<br>4'h2: 5-6-5 bits<br>4'h3: 6 bits<br>4'h5: 8 bits<br>4'h6: 10 bits<br>Others: Reserved |
| 3:0 | RW | 0x0 | dsihost0_ipi_format<br>Image pixel interface video format, only used when DSIHOST0 operates in auto mode.<br>4'h0: RGB<br>4'hb: Compressed data<br>Others: Reserved |

**VOP_GRF_VOP_CON1**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | dsihost1_txreqclkhs_ena<br>Enable phy_txskewcalhs condition for DSIHOST1 txrequestclkhs signal.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | dsihost1_gating_en<br>Enable clock gating for DSIHOST1.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | dsihost1_ipi_shutdn<br>Image pixel interface shutdown command for DSIHOST1.<br>1'b0: Shut down peripheral command request<br>1'b1: Turn on peripheral command request |
| 8 | RW | 0x0 | dsihost1_ipi_colorm<br>Image pixel interface color mode command for DSIHOST1.<br>1'b0: Color mode off command request<br>1'b1: Color mode on command request |
| 7:4 | RW | 0x0 | dsihost1_ipi_color_depth<br>Image pixel interface color depth, only used when DSIHOST1 operates in auto mode.<br>4'h2: 5-6-5 bits<br>4'h3: 6 bits<br>4'h5: 8 bits<br>4'h6: 10 bits<br>Others: Reserved |
| 3:0 | RW | 0x0 | dsihost1_ipi_format<br>Image pixel interface video format, only used when DSIHOST1 operates in auto mode.<br>4'h0: RGB<br>4'hb: Compressed data<br>Others: Reserved |

Rockchip Confidential

**VOP_GRF_VOP_CON2**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x0 | hdmitx1_compress_mode<br>Enable data compress for HDMITX interface 1 .<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | hdmitx1_mode<br>Enable HDMITX interface 1 .<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | edp1_mode<br>Enable EDP interface 1 .<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | hdmitx0_compress_mode<br>Enable data compress for HDMITX interface 0 .<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | hdmitx0_mode<br>Enable HDMITX interface 0 .<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | edp0_mode<br>Enable EDP interface 0 .<br>1'b0: Disable<br>1'b1: Enable |

**VOP_GRF_MEM_CON0**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x1410 | mem_cfg_hdsprf<br>Interface configuration for HDSPRF type memory in PD_VOP.<br>Bit[0]: TEST1<br>Bit[1]: TEST_RNM<br>Bit[4:2]: RM<br>Bit[5]: WMD<br>Bit[7]: LS<br>Bit[11:10]: WPULSE<br>Bit[13:12]: RA<br>Other bits: Reserved |

**VOP_GRF_MEM_CON1**

Address: Operational Base + offset (0x0014)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x8010 | mem_cfg_hsdpra_l16<br>Interface configuration for HSDPRA type memory in PD_VOP, lower 16 bits.<br>Bit[0]: TEST1A<br>Bit[1]: TEST_RNMA<br>Bit[4:2]: RMA<br>Bit[5]: WMDA<br>Bit[7]: LS<br>Bit[11:10]: WPULSE<br>Bit[13:12]: RA<br>Bit[15:14]: WA |

**VOP_GRF_MEM_CON2**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x010 | mem_cfg_hsdpra_h9<br>Interface configuration for HSDPRA type memory in PD_VOP, higher 9 bits.<br>Bit[0]: TEST1B<br>Bit[1]: TEST_RNMB<br>Bit[4:2]: RMB<br>Bit[5]: WMDB<br>Other bits: Reserved |

**VOP_GRF_MEM_CON3**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x8010 | mem_cfg_hddprf_l16<br>Interface configuration for HDDPRF type memory in PD_VOP, lower 16 bits.<br>Bit[0]: TEST1<br>Bit[1]: TEST_RNM<br>Bit[4:2]: RM<br>Bit[5]: WMD<br>Bit[7]: LS<br>Bit[11:10]: WPULSE<br>Bit[13:12]: RA<br>Bit[15:14]: WA |

**VOP_GRF_MEM_CON4**

Address: Operational Base + offset (0x0020)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:3 | RO | 0x0000 | reserved |
| 2:0 | RW | 0x0 | mem_cfg_hddprf_h3<br>Interface configuration for HDDPRF type memory in PD_VOP, higher 3 bits.<br>Bit[0]: TESTRWM<br>Other bits: Reserved |

**VOP_GRF_MEM_CON5**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6:0 | RW | 0x08 | mem_cfg_rom<br>Interface configuration for ROM in PD_VOP.<br>Bit[0]: TEST1<br>Bit[4:1]: RM<br>Other bits: Reserved |

**VOP_GRF_MEM_CON6**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0010 | mem_cfg_hsdprf_l16<br>Interface configuration for HSDPRF type memory in PD_VOP, lower 16 bits.<br>Bit[0]: TEST1A<br>Bit[1]: TEST_RNMA<br>Bit[5:2]: RMA<br>Bit[6]: WMDA<br>Bit[8]: LS<br>Bit[12:11]: WPULSE<br>Bit[14:13]: RA<br>Bit[15]: WA[0] |

**VOP_GRF_MEM_CON7**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:0 | RW | 0x11 | mem_cfg_hsdprf_h8<br>Interface configuration for HSDPRF type memory in PD_VOP, higher 8 bits.<br>Bit[0]: WA[1]<br>Bit[1]: TEST1B<br>Bit[5:2]: RMB<br>Other bits: Reserved |

**VOP_GRF_VOP_STS**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23 | RO | 0x0 | dsiphy1_l3_phyenable<br>Enable DSIPHY1 lane 3.<br>1'b0: Disable<br>1'b1: Enable |
| 22 | RO | 0x0 | dsiphy1_l2_phyenable<br>Enable DSIPHY1 lane 2.<br>1'b0: Disable<br>1'b1: Enable |
| 21 | RO | 0x0 | dsiphy1_l1_phyenable<br>Enable DSIPHY1 lane 1.<br>1'b0: Disable<br>1'b1: Enable |
| 20 | RO | 0x0 | dsiphy1_l0_phyenable<br>Enable DSIPHY1 lane 0.<br>1'b0: Disable<br>1'b1: Enable |
| 19 | RO | 0x0 | dsiphy1_l3_txdatatransferenhs<br>High-speed data transfer enable for DSIPHY1 lane 3.<br>1'b0: Disable<br>1'b1: Enable |
| 18 | RO | 0x0 | dsiphy1_l2_txdatatransferenhs<br>High-speed data transfer enable for DSIPHY1 lane 2.<br>1'b0: Disable<br>1'b1: Enable |
| 17 | RO | 0x0 | dsiphy1_l1_txdatatransferenhs<br>High-speed data transfer enable for DSIPHY1 lane 1.<br>1'b0: Disable<br>1'b1: Enable |
| 16 | RO | 0x0 | dsiphy1_l0_txdatatransferenhs<br>High-speed data transfer enable for DSIPHY1 lane 0.<br>1'b0: Disable<br>1'b1: Enable |
| 15 | RO | 0x0 | dsiphy1_l3_txdatawidthhs<br>High-speed transmit data bus width select for DSIPHY1 lane 3.<br>1'b0: 8-bit<br>1'b1: 16-bit |
| 14 | RO | 0x0 | dsiphy1_l2_txdatawidthhs<br>High-speed transmit data bus width select for DSIPHY1 lane 2.<br>1'b0: 8-bit<br>1'b1: 16-bit |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RO | 0x0 | dsiphy1_l1_txdatawidthhs<br>High-speed transmit data bus width select for DSIPHY1 lane 1.<br>1'b0: 8-bit<br>1'b1: 16-bit |
| 12 | RO | 0x0 | dsiphy1_l0_txdatawidthhs<br>High-speed transmit data bus width select for DSIPHY1 lane 0.<br>1'b0: 8-bit<br>1'b1: 16-bit |
| 11 | RO | 0x0 | dsiphy0_l3_phyenable<br>Enable DSIPHY0 lane 3.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RO | 0x0 | dsiphy0_l2_phyenable<br>Enable DSIPHY0 lane 2.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RO | 0x0 | dsiphy0_l1_phyenable<br>Enable DSIPHY0 lane 1.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RO | 0x0 | dsiphy0_l0_phyenable<br>Enable DSIPHY0 lane 0.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RO | 0x0 | dsiphy0_l3_txdatatransferenhs<br>High-speed data transfer enable for DSIPHY0 lane 3.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RO | 0x0 | dsiphy0_l2_txdatatransferenhs<br>High-speed data transfer enable for DSIPHY0 lane 2.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RO | 0x0 | dsiphy0_l1_txdatatransferenhs<br>High-speed data transfer enable for DSIPHY0 lane 1.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RO | 0x0 | dsiphy0_l0_txdatatransferenhs<br>High-speed data transfer enable for DSIPHY0 lane 0.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RO | 0x0 | dsiphy0_l3_txdatawidthhs<br>High-speed transmit data bus width select for DSIPHY0 lane 3.<br>1'b0: 8-bit<br>1'b1: 16-bit |
| 2 | RO | 0x0 | dsiphy0_l2_txdatawidthhs<br>High-speed transmit data bus width select for DSIPHY0 lane 2.<br>1'b0: 8-bit<br>1'b1: 16-bit |
| 1 | RO | 0x0 | dsiphy0_l1_txdatawidthhs<br>High-speed transmit data bus width select for DSIPHY0 lane 1.<br>1'b0: 8-bit<br>1'b1: 16-bit |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RO | 0x0 | dsiphy0_l0_txdatawidthhs<br>High-speed transmit data bus width select for DSIPHY0 lane 0.<br>1'b0: 8-bit<br>1'b1: 16-bit |

## 6.14 VO0_GRF Register Description

### 6.14.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VO0_GRF_VO0_CON0 | 0x0000 | W | 0x000000E4 | Video output system control register 0 |
| VO0_GRF_VO0_CON1 | 0x0004 | W | 0x00000000 | Video output system control register 1 |
| VO0_GRF_VO0_CON2 | 0x0008 | W | 0x000000E4 | Video output system control register 2 |
| VO0_GRF_VO0_CON3 | 0x000C | W | 0x00000000 | Video output system control register 3 |
| VO0_GRF_VO0_CON4 | 0x0010 | W | 0x00000000 | Video output system control register 4 |
| VO0_GRF_VO0_CON5 | 0x0014 | W | 0x00000000 | Video output system control register 5 |
| VO0_GRF_VO0_CON6 | 0x0018 | W | 0x00000000 | Video output system control register 6 |
| VO0_GRF_VO0_STS0 | 0x0020 | W | 0x00000000 | Video output system status register 0 |
| VO0_GRF_VO0_STS1 | 0x0024 | W | 0x00000000 | Video output system status register 1 |
| VO0_GRF_VO0_STS2 | 0x0028 | W | 0x00000000 | Video output system status register 2 |
| VO0_GRF_VO0_STS3 | 0x002C | W | 0x00000000 | Video output system status register 3 |
| VO0_GRF_VO0_STS4 | 0x0030 | W | 0x00000000 | Video output system status register 4 |
| VO0_GRF_VO0_STS5 | 0x0034 | W | 0x00000000 | Video output system status register 5 |
| VO0_GRF_VO0_STS6 | 0x0038 | W | 0x00000000 | Video output system status register 6 |
| VO0_GRF_VO0_STS7 | 0x003C | W | 0x00000000 | Video output system status register 7 |
| VO0_GRF_MEM_CON0 | 0x0040 | W | 0x00001410 | Video output system memory interface control register 0 |
| VO0_GRF_MEM_CON1 | 0x0044 | W | 0x80101410 | Video output system memory interface control register 1 |
| VO0_GRF_MEM_CON2 | 0x0048 | W | 0x00000010 | Video output system memory interface control register 2 |
| VO0_GRF_MEM_CON3 | 0x004C | W | 0x00000011 | Video output system memory interface control register 3 |
| VO0_GRF_MEM_CON4 | 0x0050 | W | 0x00008010 | Video output system memory interface control register 4 |
| VO0_GRF_MEM_CON5 | 0x0054 | W | 0x00000000 | Video output system memory interface control register 5 |

Rockchip Confidential

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.14.2 Detail Registers Description

**VO0_GRF_VO0_CON0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | dp0_tca_disable<br>Disable DP0 input from the type-C assit block.<br>1'b0: Enable<br>1'b1: Disable |
| 11 | RW | 0x0 | dp0_sink_hpd_cfg<br>Software configuration for DP0 hot plug detect input |
| 10 | RW | 0x0 | dp0_sink_hpd_sel<br>Source selection for DP0 hot plug detect input.<br>1'b0: DP0 hot plug detect input controlled by hardware<br>1'b1: DP0 hot plug detect input controlled by software |
| 9 | RW | 0x0 | dp0_aux_din_sel<br>Polarity of DP0 aux data input.<br>1'b0: Normal<br>1'b1: Inverted |
| 8 | RW | 0x0 | dp0_aux_dout_sel<br>Polarity of DP0 aux data output.<br>1'b0: Normal<br>1'b1: Inverted |
| 7:6 | RW | 0x3 | dp0_lane3_sel<br>Data source selection for DPPHY0 lane 3.<br>2'h0: Select DP0 host lane 0 transmit parallel data output as DPPHY0 lane 3 data source<br>2'h1: Select DP0 host lane 1 transmit parallel data output as DPPHY0 lane 3 data source<br>2'h2: Select DP0 host lane 2 transmit parallel data output as DPPHY0 lane 3 data source<br>2'h3: Select DP0 host lane 3 transmit parallel data output as DPPHY0 lane 3 data source |
| 5:4 | RW | 0x2 | dp0_lane2_sel<br>Data source selection for DPPHY0 lane 2.<br>2'h0: Select DP0 host lane 0 transmit parallel data output as DPPHY0 lane 2 data source<br>2'h1: Select DP0 host lane 1 transmit parallel data output as DPPHY0 lane 2 data source<br>2'h2: Select DP0 host lane 2 transmit parallel data output as DPPHY0 lane 2 data source<br>2'h3: Select DP0 host lane 3 transmit parallel data output as DPPHY0 lane 2 data source |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:2 | RW | 0x1 | dp0_lane1_sel<br>Data source selection for DPPHY0 lane 1.<br>2'h0: Select DP0 host lane 0 transmit parallel data output as DPPHY0 lane 1 data source<br>2'h1: Select DP0 host lane 1 transmit parallel data output as DPPHY0 lane 1 data source<br>2'h2: Select DP0 host lane 2 transmit parallel data output as DPPHY0 lane 1 data source<br>2'h3: Select DP0 host lane 3 transmit parallel data output as DPPHY0 lane 1 data source |
| 1:0 | RW | 0x0 | dp0_lane0_sel<br>Data source selection for DPPHY0 lane 0.<br>2'h0: Select DP0 host lane 0 transmit parallel data output as DPPHY0 lane 0 data source<br>2'h1: Select DP0 host lane 1 transmit parallel data output as DPPHY0 lane 0 data source<br>2'h2: Select DP0 host lane 2 transmit parallel data output as DPPHY0 lane 0 data source<br>2'h3: Select DP0 host lane 3 transmit parallel data output as DPPHY0 lane 0 data source |

**VO0_GRF_VO0_CON1**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | dp0_lane3_phystatus_cfg<br>Software configuration for DPPHY0 lane 3 PHY status |
| 10 | RW | 0x0 | dp0_lane2_phystatus_cfg<br>Software configuration for DPPHY0 lane 2 PHY status |
| 9 | RW | 0x0 | dp0_lane1_phystatus_cfg<br>Software configuration for DPPHY0 lane 1 PHY status |
| 8 | RW | 0x0 | dp0_lane0_phystatus_cfg<br>Software configuration for DPPHY0 lane 0 PHY status |
| 7 | RW | 0x0 | dp0_lane3_phystatus_sel<br>DPPHY0 lane 3 PHY status selection.<br>1'b0: DPPHY0 lane 3 PHY status controlled by hardware<br>1'b1: DPPHY0 lane 3 PHY status controlled by software |
| 6 | RW | 0x0 | dp0_lane2_phystatus_sel<br>DPPHY0 lane 2 PHY status selection.<br>1'b0: DPPHY0 lane 2 PHY status controlled by hardware<br>1'b1: DPPHY0 lane 2 PHY status controlled by software |
| 5 | RW | 0x0 | dp0_lane1_phystatus_sel<br>DPPHY0 lane 1 PHY status selection.<br>1'b0: DPPHY0 lane 1 PHY status controlled by hardware<br>1'b1: DPPHY0 lane 1 PHY status controlled by software |
| 4 | RW | 0x0 | dp0_lane0_phystatus_sel<br>DPPHY0 lane 0 PHY status selection.<br>1'b0: DPPHY0 lane 0 PHY status controlled by hardware<br>1'b1: DPPHY0 lane 0 PHY status controlled by software |
| 3:0 | RO | 0x0 | reserved |

Rockchip Confidential

**VO0_GRF_VO0_CON2**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | dp1_tca_disable<br>Disable DP1 input from the type-C assit block.<br>1'b0: Enable<br>1'b1: Disable |
| 11 | RW | 0x0 | dp1_sink_hpd_cfg<br>Software configuration for DP0 hot plug detect input |
| 10 | RW | 0x0 | dp1_sink_hpd_sel<br>Source selection for DP0 hot plug detect input.<br>1'b0: DP0 hot plug detect input controlled by hardware<br>1'b1: DP0 hot plug detect input controlled by software |
| 9 | RW | 0x0 | dp1_aux_din_sel<br>Polarity of DP0 aux data input.<br>1'b0: Normal<br>1'b1: Inverted |
| 8 | RW | 0x0 | dp1_aux_dout_sel<br>Polarity of DP0 aux data output.<br>1'b0: Normal<br>1'b1: Inverted |
| 7:6 | RW | 0x3 | dp1_lane3_sel<br>Data source selection for DPPHY1 lane 3.<br>2'h0: Select DP0 host lane 0 transmit parallel data output as DPPHY1 lane 3 data source<br>2'h1: Select DP0 host lane 1 transmit parallel data output as DPPHY1 lane 3 data source<br>2'h2: Select DP0 host lane 2 transmit parallel data output as DPPHY1 lane 3 data source<br>2'h3: Select DP0 host lane 3 transmit parallel data output as DPPHY1 lane 3 data source |
| 5:4 | RW | 0x2 | dp1_lane2_sel<br>Data source selection for DPPHY1 lane 2.<br>2'h0: Select DP0 host lane 0 transmit parallel data output as DPPHY1 lane 2 data source<br>2'h1: Select DP0 host lane 1 transmit parallel data output as DPPHY1 lane 2 data source<br>2'h2: Select DP0 host lane 2 transmit parallel data output as DPPHY1 lane 2 data source<br>2'h3: Select DP0 host lane 3 transmit parallel data output as DPPHY1 lane 2 data source |
| 3:2 | RW | 0x1 | dp1_lane1_sel<br>Data source selection for DPPHY1 lane 1.<br>2'h0: Select DP0 host lane 0 transmit parallel data output as DPPHY1 lane 1 data source<br>2'h1: Select DP0 host lane 1 transmit parallel data output as DPPHY1 lane 1 data source<br>2'h2: Select DP0 host lane 2 transmit parallel data output as DPPHY1 lane 1 data source<br>2'h3: Select DP0 host lane 3 transmit parallel data output as DPPHY1 lane 1 data source |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1:0 | RW | 0x0 | dp1_lane0_sel<br>Data source selection for DPPHY1 lane 0.<br>2'h0: Select DP0 host lane 0 transmit parallel data output as DPPHY1 lane 0 data source<br>2'h1: Select DP0 host lane 1 transmit parallel data output as DPPHY1 lane 0 data source<br>2'h2: Select DP0 host lane 2 transmit parallel data output as DPPHY1 lane 0 data source<br>2'h3: Select DP0 host lane 3 transmit parallel data output as DPPHY1 lane 0 data source |

**VO0_GRF_VO0_CON3**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | dp1_lane3_phystatus_cfg<br>Software configuration for DPPHY1 lane 3 PHY status |
| 10 | RW | 0x0 | dp1_lane2_phystatus_cfg<br>Software configuration for DPPHY1 lane 2 PHY status |
| 9 | RW | 0x0 | dp1_lane1_phystatus_cfg<br>Software configuration for DPPHY1 lane 1 PHY status |
| 8 | RW | 0x0 | dp1_lane0_phystatus_cfg<br>Software configuration for DPPHY1 lane 0 PHY status |
| 7 | RW | 0x0 | dp1_lane3_phystatus_sel<br>DPPHY1 lane 3 PHY status selection.<br>1'b0: DPPHY1 lane 3 PHY status controlled by hardware<br>1'b1: DPPHY1 lane 3 PHY status controlled by software |
| 6 | RW | 0x0 | dp1_lane2_phystatus_sel<br>DPPHY1 lane 2 PHY status selection.<br>1'b0: DPPHY1 lane 2 PHY status controlled by hardware<br>1'b1: DPPHY1 lane 2 PHY status controlled by software |
| 5 | RW | 0x0 | dp1_lane1_phystatus_sel<br>DPPHY1 lane 1 PHY status selection.<br>1'b0: DPPHY1 lane 1 PHY status controlled by hardware<br>1'b1: DPPHY1 lane 1 PHY status controlled by software |
| 4 | RW | 0x0 | dp1_lane0_phystatus_sel<br>DPPHY1 lane 0 PHY status selection.<br>1'b0: DPPHY1 lane 0 PHY status controlled by hardware<br>1'b1: DPPHY1 lane 0 PHY status controlled by software |
| 3:0 | RO | 0x0 | reserved |

**VO0_GRF_VO0_CON4**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | hdcp0_clk_gating_en<br>Enable auto clock gating for HDCP0 memory.<br>1'b0: Disable<br>1'b1: Enable |
| 7:4 | RW | 0x0 | hdcp0_global_gpio_in<br>HDCP0 global GPIO input |
| 3 | RW | 0x0 | hdcp0_aes1_debug_trigger<br>HDCP0 DP AES port 1 debug trigger configuration. When asserted, the hdcp_aes1_debug_data is captured internally by HDCP0. |
| 2 | RW | 0x0 | hdcp0_aes0_debug_trigger<br>HDCP0 DP AES port 0 debug trigger configuration. When asserted, the hdcp_aes0_debug_data is captured internally by HDCP0. |
| 1 | RW | 0x0 | trng0_ctrl_reseed<br>Enable TRNG0 reseed operation.<br>1'b0: Disable<br>1'b1: Enable<br>When it is asserted, the TRNG0 responds by stopping any reseed operation that is currently underway and initiating a new reseed operation. |
| 0 | RW | 0x0 | trng0_ctrl_zeroize<br>Enable TRNG0 zeroize operation.<br>1'b0: Disable<br>1'b1: Enable |

**VO0_GRF_VO0_CON5**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | hdcp0_aes0_debug_data<br>HDCP0 DP AES port 0 debug data configuration |

**VO0_GRF_VO0_CON6**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | hdcp0_aes1_debug_data<br>HDCP0 DP AES port 1 debug data configuration |

**VO0_GRF_VO0_STS0**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27:24 | RO | 0x0 | dp1_p0_gpio_out<br>DP1 port 0 GPIO output |
| 23:20 | RO | 0x0 | dp1_global_gpio_out<br>DP1 global GPIO output |
| 19 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 18 | RO | 0x0 | dp1_tca_disable_ack<br>Acknowledge from DP1 to the Type-C assit block.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 17 | RO | 0x0 | reserved |
| 16 | RO | 0x0 | dp1_aux_timeout<br>DP1 aux transfer timeout indication.<br>1'b0: Inactive<br>1'b1: Active |
| 15:12 | RO | 0x0 | reserved |
| 11:8 | RO | 0x0 | dp0_p0_gpio_out<br>DP0 port0 GPIO output |
| 7:4 | RO | 0x0 | dp0_global_gpio_out<br>DP0 global GPIO output |
| 3 | RO | 0x0 | reserved |
| 2 | RO | 0x0 | dp0_tca_disable_ack<br>Acknowledge from DP0 to the Type-C assit block.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 1 | RO | 0x0 | reserved |
| 0 | RO | 0x0 | dp0_aux_timeout<br>DP0 aux transfer timeout indication.<br>1'b0: Inactive<br>1'b1: Active |

**VO0_GRF_VO0_STS1**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | dp0_debug_l32<br>DP0 debug output lower 32 bits |

**VO0_GRF_VO0_STS2**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | dp0_debug_h32<br>DP0 debug output higher 32 bits |

**VO0_GRF_VO0_STS3**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:8 | RO | 0x0 | hdcp0_global_gpio_out<br>HDCP0 global GPIO output |
| 7:6 | RO | 0x0 | reserved |
| 5 | RO | 0x0 | trng0_ctrl_rand_vld<br>TRNG0 serial random bit valid output.<br>1'b0: Inactive<br>1'b1: Active |
| 4 | RO | 0x0 | trng0_ctrl_rand_bit<br>TRNG0 serial random bit output<br>1'b0: Inactive<br>1'b1: Active |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RO | 0x0 | trng0_ctrl_seeded<br>TRNG0 reseeding/seeding completion output.<br>1'b0: Inactive<br>1'b1: Active |
| 2 | RO | 0x0 | trng0_ctrl_reseeding<br>TRNG0 reseeding activity output.<br>1'b0: Inactive<br>1'b1: Active |
| 1 | RO | 0x0 | trng0_ctrl_reminder<br>TRNG0 reseed reminder output.<br>1'b0: Inactive<br>1'b1: Active |
| 0 | RO | 0x0 | trng0_ctrl_secure<br>TRNG0 secure mode output.<br>1'b0: Inactive<br>1'b1: Active |

**VO0_GRF_VO0_STS4**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | dp1_debug_l32<br>DP1 debug output lower 32 bits |

**VO0_GRF_VO0_STS5**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | dp1_debug_h32<br>DP1 debug output higher 32 bits |

**VO0_GRF_VO0_STS6**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | hdcp0_diag_out<br>HDCP0 diagnostic output |

**VO0_GRF_VO0_STS7**

Address: Operational Base + offset (0x003C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | hdcp0_p1_gpio_out<br>HDCP0 port 1 GPIO output |
| 15:0 | RO | 0x0000 | hdcp0_p0_gpio_out<br>HDCP0 port 0 GPIO output |

**VO0_GRF_MEM_CON0**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x1410 | mem_cfg_hdspra<br>Interface configuration for HDSPRA type memory in PD_VO0. |

**VO0_GRF_MEM_CON1**

Rockchip Confidencial

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x8010 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x1410 | mem_cfg_hdsprf<br>Interface configuration for HDSPRF type memory in PD_VO0. |

**VO0_GRF_MEM_CON2**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x010 | mem_cfg_hsdprf_l16<br>Interface configuration for HSDPRF type memory in PD_VO0, lower 16 bits. |

**VO0_GRF_MEM_CON3**

Address: Operational Base + offset (0x004C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7:0 | RW | 0x11 | mem_cfg_hsdprf_h8<br>Interface configuration for HSDPRF type memory in PD_VO0, higher 16 bits. |

**VO0_GRF_MEM_CON4**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x8010 | mem_cfg_uhdpdprf_l16<br>Interface configuration for UHDPDPRF type memory in PD_VO0, lower 16 bits. |

**VO0_GRF_MEM_CON5**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:3 | RO | 0x0000 | reserved |
| 2:0 | RW | 0x0 | mem_cfg_uhdpdprf_h3<br>Interface configuration for UHDPDPRF type memory in PD_VO0, higher 3 bits. |

Rockchip Confidencial

# 6.15 VO1_GRF Register Description

## 6.15.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VO1_GRF_VO1_CON0 | 0x0000 | W | 0x00000000 | Video output system control register 0 |
| VO1_GRF_VO1_CON1 | 0x0004 | W | 0x00000000 | Video output system control register 1 |
| VO1_GRF_VO1_CON2 | 0x0008 | W | 0x00000000 | Video output system control register 2 |
| VO1_GRF_VO1_CON3 | 0x000C | W | 0x00000000 | Video output system control register 3 |
| VO1_GRF_VO1_CON4 | 0x0010 | W | 0x00000000 | Video output system control register 4 |
| VO1_GRF_VO1_CON6 | 0x0018 | W | 0x00000000 | Video output system control register 6 |
| VO1_GRF_VO1_CON7 | 0x001C | W | 0x00000000 | Video output system control register 7 |
| VO1_GRF_VO1_CON9 | 0x0024 | W | 0x00000000 | Video output system control register 9 |
| VO1_GRF_VO1_STS0 | 0x0030 | W | 0x00000000 | Video output system status register 0 |
| VO1_GRF_VO1_STS1 | 0x0034 | W | 0x00000000 | Video output system status register 1 |
| VO1_GRF_VO1_STS2 | 0x0038 | W | 0x00000000 | Video output system status register 2 |
| VO1_GRF_VO1_STS3 | 0x003C | W | 0x00000000 | Video output system status register 3 |
| VO1_GRF_VO1_STS4 | 0x0040 | W | 0x00000000 | Video output system status register 4 |
| VO1_GRF_VO1_STS5 | 0x0044 | W | 0x00000000 | Video output system status register 5 |
| VO1_GRF_VO1_STS6 | 0x0048 | W | 0x00000000 | Video output system status register 6 |
| VO1_GRF_MEM_CON0 | 0x0050 | W | 0x00001410 | Video output system memory interface control register 0 |
| VO1_GRF_MEM_CON1 | 0x0054 | W | 0x80100010 | Video output system memory interface control register 1 |
| VO1_GRF_MEM_CON2 | 0x0058 | W | 0x00000011 | Video output system memory interface control register 2 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.15.2 Detail Registers Description

**VO1_GRF_VO1_CON0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | hdmitx1_hsync_pol<br>Polarity selection for hdmitx1_hsync.<br>1'b0: Normal<br>1'b1: Inverted |
| 7 | RW | 0x0 | hdmitx1_vsync_pol<br>Polarity selection for hdmitx1_vsync.<br>1'b0: Normal<br>1'b1: Inverted |
| 6 | RW | 0x0 | hdmitx0_hsync_pol<br>Polarity selection for hdmitx0_hsync.<br>1'b0: Normal<br>1'b1: Inverted |
| 5 | RW | 0x0 | hdmitx0_vsync_pol<br>Polarity selection for hdmitx0_vsync.<br>1'b0: Normal<br>1'b1: Inverted |
| 4 | RW | 0x0 | edp0_spdif_sel<br>Enable connect SPDIF3 interface to EDP0 SPDIF port.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | edp0_i2s_sel<br>Enable connect I2S5_8CH interface to EDP0 I2S port.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | edp0_video_bist_en<br>Enable EDP0 video bist function.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x1 | edp0_hdcp_protect<br>Enable EDP0 hdcp protect function.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | edp0_mode<br>Enable EDP0 interface.<br>1'b0: Disable<br>1'b1: Enable |

**VO1_GRF_VO1_CON1**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | hdcp1_p2_gpio_in_sel<br>Source selection for HDCP1 port 2 GPIO input.<br>1'b0: Select {2'h0,hdmitx1_hdcp_i2c_grant,1'b1} as HDCP1 port 2 GPIO input<br>1'b1: Select hdmitx1_hdcp_p0_gpio_in as HDCP1 port 2 GPIO input |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RW | 0x0 | hdcp1_p1_gpio_in_sel<br>Source selection for HDCP1 port 1 GPIO input.<br>1'b0: Select {2'h0,hdmitx0_hdcp_i2c_grant,1'b1} as HDCP1 port 1 GPIO input<br>1'b1: Select hdmitx0_hdcp_p0_gpio_in as HDCP1 port 1 GPIO input |
| 8 | RW | 0x0 | hdcp1_p0_gpio_in_sel<br>Source selection for HDCP1 port 0 GPIO input.<br>1'b0: Select {3'h0,hdmirx_connect} as HDCP1 port 0 GPIO input<br>1'b1: Select {1'b0,hdmirx_hdcp_p0_gpio_in} as HDCP1 port 0 GPIO input |
| 7:5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | edp1_spdif_sel<br>Enable connect SPDIF4 interface to EDP1 SPDIF port.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | edp1_i2s_sel<br>Enable connect I2S6_8CH interface to EDP1 I2S port.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | edp1_video_bist_en<br>Enable EDP1 video bist function.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x1 | edp1_hdcp_protect<br>Enable EDP1 hdcp protect function.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | edp1_mode<br>Enable EDP1 interface.<br>1'b0: Disable<br>1'b1: Enable |

**VO1_GRF_VO1_CON2**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | hdmirx_global_gpio_out_sel<br>Selection for hdmirx_global_gpio_out.<br>1'b0: Select hdcp1_global_gpio_out as hdmirx_global_gpio_out<br>1'b1: Select hdmirx_global_gpio_out_sw as hdmirx_global_gpio_out |
| 14:11 | RW | 0x0 | hdcp1_global_gpio_in<br>HDCP1 global GPIO input by software |
| 10 | RW | 0x0 | hdcp1_gating_en<br>Enable HDCP1 memory auto clock gating.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RW | 0x0 | trng1_ctrl_reseed<br>Enable TRNG1 reseed operation.<br>1'b0: Disable<br>1'b1: Enable<br>When it is asserted, the TRNG1 responds by stopping any reseed operation that is currently underway and initiating a new reseed operation. |
| 8 | RW | 0x0 | trng1_ctrl_zeroize<br>Enable TRNG1 zeroize operation.<br>1'b0: Disable<br>1'b1: Enable |
| 7:4 | RW | 0x0 | hdmirx_global_gpio_out_sw<br>HDMIRX global GPIO output by software |
| 3 | RW | 0x0 | hdcp_hdmirx_stall<br>HDCP0 HDMI TMDS port 0 input internal test signal. This signal is for internal use only and must be tied off to 1'b0.<br>1'b0: Inactive<br>1'b1: Active |
| 2 | RW | 0x0 | hdmirx_sdain_msk<br>Mask for HDMIRX DDC SDA data input.<br>1'b0: Masked, HDMIRX DDC SDA data input is tied to 1<br>1'b1: Not masked, HDMIRX DDC SDA data input is from IO |
| 1 | RW | 0x0 | hdmirx_sclin_msk<br>Mask for HDMIRX DDC SCL data input.<br>1'b0: Masked, HDMIRX DDC SCL data input is tied to 1<br>1'b1: Not masked, HDMIRX DDC SCL data input is from IO |
| 0 | RW | 0x0 | hdmirx_cecin_msk<br>Mask for HDMIRX CEC data input.<br>1'b0: Not masked, HDMIRX CEC data input is from IO<br>1'b1: Masked, HDMIRX CEC data input is tied to 1 |

**VO1_GRF_VO1_CON3**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | hdmitx0_global_gpio_out_sel<br>Selection for hdmitx0_global_gpio_out.<br>1'b0: Select hdcp1_global_gpio_out as hdmitx0_global_gpio_out<br>1'b1: Select hdmitx0_hdcp_global_gpio_out_sw as hdmitx0_global_gpio_out |
| 14 | RW | 0x0 | hdmitx0_spdif_sel<br>Enable connect SPDIF3 interface to HDMITX0 SPDIF port.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | hdmitx0_i2s_sel<br>Enable connect I2S5_8CH interface to HDMITX0 I2S port.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | hdmitx0_compress_mode<br>Enable data compress for HDMITX0 interface .<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11 | RW | 0x0 | hdmitx0_mode<br>Enable HDMITX0 interface.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | hdmitx0_sdain_msk<br>Mask for HDMITX0 DDC SDA data input.<br>1'b0: Masked, HDMITX0 DDC SDA data input is tied to 1<br>1'b1: Not masked, HDMITX0 DDC SDA data input is from IO |
| 9 | RW | 0x0 | hdmitx0_sclin_msk<br>Mask for HDMITX0 DDC SCL data input.<br>1'b0: Masked, HDMITX0 DDC SCL data input is tied to 1<br>1'b1: Not masked, HDMITX0 DDC SCL data input is from IO |
| 8 | RW | 0x0 | hdmitx0_cecin_msk<br>Mask for HDMITX0 CEC data input.<br>1'b0: Not masked, HDMITX0 CEC data input is from IO<br>1'b1: Masked, HDMITX0 CEC data input is tied to 1 |
| 7:4 | RW | 0x0 | hdmitx0_color_depth<br>HDMITX0 image pixel interace video color depth.<br>4'h5: 8 bits per component<br>4'h6: 10 bits per component<br>Others: Reserved |
| 3:0 | RW | 0x0 | hdmitx0_ipi_format<br>HDMITX0 image pixel interace video format.<br>4'h0: RGB<br>4'h2: YCbCr 4:4:4<br>4'h3: YCbCr 4:2:0<br>4'hb: Compressed Data<br>Others: Reserved |

**VO1_GRF_VO1_CON4**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | hdmitx0_grf_revapb_sel<br>Control for HDMITX0 REVOC FIFO memory.<br>1'b0: Select HDMITX0 to control the REVOC FIFO memory<br>1'b1: Select CPU to control the REVOC FIFO memory |
| 14 | RW | 0x0 | hdmitx0_iearcbpclk_valid<br>HDMITX0 IEARC_BPCLK enable by softwar<br>1'b0: Enable IEARC_BPCLK<br>1'b1: Disable IEARC_BPCLK |
| 13 | RW | 0x0 | hdmitx0_dbgcmdc_rcven<br>HDMITX0 phyi_earc_dmac_en configuration by software.<br>1'b0: Set phyi_earc_dmac_en as 1'b0<br>1'b1: Set phyi_earc_dmac_en as 1'b1<br>Active when hdmitx0_dbgearc_mod is 1. |
| 12 | RW | 0x0 | hdmitx0_dbgcmdc_rxen<br>HDMITX0 phyi_earc_rx_mode configuration by software.<br>1'b0: Set phyi_earc_rx_mode as 1'b0<br>1'b1: Set phyi_earc_rx_mode as 1'b1<br>Active when hdmitx0_dbgearc_mod is 1. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11 | RW | 0x0 | hdmitx0_dbgcmdc_drv<br>HDMITX0 phyi_earc_tx_mode configuration by software.<br>1'b0: Set phyi_earc_tx_mode as 1'b0<br>1'b1: Set phyi_earc_tx_mode as 1'b1<br>Active when hdmitx0_dbgearc_mod is 1. |
| 10 | RW | 0x0 | hdmitx0_dbgcmdc_ack<br>HDMITX0 iearcrx_cmdc_dataout_drv_en_ack configuration by software.<br>1'b0: Set iearcrx_cmdc_dataout_drv_en_ack as 1'b0<br>1'b1: Set iearcrx_cmdc_dataout_drv_en_ack as 1'b1<br>Active when hdmitx0_dbgearc_mod is 1 |
| 9 | RW | 0x0 | hdmitx0_dbgearc_mod<br>Enable HDMITX0 eARC debug mode.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | hdmitx0_earc_selcru<br>Clock selection for HDMITX0 iearc_bpclk.<br>1'b0: Select the phyo_earc_dmac_rxclk generated HDMITXPHY0 as the HDMITX0 iearc_bpclk<br>1'b1: Select the cruo_earc_dmac_rxclk generated by CRU as the HDMITX0 iearc_bpclk |
| 7:6 | RW | 0x0 | hdmitx0_select_sao_spdifrx<br>Select data for HDMITX0 ARC serial audio output to SPDIF.<br>2'b01: Select phyo_aux_arc_rxdata from HDMITXPHY0<br>2'b10: Select phyo_earc_or_arc_dmac_rxdata from HDMITXPHY0<br>Others: Select oearcrx_dmac_sao_spdif from HDMITX0 |
| 5 | RW | 0x0 | hdmitx0_frlchar_mem_gating<br>Enable clock gating for HDMITX0 FRLCHAR memory.<br>1'b0: Enable clock gating<br>1'b1: Disable clock gating |
| 4 | RW | 0x0 | hdmitx0_set_phyclk_phase<br>Select HDMITXPHY0 clock phase.<br>1'b0: 0 degree<br>1'b1: 180 degree |
| 3 | RW | 0x0 | hdmitx0_set_clr<br>HDMITX0 54-bit data bus clear.<br>1'b0: Release the 54-bit data bus to normal work<br>1'b1: Reset the 54-bit data bus to 0 |
| 2 | RW | 0x0 | hdmitx0_sample_value<br>Enable sample shift data for HDMITX0.<br>1'b0: Enable sample shift data when cnt value=0<br>1'b1: Enable sample shift data when cnt value=1 |
| 1 | RW | 0x0 | hdmitx0_to_b18_en<br>HDMITX0 interface convertion.<br>1'b0: Convert 54-bit bus to 36-bit bus interface<br>1'b1: Convert 54-bit bus to 18-bit bus interface |
| 0 | RW | 0x0 | hdmitx0_frl_mode<br>HDMITX0 mode selection.<br>1'b0: TMDS mode<br>1'b1: FRL mode |

**VO1_GRF_VO1_CON6**

Address: Operational Base + offset (0x0018)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | hdmitx1_global_gpio_out_sel<br>Selection for hdmitx1_global_gpio_out.<br>1'b0: Select hdcp1_global_gpio_out as hdmitx1_global_gpio_out<br>1'b1: Select hdmitx1_hdcp_global_gpio_out_sw as hdmitx1_global_gpio_out |
| 14 | RW | 0x0 | hdmitx1_spdif_sel<br>Enable connect SPDIF4 interface to HDMITX1 SPDIF port.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | hdmitx1_i2s_sel<br>Enable connect I2S6_8CH interface to HDMITX1 I2S port.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | hdmitx1_compress_mode<br>Enable data compress for HDMITX1 interface.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | hdmitx1_mode<br>Enable HDMITX1 interface.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | hdmitx1_sdain_msk<br>Mask for HDMITX1 DDC SDA data input.<br>1'b0: Masked, HDMITX1 DDC SDA data input is tied to 1<br>1'b1: Not masked, HDMITX1 DDC SDA data input is from IO |
| 9 | RW | 0x0 | hdmitx1_sclin_msk<br>Mask for HDMITX1 DDC SCL data input.<br>1'b0: Masked, HDMITX1 DDC SCL data input is tied to 1<br>1'b1: Not masked, HDMITX1 DDC SCL data input is from IO |
| 8 | RW | 0x0 | hdmitx1_cecin_msk<br>Mask for HDMITX1 CEC data input.<br>1'b0: Not masked, HDMITX1 CEC data input is from IO<br>1'b1: Masked, HDMITX1 CEC data input is tied to 1 |
| 7:4 | RW | 0x0 | hdmitx1_color_depth<br>HDMITX1 image pixel interace video color depth.<br>4'h5: 8 bits per component<br>4'h6: 10 bits per component<br>Others: Reserved |
| 3:0 | RW | 0x0 | hdmitx1_ipi_format<br>HDMITX1 image pixel interace video format.<br>4'h0: RGB<br>4'h2: YCbCr 4:4:4<br>4'h3: YCbCr 4:2:0<br>4'hb: Compressed Data<br>Others: Reserved |

**VO1_GRF_VO1_CON7**

Address: Operational Base + offset (0x001C)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | hdmitx1_grf_revapb_sel<br>Control for HDMITX1 REVOC FIFO memory.<br>1'b0: Select HDMITX1 to control the REVOC FIFO memory<br>1'b1: Select CPU to control the REVOC FIFO memory |
| 14 | RW | 0x0 | hdmitx1_iearcbpclk_valid<br>HDMITX1 IEARC_BPCLK enable by software.<br>1'b0: Enable IEARC_BPCLK<br>1'b1: Disable IEARC_BPCLK |
| 13 | RW | 0x0 | hdmitx1_dbgcmdc_rcven<br>HDMITX1 phyi_earc_dmac_en configuration by software.<br>1'b0: Set phyi_earc_dmac_en as 1'b0<br>1'b1: Set phyi_earc_dmac_en as 1'b1<br>Active when hdmitx1_dbgearc_mod is 1. |
| 12 | RW | 0x0 | hdmitx1_dbgcmdc_rxen<br>HDMITX1 phyi_earc_rx_mode configuration by software.<br>1'b0: Set phyi_earc_rx_mode as 1'b0<br>1'b1: Set phyi_earc_rx_mode as 1'b1<br>Active when hdmitx1_dbgearc_mod is 1. |
| 11 | RW | 0x0 | hdmitx1_dbgcmdc_drv<br>HDMITX1 phyi_earc_tx_mode configuration by software.<br>1'b0: Set phyi_earc_tx_mode as 1'b0<br>1'b1: Set phyi_earc_tx_mode as 1'b1<br>Active when hdmitx1_dbgearc_mod is 1. |
| 10 | RW | 0x0 | hdmitx1_dbgcmdc_ack<br>HDMITX1 iearcrx_cmdc_dataout_drv_en_ack configuration by software.<br>1'b0: Set iearcrx_cmdc_dataout_drv_en_ack as 1'b0<br>1'b1: Set iearcrx_cmdc_dataout_drv_en_ack as 1'b1<br>Active when hdmitx1_dbgearc_mod is 1 |
| 9 | RW | 0x0 | hdmitx1_dbgearc_mod<br>Enable HDMITX1 eARC debug mode.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | hdmitx1_earc_selcru<br>Clock selection for HDMITX1 iearc_bpclk.<br>1'b0: Select the phyo_earc_dmac_rxclk generated HDMITXPHY1 as the HDMITX1 iearc_bpclk<br>1'b1: Select the cruo_earc_dmac_rxclk generated by CRU as the HDMITX1 iearc_bpclk |
| 7:6 | RW | 0x0 | hdmitx1_select_sao_spdifrx<br>Select data for HDMITX1 ARC serial audio output to SPDIF.<br>2'b01: Select phyo_aux_arc_rxdata from HDMITXPHY1<br>2'b10: Select phyo_earc_or_arc_dmac_rxdata from HDMITXPHY1<br>Others: Select oearcrx_dmac_sao_spdif from HDMITX1 |
| 5 | RW | 0x0 | hdmitx1_frlchar_mem_gating<br>Enable clock gating for HDMITX1 FRLCHAR memory.<br>1'b0: Enable clock gating<br>1'b1: Disable clock gating |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | hdmitx1_set_phyclk_phase<br>Select HDMITXPHY1 clock phase.<br>1'b0: 0 degree<br>1'b1: 180 degree |
| 3 | RW | 0x0 | hdmitx1_set_clr<br>HDMITX1 54-bit data bus clear.<br>1'b0: Release the 54-bit data bus to normal work<br>1'b1: Reset the 54-bit data bus to 0 |
| 2 | RW | 0x0 | hdmitx1_sample_value<br>Enable sample shift data for HDMITX1.<br>1'b0: Enable sample shift data when cnt value=0<br>1'b1: Enable sample shift data when cnt value=1 |
| 1 | RW | 0x0 | hdmitx1_to_b18_en<br>HDMITX1 interface convertion.<br>1'b0: Convert 54-bit bus to 36-bit bus interface<br>1'b1: Convert 54-bit bus to 18-bit bus interface |
| 0 | RW | 0x0 | hdmitx1_frl_mode<br>HDMITX1 mode selection.<br>1'b0: TMDS mode<br>1'b1: FRL mode |

**VO1_GRF_VO1_CON9**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | hdmirx_hdcp_i2c_grant_sw<br>Generate HDMIRX external I2C master interface access granted indication by software.<br>1'b0: Inactive<br>1'b1: Active |
| 13 | RW | 0x0 | hdmitx1_hdcp_i2c_grant_sw<br>Generate HDMITX1 external I2C master interface access granted indication by software.<br>1'b0: Inactive<br>1'b1: Active |
| 12 | RW | 0x0 | hdmitx1_hdcp_i2c_grant_sel<br>Source selection for HDMITX1 external I2C master interface access granted indication.<br>1'b0: Select from HDMITX1 output<br>1'b1: Select from hdmitx1_hdcp_i2c_grant_sw |
| 11 | RW | 0x0 | hdmitx0_hdcp_i2c_grant_sw<br>Generate HDMITX0 external I2C master interface access granted indication by software.<br>1'b0: Inactive<br>1'b1: Active |
| 10 | RW | 0x0 | hdmitx0_hdcp_i2c_grant_sel<br>Source selection for HDMITX0 external I2C master interface access granted indication.<br>1'b0: Select from HDMITX0 output<br>1'b1: Select from hdmitx0_hdcp_i2c_grant_sw |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9:8 | RW | 0x0 | hdmirx_debug_io_mode<br>HDMIRX debug output information selection.<br>2'b00: Select HDMIRX phy signal as debug output<br>2'b01: Select HDMIRX video output signal as debug output<br>2'b10: Select HDMIRX audio output signal as debug output<br>2'b11: Select HDMIRX ddc signal as debug output |
| 7:4 | RW | 0x0 | hdmitx1_hdcp_global_gpio_out_sw<br>Sofwrare configuration for HDMITX1 global GPIO output to HDCP. |
| 3:0 | RW | 0x0 | hdmitx0_hdcp_global_gpio_out_sw<br>Sofwrare configuration for HDMITX0 global GPIO output to HDCP. |

**VO1_GRF_VO1_STS0**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | hdcp1_diag_out<br>HDCP1 HPI diagnosis output |

**VO1_GRF_VO1_STS1**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:27 | RO | 0x00 | reserved |
| 26 | RO | 0x0 | hdmirx_oavmute<br>HDMIRX avmute indication.<br>1'b0: Inactive<br>1'b1: Active |
| 25 | RO | 0x0 | trng1_ctrl_rand_vld<br>TRNG1 serial random bit valid output.<br>1'b0: Inactive<br>1'b1: Active |
| 24 | RO | 0x0 | trng1_ctrl_rand_bit<br>TRNG1 serial random bit output<br>1'b0: Inactive<br>1'b1: Active |
| 23 | RO | 0x0 | trng1_ctrl_seeded<br>TRNG1 reseeding/seeding completion output.<br>1'b0: Inactive<br>1'b1: Active |
| 22 | RO | 0x0 | trng1_ctrl_reseeding<br>TRNG1 reseeding activity output.<br>1'b0: Inactive<br>1'b1: Active |
| 21 | RO | 0x0 | trng1_ctrl_reminder<br>TRNG1 reseed reminder output.<br>1'b0: Inactive<br>1'b1: Active |
| 20 | RO | 0x0 | trng1_ctrl_secure<br>TRNG1 secure mode output.<br>1'b0: Inactive<br>1'b1: Active |
| 19 | RO | 0x0 | hdmirx_hdcp_encryption_state<br>HDMIRX HDCP video field encryption state.<br>1'b0: Inactive<br>1'b1: Active |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 18 | RO | 0x0 | hdmirx_hdcp_authentication_start<br>HDMIRX HDCP authentication state.<br>1'b0: Inactive<br>1'b1: Active |
| 17:14 | RO | 0x0 | hdmirx_aud_sample_flat<br>HDMIRX audio sample flat or invalid from audio packet |
| 13 | RO | 0x0 | hdmirx_aud_external_mute<br>HDMIRX external mute status.<br>1'b0: Inactive<br>1'b1: Active |
| 12 | RO | 0x0 | hdmirx_aud_fifo_mute_low_sts<br>HDMIRX audio FIFO mute low status.<br>1'b0: Inactive<br>1'b1: Active |
| 11 | RO | 0x0 | hdmirx_aud_fifo_mute_high_sts<br>HDMIRX audio FIFO mute high status.<br>1'b0: Inactive<br>1'b1: Active |
| 10 | RO | 0x0 | hdmirx_aud_fifo_thr_low_sts<br>HDMIRX audio FIFO threshold low status.<br>1'b0: Inactive<br>1'b1: Active |
| 9 | RO | 0x0 | hdmirx_aud_fifo_thr_high_sts<br>HDMIRX audio FIFO threshold high status.<br>1'b0: Inactive<br>1'b1: Active |
| 8 | RO | 0x0 | hdmirx_pkt_rcv<br>HDMIRX packet received marker.<br>1'b0: Inactive<br>1'b1: Active |
| 7 | RO | 0x0 | hdmirx_pkt_err<br>HDMIRX packet error status.<br>1'b0: Inactive<br>1'b1: Active |
| 6 | RO | 0x0 | hdmirx_connect<br>HDMIRX connection to external HDCP status.<br>1'b0: Inactive<br>1'b1: Active |
| 5 | RO | 0x0 | hdmirx_avmute_sts<br>HDMIRX GCP avmute status.<br>1'b0: Inactive<br>1'b1: Active |
| 4 | RO | 0x0 | hdmirx_hpd<br>Hot plug detect output for HDMI source input.<br>1'b0: Inactive<br>1'b1: Active |
| 3 | RO | 0x0 | hdcp1_tmds2_secure<br>HDCP1 TMDS port 2 secure signal. When asserted this signal indicates the video and data islands for the frame are encrypted on the link.<br>1'b0: Inactive<br>1'b1: Active |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RO | 0x0 | hdcp1_tmds1_secure<br>HDCP1 TMDS port 1 secure signal. When asserted this signal indicates the video and data islands for the frame are encrypted on the link.<br>1'b0: Inactive<br>1'b1: Active |
| 1 | RO | 0x0 | hdcp1_tmds0_secure<br>HDCP1 TMDS port 0 secure signal. When asserted this signal indicates the video and data islands for the frame are encrypted on the link.<br>1'b0: Inactive<br>1'b1: Active |
| 0 | RO | 0x0 | reserved |

**VO1_GRF_VO1_STS2**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | hdcp1_p1_gpio_out<br>HDCP1 port 1 GPIO output |
| 15:0 | RO | 0x0000 | hdcp1_p0_gpio_out<br>HDCP1 port 0 GPIO output |

**VO1_GRF_VO1_STS3**

Address: Operational Base + offset (0x003C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27:24 | RO | 0x0 | hdmitx0_hdcp_global_gpio_in<br>HDMITX0 global GPIO input |
| 23:20 | RO | 0x0 | hdmitx0_hdcp_p0_gpio_in<br>HDMITX0 port 0 GPIO input |
| 19:16 | RO | 0x0 | hdcp1_global_gpio_out<br>HDCP1 global GPIO output |
| 15:0 | RO | 0x0000 | hdcp1_p2_gpio_out<br>HDCP1 port 2 GPIO output |

**VO1_GRF_VO1_STS4**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x000 | reserved |
| 22:16 | RO | 0x00 | hdmirx_debug_io<br>HDMIRX debug output. |
| 15:12 | RO | 0x0 | hdmirx_hdcp_global_gpio_in<br>HDMIRX global GPIO input |
| 11 | RO | 0x0 | reserved |
| 10:8 | RO | 0x0 | hdmirx_hdcp_p0_gpio_in<br>HDMIRX port 0 GPIO input |
| 7:4 | RO | 0x0 | hdmitx1_hdcp_global_gpio_in<br>HDMITX1 global GPIO input |
| 3:0 | RO | 0x0 | hdmitx1_hdcp_p0_gpio_in<br>HDMITX1 port 0 GPIO input |

**VO1_GRF_VO1_STS5**

Address: Operational Base + offset (0x0044)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28 | RO | 0x0 | hdmitx0_oearctx_h14arc_sel<br>HDMITX0 eARC RX PHY HDMI14b ARC mode selection.<br>1'b0: Inactive<br>1'b1: Active |
| 27 | RO | 0x0 | hdmitx0_oearcrx_dmac_phy_rcv_en<br>HDMITX0 eARC RX PHY DMAC receiver enable status.<br>1'b0: Inactive<br>1'b1: Active |
| 26 | RO | 0x0 | hdmitx0_oearcrx_cmdc_rx_en<br>HDMITX0 eARC RX PHY common mode receiver enable status.<br>1'b0: Inactive<br>1'b1: Active |
| 25 | RO | 0x0 | hdmitx0_oearcrx_cmdc_dataout_drv_en<br>HDMITX0 eARC RX PHY common mode driver enable status.<br>1'b0: Inactive<br>1'b1: Active |
| 24 | RO | 0x0 | hdmitx0_phyo_sb_rdy<br>HDMITXPHY0 sideband ready status.<br>1'b0: Inactive<br>1'b1: Active |
| 23:22 | RO | 0x0 | hdmitx0_ophy_data_l3<br>Bit[1:0] of HDMITX0 data output to PHY lane 3 |
| 21:20 | RO | 0x0 | hdmitx0_ophy_data_l2<br>Bit[1:0] of HDMITX0 data output to PHY lane 2 |
| 19:18 | RO | 0x0 | hdmitx0_ophy_data_l1<br>Bit[1:0] of HDMITX0 data output to PHY lane 1 |
| 17:16 | RO | 0x0 | hdmitx0_ophy_data_l0<br>Bit[1:0] of HDMITX0 data output to PHY lane 0 |
| 15:12 | RO | 0x0 | hdmitx0_ophy_txffe3<br>HDMITX0 TxFFE setting for PHY lane 3 |
| 11:8 | RO | 0x0 | hdmitx0_ophy_txffe2<br>HDMITX0 TxFFE setting for PHY lane 2 |
| 7:4 | RO | 0x0 | hdmitx0_ophy_txffe1<br>HDMITX0 TxFFE setting for PHY lane 1 |
| 3:0 | RO | 0x0 | hdmitx0_ophy_txffe0<br>HDMITX0 TxFFE setting for PHY lane 0 |

**VO1_GRF_VO1_STS6**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28 | RO | 0x0 | hdmitx1_oearctx_h14arc_sel<br>HDMITX1 eARC RX PHY HDMI14b ARC mode selection.<br>1'b0: Inactive<br>1'b1: Active |
| 27 | RO | 0x0 | hdmitx1_oearcrx_dmac_phy_rcv_en<br>HDMITX1 eARC RX PHY DMAC receiver enable status.<br>1'b0: Inactive<br>1'b1: Active |
| 26 | RO | 0x0 | hdmitx1_oearcrx_cmdc_rx_en<br>HDMITX1 eARC RX PHY common mode receiver enable status.<br>1'b0: Inactive<br>1'b1: Active |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 25 | RO | 0x0 | hdmitx1_oearcrx_cmdc_dataout_drv_en<br>HDMITX1 eARC RX PHY common mode driver enable status.<br>1'b0: Inactive<br>1'b1: Active |
| 24 | RO | 0x0 | hdmitx1_phyo_sb_rdy<br>HDMITXPHY1 sideband ready status.<br>1'b0: Inactive<br>1'b1: Active |
| 23:22 | RO | 0x0 | hdmitx1_ophy_data_l3<br>Bit[1:0] of HDMITX1 data output to PHY lane 3 |
| 21:20 | RO | 0x0 | hdmitx1_ophy_data_l2<br>Bit[1:0] of HDMITX1 data output to PHY lane 2 |
| 19:18 | RO | 0x0 | hdmitx1_ophy_data_l1<br>Bit[1:0] of HDMITX1 data output to PHY lane 1 |
| 17:16 | RO | 0x0 | hdmitx1_ophy_data_l0<br>Bit[1:0] of HDMITX1 data output to PHY lane 0 |
| 15:12 | RO | 0x0 | hdmitx1_ophy_txffe3<br>HDMITX1 TxFFE setting for PHY lane 3 |
| 11:8 | RO | 0x0 | hdmitx1_ophy_txffe2<br>HDMITX1 TxFFE setting for PHY lane 2 |
| 7:4 | RO | 0x0 | hdmitx1_ophy_txffe1<br>HDMITX1 TxFFE setting for PHY lane 1 |
| 3:0 | RO | 0x0 | hdmitx1_ophy_txffe0<br>HDMITX1 TxFFE setting for PHY lane 0 |

**VO1_GRF_MEM_CON0**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x1410 | mem_cfg_hdsprf<br>Interface configuration for HDSPRF type memory in PD_VO1.<br>Bit[0]: TEST1<br>Bit[1]: TEST_RNM<br>Bit[4:2]: RM<br>Bit[5]: WMD<br>Bit[7]: LS<br>Bit[11:10]: WPULSE<br>Bit[13:12]: RA<br>Other bits: Reserved |

**VO1_GRF_MEM_CON1**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x8010 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0010 | mem_cfg_hsdprf_l16<br>Interface configuration for HSDPRF type memory in PD_VO1, lower 16 bits.<br>Bit[0]: TEST1A<br>Bit[1]: TEST_RNMA<br>Bit[5:2]: RMA<br>Bit[6]: WMDA<br>Bit[8]: LS<br>Bit[11:11]: WPULSE<br>Bit[14:13]: RA<br>Bit[15]: WA[0] |

**VO1_GRF_MEM_CON2**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x011 | mem_cfg_hsdprf_h8<br>Interface configuration for HSDPRF type memory in PD_VO1, higher 8 bits.<br>Bit[0]: WA[1]<br>Bit[1]: TEST1B<br>Bit[5:2]: RMB<br>Other bits: Reserved |

# 6.16 USB_GRF Register Description

## 6.16.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| USB_GRF_HOST0_CON0 | 0x0000 | W | 0x00000820 | usb host0 fladj control |
| USB_GRF_HOST0_CON1 | 0x0004 | W | 0x000004BC | usb host0 control1 |
| USB_GRF_HOST1_CON0 | 0x0008 | W | 0x00000820 | usb host1 fladj control |
| USB_GRF_HOST1_CON1 | 0x000C | W | 0x000004BC | usb host1 control1 |
| USB_GRF_HOST0_STATUS | 0x0010 | W | 0x00000000 | usb host0 status |
| USB_GRF_HOST1_STATUS | 0x0014 | W | 0x00000000 | usb host0 status |
| USB_GRF_USB3OTG0_CON0 | 0x0018 | W | 0x00002000 | usb3otg_0 control0 |
| USB_GRF_USB3OTG0_CON1 | 0x001C | W | 0x00001100 | usb3otg_0 control1 |
| USB_GRF_USB3OTG0_STATUS_LAT0 | 0x0020 | W | 0x00000000 | usb3otg_0 logic analyzer Trace low |
| USB_GRF_USB3OTG0_STATUS_LAT1 | 0x0024 | W | 0x00000000 | usb3otg_0 logic analyzer Trace high |
| USB_GRF_USB3OTG0_STATUS_CB | 0x0028 | W | 0x000007E8 | usb3otg_0 current BELT value |

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| USB_GRF_USB3OTG0_STATUS | 0x002C | W | 0x00000000 | usb3otg_0 status |
| USB_GRF_USB3OTG1_CON0 | 0x0030 | W | 0x00002000 | usb3otg_1 control0 |
| USB_GRF_USB3OTG1_CON1 | 0x0034 | W | 0x00001100 | usb3otg_2 control0 |
| USB_GRF_USB3OTG1_STATUS_LAT0 | 0x0038 | W | 0x00000000 | usb3otg_1 logic analyzer Trace low |
| USB_GRF_USB3OTG1_STATUS_LAT1 | 0x003C | W | 0x00000000 | usb3otg_1 logic analyzer Trace high |
| USB_GRF_USB3OTG1_STATUS_CB | 0x0040 | W | 0x0000078E | usb3otg_1 current BELT value |
| USB_GRF_USB3OTG1_STATUS | 0x0044 | W | 0x00000000 | usb3otg_1 status |
| USB_GRF_USB3OTG0_INTCON | 0x0048 | W | 0x00000000 | usb3otg_0 interrupt control |
| USB_GRF_USB3OTG1_INTCON | 0x004C | W | 0x00000000 | usb3otg_1 interript control |
| USB_GRF_GRF_MEM_CON0 | 0x0050 | W | 0x00008010 | usb memory configuration signal for uhdpdprf |
| USB_GRF_GRF_MEM_CON2 | 0x0058 | W | 0x00001410 | usb memory configuration signal for hdsprf |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.16.2 Detail Registers Description

### USB_GRF_HOST0_CON0

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11:6 | RW | 0x20 | host0_fladj_val_common<br>This feature adjusts any offset from the clock source that drives the macro-SOF counter. The macro-SOF cycle time (number of macro-SOF counter clock periods to generate a macro-SOF microframe length) is equal to 59488 plus this value. The default value is decimal 32, which gives an SOF cycle time of 60000 (each microframe has 60000 bit times).<br>Frame Length (decimal) FLADJ Value (decimal)<br>59488 0 (0x00)<br>59504 1 (0x01)<br>59520 2 (0x02)<br>... ...<br>59984 31 (0x1F)<br>60000 32 (0x20)<br>... ...<br>60496 63 (0x3F) |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5:0 | RW | 0x20 | host0_fladj_val<br>USBHOST fladj bit control.<br>This feature adjusts the frame length of the microframe per port. This value must be the same as that of host0_fladj_val_common, or the EHCI yields undefined results. |

**USB_GRF_HOST0_CON1**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | host0_arb_pause<br>USBHOST ehci/ohci arbiter pause control.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | host0_ohci_susp_lgcy<br>OHCI Clock control signal<br>This is a static strap signal.<br>When tied HIGH and the USB port is owned by OHCI, the signal utmi_suspend_o_n reflects the status of the USB port. (suspend or not suspend). |
| 11 | RW | 0x0 | host0_ohci_cntsel<br>Count Select<br>Selects the counter value for simulation or real time for 1 ms.<br>1'b0: Count full 1 ms<br>1'b1: Simulation time |
| 10 | RW | 0x1 | host0_ohci_clkcktrst<br>Clear Clock Reset<br>Initial reset signal for the Digital Phase-Locked Loop (DPLL) block. This is needed only for simulation and can be tied to inactive in the real netlist. The duration of the reset in simulation must be the same as hreset_n. |
| 9 | RW | 0x0 | host0_app_prt_ovrcur<br>Port Overcurrent Indication from Application<br>When asserted by the application, the corresponding port enters Disable state. This signal controls both EHCI and OHCI controller port state machines. Depending on ownership of the port, the corresponding EHCI or OHCI controller generates an Overcurrent Detect interrupt. |
| 8 | RW | 0x0 | host0_autoppd_on_overcur_en<br>Auto Port Power Disable on Overcurrent<br>This strap signal enables automatic port power disable in the host controller. When this signal is active, if an over-current condition is detected on a powered port and PPC is 1, the PP bit in each affected port is automatically transitioned by the host controller from a 1 to 0, removing power from the port. |
| 7 | RW | 0x1 | host0_word_if<br>Word Interface<br>Selects the data width of the UTMI PHY interface.<br>1'b1: 16bit interface<br>1'b0: 8bit interface<br>Only 16bit used in this application. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | host0_sim_mode<br>USB HOST0 simulation mode bit control<br>Not used in application. |
| 5 | RW | 0x1 | host0_incrx_en<br>Burst Alignment Enable<br>Forces AHB master to start INCR4/8/16 busts only on burst boundaries. AHB requires that double word width burst be addressed aligned only to the double-word boundary.<br>1'b1: Start INCRX burst only on burst x-aligned addresses.<br>1'b0: Normal AHB operation; start bursts on any double word boundary.<br>Note: When this function is enabled, the burst is started only when the lowest bits of haddr are:<br>INCR4: haddr[3:0] == 4'b0000<br>INCR8: haddr[4:0] == 5'b00000<br>INCR16: haddr[5:0] == 6'b000000 |
| 4 | RW | 0x1 | host0_incr8_en<br>AHB Burst Type INCR8 Enable<br>Enables the AHB master interface to utilize burst INCR8 when appropriate.<br>1'b1: Use INCR8 when appropriate.<br>1'b0: Do not use INCR8; use other enabled INCRX bursts or unspecified length burst INCR. |
| 3 | RW | 0x1 | host0_incr4_en<br>AHB Burst Type INCR4 Enable<br>Enables the AHB master interface to utilize burst INCR4 when appropriate.<br>1'b1: Use INCR4 when appropriate.<br>1'b0: Do not use INCR4; use other enabled INCRX bursts or unspecified length burst INCR. |
| 2 | RW | 0x1 | host0_incr16_en<br>AHB Burst Type INCR16 Enable<br>Enables the AHB master interface to utilize burst INCR16 when appropriate.<br>1'b1: Use INCR16 when appropriate.<br>1'b0: Do not use INCR16; use other enabled INCRX bursts or unspecified length burst INCR. |
| 1 | RW | 0x0 | host0_hubsetup_min<br>Some FS devices down the hub do not recover properly after a pre-amble packet, directed at other LS device, if the hub setup time is four FS clocks. Four FS clocks just meet the specification. By adding one extra clock, these FS devices are made to work better. This strap selects four or five FS clocks as hub setup time for interoperability with the various devices. It is recommended to tie low, that is, for five FS clocks. |
| 0 | RW | 0x0 | host0_app_start_clk<br>OHCI Clock control signal<br>This is an asynchronous primary input to the host core. When the OHCI clocks are suspended, the system has to assert this signal to start the clocks (12 and 48 MHz). This should be de-asserted after the clocks are started and before the host is suspended again. (Host is suspended means HCFS = SUSPEND or all the OHCI ports are suspended). |

**USB_GRF_HOST1_CON0**

Rockchip Confidential

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11:6 | RW | 0x20 | host0_fladj_val_common<br>This feature adjusts any offset from the clock source that drives the macro-SOF counter. The macro-SOF cycle time (number of macro-SOF counter clock periods to generate a macro-SOF microframe length) is equal to 59488 plus this value. The default value is decimal 32, which gives an SOF cycle time of 60000 (each microframe has 60000 bit times).<br>Frame Length (decimal) FLADJ Value (decimal)<br>59488 0 (0x00)<br>59504 1 (0x01)<br>59520 2 (0x02)<br>... ...<br>59984 31 (0x1F)<br>60000 32 (0x20)<br>... ...<br>60496 63 (0x3F) |
| 5:0 | RW | 0x20 | host0_fladj_val<br>USBHOST fladj bit control.<br>This feature adjusts the frame length of the microframe per port. This value must be the same as that of host0_fladj_val_common, or the EHCI yields undefined results. |

**USB_GRF_HOST1_CON1**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | host0_arb_pause<br>USBHOST ehci/ohci arbiter pause control.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | host0_ohci_susp_lgcy<br>OHCI Clock control signal<br>This is a static strap signal.<br>When tied HIGH and the USB port is owned by OHCI, the signal utmi_suspend_o_n reflects the status of the USB port. (suspend or not suspend). |
| 11 | RW | 0x0 | host0_ohci_cntsel<br>Count Select<br>Selects the counter value for simulation or real time for 1 ms.<br>1'b0: Count full 1 ms<br>1'b1: Simulation time |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10 | RW | 0x1 | host0_ohci_clkcktrst<br>Clear Clock Reset<br>Initial reset signal for the Digital Phase-Locked Loop (DPLL) block. This is needed only for simulation and can be tied to inactive in the real netlist. The duration of the reset in simulation must be the same as hreset_n. |
| 9 | RW | 0x0 | host0_app_prt_ovrcur<br>Port Overcurrent Indication from Application<br>When asserted by the application, the corresponding port enters Disable state. This signal controls both EHCI and OHCI controller port state machines. Depending on ownership of the port, the corresponding EHCI or OHCI controller generates an Overcurrent Detect interrupt. |
| 8 | RW | 0x0 | host0_autoppd_on_overcur_en<br>Auto Port Power Disable on Overcurrent<br>This strap signal enables automatic port power disable in the host controller. When this signal is active, if an over-current condition is detected on a powered port and PPC is 1, the PP bit in each affected port is automatically transitioned by the host controller from a 1 to 0, removing power from the port. |
| 7 | RW | 0x1 | host0_word_if<br>Word Interface<br>Selects the data width of the UTMI PHY interface.<br>1'b1: 16bit interface<br>1'b0: 8bit interface<br>Only 16bit used in this application. |
| 6 | RW | 0x0 | host0_sim_mode<br>USB HOST0 simulation mode bit control<br>Not used in application. |
| 5 | RW | 0x1 | host0_incrx_en<br>Burst Alignment Enable<br>Forces AHB master to start INCR4/8/16 busts only on burst boundaries. AHB requires that double word width burst be addressed aligned only to the double-word boundary.<br>1'b1: Start INCRX burst only on burst x-aligned addresses.<br>1'b0: Normal AHB operation; start bursts on any double word boundary.<br>Note: When this function is enabled, the burst is started only when the lowest bits of haddr are:<br>INCR4: haddr[3:0] == 4'b0000<br>INCR8: haddr[4:0] == 5'b00000<br>INCR16: haddr[5:0] == 6'b000000 |
| 4 | RW | 0x1 | host0_incr8_en<br>AHB Burst Type INCR8 Enable<br>Enables the AHB master interface to utilize burst INCR8 when appropriate.<br>1'b1: Use INCR8 when appropriate.<br>1'b0: Do not use INCR8; use other enabled INCRX bursts or unspecified length burst INCR. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x1 | host0_incr4_en<br>AHB Burst Type INCR4 Enable<br>Enables the AHB master interface to utilize burst INCR4 when appropriate.<br>1'b1: Use INCR4 when appropriate.<br>1'b0: Do not use INCR4; use other enabled INCRX bursts or unspecified length burst INCR. |
| 2 | RW | 0x1 | host0_incr16_en<br>AHB Burst Type INCR16 Enable<br>Enables the AHB master interface to utilize burst INCR16 when appropriate.<br>1'b1: Use INCR16 when appropriate.<br>1'b0: Do not use INCR16; use other enabled INCRX bursts or unspecified length burst INCR. |
| 1 | RW | 0x0 | host0_hubsetup_min<br>Some FS devices down the hub do not recover properly after a pre-amble packet, directed at other LS device, if the hub setup time is four FS clocks. Four FS clocks just meet the specification. By adding one extra clock, these FS devices are made to work better. This strap selects four or five FS clocks as hub setup time for interoperability with the various devices. It is recommended to tie low, that is, for five FS clocks. |
| 0 | RW | 0x0 | host0_app_start_clk<br>OHCI Clock control signal<br>This is an asynchronous primary input to the host core. When the OHCI clocks are suspended, the system has to assert this signal to start the clocks (12 and 48 MHz). This should be de-asserted after the clocks are started and before the host is suspended again. (Host is suspended means HCFS = SUSPEND or all the OHCI ports are suspended). |

**USB_GRF_HOST0_STATUS**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |
| 30 | RO | 0x0 | host0_ehci_power_state_ack<br>Power State ACK<br>This signal indicates the power state change acknowledgement from the EHCI to the PCI for PCI power management. |
| 29 | RO | 0x0 | host0_ehci_pme_status<br>PME Status<br>This signal displays the PME status. This value is updated in the PCI PMCSR's pme_status bit. |
| 28 | RO | 0x0 | host0_ehci_bufacc<br>EHCI Buffer Access<br>Level signal that is asserted whenever the host controller does a data read/write transfer. If this signal is de-asserted while the AHB is active, the host controller is performing a descriptor read/write. This signal can be used to support Big Endian operation. |
| 27 | RO | 0x0 | host0_ehci_xfer_prdc<br>Transfer Periodic<br>Indicates that the current transfer of the EHCI master on the AHB bus belongs to periodic descriptor/data. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 26 | RO | 0x0 | host0_ohci_ccs<br>Current Connect Status of Each Port<br>When set, this bit indicates that the port state machine is in a connected state. If the bit is cleared, the port state machine is in either a disconnected or powered-off state. |
| 25 | RO | 0x0 | host0_ohci_rwe<br>Remote Wake Up Enable<br>This bit reflects the HcControl.RWE bit. This is brought out as a status signal and can be ignored by the application for normal host controller operation. |
| 24 | RO | 0x0 | host0_ohci_drwe<br>Device Remote Wake-Up Enable<br>This signal reflects the HcRhStatus.DRWE bit. When active, it causes the host controller to treat a connect or disconnect event as a remote wake-up, which in turn causes the host controller to enter the Global Resume state from the Global Suspend state. If this bit is cleared, a connect or disconnect event is not treated as a remote wake-up event. |
| 23 | RO | 0x0 | host0_ohci_globalsuspend<br>Host Controller is in Global Suspend State<br>This signal is asserted 5 ms after the host controller enters the USB Suspend state, and is asserted as long as the host controller remains in this state. The host controller enters the USB Suspend state when the Host Controller Driver forces it by writing to the HcControl.HCFS bits. The host controller exits this state when either the Host Controller Driver moves it to USB Reset (Global USB Reset) or USB Resume (Global Resume) or when a remote wake-up event is seen at one of the downstream USB ports. |
| 22 | RO | 0x0 | host0_ohci_bufacc<br>Host Controller Buffer Access Indicator<br>When active, this signal indicates that the host controller is currently accessing the data buffer indicated by the TD. This is simply a status signal to let the application know whether the host controller is reading from or writing to the data buffer indicated by TD, or reading from or writing to the ED, TD descriptor, etc. If this is set (1) during the cycle on the HCI master bus, it indicates buffer fetch and if reset (0), all other transfers (such as ED, TD fetch, and Status Writeback). This is a status signal; the application need not take any action when it is asserted. |
| 21 | RO | 0x0 | host0_ohci_rmtwkp<br>Remote Wakeup Status<br>See the HCI_MRmtWkp signal description in the USB 1.1 OHCI Host Controller Family Databook. |
| 20:17 | RO | 0x0 | host0_ehci_lpsmc_state<br>LPSMC State<br>This signal indicates the state of the LPSMC module. It is used only for debugging. |
| 16:11 | RO | 0x00 | host0_ehci_usbsts<br>USB Status<br>EHCI USBSTS register[5:0] bits. This signal indicates pending interrupts and various host controller statuses. These 6 bits reflect the value in the USBSTS[5:0] register.<br>Active High. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10:0 | RO | 0x000 | host0_ehci_xfer_cnt<br>Transfer Count<br>Transfer byte count from the EHCI master of the current AHB transaction. This is a constant signal and its value is valid when the EHCI starts its AHB address phase.<br>The host controller aborts an AHB transfer before completing the transactions specified in ehci_xfer_cnt when a data read transaction is in progress and both these conditions are true:<br>1. There is insufficient time to complete the USB transfer.<br>2. The Root Hub detects an underrun condition. |

**USB_GRF_HOST1_STATUS**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |
| 30 | RO | 0x0 | host1_ehci_power_state_ack<br>Power State ACK<br>This signal indicates the power state change acknowledgement from the EHCI to the PCI for PCI power management. |
| 29 | RO | 0x0 | host1_ehci_pme_status<br>PME Status<br>This signal displays the PME status. This value is updated in the PCI PMCSR's pme_status bit. |
| 28 | RO | 0x0 | host1_ehci_bufacc<br>EHCI Buffer Access<br>Level signal that is asserted whenever the host controller does a data read/write transfer. If this signal is de-asserted while the AHB is active, the host controller is performing a descriptor read/write. This signal can be used to support Big Endian operation. |
| 27 | RO | 0x0 | host1_ehci_xfer_prdc<br>Transfer Periodic<br>Indicates that the current transfer of the EHCI master on the AHB bus belongs to periodic descriptor/data. |
| 26 | RO | 0x0 | host1_ohci_ccs<br>Current Connect Status of Each Port<br>When set, this bit indicates that the port state machine is in a connected state. If the bit is cleared, the port state machine is in either a disconnected or powered-off state. |
| 25 | RO | 0x0 | host1_ohci_rwe<br>Remote Wake Up Enable<br>This bit reflects the HcControl.RWE bit. This is brought out as a status signal and can be ignored by the application for normal host controller operation. |
| 24 | RO | 0x0 | host1_ohci_drwe<br>Device Remote Wake-Up Enable<br>This signal reflects the HcRhStatus.DRWE bit. When active, it causes the host controller to treat a connect or disconnect event as a remote wake-up, which in turn causes the host controller to enter the Global Resume state from the Global Suspend state. If this bit is cleared, a connect or disconnect event is not treated as a remote wake-up event. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23 | RO | 0x0 | host1_ohci_globalsuspend<br>Host Controller is in Global Suspend State<br>This signal is asserted 5 ms after the host controller enters the USB Suspend state, and is asserted as long as the host controller remains in this state. The host controller enters the USB Suspend state when the Host Controller Driver forces it by writing to the HcControl.HCFS bits. The host controller exits this state when either the Host Controller Driver moves it to USB Reset (Global USB Reset) or USB Resume (Global Resume) or when a remote wake-up event is seen at one of the downstream USB ports. |
| 22 | RO | 0x0 | host1_ohci_bufacc<br>Host Controller Buffer Access Indicator<br>When active, this signal indicates that the host controller is currently accessing the data buffer indicated by the TD. This is simply a status signal to let the application know whether the host controller is reading from or writing to the data buffer indicated by TD, or reading from or writing to the ED, TD descriptor, etc. If this is set (1) during the cycle on the HCI master bus, it indicates buffer fetch and if reset (0), all other transfers (such as ED, TD fetch, and Status Writeback). This is a status signal; the application need not take any action when it is asserted. |
| 21 | RO | 0x0 | host1_ohci_rmtwkp<br>Remote Wakeup Status<br>See the HCI_MRmtWkp signal description in the USB 1.1 OHCI Host Controller Family Databook. |
| 20:17 | RO | 0x0 | host1_ehci_lpsmc_state<br>LPSMC State<br>This signal indicates the state of the LPSMC module. It is used only for debugging. |
| 16:11 | RO | 0x00 | host1_ehci_usbsts<br>USB Status<br>EHCI USBSTS register[5:0] bits. This signal indicates pending interrupts and various host controller statuses. These 6 bits reflect the value in the USBSTS[5:0] register.<br>Active High. |
| 10:0 | RO | 0x000 | host1_ehci_xfer_cnt<br>Transfer Count<br>Transfer byte count from the EHCI master of the current AHB transaction. This is a constant signal and its value is valid when the EHCI starts its AHB address phase.<br>The host controller aborts an AHB transfer before completing the transactions specified in ehci_xfer_cnt when a data read transaction is in progress and both these conditions are true:<br>1. There is insufficient time to complete the USB transfer.<br>2. The Root Hub detects an underrun condition. |

**USB_GRF_USB3OTG0_CON0**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x0 | usb3otg0_host_u2_port_disable<br>USB2.0 Port Disable control.<br>1'b0: Port Enabled.<br>1'b1: Port Disabled When 1, this signal stops reporting connect/disconnect events the port and keeps the port in disabled state. |
| 14 | RW | 0x0 | usb3otg0_host_port_power_control_present<br>This indicates whether the host controller implementation includes port power control.<br>1'b0: Indicates that the port does not have port power switches.<br>1'b1: Indicates that the port has port power switches. |
| 13:8 | RW | 0x20 | usb3otg0_fladj_30mhz_reg<br>HS Jitter Adjustment. Indicates the correction required to accommodate mac3 clock and utmi clock jitter to measure 125 's duration.<br>With fladj_30mhz_reg tied to zero, the high speed 125us micro-frame is counted for 123933ns. You must program the value in terms of high speed bit times in a 30 MHz cycle. The default value that must be driven is 32 (assuming 30 MHz perfect clock). Fladj_30mhz_reg connects to the FLADJ register defined in the xHCI spec in the PCI configuration space. Each count is equal to 16 high speed bit times. By default, when this register is set to 32, it gives a 125us interval.<br>Now, based the clock accuracy you can decrement the count or increment the count to get the 125 us uSOF window. For non-PCI systems, it is recommended that this strap is connected to a register that can be controlled by software. This strap is used in device mode also. If device only mode is implemented, it is recommended to tie this input to 'd32. |
| 7:6 | RW | 0x0 | usb3otg0_hub_port_perm_attach<br>Indicates if the device attached to a downstream port is permanently attached or not.<br>1'b0: Not permanently attached<br>1'b1: Permanently attached<br>Bit0 is for USB2.0 port and bit1 are for USB 3.0 SS port. |
| 5:4 | RW | 0x0 | usb3otg0_hub_port_overcurrent<br>This is the per port Overcurrent indication of the root-hub ports:<br>1'b0: No Overcurrent<br>1'b1: Overcurrent<br>Bit0 is for USB 2.0 port and bit1 are for USB 3.0 SS port. |
| 3:0 | RW | 0x0 | usb3otg0_bus_filter_bypass<br>It is expected that this signal is set or reset at power-on reset and is not changed during the normal<br>operation of the core. The function of each bit is:<br>bus_filter_bypass[3]: Bypass the filter for utmiotg_iddig<br>bus_filter_bypass[2]: Bypass the filters for utmisrp_bvalid and utmisrp_sessend<br>bus_filter_bypass[1]: Bypass the filter for pipe3_PowerPresent all U3 ports<br>bus_filter_bypass[0]: Bypass the filter for utmiotg_vbusvalid all U2 ports<br>In non-OTG Host-only mode, internal bus filters are not needed. Values:<br>1'b0: Bus filter(s) enabled<br>1'b1: Bus filter(s) disabled (bypassed) |

Rockchip Confidential

**USB_GRF_USB3OTG0_CON1**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x1 | usb3otg0_host_num_u3_port<br>xHCI usb3 port number, default as 1 |
| 11:8 | RW | 0x1 | usb3otg0_host_num_u2_port<br>xHCI host USB2 Port number, default as 1 |
| 7 | RW | 0x0 | usb3otg0_pipe_clk_sel<br>usb3otg0_pipe3_rx_pclk/tx_pclk input source clock select<br>1'b0: Select clk_usb3otg0_pipe for source clock<br>1'b0: Select clk_usb3otg0_utmi for source clock |
| 6 | RO | 0x0 | reserved |
| 5 | RW | 0x0 | usb3otg0_host_legacy_smi_bar<br>Use this register to support SMI on BAR defined in xHCI spec.<br>SW must set this register, then clear this register to indicate Base Address Register written. |
| 4 | RW | 0x0 | usb3otg0_host_legacy_smi_pci_cmd<br>Use this register to support SMI on PCI Command defined in xHCI spec.<br>SW must set this register, then clear this register to indicate PCI command register written. |
| 3:2 | RW | 0x0 | usb3otg0_phystatus_con<br>Grf controll usb pipe phystatus.<br>2'b00: Select phystatus form PHY.<br>2'b10: Select phystatus to 0. |
| 1 | RW | 0x0 | usb3otg0_pme_en<br>Enable signal for the pme_generation. Enable the core to assert pme_generation. |
| 0 | RW | 0x0 | usb3otg0_host_u3_port_disable<br>USB 3.0 SS Port Disable control.<br>1'b0: Port Enabled<br>1'b1: Port Disabled |

**USB_GRF_USB3OTG0_STATUS_LAT0**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | usb3otg_logic_analyzer_trace0<br>Usb3otg_logic_analyzer_trace[31:0] bit status.<br>Logic Analyzer Trace. These are internal design signals that you can use for debug purposes. Some of the signals are interface signals like PIPE, UTMI, ULPI, AXI, and AHB, and others are internal state machines and status information signals. During chip bring-up, to debug functional issues, you can probe the interface signals for additional visibility. |

**USB_GRF_USB3OTG0_STATUS_LAT1**

Address: Operational Base + offset (0x0024)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | usb3otg_logic_analyzer_trace1<br>Usb3otg_logic_analyzer_trace[63:32] bit status<br>Logic Analyzer Trace. These are internal design signals that you can use for debug purposes. Some of the signals are interface signals like PIPE, UTMI, ULPI, AXI, and AHB, and others are internal state machines and status information signals. During chip bring-up, to debug functional issues, you can probe the interface signals for additional visibility. |

**USB_GRF_USB3OTG0_STATUS_CB**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x7e8 | usb3otg_host_current_belt[11:0]<br>Usb3otg_host_current_belt[11:0] bit status<br>Current BELT Value.<br>This signal indicates the minimum value of all received BELT values and the BELT that is set by the Set LTV command. This signal is valid only in Host mode. |

**USB_GRF_USB3OTG0_STATUS**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RO | 0x0 | usb3otg0_pme_generation<br>PME Generation.<br>This signal is used to generate a PME (Power Management Event). When the Run/Stop bit of the USB Command Register is cleared during USB suspend mode, the core cannot generate an event and cannot assert a regular interrupt. In this case, the core asserts a pme_generation signal to report any wakeup condition if pme_en is high.<br>If the system does not support PCI-like PME interface, then it must not clear the Run/Stop bit during USB suspend mode. In this case, the core generates an event and asserts an interrupt when there is any wakeup event. |
| 0 | RO | 0x0 | usb3otg0_host_sys_err<br>Host System Error.<br>This signal indicates that a Host System Error has occurred as reflected in the USBSTS.HSE field. This signal is asserted only if the USBCMD.HSEE field is set to '1'. It can occur when the host controller encounters an 'Error' response in the AHB, the AXI, or the Native Master Bus. When the USBSTS.HSE field is cleared by software, this signal is de-asserted unless the master continues to assert its bus error output. The typical software response to an HSE is to reset the core. For more details, refer to section 4.10.2.6 of the xHCI 1.0 specification. |

**USB_GRF_USB3OTG1_CON0**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x0 | usb3otg1_host_u2_port_disable<br>USB2.0 Port Disable control.<br>1'b0: Port Enabled.<br>1'b1: Port Disabled When 1, this signal stops reporting connect/disconnect events the port and keeps the port in disabled state. |
| 14 | RW | 0x0 | usb3otg1_host_port_power_control_present<br>This indicates whether the host controller implementation includes port power control.<br>1'b0: Indicates that the port does not have port power switches.<br>1'b1: Indicates that the port has port power switches. |
| 13:8 | RW | 0x20 | usb3otg1_fladj_30mhz_reg<br>HS Jitter Adjustment. Indicates the correction required to accommodate mac3 clock and utmi clock jitter to measure 125 's duration.<br>With fladj_30mhz_reg tied to zero, the high speed 125us micro-frame is counted for 123933ns. You must program the value in terms of high speed bit times in a 30 MHz cycle. The default value that must be driven is 32 (assuming 30 MHz perfect clock). Fladj_30mhz_reg connects to the FLADJ register defined in the xHCI spec in the PCI configuration space. Each count is equal to 16 high speed bit times. By default, when this register is set to 32, it gives a 125us interval.<br>Now, based the clock accuracy you can decrement the count or increment the count to get the 125 us uSOF window. For non-PCI systems, it is recommended that this strap is connected to a register that can be controlled by software. This strap is used in device mode also. If device only mode is implemented, it is recommended to tie this input to 'd32. |
| 7:6 | RW | 0x0 | usb3otg1_hub_port_perm_attach<br>Indicates if the device attached to a downstream port is permanently attached or not.<br>1'b0: Not permanently attached<br>1'b1: Permanently attached<br>Bit0 is for USB2.0 port and bit1 are for USB 3.0 SS port. |
| 5:4 | RW | 0x0 | usb3otg1_hub_port_overcurrent<br>This is the per port Overcurrent indication of the root-hub ports:<br>1'b0: No Overcurrent<br>1'b1: Overcurrent<br>Bit0 is for USB 2.0 port and bit1 are for USB 3.0 SS port. |
| 3:0 | RW | 0x0 | usb3otg1_bus_filter_bypass<br>It is expected that this signal is set or reset at power-on reset and is not changed during the normal<br>operation of the core. The function of each bit is:<br>bus_filter_bypass[3]: Bypass the filter for utmiotg_iddig<br>bus_filter_bypass[2]: Bypass the filters for utmisrp_bvalid and utmisrp_sessend<br>bus_filter_bypass[1]: Bypass the filter for pipe3_PowerPresent all U3 ports<br>bus_filter_bypass[0]: Bypass the filter for utmiotg_vbusvalid all U2 ports<br>In non-OTG Host-only mode, internal bus filters are not needed. Values:<br>1'b0: Bus filter(s) enabled<br>1'b1: Bus filter(s) disabled (bypassed) |

Rockchip Confidential

**USB_GRF_USB3OTG1_CON1**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x1 | usb3otg1_host_num_u3_port<br>xHCI usb3 port number, default as 1 |
| 11:8 | RW | 0x1 | usb3otg1_host_num_u2_port<br>xHCI host USB2 Port number, default as 1 |
| 7 | RW | 0x0 | usb3otg1_pipe_clk_sel<br>usb3otg1_pipe3_rx_pclk/tx_pclk input source clock select<br>1'b0: Select clk_usb3otg0_pipe for source clock<br>1'b0: Select clk_usb3otg0_utmi for source clock |
| 6 | RO | 0x0 | reserved |
| 5 | RW | 0x0 | usb3otg1_host_legacy_smi_bar<br>Use this register to support SMI on BAR defined in xHCI spec.<br>SW must set this register, then clear this register to indicate Base Address Register written. |
| 4 | RW | 0x0 | usb3otg1_host_legacy_smi_pci_cmd<br>Use this register to support SMI on PCI Command defined in xHCI spec.<br>SW must set this register, then clear this register to indicate PCI command register written. |
| 3:2 | RW | 0x0 | usb3otg1_phystatus_con<br>Grf controll usb pipe phystatus.<br>2'b00: Select phystatus form phy.<br>2'b10: Select phystatus to 0. |
| 1 | RW | 0x0 | usb3otg1_pme_en<br>Enable signal for the pme_generation. Enable the core to assert pme_generation. |
| 0 | RW | 0x0 | usb3otg1_host_u3_port_disable<br>USB 3.0 SS Port Disable control.<br>1'b0: Port Enabled<br>1'b1: Port Disabled |

**USB_GRF_USB3OTG1_STATUS_LAT0**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | usb3otg_logic_analyzer_trace0<br>Usb3otg_logic_analyzer_trace[31:0] bit status.<br>Logic Analyzer Trace. These are internal design signals that you can use for debug purposes. Some of the signals are interface signals like PIPE, UTMI, ULPI, AXI, and AHB, and others are internal state machines and status information signals. During chip bring-up, to debug functional issues, you can probe the interface signals for additional visibility. |

**USB_GRF_USB3OTG1_STATUS_LAT1**

Address: Operational Base + offset (0x003C)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | usb3otg_logic_analyzer_trace1<br>Usb3otg_logic_analyzer_trace[63:32] bit status<br>Logic Analyzer Trace. These are internal design signals that you can use for debug purposes. Some of the signals are interface signals like PIPE, UTMI, ULPI, AXI, and AHB, and others are internal state machines and status information signals. During chip bring-up, to debug functional issues, you can probe the interface signals for additional visibility. |

**USB_GRF_USB3OTG1_STATUS_CB**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x78e | usb3otg_host_current_belt[11:0]<br>Usb3otg_host_current_belt[11:0] bit status<br>Current BELT Value.<br>This signal indicates the minimum value of all received BELT values and the BELT that is set by the Set LTV command. This signal is valid only in Host mode. |

**USB_GRF_USB3OTG1_STATUS**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RO | 0x0 | usb3otg0_pme_generation<br>PME Generation.<br>This signal is used to generate a PME(Power Management Event). When the Run/Stop bit of the USB Command Register is cleared during USB suspend mode, the core cannot generate an event and cannot assert a regular interrupt. In this case, the core asserts a pme_generation signal to report any wakeup condition if pme_en is high.<br>If the system does not support PCI-like PME interface, then it must not clear the Run/Stop bit during USB suspend mode. In this case, the core generates an event and asserts an interrupt when there is any wakeup event. |
| 0 | RO | 0x0 | usb3otg0_host_sys_err<br>Host System Error.<br>This signal indicates that a Host System Error has occurred as reflected in the USBSTS.HSE field. This signal is asserted only if the USBCMD.HSEE field is set to '1'. It can occur when the host controller encounters an 'Error' response in the AHB, the AXI, or the Native Master Bus. When the USBSTS.HSE field is cleared by software, this signal is de-asserted unless the master continues to assert its bus error output. The typical software response to an HSE is to reset the core. For more details, refer to section 4.10.2.6 of the xHCI 1.0 specification. |

**USB_GRF_USB3OTG0_INTCON**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | usb3otg0_pme_generation_irq_en<br>1'b0: IRQ disable<br>1'b1: IRQ enable |
| 0 | RW | 0x0 | usb3otg0_host_sys_err_irq_en<br>1'b0: IRQ disable<br>1'b1: IRQ enable |

**USB_GRF_USB3OTG1_INTCON**

Address: Operational Base + offset (0x004C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | usb3otg1_pme_generation_irq_en<br>1'b0: IRQ disable<br>1'b1: IRQ enable |
| 0 | RW | 0x0 | usb3otg1_host_sys_err_irq_en<br>1'b0: IRQ disable<br>1'b1: IRQ enable |

**USB_GRF_GRF_MEM_CON0**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16:0 | RW | 0x08010 | mem_cfg_uhddprf<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMDA<br>bit 7: LS<br>bit 16: TESTRWM |

**USB_GRF_GRF_MEM_CON2**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x1410 | mem_cfg_hdsprf<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMD<br>bit 7: LS<br>bit 11~10: WPULSE<br>bit 13~12: RA |

# 6.17 PHP_GRF Register Description

## 6.17.1 Registers Summary

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PHP_GRF_PHP_CON0 | 0x0000 | W | 0x00000820 | PHP GRF control register0 |
| PHP_GRF_PHP_CON1 | 0x0004 | W | 0x00000000 | PHP GRF control register1 |
| PHP_GRF_GMAC_CON0 | 0x0008 | W | 0x00000020 | PHP GMAC GRF control register0 |
| PHP_GRF_SATA_CON0 | 0x0010 | W | 0x00000020 | PHP SATA GRF PIPE interface control register1 |
| PHP_GRF_SATA_CON1 | 0x0014 | W | 0x00000020 | PHP SATA GRF PIPE interface control register1 |
| PHP_GRF_SATA_CON2 | 0x0018 | W | 0x00000020 | PHP SATA GRF PIPE interface control register2 |
| PHP_GRF_PHP_MMU_CON0 | 0x001C | W | 0x00000028 | PHP MMU control register0 |
| PHP_GRF_PHP_MMU_CON1 | 0x0020 | W | 0x0000000C | PHP MMU control register1 |
| PHP_GRF_PHP_MMU_CON2 | 0x0024 | W | 0x00000000 | PHP MMU control register2 |
| PHP_GRF_ITS_TADDR0 | 0x0028 | W | 0x0000FE65 | PHP MMU GRF ITS target address0 |
| PHP_GRF_ITS_TADDR1 | 0x002C | W | 0x0000FE67 | PHP MMU GRF ITS target address1 |
| PHP_GRF_PCIE_MMU_PCIEMODE | 0x0030 | W | 0x00000003 | PCIe MMU PCIe mode control |
| PHP_GRF_PCIE_MMU_CON0 | 0x0034 | W | 0x00000028 | PCIe MMU control register0 |
| PHP_GRF_PCIE_MMU_CON1 | 0x0038 | W | 0x0000001C | PCIe MMU control register1 |
| PHP_GRF_PCIE_MMU_CON2 | 0x003C | W | 0x0000001C | PCIe MMU control register2 |
| PHP_MEM_CON0 | 0x0040 | W | 0x00110010 | PHP memory configuration signal for hsdprf |
| PHP_GRF_PHP_ST0 | 0x0044 | W | 0x00000000 | PHP status register0 |
| PHP_GRF_PHP_ST1 | 0x0048 | W | 0x00000000 | PHP status register1 |
| PHP_GRF_PHP_ST2 | 0x004C | W | 0x00000000 | PHP status register2 |
| PHP_GRF_PHP_ST3 | 0x0050 | W | 0x00000000 | PHP status register3 |
| PHP_GRF_PHP_ST4 | 0x0054 | W | 0x00000000 | PHP status register4 |
| PHP_GRF_MMU_PMU_ACK | 0x0058 | W | 0x00000000 | MMU PMU acknowledge status |
| PHP_GRF_PCIE_MMU_CON6 | 0x005C | W | 0x00000000 | PCIe MMU control register6 |
| PHP_GRF_PCIE_MMU_CON7 | 0x0060 | W | 0x00000000 | PCIe MMU control register7 |
| PHP_GRF_MEM_CON5 | 0x0064 | W | 0x00008010 | PHP memory configuration signal for uhdpdprf |
| PHP_GRF_MEM_CON10 | 0x0068 | W | 0x00001410 | PHP memory configuration signal for hdsprf |
| PHP_GRF_CLK_CON1 | 0x0070 | W | 0x00000000 | GMAC clk control register |
| PHP_GRF_GMAC0_SID_AW | 0x0074 | W | 0x00000000 | GMAC0 SID control for AW channel |
| PHP_GRF_GMAC0_SSID_AW | 0x0078 | W | 0x00000000 | GMAC1 SSID control for AW channel |
| PHP_GRF_GMAC1_SID_AW | 0x007C | W | 0x00000000 | GMAC1 SID control for AW channel |
| PHP_GRF_GMAC1_SSID_AW | 0x0080 | W | 0x00000000 | GMAC1 SSID control for AW channel |
| PHP_GRF_SATA0_SID_AW | 0x0084 | W | 0x00000000 | SATA0 SID control for AW channel |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PHP_GRF_SATA0_SSID_AW | 0x0088 | W | 0x00000000 | SATA0 SSID control for AW channel |
| PHP_GRF_SATA1_SID_AW | 0x008C | W | 0x00000000 | SATA1 SID control for AW channel |
| PHP_GRF_SATA1_SSID_AW | 0x0090 | W | 0x00000000 | SATA1 SSID control for AW channel |
| PHP_GRF_SATA2_SID_AW | 0x0094 | W | 0x00000000 | SATA2 SID control for AW channel |
| PHP_GRF_SATA2_SSID_AW | 0x0098 | W | 0x00000000 | SATA2 SSID control for AW channel |
| PHP_GRF_GMAC0_SID_AR | 0x009C | W | 0x00000000 | GMAC0 SID control for AR channel |
| PHP_GRF_GMAC0_SSID_AR | 0x00A0 | W | 0x00000000 | GMAC0 SSID control for AR channel |
| PHP_GRF_GMAC1_SID_AR | 0x00A4 | W | 0x00000000 | GMAC1 SID control for AR channel |
| PHP_GRF_GMAC1_SSID_AR | 0x00A8 | W | 0x00000000 | GMAC1 SSID control for AR channel |
| PHP_GRF_SATA0_SID_AR | 0x00AC | W | 0x00000000 | SATA0 SID control for AR channel |
| PHP_GRF_SATA0_SSID_AR | 0x00B0 | W | 0x00000000 | SATA0 SSID control for AR channel |
| PHP_GRF_SATA1_SID_AR | 0x00B4 | W | 0x00000000 | SATA1 SID control for AR channel |
| PHP_GRF_SATA1_SSID_AR | 0x00B8 | W | 0x00000000 | SATA1 SSID control for AR channel |
| PHP_GRF_SATA2_SID_AR | 0x00BC | W | 0x00000000 | SATA2 SID control for AR channel |
| PHP_GRF_SATA2_SSID_AR | 0x00C0 | W | 0x00000000 | SATA2 SSID control for AR channel |
| PHP_GRF_USB3OTG_2_SID_AR | 0x00C4 | W | 0x00000000 | USB3OTG_2 SID control for AR channel |
| PHP_GRF_USB3OTG_2_SSID_AR | 0x00C8 | W | 0x00000000 | USB3OTG_2 SID control for AR channel |
| PHP_GRF_USB3OTG_2_SID_AW | 0x00CC | W | 0x00000000 | USB3OTG_2 SID control for AW channel |
| PHP_GRF_USB3OTG_2_SSID_AW | 0x00D0 | W | 0x00000000 | USB3OTG_2 SSID control for AW channel |
| PHP_GRF_GMAC_CON_PST | 0x00D4 | W | 0x00000000 | GMAC media clock generation control |
| PHP_GRF_GMAC0_CMD | 0x00D8 | W | 0x00000000 | GMAC0 command |
| PHP_GRF_GMAC1_CMD | 0x00DC | W | 0x00000000 | GMAC0 command |
| PHP_GRF_MEM_CON11 | 0x00E0 | W | 0x00001410 | PHP memory configuration signal for hdspra |
| PHP_GRF_USB3OTG_2_CON0 | 0x00E4 | W | 0x00002000 | USB3OTG_0 control0 |
| PHP_GRF_USB3OTG_2_CON1 | 0x00E8 | W | 0x00001100 | USB3OTG_0 control1 |
| PHP_GRF_USB3OTG_2_INTCON | 0x00EC | W | 0x00000000 | USB3OTG_2 int control |
| PHP_GRF_USB3OTG_2_ST_LAT0 | 0x00F0 | W | 0x00000000 | USB3OTG_2 logic analyzer Trace low |
| PHP_GRF_USB3OTG_2_ST_LAT1 | 0x00F4 | W | 0x00000000 | USB3OTG_2 logic analyzer Trace high |
| PHP_GRF_USB3OTG_2_ST_CB | 0x00F8 | W | 0x0000078E | USB3OTG_2 current BELT value |
| PHP_GRF_USB3OTG_2_ST | 0x00FC | W | 0x00000000 | USB3OTG_2 status |
| PHP_GRF_PCIESEL_CON | 0x0100 | W | 0x00000003 | PCIe PHY interface select |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PHP_GRF_UTMI_CON | 0x0104 | W | 0x00000300 | GRF control UTMI interface for USB3 only mode |
| PHP_GRF_PCIE4L_SID_AW | 0x010C | W | 0x00000000 | GRF controller PCIe4L SID for AW channel |
| PHP_GRF_PCIE4L_SID_AR | 0x0110 | W | 0x00000000 | GRF controller PCIe4L SID for AR channel |
| PHP_GRF_PCIE2L_SID_AW | 0x0114 | W | 0x00000000 | GRF controller PCIe2L SID for AW channel |
| PHP_GRF_PCIE2L_SID_AR | 0x0118 | W | 0x00000000 | GRF controller PCIe2L SID for AR channel |
| PHP_GRF_PCIE1L0_SID_AW | 0x011C | W | 0x00000000 | GRF controller PCIe1L0 SID for AW channel |
| PHP_GRF_PCIE1L0_SID_AR | 0x0120 | W | 0x00000000 | GRF controller PCIe1L0 SID for AR channel |
| PHP_GRF_PCIE1L1_SID_AW | 0x0124 | W | 0x00000000 | GRF controller PCIe1L1 SID for AW channel |
| PHP_GRF_PCIE1L1_SID_AR | 0x0128 | W | 0x00000000 | GRF controller PCIe1L1 SID for AR channel |
| PHP_GRF_PCIE1L2_SID_AW | 0x012C | W | 0x00000000 | GRF controller PCIe1L2 SID for AW channel |
| PHP_GRF_PCIE1L2_SID_AR | 0x0130 | W | 0x00000000 | GRF controller PCIe1L2 SID for AR channel |
| PHP_GRF_PCIE_ATS | 0x0138 | W | 0x00000000 | GRF control PCIe ATS |
| PHP_GRF_ST_UTMI | 0x013C | W | 0x00000034 | USB3OTG_2 UTMI interface status for usb3 only mode |
| PHP_GRF_PCIE4L_SSID_AW | 0x0144 | W | 0x00000000 | GRF controller PCIe4L SID for AW channel |
| PHP_GRF_PCIE4L_SSID_AR | 0x0148 | W | 0x00000000 | GRF controller PCIe4L SID for AR channel |
| PHP_GRF_PCIE2L_SSID_AW | 0x014C | W | 0x00000000 | GRF controller PCIe2L SID for AW channel |
| PHP_GRF_PCIE2L_SSID_AR | 0x0150 | W | 0x00000000 | GRF controller PCIe2L SID for AR channel |
| PHP_GRF_PCIE1L0_SSID_AW | 0x0154 | W | 0x00000000 | GRF controller PCIe1L0 SID for AW channel |
| PHP_GRF_PCIE1L0_SSID_AR | 0x0158 | W | 0x00000000 | GRF controller PCIe1L1 SID for AW channel |
| PHP_GRF_PCIE1L1_SSID_AW | 0x015C | W | 0x00000000 | GRF controller PCIe1L1 SID for AW channel |
| PHP_GRF_PCIE1L1_SSID_AR | 0x0160 | W | 0x00000000 | GRF controller PCIe1L1 SID for AR channel |
| PHP_GRF_PCIE1L2_SSID_AW | 0x0164 | W | 0x00000000 | GRF controller PCIe1L2 SID for AW channel |
| PHP_GRF_PCIE1L2_SSID_AR | 0x0168 | W | 0x00000000 | GRF controller PCIe1L2 SID for AR channel |
| PHP_GRF_PCIE_SSID_V | 0x016C | W | 0x00000000 | GRF controller PCIe SSID_V |
| PHP_GRF_SATA_PD_SEL | 0x0174 | W | 0x00000000 | SATA pipe interface power down sel |
| PHP_PCIE_MMU_IRQ_CLR | 0x0178 | W | 0x00000000 | PCIe MMU interrupt clear |
| PHP_PHP_MMU_IRQ_CLR | 0x017C | W | 0x00000000 | PHP MMU interrupt clear |
| PHP_PCIE_MMU_ST | 0x0180 | W | 0x00000000 | PCIe MMU interrupt state |
| PHP_PHP_MMU_ST | 0x0184 | W | 0x00000000 | PHP MMU interrupt state |
| PHP_PHP_ST0B | 0x018C | W | 0x00000000 | PHP status register0b |

Rockchip Confidential

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.17.2 Detail Registers Description

**PHP_GRF_PHP_CON0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | pcie2_pclkreq_n<br>Combo PHY2 CLKREQ control.<br>Only when PCIe mode be set to comb PHY, this bit can be selected, otherwise this bit will not take effect. This will be selected with PCIe1l1 controller. |
| 12 | RW | 0x0 | pcie1_pclkreq_n<br>Combo PHY1 CLKREQ control.<br>Only when PCIe mode be set to comb PHY, this bit can be selected, otherwise this bit will not take effect. This will be selected with PCIe1l0 controller. |
| 11 | RW | 0x1 | sata1_phy_rx_err<br>SATA1 phy_rx_err input control, before using set this bit to 1'b0. |
| 10:9 | RW | 0x0 | sata1_phy_spdmode<br>SATA1 phy_spdmode input control<br>2'b00: 1.5Gb/s<br>2'b01: 3.0Gb/s<br>2'b10: 6.0Gb/s<br>2'b11: Reserved<br>This should be set before using SATA. |
| 8 | RO | 0x0 | reserved |
| 7 | RW | 0x0 | sata0_phy_rx_err<br>SATA0 phy_rx_err input control, before using set this bit to 1'b0. |
| 6:5 | RW | 0x1 | sata0_phy_spdmode<br>SATA0 phy_spdmode input control<br>2'b00: 1.5Gb/s<br>2'b01: 3.0Gb/s<br>2'b10: 6.0Gb/s<br>2'b11: Reserved<br>This should be set before using SATA. |
| 4 | RW | 0x0 | pcie1l2_link_rst_grt<br>PCIe 1lane2 link reset grant control. |
| 3 | RW | 0x0 | pcie1l1_link_rst_grt<br>PCIe 1lane1 link reset grant control. |
| 2 | RW | 0x0 | pcie1l0_link_rst_grt<br>PCIe 1lane0 link reset grant control. |
| 1 | RW | 0x0 | pcie2l_link_rst_grt<br>PCIe 2lane link reset grant control. |
| 0 | RW | 0x0 | pie4l_link_rst_grt<br>PCIe 4lane link reset grant control. |

**PHP_GRF_PHP_CON1**

Address: Operational Base + offset (0x0004)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:3 | RO | 0x0000 | reserved |
| 2 | RW | 0x0 | sata2_phy_rx_err<br>SATA1 phy_rx_err input control, before using set this bit to 1'b0. |
| 1:0 | RW | 0x0 | sata2_phy_spdmode<br>SATA2 phy_spdmode input control<br>2'b00: 1.5Gb/s<br>2'b01: 3.0Gb/s<br>2'b10: 6.0Gb/s<br>2'b11: Reserved<br>This should be set before using SATA. |

**PHP_GRF_GMAC_CON0**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11:9 | RW | 0x0 | gmac1_phy_intf_sel<br>PHY Interface Select.<br>3'b000: GMII/MII<br>3'b001: RGMII<br>3'b100: RMII |
| 8 | RW | 0x0 | gmac1_ptp_aux_ts_trig<br>Auxiliary Time Stamp Trigger.<br>This signal is asserted to take an auxiliary snapshot of the time and store it in the auxiliary time stamp FIFO. A rising edge on this port is used to trigger the auxiliary snapshot. |
| 7:6 | RW | 0x0 | gmac1_sbd_flowctrl<br>Sideband Flow Control.<br>When set high, instructs the MAC to transmit Pause frames in Full-duplex mode. In half-duplex mode, the MAC enables the Back-pressure function until this signal is made low again. |
| 5:3 | RW | 0x4 | gmac0_phy_intf_sel<br>PHY Interface Select.<br>3'b000: GMII/MII<br>3'b001: RGMII<br>3'b100: RMII |
| 2 | RW | 0x0 | gmac0_ptp_aux_ts_trig<br>Auxiliary Time Stamp Trigger.<br>This signal is asserted to take an auxiliary snapshot of the time and store it in the auxiliary time stamp FIFO. A rising edge on this port is used to trigger the auxiliary snapshot. |
| 1:0 | RW | 0x0 | gmac0_sbd_flowctrl<br>Sideband Flow Control.<br>When set high, instructs the MAC to transmit Pause frames in Full-duplex mode. In half-duplex mode, the MAC enables the Back-pressure function until this signal is made low again. |

**PHP_GRF_SATA_CON0**

Rockchip Confidencial

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | sata0_txcommonmode_disable<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>TX common mode disable |
| 14 | RW | 0x0 | sata0_exelecidle_disable<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>TX output to electrical idle disable. |
| 13:11 | RW | 0x0 | sata0_txmargin<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>TX_SWING and TX_MARGIN[2:0] are combined together to control TX output amplitude. |
| 10:9 | RW | 0x0 | sata0_txdeemph<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>Transmitter de-emphasis level configuration. |
| 8 | RW | 0x0 | sata0_txswing<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>PHY TX_SWING control<br>When TX_SWING =1, transmitter is in low swing mode, the output amplitude can achieve 500mV,600mV,700mv,800mV,900mV,1000mV,1100mV and 1200mV, the 800mV to 1200mV output has no difference with the cases when TX_SWING =0. |
| 7 | RW | 0x0 | sata0_txoneszeros<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>This signal is used in USB3.0 mode for transmitting compliance pattern CP7 and CP8.<br>When set to high, it causes the transmitter to transmit an alternating sequence of 0s and 1s, regardless the states of TX_DATA.<br>In PCIE and SATA mode, this signal should be tied to low. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | sata0_compliance<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>This signal is used in PCIE mode only; in other application it should be tied to low.<br>TX_COMPLIANCE become high will set the running disparity to negative.<br>The lowest byte of 16bits transmitted data will be the byte that running disparity set to negative.<br>When TX_COMPLIANCE and TX_ELECIDLE are both set to low, PHY IP is power down completely. |
| 5 | RW | 0x1 | sata0_rxtermination<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>Connect/Remove of receiver termination resistor.<br>1'b0: RX termination removed<br>1'b1: RX termination connected<br>This signal is used in USB3.0 mode only, in other application it should be tied to high. |
| 4 | RW | 0x0 | sata0_rxpolarity<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>PHY RX polarity inversion control.<br>When this signal set to high, it instructs a polarity inversion in RX_DATA.<br>RX_POLAR applies to USB3.0 and PCIE mode only, in SATA mode it should be tied to low. |
| 3 | RW | 0x0 | sata0_rxeqtrain<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>RX EQ training mode enable signal:<br>This signal is used to instruct the receiver to bypass normal operation and perform equalization training. This signal is used in USB3.0 mode only, should be set to low in any other application. |
| 2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | sata0_encodedecodebypass<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>Controls whether the PHY performs 8b/10b encode and decode.<br>1'b0: 8b/10b encode/decode performed normally by the PHY.<br>1'b1: 8b/10b encode/decode bypassed, 20bit 8b/10b encode/decode bypass mode works only when BUS_WIDTH=2b01. |
| 0 | RW | 0x0 | sata0_elasbuffermode<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>1'b0: Nominal half-full buffer mode<br>1'b1: Nominal empty buffer mode |

Rockchip Confidential

**PHP_GRF_SATA_CON1**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | sata1_txcommonmode_disable<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>TX common mode disable |
| 14 | RW | 0x0 | sata1_exelecidle_disable<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>TX output to electrical idle disable. |
| 13:11 | RW | 0x0 | sata1_txmargin<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>TX_SWING and TX_MARGIN[2:0] are combined together to control TX output amplitude. |
| 10:9 | RW | 0x0 | sata1_txdeemph<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>Transmitter de-emphasis level configuration. |
| 8 | RW | 0x0 | sata1_txswing<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>PHY TX_SWING control<br>When TX_SWING =1, transmitter is in low swing mode, the output amplitude can achieve 500mV,600mV,700mv,800mV,900mV,1000mV,1100mV and 1200mV, the 800mV to 1200mV output has no difference with the cases when TX_SWING =0. |
| 7 | RW | 0x0 | sata1_txoneszeros<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>This signal is used in USB3.0 mode for transmitting compliance pattern CP7 and CP8.<br>When set to high, it causes the transmitter to transmit an alternating sequence of 0s and 1s, regardless the states of TX_DATA.<br>In PCIE and SATA mode, this signal should be tied to low. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | sata1_compliance<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>This signal is used in PCIE mode only; in other application it should be tied to low.<br>TX_COMPLIANCE become high will set the running disparity to negative.<br>The lowest byte of 16bits transmitted data will be the byte that running disparity set to negative.<br>When TX_COMPLIANCE and TX_ELECIDLE are both set to low, PHY IP is power down completely. |
| 5 | RW | 0x1 | sata1_rxtermination<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>Connect/Remove of receiver termination resistor.<br>1'b0: RX termination removed<br>1'b1: RX termination connected<br>This signal is used in USB3.0 mode only, in other application it should be tied to high. |
| 4 | RW | 0x0 | sata1_rxpolarity<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>PHY RX polarity inversion control.<br>When this signal set to high, it instructs a polarity inversion in RX_DATA.<br>RX_POLAR applies to USB3.0 and PCIE mode only, in SATA mode it should be tied to low. |
| 3 | RW | 0x0 | sata1_rxeqtrain<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>RX EQ training mode enable signal:<br>This signal is used to instruct the receiver to bypass normal operation and perform equalization training. This signal is used in USB3.0 mode only, should be set to low in any other application. |
| 2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | sata1_encodedecodebypass<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>Controls whether the PHY performs 8b/10b encode and decode.<br>1'b0: 8b/10b encode/decode performed normally by the PHY.<br>1'b1: 8b/10b encode/decode bypassed, 20bit 8b/10b encode/decode bypass mode works only when BUS_WIDTH=2b01. |
| 0 | RW | 0x0 | sata1_elasbuffermode<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>1'b0: Nominal half-full buffer mode<br>1'b1: Nominal empty buffer mode |

Rockchip Confidential

**PHP_GRF_SATA_CON2**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | sata2_txcommonmode_disable<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>TX common mode disable. |
| 14 | RW | 0x0 | sata2_exelecidle_disable<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>TX output to electrical idle disable. |
| 13:11 | RW | 0x0 | sata2_txmargin<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>TX_SWING and TX_MARGIN[2:0] are combined together to control TX output amplitude. |
| 10:9 | RW | 0x0 | sata2_txdeemph<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>Transmitter de-emphasis level configuration. |
| 8 | RW | 0x0 | sata2_txswing<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>PHY TX_SWING control<br>When TX_SWING =1, transmitter is in low swing mode, the output amplitude can achieve 500mV,600mV,700mv,800mV,900mV,1000mV,1100mV and 1200mV, the 800mV to 1200mV output has no difference with the cases when TX_SWING =0. |
| 7 | RW | 0x0 | sata2_txoneszeros<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>This signal is used in USB3.0 mode for transmitting compliance pattern CP7 and CP8.<br>When set to high, it causes the transmitter to transmit an alternating sequence of 0s and 1s, regardless the states of TX_DATA.<br>In PCIE and SATA mode, this signal should be tied to low. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | sata2_compliance<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>This signal is used in PCIE mode only; in other application it should be tied to low.<br>TX_COMPLIANCE become high will set the running disparity to negative.<br>The lowest byte of 16bits transmitted data will be the byte that running disparity set to negative.<br>When TX_COMPLIANCE and TX_ELECIDLE are both set to low, PHY IP is power down completely. |
| 5 | RW | 0x1 | sata2_rxtermination<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>Connect/Remove of receiver termination resistor.<br>1'b0: RX termination removed<br>1'b1: RX termination connected<br>This signal is used in USB3.0 mode only, in other application it should be tied to high. |
| 4 | RW | 0x0 | sata2_rxpolarity<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>PHY RX polarity inversion control.<br>When this signal set to high, it instructs a polarity inversion in RX_DATA.<br>RX_POLAR applies to USB3.0 and PCIE mode only, in SATA mode it should be tied to low. |
| 3 | RW | 0x0 | sata2_rxeqtrain<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>RX EQ training mode enable signal:<br>This signal is used to instruct the receiver to bypass normal operation and perform equalization training. This signal is used in USB3.0 mode only, should be set to low in any other application. |
| 2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | sata2_encodedecodebypass<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>Controls whether the PHY performs 8b/10b encode and decode.<br>1'b0: 8b/10b encode/decode performed normally by the PHY.<br>1'b1: 8b/10b encode/decode bypassed, 20bit 8b/10b encode/decode bypass mode works only when BUS_WIDTH=2b01. |
| 0 | RW | 0x0 | sata2_elasbuffermode<br>This is redundancy design used to control PHY pipe interface as supplement for controller. From PHY interface, this is form controller. More setting please refer to PHY GRF section.<br>1'b0: Nominal half-full buffer mode<br>1'b1: Nominal empty buffer mode |

Rockchip Confidential

**PHP_GRF_PHP_MMU_CON0**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | php_mmu600_tcu_pmusnapshot_req<br>PMU snapshot request. The PMU snapshot occurs on the rising edge of pmusnapshot_req. |
| 9:6 | RW | 0x0 | php_mmu600_tcu_ecorevnum<br>Tie this signal to 0 for normal use. |
| 5:3 | RW | 0x5 | php_mmu600_tcu_sup_oas<br>Output address size supported.<br>The encodings for this input are:<br>3'b000 32 bits.<br>3'b001 36 bits.<br>3'b010 40 bits.<br>3'b011 42 bits.<br>3'b100 44 bits.<br>3'b101 48 bits.<br>You must not use other encodings, including 3'b110 defines to indicate 52-bit addresses. They are treated as 3'b101. |
| 2 | RW | 0x0 | php_mmu600_tcu_sup_sev<br>This signal indicates whether the Send Event mechanism is supported. Tie HIGH when evento is connected. |
| 1 | RW | 0x0 | php_mmu600_tcu_sup_btm<br>This signal indicates whether the Broadcast TLB Maintenance is supported. Tie HIGH when the TCU is connected to an interconnect that supports DVM. |
| 0 | RO | 0x0 | reserved |

**PHP_GRF_PHP_MMU_CON1**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10:7 | RW | 0x0 | php_mmu600_tbu_0_ecorevnum<br>Tie this signal to 0 for normal use. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | php_mmu600_tbu_0_utlb_roundrobin<br>Defines the Micro TLB entry replacement policy.<br>When LOW, the Micro TLB uses a Pseudo Least Recently Used (PLRU) replacement policy. This policy typically provides the best average performance. However, when multiple translations are prefetched using a StashTranslation transaction, they might evict each other.<br>When HIGH, the Micro TLB uses a round-robin replacement policy. With this policy, you can prefetch multiple translations using a StashTranslation transaction without evictions occurring, as long as the Micro TLB size is not exceeded.<br>Tie this signal HIGH if a real-time upstream master prefetches translations and you want to avoid transactions evicting each other.<br>Otherwise, tie this signal LOW. |
| 5:2 | RW | 0x3 | php_mmu600_tbu_0_max_tok_trans<br>Indicates the number of DTI translation tokens to request when connecting to the TCU, minus 1. |
| 1 | RW | 0x0 | php_mmu600_tbu_0_cmo_disable<br>Tie this signal HIGH to disable cache maintenance operations. When this signal is HIGH, the following transactions are always aborted with an SLVERR response:<br>CleanInvalid.<br>CleanShared.<br>CleanSharedPersist.<br>MakeInvalid.<br>Cache maintenance operations can sometimes break the requirements of limited sideband channel communication, such as when a master component accesses protected content. You can disable cache maintenance operations in such cases. Cache maintenance operations are always disabled for ACE interfaces. This signal is therefore not present when the connected interface is configured as an ACE interface. |
| 0 | RW | 0x0 | php_mmu600_tbu_0_pmusnapshot_req<br>PMU snapshot request. The PMU snapshot occurs on the rising edge of pmusnapshot_req. |

**PHP_GRF_PHP_MMU_CON2**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RW | 0x00 | php_mmu600_tbu_0_s_sid_high<br>Provides the high-order StreamID bits for all transactions with a Secure StreamID that pass through the TBU. |
| 7:0 | RW | 0x00 | php_mmu600_tbu_0_ns_sid_high<br>Provides the high-order StreamID bits for all transactions with a Non-secure StreamID that pass through the TBU. |

**PHP_GRF_ITS_TADDR0**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:19 | RO | 0x0000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 18:0 | RW | 0x0fe65 | grf_its_targer_address0<br>Modifies the address map to ensure only writes to the correct location trigger MSI requests. Only present when the bypass switch is configured.<br>Specifies the 64K page address that includes the GITS_TRANSLATER register address, and is matched against axaddr[ADDR_WIDTH-1:16]. |

**PHP_GRF_ITS_TADDR1**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:19 | RO | 0x0000 | reserved |
| 18:0 | RW | 0x0fe67 | grf_its_targer_address1<br>Modifies the address map to ensure only writes to the correct location trigger MSI requests. Only present when the bypass switch is configured.<br>Specifies the 64K page address that includes the GITS_TRANSLATER register address, and is matched against axaddr[ADDR_WIDTH-1:16]. |

**PHP_GRF_PCIE_MMU_PCIEMODE**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x1 | pcie_mmu_tbu1_pcie_mode<br>You must tie this signal HIGH when the TBU is connected to a PCIe interface.<br>When this signal is HIGH, the TBU behaves as if the PCIe 'No Snoop' property is applied to transactions downstream of the SMMU, as long as the PCIe interface outputs transactions with the following AXI memory types:<br>1. Normal Non-Cacheable Bufferable, when 'No Snoop' is set for the transaction.<br>2. Write-Back, when 'No Snoop' is not set for the transaction.<br>This TBU behaviour is a requirement of the Arm Server Base System Architecture.<br>If this signal is HIGH, the attributes of TBS interface transactions are always combined with the translation attributes, even if stage 1 translation is enabled. That is, the transaction attributes are always calculated as if the DTI_TBU_TRANS_RESP.STRW field is EL1-<br>S2, regardless of the actual STRW value.<br>If this signal is HIGH, the input attribute and shareability override information in the ATTR_OVR field of the DTI_TBU_TRANS_RESP message is ignored. For SMMUv3, PCIe masters do not support this feature. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x1 | pcie_mmu_tbu0_pcie_mode<br>You must tie this signal HIGH when the TBU is connected to a PCIe interface.<br>When this signal is HIGH, the TBU behaves as if the PCIe 'No Snoop' property is applied to transactions downstream of the SMMU, as long as the PCIe interface outputs transactions with the following AXI memory types:<br>1. Normal Non-Cacheable Bufferable, when 'No Snoop' is set for the transaction.<br>2. Write-Back, when 'No Snoop' is not set for the transaction.<br>This TBU behaviour is a requirement of the Arm Server Base System Architecture.<br>If this signal is HIGH, the attributes of TBS interface transactions are always combined with the translation attributes, even if stage 1 translation is enabled. That is, the transaction attributes are always calculated as if the DTI_TBU_TRANS_RESP.STRW field is EL1-<br>S2, regardless of the actual STRW value.<br>If this signal is HIGH, the input attribute and shareability override information in the ATTR_OVR field of the DTI_TBU_TRANS_RESP message is ignored. For SMMUv3, PCIe masters do not support this feature. |

**PHP_GRF_PCIE_MMU_CON0**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | pcie_mmu600_tcu_pmusnapshot_req<br>PMU snapshot request. The PMU snapshot occurs on the rising edge of pmusnapshot_req. |
| 9:6 | RW | 0x0 | pcie_mmu600_tcu_ecorevnum<br>Tie this signal to 0 unless directed otherwise by Arm. |
| 5:3 | RW | 0x5 | pcie_mmu600_tcu_sup_oas<br>Output address size supported.<br>The encodings for this input are:<br>3'b000 32 bits.<br>3'b001 36 bits.<br>3'b010 40 bits.<br>3'b011 42 bits.<br>3'b100 44 bits.<br>3'b101 48 bits.<br>You must not use other encodings, including 3'b110 that SMMUv3.1 defines to indicate 52-bit addresses. They are treated as 3'b101 |
| 2 | RW | 0x0 | pcie_mmu600_tcu_sup_sev<br>This signal indicates whether the Send Event mechanism is supported. Tie HIGH when evento is connected. |
| 1 | RW | 0x0 | pcie_mmu600_tcu_sup_btm<br>This signal indicates whether the Broadcast TLB Maintenance is supported. Tie HIGH when the TCU is connected to an interconnect that supports DVM |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | pcie_mmu600_tcu_sup_cohacc<br>This signal indicates whether the QTW interface is I/O-coherent.<br>Tie HIGH when the TCU is connected to a coherent interconnect. |

**PHP_GRF_PCIE_MMU_CON1**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10:7 | RW | 0x0 | pcie_mmu600_tbu_0_ecorevnum<br>Tie this signal to for normal use. |
| 6 | RW | 0x0 | pcie_mmu600_tbu_0_utlb_roundrobin<br>Defines the Micro TLB entry replacement policy.<br>When LOW, the Micro TLB uses a Pseudo Least Recently Used (PLRU) replacement policy. This policy typically provides the best average performance. However, when multiple translations are prefetched using a StashTranslation transaction, they might evict each other.<br>When HIGH, the Micro TLB uses a round-robin replacement policy. With this policy, you can prefetch multiple translations using a StashTranslation transaction without evictions occurring, as long as the Micro TLB size is not exceeded.<br>Tie this signal HIGH if a real-time upstream master prefetches translations and you want to avoid transactions evicting each other.<br>Otherwise, tie this signal LOW. |
| 5:2 | RW | 0x7 | pcie_mmu600_tbu_0_max_tok_trans<br>Indicates the number of DTI translation tokens to request when connecting to the TCU, minus 1. |
| 1 | RW | 0x0 | pcie_mmu600_tbu_0_cmo_disable<br>Tie this signal HIGH to disable cache maintenance operations.<br>When this signal is HIGH, the following transactions are always aborted with an SLVERR response:<br>CleanInvalid.<br>CleanShared.<br>CleanSharedPersist.<br>MakeInvalid.<br>Cache maintenance operations can sometimes break the requirements of limited sideband channel communication, such as when a master component accesses protected content. You can disable cache maintenance operations in such cases. Cache maintenance operations are always disabled for ACE interfaces. This signal is therefore not present when the connected interface is configured as an ACE interface. |
| 0 | RW | 0x0 | pcie_mmu600_tbu_0_pmusnapshot_req<br>PMU snapshot request. The PMU snapshot occurs on the rising edge of pmusnapshot_req |

**PHP_GRF_PCIE_MMU_CON2**

Address: Operational Base + offset (0x003C)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10:7 | RW | 0x0 | pcie_mmu600_tbu_1_ecorevnum<br>Tie this signal to 0 unless directed otherwise by Arm. |
| 6 | RW | 0x0 | pcie_mmu600_tbu_1_utlb_roundrobin<br>Defines the Micro TLB entry replacement policy.<br>When LOW, the Micro TLB uses a Pseudo Least Recently Used (PLRU) replacement policy. This policy typically provides the best average performance. However, when multiple translations are prefetched using a StashTranslation transaction, they might evict each other.<br>When HIGH, the Micro TLB uses a round-robin replacement policy. With this policy, you can prefetch multiple translations using a StashTranslation transaction without evictions occurring, as long as the Micro TLB size is not exceeded.<br>Tie this signal HIGH if a real-time upstream master prefetches translations and you want to avoid transactions evicting each other.<br>Otherwise, tie this signal LOW. |
| 5:2 | RW | 0x7 | pcie_mmu600_tbu_1_max_tok_trans<br>Indicates the number of DTI translation tokens to request when connecting to the TCU, minus 1. |
| 1 | RW | 0x0 | pcie_mmu600_tbu_1_cmo_disable<br>Tie this signal HIGH to disable cache maintenance operations.<br>When this signal is HIGH, the following transactions are always aborted with an SLVERR response:<br>CleanInvalid.<br>CleanShared.<br>CleanSharedPersist.<br>MakeInvalid.<br>Cache maintenance operations can sometimes break the requirements of limited sideband channel communication, such as when a master component accesses protected content. You can disable cache maintenance operations in such cases. Cache maintenance operations are always disabled for ACE interfaces. This signal is therefore not present when the connected interface is configured as an ACE interface. |
| 0 | RW | 0x0 | pcie_mmu600_tbu_1_pmusnapshot_req<br>PMU snapshot request. The PMU snapshot occurs on the rising edge of pmusnapshot_req |

**PHP_MEM_CON0**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:0 | RW | 0x110010 | mem_cfg_hsdprf<br>bit 0: TEST1A<br>bit 1: TEST_RNMA<br>bit 5~2: RMA<br>bit 6: WMDA<br>bit 8: LS<br>bit 14~13: RA<br>bit 17: TEST1B<br>bit 21~18: RMB |

**PHP_GRF_PHP_ST0**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4 | RO | 0x0 | gmac0_mcgr_dma_req_intr<br>MCGR DMA Read Request<br>Used to Request a Target Presentation time value for one of the comparator modules when the instance is running in recovery mode. In Media Clock generation mode, this I/O signal is held high indicating a valid Presentation time is captured and updated in MAC_PPS(i)_Target_Time_Seconds register. One or more DMA read requests can simultaneously active, it is up to the DMA logic to maintain priority. Bits have a 1-1 correspondence to the comparator instances<br>(i.e. Bit-0 belongs to comparator 0, bit-1 belongs to comparator-1 and so on). Once set, will hold high and will be reset the cycle after receiving the mcgr_dma_ack for that comparator. Width of this IO changes with the configured number of PPS instances. |
| 3:2 | RO | 0x0 | gmac0_speed<br>Mac Speed indication/status.<br>2'b00:1000Mbps (GMII)<br>2'b01: 2500Mbps (GMII)<br>2'b10: 10Mbps (MII)<br>2'b11: 100Mbps (MII) |
| 1 | RO | 0x0 | gmac0_ptp_pps<br>Pulse Per Second.<br>This signal is high based on the PPS mode selected in the MAC_PPS_Control register. When PPS is programmed in Media Clock recovery Mode, this port indicates the recovered clock. |
| 0 | RO | 0x0 | gmac0_sdb_tx_clk_gating_ctrl<br>LPI Tx Clock Gating Control.<br>This signal is high after the MAC enters the Tx LPI (low power idle) mode. You can use this signal to control the Tx clock gating. |

**PHP_GRF_PHP_ST1**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | gmac0_ptp_timestamp0<br>GMAC0 ptp timestamp[31:0]<br>Reference Time Output.<br>This bus provides the System Time output when it is generated internally. |

**PHP_GRF_PHP_ST2**

Address: Operational Base + offset (0x004C)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | gmac0_ptp_timestamp1<br>GMAC0 ptp timestamp[63:32]<br>Reference Time Output.<br>This bus provides the System Time output when it is generated internally. |

**PHP_GRF_PHP_ST3**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | gmac1_ptp_timestamp0<br>GMAC1 ptp timestamp[31:0]<br>Reference Time Output.<br>This bus provides the System Time output when it is generated internally. |

**PHP_GRF_PHP_ST4**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | gmac1_ptp_timestamp1<br>GMAC1 ptp timestamp[63:32]<br>Reference Time Output.<br>This bus provides the System Time output when it is generated internally. |

**PHP_GRF_MMU_PMU_ACK**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4 | RO | 0x0 | pcie_mmu_tbu1_pmusnapshot_ack<br>PMU snapshot acknowledge. The TBU uses this signal to acknowledge that the PMU snapshot has occurred.<br>This signal is LOW after reset. |
| 3 | RO | 0x0 | pcie_mmu_tbu0_pmusnapshot_ack<br>PMU snapshot acknowledge. The TBU uses this signal to acknowledge that the PMU snapshot has occurred.<br>This signal is LOW after reset. |
| 2 | RO | 0x0 | pcie_mmu_tcu_pmusnapshot_ack<br>PMU snapshot acknowledge. The TCU uses this signal to acknowledge that the PMU snapshot has occurred.<br>This signal is LOW after reset. |
| 1 | RO | 0x0 | php_mmu_tbu_pmusnapshot_ack<br>PMU snapshot acknowledge. The TBU uses this signal to acknowledge that the PMU snapshot has occurred.<br>This signal is LOW after reset. |
| 0 | RO | 0x0 | php_mmu_tcu_pmusnapshot_ack<br>PMU snapshot acknowledge. The TCU uses this signal to acknowledge that the PMU snapshot has occurred.<br>This signal is LOW after reset. |

**PHP_GRF_PCIE_MMU_CON6**

Address: Operational Base + offset (0x005C)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RW | 0x00 | pcie_mmu_tbu0_s_sid<br>Provides the high-order StreamID bits for all transactions with a Secure StreamID that pass through the TBU. |
| 7:0 | RW | 0x00 | pcie_mmu_tbu0_ns_sid<br>Provides the high-order StreamID bits for all transactions with a Non-secure StreamID that pass through the TBU |

**PHP_GRF_PCIE_MMU_CON7**

Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RW | 0x00 | pcie_mmu_tbu1_s_sid<br>Provides the high-order StreamID bits for all transactions with a Secure StreamID that pass through the TBU. |
| 7:0 | RW | 0x00 | pcie_mmu_tbu1_ns_sid<br>Provides the high-order StreamID bits for all transactions with a Non-secure StreamID that pass through the TBU. |

**PHP_GRF_MEM_CON5**

Address: Operational Base + offset (0x0064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16:0 | RW | 0x08010 | mem_cfg_uhddprf<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMDA<br>bit 7: LS<br>bit 16: TESTRWM |

**PHP_GRF_MEM_CON10**

Address: Operational Base + offset (0x0068)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x1410 | mem_cfg_hdsprf<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMD<br>bit 7: LS<br>bit 11~10: WPULSE<br>bit 13~12: RA |

**PHP_GRF_CLK_CON1**

Address: Operational Base + offset (0x0070)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | io_clksel_gmac1<br>GMAC1 tx clock select control.<br>1'b1: Select clock form cru.<br>1'b0: Select clock form io. |
| 8:7 | RW | 0x0 | mii_tx_clk_sel_gamc1<br>GMAC1 controller clock tx division select.<br>In RMII mode:<br>2'b0: 25Mhz<br>2'b1: 2.5Mhz<br>In RGMII mode:<br>2'b10: 2.5Mhz<br>2'b11: 25Mhz<br>other: 125Mhz |
| 6 | RW | 0x0 | rmii_gate_en_gamc1<br>Clock gate enable for RMII clock.<br>1'b1: Gate RMII clk.<br>1'b0: Not gate RMII clk.<br>This bit will gate RMII clk no matter if RMII mode set. |
| 5 | RW | 0x0 | rmii_mode_gmac1<br>GMAC1 RMII/RGMII mode control.<br>1'b1: RMII mode.<br>1'b0: RGMII mode. |
| 4 | RW | 0x0 | io_clksel_gmac0<br>GMAC0 tx clock select control.<br>1'b1: Select clock form cru.<br>1'b0: Select clock form io. |
| 3:2 | RW | 0x0 | mii_tx_clk_sel_gamc0<br>GMAC0 controller clock tx division select.<br>In RMII mode:<br>2'b0: 25Mhz<br>2'b1: 2.5Mhz<br>In RGMII mode:<br>2'b10: 2.5Mhz<br>2'b11: 25Mhz<br>other: 125Mhz |
| 1 | RW | 0x0 | rmii_gate_en_gamc0<br>Clock gate enable for RMII clock.<br>1'b1: Gate RMII clk.<br>1'b0: Not gate RMII clk.<br>This bit will gate RMII clk no matter if RMII mode set. |
| 0 | RW | 0x0 | rmii_mode_gmac0<br>GMAC0 RMII/RGMII mode control.<br>1'b1: RMII mode.<br>1'b0: RGMII mode. |

**PHP_GRF_GMAC0_SID_AW**

Address: Operational Base + offset (0x0074)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17 | RW | 0x0 | gmac0_aw_atst<br>GAMC0 aw atst for MMU.<br>This is used for PHP MMU. |
| 16 | RW | 0x0 | gmac0_aw_ssdiv<br>GAMC0 aw ssdiv for MMU.<br>This is used for PHP MMU. |
| 15:0 | RW | 0x0000 | gmac0_aw_sid<br>GAMC0 aw sid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_GMAC0_SSID_AW**

Address: Operational Base + offset (0x0078)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | gmac0_aw_ssid<br>GMAC0 aw ssid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_GMAC1_SID_AW**

Address: Operational Base + offset (0x007C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17 | RW | 0x0 | gmac1_aw_atst<br>GMAC1 aw atst for MMU.<br>This is used for PHP MMU. |
| 16 | RW | 0x0 | gmac1_aw_ssdiv<br>GMAC1 aw ssdiv for MMU.<br>This is used for PHP MMU. |
| 15:0 | RO | 0x0000 | reserved |

**PHP_GRF_GMAC1_SSID_AW**

Address: Operational Base + offset (0x0080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | gmac1_aw_ssid<br>GMAC1 aw ssid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_SATA0_SID_AW**

Address: Operational Base + offset (0x0084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17 | RW | 0x0 | sata0_aw_atst<br>SATA0 aw atst for MMU.<br>This is used for PHP MMU. |
| 16 | RW | 0x0 | sata0_aw_ssdiv<br>SATA0 aw ssdiv for MMU.<br>This is used for PHP MMU. |
| 15:0 | RW | 0x0000 | sata0_aw_sid<br>SATA0 aw sid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_SATA0_SSID_AW**

Address: Operational Base + offset (0x0088)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sata0_aw_ssid<br>SATA0 aw ssid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_SATA1_SID_AW**

Address: Operational Base + offset (0x008C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17 | RW | 0x0 | sata1_aw_atst<br>SATA1 aw atst for MMU.<br>This is used for PHP MMU. |
| 16 | RW | 0x0 | sata1_aw_ssdiv<br>SATA1 aw ssdiv for MMU.<br>This is used for PHP MMU. |
| 15:0 | RW | 0x0000 | sata1_aw_sid<br>SATA0 aw sid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_SATA1_SSID_AW**

Address: Operational Base + offset (0x0090)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sata1_aw_ssid<br>SATA1 aw ssid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_SATA2_SID_AW**

Address: Operational Base + offset (0x0094)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17 | RW | 0x0 | sata2_aw_atst<br>SATA2 aw atst for MMU.<br>This is used for PHP MMU. |
| 16 | RW | 0x0 | sata2_aw_ssdiv<br>SATA2 aw ssdiv for MMU.<br>This is used for PHP MMU. |
| 15:0 | RW | 0x0000 | sata2_aw_sid<br>SATA2 aw sid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_SATA2_SSID_AW**

Address: Operational Base + offset (0x0098)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sata2_aw_ssid<br>SATA2 aw ssid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_GMAC0_SID_AR**

Address: Operational Base + offset (0x009C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17 | RW | 0x0 | gmac0_ar_atst<br>GMAC0 ar atst for MMU.<br>This is used for PHP MMU. |
| 16 | RO | 0x0 | reserved |
| 15:0 | RW | 0x0000 | gmac0_ar_sid<br>GMAC0 ar sid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_GMAC0_SSID_AR**

Address: Operational Base + offset (0x00A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | gmac0_ar_ssid<br>GMAC0 ar ssid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_GMAC1_SID_AR**

Address: Operational Base + offset (0x00A4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17 | RW | 0x0 | gmac1_ar_atst<br>GMAC1 ar atst for MMU.<br>This is used for PHP MMU. |
| 16 | RW | 0x0 | gmac1_ar_ssdiv<br>GMAC1 ar ssdiv for MMU.<br>This is used for PHP MMU. |
| 15:0 | RW | 0x0000 | gmac1_ar_sid<br>GMAC1 ar sid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_GMAC1_SSID_AR**

Address: Operational Base + offset (0x00A8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | gmac1_ar_ssid<br>GMAC1 ar ssid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_SATA0_SID_AR**

Address: Operational Base + offset (0x00AC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17 | RW | 0x0 | sata0_ar_atst<br>SATA0 ar atst for MMU.<br>This is used for PHP MMU. |
| 16 | RW | 0x0 | sata0_ar_ssdiv<br>SATA0 ar ssdiv for MMU.<br>This is used for PHP MMU. |
| 15:0 | RW | 0x0000 | sata0_ar_sid<br>SATA0 ar sid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_SATA0_SSID_AR**

Address: Operational Base + offset (0x00B0)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sata0_ar_ssid<br>SATA0 ar ssid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_SATA1_SID_AR**

Address: Operational Base + offset (0x00B4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17 | RW | 0x0 | sata1_ar_atst<br>SATA1 ar atst for MMU.<br>This is used for PHP MMU. |
| 16 | RW | 0x0 | sata1_ar_ssdiv<br>SATA1 ar ssdiv for MMU.<br>This is used for PHP MMU. |
| 15:0 | RW | 0x0000 | sata1_ar_sid<br>SATA1 ar sid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_SATA1_SSID_AR**

Address: Operational Base + offset (0x00B8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sata1_ar_ssid<br>SATA1 ar ssid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_SATA2_SID_AR**

Address: Operational Base + offset (0x00BC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17 | RW | 0x0 | sata2_ar_atst<br>SATA2 ar atst for MMU.<br>This is used for PHP MMU. |
| 16 | RO | 0x0 | reserved |
| 15:0 | RW | 0x0000 | sata2_ar_sid<br>SATA2 ar sid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_SATA2_SSID_AR**

Address: Operational Base + offset (0x00C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sata2_ar_ssid<br>SATA2 ar ssid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_USB3OTG_2_SID_AR**

Address: Operational Base + offset (0x00C4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17 | RW | 0x0 | usb3otg_2_ar_atst<br>USB3OTG_2 ar atst for MMU.<br>This is used for PHP MMU. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 16 | RW | 0x0 | usb3otg_2_ar_ssdiv<br>USB3OTG_2 ar ssdiv for MMU.<br>This is used for PHP MMU. |
| 15:0 | RW | 0x0000 | usb3otg_2_ar_sid<br>USB3OTG_2 ar sid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_USB3OTG_2_SSID_AR**

Address: Operational Base + offset (0x00C8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | usb3otg_2_ar_ssid<br>USB3OTG_2 ar ssid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_USB3OTG_2_SID_AW**

Address: Operational Base + offset (0x00CC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17 | RW | 0x0 | usb3otg_2_aw_atst<br>USB3OTG_2 aw atst for MMU.<br>This is used for PHP MMU. |
| 16 | RW | 0x0 | usb3otg_2_aw_ssdiv<br>USB3OTG_2 aw ssdiv for MMU.<br>This is used for PHP MMU. |
| 15:0 | RW | 0x0000 | usb3otg_2_aw_sid<br>USB3OTG_2 aw sid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_USB3OTG_2_SSID_AW**

Address: Operational Base + offset (0x00D0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | usb3otg_2_aw_ssid<br>USB3OTG_2 aw ssid for MMU.<br>This is used for PHP MMU. |

**PHP_GRF_GMAC_CON_PST**

Address: Operational Base + offset (0x00D4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | mcg_pst_trig_sel_gmac1<br>Select mcg_pst_trig from IO or GRF (mcg_pst_trig_gmac1).<br>1'b1: From IO.<br>1'b0: From GRF. |
| 2 | RW | 0x0 | mcg_pst_trig_gmac1<br>Grf control GMAC1 media clock generation tigger input. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | mcg_pst_trig_sel_gmac0<br>Select mcg_pst_trig from IO or GRF (mcg_pst_trig_gmac0).<br>1'b1: From IO.<br>1'b0: From GRF. |
| 0 | RW | 0x0 | mcg_pst_trig_gmac0<br>Grf control GMAC0 media clock generation tigger input. |

**PHP_GRF_GMAC0_CMD**

Address: Operational Base + offset (0x00D8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | gmac0_mcgr_dma_ack_cmd<br>If write this be written to 1, a pulse will be set to GMAC0. |

**PHP_GRF_GMAC1_CMD**

Address: Operational Base + offset (0x00DC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | gmac1_mcgr_dma_ack_cmd<br>If write this be written to 1, a pulse will be set to GMAC1. |

**PHP_GRF_MEM_CON11**

Address: Operational Base + offset (0x00E0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x1410 | mem_cfg_hdspra<br>bit 0: TEST1<br>bit 1: TEST_RNM<br>bit 4~2: RM<br>bit 5: WMD<br>bit 7: LS<br>bit 11~10: WPULSE<br>bit 13~12: RA |

**PHP_GRF_USB3OTG_2_CON0**

Address: Operational Base + offset (0x00E4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | usb3otg_host_u2_port_disable<br>USB2.0 Port Disable control.<br>1'b0: Port Enabled<br>1'b1: Port Disabled When 1, this signal stops reporting connect/disconnect events the port and keeps the port in disabled state |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14 | RW | 0x0 | usb3otg_host_port_power_control_present<br>This indicates whether the host controller implementation includes port power control.<br>1'b0: Indicates that the port does not have port power switches<br>1'b1: Indicates that the port has port power switches |
| 13:8 | RW | 0x20 | usb3otg_fladj_30mhz_reg<br>HS Jitter Adjustment. Indicates the correction required to accommodate mac3 clock and utmi clock jitter to measure 125 's duration.<br>With fladj_30mhz_reg tied to zero, the high speed 125us micro-frame is counted for 123933ns. You must program the value in terms of high speed bit times in a 30 MHz cycle. The default value that must be driven is 32 (assuming 30 MHz perfect clock).<br>Fladj_30mhz_reg connects to the FLADJ register defined in the xHCI spec in the PCI configuration space. Each count is equal to 16 high speed bit times. By default, when this register is set to 32, it gives a 125us interval.<br>Now, based the clock accuracy you can decrement the count or increment the count to get the 125 us uSOF window. For non-PCI systems, it is recommended that this strap is connected to a register that can be controlled by software. This strap is used in device mode also. If device only mode is implemented, it is recommended to tie this input to 'd32. |
| 7:6 | RW | 0x0 | usb3otg_hub_port_perm_attach<br>Indicates if the device attached to a downstream port is permanently attached or not.<br>1'b0: Not permanently attached<br>1'b1: Permanently attached<br>Bit0 is for USB2.0 port and bit1 are for USB 3.0 SS port |
| 5:4 | RW | 0x0 | usb3otg_hub_port_overcurrent<br>This is the per port Overcurrent indication of the root-hub ports:<br>1'b0: No Overcurrent<br>1'b1: Overcurrent<br>Bit0 is for USB 2.0 port and bit1 are for USB 3.0 SS port |
| 3:0 | RW | 0x0 | usb3otg_bus_filter_bypass<br>It is expected that this signal is set or reset at power-on reset and is not changed during the normal<br>operation of the core. The function of each bit is:<br>bus_filter_bypass[3]: Bypass the filter for utmiotg_iddig<br>bus_filter_bypass[2]: Bypass the filters for utmisrp_bvalid and utmisrp_sessend<br>bus_filter_bypass[1]: Bypass the filter for pipe3_PowerPresent all U3 ports<br>bus_filter_bypass[0]: Bypass the filter for utmiotg_vbusvalid all U2 ports<br>In non-OTG Host-only mode, internal bus filters are not needed.<br>Values:<br>1'b0: Bus filter(s) enabled<br>1'b1: Bus filter(s) disabled (bypassed) |

**PHP_GRF_USB3OTG_2_CON1**

Address: Operational Base + offset (0x00E8)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12 | RW | 0x1 | usb3otg1_host_num_u3_port<br>xHCI usb3 port number, default as 1 |
| 11:8 | RW | 0x1 | usb3otg1_host_num_u2_port<br>xHCI host USB2 Port number, default as 1 |
| 7 | RW | 0x0 | usb3otg1_pipe_clk_sel<br>usb3otg1_pipe3_rx_pclk/tx_pclk input source clk select<br>1'b0: Select clk_usb3otg0_pipe for source clk<br>1'b1: Select clk_usb3otg0_utmi for source clk |
| 6 | RO | 0x0 | reserved |
| 5 | RW | 0x0 | usb3otg1_host_legacy_smi_bar<br>Use this register to support SMI on BAR defined in xHCI spec.<br>SW must set this register, then clear this register to indicate Base Address Register written |
| 4 | RW | 0x0 | usb3otg1_host_legacy_smi_pci_cmd<br>Use this register to support SMI on PCI Command defined in xHCI spec.<br>SW must set this register, then clear this register to indicate PCI command register written. |
| 3:2 | RW | 0x0 | usb3otg1_pipe_rate<br>Not used. |
| 1 | RW | 0x0 | usb3otg1_pme_en<br>Enable signal for the pme_generation. Enable the core to assert pme_generation. |
| 0 | RW | 0x0 | usb3otg1_host_u3_port_disable<br>USB 3.0 SS Port Disable control.<br>1'b0: Port Enabled<br>1'b1: Port Disabled |

**PHP_GRF_USB3OTG_2_INTCON**

Address: Operational Base + offset (0x00EC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | usb3_pme_gen_inten<br>1'b0: IRQ disable<br>1'b1: IRQ enable |
| 0 | RW | 0x0 | usb_host_sys_err_en<br>1'b0: IRQ disable<br>1'b1: IRQ enable |

**PHP_GRF_USB3OTG_2_ST_LAT0**

Address: Operational Base + offset (0x00F0)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | usb3otg_logic_analyzer_trace0<br>Usb3otg_logic_analyzer_trace[31:0] bit status.<br>Logic Analyzer Trace. These are internal design signals that you can use for debug purposes. Some of the signals are interface signals like PIPE, UTMI, ULPI, AXI, and AHB, and others are internal state machines and status information signals. During chip bring-up, to debug functional issues, you can probe the interface signals for additional visibility. |

**PHP_GRF_USB3OTG_2_ST_LAT1**

Address: Operational Base + offset (0x00F4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | usb3otg_logic_analyzer_trace0<br>Usb3otg_logic_analyzer_trace[63:32] bit status.<br>Logic Analyzer Trace. These are internal design signals that you can use for debug purposes. Some of the signals are interface signals like PIPE, UTMI, ULPI, AXI, and AHB, and others are internal state machines and status information signals. During chip bring-up, to debug functional issues, you can probe the interface signals for additional visibility. |

**PHP_GRF_USB3OTG_2_ST_CB**

Address: Operational Base + offset (0x00F8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x78e | usb3otg_host_current_belt<br>Usb3otg_host_current_belt[11:0] bit status<br>Current BELT Value.<br>This signal indicates the minimum value of all received BELT values and the BELT that is set by the Set LTV command. This signal is valid only in Host mode. |

**PHP_GRF_USB3OTG_2_ST**

Address: Operational Base + offset (0x00FC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RO | 0x0 | usb3otg_pme_generation<br>PME Generation.<br>This signal is used to generate a PME (Power Management Event). When the Run/Stop bit of the USB Command Register is cleared during USB suspend mode, the core cannot generate an event and cannot assert a regular interrupt. In this case, the core asserts a pme_generation signal to report any wakeup condition if pme_en is high.<br>If the system does not support PCI-like PME interface, then it must not clear the Run/Stop bit during USB suspend mode. In this case, the core generates an event and asserts an interrupt when there is any wakeup event. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RO | 0x0 | usb3otg_host_sys_err<br>Host System Error.<br>This signal indicates that a Host System Error has occurred as reflected in the USBSTS.HSE field. This signal is asserted only if the USBCMD.HSEE field is set to '1'. It can occur when the host controller encounters an 'Error' response in the AHB, the AXI, or the Native Master Bus. When the USBSTS.HSE field is cleared by software, this signal is de-asserted unless the master continues to assert its bus error output. The typical software response to an HSE is to reset the core. For more details, refer to section 4.10.2.6 of the xHCI 1.0 specification. |

**PHP_GRF_PCIESEL_CON**

Address: Operational Base + offset (0x0100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x1 | pcie1l1_sel<br>Select the signal form PHY to PCIe1l1<br>1'b0: Select comb PHY<br>1'b1: Select PCIE3 PHY |
| 0 | RW | 0x1 | pcie1l0_sel<br>Select the signal form PHY to PCIe1l0<br>1'b0: Select comb PHY<br>1'b1: Select PCIE3 PHY |

**PHP_GRF_UTMI_CON**

Address: Operational Base + offset (0x0104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x1 | utmi_bvalid<br>GRF control utmi bvalid. |
| 8 | RW | 0x1 | utmi_vbusvalid<br>GRF control utmi vbus valid. |
| 7 | RW | 0x0 | utmi_txready<br>GRF control utmi txready. |
| 6 | RW | 0x0 | utmi_rxvalidh<br>GRF control utmi rxvalidh. |
| 5 | RW | 0x0 | utmi_rxvalid<br>GRF control utmi rxvalid. |
| 4 | RW | 0x0 | utmi_rxerror<br>GRF control utmi rxerror. |
| 3 | RW | 0x0 | utmi_rxactive<br>GRF control rxactive. |
| 2:1 | RW | 0x0 | utmi_linestate<br>GRF control utmi linestate. |
| 0 | RW | 0x0 | utmi_hostdisconnect<br>GRF control utmi hostdisconnect for usb3otg. |

Rockchip Confidencial

**PHP_GRF_PCIE4L_SID_AW**

Address: Operational Base + offset (0x010C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | grf_pcie4l_sid_aw<br>GRF control PCIe sid for aw channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

**PHP_GRF_PCIE4L_SID_AR**

Address: Operational Base + offset (0x0110)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | grf_pcie4l_sid_ar<br>GRF control PCIe sid for ar channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

**PHP_GRF_PCIE2L_SID_AW**

Address: Operational Base + offset (0x0114)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | grf_pcie2l_sid_aw<br>GRF control PCIe sid for aw channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

**PHP_GRF_PCIE2L_SID_AR**

Address: Operational Base + offset (0x0118)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | grf_pcie2l_sid_ar<br>GRF control PCIe sid for ar channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

**PHP_GRF_PCIE1L0_SID_AW**

Address: Operational Base + offset (0x011C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | grf_pcie1l0_sid_aw<br>GRF control PCIe sid for aw channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

**PHP_GRF_PCIE1L0_SID_AR**

Address: Operational Base + offset (0x0120)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | grf_pcie1l0_sid_ar<br>GRF control PCIe sid for ar channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

Rockchip Confidencial

**PHP_GRF_PCIE1L1_SID_AW**

Address: Operational Base + offset (0x0124)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | grf_pcie1l1_sid_aw<br>GRF control PCIe sid for aw channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

**PHP_GRF_PCIE1L1_SID_AR**

Address: Operational Base + offset (0x0128)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | grf_pcie1l1_sid_ar<br>GRF control PCIe sid for ar channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

**PHP_GRF_PCIE1L2_SID_AW**

Address: Operational Base + offset (0x012C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | grf_pcie1l2_sid_aw<br>GRF control PCIe sid for aw channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

**PHP_GRF_PCIE1L2_SID_AR**

Address: Operational Base + offset (0x0130)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | grf_pcie1l2_sid_ar<br>GRF control PCIe sid for ar channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

**PHP_GRF_PCIE_ATS**

Address: Operational Base + offset (0x0138)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | grf_pcie1l2_ar_ats<br>GRF controller PCIe ats for ar channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |
| 8 | RW | 0x0 | grf_pcie1l1_ar_ats<br>GRF controller PCIe ats for ar channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x0 | grf_pcie1l0_ar_ats<br>GRF controller PCIe ats for ar channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |
| 6 | RW | 0x0 | grf_pcie2l_ar_ats<br>GRF controller PCIe ats for ar channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |
| 5 | RW | 0x0 | grf_pcie4l_ar_ats<br>GRF controller PCIe ats for ar channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |
| 4 | RW | 0x0 | grf_pcie1l2_aw_ats<br>GRF controller PCIe ats for aw channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |
| 3 | RW | 0x0 | grf_pcie1l1_aw_ats<br>GRF controller PCIe ats for aw channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |
| 2 | RW | 0x0 | grf_pcie1l0_aw_ats<br>GRF controller PCIe ats for aw channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |
| 1 | RW | 0x0 | grf_pcie2l_aw_ats<br>GRF controller PCIe ats for aw channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |
| 0 | RW | 0x0 | grf_pcie4l_aw_ats<br>GRF controller PCIe ats for aw channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

**PHP_GRF_ST_UTMI**

Address: Operational Base + offset (0x013C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6 | RO | 0x0 | grf_utmi_l1_suspend_com_n<br>Status for utmi_l1_suspend_com_n. |
| 5 | RO | 0x1 | grf_utmi_l1_suspend_n<br>Status for utmi_l1_suspend_n. |
| 4 | RO | 0x1 | grf_utmi_sleep_n<br>Status for utmi_sleep_n. |
| 3 | RO | 0x0 | grf_utmi_suspend_com_n<br>Status for utmi suspend_com_n. |
| 2 | RO | 0x1 | grf_utmi_suspend_n<br>Status for utmi suspend_n. |
| 1 | RO | 0x0 | grf_utmi_dmpulldowm<br>Status for utmi dmpulldown. |
| 0 | RO | 0x0 | grf_utmi_dppulldown<br>Status for utmi dppulldown. |

**PHP_GRF_PCIE4L_SSID_AW**

Address: Operational Base + offset (0x0144)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | grf_pcei4l_ssid_aw<br>GRF controller PCIe ssid for aw channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

**PHP_GRF_PCIE4L_SSID_AR**

Address: Operational Base + offset (0x0148)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | grf_pcei4l_ssid_ar<br>GRF controller PCIe ssid for ar channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

**PHP_GRF_PCIE2L_SSID_AW**

Address: Operational Base + offset (0x014C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | grf_pcei2l_ssid_aw<br>GRF controller PCIe ssid for aw channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

**PHP_GRF_PCIE2L_SSID_AR**

Address: Operational Base + offset (0x0150)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | grf_pcei2l_ssid_ar<br>GRF controller PCIe ssid for ar channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

**PHP_GRF_PCIE1L0_SSID_AW**

Address: Operational Base + offset (0x0154)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | grf_pcei1l0_ssid_aw<br>GRF controller PCIe ssid for aw channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

**PHP_GRF_PCIE1L0_SSID_AR**

Address: Operational Base + offset (0x0158)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | grf_pcei1l0_ssid_ar<br>GRF controller PCIe ssid for ar channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

**PHP_GRF_PCIE1L1_SSID_AW**

Address: Operational Base + offset (0x015C)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | grf_pcei1l1_ssid_aw<br>GRF controller PCIe ssid for aw channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

**PHP_GRF_PCIE1L1_SSID_AR**

Address: Operational Base + offset (0x0160)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | grf_pcei1l1_ssid_ar<br>GRF controller PCIe ssid for ar channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

**PHP_GRF_PCIE1L2_SSID_AW**

Address: Operational Base + offset (0x0164)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | grf_pcei1l2_ssid_aw<br>GRF controller PCIe ssid for aw channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

**PHP_GRF_PCIE1L2_SSID_AR**

Address: Operational Base + offset (0x0168)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | grf_pcei1l2_ssid_aw<br>GRF controller PCIe ssid for ar channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

**PHP_GRF_PCIE_SSID_V**

Address: Operational Base + offset (0x016C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | grf_pcie1l2_arssid_v<br>GRF control PCIe ssid valid for ar channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |
| 8 | RW | 0x0 | grf_pcie1l1_arssid_v<br>GRF control PCIe ssid valid for ar channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |
| 7 | RW | 0x0 | grf_pcie1l0_arssid_v<br>GRF control PCIe ssid valid for ar channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | grf_pcie2l_arssid_v<br>GRF control PCIe ssid valid for ar channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |
| 5 | RW | 0x0 | grf_pcie4l_arssid_v<br>GRF control PCIe ssid valid for ar channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |
| 4 | RW | 0x0 | grf_pcie1l2_awssid_v<br>GRF control PCIe ssid valid for aw channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |
| 3 | RW | 0x0 | grf_pcie1l1_awssid_v<br>GRF control PCIe ssid valid for aw channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |
| 2 | RW | 0x0 | grf_pcie1l0_awssid_v<br>GRF control PCIe ssid valid for aw channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |
| 1 | RW | 0x0 | grf_pcie2l_awssid_v<br>GRF control PCIe ssid valid for aw channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |
| 0 | RW | 0x0 | grf_pcie4l_awssid_v<br>GRF control PCIe ssid valid for aw channel.<br>This will be select with PCIe controller output, please refer to SGRF and PCIe section. |

**PHP_GRF_SATA_PD_SEL**

Address: Operational Base + offset (0x0174)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x0 | sata2_pd_sel1<br>Select SATA2 powerdown to PHY when powerdown is 4'd1.<br>1'b1: Powerdown to PHY is 4'd1.<br>1'b0: Powerdown to PHY is 4'd3. |
| 4 | RW | 0x0 | sata2_pd_sel0<br>Select SATA2 powerdown to PHY when powerdown is 4'd1.<br>1'b1: Powerdown to PHY is 4'd1.<br>1'b0: Powerdown to PHY is 4'd3. |
| 3 | RW | 0x0 | sata1_pd_sel1<br>Select SATA1 powerdown to PHY when powerdown is 4'd2.<br>1'b1: Powerdown to PHY is 4'd5.<br>1'b0: Powerdown to PHY is 4'd7. |
| 2 | RW | 0x0 | sata1_pd_sel0<br>Select SATA1 powerdown to PHY when powerdown is 4'd1.<br>1'b1: Powerdown to PHY is 4'd1.<br>1'b0: Powerdown to PHY is 4'd3. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | sata0_pd_sel1<br>Select SATA0 powerdown to PHY when powerdown is 4'd2.<br>1'b1: Powerdown to PHY is 4'd5.<br>1'b0: Powerdown to PHY is 4'd7. |
| 0 | RW | 0x0 | sata0_pd_sel0<br>Select SATA0 powerdown to PHY when powerdown is 4'd1.<br>1'b1: Powerdown to PHY is 4'd1.<br>1'b0: Powerdown to PHY is 4'd3. |

**PHP_PCIE_MMU_IRQ_CLR**

Address: Operational Base + offset (0x0178)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tbu0_pmu_irpt<br>Clear irq_pcie_mmu600_r2_tbu0_pmu_irpt.<br>Write 1'b1 to clear then comes to 1'b0. |
| 12 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tbu0_ras_irpt<br>Clear irq_pcie_mmu600_r2_tbu0_ras_irpt.<br>Write 1'b1 to clear then comes to 1'b0. |
| 11 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tbu1_pmu_irpt<br>Clear irq_pcie_mmu600_r2_tbu1_pmu_irpt.<br>Write 1'b1 to clear then comes to 1'b0. |
| 10 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tbu1_ras_irpt<br>Clear irq_pcie_mmu600_r2_tbu1_ras_irpt.<br>Write 1'b1 to clear then comes to 1'b0. |
| 9 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tcu_cmd_sync_irpt_ns<br>Clear irq_pcie_mmu600_r2_tcu_cmd_sync_irpt_ns.<br>Write 1'b1 to clear then comes to 1'b0. |
| 8 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tcu_cmd_sync_irpt_s<br>Clear irq_pcie_mmu600_r2_tcu_cmd_sync_irpt_s.<br>Write 1'b1 to clear then comes to 1'b0. |
| 7 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tcu_event_q_irpt_ns<br>Clear irq_pcie_mmu600_r2_tcu_event_q_irpt_ns.<br>Write 1'b1 to clear then comes to 1'b0. |
| 6 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tcu_event_q_irpt_s<br>Clear irq_pcie_mmu600_r2_tcu_event_q_irpt_s.<br>Write 1'b1 to clear then comes to 1'b0. |
| 5 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tcu_pcie_evento<br>Clear irq_pcie_mmu600_r2_tcu_pcie_evento.<br>Write 1'b1 to clear then comes to 1'b0. |
| 4 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tcu_global_irpt_ns<br>Clear irq_pcie_mmu600_r2_tcu_global_irpt_ns.<br>Write 1'b1 to clear then comes to 1'b0. |
| 3 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tcu_global_irpt_s<br>Clear irq_pcie_mmu600_r2_tcu_global_irpt_s.<br>Write 1'b1 to clear then comes to 1'b0. |
| 2 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tcu_pmu_pcie_irp<br>Clear irq_pcie_mmu600_r2_tcu_pmu_php_irp.<br>Write 1'b1 to clear then comes to 1'b0. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tcu_pri_q_irpt_ns<br>Clear irq_pcie_mmu600_r2_tcu_pri_q_irpt_ns.<br>Write 1'b1 to clear then comes to 1'b0. |
| 0 | R/WSC | 0x0 | clr_irq_pcie_mmu600_r2_tcu_ras_irp<br>Clear irq_pcie_mmu600_r2_tcu_ras_irp.<br>Write 1'b1 to clear then comes to 1'b0. |

**PHP_PHP_MMU_IRQ_CLR**

Address: Operational Base + offset (0x017C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tbu1_pmu_irpt<br>Clear irq_pcie_mmu600_r2_tbu0_pmu_irpt.<br>Write 1'b1 to clear then comes to 1'b0. |
| 12 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tbu0_ras_irpt<br>Clear irq_pcie_mmu600_r2_tbu0_ras_irpt.<br>Write 1'b1 to clear then comes to 1'b0. |
| 11:10 | RO | 0x0 | reserved |
| 9 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tcu_cmd_sync_irpt_ns<br>Clear irq_pcie_mmu600_r2_tcu_cmd_sync_irpt_ns.<br>Write 1'b1 to clear then comes to 1'b0. |
| 8 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tcu_cmd_sync_irpt_s<br>Clear irq_pcie_mmu600_r2_tcu_cmd_sync_irpt_s.<br>Write 1'b1 to clear then comes to 1'b0. |
| 7 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tcu_event_q_irpt_ns<br>Clear irq_pcie_mmu600_r2_tcu_event_q_irpt_ns.<br>Write 1'b1 to clear then comes to 1'b0. |
| 6 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tcu_event_q_irpt_s<br>Clear irq_pcie_mmu600_r2_tcu_event_q_irpt_s.<br>Write 1'b1 to clear then comes to 1'b0. |
| 5 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tcu_php_evento<br>Clear irq_pcie_mmu600_r2_tcu_php_evento.<br>Write 1'b1 to clear then comes to 1'b0. |
| 4 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tcu_global_irpt_ns<br>Clear irq_pcie_mmu600_r2_tcu_global_irpt_ns.<br>Write 1'b1 to clear then comes to 1'b0. |
| 3 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tcu_global_irpt_s<br>Clear irq_pcie_mmu600_r2_tcu_global_irpt_s.<br>Write 1'b1 to clear then comes to 1'b0. |
| 2 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tcu_pmu_php_irp<br>Clear irq_pcie_mmu600_r2_tcu_pmu_php_irp.<br>Write 1'b1 to clear then comes to 1'b0. |
| 1 | RW | 0x0 | clr_irq_pcie_mmu600_r2_tcu_pri_q_irpt_ns<br>Clear irq_pcie_mmu600_r2_tcu_pri_q_irpt_ns.<br>Write 1'b1 to clear then comes to 1'b0. |
| 0 | R/WSC | 0x0 | clr_irq_pcie_mmu600_r2_tcu_ras_irp<br>Clear irq_pcie_mmu600_r2_tcu_ras_irp.<br>Write 1'b1 to clear then comes to 1'b0. |

**PHP_PCIE_MMU_ST**

Address: Operational Base + offset (0x0180)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RO | 0x00000 | reserved |
| 13 | RO | 0x0 | st_pcie_mmu600_r2_tbu0_pmu_irpt<br>PMU interrupt. |
| 12 | RO | 0x0 | st_pcie_mmu600_r2_tbu0_ras_irpt<br>RAS interrupt. |
| 11 | RO | 0x0 | st_pcie_mmu600_r2_tbu1_pmu_irpt<br>PMU interrupt. |
| 10 | RO | 0x0 | st_pcie_mmu600_r2_tbu1_ras_irpt<br>RAS interrupt. |
| 9 | RO | 0x0 | st_pcie_mmu600_r2_tcu_cmd_sync_irpt_ns<br>SYNC complete, Non-secure interrupt. Asserts a Non-secure interrupt to indicate that the CMD_SYNC command is complete. |
| 8 | RO | 0x0 | st_pcie_mmu600_r2_tcu_cmd_sync_irpt_s<br>SYNC complete, Secure interrupt. Asserts a Secure interrupt to indicate that the CMD_SYNC command is complete. |
| 7 | RO | 0x0 | st_pcie_mmu600_r2_tcu_event_q_irpt_ns<br>Event queue, Non-secure interrupt. Asserts a Non-secure interrupt to indicate that the Event queue is not empty or has overflowed. |
| 6 | RO | 0x0 | st_pcie_mmu600_r2_tcu_event_q_irpt_s<br>Event queue, Secure interrupt. Asserts a Secure interrupt to indicate that the Event queue is not empty or has overflowed. |
| 5 | RO | 0x0 | st_pcie_mmu600_r2_tcu_pcie_evento<br>Event output for connection to processors. This signal is asserted for one cycle to indicate an event that enables processors to wake up from WFE low-power state. |
| 4 | RO | 0x0 | st_pcie_mmu600_r2_tcu_global_irpt_ns<br>Asserts a global Non-secure interrupt. |
| 3 | RO | 0x0 | st_pcie_mmu600_r2_tcu_global_irpt_s<br>Asserts a global Secure interrupt. |
| 2 | RO | 0x0 | st_pcie_mmu600_r2_tcu_pmu_pcie_irp<br>Asserts a PMU interrupt. |
| 1 | RO | 0x0 | st_pcie_mmu600_r2_tcu_pri_q_irpt_ns<br>Asserts a Page Request Interface (PRI) queue interrupt. |
| 0 | RO | 0x0 | st_pcie_mmu600_r2_tcu_ras_irp<br>Asserts a Reliability, Availability, and Serviceability (RAS) interrupt. |

**PHP_PHP_MMU_ST**

Address: Operational Base + offset (0x0184)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RO | 0x00000 | reserved |
| 13 | RO | 0x0 | st_pcie_mmu600_r2_tbu0_pmu_irpt<br>PMU interrupt. |
| 12 | RO | 0x0 | st_pcie_mmu600_r2_tbu0_ras_irpt<br>RAS interrupt. |
| 11:10 | RO | 0x0 | reserved |
| 9 | RO | 0x0 | st_pcie_mmu600_r2_tcu_cmd_sync_irpt_ns<br>SYNC complete, Non-secure interrupt. Asserts a Non-secure interrupt to indicate that the CMD_SYNC command is complete. |
| 8 | RO | 0x0 | st_pcie_mmu600_r2_tcu_cmd_sync_irpt_s<br>SYNC complete, Secure interrupt. Asserts a Secure interrupt to indicate that the CMD_SYNC command is complete. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RO | 0x0 | st_pcie_mmu600_r2_tcu_event_q_irpt_ns<br>Event queue, Non-secure interrupt. Asserts a Non-secure interrupt to indicate that the Event queue is not empty or has overflowed. |
| 6 | RO | 0x0 | st_pcie_mmu600_r2_tcu_event_q_irpt_s<br>Event queue, Secure interrupt. Asserts a Secure interrupt to indicate that the Event queue is not empty or has overflowed. |
| 5 | RO | 0x0 | st_pcie_mmu600_r2_tcu_php_evento<br>Event output for connection to processors. This signal is asserted for one cycle to indicate an event that enables processors to wake up from WFE low-power state. |
| 4 | RO | 0x0 | st_pcie_mmu600_r2_tcu_global_irpt_ns<br>Asserts a global Non-secure interrupt. |
| 3 | RO | 0x0 | st_pcie_mmu600_r2_tcu_global_irpt_s<br>Asserts a global Secure interrupt. |
| 2 | RO | 0x0 | st_pcie_mmu600_r2_tcu_pmu_php_irp<br>Asserts a PMU interrupt. |
| 1 | RO | 0x0 | st_pcie_mmu600_r2_tcu_pri_q_irpt_ns<br>Asserts a Page Request Interface (PRI) queue interrupt. |
| 0 | RO | 0x0 | st_pcie_mmu600_r2_tcu_ras_irp<br>Asserts a Reliability, Availability, and Serviceability (RAS) interrupt. |

**PHP_PHP_ST0B**

Address: Operational Base + offset (0x018C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4 | RO | 0x0 | gmac1_mcgr_dma_req_intr<br>MCGR DMA Read Request<br>Used to Request a Target Presentation time value for one of the comparator modules when the instance is running in recovery mode. In Media Clock generation mode, this I/O signal is held high indicating a valid Presentation time is captured and updated in MAC_PPS(i)_Target_Time_Seconds register. One or more DMA read requests can simultaneously active, it is up to the DMA logic to maintain priority. Bits have a 1-1 correspondence to the comparator instances<br>(i.e. Bit-0 belongs to comparator 0, bit-1 belongs to comparator-1 and so on). Once set, will hold high and will be reset the cycle after receiving the mcgr_dma_ack for that comparator. Width of this IO changes with the configured number of PPS instances. |
| 3:2 | RO | 0x0 | gmac1_speed<br>Mac Speed indication/status.<br>2'b00:1000Mbps (GMII)<br>2'b01:2500Mbps (GMII)<br>2'b10:10Mbps (MII)<br>2'b11:100Mbps (MII) |
| 1 | RO | 0x0 | gmac1_ptp_pps<br>Pulse Per Second.<br>This signal is high based on the PPS mode selected in the MAC_PPS_Control register. When PPS is programmed in Media Clock recovery Mode, this port indicates the recovered clock. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RO | 0x0 | gmac1_sdb_tx_clk_gating_ctrl<br>LPI Tx Clock Gating Control.<br>This signal is high after the MAC enters the Tx LPI (low power idle) mode. You can use this signal to control the Tx clock gating. |

# 6.18 CSIDPHY_GRF Register Description

There are two CSIDPHY_GRF modules in RK3588.They have different base address.

## 6.18.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CSIDPHY_GRF_CON0 | 0x0000 | W | 0x00000000 | CSIDPHY Control Register |
| CSIDPHY_GRF_STATUS0 | 0x0080 | W | 0x00000000 | CSIDPHY Status Register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.18.2 Detail Registers Description

**CSIDPHY_GRF_CON0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | csidphy_clk_1_inv<br>Invert CSIDPHY clock lane1 rxbyte clock<br>1'b1: Invert CSIDPHY clock lane 1 rxbyte_clk_hs<br>1'b0: Do not invert CSIDPHY clock lane 1 rxbyte_clk_hs |
| 10 | RW | 0x0 | csidphy_enable_ck_1<br>CSIDPHY Clock Lane 1 enable signal<br>Active State: High |
| 9 | RW | 0x0 | csidphy_clk_0_inv<br>Invert CSIDPHY rxbyte clock<br>1'b1: Invert CSIDPHY rxbyte_clk_hs<br>1'b0: Do not invert CSIDPHY rxbyte_clk_hs |
| 8 | RW | 0x0 | csidphy_enable_ck_0<br>CSIDPHY Clock Lane enable signal<br>Active State: High |
| 7:4 | RW | 0x0 | csidphy_enable_dat<br>CSIDPHY enable lane module<br>This active high signal forces the Lane Module out of "shutdown". All line drivers, receivers, terminators, and connection detectors are turned off when Enable is low. Enable is a level sensitive signal and does not depend on any clock. |
| 3:0 | RW | 0x0 | csidphy_forcerxmode<br>CSIDPHY force receive mode<br>Force Lane Module Into Receive mode / Wait for Stop state.This signal allows the protocol to initialize a Lane Module, or force a bi-directional Lane Module, into receive mode. |

**CSIDPHY_GRF_STATUS0**

Address: Operational Base + offset (0x0080)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:19 | RO | 0x0000 | reserved |
| 18 | RO | 0x0 | s_ulpsactivenotclk_1_raw<br>ULP State (not) Active 1 status<br>This active low signal is asserted to indicate that the Lane is in ULP state. |
| 17 | RO | 0x0 | s_ulpsactivenotclk_raw<br>ULP State (not) Active status<br>This active low signal is asserted to indicate that the Lane is in ULP state. |
| 16:9 | RO | 0x00 | errcontentionlp<br>LP Contention Error<br>This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line low. |
| 8:5 | RO | 0x0 | rxskewcalhs<br>High-Speed Receive Skew Calibration<br>This optional active high signal indicates that the high speed deskew burst is being received. RxSkewCalHS is set to the active state when the all-ones sync pattern is received, and is cleared to the inactive state when Dp and Dn transition back to the LP-11 Stop State. |
| 4 | RO | 0x0 | direction<br>This signal is used to indicate the current direction of the Lane interconnects. When pin_direction =0, the Lane is in transmit mode. When pin_direction =1, the Lane is in receive mode. |
| 3:0 | RO | 0x0 | ulpsactivenot<br>ULP State (not) Active.<br>This active low signal is asserted to indicate that the Lane is in ULP state. |

# 6.19 PCIe3PHY_GRF Register Description

## 6.19.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PCIe3PHY_GRF_CMN_CON0 | 0x0000 | W | 0x00003004 | PCIe 3.0 PHY Common Control Register 0 |
| PCIe3PHY_GRF_CMN_CON1 | 0x0004 | W | 0x00000001 | PCIe 3.0 PHY Common Control Register 1 |
| PCIe3PHY_GRF_CMN_CON2 | 0x0008 | W | 0x00000001 | PCIe 3.0 PHY Common Control Register 2 |
| PCIe3PHY_GRF_CMN_CON3 | 0x000C | W | 0x00000000 | PCIe 3.0 PHY Common Control Register 3 |
| PCIe3PHY_GRF_PHY0_CON0 | 0x0100 | W | 0x00000000 | PCIe 3.0 PHY 0 Control Register 0 |
| PCIe3PHY_GRF_PHY0_CON1 | 0x0104 | W | 0x00000000 | PCIe 3.0 PHY 0 Control Register 1 |
| PCIe3PHY_GRF_PHY0_CON2 | 0x0108 | W | 0x00000003 | PCIe 3.0 PHY 0 Control Register 2 |
| PCIe3PHY_GRF_PHY0_CON3 | 0x010C | W | 0x00000000 | PCIe 3.0 PHY 0 Control Register 3 |
| PCIe3PHY_GRF_PHY0_CON4 | 0x0110 | W | 0x00000033 | PCIe 3.0 PHY 0 Control Register 4 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PCIe3PHY_GRF_PHY0_CON5 | 0x0114 | W | 0x00000003 | PCIe 3.0 PHY 0 Control Register 5 |
| PCIe3PHY_GRF_PHY0_CON6 | 0x0118 | W | 0x00000004 | PCIe 3.0 PHY 0 Control Register 6 |
| PCIe3PHY_GRF_PHY0_CON7 | 0x011C | W | 0x00000000 | PCIe 3.0 PHY 0 Control Register 7 |
| PCIe3PHY_GRF_PHY0_CON8 | 0x0120 | W | 0x00000011 | PCIe 3.0 PHY 0 Control Register 8 |
| PCIe3PHY_GRF_PHY0_CON9 | 0x0124 | W | 0x00000000 | PCIe 3.0 PHY 0 Control Register 9 |
| PCIe3PHY_GRF_PHY1_CON0 | 0x0200 | W | 0x00000000 | PCIe 3.0 PHY 1 Control Register 0 |
| PCIe3PHY_GRF_PHY1_CON1 | 0x0204 | W | 0x00000000 | PCIe 3.0 PHY 1 Control Register 1 |
| PCIe3PHY_GRF_PHY1_CON2 | 0x0208 | W | 0x00000003 | PCIe 3.0 PHY 1 Control Register 2 |
| PCIe3PHY_GRF_PHY1_CON3 | 0x020C | W | 0x00000000 | PCIe 3.0 PHY 1 Control Register 3 |
| PCIe3PHY_GRF_PHY1_CON4 | 0x0210 | W | 0x00000033 | PCIe 3.0 PHY 1 Control Register 4 |
| PCIe3PHY_GRF_PHY1_CON5 | 0x0214 | W | 0x00000003 | PCIe 3.0 PHY 1 Control Register 5 |
| PCIe3PHY_GRF_PHY1_CON6 | 0x0218 | W | 0x00000004 | PCIe 3.0 PHY 1 Control Register 6 |
| PCIe3PHY_GRF_PHY1_CON7 | 0x021C | W | 0x00000000 | PCIe 3.0 PHY 1 Control Register 7 |
| PCIe3PHY_GRF_PHY1_CON8 | 0x0220 | W | 0x00000011 | PCIe 3.0 PHY 1 Control Register 8 |
| PCIe3PHY_GRF_PHY1_CON9 | 0x0224 | W | 0x00000000 | PCIe 3.0 PHY 1 Control Register 9 |
| PCIe3PHY_GRF_CMN_STATUS0 | 0x0800 | W | 0x00000002 | PCIe 3.0 PHY Common Status Register 0 |
| PCIe3PHY_GRF_PHY0_STATUS0 | 0x0900 | W | 0x00000000 | PCIe 3.0 PHY 0 Common Status Register 0 |
| PCIe3PHY_GRF_PHY0_STATUS1 | 0x0904 | W | 0x00000006 | PCIe 3.0 PHY 0 Common Status Register 1 |
| PCIe3PHY_GRF_PHY0_STATUS2 | 0x0908 | W | 0x00000004 | PCIe 3.0 PHY 0 Common Status Register 2 |
| PCIe3PHY_GRF_PHY0_STATUS3 | 0x090C | W | 0x00000004 | PCIe 3.0 PHY 0 Common Status Register 3 |
| PCIe3PHY_GRF_PHY0_STATUS4 | 0x0910 | W | 0x00000000 | PCIe 3.0 PHY 0 Common Status Register 4 |
| PCIe3PHY_GRF_PHY1_STATUS0 | 0x0A00 | W | 0x00000000 | PCIe 3.0 PHY 1 Common Status Register 0 |
| PCIe3PHY_GRF_PHY1_STATUS1 | 0x0A04 | W | 0x00000006 | PCIe 3.0 PHY 1 Common Status Register 1 |
| PCIe3PHY_GRF_PHY1_STATUS2 | 0x0A08 | W | 0x00000004 | PCIe 3.0 PHY 1 Common Status Register 2 |
| PCIe3PHY_GRF_PHY1_STATUS3 | 0x0A0C | W | 0x00000004 | PCIe 3.0 PHY 1 Common Status Register 3 |
| PCIe3PHY_GRF_PHY1_STATUS4 | 0x0A10 | W | 0x00000000 | PCIe 3.0 PHY 1 Common Status Register 4 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PCIe3PHY_GRF_PHY0_LN0_CON0 | 0x1000 | W | 0x00000310 | PCIe 3.0 PHY 0 Lane 0 Control Register 0 |
| PCIe3PHY_GRF_PHY0_LN0_CON1 | 0x1004 | W | 0x000000A0 | PCIe 3.0 PHY 0 Lane 0 Control Register 1 |
| PCIe3PHY_GRF_PHY0_LN0_CON2 | 0x1008 | W | 0x00000000 | PCIe 3.0 PHY 0 Lane 0 Control Register 2 |
| PCIe3PHY_GRF_PHY0_LN0_CON3 | 0x100C | W | 0x00000000 | PCIe 3.0 PHY 0 Lane 0 Control Register 3 |
| PCIe3PHY_GRF_PHY0_LN0_CON4 | 0x1010 | W | 0x00000000 | PCIe 3.0 PHY 0 Lane 0 Control Register 4 |
| PCIe3PHY_GRF_PHY0_LN1_CON0 | 0x1100 | W | 0x00000310 | PCIe 3.0 PHY 0 Lane 1 Control Register 0 |
| PCIe3PHY_GRF_PHY0_LN1_CON1 | 0x1104 | W | 0x000000A0 | PCIe 3.0 PHY 0 Lane 1 Control Register 1 |
| PCIe3PHY_GRF_PHY0_LN1_CON2 | 0x1108 | W | 0x00000000 | PCIe 3.0 PHY 0 Lane 1 Control Register 2 |
| PCIe3PHY_GRF_PHY0_LN1_CON3 | 0x110C | W | 0x00000000 | PCIe 3.0 PHY 0 Lane 1 Control Register 3 |
| PCIe3PHY_GRF_PHY0_LN1_CON4 | 0x1110 | W | 0x00000000 | PCIe 3.0 PHY 0 Lane 1 Control Register 4 |
| PCIe3PHY_GRF_PHY1_LN0_CON0 | 0x2000 | W | 0x00000310 | PCIe 3.0 PHY 1 Lane 0 Control Register 0 |
| PCIe3PHY_GRF_PHY1_LN0_CON1 | 0x2004 | W | 0x000000A0 | PCIe 3.0 PHY 1 Lane 0 Control Register 1 |
| PCIe3PHY_GRF_PHY1_LN0_CON2 | 0x2008 | W | 0x00000000 | PCIe 3.0 PHY 1 Lane 0 Control Register 2 |
| PCIe3PHY_GRF_PHY1_LN0_CON3 | 0x200C | W | 0x00000000 | PCIe 3.0 PHY 1 Lane 0 Control Register 3 |
| PCIe3PHY_GRF_PHY1_LN0_CON4 | 0x2010 | W | 0x00000000 | PCIe 3.0 PHY 1 Lane 0 Control Register 4 |
| PCIe3PHY_GRF_PHY1_LN1_CON0 | 0x2100 | W | 0x00000310 | PCIe 3.0 PHY 1 Lane 1 Control Register 0 |
| PCIe3PHY_GRF_PHY1_LN1_CON1 | 0x2104 | W | 0x000000A0 | PCIe 3.0 PHY 1 Lane 1 Control Register 1 |
| PCIe3PHY_GRF_PHY1_LN1_CON2 | 0x2108 | W | 0x00000000 | PCIe 3.0 PHY 1 Lane 1 Control Register 2 |
| PCIe3PHY_GRF_PHY1_LN1_CON3 | 0x210C | W | 0x00000000 | PCIe 3.0 PHY 1 Lane 1 Control Register 3 |
| PCIe3PHY_GRF_PHY1_LN1_CON4 | 0x2110 | W | 0x00000000 | PCIe 3.0 PHY 1 Lane 1 Control Register 4 |
| PCIe3PHY_GRF_PRT0_CON0 | 0x3000 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 0 |
| PCIe3PHY_GRF_PRT0_CON1 | 0x3004 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 1 |
| PCIe3PHY_GRF_PRT0_CON2 | 0x3008 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 2 |
| PCIe3PHY_GRF_PRT0_CON3 | 0x300C | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 3 |
| PCIe3PHY_GRF_PRT0_CON4 | 0x3010 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 4 |
| PCIe3PHY_GRF_PRT0_CON5 | 0x3014 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 5 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PCIe3PHY_GRF_PRT0_CON6 | 0x3018 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 6 |
| PCIe3PHY_GRF_PRT0_CON7 | 0x301C | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 7 |
| PCIe3PHY_GRF_PRT0_CON8 | 0x3020 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 8 |
| PCIe3PHY_GRF_PRT0_CON9 | 0x3024 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 9 |
| PCIe3PHY_GRF_PRT0_CON10 | 0x3028 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 10 |
| PCIe3PHY_GRF_PRT0_CON11 | 0x302C | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 11 |
| PCIe3PHY_GRF_PRT0_CON12 | 0x3030 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 12 |
| PCIe3PHY_GRF_PRT0_CON13 | 0x3034 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 13 |
| PCIe3PHY_GRF_PRT0_CON14 | 0x3038 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 14 |
| PCIe3PHY_GRF_PRT0_CON15 | 0x303C | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 15 |
| PCIe3PHY_GRF_PRT0_CON16 | 0x3040 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 16 |
| PCIe3PHY_GRF_PRT0_CON17 | 0x3044 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 17 |
| PCIe3PHY_GRF_PRT0_CON18 | 0x3048 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 18 |
| PCIe3PHY_GRF_PRT0_CON19 | 0x304C | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 19 |
| PCIe3PHY_GRF_PRT0_CON20 | 0x3050 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 20 |
| PCIe3PHY_GRF_PRT0_CON21 | 0x3054 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 21 |
| PCIe3PHY_GRF_PRT0_CON22 | 0x3058 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 22 |
| PCIe3PHY_GRF_PRT0_CON23 | 0x305C | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 23 |
| PCIe3PHY_GRF_PRT0_CON24 | 0x3060 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 24 |
| PCIe3PHY_GRF_PRT0_CON25 | 0x3064 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 25 |
| PCIe3PHY_GRF_PRT0_CON26 | 0x3068 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 26 |
| PCIe3PHY_GRF_PRT0_CON27 | 0x306C | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 27 |
| PCIe3PHY_GRF_PRT0_CON28 | 0x3070 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 28 |
| PCIe3PHY_GRF_PRT0_CON29 | 0x3074 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 29 |
| PCIe3PHY_GRF_PRT0_CON30 | 0x3078 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 30 |
| PCIe3PHY_GRF_PRT0_CON31 | 0x307C | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 31 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PCIe3PHY_GRF_PRT0_CON32 | 0x3080 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 32 |
| PCIe3PHY_GRF_PRT0_CON33 | 0x3084 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 33 |
| PCIe3PHY_GRF_PRT0_CON34 | 0x3088 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 34 |
| PCIe3PHY_GRF_PRT0_CON35 | 0x308C | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 35 |
| PCIe3PHY_GRF_PRT0_CON36 | 0x3090 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 36 |
| PCIe3PHY_GRF_PRT0_CON37 | 0x3094 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 37 |
| PCIe3PHY_GRF_PRT0_CON38 | 0x3098 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 38 |
| PCIe3PHY_GRF_PRT0_CON39 | 0x309C | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 39 |
| PCIe3PHY_GRF_PRT0_CON50 | 0x3140 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 50 |
| PCIe3PHY_GRF_PRT0_CON51 | 0x3144 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 51 |
| PCIe3PHY_GRF_PRT0_CON52 | 0x3148 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 52 |
| PCIe3PHY_GRF_PRT0_CON53 | 0x314C | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 53 |
| PCIe3PHY_GRF_PRT0_CON54 | 0x3150 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 54 |
| PCIe3PHY_GRF_PRT0_CON55 | 0x3154 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 55 |
| PCIe3PHY_GRF_PRT0_CON56 | 0x3158 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 56 |
| PCIe3PHY_GRF_PRT0_CON57 | 0x315C | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 57 |
| PCIe3PHY_GRF_PRT0_CON58 | 0x3160 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 58 |
| PCIe3PHY_GRF_PRT0_CON59 | 0x3164 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 59 |
| PCIe3PHY_GRF_PRT0_CON60 | 0x3168 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 60 |
| PCIe3PHY_GRF_PRT0_CON61 | 0x316C | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 61 |
| PCIe3PHY_GRF_PRT0_CON62 | 0x3170 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 62 |
| PCIe3PHY_GRF_PRT0_CON63 | 0x3174 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 63 |
| PCIe3PHY_GRF_PRT0_CON64 | 0x3178 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 64 |
| PCIe3PHY_GRF_PRT0_CON65 | 0x317C | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 65 |
| PCIe3PHY_GRF_PRT0_CON66 | 0x3180 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 66 |
| PCIe3PHY_GRF_PRT0_CON67 | 0x3184 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 67 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PCIe3PHY_GRF_PRT0_CON68 | 0x3188 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 68 |
| PCIe3PHY_GRF_PRT0_CON69 | 0x318C | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 69 |
| PCIe3PHY_GRF_PRT0_CON70 | 0x3190 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 70 |
| PCIe3PHY_GRF_PRT0_CON71 | 0x3194 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 71 |
| PCIe3PHY_GRF_PRT0_CON72 | 0x3198 | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 72 |
| PCIe3PHY_GRF_PRT0_CON73 | 0x319C | W | 0x00000000 | PCIe 3.0 PHY Protocol 0 Control Register 73 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.19.2 Detail Registers Description

**PCIe3PHY_GRF_CMN_CON0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x1 | link_num_ctrl_mode<br>Link number assignment method<br>1'b0: Overwrite by PHY GRF<br>1'b1: Auto generation by hardware<br>Reserved for RK3588 |
| 12 | RW | 0x1 | pipe_rx_recal_cont_en<br>This pin enables re-locking when alignment is lost in non-8B10 mode. Default value is 1; it is recommended that you control this signal in your SoC via register. |
| 11:9 | RO | 0x0 | reserved |
| 8 | RW | 0x0 | pcie30_clamp_n<br>PMA output clamp for PCS.<br>If the PHY analog power is not present, it should be clamp.<br>1'b0: Clamp enable<br>1'b1: Clamp release |
| 7:3 | RO | 0x00 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2:0 | RW | 0x4 | pcie30_phy_mode<br>PCIe30 PHY mode.<br>pcie30_phy_mode[2].<br>The PHY0 and PHY1 aggregation as 1 link when this bit set to 1'b1, and the pcie30_phy_mode[1:0] become invalid. When aggregation is enabled, the 4L controller is integrated as a X4 link controller. If this bit is set to 1'b0, the usage of PHY0 and PHY1 depends on pcie30_phy_mode[1:0].<br>1'b0: Aggregation disable<br>1'b1: Aggregation enable<br><br>pcie30_phy_mode[1].<br>The PHY1 bifurcation enable control, only valid when pcie30_phy_mode[2] is set to 1'b0. If this bit set to 1'b1 the PHY1 (lane 2 and lane3) can work as two links, and the two link PMA share the common analog and reference clock for PHY1. When bifurcation is disable, the 2L controller is integrated with PHY1 as a X2 link. When bifurcation is enabled, the 2L controller connects to lane2 and 1L1 controller connects to lane3 (The pcie1l1_sel in PD PHP GRF should set to 1'b1).<br>1'b0: Bifurcation disable<br>1'b1: Bifurcation enable<br><br>pcie30_phy_mode[0].<br>The PHY0 bifurcation enable control, only valid when pcie30_phy_mode[2] is set to 1'b0. If this bit set to 1'b1 the PHY0 (lane 0 and lane1) can work as two links, and the two link PMA share the common analog and reference clock for PHY0. When bifurcation is disable, the 4L controller is integrated with PHY0 as a X2 link. When bifurcation is enabled, the 4L controller connects to lane0 and 1L0 controller connects to lane1 (The pcie1l0_sel in PD PHP GRF should set to 1'b1).<br>1'b0: Bifurcation disable<br>1'b1: Bifurcation enable |

**PCIe3PHY_GRF_CMN_CON1**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0001 | upcs_pipe_config<br>PCS PIPE configuration.<br>When upcs_pipe_config[0] is set to 1, the PCS ignores lane-off via PIPE specification method (TxElecIdle = 1 and TxCompliance = 1) and responds to power-down/rate/width changes. Otherwise, until the MAC de-assert the "turned off" signaling, the PCS ignores any commands to change power-down/rate/width after being turned off. |

**PCIe3PHY_GRF_CMN_CON2**

Address: Operational Base + offset (0x0008)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | ext_pclk_req<br>I External PCLK request.<br>When asserted, the MPLL clock sources in the PHY are powered up and pcs_laneX_pclk outputs stay active, regardless of the pcs_laneX_powerdown[3:0] inputs. |
| 2 | RW | 0x0 | phy_rtune_req<br>Resistor tune request.<br>Assertion of it triggers a resistor tune request to PHYN. |
| 1 | RW | 0x0 | phy_ext_ctrl_sel<br>phy_ext_ctrl_sel is PHY configuration setting per-protocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY Databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 0 | RW | 0x1 | upcs_pwr_stable<br>Power stable to PCS.<br>Status signal indicating that power for the PCS is stable.<br>For information about power gating, see "Power Gating Support" section. TIE to 1. |

**PCIe3PHY_GRF_CMN_CON3**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | phy_test_burnin<br>All circuits activators.<br>Reserved. Tie off to 1'b0.<br>For the full signal description, refer to the PHY Databook, "Signal Descriptions" chapter. |
| 0 | RW | 0x0 | phy_test_powerdown<br>All circuits power-down control.<br>Powers down all circuitry in the PHY for IDDQ testing.<br>Note:<br>The PHY is not functional in this mode and must be reset after this signal is de-asserted.<br>For the full signal description, refer to the PHY Databook, "Signal Descriptions" chapter. |

Rockchip Confidential

**PCIe3PHY_GRF_PHY0_CON0**

Address: Operational Base + offset (0x0100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x000 | txdn_term_offset<br>Reserved |

**PCIe3PHY_GRF_PHY0_CON1**

Address: Operational Base + offset (0x0104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x000 | txup_term_offset<br>Reserved |

**PCIe3PHY_GRF_PHY0_CON2**

Address: Operational Base + offset (0x0108)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x1 | rx1_term_acdc<br>Reserved |
| 0 | RW | 0x1 | rx0_term_acdc<br>Reserved |

**PCIe3PHY_GRF_PHY0_CON3**

Address: Operational Base + offset (0x010C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:5 | RO | 0x000 | reserved |
| 4:0 | RW | 0x00 | rx_term_offset<br>Reserved |

**PCIe3PHY_GRF_PHY0_CON4**

Address: Operational Base + offset (0x0110)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x1 | pma_pwr_stable<br>Power stable for PMA.<br>Status signal indicating that the power for the PMA is stable. For more information see "Power Gating" in the "PHY Usage and Configuration" chapter. |
| 4 | RW | 0x1 | pcs_pwr_stable<br>Power stable for Raw PCS.<br>Status signal indicating that the power for the Raw PCS is stable. For more information see "Power Gating" in the "PHY Usage and Configuration" chapter. |
| 3:2 | RO | 0x0 | reserved |
| 1:0 | RW | 0x3 | nominal_vph_sel<br>Reserved |

**PCIe3PHY_GRF_PHY0_CON5**

Address: Operational Base + offset (0x0114)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x1 | lane1_power_present<br>VBUS power present.<br>Signal from external VBUS detection circuit. |
| 0 | RW | 0x1 | lane0_power_present<br>VBUS power present.<br>Signal from external VBUS detection circuit. |

**PCIe3PHY_GRF_PHY0_CON6**

Address: Operational Base + offset (0x0118)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:3 | RO | 0x0000 | reserved |
| 2 | RW | 0x1 | ref_use_pad<br>Select reference clock connected to ref_pad_clk_p/ref_pad_clk_m. Selects the external ref_pad_clk_p and ref_pad_clk_m inputs as the reference clock source when asserted. When de-asserted, ref_alt_clk_p and ref_alt_clk_m are the sources of the reference clock. Any change in this input must be followed by phy_reset assertion.<br>Note:<br>A transition on this input must be followed by the assertion of phy_reset. |
| 1 | RW | 0x0 | ref_repeat_clk_en<br>Repeat reference clock enable<br>Enables the CMOS output clocks ref_repeat_clk_(p,m). This pair of clocks can be used as reference clocks for other on-chip PHYs. |
| 0 | RW | 0x0 | ref_clkdet_en<br>Reserved |

**PCIe3PHY_GRF_PHY0_CON7**

Rockchip Confidencial

Address: Operational Base + offset (0x011C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x0 | mpllb_ssc_en<br>Spread spectrum enable.<br>Enables spread-spectrum clock (SSC) generation on the mpllb_div_clk output. If the reference clock already has spread spectrum applied, mpllb_ssc_en must be de-asserted. These inputs can only be changed when the txX_mpll_en inputs for all lanes are de-asserted. |
| 4 | RW | 0x0 | mpllb_force_en<br>MPLLB force enable.<br>When asserted, the corresponding MPLL is forced to be powered up, irrespective of the txX_mpll_en input.<br>This input is used for applications where a free-running MPLL clock output is required. There are no restrictions on when the mpllb_force_en signal can be transitioned. If MPLL is not powered up, we recommend that you follow the txX_mpll_en controls as shown in the "MPLLA Configuration Settings Update Followed By a TX Power-state Change" figure in the "PHY Usage and Configuration" chapter. |
| 3:2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | mplla_ssc_en<br>Spread spectrum enable.<br>Enables spread-spectrum clock (SSC) generation on the mplla_div_clk output. If the reference clock already has spread spectrum applied, mplla_ssc_en must be de-asserted. These inputs can only be changed when the txX_mpll_en inputs for all lanes are de-asserted. |
| 0 | RW | 0x0 | mplla_force_en<br>MPLLA force enable.<br>When asserted, the corresponding MPLL is forced to be powered up, irrespective of the txX_mpll_en input.<br>This input is used for applications where a free-running MPLL clock output is required. There are no restrictions on when the mplla_force_en signal can be transitioned. If MPLL is not powered up, we recommend that you follow the txX_mpll_en controls as shown in the "MPLLA Configuration Settings Update Followed By a TX Power-state Change" figure in the "PHY Usage and Configuration" chapter. |

**PCIe3PHY_GRF_PHY0_CON8**

Address: Operational Base + offset (0x0120)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:5 | RO | 0x000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x1 | cr_para_sel<br>Control Register (CR) parallel interface select.<br>Controls selection between JTAG and CR interfaces:<br>1'b0: JTAG<br>1'b1: Control Register (CR)<br>This input can only be changed when the cr_para_clk and jtag_tck clock inputs are disabled. |
| 3:2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | sram_ext_ld_done<br>SRAM external load done.<br>Signal asserted by user after any updates to the SRAM have been loaded.<br>For the full signal description, refer to the PHY Databook, "Signal Descriptions" chapter. |
| 0 | RW | 0x1 | sram_bypass<br>SRAM bypass control signal when asserted, bypasses the SRAM interface.<br>In this case, the adaptation and calibration algorithms are executed from the hard-wired values within the Raw PCS.<br>If SRAM is not bypassed, the internal algorithms are first loaded by Raw PCS into the SRAM at which point user can change the contents of the SRAM. The updated SRAM contents are used for the adaptation and calibration routines.<br>This signal is meant to be used only for debugging purposes and must not change after phy_reset is negated.<br>For the full signal description, refer to the PHY Databook, "Signal Descriptions" chapter. |

**PCIe3PHY_GRF_PHY0_CON9**

Address: Operational Base + offset (0x0124)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | lane1_rx2tx_par_lb_en<br>Parallel (RX to TX) loopback enable.<br>When this signal is asserted, recovered parallel data from the receiver is looped back to the transmit serializer. |
| 0 | RW | 0x0 | lane0_rx2tx_par_lb_en<br>Parallel (RX to TX) loopback enable.<br>When this signal is asserted, recovered parallel data from the receiver is looped back to the transmit serializer. |

**PCIe3PHY_GRF_PHY1_CON0**

Address: Operational Base + offset (0x0200)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x000 | txdn_term_offset<br>Reserved |

Rockchip Confidential

**PCIe3PHY_GRF_PHY1_CON1**

Address: Operational Base + offset (0x0204)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x000 | txup_term_offset<br>Reserved |

**PCIe3PHY_GRF_PHY1_CON2**

Address: Operational Base + offset (0x0208)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x1 | rx1_term_acdc<br>Reserved |
| 0 | RW | 0x1 | rx0_term_acdc<br>Reserved |

**PCIe3PHY_GRF_PHY1_CON3**

Address: Operational Base + offset (0x020C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:5 | RO | 0x000 | reserved |
| 4:0 | RW | 0x00 | rx_term_offset<br>Reserved |

**PCIe3PHY_GRF_PHY1_CON4**

Address: Operational Base + offset (0x0210)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x1 | pma_pwr_stable<br>Power stable for PMA.<br>Status signal indicating that the power for the PMA is stable. For more information see "Power Gating" in the "PHY Usage and Configuration" chapter. |
| 4 | RW | 0x1 | pcs_pwr_stable<br>Power stable for Raw PCS.<br>Status signal indicating that the power for the Raw PCS is stable. For more information see "Power Gating" in the "PHY Usage and Configuration" chapter. |
| 3:2 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1:0 | RW | 0x3 | nominal_vph_sel<br>Reserved |

**PCIe3PHY_GRF_PHY1_CON5**

Address: Operational Base + offset (0x0214)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x1 | lane1_power_present<br>VBUS power present.<br>Signal from external VBUS detection circuit. |
| 0 | RW | 0x1 | lane0_power_present<br>VBUS power present.<br>Signal from external VBUS detection circuit. |

**PCIe3PHY_GRF_PHY1_CON6**

Address: Operational Base + offset (0x0218)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:3 | RO | 0x0000 | reserved |
| 2 | RW | 0x1 | ref_use_pad<br>Select reference clock connected to ref_pad_clk_p/ref_pad_clk_m. Selects the external ref_pad_clk_p and ref_pad_clk_m inputs as the reference clock source when asserted. When de-asserted, ref_alt_clk_p and ref_alt_clk_m are the sources of the reference clock. Any change in this input must be followed by phy_reset assertion.<br>Note:<br>A transition on this input must be followed by the assertion of phy_reset. |
| 1 | RW | 0x0 | ref_repeat_clk_en<br>Repeat reference clock enable<br>Enables the CMOS output clocks ref_repeat_clk_(p,m). This pair of clocks can be used as reference clocks for other on-chip PHYs. |
| 0 | RW | 0x0 | ref_clkdet_en<br>Reserved |

**PCIe3PHY_GRF_PHY1_CON7**

Address: Operational Base + offset (0x021C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | mpllb_ssc_en<br>Spread spectrum enable.<br>Enables spread-spectrum clock (SSC) generation on the mpllb_div_clk output. If the reference clock already has spread spectrum applied, mpllb_ssc_en must be de-asserted. These inputs can only be changed when the txX_mpll_en inputs for all lanes are de-asserted. |
| 4 | RW | 0x0 | mpllb_force_en<br>MPLLB force enable.<br>When asserted, the corresponding MPLL is forced to be powered up, irrespective of the txX_mpll_en input.<br>This input is used for applications where a free-running MPLL clock output is required. There are no restrictions on when the mpllb_force_en signal can be transitioned. If MPLL is not powered up, we recommend that you follow the txX_mpll_en controls as shown in the "MPLLA Configuration Settings Update Followed By a TX Power-state Change" figure in the "PHY Usage and Configuration" chapter. |
| 3:2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | mplla_ssc_en<br>Spread spectrum enable.<br>Enables spread-spectrum clock (SSC) generation on the mplla_div_clk output. If the reference clock already has spread spectrum applied, mplla_ssc_en must be de-asserted. These inputs can only be changed when the txX_mpll_en inputs for all lanes are de-asserted. |
| 0 | RW | 0x0 | mplla_force_en<br>MPLLA force enable.<br>When asserted, the corresponding MPLL is forced to be powered up, irrespective of the txX_mpll_en input.<br>This input is used for applications where a free-running MPLL clock output is required. There are no restrictions on when the mplla_force_en signal can be transitioned. If MPLL is not powered up, we recommend that you follow the txX_mpll_en controls as shown in the "MPLLA Configuration Settings Update Followed By a TX Power-state Change" figure in the "PHY Usage and Configuration" chapter. |

**PCIe3PHY_GRF_PHY1_CON8**

Address: Operational Base + offset (0x0220)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:5 | RO | 0x000 | reserved |
| 4 | RW | 0x1 | cr_para_sel<br>Control Register (CR) parallel interface select.<br>Controls selection between JTAG and CR interfaces:<br>1'b0: JTAG<br>1'b1: Control Register (CR)<br>This input can only be changed when the cr_para_clk and jtag_tck clock inputs are disabled. |
| 3:2 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | sram_ext_ld_done<br>SRAM external load done.<br>Signal asserted by user after any updates to the SRAM have been loaded.<br>For the full signal description, refer to the PHY Databook, "Signal Descriptions" chapter. |
| 0 | RW | 0x1 | sram_bypass<br>SRAM bypass control signal when asserted, bypasses the SRAM interface.<br>In this case, the adaptation and calibration algorithms are executed from the hard-wired values within the Raw PCS.<br>If SRAM is not bypassed, the internal algorithms are first loaded by Raw PCS into the SRAM at which point user can change the contents of the SRAM. The updated SRAM contents are used for the adaptation and calibration routines.<br>This signal is meant to be used only for debugging purposes and must not change after phy_reset is negated.<br>For the full signal description, refer to the PHY Databook, "Signal Descriptions" chapter. |

**PCIe3PHY_GRF_PHY1_CON9**

Address: Operational Base + offset (0x0224)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | lane1_rx2tx_par_lb_en<br>Parallel (RX to TX) loopback enable.<br>When this signal is asserted, recovered parallel data from the receiver is looped back to the transmit serializer. |
| 0 | RW | 0x0 | lane0_rx2tx_par_lb_en<br>Parallel (RX to TX) loopback enable.<br>When this signal is asserted, recovered parallel data from the receiver is looped back to the transmit serializer. |

**PCIe3PHY_GRF_CMN_STATUS0**

Address: Operational Base + offset (0x0800)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RO | 0x1 | upcs_pwr_en<br>Power enables for PCS power switch(es).<br>Enable signal for external switch(es) to supply power to the power-gated logic in the PCS.<br>For information about power gating, see "Power Gating Support" section. |
| 0 | RO | 0x0 | phy_rtune_ack<br>Resistor tune acknowledgement.<br>Indicates that a resistor tune request is completed for all PHYN. |

**PCIe3PHY_GRF_PHY0_STATUS0**

Address: Operational Base + offset (0x0900)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:15 | RO | 0x00000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14 | RO | 0x0 | rx1_ppm_drift_vld<br>Reserved |
| 13:9 | RO | 0x00 | reserved |
| 8 | RO | 0x0 | rx1_ppm_drift<br>Reserved |
| 7 | RO | 0x0 | reserved |
| 6 | RO | 0x0 | rx0_ppm_drift_vld<br>Reserved |
| 5:0 | RO | 0x00 | rx0_ppm_drift<br>Reserved |

**PCIe3PHY_GRF_PHY0_STATUS1**

Address: Operational Base + offset (0x0904)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6 | RO | 0x0 | mpllb_state<br>Connects to the mpllb_state signal on PHYN.<br>For the full signal description, refer to the PHY databook, "Signal Descriptions" chapter. |
| 5:4 | RO | 0x0 | reserved |
| 3 | RO | 0x0 | mplla_state<br>Connects to the mplla_state signal on PHYN.<br>For the full signal description, refer to the PHY databook, "Signal Descriptions" chapter. |
| 2 | RO | 0x1 | pma_pwr_en<br>Power enable for PMA power switch.<br>Enable signal for PMA power switch (external) to supply power to the PMA.<br>For more information see "Power Gating" in the "PHY Usage and Configuration" chapter. |
| 1 | RO | 0x1 | pcs_pwr_en<br>Power enable for Raw PCS power switches.<br>Enable signal for external switches to supply power to the power gated logic in Raw PCS.<br>For more information see "Power Gating" in the "PHY Usage and Configuration" chapter. |
| 0 | RO | 0x0 | sram_init_done<br>SRAM Initialization done.<br>Signal indicating that the SRAM has been initialized by the boot loader in the Raw PCS.<br>This signal will not assert if sram_bypass is asserted.<br>For the full signal description, refer to the PHY databook, "Signal Descriptions" chapter |

**PCIe3PHY_GRF_PHY0_STATUS2**

Address: Operational Base + offset (0x0908)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3 | RO | 0x0 | rx0_align_detect<br>RX ALIGN symbol detected for lane X; PIPE 4.3 signal "AlignDetect" (Sec 6.1, PIPE 4.3).<br>Indicates receiver detection of an Align. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2:1 | RO | 0x2 | pipe_lane0_databuswidth<br>Bus width configuration for lane X; PIPE 4.3 signal "DataBusWidth[1:0]" (Sec 6.1, PIPE 4.3). This field reports the width of the data bus configured for the PHY. |
| 0 | RO | 0x0 | pipe_lane0_clkack_n<br>Clock acknowledge for lane X.<br>This is a side-band signal needed for the PIPE 4.2 controller to enter and exit P1.CPM, P1.1, and P1.2 power states.<br>For information about using this signal, see "PCIe L1 Substate Transitions" section.<br>When integrating with a PIPE 4.3 controller, this output can be ignored. |

**PCIe3PHY_GRF_PHY0_STATUS3**

Address: Operational Base + offset (0x090C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3 | RO | 0x0 | rx1_align_detect<br>RX ALIGN symbol detected for lane X; PIPE 4.3 signal "AlignDetect" (Sec 6.1, PIPE 4.3).<br>Indicates receiver detection of an Align. |
| 2:1 | RO | 0x2 | pipe_lane1_databuswidth<br>Bus width configuration for lane X; PIPE 4.3 signal "DataBusWidth[1:0]" (Sec 6.1, PIPE 4.3). This field reports the width of the data bus configured for the PHY. |
| 0 | RO | 0x0 | pipe_lane1_clkack_n<br>Clock acknowledge for lane X.<br>This is a side-band signal needed for the PIPE 4.2 controller to enter and exit P1.CPM, P1.1, and P1.2 power states.<br>For information about using this signal, see "PCIe L1 Substate Transitions" section.<br>When integrating with a PIPE 4.3 controller, this output can be ignored. |

**PCIe3PHY_GRF_PHY0_STATUS4**

Address: Operational Base + offset (0x0910)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x00 | reserved |
| 24:16 | RO | 0x000 | rx1_ebuff_location<br>Entries in elastic buffer for lane X; PIPE 4.3 signal "ElasticBufferLocation[8:0]" (Sec 6.1, PIPE 4.3).<br>Encodes the number of entries currently in the elastic buffer. |
| 15:9 | RO | 0x00 | reserved |
| 8:0 | RO | 0x000 | rx0_ebuff_location<br>Entries in elastic buffer for lane X; PIPE 4.3 signal "ElasticBufferLocation[8:0]" (Sec 6.1, PIPE 4.3).<br>Encodes the number of entries currently in the elastic buffer. |

**PCIe3PHY_GRF_PHY1_STATUS0**

Address: Operational Base + offset (0x0A00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:15 | RO | 0x00000 | reserved |
| 14 | RO | 0x0 | rx1_ppm_drift_vld<br>Reserved |
| 13:9 | RO | 0x00 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RO | 0x0 | rx1_ppm_drift<br>Reserved |
| 7 | RO | 0x0 | reserved |
| 6 | RO | 0x0 | rx0_ppm_drift_vld<br>Reserved |
| 5:0 | RO | 0x00 | rx0_ppm_drift<br>Reserved |

**PCIe3PHY_GRF_PHY1_STATUS1**

Address: Operational Base + offset (0x0A04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6 | RO | 0x0 | mpllb_state<br>Connects to the mpllb_state signal on PHYN.<br>For the full signal description, refer to the PHY databook, "Signal Descriptions" chapter. |
| 5:4 | RO | 0x0 | reserved |
| 3 | RO | 0x0 | mplla_state<br>Connects to the mplla_state signal on PHYN.<br>For the full signal description, refer to the PHY databook, "Signal Descriptions" chapter. |
| 2 | RO | 0x1 | pma_pwr_en<br>Power enable for PMA power switch.<br>Enable signal for PMA power switch (external) to supply power to the PMA.<br>For more information see "Power Gating" in the "PHY Usage and Configuration" chapter. |
| 1 | RO | 0x1 | pcs_pwr_en<br>Power enable for Raw PCS power switches.<br>Enable signal for external switches to supply power to the power gated logic in Raw PCS.<br>For more information see "Power Gating" in the "PHY Usage and Configuration" chapter. |
| 0 | RO | 0x0 | sram_init_done<br>SRAM Initialization done.<br>Signal indicating that the SRAM has been initialized by the boot loader in the Raw PCS.<br>This signal will not assert if sram_bypass is asserted.<br>For the full signal description, refer to the PHY databook, "Signal Descriptions" chapter |

**PCIe3PHY_GRF_PHY1_STATUS2**

Address: Operational Base + offset (0x0A08)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3 | RO | 0x0 | rx0_align_detect<br>RX ALIGN symbol detected for lane X; PIPE 4.3 signal "AlignDetect" (Sec 6.1, PIPE 4.3).<br>Indicates receiver detection of an Align. |
| 2:1 | RO | 0x2 | pipe_lane0_databuswidth<br>Bus width configuration for lane X; PIPE 4.3 signal "DataBusWidth[1:0]" (Sec 6.1, PIPE 4.3). This field reports the width of the data bus configured for the PHY. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RO | 0x0 | pipe_lane0_clkack_n<br>Clock acknowledge for lane X.<br>This is a side-band signal needed for the PIPE 4.2 controller to enter and exit P1.CPM, P1.1, and P1.2 power states.<br>For information about using this signal, see "PCIe L1 Substate Transitions" section.<br>When integrating with a PIPE 4.3 controller, this output can be ignored. |

**PCIe3PHY_GRF_PHY1_STATUS3**

Address: Operational Base + offset (0x0A0C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3 | RO | 0x0 | rx1_align_detect<br>RX ALIGN symbol detected for lane X; PIPE 4.3 signal "AlignDetect" (Sec 6.1, PIPE 4.3).<br>Indicates receiver detection of an Align. |
| 2:1 | RO | 0x2 | pipe_lane1_databuswidth<br>Bus width configuration for lane X; PIPE 4.3 signal "DataBusWidth[1:0]" (Sec 6.1, PIPE 4.3). This field reports the width of the data bus configured for the PHY. |
| 0 | RO | 0x0 | pipe_lane1_clkack_n<br>Clock acknowledge for lane X.<br>This is a side-band signal needed for the PIPE 4.2 controller to enter and exit P1.CPM, P1.1, and P1.2 power states.<br>For information about using this signal, see "PCIe L1 Substate Transitions" section.<br>When integrating with a PIPE 4.3 controller, this output can be ignored. |

**PCIe3PHY_GRF_PHY1_STATUS4**

Address: Operational Base + offset (0x0A10)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x00 | reserved |
| 24:16 | RO | 0x000 | rx1_ebuff_location<br>Entries in elastic buffer for lane X; PIPE 4.3 signal "ElasticBufferLocation[8:0]" (Sec 6.1, PIPE 4.3).<br>Encodes the number of entries currently in the elastic buffer. |
| 15:9 | RO | 0x00 | reserved |
| 8:0 | RO | 0x000 | rx0_ebuff_location<br>Entries in elastic buffer for lane X; PIPE 4.3 signal "ElasticBufferLocation[8:0]" (Sec 6.1, PIPE 4.3).<br>Encodes the number of entries currently in the elastic buffer. |

**PCIe3PHY_GRF_PHY0_LN0_CON0**

Address: Operational Base + offset (0x1000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:8 | RW | 0x3 | powerdown<br>Power state for lane X; PIPE 4.3 signal "PowerDown[3:0]" (Sec 6.1, PIPE 4.3).<br>Controls the PHY power states.<br>The power-state mapping is as follows:<br>4'h0: P0<br>4'h1: P0s<br>4'h2: P1<br>4'h3: P2<br>4'h4: P1.CPM<br>4'h5: P1.1<br>4'h6: P1.2<br>4'h7: P2.CPM<br>For information about power state transitions, see "Power State Transitions" section. |
| 7 | RO | 0x0 | reserved |
| 6 | RW | 0x0 | clkreq_n<br>Clock request for lane X.<br>This is a side-band signal that a PIPE 4.2 controller needs to enter and exit P1.CPM, P1.1, and P1.2 power states.<br>For information about using this signal, see "PCIe L1 Substate Transitions" section.<br>When integrating with a PIPE 4.3-compliant controller, set this input to an asserted value of 0. |
| 5 | RW | 0x0 | tx2rx_loopbk<br>TX-to-RX loopback enable for lane X.<br>When asserted, this input turns on the TX-to-RX serial loopback within the PHY.<br>This signal is for debug purposes only. |
| 4 | RW | 0x1 | mpll_mode<br>Reserved |
| 3:0 | RW | 0x0 | lane0_link_num<br>Reserved |

**PCIe3PHY_GRF_PHY0_LN0_CON1**

Address: Operational Base + offset (0x1004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | rxX_standby<br>RX standby enable for lane X; PIPE 4.3 signal "RxStandby" (Sec 6.1, PIPE 4.3).<br>When asserted, the RX CDR for lane X is disabled. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x1 | rxX_cmn_refclk_mode<br>RX common reference clock mode for lane X.<br>This mode should be enabled only when the far-end and near-end devices are running with a common reference clock. When asserted, this input configures the elastic buffer to operate in the lowest latency mode.<br>Note:<br>SKP symbol manipulation is disabled in this mode, because SKP symbol manipulation is not needed when the reference clock is common between near-end and far-end (that is, local clock and recovered clock have the same frequency).<br>Any change to this input must be followed by phy_reset assertion. |
| 6 | RW | 0x0 | rxX_sris_mode_en<br>RX SRIS ECM mode enable for lane X.<br>When asserted, this input configures the PHY CDR and the elastic buffer to recover Independent Spread Spectrum Data.<br>Note: Any change to this input must be followed by phy_reset assertion. |
| 5 | RW | 0x1 | rxX_termination<br>RX termination enable for lane X; PIPE 4.3 signal "RX Termination" (Sec 6.1, PIPE 4.3).<br>When asserted, the RX terminations are enabled. |
| 4 | RW | 0x0 | rxX_disable<br>RX disable control for lane X.<br>This is a side-band signal that a PIPE 4.2 controller needs to enter and exit P1.1 and P1.2 power states. When asserted, all RX lane circuitry (including RX Electrical Idle Exit Detection) for lane X is disabled.<br>When integrating with a PIPE 4.3 controller, pcs_rxX_disable must be set to 0.<br>For P1.1 and P1.2 entry and exit sequences, see "PCIe L1 Substate Transitions" section. |
| 3 | RW | 0x0 | rxX_eb_empty_mode<br>I Elastic buffer mode for lane X; PIPE 4.3 signal "Elasticity Buffer Mode" (Sec 6.1, PIPE 4.3).<br>Selects Elasticity Buffer operating mode.<br>1'b0: Nominal Half-Full Buffer mode<br>1'b1: Hybrid Pipe Buffer Mode<br>Note: Any change to this input must be followed by phy_reset assertion. |
| 2 | RW | 0x0 | txX_compliance<br>TX compliance for lane X; PIPE 4.3 signal "TxCompliance" (Sec 6.1,PIPE 4.3).<br>Sets the running disparity to negative. |
| 1 | RW | 0x0 | txX_elecidle<br>TX electrical idle enable for lane X; PIPE 4.3 signal "TxElecIdle" (Sec 6.1, PIPE 4.3).<br>When asserted (except during loopback), forces TX output to electrical idle. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | txX_disable<br>Transmitter disable.<br>This is a side-band signal that a PIPE 4.2 controller needs to enter and exit P1.2 power state. When asserted, the TX common mode for lane X is disabled.<br>When integrating with a PIPE 4.3 controller, pcs_txX_disable must be set to 0.<br>For P1.2 entry and exit sequences, see "PCIe L1 Substate Transitions" section. |

**PCIe3PHY_GRF_PHY0_LN0_CON2**

Address: Operational Base + offset (0x1008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5:0 | RW | 0x00 | rxX_idle_los_cnt_g1<br>These pins provide a control to disable the CDR in PCIE GEN1 mode when there is electrical idle on rx line without EIOS.<br>It is recommended that you control this signal in your SoC register with default value 000000 (disabled).<br>Note: When 000000, the feature is disabled. The other values decide the duration of electrical idle which should be conceived as EIOS by PHY in terms of PCS_CLK. |

**PCIe3PHY_GRF_PHY0_LN0_CON3**

Address: Operational Base + offset (0x100C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | reserved<br>reserved |

**PCIe3PHY_GRF_PHY0_LN0_CON4**

Address: Operational Base + offset (0x1010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x0 | sel_rxX_standby<br>Override enable for rxX_standby.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |
| 5 | RW | 0x0 | sel_rxX_disable<br>Override enable for rxX_disable.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |
| 4 | RW | 0x0 | sel_rxX_eb_empty_mode<br>Override enable for rxX_eb_empty_mode.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |
| 3 | RW | 0x0 | sel_txX_compliance<br>Override enable for txX_compliance.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | sel_txX_elecidle<br>Override enable for txX_elecidle.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |
| 1 | RW | 0x0 | sel_txX_disable<br>Override enable for txX_disable.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |
| 0 | RW | 0x0 | sel_powerdown<br>Override enable for powerdown.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |

**PCIe3PHY_GRF_PHY0_LN1_CON0**

Address: Operational Base + offset (0x1100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11:8 | RW | 0x3 | powerdown<br>Power state for lane X; PIPE 4.3 signal "PowerDown[3:0]" (Sec 6.1, PIPE 4.3).<br>Controls the PHY power states.<br>The power-state mapping is as follows:<br>4'h0: P0<br>4'h1: P0s<br>4'h2: P1<br>4'h3: P2<br>4'h4: P1.CPM<br>4'h5: P1.1<br>4'h6: P1.2<br>4'h7: P2.CPM<br>For information about power state transitions, see "Power State Transitions" section. |
| 7 | RO | 0x0 | reserved |
| 6 | RW | 0x0 | clkreq_n<br>Clock request for lane X.<br>This is a side-band signal that a PIPE 4.2 controller needs to enter and exit P1.CPM, P1.1, and P1.2 power states.<br>For information about using this signal, see "PCIe L1 Substate Transitions" section.<br>When integrating with a PIPE 4.3-compliant controller, set this input to an asserted value of 0. |
| 5 | RW | 0x0 | tx2rx_loopbk<br>TX-to-RX loopback enable for lane X.<br>When asserted, this input turns on the TX-to-RX serial loopback within the PHY.<br>This signal is for debug purposes only. |
| 4 | RW | 0x1 | mpll_mode<br>Reserved |
| 3:0 | RW | 0x0 | lane0_link_num<br>Reserved |

Rockchip Confidencial

**PCIe3PHY_GRF_PHY0_LN1_CON1**

Address: Operational Base + offset (0x1104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | rxX_standby<br>RX standby enable for lane X; PIPE 4.3 signal "RxStandby" (Sec 6.1, PIPE 4.3).<br>When asserted, the RX CDR for lane X is disabled. |
| 7 | RW | 0x1 | rxX_cmn_refclk_mode<br>RX common reference clock mode for lane X.<br>This mode should be enabled only when the far-end and near-end devices are running with a common reference clock. When asserted, this input configures the elastic buffer to operate in the lowest latency mode.<br>Note:<br>SKP symbol manipulation is disabled in this mode, because SKP symbol manipulation is not needed when the reference clock is common between near-end and far-end (that is, local clock and recovered clock have the same frequency).<br>Any change to this input must be followed by phy_reset assertion. |
| 6 | RW | 0x0 | rxX_sris_mode_en<br>RX SRIS ECM mode enable for lane X.<br>When asserted, this input configures the PHY CDR and the elastic buffer to recover Independent Spread Spectrum Data.<br>Note: Any change to this input must be followed by phy_reset assertion. |
| 5 | RW | 0x1 | rxX_termination<br>RX termination enable for lane X; PIPE 4.3 signal "RX Termination" (Sec 6.1, PIPE 4.3).<br>When asserted, the RX terminations are enabled. |
| 4 | RW | 0x0 | rxX_disable<br>RX disable control for lane X.<br>This is a side-band signal that a PIPE 4.2 controller needs to enter and exit P1.1 and P1.2 power states. When asserted, all RX lane circuitry (including RX Electrical Idle Exit Detection) for lane X is disabled.<br>When integrating with a PIPE 4.3 controller, pcs_rxX_disable must be set to 0.<br>For P1.1 and P1.2 entry and exit sequences, see "PCIe L1 Substate Transitions" section. |
| 3 | RW | 0x0 | rxX_eb_empty_mode<br>I Elastic buffer mode for lane X; PIPE 4.3 signal "Elasticity Buffer Mode" (Sec 6.1, PIPE 4.3).<br>Selects Elasticity Buffer operating mode.<br>1'b0: Nominal Half-Full Buffer mode<br>1'b1: Hybrid Pipe Buffer Mode<br>Note: Any change to this input must be followed by phy_reset assertion. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | txX_compliance<br>TX compliance for lane X; PIPE 4.3 signal "TxCompliance" (Sec 6.1,PIPE 4.3).<br>Sets the running disparity to negative. |
| 1 | RW | 0x0 | txX_elecidle<br>TX electrical idle enable for lane X; PIPE 4.3 signal "TxElecIdle" (Sec 6.1, PIPE 4.3).<br>When asserted (except during loopback), forces TX output to electrical idle. |
| 0 | RW | 0x0 | txX_disable<br>Transmitter disable.<br>This is a side-band signal that a PIPE 4.2 controller needs to enter and exit P1.2 power state. When asserted, the TX common mode for lane X is disabled.<br>When integrating with a PIPE 4.3 controller, pcs_txX_disable must be set to 0.<br>For P1.2 entry and exit sequences, see "PCIe L1 Substate Transitions" section. |

**PCIe3PHY_GRF_PHY0_LN1_CON2**

Address: Operational Base + offset (0x1108)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5:0 | RW | 0x00 | rxX_idle_los_cnt_g1<br>These pins provide a control to disable the CDR in PCIE GEN1 mode when there is electrical idle on rx line without EIOS.<br>It is recommended that you control this signal in your SoC register with default value 000000 (disabled).<br>Note: When 000000, the feature is disabled. The other values decide the duration of electrical idle which should be conceived as EIOS by PHY in terms of PCS_CLK. |

**PCIe3PHY_GRF_PHY0_LN1_CON3**

Address: Operational Base + offset (0x110C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | reserved<br>reserved |

**PCIe3PHY_GRF_PHY0_LN1_CON4**

Address: Operational Base + offset (0x1110)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x0 | sel_rxX_standby<br>Override enable for rxX_standby.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | sel_rxX_disable<br>Override enable for rxX_disable.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |
| 4 | RW | 0x0 | sel_rxX_eb_empty_mode<br>Override enable for rxX_eb_empty_mode.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |
| 3 | RW | 0x0 | sel_txX_compliance<br>Override enable for txX_compliance.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |
| 2 | RW | 0x0 | sel_txX_elecidle<br>Override enable for txX_elecidle.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |
| 1 | RW | 0x0 | sel_txX_disable<br>Override enable for txX_disable.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |
| 0 | RW | 0x0 | sel_powerdown<br>Override enable for powerdown.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |

**PCIe3PHY_GRF_PHY1_LN0_CON0**

Address: Operational Base + offset (0x2000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11:8 | RW | 0x3 | powerdown<br>Power state for lane X; PIPE 4.3 signal "PowerDown[3:0]" (Sec 6.1, PIPE 4.3).<br>Controls the PHY power states.<br>The power-state mapping is as follows:<br>4'h0: P0<br>4'h1: P0s<br>4'h2: P1<br>4'h3: P2<br>4'h4: P1.CPM<br>4'h5: P1.1<br>4'h6: P1.2<br>4'h7: P2.CPM<br>For information about power state transitions, see "Power State Transitions" section. |
| 7 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | clkreq_n<br>Clock request for lane X.<br>This is a side-band signal that a PIPE 4.2 controller needs to enter and exit P1.CPM, P1.1, and P1.2 power states.<br>For information about using this signal, see "PCIe L1 Substate Transitions" section.<br>When integrating with a PIPE 4.3-compliant controller, set this input to an asserted value of 0. |
| 5 | RW | 0x0 | tx2rx_loopbk<br>TX-to-RX loopback enable for lane X.<br>When asserted, this input turns on the TX-to-RX serial loopback within the PHY.<br>This signal is for debug purposes only. |
| 4 | RW | 0x1 | mpll_mode<br>Reserved |
| 3:0 | RW | 0x0 | lane0_link_num<br>Reserved |

**PCIe3PHY_GRF_PHY1_LN0_CON1**

Address: Operational Base + offset (0x2004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | rxX_standby<br>RX standby enable for lane X; PIPE 4.3 signal "RxStandby" (Sec 6.1, PIPE 4.3).<br>When asserted, the RX CDR for lane X is disabled. |
| 7 | RW | 0x1 | rxX_cmn_refclk_mode<br>RX common reference clock mode for lane X.<br>This mode should be enabled only when the far-end and near-end devices are running with a common reference clock. When asserted, this input configures the elastic buffer to operate in the lowest latency mode.<br>Note:<br>SKP symbol manipulation is disabled in this mode, because SKP symbol manipulation is not needed when the reference clock is common between near-end and far-end (that is, local clock and recovered clock have the same frequency).<br>Any change to this input must be followed by phy_reset assertion. |
| 6 | RW | 0x0 | rxX_sris_mode_en<br>RX SRIS ECM mode enable for lane X.<br>When asserted, this input configures the PHY CDR and the elastic buffer to recover Independent Spread Spectrum Data.<br>Note: Any change to this input must be followed by phy_reset assertion. |
| 5 | RW | 0x1 | rxX_termination<br>RX termination enable for lane X; PIPE 4.3 signal "RX Termination" (Sec 6.1, PIPE 4.3).<br>When asserted, the RX terminations are enabled. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | rxX_disable<br>RX disable control for lane X.<br>This is a side-band signal that a PIPE 4.2 controller needs to enter and exit P1.1 and P1.2 power states. When asserted, all RX lane circuitry (including RX Electrical Idle Exit Detection) for lane X is disabled.<br>When integrating with a PIPE 4.3 controller, pcs_rxX_disable must be set to 0.<br>For P1.1 and P1.2 entry and exit sequences, see "PCIe L1 Substate Transitions" section. |
| 3 | RW | 0x0 | rxX_eb_empty_mode<br>I Elastic buffer mode for lane X; PIPE 4.3 signal "Elasticity Buffer Mode" (Sec 6.1, PIPE 4.3).<br>Selects Elasticity Buffer operating mode.<br>1'b0: Nominal Half-Full Buffer mode<br>1'b1: Hybrid Pipe Buffer Mode<br>Note: Any change to this input must be followed by phy_reset assertion. |
| 2 | RW | 0x0 | txX_compliance<br>TX compliance for lane X; PIPE 4.3 signal "TxCompliance" (Sec 6.1,PIPE 4.3).<br>Sets the running disparity to negative. |
| 1 | RW | 0x0 | txX_elecidle<br>TX electrical idle enable for lane X; PIPE 4.3 signal "TxElecIdle" (Sec 6.1, PIPE 4.3).<br>When asserted (except during loopback), forces TX output to electrical idle. |
| 0 | RW | 0x0 | txX_disable<br>Transmitter disable.<br>This is a side-band signal that a PIPE 4.2 controller needs to enter and exit P1.2 power state. When asserted, the TX common mode for lane X is disabled.<br>When integrating with a PIPE 4.3 controller, pcs_txX_disable must be set to 0.<br>For P1.2 entry and exit sequences, see "PCIe L1 Substate Transitions" section. |

**PCIe3PHY_GRF_PHY1_LN0_CON2**

Address: Operational Base + offset (0x2008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5:0 | RW | 0x00 | rxX_idle_los_cnt_g1<br>These pins provide a control to disable the CDR in PCIE GEN1 mode when there is electrical idle on rx line without EIOS.<br>It is recommended that you control this signal in your SoC register with default value 000000 (disabled).<br>Note: When 000000, the feature is disabled. The other values decide the duration of electrical idle which should be conceived as EIOS by PHY in terms of PCS_CLK. |

**PCIe3PHY_GRF_PHY1_LN0_CON3**

Rockchip Confidencial

Address: Operational Base + offset (0x200C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | reserved<br>reserved |

**PCIe3PHY_GRF_PHY1_LN0_CON4**

Address: Operational Base + offset (0x2010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x0 | sel_rxX_standby<br>Override enable for rxX_standby.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |
| 5 | RW | 0x0 | sel_rxX_disable<br>Override enable for rxX_disable.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |
| 4 | RW | 0x0 | sel_rxX_eb_empty_mode<br>Override enable for rxX_eb_empty_mode.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |
| 3 | RW | 0x0 | sel_txX_compliance<br>Override enable for txX_compliance.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |
| 2 | RW | 0x0 | sel_txX_elecidle<br>Override enable for txX_elecidle.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |
| 1 | RW | 0x0 | sel_txX_disable<br>Override enable for txX_disable.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |
| 0 | RW | 0x0 | sel_powerdown<br>Override enable for powerdown.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |

**PCIe3PHY_GRF_PHY1_LN1_CON0**

Address: Operational Base + offset (0x2100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:8 | RW | 0x3 | powerdown<br>Power state for lane X; PIPE 4.3 signal "PowerDown[3:0]" (Sec 6.1, PIPE 4.3).<br>Controls the PHY power states.<br>The power-state mapping is as follows:<br>4'h0: P0<br>4'h1: P0s<br>4'h2: P1<br>4'h3: P2<br>4'h4: P1.CPM<br>4'h5: P1.1<br>4'h6: P1.2<br>4'h7: P2.CPM<br>For information about power state transitions, see "Power State Transitions" section. |
| 7 | RO | 0x0 | reserved |
| 6 | RW | 0x0 | clkreq_n<br>Clock request for lane X.<br>This is a side-band signal that a PIPE 4.2 controller needs to enter and exit P1.CPM, P1.1, and P1.2 power states.<br>For information about using this signal, see "PCIe L1 Substate Transitions" section.<br>When integrating with a PIPE 4.3-compliant controller, set this input to an asserted value of 0. |
| 5 | RW | 0x0 | tx2rx_loopbk<br>TX-to-RX loopback enable for lane X.<br>When asserted, this input turns on the TX-to-RX serial loopback within the PHY.<br>This signal is for debug purposes only. |
| 4 | RW | 0x1 | mpll_mode<br>Reserved |
| 3:0 | RW | 0x0 | lane0_link_num<br>Reserved |

**PCIe3PHY_GRF_PHY1_LN1_CON1**

Address: Operational Base + offset (0x2104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | rxX_standby<br>RX standby enable for lane X; PIPE 4.3 signal "RxStandby" (Sec 6.1, PIPE 4.3).<br>When asserted, the RX CDR for lane X is disabled. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x1 | rxX_cmn_refclk_mode<br>RX common reference clock mode for lane X.<br>This mode should be enabled only when the far-end and near-end devices are running with a common reference clock. When asserted, this input configures the elastic buffer to operate in the lowest latency mode.<br>Note:<br>SKP symbol manipulation is disabled in this mode, because SKP symbol manipulation is not needed when the reference clock is common between near-end and far-end (that is, local clock and recovered clock have the same frequency).<br>Any change to this input must be followed by phy_reset assertion. |
| 6 | RW | 0x0 | rxX_sris_mode_en<br>RX SRIS ECM mode enable for lane X.<br>When asserted, this input configures the PHY CDR and the elastic buffer to recover Independent Spread Spectrum Data.<br>Note: Any change to this input must be followed by phy_reset assertion. |
| 5 | RW | 0x1 | rxX_termination<br>RX termination enable for lane X; PIPE 4.3 signal "RX Termination" (Sec 6.1, PIPE 4.3).<br>When asserted, the RX terminations are enabled. |
| 4 | RW | 0x0 | rxX_disable<br>RX disable control for lane X.<br>This is a side-band signal that a PIPE 4.2 controller needs to enter and exit P1.1 and P1.2 power states. When asserted, all RX lane circuitry (including RX Electrical Idle Exit Detection) for lane X is disabled.<br>When integrating with a PIPE 4.3 controller, pcs_rxX_disable must be set to 0.<br>For P1.1 and P1.2 entry and exit sequences, see "PCIe L1 Substate Transitions" section. |
| 3 | RW | 0x0 | rxX_eb_empty_mode<br>I Elastic buffer mode for lane X; PIPE 4.3 signal "Elasticity Buffer Mode" (Sec 6.1, PIPE 4.3).<br>Selects Elasticity Buffer operating mode.<br>1'b0: Nominal Half-Full Buffer mode<br>1'b1: Hybrid Pipe Buffer Mode<br>Note: Any change to this input must be followed by phy_reset assertion. |
| 2 | RW | 0x0 | txX_compliance<br>TX compliance for lane X; PIPE 4.3 signal "TxCompliance" (Sec 6.1,PIPE 4.3).<br>Sets the running disparity to negative. |
| 1 | RW | 0x0 | txX_elecidle<br>TX electrical idle enable for lane X; PIPE 4.3 signal "TxElecIdle" (Sec 6.1, PIPE 4.3).<br>When asserted (except during loopback), forces TX output to electrical idle. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | txX_disable<br>Transmitter disable.<br>This is a side-band signal that a PIPE 4.2 controller needs to enter and exit P1.2 power state. When asserted, the TX common mode for lane X is disabled.<br>When integrating with a PIPE 4.3 controller, pcs_txX_disable must be set to 0.<br>For P1.2 entry and exit sequences, see "PCIe L1 Substate Transitions" section. |

**PCIe3PHY_GRF_PHY1_LN1_CON2**

Address: Operational Base + offset (0x2108)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5:0 | RW | 0x00 | rxX_idle_los_cnt_g1<br>These pins provide a control to disable the CDR in PCIE GEN1 mode when there is electrical idle on rx line without EIOS.<br>It is recommended that you control this signal in your SoC register with default value 000000 (disabled).<br>Note: When 000000, the feature is disabled. The other values decide the duration of electrical idle which should be conceived as EIOS by PHY in terms of PCS_CLK. |

**PCIe3PHY_GRF_PHY1_LN1_CON3**

Address: Operational Base + offset (0x210C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | reserved<br>reserved |

**PCIe3PHY_GRF_PHY1_LN1_CON4**

Address: Operational Base + offset (0x2110)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x0 | sel_rxX_standby<br>Override enable for rxX_standby.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |
| 5 | RW | 0x0 | sel_rxX_disable<br>Override enable for rxX_disable.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |
| 4 | RW | 0x0 | sel_rxX_eb_empty_mode<br>Override enable for rxX_eb_empty_mode.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | sel_txX_compliance<br>Override enable for txX_compliance.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |
| 2 | RW | 0x0 | sel_txX_elecidle<br>Override enable for txX_elecidle.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |
| 1 | RW | 0x0 | sel_txX_disable<br>Override enable for txX_disable.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |
| 0 | RW | 0x0 | sel_powerdown<br>Override enable for powerdown.<br>1'b0: PIPE signal from controller<br>1'b1: PIPE signal from PCIe30 PHY GRF |

**PCIe3PHY_GRF_PRT0_CON0**

Address: Operational Base + offset (0x3000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | ext_mplla_bandwidth<br>protocolP_ext_mplla_bandwidth is a PHY configuration setting perprotocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs.<br>(For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

**PCIe3PHY_GRF_PRT0_CON1**

Address: Operational Base + offset (0x3004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | ext_bs_rx_lowswing<br>protocolP_ext_bs_tx_lowswing is TX/RX boundary scan swing/level settings.<br>Sets the boundary scan swing and level settings for the PHY. These inputs are selected irrespective of the phy_ext_ctrl_sel setting.<br>For recommended values, see PHY databook, "PHY Usage and Configuration" chapter. |
| 5 | RW | 0x0 | ext_bs_rx_bigswing<br>protocolP_ext_bs_rx_bigswing is TX/RX boundary scan swing/level settings.<br>Sets the boundary scan swing and level settings for the PHY. These inputs are selected irrespective of the phy_ext_ctrl_sel setting.<br>For recommended values, see PHY databook, "PHY Usage and Configuration" chapter. |
| 4:0 | RW | 0x00 | ext_bs_rx_level<br>protocolP_ext_bs_rx_level is TX/RX boundary scan swing/level settings.<br>Sets the boundary scan swing and level settings for the PHY. These inputs are selected irrespective of the phy_ext_ctrl_sel setting.<br>For recommended values, see PHY databook, "PHY Usage and Configuration" chapter. |

**PCIe3PHY_GRF_PRT0_CON2**

Address: Operational Base + offset (0x3008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | ext_mplla_div_clk_en<br>protocolP_ext_mplla_div_clk_en is PHY configuration setting perprotocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs.<br>(For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RW | 0x0 | ext_mplla_div8_clk_en<br>protocolP_ext_mplla_div8_clk_en is PHY configuration setting perprotocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs.<br>(For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 8 | RW | 0x0 | ext_mplla_div10_clk_en<br>protocolP_ext_mplla_div10_clk_en is PHY configuration setting perprotocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs.<br>(For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 7:0 | RW | 0x00 | ext_mplla_div_multiplier<br>protocolP_ext_mplla_div_multiplier is PHY configuration setting perprotocol. External overrides for the per-protocol settings of the PHY<br>configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

**PCIe3PHY_GRF_PRT0_CON3**

Address: Operational Base + offset (0x300C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10:0 | RW | 0x000 | ext_mplla_fracn_ctrl<br>protocolP_ext_mplla_fracn_ctrl is a PHY configuration setting perprotocol. External overrides for the per-protocol settings of the PHY configuration inputs.<br>(For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signal correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

**PCIe3PHY_GRF_PRT0_CON4**

Address: Operational Base + offset (0x3010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10:8 | RW | 0x0 | ext_mplla_ssc_clk_sel<br>protocolP_ext_mplla_ssc_clk_sel is a PHY configuration setting perprotocol. External overrides for the per-protocol settings of the PHY configuration inputs.<br>(For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signal correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 7:0 | RW | 0x00 | ext_mplla_multiplier<br>protocolP_ext_mplla_multiplier is PHY configuration setting perprotocol. External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

**PCIe3PHY_GRF_PRT0_CON5**

Address: Operational Base + offset (0x3014)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | ext_mplla_ssc_freq_cnt_ovrd_en<br>protocolP_ext_mplla_ssc_freq_cnt_ovrd_en are MPLL frequency controls.<br>protocol*_ext_mpll{a,b}_ssc_freq_cnt_ovrd_en settings are independent of phy_ext_ctrl_sel.<br>Based on protocol*_ext_mplla_ssc_freq_cnt_ovrd_en, these settings are generated from internally generated values (from a LUT for SSC) in RAW PCS or from respective protocol* signals.<br>For recommended values, see PHY databook, "PHY Usage and Configuration" chapter. |
| 14:12 | RW | 0x0 | ext_mplla_ssc_range<br>protocolP_ext_mplla_ssc_range is a PHY configuration setting perprotocol. External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 11:0 | RW | 0x000 | ext_mplla_ssc_freq_cnt_init<br>protocolP_ext_mplla_ssc_freq_cnt_init[11:0] is PHY configuration setting per-protocol. External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration"chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signal correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

**PCIe3PHY_GRF_PRT0_CON6**

Address: Operational Base + offset (0x3018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | ext_mplla_word_div2_en<br>protocolP_ext_mplla_word_div2_en is a PHY configuration setting per-protocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter.)<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x0 | ext_mplla_tx_clk_div<br>protocolP_ext_mplla_tx_clk_div is PHY configuration setting per protocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 7:0 | RW | 0x00 | ext_mplla_ssc_freq_cnt_peak<br>protocolP_ext_mplla_ssc_freq_cnt_peak[7:0] is PHY configuration setting per-protocol. External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the Cores PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signal correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

**PCIe3PHY_GRF_PRT0_CON7**

Address: Operational Base + offset (0x301C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0000 | ext_mpllb_bandwidth<br>protocolP_ext_mpllb_bandwidth is a PHY configuration setting per-protocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

**PCIe3PHY_GRF_PRT0_CON8**

Address: Operational Base + offset (0x3020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | ext_mpllb_div_clk_en<br>protocolP_ext_mpllb_div_clk_en is PHY configuration setting perprotocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs.<br>(For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 9 | RW | 0x0 | ext_mpllb_div8_clk_en<br>protocolP_ext_mpllb_div8_clk_en is PHY configuration setting perprotocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs.<br>(For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | ext_mpllb_div10_clk_en<br>protocolP_ext_mpllb_div10_clk_en is PHY configuration setting perprotocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs.<br>(For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 7:0 | RW | 0x00 | ext_mpllb_div_multiplier<br>protocolP_ext_mpllb_div_multiplier is PHY configuration setting perprotocol. External overrides for the per-protocol settings of the PHY<br>configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

**PCIe3PHY_GRF_PRT0_CON9**

Address: Operational Base + offset (0x3024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10:0 | RW | 0x000 | ext_mpllb_fracn_ctrl<br>protocolP_ext_mpllb_fracn_ctrl is a PHY configuration setting perprotocol. External overrides for the per-protocol settings of the PHY configuration inputs.<br>(For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signal correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

**PCIe3PHY_GRF_PRT0_CON10**

Rockchip Confidential

Address: Operational Base + offset (0x3028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10:8 | RW | 0x0 | ext_mpllb_ssc_clk_sel<br>protocolP_ext_mpllb_ssc_clk_sel is a PHY configuration setting perprotocol. External overrides for the per-protocol settings of the PHY configuration inputs.<br>(For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signal correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 7:0 | RW | 0x00 | ext_mpllb_multiplier<br>protocolP_ext_mpllb_multiplier is PHY configuration setting perprotocol. External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

**PCIe3PHY_GRF_PRT0_CON11**

Address: Operational Base + offset (0x302C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | ext_mpllb_ssc_freq_cnt_ovrd_en<br>protocolP_ext_mpllb_ssc_freq_cnt_ovrd_en are MPLL frequency controls.<br>protocol*_ext_mpll{a,b}_ssc_freq_cnt_ovrd_en settings are independent of phy_ext_ctrl_sel.<br>Based on protocol*_ext_mpllb_ssc_freq_cnt_ovrd_en, these settings are generated from internally generated values (from a LUT for SSC) in RAW PCS or from respective protocol* signals.<br>For recommended values, see PHY databook, "PHY Usage and Configuration" chapter. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14:12 | RW | 0x0 | ext_mpllb_ssc_range<br>protocolP_ext_mpllb_ssc_range is a PHY configuration setting perprotocol. External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 11:0 | RW | 0x000 | ext_mpllb_ssc_freq_cnt_init<br>protocolP_ext_mpllb_ssc_freq_cnt_init[11:0] is PHY configuration setting per-protocol. External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration"chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signal correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

**PCIe3PHY_GRF_PRT0_CON12**

Address: Operational Base + offset (0x3030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | ext_mpllb_word_div2_en<br>protocolP_ext_mpllb_word_div2_en is a PHY configuration setting per-protocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter.)<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 11 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10:8 | RW | 0x0 | ext_mpllb_tx_clk_div<br>protocolP_ext_mpllb_tx_clk_div is PHY configuration setting per protocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 7:0 | RW | 0x00 | ext_mpllb_ssc_freq_cnt_peak<br>protocolP_ext_mpllb_ssc_freq_cnt_peak[7:0] is PHY configuration setting per-protocol. External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the Cores PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signal correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

**PCIe3PHY_GRF_PRT0_CON13**

Address: Operational Base + offset (0x3034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x0 | ext_ref_clk_mpllb_div2_en<br>protocolP_ext_ref_clk_mpllb_div2_en is a PHY configuration setting per-protocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter.)<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocol signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | ext_ref_clk_mplla_div2_en<br>protocolP_ext_ref_clk_mplla_div2_en is a PHY configuration setting per-protocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 3 | RW | 0x0 | ext_ref_clk_div2_en<br>protocolP_ext_ref_clk_div2_en is PHY configuration setting per protocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 2:0 | RW | 0x0 | ext_ref_range<br>protocolP_ext_ref_range is PHY configuration setting per-protocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

**PCIe3PHY_GRF_PRT0_CON14**

Address: Operational Base + offset (0x3038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 27:24 | RW | 0x0 | ext_rx_adapt_dfe_en_g3<br>protocolP_ext_rx_adapt_dfe_en_g3 is a receiver equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's RX equalization inputs. The PCS 3.0 internally determines the hardcoded optimal RX equalization settings for each protocol and rate.<br>However, these settings can be overwritten on a per-protocol basis from these top-level pins when the phy_ext_ctrl input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively. Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs. These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |
| 23:20 | RW | 0x0 | ext_rx_adapt_dfe_en_g2<br>protocolP_ext_rx_adapt_dfe_en_g2 is a receiver equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's RX equalization inputs. The PCS 3.0 internally determines the hardcoded optimal RX equalization settings for each protocol and rate.<br>However, these settings can be overwritten on a per-protocol basis from these top-level pins when the phy_ext_ctrl input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively. Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs. These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |
| 19:16 | RW | 0x0 | ext_rx_adapt_dfe_en_g1<br>protocolP_ext_rx_adapt_dfe_en_g1 is a receiver equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's RX equalization inputs. The PCS 3.0 internally determines the hardcoded optimal RX equalization settings for each protocol and rate.<br>However, these settings can be overwritten on a per-protocol basis from these top-level pins when the phy_ext_ctrl input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively. Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs. These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |
| 15:12 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:8 | RW | 0x0 | ext_rx_adapt_afe_en_g3<br>protocolP_ext_rx_adapt_afe_en_g3 is a receiver equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's RX equalization inputs. The PCS 3.0 internally determines the hardcoded optimal RX equalization settings for each protocol and rate.<br>However, these settings can be overwritten on a per-protocol basis from these top-level pins when the phy_ext_ctrl input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively. Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs. These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |
| 7:4 | RW | 0x0 | ext_rx_adapt_afe_en_g2<br>protocolP_ext_rx_adapt_afe_en_g2 is a receiver equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's RX equalization inputs. The PCS 3.0 internally determines the hardcoded optimal RX equalization settings for each protocol and rate.<br>However, these settings can be overwritten on a per-protocol basis from these top-level pins when the phy_ext_ctrl input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively. Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs. These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |
| 3:0 | RW | 0x0 | ext_rx_adapt_afe_en_g1<br>protocolP_ext_rx_adapt_afe_en_g1 is a receiver equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's RX equalization inputs. The PCS 3.0 internally determines the hardcoded optimal RX equalization settings for each protocol and rate.<br>However, these settings can be overwritten on a per-protocol basis from these top-level pins when the phy_ext_ctrl input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively. Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs. These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON15**

Address: Operational Base + offset (0x303C)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:10 | RW | 0x00 | ext_rx_cdr_ppm_max_g3<br>Reserved |
| 9:5 | RW | 0x00 | ext_rx_cdr_ppm_max_g2<br>Reserved |
| 4:0 | RW | 0x00 | ext_rx_cdr_ppm_max_g1<br>Reserved |

**PCIe3PHY_GRF_PRT0_CON16**

Address: Operational Base + offset (0x3040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5:4 | RW | 0x0 | ext_rx_cdr_vco_freqband_g3<br>Reserved |
| 3:2 | RW | 0x0 | ext_rx_cdr_vco_freqband_g2<br>Reserved |
| 1:0 | RW | 0x0 | ext_rx_cdr_vco_freqband_g1<br>Reserved |

**PCIe3PHY_GRF_PRT0_CON17**

Address: Operational Base + offset (0x3044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11:8 | RW | 0x0 | ext_rx_data_iq_g3<br>Reserved |
| 7:4 | RW | 0x0 | ext_rx_data_iq_g2<br>Reserved |
| 3:0 | RW | 0x0 | ext_rx_data_iq_g1<br>Reserved |

**PCIe3PHY_GRF_PRT0_CON18**

Address: Operational Base + offset (0x3048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | reserved |

**PCIe3PHY_GRF_PRT0_CON19**

Address: Operational Base + offset (0x304C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | reserved |

**PCIe3PHY_GRF_PRT0_CON20**

Address: Operational Base + offset (0x3050)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8:6 | RW | 0x0 | ext_rx_eq_ctle_pole_g3<br>Reserved |
| 5:3 | RW | 0x0 | ext_rx_eq_ctle_pole_g2<br>Reserved |
| 2:0 | RW | 0x0 | ext_rx_eq_ctle_pole_g1<br>Reserved |

**PCIe3PHY_GRF_PRT0_CON21**

Address: Operational Base + offset (0x3054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | reserved |

**PCIe3PHY_GRF_PRT0_CON22**

Address: Operational Base + offset (0x3058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | ext_rx_eq_vga1_gain_g2<br>Reserved |
| 11:8 | RW | 0x0 | ext_rx_eq_vga1_gain_g1<br>Reserved |
| 7:0 | RO | 0x00 | reserved |

**PCIe3PHY_GRF_PRT0_CON23**

Address: Operational Base + offset (0x305C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | ext_rx_eq_vga2_gain_g3<br>Reserved |
| 11:8 | RW | 0x0 | ext_rx_eq_vga2_gain_g2<br>Reserved |
| 7:4 | RW | 0x0 | ext_rx_eq_vga2_gain_g1<br>Reserved |
| 3:0 | RW | 0x0 | ext_rx_eq_vga1_gain_g3<br>Reserved |

**PCIe3PHY_GRF_PRT0_CON24**

Address: Operational Base + offset (0x3060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:4 | RW | 0x000 | ext_rx_los_threshold<br>protocolP_ext_rx_los_threshold is a PHY configuration setting per-protocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | ext_rx_los_lfps_en<br>protocolP_ext_rx_los_lfps_en is a PHY configuration setting per-protocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs.(For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 1:0 | RO | 0x0 | reserved |

**PCIe3PHY_GRF_PRT0_CON25**

Address: Operational Base + offset (0x3064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RW | 0x00 | ext_rx_misc_g2<br>Reserved |
| 7:0 | RW | 0x00 | ext_rx_misc_g1<br>Reserved |

**PCIe3PHY_GRF_PRT0_CON26**

Address: Operational Base + offset (0x3068)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7:0 | RW | 0x00 | ext_rx_misc_g3<br>Reserved |

Rockchip Confidential

**PCIe3PHY_GRF_PRT0_CON27**

Address: Operational Base + offset (0x306C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11:6 | RW | 0x00 | ext_rx_ref_ld_val_g2<br>protocolP_ext_rx_ref_ld_val_g2 is a PHY configuration setting per-protocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 5:0 | RW | 0x00 | ext_rx_ref_ld_val_g1<br>protocolP_ext_rx_ref_ld_val_g1 is a PHY configuration setting per-protocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

**PCIe3PHY_GRF_PRT0_CON28**

Address: Operational Base + offset (0x3070)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5:0 | RW | 0x00 | ext_rx_ref_ld_val_g3<br>protocolP_ext_rx_ref_ld_val_g3 is a PHY configuration setting pe-rprotocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

**PCIe3PHY_GRF_PRT0_CON29**

Address: Operational Base + offset (0x3074)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12:0 | RW | 0x0000 | ext_rx_vco_ld_val_g1<br>protocolP_ext_rx_vco_ld_val_g1 is a PHY configuration setting pe-rprotocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

**PCIe3PHY_GRF_PRT0_CON30**

Address: Operational Base + offset (0x3078)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12:0 | RW | 0x0000 | ext_rx_vco_ld_val_g2<br>protocolP_ext_rx_vco_ld_val_g2 is a PHY configuration setting pe-rprotocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

**PCIe3PHY_GRF_PRT0_CON31**

Address: Operational Base + offset (0x307C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12:0 | RW | 0x0000 | ext_rx_vco_ld_val_g3<br>protocolP_ext_rx_vco_ld_val_g3 is a PHY configuration setting pe-rprotocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

**PCIe3PHY_GRF_PRT0_CON32**

Address: Operational Base + offset (0x3080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12:8 | RW | 0x00 | ext_rx_vref_ctrl<br>protocolP_ext_rx_vref_ctrl is a PHY configuration setting pe-rprotocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 7:0 | RW | 0x00 | ext_sup_misc<br>Reserved |

**PCIe3PHY_GRF_PRT0_CON33**

Address: Operational Base + offset (0x3084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | reserved |

**PCIe3PHY_GRF_PRT0_CON34**

Address: Operational Base + offset (0x3088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | reserved |

**PCIe3PHY_GRF_PRT0_CON35**

Address: Operational Base + offset (0x308C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11:8 | RW | 0x0 | ext_tx_eq_ovrd_g3<br>protocolP_ext_tx_eq_ovrd_g3 is a transmitter equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's TX equalization inputs.<br>The PCS 3.0 internally determines the hard-coded optimal TX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these toplevel pins when the corresponding protocol[0,1,2]_ext_tx_eq_ovrd_[g1,g2,g3,g4] input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:4 | RW | 0x0 | ext_tx_eq_ovrd_g2<br>protocolP_ext_tx_eq_ovrd_g2 is a transmitter equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's TX equalization inputs.<br>The PCS 3.0 internally determines the hard-coded optimal TX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these toplevel pins when the corresponding protocol[0,1,2]_ext_tx_eq_ovrd_[g1,g2,g3,g4] input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |
| 3:0 | RW | 0x0 | ext_tx_eq_ovrd_g1<br>protocolP_ext_tx_eq_ovrd_g1 is a transmitter equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's TX equalization inputs.<br>The PCS 3.0 internally determines the hard-coded optimal TX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these toplevel pins when the corresponding protocol[0,1,2]_ext_tx_eq_ovrd_[g1,g2,g3,g4] input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON36**

Address: Operational Base + offset (0x3090)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | reserved |

**PCIe3PHY_GRF_PRT0_CON37**

Address: Operational Base + offset (0x3094)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0000 | ext_tx_iboost_lvl<br>protocolP_ext_tx_iboost_lvl is a PHY configuration setting per-rprotocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

**PCIe3PHY_GRF_PRT0_CON38**

Address: Operational Base + offset (0x3098)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RW | 0x00 | ext_tx_misc_g2<br>Reserved |
| 7:0 | RW | 0x00 | ext_tx_misc_g1<br>Reserved |

**PCIe3PHY_GRF_PRT0_CON39**

Address: Operational Base + offset (0x309C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10:8 | RW | 0x0 | tx_vboost_lvl<br>protocolP_ext_tx_vboost_lvl is lane-based PHY configuration setting per-protocol.<br>Lane-based external overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when the phy_ext_ctrl_sel input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |
| 7:0 | RW | 0x00 | ext_tx_misc_g3<br>Reserved |

Rockchip Confidential

**PCIe3PHY_GRF_PRT0_CON50**

Address: Operational Base + offset (0x3140)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:8 | RW | 0x0 | ext_rx_cdr_vco_lowfreq_g3<br>protocolP_ext_rx_cdr_vco_lowfreq_g3 is external overrides settings for receiver vco lower frequency band per protocol. PCS internally drives it to the hard coded default settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted.<br>The protocol0, protocol1, protocol2 correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10 and, g1, g2, g3 correspond to the pcs_laneX_rate[1:0] value of 00, 01, 10 respectively.<br>Note: Protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 7:4 | RW | 0x0 | ext_rx_cdr_vco_lowfreq_g2<br>protocolP_ext_rx_cdr_vco_lowfreq_g2 is external overrides settings for receiver vco lower frequency band per protocol. PCS internally drives it to the hard coded default settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted.<br>The protocol0, protocol1, protocol2 correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10 and, g1, g2, g3 correspond to the pcs_laneX_rate[1:0] value of 00, 01, 10 respectively.<br>Note: Protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 3:0 | RW | 0x0 | ext_rx_cdr_vco_lowfreq_g1<br>protocolP_ext_rx_cdr_vco_lowfreq_g1 is external overrides settings for receiver vco lower frequency band per protocol. PCS internally drives it to the hard coded default settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted.<br>The protocol0, protocol1, protocol2 correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10 and, g1, g2, g3 correspond to the pcs_laneX_rate[1:0] value of 00, 01, 10 respectively.<br>Note: Protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

**PCIe3PHY_GRF_PRT0_CON51**

Address: Operational Base + offset (0x3144)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0000 | ext_rx_eq_afe_gain_g1<br>protocolP_ext_rx_eq_afe_gain_g1 is a receiver equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's RX equalization inputs. The PCS 3.0 internally determines the hardcoded optimal RX equalization settings for each protocol and rate.<br>However, these settings can be overwritten on a per-protocol basis from these top-level pins when the phy_ext_ctrl input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON52**

Address: Operational Base + offset (0x3148)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | ext_rx_eq_afe_gain_g2<br>protocolP_ext_rx_eq_afe_gain_g2 is a receiver equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's RX equalization inputs. The PCS 3.0 internally determines the hardcoded optimal RX equalization settings for each protocol and rate.<br>However, these settings can be overwritten on a per-protocol basis from these top-level pins when the phy_ext_ctrl input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON53**

Address: Operational Base + offset (0x314C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0000 | ext_rx_eq_afe_gain_g3<br>protocolP_ext_rx_eq_afe_gain_g3 is a receiver equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's RX equalization inputs. The PCS 3.0 internally determines the hardcoded optimal RX equalization settings for each protocol and rate.<br>However, these settings can be overwritten on a per-protocol basis from these top-level pins when the phy_ext_ctrl input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON54**

Address: Operational Base + offset (0x3150)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | ext_rx_eq_att_lvl_g1<br>protocolP_ext_rx_eq_att_lvl_g1 is a receiver equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's RX equalization inputs. The PCS 3.0 internally determines the hardcoded optimal RX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these top-level pins when the phy_ext_ctrl input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON55**

Address: Operational Base + offset (0x3154)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:0 | RW | 0x000 | ext_rx_eq_att_lvl_g2<br>protocolP_ext_rx_eq_att_lvl_g2 is a receiver equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's RX equalization inputs. The PCS 3.0 internally determines the hardcoded optimal RX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these top-level pins when the phy_ext_ctrl input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON56**

Address: Operational Base + offset (0x3158)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | ext_rx_eq_att_lvl_g3<br>protocolP_ext_rx_eq_att_lvl_g2 is a receiver equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's RX equalization inputs. The PCS 3.0 internally determines the hardcoded optimal RX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these top-level pins when the phy_ext_ctrl input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON57**

Address: Operational Base + offset (0x315C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0000 | ext_rx_eq_delta_iq_g1<br>protocolP_ext_rx_eq_delta_iq_g1 is a receiver equalization setting overrides.<br>External overrides for the per-protocol settings of the PHY's RX equalization inputs.<br>The PCIe 3.0 internally determines the hard-coded optimal RX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these toplevel pins when the phy_ext_ctrl input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON58**

Address: Operational Base + offset (0x3160)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | ext_rx_eq_delta_iq_g2<br>protocolP_ext_rx_eq_delta_iq_g2 is a receiver equalization setting overrides.<br>External overrides for the per-protocol settings of the PHY's RX equalization inputs.<br>The PCIe 3.0 internally determines the hard-coded optimal RX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these toplevel pins when the phy_ext_ctrl input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON59**

Address: Operational Base + offset (0x3164)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0000 | ext_rx_eq_delta_iq_g3<br>protocolP_ext_rx_eq_delta_iq_g3 is a receiver equalization setting overrides.<br>External overrides for the per-protocol settings of the PHY's RX equalization inputs.<br>The PCIe 3.0 internally determines the hard-coded optimal RX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these toplevel pins when the phy_ext_ctrl input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON60**

Address: Operational Base + offset (0x3168)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | ext_rx_eq_ctle_boost_g1<br>protocolP_ext_rx_eq_ctle_boost_g1 is a receiver equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's RX equalization inputs. The PCS 3.0 internally determines the hardcoded optimal RX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these top-level pins when the phy_ext_ctrl input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON61**

Address: Operational Base + offset (0x316C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19:0 | RW | 0x00000 | ext_rx_eq_ctle_boost_g2<br>protocolP_ext_rx_eq_ctle_boost_g2 is a receiver equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's RX equalization inputs. The PCS 3.0 internally determines the hardcoded optimal RX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these top-level pins when the phy_ext_ctrl input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON62**

Address: Operational Base + offset (0x3170)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | ext_rx_eq_ctle_boost_g3<br>protocolP_ext_rx_eq_ctle_boost_g3 is a receiver equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's RX equalization inputs. The PCS 3.0 internally determines the hardcoded optimal RX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these top-level pins when the phy_ext_ctrl input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON63**

Address: Operational Base + offset (0x3174)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ext_rx_eq_dfe_tap1_g1<br>protocolP_ext_rx_eq_dfe_tap1_g1 is a receiver equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's RX equalization inputs. The PCS 3.0 internally determines the hardcoded optimal RX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these top-level pins when the phy_ext_ctrl input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON64**

Address: Operational Base + offset (0x3178)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ext_rx_eq_dfe_tap1_g2<br>protocolP_ext_rx_eq_dfe_tap1_g2 is a receiver equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's RX equalization inputs. The PCS 3.0 internally determines the hardcoded optimal RX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these top-level pins when the phy_ext_ctrl input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON65**

Address: Operational Base + offset (0x317C)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ext_rx_eq_dfe_tap1_g3<br>protocolP_ext_rx_eq_dfe_tap1_g3 is a receiver equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's RX equalization inputs. The PCS 3.0 internally determines the hardcoded optimal RX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these top-level pins when the phy_ext_ctrl input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON66**

Address: Operational Base + offset (0x3180)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9:6 | RW | 0x0 | ext_tx_vboost_en<br>protocolP_ext_tx_vboost_en configuration setting per protocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs.<br>(For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter).<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |
| 5:3 | RW | 0x0 | ext_tx_term_ctrl<br>protocolP_ext_tx_term_ctrl is a PHY configuration setting per-protocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter.)<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2:0 | RW | 0x0 | ext_rx_term_ctrl<br>protocolP_ext_rx_term_ctrl is a PHY configuration setting per-protocol.<br>External overrides for the per-protocol settings of the PHY configuration inputs. (For per-protocol settings to configure the PHY, refer to the PHY databook, "PHY Usage and Configuration" chapter.)<br>The PCS 3.0 internally determines the hard-coded optimal settings for each protocol. However, these settings can be overwritten on a per-protocol basis from these top-level pins when phy_ext_ctrl_sel input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Note: Because protocol1 supports only two rates, protocol1_ext_*_g3 inputs are not provided. |

**PCIe3PHY_GRF_PRT0_CON67**

Address: Operational Base + offset (0x3184)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | ext_tx_eq_main_g1<br>protocolP_ext_tx_eq_main_g1 is a transmitter equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's TX equalization inputs.<br>The PCS 3.0 internally determines the hard-coded optimal TX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these toplevel pins when the corresponding protocol[0,1,2]_ext_tx_eq_ovrd_[g1,g2,g3,g4] input is asserted. The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON68**

Address: Operational Base + offset (0x3188)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19:0 | RW | 0x00000 | ext_tx_eq_main_g2<br>protocolP_ext_tx_eq_main_g2 is a transmitter equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's TX equalization inputs.<br>The PCS 3.0 internally determines the hard-coded optimal TX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these toplevel pins when the corresponding protocol[0,1,2]_ext_tx_eq_ovrd_[g1,g2,g3,g4] input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON69**

Address: Operational Base + offset (0x318C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | ext_tx_eq_main_g3<br>protocolP_ext_tx_eq_main_g3 is a transmitter equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's TX equalization inputs.<br>The PCS 3.0 internally determines the hard-coded optimal TX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these toplevel pins when the corresponding protocol[0,1,2]_ext_tx_eq_ovrd_[g1,g2,g3,g4] input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON70**

Address: Operational Base + offset (0x3190)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 30:16 | RW | 0x0000 | ext_tx_eq_post_g2<br>protocolP_ext_tx_eq_post_g2 is a transmitter equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's TX equalization inputs.<br>The PCS 3.0 internally determines the hard-coded optimal TX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these toplevel pins when the corresponding protocol[0,1,2]_ext_tx_eq_ovrd_[g1,g2,g3,g4] input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |
| 15 | RO | 0x0 | reserved |
| 14:0 | RW | 0x0000 | ext_tx_eq_post_g1<br>protocolP_ext_tx_eq_post_g1 is a transmitter equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's TX equalization inputs.<br>The PCS 3.0 internally determines the hard-coded optimal TX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these toplevel pins when the corresponding protocol[0,1,2]_ext_tx_eq_ovrd_[g1,g2,g3,g4] input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON71**

Address: Operational Base + offset (0x3194)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:15 | RO | 0x00000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14:0 | RW | 0x0000 | ext_tx_eq_post_g3<br>protocolP_ext_tx_eq_post_g3 is a transmitter equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's TX equalization inputs.<br>The PCS 3.0 internally determines the hard-coded optimal TX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these toplevel pins when the corresponding protocol[0,1,2]_ext_tx_eq_ovrd_[g1,g2,g3,g4] input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON72**

Address: Operational Base + offset (0x3198)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | ext_tx_eq_pre_g2<br>protocolP_ext_tx_eq_pre_g2 is a transmitter equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's TX equalization inputs.<br>The PCS 3.0 internally determines the hard-coded optimal TX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these toplevel pins when the corresponding protocol[0,1,2]_ext_tx_eq_ovrd_[g1,g2,g3,g4] input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0000 | ext_tx_eq_pre_g1<br>protocolP_ext_tx_eq_pre_g1 is a transmitter equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's TX equalization inputs.<br>The PCS 3.0 internally determines the hard-coded optimal TX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these toplevel pins when the corresponding protocol[0,1,2]_ext_tx_eq_ovrd_[g1,g2,g3,g4] input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

**PCIe3PHY_GRF_PRT0_CON73**

Address: Operational Base + offset (0x319C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | ext_tx_eq_pre_g3<br>protocolP_ext_tx_eq_pre_g3 is a transmitter equalization setting for overrides.<br>External overrides for the per-protocol settings of the PHY's TX equalization inputs.<br>The PCS 3.0 internally determines the hard-coded optimal TX equalization settings for each protocol and rate. However, these settings can be overwritten on a per-protocol basis from these toplevel pins when the corresponding protocol[0,1,2]_ext_tx_eq_ovrd_[g1,g2,g3,g4] input is asserted.<br>The protocolP signals correspond to the pcs_laneX_protocol[1:0] value of 00, 01, 10, respectively.<br>Because protocol1 supports only two rates, there are no protocol1_ext_*_g3 inputs. Because only protocol0 supports four rates, there are no protocol[1,2]_ext_*_g4 inputs.<br>These signals are concatenated buses whose width is dependent on the number of lanes in the PCS (NLANES). The buses are ordered from highest lane in the MSBs to lane0 in the LSBs. |

## 6.20 PIPE_PHY_GRF Register Description

There are three PCIe2PHY_GRF modules in RK3588.They have different base address.

### 6.20.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PIPE_PHY_GRF_PIPE_CON0 | 0x0000 | W | 0x00000110 | PIPE Combo PHY Configuration Register 0 |
| PIPE_PHY_GRF_PIPE_CON1 | 0x0004 | W | 0x00000000 | PIPE Combo PHY Configuration Register 1 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PIPE_PHY_GRF_PIPE_CON2 | 0x0008 | W | 0x00009401 | PIPE Combo PHY Configuration Register 2 |
| PIPE_PHY_GRF_PIPE_CON3 | 0x000C | W | 0x00000002 | PIPE Combo PHY Configuration Register 3 |
| PIPE_PHY_GRF_PIPE_CON4 | 0x0010 | W | 0x00000000 | PIPE Combo PHY Configuration Register 4 |
| PIPE_PHY_GRF_PIPE_STATUS1 | 0x0034 | W | 0x000000C0 | PIPE Combo PHY Status Register1 |
| PIPE_PHY_GRF_LFPS_DET_CON | 0x0080 | W | 0x00000009 | PIPE Combo PHY LFPS Detect Control Register |
| PIPE_PHY_GRF_PHY_INT_EN | 0x00A0 | W | 0x00000000 | PIPE Combo PHY Interrupt Signal Enable |
| PIPE_PHY_GRF_PHY_INT_STATUS | 0x00A4 | W | 0x00000000 | PIPE Combo PHY Interrupt Status |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.20.2 Detail Registers Description

**PIPE_PHY_GRF_PIPE_CON0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | pipe_rxstandby<br>SATA mode<br>Controls whether the PHY RX is active when the PHY is in any power state with PCLK on. RX_STANDBY is ignored when the PHY is in any power state where the high-speed receiver is always off.<br>1'b0: Active<br>1'b1: Standby<br><br>PCIe mode<br>Controls whether the PHY RX is active when the PHY is in P0 or P0s. RX_STANDBY is ignored when the PHY is in P1 or P2<br>1'b0: Active<br>1'b1: Standby<br><br>Only used in SATA and PCIe mode. USB3.0 mode should be tied to 1'b0.<br>The value when override enable is selected. |
| 13 | RW | 0x0 | pipe_rxelecidle_disable<br>RX electrical idle detect disable. The value when override enable is selected.<br>1'b0: Idle detect enable<br>1'b1: Idle detect disable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | pipe_rxterm<br>Control presence of receiver terminations. The value when override enable is selected.<br>1'b0: Termination removed<br>1'b1: Termination present<br>Only used in USB3.0 mode, PCIe and SATA mode should be tied to 1'b1. |
| 11 | RW | 0x0 | pipe_bypass_codec<br>PCIe mode, USB mode, and SATA mode. The value when override enable is selected.<br>Controls whether the PHY performs 8b/10b encode and decode.<br>1'b0: 8b/10b encode/decode performed normally by the PHY<br>1'b1: 8b/10b encode/decode bypassed, 20bit<br>8b/10b encode/decode bypass mode works only when BUS_WIDTH=2'b01<br>It should be tie to 1'b1 in SATA low latency and SERDES mode. |
| 10 | RW | 0x0 | pipe_ebuffmode<br>RX Elasticity Buffer operating mode selection. The value when override enable is selected.<br>1'b0: Nominal half-full buffer mode<br>1'b1: Nominal empty buffer mode<br>In SATA and USB3.0 mode, when RX elastic buffer is operating at nominal empty buffer mode, RX_DATA_VALID is de-asserted which means elastic buffer is empty and no data is available.<br>In PCIe mode, only nominal half-full Elasticity Buffer mode is supported. |
| 9 | RW | 0x0 | pipe_l1sub_entreq<br>In PCIe mode<br>L1 sub-state entry request signal in PCIe mode.<br>When set to high, it instructs PHY to do power transition to L1 sub-state.<br><br>In SATA Mode<br>When set to high, it will be power down PLL.<br><br>This signal could be connected to the L1 sub-state enable/request signal from controller<br>Only used in PCIe and SATA mode, USB mode should be tied to 1'b0.<br>The value when override enable is selected.<br>Reserved for current chip. |
| 8 | RW | 0x1 | pipe_mac_pclkreq_n<br>PCIe common clock request signal in PCIe mode.<br>The signal shall be low and CKREF_SRC[1:0] is set to 2'b10 when CKREFP/N and PCI_100M_CLK output from PHY is used for PCIe system with common clock<br>Note: Details refer to CKREFP/N and PCI_100M_CLK.<br>Only used in PCIe mode, USB and SATA mode should be tied to 1'b1.<br>This bit is a override bit for input CLKREQ for PHY when override selection enable. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:6 | RW | 0x0 | pipe_powerdown<br>Power up or power down status control of Transceiver. If PIPE PHY support PIPE4.3, the powerdown is 4-bit, PIPE4.2 or below 2-bit. This filed is powerdown [1:0], powerdown[3:2] is controlled by pipe_powerdown_4p3. The value when override enable is selected.<br>In PCIe mode<br>4'h0: P0, normal mode<br>4'h1: P0s, low recovery time latency, power saving state<br>4'h2: P1, longer recovery time latency, lower power saving<br>4'h3: P2, lowest power state<br>4'h4: P1.CPM<br>4'h5: P1.1<br>4'hc: P1.2<br>Others: Reserved<br><br>In USB3.0 mode<br>4'h0: P0, normal mode<br>4'h1: P1, low recovery time latency, power saving state<br>4'h2: P2, longer recovery time latency, lower power saving<br>4'h3: P3, lowest power state<br>Others: Reserved<br><br>In SATA and Serdes mode<br>4'h0: POWER_STATE_0 operational state, PHY normal operation<br>4'h1: PCLK on, TX common mode on<br>4'h3: PCLK on, TX common mode off<br>4'h5: PCLK off, TX common mode on<br>4'h7: PCLK off, TX common mode off<br>Others: Reserved |
| 5:4 | RW | 0x1 | pipe_rate<br>Combo PHY link signaling rate. The value when override enable is selected.<br>In PCIe mode<br>2'b00: 2.5GT/s<br>2'b01: 5.0GT/s<br>Others: Reserved<br><br>In USB3.0 mode<br>2'b00: 5GT/s<br>Others: Reserved<br><br>In SATA mode<br>2'b00: 1.5GT/s<br>2'b01: 3.0GT/s<br>2'b10: 6.0GT/s<br>2'b11: Reserved<br><br>In SERDES(QSGMII/SGMII) mode<br>2'b00: 1.25Gbps<br>2'b01: Reserved<br>2'b10: 5.0Gbps<br>2'b11: Reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:2 | RW | 0x0 | pipe_phymode<br>Combo PHY mode.<br>2'b00: PCIe<br>2'b01: USB3<br>2'b10: SATA<br>2'b11: Serdes<br>In RK3588 Combo PHY PIPE4.3. The PHY and controller usage list below when each PHY mode is set to PCIe:<br>1L0 connects to Combo PHY1, when pcie1l0_sel is set to 1'b1.<br>1L1 connects to Combo PHY2, when pcie1l1_sel is set to 1'b1.<br>1L2 connects to Combo PHY0. |
| 1:0 | RW | 0x0 | pipe_databuswidth<br>Combo PHY PIPE data bus width. The value when override enable is selected.<br>2'b00: 32-bit, PCIe and USB3 only support 32-bit<br>2'b01: 16-bit, SATA only support 16-bit<br>2'b10: Reserved<br>2'b11: Reserved |

**PIPE_PHY_GRF_PIPE_CON1**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:13 | RW | 0x0 | phy_clk_sel<br>Combo Phy PIPE reference clock frequency selection.<br>2'b00: 24M<br>2'b01: 25M<br>2'b10: 100M<br>2'b11: Reserved |
| 12:11 | RW | 0x0 | pipe_txpattern_sata<br>Controls which pattern the PHY sends at the Gen 1 rate when sending OOB or initialization signaling. The PHY transmits this pattern at the Gen 1 rate regardless of what rate the PHY is configured at. Used in SATA mode only. The value when override enable is selected.<br>2'b00: C ALIGN<br>2'b01: C D24.3<br>2'b10: C D10.2<br>2'b11: C Reserved |
| 10:8 | RW | 0x0 | pipe_txmargin<br>Transmit margin control, combined with txswing to control TX output amplitude. The value when override enable is selected. |
| 7:6 | RW | 0x0 | pipe_txdeemph<br>Transmitter de-emphasis level configuration. The value when override enable is selected.<br>2'b00: -6dB<br>2'b01: -3.5dB<br>2'b10: No de-emphasis<br>2'b11: Reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | pipe_txswing<br>Control transmitter voltage swing level. The value when override enable is selected.<br>1'b0: Full swing<br>1'b1: Low swing |
| 4 | RW | 0x0 | pipe_txcompliance<br>Set the running disparity to negative.<br>Only used in PCIe mode, USB and SATA mode should be tied to 1'b0.<br>The value when override enable is selected. |
| 3 | RW | 0x0 | pipe_txcommonmode_disable<br>TX Common mode Control.<br>1'b0: Enable<br>1'b1: Disable<br>The value when override enable is selected. |
| 2 | RW | 0x0 | pipe_txoneszeros<br>This signal is used in USB3.0 mode for transmitting compliance pattern CP7 and CP8.<br>When set to high, it causes the transmitter to transmit an alternating sequence of 0s and 1s, regardless the states of TX_DATA.<br>Only used in USB mode, PCIE and SATA mode should be tied to 1'b0.<br>The value when override enable is selected. |
| 1 | RW | 0x0 | pipe_txelecidle<br>Forces TX output to electrical idle when asserted except in loopback, refer to PIPE spec for details on control signal usage.<br>When asserted with TX_COMPLIANCE high, the PHY is fully powered off.<br>Shall be kept high when SATA mode that is not in P0.<br>The value when override enable is selected. |
| 0 | RW | 0x0 | pipe_txdectrx_loopback<br>Used to tell the PHY to begin a receiver detection operation or to begin loopback. Refer to s PIPE spec for detail description.<br>This signal shall be set to low when SATA mode that is not in P0.<br>The value when override enable is selected. |

**PIPE_PHY_GRF_PIPE_CON2**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | sel_pipe_txcompliance<br>pipe_txcompliance selection. Override value is selected for PIPE PHY interface.<br>1'b0: From controller side (Controller/Constant/PD GRF)<br>1'b1: From PHY GRF |
| 14 | RW | 0x0 | sel_pipe_txcommonmode_disable<br>pipe_txcommonmode_disable selection. Override value is selected for PIPE PHY interface.<br>1'b0: From controller side (Controller/Constant/PD GRF)<br>1'b1: From PHY GRF |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | sel_pipe_txoneszeros<br>pipe_txoneszeros selection. Override value is selected for PIPE PHY interface.<br>1'b0: From controller side (Controller/Constant/PD GRF)<br>1'b1: From PHY GRF |
| 12 | RW | 0x1 | sel_pipe_txelecidle<br>pipe_txelecidle selection. Override value is selected for PIPE PHY interface.<br>1'b0: From controller side (Controller/Constant/PD GRF)<br>1'b1: From PHY GRF |
| 11 | RW | 0x0 | sel_pipe_txdectrx_loopback<br>pipe_txdectrx_loopback selection. Override value is selected for PIPE PHY interface.<br>1'b0: From controller side (Controller/Constant/PD GRF)<br>1'b1: From PHY GRF |
| 10 | RW | 0x1 | sel_pipe_rxstandby<br>sel_pipe_rxstandby selection. Override value is selected for PIPE PHY interface.<br>1'b0: From controller side (Controller/Constant/PD GRF)<br>1'b1: From PHY GRF |
| 9 | RW | 0x0 | sel_pipe_rxelecidle_disable<br>pipe_rxelecidle_disable selection. Override value is selected for PIPE PHY interface.<br>1'b0: From controller side (Controller/Constant/PD GRF)<br>1'b1: From PHY GRF |
| 8 | RW | 0x0 | sel_pipe_rxterm<br>pipe_rxterm selection. Override value is selected for PIPE PHY interface.<br>1'b0: From controller side (Controller/Constant/PD GRF)<br>1'b1: From PHY GRF |
| 7 | RW | 0x0 | sel_pipe_bypass_codec<br>pipe_bypass_codec selection. Override value is selected for PIPE PHY interface.<br>1'b0: From controller side (Controller/Constant/PD GRF)<br>1'b1: From PHY GRF |
| 6 | RW | 0x0 | sel_pipe_ebuffmode<br>pipe_ebuffmode selection. Override value is selected for PIPE PHY interface.<br>1'b0: From controller side (Controller/Constant/PD GRF)<br>1'b1: From PHY GRF |
| 5 | RW | 0x0 | sel_pipe_l1sub_entreq<br>pipe_l1sub_entreq selection. Override value is selected for PIPE PHY interface.<br>1'b0: From controller side (Controller/Constant/PD GRF)<br>1'b1: From PHY GRF |
| 4 | RW | 0x0 | sel_pipe_powerdown<br>pipe_powerdown selection. Override value is selected for PIPE PHY interface.<br>1'b0: From controller side (Controller/Constant/PD GRF)<br>1'b1: From PHY GRF |
| 3 | RW | 0x0 | sel_pipe_mac_pclkreq_n<br>pipe_mac_pclkreq_n selection. Override value is selected for PIPE PHY interface.<br>1'b0: From controller side (Controller/Constant/PD GRF)<br>1'b1: From PHY GRF |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | sel_pipe_rate<br>pipe_rate selection. Override value is selected for PIPE PHY interface.<br>1'b0: From controller side (Controller/Constant/PD GRF)<br>1'b1: From PHY GRF |
| 1 | RW | 0x0 | sel_pipe_phymode<br>pipe_phymode selection. Override value is selected for PIPE PHY interface.<br>1'b0: From controller side (Controller/Constant/PD GRF)<br>1'b1: From PHY GRF<br>Reserved for RK3588 |
| 0 | RW | 0x1 | sel_pipe_databuswidth<br>pipe_databuswidth selection. Override value is selected for PIPE PHY interface.<br>1'b0: From controller side (Controller/Constant/PD GRF)<br>1'b1: From PHY GRF |

**PIPE_PHY_GRF_PIPE_CON3**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | qsgm_mode<br>QSGMII mode enable.<br>1'b0: Other mode<br>1'b1: QSGMII/SGMII mode<br>Reserved in RK3588 |
| 14:13 | RW | 0x0 | pipe_sel<br>Control the PD PIPE interface source selection.<br>For Combo PIPE PHY0<br>2'b01: Connect to USB3 Controller 0<br>2'b10: Connect to SATA Port 0<br>Others: Reserved<br><br>For Combo PIPE PHY1<br>2'b01: Connect to USB3 Controller 1<br>2'b10: Connect to SATA Port 1<br>2'b11: Connect to QSGMII Controller<br>Others: Reserved<br><br>For Combo PIPE PHY2<br>2'b00: Connect to PCIe2.0 Controller<br>2'b10: Connect to SATA Port 2<br>2'b11: Connect to QSGMII Controller<br>Others: Reserved<br>Reserved in RK3588 |
| 12 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11 | RW | 0x0 | sel_clkreq<br>CLKREQ for PIPE PHY source selection. Override value is selected for PIPE PHY interface.<br>1'b0: From controller side(Controller/Constant/PD GRF/PHY GRF)<br>1'b1: From GPIO mux for CLKREQ_N<br>Because the CLKREQ is valid when high, so the pipe_mac_pclkreq_n should set to "0" when sel_pipe_mac_pclkreq_n is set to "1". |
| 10 | RW | 0x0 | sel_rxelecidle<br>Rxelecidle to controller source selection. Override value is selected for PIPE PHY interface.<br>1'b0: From PIPE PHY<br>1'b1: When rxelecidle_disable is high, rxelecidle return "1" to controller |
| 9:8 | RW | 0x0 | phy_clk_ref_src<br>Combo PHY PIPE reference clock source selection.<br>2'b00: Use PLL_CKREF_INNER as reference clock source, CKREFP/N is not active, the PAD can be floating<br>2'b01: Use CKREFP/N as input reference clock source<br>2'b10: Use PLL_CKREF_INNER (From SoC CRU) as reference clock source, Use CKREFP/N as output clock to provide a differential 100M reference clock in PCIe mode while PIPE PHY CLKREQ is high.<br>2'b11: Not allowed |
| 7:4 | RO | 0x0 | reserved |
| 3 | RW | 0x0 | sel_pipe_txpattern_sata<br>pipe_txpattern_sata selection. Override value is selected for PIPE PHY interface.<br>1'b0: From controller side (Controller/Constant/PD GRF)<br>1'b1: From PHY GRF |
| 2 | RW | 0x0 | sel_pipe_txmargin<br>pipe_txmargin selection. Override value is selected for PIPE PHY interface.<br>1'b0: From controller side (Controller/Constant/PD GRF)<br>1'b1: From PHY GRF |
| 1 | RW | 0x1 | sel_pipe_txdeemph<br>pipe_txdeemph selection. Override value is selected for PIPE PHY interface.<br>1'b0: From controller side (Controller/Constant/PD GRF)<br>1'b1: From PHY GRF |
| 0 | RW | 0x0 | sel_pipe_txswing<br>pipe_txswing selection. Override value is selected select for PIPE PHY interface.<br>1'b0: From controller side (Controller/Constant/PD GRF)<br>1'b1: From PHY GRF |

**PIPE_PHY_GRF_PIPE_CON4**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | pipe_txdeemph_ext<br>Extra direct control the txdeemph bit3. |
| 7:4 | RW | 0x0 | bist_mode<br>BIST mode test in normal operation.<br>4'h0: PHY Normal operation, default value of BIST_MODE<br>4'h8: PHY external BIST from TXP/TXN to RXP/RXN<br>4'h9: PHY internal BIST<br>4'ha: PHY send 1'b0 on TXP and 1'b1 on TXN (only for VOL test)<br>4'hc: PHY send 1'b1 on TXP and 1'b0 on TXN (only for VOH test)<br>4'he: PHY send D10.2 (only for Eye-Diagram test)<br>Others: Reserved |
| 3:2 | RW | 0x0 | serdes_arch<br>This signal indicates whether Serdes architecture and SATA low latency is enabled.<br>2'b00: PCIe/USB/SATA normal working<br>2'b01: Used for SATA SAPIS compliant controller, that bypass PHY elastic buffer to reduce latency, RX_DATA is the result of comma align.<br>2'b10: General serdes mode and RX_DATA is the result of CDR in PMA<br>2'b11: General serdes mode and RX_DATA is the result of comma align |
| 1:0 | RW | 0x0 | pipe_powerdown_4p3<br>For PIPE4.3 interface, the powerdown are 4 bit, the field is for powerdown[3:2]. Override value when override enable is selected. |

**PIPE_PHY_GRF_PIPE_STATUS1**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9 | RO | 0x0 | pipe_clkreq_n<br>Indicates that the PHY is in corresponding state to L1-sub-state in PCIE mode, during which PHY reference clock could be turned off. This signal could connect to corresponding signal in controller IP, if applicable. |
| 8 | RO | 0x0 | pipe_power_presetn<br>Reserved |
| 7 | RO | 0x1 | pipe_rxelecidle_o<br>Indicates receiver detection of an electrical idle. When de-asserted with the PHY in P2 (PCIE Mode), indicates a detection of beacon, while indicate exit from electrical idle in other power states in PCIe mode.<br>In USB3.0 mode, it indicates the detection of LFPS.<br>In SATA mode, it indicates if there is no data/OOB received. |
| 6 | RO | 0x1 | pipe_phystatus_o<br>Used to communicate completion of several PHY functions including power management state transitions, rate change and receiver detection. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5:3 | RO | 0x0 | pipe_rxstatus_o<br>PIPE PHY receiver status. Encode receiver status and error codes for the received data stream when receiving data.<br>3'b000: Received data OK<br>3'b001: PCIe mode, 1 SKP added; USB mode: 1 SKP added; SATA mode: 1 ALIGN added Asseted width first byte of Align that was added<br>3'b010: PCIe mode: 1 SKP Ordered set removed; 1 SKP Ordered Set removed; SATA mode: 1 or more ALIGNs<br>3'b011: PCIe and USB mode: Receiver detected<br>3'b100: 8B/10B decode error<br>3'b101: Elastic buffer overflow<br>3'b110: Elastic buffer under flow, this error code is not used if the elastic buffer is operating in the nominal buffer empty mode<br>3'b111: Receive disparity error, overwritten by decode error |
| 2:0 | RO | 0x0 | reserved |

**PIPE_PHY_GRF_LFPS_DET_CON**

Address: Operational Base + offset (0x0080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x09 | lfps_detect_con<br>LFPS Detect Count Filter Control.<br>This counter determines whether a rxelecidle (high pulse) is valid or not. The counter is based on Combo PIPE PHY APB PCLK. |

**PIPE_PHY_GRF_PHY_INT_EN**

Address: Operational Base + offset (0x00A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2 | RW | 0x0 | rxelecidle_l1_fall_irq_en<br>rxelecidle_l1_fall irq enable.<br>1'b0: IRQ disable<br>1'b1: IRQ enable<br>Reserved for current PHY. |
| 1:0 | RW | 0x0 | rxelecidle_l0_fall_irq_en<br>rxelecidle_l0_fall irq enable.<br>1'b0: IRQ disable<br>1'b1: IRQ enable |

**PIPE_PHY_GRF_PHY_INT_STATUS**

Address: Operational Base + offset (0x00A4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | W1C | 0x0 | rxelecidle_l1_fall_irq_st<br>rxelecidle_l1_fall irq status.<br>1'b0: Interrupt inactive<br>1'b1: Interrupt active<br>Reserved for current PHY. |
| 0 | W1C | 0x0 | rxelecidle_l0_fall_irq_st<br>rxelecidle_l0_fall irq status.<br>1'b0: Interrupt inactive<br>1'b1: Interrupt active |

Rockchip Confidential

# 6.21 USBDPPHY_GRF Register Description

There are two USBDPPHY_GRF modules in RK3588.They have different base address.

## 6.21.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| USBDPPHY_GRF_CON1 | 0x0004 | W | 0x00000000 | USBDPPHY Control Register 1 |
| USBDPPHY_GRF_CON2 | 0x0008 | W | 0x00000000 | USBDPPHY Control Register 2 |
| USBDPPHY_GRF_CON3 | 0x000C | W | 0x00000000 | USBDPPHY Control Register 3 |
| USBDPPHY_GRF_STATUS1 | 0x0084 | W | 0x00000000 | USBDPPHY Status Register |
| USBDPPHY_GRF_LFPS_DET_CON | 0x00C0 | W | 0x00000009 | LFPS Detect Control |
| USBDPPHY_GRF_INT_EN | 0x00C4 | W | 0x00000000 | Interrupt Enable Register |
| USBDPPHY_GRF_INT_STATUS | 0x00C8 | W | 0x00000000 | Interrupt Status Register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.21.2 Detail Registers Description

**USBDPPHY_GRF_CON1**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | rx_lfps_en<br>Enable RX LFPS Detector Block.<br>1'b1: RX SQ enable<br>1'b0: RX SQ disable |
| 13 | RW | 0x0 | usbdp_low_pwrn<br>Used for the PMA power off function.<br>1'b0: PMA block power off<br>1'b1: PMA block power on |
| 12:0 | RO | 0x0000 | reserved |

**USBDPPHY_GRF_CON2**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | phy_clamp<br>1'b0: Normal mode<br>1'b1: Clamp PHY output to special value |
| 14:13 | RW | 0x0 | debug_clock_sel<br>select phy debug clock output<br>2'b00: o_vcoclk_div40_mon<br>2'b01: o_dbg_clk<br>2'b10: o_dp_txclk<br>2'b11: o_vcoclk_div40_mon |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | debug_clk_gate_disable<br>1'b0: Gate phy debug clock output<br>1'b1: Do not gate phy debug clock output |
| 11:0 | RO | 0x000 | reserved |

**USBDPPHY_GRF_CON3**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x0 | soft_pipe3_txdetectrxloopbk<br>When USBDPPHY_GRF_CON3[0] is 1'b1, tx_detectrx_loopback is controlled by this bit. |
| 4:3 | RW | 0x0 | soft_pipe3_powerdown<br>When USBDPPHY_GRF_CON3[0] is 1'b1, powerdown is controlled by this bit. |
| 2 | RW | 0x0 | soft_pipe3_txelecidle<br>When USBDPPHY_GRF_CON3[0] is 1'b1, tx_elecidle is controlled by this bit. |
| 1 | RW | 0x0 | soft_pipe3_rxtermination<br>When USBDPPHY_GRF_CON3[0] is 1'b1, rx_termination is controlled by this bit. |
| 0 | RW | 0x0 | grf_control_sel<br>1'b0: Normal mode<br>1'b1: rx_termination , tx_elecidle, powerdown, tx_detectrx_loopback are controlled by GRF |

**USBDPPHY_GRF_STATUS1**

Address: Operational Base + offset (0x0084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x00 | reserved |
| 24:22 | RO | 0x0 | pipe_rxstatus<br>Encodes receiver status and error codes for the received data stream when receiving data. |
| 21 | RO | 0x0 | pipe_rxelecidle<br>Indicates receiver detection of an electrical idle. While deasserted with the PHY in P2, indicates detection of a beacon. |
| 20 | RO | 0x0 | pipe_phy_status<br>Used to communicate completion of several PHY functions including power management state transitions, rate change, and receiver detection. |
| 19 | RO | 0x0 | pll_lock_done<br>PLL Lock Indication<br>This bit is high when PLL Locking is complete. |
| 18:0 | RO | 0x00000 | reserved |

**USBDPPHY_GRF_LFPS_DET_CON**

Address: Operational Base + offset (0x00C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:0 | RW | 0x09 | lfps_detect_con<br>LFPS filter counter control |

**USBDPPHY_GRF_INT_EN**

Address: Operational Base + offset (0x00C4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | lfps_l0_beacon_int_en<br>beacon interrupt enable<br>1'b0: Interrupt disable<br>1'b1: Interrupt enable |

**USBDPPHY_GRF_INT_STATUS**

Address: Operational Base + offset (0x00C8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | lfps_l0_beacon_int_status<br>beacon interrupt status<br>Write 1 to this bit will clear the interrupt |

# 6.22 USB2PHY_GRF Register Description

There are four USB2PHY_GRF modules in RK3588.They have different base address.

## 6.22.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| USB2PHY_GRF_CON0 | 0x0000 | W | 0x00007066 | USB2PHY Control Register 0 |
| USB2PHY_GRF_CON1 | 0x0004 | W | 0x00007633 | USB2PHY Control Register 1 |
| USB2PHY_GRF_CON2 | 0x0008 | W | 0x00000D00 | USB2PHY Control Register 2 |
| USB2PHY_GRF_CON3 | 0x000C | W | 0x00000200 | USB2PHY Control Register 3 |
| USB2PHY_GRF_CON4 | 0x0010 | W | 0x00000000 | USB2PHY Control Register 4 |
| USB2PHY_GRF_LS_CON | 0x0040 | W | 0x00030100 | USB2PHY Linestate Filter Control |
| USB2PHY_GRF_DIS_CON | 0x0044 | W | 0x00030100 | USB2PHY Disconnect Filter Control |
| USB2PHY_GRF_BVALID_CON | 0x0048 | W | 0x00030100 | USB2PHY BValid Filter Control |
| USB2PHY_GRF_ID_CON | 0x004C | W | 0x00030100 | USB2PHY ID Filter Control |
| USB2PHY_GRF_INT_MASK | 0x0080 | W | 0x00000000 | Interrupt Mask Register |
| USB2PHY_GRF_INT_STATUS | 0x0084 | W | 0x00000000 | Interrupt Status Register |
| USB2PHY_GRF_INT_STATUS_CLR | 0x0088 | W | 0x00000000 | Interrupt Clear Register |
| USB2PHY_GRF_STATUS0 | 0x00C0 | W | 0x00000000 | USB2PHY Status Register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.22.2 Detail Registers Description

**USB2PHY_GRF_CON0**

Address: Operational Base + offset (0x0000)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | port_reset<br>Per-Port Reset<br>When asserted, this signal resets the corresponding port's transmit and receive logic without disabling the clocks within the USB 2.0 PHY.<br>1'b1: The transmit and receive finite state machines (FSMs) are reset, and the line_state logic combinatorially reflects the state of the single-ended receivers.<br>1'b0: The transmit and receive FSMs are operational, and the line_state logic becomes sequential after 11 PHYCLOCK0 cycles. |
| 14 | RW | 0x1 | pllbtune<br>PLL Bandwidth adjustment<br>This adjustment doubles the bandwidth of the PLL as needed for some input reference clock frequencies. |
| 13:10 | RW | 0xc | pllptune<br>PLL Proportional Path Tune<br>This signal should be set to the Design default.<br>4'b1111: 4.75x<br>4'b1110: 4.50x<br>4'b1101: 4.25x<br>4'b1100: 4.00x, Design default<br>4'b1011: 3.75x<br>4'b1010: 3.50x<br>4'b1001: 3.25x<br>4'b1000: 3.00x<br>4'b0111: 2.75x<br>4'b0110: 2.50x<br>4'b0101: 2.25x<br>4'b0100: 2.00x<br>4'b0011: 1.75x<br>4'b0010: 1.50x<br>4'b0001: 1.25x<br>4'b0000: 1.00x |
| 9:8 | RW | 0x0 | pllitune<br>PLL Integral Path Tune<br>This signal should be set to the Design default.<br>2'b11: 2.0x<br>2'b10: 1.5x<br>2'b01: 1.0x<br>2'b00: 0.5x, Design |
| 7:5 | RW | 0x3 | tune<br>VBUS Valid Threshold Adjustment<br>This bus adjusts the voltage level for the VBUS Valid threshold.<br>3'b111: +12.59%<br>3'b110: +9.63%<br>3'b101: +6.42%<br>3'b100: +3.21%<br>3'b011: 0, Design default<br>3'b010: -2.96%<br>3'b001: -6.17%<br>3'b000: -9.38% |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | disable<br>OTG Block Disable<br>This signal powers down the VBUS Valid comparator, but not the Session Valid comparator, nor the ID detection circuitry. To save power, if the application does not use the OTG function, this input can be set high.<br>1'b1: The OTG block is powered down.<br>1'b0: The OTG block is powered up. |
| 3:1 | RW | 0x3 | compdistune<br>Disconnect Threshold Adjustment<br>This bus adjusts the voltage level for the threshold used to detect a disconnect event at the host.<br>3'b111: +15.20%<br>3'b110: +11.15%<br>3'b101: +7.05%<br>3'b100: +3.59%<br>3'b011: 0<br>3'b010: -2.94%<br>3'b001: -5.96%<br>3'b000: -8.58% |
| 0 | RW | 0x0 | common_on_n<br>Common Block Power-Down Control<br>This signal controls the power-down signals in the REFCLK_LOGIC, Bias, and PLL blocks when the USB 2.0 PHY is in Suspend, or Sleep mode.<br>1'b1: In Suspend mode, the REFCLK_LOGIC, Bias, and PLL blocks are powered down. In Sleep mode, the Bias and PLL blocks are powered down.<br>1'b0: In Suspend or Sleep modes, the REFCLK_LOGIC, Bias, and PLL blocks remain powered. With this setting, the input reference clock must remain on and valid during suspend or sleep. |

**USB2PHY_GRF_CON1**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RW | 0x1 | txrisetune<br>HS Transmitter Rise/Fall Time Adjustment<br>This bus adjusts the rise/fall times of the high-speed waveform.<br>2'b11: -3.24%<br>2'b10: -1.33%<br>2'b01: 0, Design default<br>2'b00: +2.19% |
| 13:12 | RW | 0x3 | txhsxvtune<br>Transmitter High-Speed Crossover Adjustment<br>This bus adjusts the voltage at which the DP0 and DM0 signals cross while transmitting in HS mode.<br>2'b11: 0, Default setting<br>2'b10: +11.05 mV<br>2'b01: -9.2 mV<br>2'b00: +0.67 mV |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:8 | RW | 0x6 | txvreftune<br>HS DC Voltage Level Adjustment<br>This bus adjusts the high-speed DC level voltage.<br>4'b1111: +21.58%<br>4'b1110: +17.66%<br>4'b1101: +13.74%<br>4'b1100: +11.78%<br>4'b1011: +9.81%<br>4'b1010: +7.85%<br>4'b1001: +5.89%<br>4'b1000: +3.92%<br>4'b0111: +1.96%<br>4'b0110: 0, Design default<br>4'b0101: -1.96%<br>4'b0100: -3.92%<br>4'b0011: -5.89%<br>4'b0010: -7.85%<br>4'b0001: -9.81%<br>4'b0000: -13.73% |
| 7:4 | RW | 0x3 | txfslstune<br>This bus adjusts the low- and full-speed single-ended source impedance while driving high. The following adjustment values are based on nominal process, voltage, and temperature.<br>4'b1111: -10.33%<br>4'b0111: -5.49%<br>4'b0011: 0, Design default<br>4'b0001: +6.34%<br>4'b0000: +13.63%<br>All other bit settings are reserved. |
| 3 | RW | 0x0 | txpreemppulsetune<br>This signal controls the duration for which the HS pre-emphasis current is sourced onto DP0 or DM0. The HS Transmitter preemphasis duration is defined in terms of unit amounts. One unit of pre- emphasis duration is approximately 580 ps and is defined as 1X pre- emphasis duration.<br>1'b1: 1x, short pre-emphasis current duration<br>1'b0 (design default): 2x, long pre-emphasis current duration |
| 2:0 | RW | 0x3 | sqrxtune<br>Squelch Threshold Adjustment<br>This bus adjusts the voltage level for the threshold used to detect valid high-speed data.<br>3'b111: -21.12%<br>3'b110: -15.93%<br>3'b101: -10.53%<br>3'b100: -5.41%<br>3'b011: 0, Design default<br>3'b010: +5.14%<br>3'b001: +10.51%<br>3'b000: +15.68% |

**USB2PHY_GRF_CON2**

Address: Operational Base + offset (0x0008)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | dcdenb<br>Enhanced Data Contact Detection Enable<br>Enables current sourcing on the D+ line. For special applications, the IDP_SRC control and the RDM_DWN control are separated. For standard DCD operation in accordance with the Battery Charger v1.2 specification, simultaneously set DCDENB0=1'b1 (to enable IDP_SRC) and set DMPULLDOWN0=1'b1 (to enable RDM_DWN). Set both signals to 1'b0 when DCD is completed.<br>1'b1: IDP_SRC current is sourced onto DP0<br>1'b0: IDP_SRC current is disabled |
| 13 | RW | 0x0 | siddq<br>IDDQ Test Enable<br>This test signal enables you to perform IDDQ testing by powering down all analog blocks. Before asserting SIDDQ, ensure that TESTBURNIN is set to 1'b0, and RETENABLEN is set to 1'b1.<br>1'b1: The analog blocks are powered down.<br>1'b0: The analog blocks are powered up. |
| 12:11 | RW | 0x1 | txrestune<br>USB Source Impedance Adjustment<br>In some applications, there can be significant series resistance on the D+ and D- paths between the transceiver and cable. This bus adjusts the driver source impedance to compensate for added series resistance on the USB.<br>Note: Any setting other than the default can result in source impedance variation across process, voltage, and temperature conditions that does not meet USB 2.0 specification limits.<br>2'b11: Source impedance is decreased by approximately 4.74 ohm<br>2'b10: Source impedance is decreased by approximately 2.5 ohm<br>2'b01: 0, Design default<br>2'b00: Source impedance is increased by approximately 3.23 ohm<br>If this bus is not used, leave it at the default setting. |
| 10 | RW | 0x1 | sleempm<br>Sleep Assertion<br>Asserting this signal places the USB 2.0 PHY in Sleep mode according to the USB 2.0 Link Power Management (LPM) addendum to the USB 2.0 specification. In Sleep mode, the transmitter is tristated and the USB 2.0 PHY circuits are powered down except for the REFCLK_LOGIC block. The REFCLK_LOGIC block remains powered when the USB 2.0 PHY is placed in Sleep mode.<br>1'b1: Normal operating mode<br>1'b0: Sleep mode |
| 9 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x1 | retenable_n<br>Retention Mode Enable<br>Retention mode allows the USB 2.0 PHY to retain internal digital core signal states when the PHY DVDD supply is lowered to a process specific retention voltage level. Retention mode also forces all internal DVDD-to-VDD18 level translators into a predefined state based on the PHY operating mode. |
| 7 | RW | 0x0 | vdatsrcenb<br>Battery Charging Sourcing Select<br>Enables or disables sourcing for battery charging.<br>1'b1: Data source voltage (VDAT_SRC) is enabled.<br>1'b0: Data source voltage (VDAT_SRC) is disabled. |
| 6 | RW | 0x0 | vdatdetenb<br>Battery Charging Attach/Connect Detection Enable<br>Enables or disables attach/connect detection.<br>1'b1: Data detect voltage (CHG_DET) is enabled.<br>1'b0: Data detect voltage (CHG_DET) is disabled. |
| 5 | RW | 0x0 | chrgsel<br>Determines whether current is sourced onto or sunk from DP0 or DM0.<br>The definitions shown below apply when CHRGSRCPUENB0[1:0]=2'b00. See CHRGSRCPUENB0[1:0] for other modes.<br>1'b1: Data source voltage (VDAT_SRC) is sourced onto DM0 and sunk from DP0.<br>1'b0: Data source voltage (VDAT_SRC) is sourced onto DP0 and sunk from DM0. |
| 4:3 | RW | 0x0 | txpreempamptune<br>HS Transmitter Pre-Emphasis Current Control<br>This signal controls the amount of current sourced to DP0 and DM0 after a J-to-K or K-to-J transition. The HS Transmitter pre-emphasis current is defined in terms of unit amounts. One unit amount is approximately 2 mA and is defined as 1X pre-emphasis current.<br>2'b11: HS Transmitter pre-emphasis circuit sources 3x pre-emphasis current.<br>2'b10: HS Transmitter pre-emphasis circuit sources 2x pre-emphasis current.<br>2'b01: HS Transmitter pre-emphasis circuit sources 1x pre-emphasis current.<br>2'b00 (design default): HS Transmitter pre-emphasis is disabled. |
| 2 | RW | 0x0 | soft_con_sel<br>Soft control select Bit. |
| 1 | RW | 0x0 | vbusvldextsel<br>External VBUS Valid Select<br>This signal selects either the VBUSVLDEXT0 input or the internal Session Valid comparator to detect whether the VBUS signal on the USB cable is valid and to assert the DP0 pull-up resistor. The activation of the DP0 pull-up resistor also depends on the state of XCVRSEL0[1:0], OPMODE0[1:0], TERMSEL0, DPPULLDOWN0, and DMPULLDOWN0.<br>1'b1: The VBUSVLDEXT0 input is used to assert the DP0 pull-up resistor.<br>1'b0: The internal Session Valid comparator is used to assert the DP0 pull-up resistor. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | vbusvldext<br>External VBUS Valid Indicator<br>This signal is valid in Device mode and only when the VBUSVLDEXTSEL0 signal is set to 1'b1. VBUSVLDEXT0 indicates whether the VBUS signal on the USB cable is valid. In addition, VBUSVLDEXT0 enables the pull-up resistor on the D+ line. VBUSVLDEXT0 does not change the OTGSESSVLD0 output.<br>1'b1: The VBUS signal is valid, and the pull-up resistor on D+ is enabled.<br>1'b0: The VBUS signal is not valid, and the pull-up resistor on D+ is disabled. In Host mode, this input is not used and can be tied to 1'b0. |

**USB2PHY_GRF_CON3**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RW | 0x00 | suspend_con<br>Only exsit in GRF for USB2PHY of U3 port.<br>usbphy suspend control signal.<br>If USB2PHY_GRF_CON3[11] is 1, USB2PHY.SUSPENDM0 is controlled by USB2PHY_GRF_CON3[12];<br>If USB2PHY_GRF_CON3[11] is 0 and USB2PHY_GRF_CON3[14:13] is 0x3, USB2PHY.SUSPENDM0 is controlled by usbotg_utmi_suspend_n & usbotg_utmi_l1_suspend_n;<br>If USB2PHY_GRF_CON3[11] is 0 and USB2PHY_GRF_CON3[14:13] is 0x1, USB2PHY.SUSPENDM0 is controlled by USB2PHY_GRF_CON3[15];<br>If USB2PHY_GRF_CON3[11] is 0 and USB2PHY_GRF_CON3[13] is 0x0, USB2PHY.SUSPENDM0 is controlled by ~usbotg_utmi_suspend_com_n & ~usbotg_utmi_l1_suspend_com_n. |
| 10:9 | RW | 0x1 | vdatreftune0<br>Data Detect Voltage Adjustment<br>This bus adjusts the threshold voltage level (Vdat_ref) used to detect data during charger type detection.<br>2'b11: -19.8%<br>2'b10: -9.84%<br>2'b01: 0, Design default<br>2'b00: +9.93% |
| 8 | RW | 0x0 | hsxcvrextctl0<br>HS Transceiver Asynchronous Control<br>This signal asynchronously selects the HS transceiver Tx/Rx path. This signal can be used with the bypass signals in "UART/Autoresume Signals" on page 50 to perform proprietary tests on the HS Tx / Rx paths. The PHY must be in an HS state with XCVRSEL0[1:0] = 2'b00 and TERMSEL0 = 1'b0.<br>1'b1: HS Tx/Rx path is selected<br>1'b0: FS Tx/Rx path is selected |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x0 | autorsmenb0<br>Autoresume Mode Enable<br>Autoresume mode can be used when the USB 2.0 PHY is operating in a host role. This mode enables the autoresume logic in the PHY, so that the PHY will automatically respond to a remote wake-up resume-k from a peripheral, without initial involvement from the host controller. The PHY will respond to a remote wake-up resume-k by driving out its own resume-k. The PHY resume-k will be held until the host controller takes over and configures the PHY to continue driving the resume-k. |
| 6 | RW | 0x0 | bypasssel<br>Transmitter Digital Bypass Select<br>Enables/disables Transmitter Digital Bypass mode. The standard FS UART mode is selected by setting HSXCVREXTCTL0 = 1'b0, and a proprietary HS test mode is selected by setting HSXCVREXTCTL0 = 1'b1.<br>1'b1: Transmitter Digital Bypass mode is enabled.<br>1'b0: Transmitter Digital Bypass mode is disabled |
| 5 | RW | 0x0 | bypassdmen<br>DM0 Transmitter Digital Bypass Enable<br>Enables/disables the DM0 FS/LS driver (if HSXCVREXTCTL0 = 1'b0) in Transmitter Digital Bypass mode. FS mode is the standard UART mode. To use this mode,BYPASSSEL0 must be 1'b1.<br>1'b1: DM0 FS/LS driver (if HSXCVREXTCTL0 = 1'b0) is enabled and driven with the BYPASSDPDATA0 signal.<br>1'b0: DM0 FS/LS driver (if HSXCVREXTCTL0 = 1'b0) is disabled in Transmitter Digital Bypass mode. |
| 4 | RW | 0x0 | sft_utmi_termselect<br>When soft_con_sel is 1'b1, termselect is controlled by sft_utmi_termselect. |
| 3:2 | RW | 0x0 | sft_utmi_xcvrselect<br>When soft_con_sel is 1'b1, xcvrselect is controlled by sft_utmi_xcvrselect. |
| 1:0 | RW | 0x0 | sft_utmi_opmode<br>When soft_con_sel is 1'b1, opmode is controlled by sft_utmi_opmode. |

**USB2PHY_GRF_CON4**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | sft_suspend_n<br>Only exsit in GRF for USB2PHY of U2 port.<br>When soft_con_sel is 1'b1, suspend is controlled by sft_suspend_n register. |
| 7:4 | RO | 0x0 | reserved |
| 3 | RW | 0x0 | sft_vbus_sel<br>VBUS software control select. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | sft_vbus<br>When sft_vbus_sel is 1'b1, vbusvalid and bvalid is controlled by sft_vbus. |
| 1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | idpullup<br>Only exsit in GRF for USB2PHY of U3 port.<br>Pull-up enable control for IDDIG pin.<br>High valid. |

**USB2PHY_GRF_LS_CON**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x30100 | linestate_filter_con<br>host/otg port linestate filter time control register. Unit:PCLK |

**USB2PHY_GRF_DIS_CON**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x30100 | disconnect_filter_con<br>host/otg port hostdisconnect filter time control register. Unit:PCLK |

**USB2PHY_GRF_BVALID_CON**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x30100 | bvalid_filter_con<br>otg port bvalid filter time control register. Unit:PCLK |

**USB2PHY_GRF_ID_CON**

Address: Operational Base + offset (0x004C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27:0 | RW | 0x0030100 | id_filter_con<br>otg ID port filter time control register. Unit:PCLK |

**USB2PHY_GRF_INT_MASK**

Address: Operational Base + offset (0x0080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6:5 | RW | 0x0 | otg0_disconnect_irq_en<br>otg0_disconnect_irq edge status enable<br>2'bx1: Disconnect rising edge irq status enable<br>2'b1x: Disconnect falling edge irq status enable |
| 4:3 | RW | 0x0 | otg0_id_irq_en<br>otg0_id edge status enable<br>2'bx1: ID rising edge irq status enable<br>2'b1x: ID falling edge irq status enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2:1 | RW | 0x0 | otg0_bvalid_irq_en<br>otg0_bvalid edge status irq enable<br>2'bx1: Bvalid rising edge irq status enable<br>2'b1x: Bvalid falling edge irq status enable |
| 0 | RW | 0x0 | otg0_linestate_irq_en<br>otg0_linestate change status irq enable<br>High valid. |

**USB2PHY_GRF_INT_STATUS**

Address: Operational Base + offset (0x0084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6:5 | RO | 0x0 | otg0_disconnect_irq<br>otg0_disconnect_irq edge status<br>2'bx1: Disconnect rising edge irq status<br>2'b1x: Disconnect falling edge irq status |
| 4:3 | RO | 0x0 | otg0_id_irq<br>otg0_id edge status<br>2'bx1: ID rising edge irq status<br>2'b1x: ID falling edge irq status |
| 2:1 | RO | 0x0 | otg0_bvalid_irq<br>otg0_bvalid edge status irq status<br>2'bx1: Bvalid rising edge irq status<br>2'b1x: Bvalid falling edge irq status |
| 0 | RO | 0x0 | otg0_linestate_irq<br>otg0_linestate change status irq status |

**USB2PHY_GRF_INT_STATUS_CLR**

Address: Operational Base + offset (0x0088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6:5 | WO | 0x0 | otg0_disconnect_irq_clr<br>otg0_disconnect_irq edge status clear, write 1 to clear irq status<br>2'bx1: Disconnect rising edge irq status clear, write 1 to clear irq status<br>2'b1x: Disconnect falling edge irq status clear, write 1 to clear irq status |
| 4:3 | WO | 0x0 | otg0_id_irq_clr<br>otg0_id edge status clear, write 1 to clear irq status<br>2'bx1: ID rising edge irq status clear, write 1 to clear irq status<br>2'b1x: ID falling edge irq status clear, write 1 to clear irq status |
| 2:1 | WO | 0x0 | otg0_bvalid_irq_clr<br>otg0_bvalid edge status irq status clear, write 1 to clear irq status<br>2'bx1: Bvalid rising edge irq status clear, write 1 to clear irq status<br>2'b1x: Bvalid falling edge irq status clear, write 1 to clear irq status |
| 0 | WO | 0x0 | otg0_linestate_irq_clr<br>otg0_linestate change status irq status clear, write 1 to clear irq status |

**USB2PHY_GRF_STATUS0**

Address: Operational Base + offset (0x00C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11 | RO | 0x0 | otgsessvld<br>OTG Device Session Valid Indicator (Low Voltage) This controller signal is output from the USB 2.0 PHY's Session Valid comparator and indicates whether the voltage on VBUS is below the OTG Device Session Valid threshold.<br>1'b1: The voltage on VBUS is above the OTG Device Session Valid threshold.<br>1'b0: The voltage on VBUS is below the OTG Device Session Valid threshold. |
| 10:9 | RO | 0x0 | utmi_linestate<br>Line State Indicator<br>This controller bus reflects the state of the single-ended receivers. In Suspend or Sleep mode, this bus is a combinatorial output (directly reflecting the current state of D- and D+, respectively).<br>11: SE1 (D+ high, D- high)<br>10: K state for high-speed and full-speed USB traffic; J state for low-speed USB traffic (D+ low, D- high)<br>01: J state for high-speed and full-speed USB traffic; K state for low-speed USB traffic (D+ high, D- low)<br>00: SE0 (D+ low, D- low) |
| 8 | RO | 0x0 | utmi_vbusvalid<br>VBUS valid status. |
| 7 | RO | 0x0 | utmi_avalid<br>VBUS avalid status. |
| 6 | RO | 0x0 | utmi_bvalid<br>VBUS bvalid status. |
| 5 | RO | 0x0 | utmi_iddig<br>IDDIG status.<br>1'b0: Host<br>1'b1: Device |
| 4 | RO | 0x0 | hsrxdat0<br>This signal asynchronously outputs the state of the HS receiver. This signal can be used with the bypass signals in "UART/Autoresume Signals" on page 50 to perform proprietary tests on the HS Rx block. The PHY must be in an HS state with XCVRSEL0[1:0] = 2'b00 and TERMSEL0 = 1'b0. HSXCVREXTCTL0 must be set to 1'b1 to use this mode. HSRXDAT0 is gated to 1'b0 if HSXCVREXTCTL0 = 1'b0.<br>1'b1: If HSXCVREXTCTL0 = 1'b1 and HSSQUELCH0 = 1'b0, the HS differential receiver has detected an HS J.<br>1'b0: If HSXCVREXTCTL0 = 1'b1 and HSSQUELCH0 = 1'b0, the HS differential receiver has detected an HS K. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RO | 0x0 | hssquelch0<br>HS Squelch Detector Asynchronous Output<br>This signal asynchronously outputs the state of the HS squelch detector. This signal can be used with the bypass signals in "UART/<br>Autoresume Signals" on page 50 to perform proprietary tests on the HS Rx block. The PHY must be in an HS state with XCVRSEL[1:0] = 2'b00 and TERMSEL = 1'b0. HSXCVREXTCTL must be set to 1'b1 to use this mode. HSSQUELCH is gated to 1'b0 if HSXCVREXTCTL = 1'b0.<br>1'b1: If HSXCVREXTCTL = 1'b1, the HS squelch detector has not detected a valid HS VIL level. The line is squelched.<br>1'b0: If HSXCVREXTCTL = 1'b1, the HS squelch detector has detected a valid HS VIL level. The line is not squelched. The HSRXDAT signal indicates whether the detected signal is a J or a K. |
| 2 | RO | 0x0 | fsvminus<br>Single-Ended D- Indicator<br>This controller signal indicates the state of the D- line in normal operation.<br>1'b1: The voltage on D- is high.<br>1'b0: The voltage on D- is low |
| 1 | RO | 0x0 | fsvplus<br>Single-Ended D+ Indicator<br>This controller signal indicates the state of the D+ line during normal operation or UART data reception.<br>1'b1: The voltage on D+ is high.<br>1'b0: The voltage on D+ is low |
| 0 | RO | 0x0 | chgdet<br>Battery Charger Detection Output<br>Indicates whether the voltage level on DP0 or DM0 is greater than VDAT_REF as defined in the Battery Charger specification.<br>1'b1: VDP > VDAT_REF (for CHRGSEL0 = 1'b1) or VDM > VDAT_REF (for CHRGSEL0 = 1'b0)<br>1'b0: VDP < VDAT_REF (for CHRGSEL0 = 1'b1) or VDM < VDAT_REF (for CHRGSEL0 = 1'b0) |

## 6.23 HDPTXPHY_GRF Register Description

There are two HDMITXPHY_GRF modules in RK3588.They have different base address.

### 6.23.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| HDPTXPHY_GRF_CON0 | 0x0000 | W | 0x00000000 | HDPTXPHY Control Register 0 |
| HDPTXPHY_GRF_CON1 | 0x0004 | W | 0x00000000 | HDPTXPHY Control Register 1 |
| HDPTXPHY_GRF_STATUS0 | 0x0080 | W | 0x00000000 | HDPTXPHY Status Register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

### 6.23.2 Detail Registers Description

**HDPTXPHY_GRF_CON0**

Address: Operational Base + offset (0x0000)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11:10 | RW | 0x0 | ro_ref_clk_sel<br>Input Reference Clock source selector<br>This pin controls reference clock source<br>2'b00: Input reference clock from refclk_xtal<br>2'b01: Input reference clock from sideband IO.<br>2'b10: Input reference clock from LC PLL (cascade mode).<br>2'b11: Input reference clock from refclk_soc_pll (System PLL). |
| 9:8 | RW | 0x0 | lc_ref_clk_sel<br>Input Reference Clock source selector<br>This pin controls reference clock source<br>2'b00: Input reference clock from refclk_xtal<br>2'b01: Input reference clock from sideband IO.<br>2'b10: Input reference clock from RO PLL.<br>2'b11: Input reference clock from refclk_soc_pll (System PLL). |
| 7 | RW | 0x0 | pll_en<br>PLL Block Enable Signal.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | bias_en<br>Bias Block Enable Signal<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | bgr_en<br>Band Gap Reference Block Enable Signal.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | tx_aux_tx_mode<br>When hdptx_mode_sel is 1'b0, this bit controls the<br>i_aux_tx_mode of PHY.<br>Enables transmission in AUX mode. |
| 3 | RW | 0x0 | earc_rx_mode<br>When hdptx_mode_sel is 1'b1, this bit controls the<br>i_earc_rx_mode of PHY.<br>Enables CMDC receiver in eARC mode. |
| 2 | RW | 0x0 | earc_tx_mode<br>When hdptx_mode_sel is 1'b1, this bit controls the<br>i_earc_tx_mode of PHY.<br>Enables CMDC transmission in eARC mode. |
| 1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | hdptx_mode_sel<br>1'b0: earc_tx_mode/earc_rx_mode/aux_tx_mode is controlled by HDMITX controller<br>1'b1: earc_tx_mode/earc_rx_mode/aux_tx_mode is controlled by EDP controller or GRF. |

**HDPTXPHY_GRF_CON1**

Address: Operational Base + offset (0x0004)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | dbgclk_gate<br>1'b0: Gate debug clock.<br>1'b1: Do not gate debug clock. |
| 6:4 | RO | 0x0 | reserved |
| 3:0 | RW | 0x0 | dbgclk_sel<br>Debug clock select:<br>4'd0: hdptx_o_dig_refclk<br>4'd1: hdptx_o_mon_clk<br>4'd2: hdptx_o_earc_dmac_rxclk<br>4'd3: hdptx_o_tx_link_sym_clk<br>4'd4: hdptx_o_tx_hs_clk<br>4'd5: hdptx_i_tx_data_clk<br>4'd6: hdptx_o_hdmi_pixel_clk<br>4'd7: hdptx_o_aux_arc_rxdata<br>4'd8: hdptx_i_aux_earc_txdata_i<br>4'd9: hdptx_i_aux_tx_mode |

**HDPTXPHY_GRF_STATUS0**

Address: Operational Base + offset (0x0080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3 | RO | 0x0 | o_pll_lock_done<br>PLL Lock Indication<br>The pin is high when PLL locking is completed. This means that all the output clocks are at the correct frequency. |
| 2 | RO | 0x0 | o_phy_clk_rdy<br>Indicates PHY data path clock outputs are stable<br>1'b1: Clocks are ready<br>1'b0: Clocks are not ready |
| 1 | RO | 0x0 | o_phy_rdy<br>Indicates PHY lanes are ready for data transmission<br>1'b1: PHY lanes are ready<br>1'b0: PHY lanes are not ready |
| 0 | RO | 0x0 | o_sb_rdy<br>Indicates sideband calibrations are complete and ready for sideband transceiver operations<br>1'b1: Sideband block ready<br>1'b0: Sideband block not ready |

# 6.24 MIPICDPHY_GRF Register Description

There are two MIPICDPHY_GRF modules in RK3588.They have different base address.

## 6.24.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| MIPICDPHY_GRF_CON0 | 0x0000 | W | 0x00000000 | MIPICDPHY Control Register 0 |
| MIPICDPHY_GRF_CON1 | 0x0004 | W | 0x00000000 | MIPICDPHY Control Register 1 |

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| MIPICDPHY_GRF_STATUS0 | 0x0080 | W | 0x00000000 | MIPICDPHY Status Register 0 |
| MIPICDPHY_GRF_STATUS1 | 0x0084 | W | 0x00000000 | MIPICDPHY Status Register 1 |
| MIPICDPHY_GRF_STATUS2 | 0x0088 | W | 0x00000000 | MIPICDPHY Status Register 2 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.24.2 Detail Registers Description

### MIPICDPHY_GRF_CON0

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | dcphy_clamp_en<br>DCPHY output clamp enable<br>1'b0: Normal mode<br>1'b1: Clamp phy output to special value |
| 14:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | s_cphy_mode<br>C-PHY mode select signal of slave data lane. |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | m_cphy_mode<br>C-PHY mode select signal of master data lane. |

### MIPICDPHY_GRF_CON1

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | dcphy_hsclk_inv_sel<br>1'b0: Normal mode<br>1'b1: Invert M_TXWORDCLKHSCLK to controller. |
| 14 | RW | 0x0 | ppi_if_man_en<br>If ppi_if_man_en is 1, M_TXREQUESTESC0, M_TXTRIGGERESC0, M_TXCLKESCCLK and M_TXCLKESC0 are controlled by GRF. |
| 13:10 | RW | 0x0 | m_txtriggeresc<br>Escape mode transmit trigger 0.<br>If ppi_if_man_en is 1, M_TXTRIGGERESC0 is controlled by this bit. |
| 9 | RW | 0x0 | m_txrequestesc<br>Escape mode transmit request, high active.<br>If ppi_if_man_en is 1, M_TXREQUESTESC0 is controlled by this bit. |
| 8 | RW | 0x0 | txclkesc<br>Escape mode clock.<br>If ppi_if_man_en is 1, M_TXCLKESCCLK and M_TXCLKESC0 is controlled by this bit. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:4 | RW | 0x0 | s_forcerxmode<br>Force lane into receive mode/wait for stop state. Active high. |
| 3:0 | RW | 0x0 | m_forcetxstopmode<br>Force lane into transmit mode generate stop state. Active high. |

**MIPICDPHY_GRF_STATUS0**

Address: Operational Base + offset (0x0080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9 | RO | 0x0 | pll_cnt_done<br>When PLL_EN is set to high , PLL lock counter is started to generate a delay to get a stabilized clock. The lock counter expires when the count value reaches the value set as REG_PLL_LOCK_CNT(pll_con7[15:0]). Then, the interface signal PLL_CNT_DONE is asserted. |
| 8 | RO | 0x0 | m_stopstateclk<br>Lane is in stop state. Active high. |
| 7:4 | RO | 0x0 | s_stop_state<br>Lane is in stop state. Active high. |
| 3:0 | RO | 0x0 | m_stopstate<br>Data lane is in stop state. Active high. |

**MIPICDPHY_GRF_STATUS1**

Address: Operational Base + offset (0x0084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4:0 | RO | 0x00 | m_phyerr0lane<br>Master lane error status. |

**MIPICDPHY_GRF_STATUS2**

Address: Operational Base + offset (0x0088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:12 | RO | 0x0 | s_phyerr3<br>Slave lane error status. |
| 11:8 | RO | 0x0 | s_phyerr2<br>Slave lane error status. |
| 7:4 | RO | 0x0 | s_phyerr1<br>Slave lane error status. |
| 3:0 | RO | 0x0 | s_phyerr0<br>Slave lane error status. |

# 6.25 PMU1_IOC Register Description

## 6.25.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PMU1_IOC_GPIO0A_IOMUX_SEL_L | 0x0000 | W | 0x00000020 | GPIO0A IOMUX Select Low bits |
| PMU1_IOC_GPIO0A_IOMUX_SEL_H | 0x0004 | W | 0x00000000 | GPIO0A IOMUX Select High bits |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PMU1_IOC_GPIO0B_IOMUX_SEL_L | 0x0008 | W | 0x00000000 | GPIO0B IOMUX Select Low bits |
| PMU1_IOC_GPIO0A_DS_L | 0x0010 | W | 0x00001111 | GPIO0A Driver Strength Control Low bits |
| PMU1_IOC_GPIO0A_DS_H | 0x0014 | W | 0x00001111 | GPIO0A Driver Strength Control High bits |
| PMU1_IOC_GPIO0B_DS_L | 0x0018 | W | 0x00001111 | GPIO0B Driver Strength Control Low bits |
| PMU1_IOC_GPIO0A_P | 0x0020 | W | 0x0000C751 | GPIO0A Pull-up/down Control |
| PMU1_IOC_GPIO0B_P | 0x0024 | W | 0x00000030 | GPIO0B Pull-up/down Control |
| PMU1_IOC_GPIO0A_IE | 0x0028 | W | 0x000000FF | GPIO0A Input Enable Control |
| PMU1_IOC_GPIO0B_IE | 0x002C | W | 0x0000000F | GPIO0B Input Enable Control |
| PMU1_IOC_GPIO0A_SMT | 0x0030 | W | 0x00000000 | GPIO0A Schmitt Trigger Control |
| PMU1_IOC_GPIO0B_SMT | 0x0034 | W | 0x00000000 | GPIO0B Schmitt Trigger Control |
| PMU1_IOC_GPIO0A_PDIS | 0x0038 | W | 0x00000000 | GPIO0A Auto Pull-up/down disable Control |
| PMU1_IOC_GPIO0B_PDIS | 0x003C | W | 0x00000000 | GPIO0B Auto Pull-up/down disable Control |
| PMU1_IOC_XIN_CON | 0x0040 | W | 0x00000008 | OSC control Register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.25.2 Detail Registers Description

**PMU1_IOC_GPIO0A_IOMUX_SEL_L**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio0a3_sel<br>4'h0: GPIO<br>4'h1: PMIC_SLEEP2 |
| 11:8 | RW | 0x0 | gpio0a2_sel<br>4'h0: GPIO<br>4'h1: PMIC_SLEEP1<br>4'h2: TSADC_SHUT_M1 |
| 7:4 | RW | 0x2 | gpio0a1_sel<br>4'h0: GPIO<br>4'h1: TSADC_SHUT_ORG<br>4'h2: TSADC_SHUT |
| 3:0 | RW | 0x0 | gpio0a0_sel<br>4'h0: GPIO<br>4'h1: REFCLK_OUT |

**PMU1_IOC_GPIO0A_IOMUX_SEL_H**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:12 | RW | 0x0 | gpio0a7_sel<br>4'h0: GPIO<br>4'h1: PMIC_INT_L |
| 11:8 | RW | 0x0 | gpio0a6_sel<br>4'h0: GPIO<br>4'h1: SPI2_MOSI_M2<br>4'h2: I2C0_SDA_M0 |
| 7:4 | RW | 0x0 | gpio0a5_sel<br>4'h0: GPIO<br>4'h1: SPI2_CLK_M2<br>4'h2: SDMMC_PWREN<br>4'h3: PMU_DEBUG |
| 3:0 | RW | 0x0 | gpio0a4_sel<br>4'h0: GPIO<br>4'h1: SDMMC_DET |

**PMU1_IOC_GPIO0B_IOMUX_SEL_L**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio0b3_sel<br>4'h0: GPIO<br>4'h1: SPI2_MISO_M2<br>4'h2: I2C0_SCL_M0 |
| 11:8 | RW | 0x0 | gpio0b2_sel<br>4'h0: GPIO<br>4'h1: CLK32K_IN<br>4'h2: CLK32K_OUT0 |
| 7:4 | RW | 0x0 | gpio0b1_sel<br>4'h0: GPIO<br>4'h1: SPI2_CS0_M2<br>4'h2: I2C1_SDA_M1<br>4'h3: PWM5_M0<br>4'h4: UART0_TX_M1 |
| 3:0 | RW | 0x0 | gpio0b0_sel<br>4'h0: GPIO<br>4'h1: SPI2_CS1_M2<br>4'h2: I2C1_SCL_M1<br>4'h4: UART0_RX_M1 |

**PMU1_IOC_GPIO0A_DS_L**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:12 | RW | 0x1 | gpio0a3_ds<br>GPIO0A3 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 11:10 | RO | 0x0 | reserved |
| 9:8 | RW | 0x1 | gpio0a2_ds<br>GPIO0A2 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 7:6 | RO | 0x0 | reserved |
| 5:4 | RW | 0x1 | gpio0a1_ds<br>GPIO0A1 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 3:2 | RO | 0x0 | reserved |
| 1:0 | RW | 0x1 | gpio0a0_ds<br>GPIO0A0 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |

**PMU1_IOC_GPIO0A_DS_H**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13:12 | RW | 0x1 | gpio0a7_ds<br>GPIO0A7 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 11:10 | RO | 0x0 | reserved |
| 9:8 | RW | 0x1 | gpio0a6_ds<br>GPIO0A6 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:6 | RO | 0x0 | reserved |
| 5:4 | RW | 0x1 | gpio0a5_ds<br>GPIO0A5 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 3:2 | RO | 0x0 | reserved |
| 1:0 | RW | 0x1 | gpio0a4_ds<br>GPIO0A4 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |

**PMU1_IOC_GPIO0B_DS_L**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13:12 | RW | 0x1 | gpio0b3_ds<br>GPIO0B3 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 11:10 | RO | 0x0 | reserved |
| 9:8 | RW | 0x1 | gpio0b2_ds<br>GPIO0B2 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 7:6 | RO | 0x0 | reserved |
| 5:4 | RW | 0x1 | gpio0b1_ds<br>GPIO0B1 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 3:2 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1:0 | RW | 0x1 | gpio0b0_ds<br>GPIO0B0 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |

**PMU1_IOC_GPIO0A_P**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | gpio0a7_ps<br>GPIO0A7 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 14 | RW | 0x1 | gpio0a7_pe<br>GPIO0A7 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 13 | RW | 0x0 | gpio0a6_ps<br>GPIO0A6 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 12 | RW | 0x0 | gpio0a6_pe<br>GPIO0A6 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 11 | RW | 0x0 | gpio0a5_ps<br>GPIO0A5 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 10 | RW | 0x1 | gpio0a5_pe<br>GPIO0A5 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 9 | RW | 0x1 | gpio0a4_ps<br>GPIO0A4 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 8 | RW | 0x1 | gpio0a4_pe<br>GPIO0A4 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x0 | gpio0a3_ps<br>GPIO0A3 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 6 | RW | 0x1 | gpio0a3_pe<br>GPIO0A3 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 5 | RW | 0x0 | gpio0a2_ps<br>GPIO0A2 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 4 | RW | 0x1 | gpio0a2_pe<br>GPIO0A2 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 3 | RW | 0x0 | gpio0a1_ps<br>GPIO0A1 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 2 | RW | 0x0 | gpio0a1_pe<br>GPIO0A1 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 1 | RW | 0x0 | gpio0a0_ps<br>GPIO0A0 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 0 | RW | 0x1 | gpio0a0_pe<br>GPIO0A0 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

**PMU1_IOC_GPIO0B_P**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | gpio0b3_ps<br>GPIO0B3 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | gpio0b3_pe<br>GPIO0B3 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 5 | RW | 0x1 | gpio0b2_ps<br>GPIO0B2 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 4 | RW | 0x1 | gpio0b2_pe<br>GPIO0B2 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 3 | RW | 0x0 | gpio0b1_ps<br>GPIO0B1 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 2 | RW | 0x0 | gpio0b1_pe<br>GPIO0B1 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 1 | RW | 0x0 | gpio0b0_ps<br>GPIO0B0 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 0 | RW | 0x0 | gpio0b0_pe<br>GPIO0B0 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

**PMU1_IOC_GPIO0A_IE**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x1 | gpio0a7_ie<br>GPIO0A7 IE control<br>Active High input buffer enable |
| 6 | RW | 0x1 | gpio0a6_ie<br>GPIO0A6 IE control<br>Active High input buffer enable |
| 5 | RW | 0x1 | gpio0a5_ie<br>GPIO0A5 IE control<br>Active High input buffer enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x1 | gpio0a4_ie<br>GPIO0A4 IE control<br>Active High input buffer enable |
| 3 | RW | 0x1 | gpio0a3_ie<br>GPIO0A3 IE control<br>Active High input buffer enable |
| 2 | RW | 0x1 | gpio0a2_ie<br>GPIO0A2 IE control<br>Active High input buffer enable |
| 1 | RW | 0x1 | gpio0a1_ie<br>GPIO0A1 IE control<br>Active High input buffer enable |
| 0 | RW | 0x1 | gpio0a0_ie<br>GPIO0A0 IE control<br>Active High input buffer enable |

**PMU1_IOC_GPIO0B_IE**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x1 | gpio0b3_ie<br>GPIO0B3 IE control<br>Active High input buffer enable |
| 2 | RW | 0x1 | gpio0b2_ie<br>GPIO0B2 IE control<br>Active High input buffer enable |
| 1 | RW | 0x1 | gpio0b1_ie<br>GPIO0B1 IE control<br>Active High input buffer enable |
| 0 | RW | 0x1 | gpio0b0_ie<br>GPIO0B0 IE control<br>Active High input buffer enable |

**PMU1_IOC_GPIO0A_SMT**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | gpio0a7_smt<br>GPIO0A7 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 6 | RW | 0x0 | gpio0a6_smt<br>GPIO0A6 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | gpio0a5_smt<br>GPIO0A5 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 4 | RW | 0x0 | gpio0a4_smt<br>GPIO0A4 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 3 | RW | 0x0 | gpio0a3_smt<br>GPIO0A3 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 2 | RW | 0x0 | gpio0a2_smt<br>GPIO0A2 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 1 | RW | 0x0 | gpio0a1_smt<br>GPIO0A1 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 0 | RW | 0x0 | gpio0a0_smt<br>GPIO0A0 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

**PMU1_IOC_GPIO0B_SMT**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | gpio0b3_smt<br>GPIO0B3 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 2 | RW | 0x0 | gpio0b2_smt<br>GPIO0B2 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 1 | RW | 0x0 | gpio0b1_smt<br>GPIO0B1 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | gpio0b0_smt<br>GPIO0B0 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

**PMU1_IOC_GPIO0A_PDIS**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | gpio0a7_pull_dis<br>when 1'b1, disable GPIO0A7 pull up/down when output enable |
| 6 | RW | 0x0 | gpio0a6_pull_dis<br>when 1'b1, disable GPIO0A6 pull up/down when output enable |
| 5 | RW | 0x0 | gpio0a5_pull_dis<br>when 1'b1, disable GPIO0A5 pull up/down when output enable |
| 4 | RW | 0x0 | gpio0a4_pull_dis<br>when 1'b1, disable GPIO0A4 pull up/down when output enable |
| 3 | RW | 0x0 | gpio0a3_pull_dis<br>when 1'b1, disable GPIO0A3 pull up/down when output enable |
| 2 | RW | 0x0 | gpio0a2_pull_dis<br>when 1'b1, disable GPIO0A2 pull up/down when output enable |
| 1 | RW | 0x0 | gpio0a1_pull_dis<br>when 1'b1, disable GPIO0A1 pull up/down when output enable |
| 0 | RW | 0x0 | gpio0a0_pull_dis<br>when 1'b1, disable GPIO0A0 pull up/down when output enable |

**PMU1_IOC_GPIO0B_PDIS**

Address: Operational Base + offset (0x003C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | gpio0b3_pull_dis<br>when 1'b1, disable GPIO0B3 pull up/down when output enable |
| 2 | RW | 0x0 | gpio0b2_pull_dis<br>when 1'b1, disable GPIO0B2 pull up/down when output enable |
| 1 | RW | 0x0 | gpio0b1_pull_dis<br>when 1'b1, disable GPIO0B1 pull up/down when output enable |
| 0 | RW | 0x0 | gpio0b0_pull_dis<br>when 1'b1, disable GPIO0B0 pull up/down when output enable |

**PMU1_IOC_XIN_CON**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:2 | RW | 0x2 | xin_osc_sf<br>XIN OSC frequency pin selection<br>2'b00: 1MHz - 12MHz<br>2'b01: 26.1MHz - 36MHz<br>2'b10: 12.1MHz - 26MHz<br>2'b11: 36.1MHz - 52MHz |
| 1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | xin_osc_en<br>XIN OSC enable |

# 6.26 PMU2_IOC Register Description

## 6.26.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PMU2_IOC_GPIO0B_IOMUX_SEL_H | 0x0000 | W | 0x00000000 | GPIO0B IOMUX Select High bits |
| PMU2_IOC_GPIO0C_IOMUX_SEL_L | 0x0004 | W | 0x00000000 | GPIO0C IOMUX Select Low bits |
| PMU2_IOC_GPIO0C_IOMUX_SEL_H | 0x0008 | W | 0x00000000 | GPIO0C IOMUX Select High bits |
| PMU2_IOC_GPIO0D_IOMUX_SEL_L | 0x000C | W | 0x00000000 | GPIO0D IOMUX Select Low bits |
| PMU2_IOC_GPIO0D_IOMUX_SEL_H | 0x0010 | W | 0x00000000 | GPIO0D IOMUX Select High bits |
| PMU2_IOC_GPIO0B_DS_H | 0x0014 | W | 0x00006660 | GPIO0B Driver Strength Control High bits |
| PMU2_IOC_GPIO0C_DS_L | 0x0018 | W | 0x00006666 | GPIO0C Driver Strength Control Low bits |
| PMU2_IOC_GPIO0C_DS_H | 0x001C | W | 0x00006666 | GPIO0C Driver Strength Control High bits |
| PMU2_IOC_GPIO0D_DS_L | 0x0020 | W | 0x00006666 | GPIO0D Driver Strength Control Low bits |
| PMU2_IOC_GPIO0D_DS_H | 0x0024 | W | 0x00000666 | GPIO0D Driver Strength Control High bits |
| PMU2_IOC_GPIO0B_P | 0x0028 | W | 0x00005400 | GPIO0B Pull-up/down Control |
| PMU2_IOC_GPIO0C_P | 0x002C | W | 0x00007D55 | GPIO0C Pull-up/down Control |
| PMU2_IOC_GPIO0D_P | 0x0030 | W | 0x00001FFD | GPIO0D Pull-up/down Control |
| PMU2_IOC_GPIO0B_IE | 0x0034 | W | 0x000000E0 | GPIO0B Input Enable Control |
| PMU2_IOC_GPIO0C_IE | 0x0038 | W | 0x000000FF | GPIO0C Input Enable Control |
| PMU2_IOC_GPIO0D_IE | 0x003C | W | 0x0000007F | GPIO0D Input Enable Control |
| PMU2_IOC_GPIO0B_SMT | 0x0040 | W | 0x00000000 | GPIO0B Schmitt Trigger Control |
| PMU2_IOC_GPIO0C_SMT | 0x0044 | W | 0x00000000 | GPIO0C Schmitt Trigger Control |
| PMU2_IOC_GPIO0D_SMT | 0x0048 | W | 0x00000000 | GPIO0D Schmitt Trigger Control |
| PMU2_IOC_GPIO0B_PDIS | 0x004C | W | 0x00000000 | GPIO0B Auto Pull-up/down disable Control |
| PMU2_IOC_GPIO0C_PDIS | 0x0050 | W | 0x00000000 | GPIO0C Auto Pull-up/down disable Control |
| PMU2_IOC_GPIO0D_PDIS | 0x0054 | W | 0x00000000 | GPIO0D Auto Pull-up/down disable Control |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

Rockchip Confidential

## 6.26.2 Detail Registers Description

**PMU2_IOC_GPIO0B_IOMUX_SEL_H**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio0b7_sel<br>4'h0: GPIO<br>4'h1: I2S1_LRCK_M1<br>4'h3: PWM0_M0<br>4'h8: Refer to BUS_IOC.GPIO0B_IOMUX_SEL_H |
| 11:8 | RW | 0x0 | gpio0b6_sel<br>4'h0: GPIO<br>4'h1: I2S1_SCLK_M1<br>4'h2: JTAG_TMS_M2<br>4'h8: Refer to BUS_IOC.GPIO0B_IOMUX_SEL_H |
| 7:4 | RW | 0x0 | gpio0b5_sel<br>4'h0: GPIO<br>4'h1: I2S1_MCLK_M1<br>4'h2: JTAG_TCK_M2<br>4'h8: Refer to BUS_IOC.GPIO0B_IOMUX_SEL_H |
| 3:0 | RO | 0x0 | reserved |

**PMU2_IOC_GPIO0C_IOMUX_SEL_L**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio0c3_sel<br>4'h0: GPIO<br>4'h1: PMIC_SLEEP5 |
| 11:8 | RW | 0x0 | gpio0c2_sel<br>4'h0: GPIO<br>4'h1: PMIC_SLEEP4 |
| 7:4 | RW | 0x0 | gpio0c1_sel<br>4'h0: GPIO<br>4'h1: PMIC_SLEEP3 |
| 3:0 | RW | 0x0 | gpio0c0_sel<br>4'h0: GPIO<br>4'h2: PDM0_CLK0_M1<br>4'h3: PWM1_M0<br>4'h8: Refer to BUS_IOC.GPIO0C_IOMUX_SEL_L |

**PMU2_IOC_GPIO0C_IOMUX_SEL_H**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:12 | RW | 0x0 | gpio0c7_sel<br>4'h0: GPIO<br>4'h1: I2S1_SDI2_M1<br>4'h2: PDM0_SDI0_M1<br>4'h8: Refer to BUS_IOC.GPIO0C_IOMUX_SEL_H |
| 11:8 | RW | 0x0 | gpio0c6_sel<br>4'h0: GPIO<br>4'h1: I2S1_SDI1_M1<br>4'h2: NPU_AVS<br>4'h4: UART0_RTSN<br>4'h8: Refer to BUS_IOC.GPIO0C_IOMUX_SEL_H |
| 7:4 | RW | 0x0 | gpio0c5_sel<br>4'h0: GPIO<br>4'h1: I2S1_SDI0_M1<br>4'h2: GPU_AVS<br>4'h4: UART0_TX_M0<br>4'h8: Refer to BUS_IOC.GPIO0C_IOMUX_SEL_H |
| 3:0 | RW | 0x0 | gpio0c4_sel<br>4'h0: GPIO<br>4'h2: PDM0_CLK1_M1<br>4'h3: PWM2_M0<br>4'h4: UART0_RX_M0<br>4'h8: Refer to BUS_IOC.GPIO0C_IOMUX_SEL_H |

**PMU2_IOC_GPIO0D_IOMUX_SEL_L**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio0d3_sel<br>4'h0: GPIO<br>4'h1: LITCPU_AVS<br>4'h8: Refer to BUS_IOC.GPIO0D_IOMUX_SEL_L |
| 11:8 | RW | 0x0 | gpio0d2_sel<br>4'h0: GPIO<br>4'h1: I2S1_SDO1_M1<br>4'h3: I2C0_SDA_M2<br>4'h8: Refer to BUS_IOC.GPIO0D_IOMUX_SEL_L |
| 7:4 | RW | 0x0 | gpio0d1_sel<br>4'h0: GPIO<br>4'h1: I2S1_SDO0_M1<br>4'h2: CPU_BIG0_AVS<br>4'h3: I2C0_SCL_M2<br>4'h4: UART0_CTSN<br>4'h8: Refer to BUS_IOC.GPIO0D_IOMUX_SEL_L |
| 3:0 | RW | 0x0 | gpio0d0_sel<br>4'h0: GPIO<br>4'h1: I2S1_SDI3_M1<br>4'h2: PDM0_SDI1_M1<br>4'h8: Refer to BUS_IOC.GPIO0D_IOMUX_SEL_L |

**PMU2_IOC_GPIO0D_IOMUX_SEL_H**

Address: Operational Base + offset (0x0010)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11:8 | RW | 0x0 | gpio0d6_sel<br>4'h0: GPIO<br>4'h1: PMIC_SLEEP6<br>4'h2: PDM0_SDI3_M1 |
| 7:4 | RW | 0x0 | gpio0d5_sel<br>4'h0: GPIO<br>4'h1: I2S1_SDO3_M1<br>4'h2: CPU_BIG1_AVS<br>4'h8: Refer to BUS_IOC.GPIO0D_IOMUX_SEL_H |
| 3:0 | RW | 0x0 | gpio0d4_sel<br>4'h0: GPIO<br>4'h1: I2S1_SDO2_M1<br>4'h2: PDM0_SDI2_M1<br>4'h3: PWM3_IR_M0<br>4'h8: Refer to BUS_IOC.GPIO0D_IOMUX_SEL_H |

**PMU2_IOC_GPIO0B_DS_H**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x6 | gpio0b7_ds<br>GPIO0B7 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x6 | gpio0b6_ds<br>GPIO0B6 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6:4 | RW | 0x6 | gpio0b5_ds<br>GPIO0B5 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3:0 | RO | 0x0 | reserved |

**PMU2_IOC_GPIO0C_DS_L**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x6 | gpio0c3_ds<br>GPIO0C3 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x6 | gpio0c2_ds<br>GPIO0C2 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x6 | gpio0c1_ds<br>GPIO0C1 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2:0 | RW | 0x6 | gpio0c0_ds<br>GPIO0C0 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**PMU2_IOC_GPIO0C_DS_H**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x6 | gpio0c7_ds<br>GPIO0C7 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x6 | gpio0c6_ds<br>GPIO0C6 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x6 | gpio0c5_ds<br>GPIO0C5 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2:0 | RW | 0x6 | gpio0c4_ds<br>GPIO0C4 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**PMU2_IOC_GPIO0D_DS_L**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x6 | gpio0d3_ds<br>GPIO0D3 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x6 | gpio0d2_ds<br>GPIO0D2 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x6 | gpio0d1_ds<br>GPIO0D1 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2:0 | RW | 0x6 | gpio0d0_ds<br>GPIO0D0 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**PMU2_IOC_GPIO0D_DS_H**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10:8 | RW | 0x6 | gpio0d6_ds<br>GPIO0D6 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x6 | gpio0d5_ds<br>GPIO0D5 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio0d4_ds<br>GPIO0D4 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**PMU2_IOC_GPIO0B_P**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x0 | gpio0b7_ps<br>GPIO0B7 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 14 | RW | 0x1 | gpio0b7_pe<br>GPIO0B7 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 13 | RW | 0x0 | gpio0b6_ps<br>GPIO0B6 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 12 | RW | 0x1 | gpio0b6_pe<br>GPIO0B6 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 11 | RW | 0x0 | gpio0b5_ps<br>GPIO0B5 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 10 | RW | 0x1 | gpio0b5_pe<br>GPIO0B5 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 9:0 | RO | 0x000 | reserved |

**PMU2_IOC_GPIO0C_P**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | gpio0c7_ps<br>GPIO0C7 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 14 | RW | 0x1 | gpio0c7_pe<br>GPIO0C7 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 13 | RW | 0x1 | gpio0c6_ps<br>GPIO0C6 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x1 | gpio0c6_pe<br>GPIO0C6 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 11 | RW | 0x1 | gpio0c5_ps<br>GPIO0C5 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 10 | RW | 0x1 | gpio0c5_pe<br>GPIO0C5 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 9 | RW | 0x0 | gpio0c4_ps<br>GPIO0C4 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 8 | RW | 0x1 | gpio0c4_pe<br>GPIO0C4 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 7 | RW | 0x0 | gpio0c3_ps<br>GPIO0C3 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 6 | RW | 0x1 | gpio0c3_pe<br>GPIO0C3 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 5 | RW | 0x0 | gpio0c2_ps<br>GPIO0C2 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 4 | RW | 0x1 | gpio0c2_pe<br>GPIO0C2 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 3 | RW | 0x0 | gpio0c1_ps<br>GPIO0C1 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 2 | RW | 0x1 | gpio0c1_pe<br>GPIO0C1 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | gpio0c0_ps<br>GPIO0C0 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 0 | RW | 0x1 | gpio0c0_pe<br>GPIO0C0 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

**PMU2_IOC_GPIO0D_P**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | gpio0d6_ps<br>GPIO0D6 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 12 | RW | 0x1 | gpio0d6_pe<br>GPIO0D6 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 11 | RW | 0x1 | gpio0d5_ps<br>GPIO0D5 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 10 | RW | 0x1 | gpio0d5_pe<br>GPIO0D5 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 9 | RW | 0x1 | gpio0d4_ps<br>GPIO0D4 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 8 | RW | 0x1 | gpio0d4_pe<br>GPIO0D4 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 7 | RW | 0x1 | gpio0d3_ps<br>GPIO0D3 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x1 | gpio0d3_pe<br>GPIO0D3 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 5 | RW | 0x1 | gpio0d2_ps<br>GPIO0D2 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 4 | RW | 0x1 | gpio0d2_pe<br>GPIO0D2 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 3 | RW | 0x1 | gpio0d1_ps<br>GPIO0D1 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 2 | RW | 0x1 | gpio0d1_pe<br>GPIO0D1 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 1 | RW | 0x0 | gpio0d0_ps<br>GPIO0D0 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 0 | RW | 0x1 | gpio0d0_pe<br>GPIO0D0 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

**PMU2_IOC_GPIO0B_IE**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x1 | gpio0b7_ie<br>GPIO0B7 IE control<br>Active High input buffer enable |
| 6 | RW | 0x1 | gpio0b6_ie<br>GPIO0B6 IE control<br>Active High input buffer enable |
| 5 | RW | 0x1 | gpio0b5_ie<br>GPIO0B5 IE control<br>Active High input buffer enable |
| 4:0 | RO | 0x00 | reserved |

Rockchip Confidencial

**PMU2_IOC_GPIO0C_IE**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x1 | gpio0c7_ie<br>GPIO0C7 IE control<br>Active High input buffer enable |
| 6 | RW | 0x1 | gpio0c6_ie<br>GPIO0C6 IE control<br>Active High input buffer enable |
| 5 | RW | 0x1 | gpio0c5_ie<br>GPIO0C5 IE control<br>Active High input buffer enable |
| 4 | RW | 0x1 | gpio0c4_ie<br>GPIO0C4 IE control<br>Active High input buffer enable |
| 3 | RW | 0x1 | gpio0c3_ie<br>GPIO0C3 IE control<br>Active High input buffer enable |
| 2 | RW | 0x1 | gpio0c2_ie<br>GPIO0C2 IE control<br>Active High input buffer enable |
| 1 | RW | 0x1 | gpio0c1_ie<br>GPIO0C1 IE control<br>Active High input buffer enable |
| 0 | RW | 0x1 | gpio0c0_ie<br>GPIO0C0 IE control<br>Active High input buffer enable |

**PMU2_IOC_GPIO0D_IE**

Address: Operational Base + offset (0x003C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x1 | gpio0d6_ie<br>GPIO0D6 IE control<br>Active High input buffer enable |
| 5 | RW | 0x1 | gpio0d5_ie<br>GPIO0D5 IE control<br>Active High input buffer enable |
| 4 | RW | 0x1 | gpio0d4_ie<br>GPIO0D4 IE control<br>Active High input buffer enable |
| 3 | RW | 0x1 | gpio0d3_ie<br>GPIO0D3 IE control<br>Active High input buffer enable |
| 2 | RW | 0x1 | gpio0d2_ie<br>GPIO0D2 IE control<br>Active High input buffer enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x1 | gpio0d1_ie<br>GPIO0D1 IE control<br>Active High input buffer enable |
| 0 | RW | 0x1 | gpio0d0_ie<br>GPIO0D0 IE control<br>Active High input buffer enable |

**PMU2_IOC_GPIO0B_SMT**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | gpio0b7_smt<br>GPIO0B7 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 6 | RW | 0x0 | gpio0b6_smt<br>GPIO0B6 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 5 | RW | 0x0 | gpio0b5_smt<br>GPIO0B5 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 4:0 | RO | 0x00 | reserved |

**PMU2_IOC_GPIO0C_SMT**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | gpio0c7_smt<br>GPIO0C7 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 6 | RW | 0x0 | gpio0c6_smt<br>GPIO0C6 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 5 | RW | 0x0 | gpio0c5_smt<br>GPIO0C5 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | gpio0c4_smt<br>GPIO0C4 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 3 | RW | 0x0 | gpio0c3_smt<br>GPIO0C3 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 2 | RW | 0x0 | gpio0c2_smt<br>GPIO0C2 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 1 | RW | 0x0 | gpio0c1_smt<br>GPIO0C1 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 0 | RW | 0x0 | gpio0c0_smt<br>GPIO0C0 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

**PMU2_IOC_GPIO0D_SMT**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x0 | gpio0d6_smt<br>GPIO0D6 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 5 | RW | 0x0 | gpio0d5_smt<br>GPIO0D5 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 4 | RW | 0x0 | gpio0d4_smt<br>GPIO0D4 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 3 | RW | 0x0 | gpio0d3_smt<br>GPIO0D3 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | gpio0d2_smt<br>GPIO0D2 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 1 | RW | 0x0 | gpio0d1_smt<br>GPIO0D1 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 0 | RW | 0x0 | gpio0d0_smt<br>GPIO0D0 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

**PMU2_IOC_GPIO0B_PDIS**

Address: Operational Base + offset (0x004C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | gpio0b7_pull_dis<br>when 1'b1, disable GPIO0B7 pull up/down when output enable |
| 6 | RW | 0x0 | gpio0b6_pull_dis<br>when 1'b1, disable GPIO0B6 pull up/down when output enable |
| 5 | RW | 0x0 | gpio0b5_pull_dis<br>when 1'b1, disable GPIO0B5 pull up/down when output enable |
| 4:0 | RO | 0x00 | reserved |

**PMU2_IOC_GPIO0C_PDIS**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | gpio0c7_pull_dis<br>when 1'b1, disable GPIO0C7 pull up/down when output enable |
| 6 | RW | 0x0 | gpio0c6_pull_dis<br>when 1'b1, disable GPIO0C6 pull up/down when output enable |
| 5 | RW | 0x0 | gpio0c5_pull_dis<br>when 1'b1, disable GPIO0C5 pull up/down when output enable |
| 4 | RW | 0x0 | gpio0c4_pull_dis<br>when 1'b1, disable GPIO0C4 pull up/down when output enable |
| 3 | RW | 0x0 | gpio0c3_pull_dis<br>when 1'b1, disable GPIO0C3 pull up/down when output enable |
| 2 | RW | 0x0 | gpio0c2_pull_dis<br>when 1'b1, disable GPIO0C2 pull up/down when output enable |
| 1 | RW | 0x0 | gpio0c1_pull_dis<br>when 1'b1, disable GPIO0C1 pull up/down when output enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | gpio0c0_pull_dis<br>when 1'b1, disable GPIO0C0 pull up/down when output enable |

**PMU2_IOC_GPIO0D_PDIS**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x0 | gpio0d6_pull_dis<br>when 1'b1, disable GPIO0D6 pull up/down when output enable |
| 5 | RW | 0x0 | gpio0d5_pull_dis<br>when 1'b1, disable GPIO0D5 pull up/down when output enable |
| 4 | RW | 0x0 | gpio0d4_pull_dis<br>when 1'b1, disable GPIO0D4 pull up/down when output enable |
| 3 | RW | 0x0 | gpio0d3_pull_dis<br>when 1'b1, disable GPIO0D3 pull up/down when output enable |
| 2 | RW | 0x0 | gpio0d2_pull_dis<br>when 1'b1, disable GPIO0D2 pull up/down when output enable |
| 1 | RW | 0x0 | gpio0d1_pull_dis<br>when 1'b1, disable GPIO0D1 pull up/down when output enable |
| 0 | RW | 0x0 | gpio0d0_pull_dis<br>when 1'b1, disable GPIO0D0 pull up/down when output enable |

# 6.27 BUS_IOC Register Description

## 6.27.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| BUS_IOC_GPIO0B_IOMUX_SEL_H | 0x000C | W | 0x00000000 | GPIO0B IOMUX Select High bits |
| BUS_IOC_GPIO0C_IOMUX_SEL_L | 0x0010 | W | 0x00000000 | GPIO0C IOMUX Select Low bits |
| BUS_IOC_GPIO0C_IOMUX_SEL_H | 0x0014 | W | 0x00000000 | GPIO0C IOMUX Select High bits |
| BUS_IOC_GPIO0D_IOMUX_SEL_L | 0x0018 | W | 0x00000000 | GPIO0D IOMUX Select Low bits |
| BUS_IOC_GPIO0D_IOMUX_SEL_H | 0x001C | W | 0x00000000 | GPIO0D IOMUX Select High bits |
| BUS_IOC_GPIO1A_IOMUX_SEL_L | 0x0020 | W | 0x00000000 | GPIO1A IOMUX Select Low bits |
| BUS_IOC_GPIO1A_IOMUX_SEL_H | 0x0024 | W | 0x00000000 | GPIO1A IOMUX Select High bits |
| BUS_IOC_GPIO1B_IOMUX_SEL_L | 0x0028 | W | 0x00000000 | GPIO1B IOMUX Select Low bits |
| BUS_IOC_GPIO1B_IOMUX_SEL_H | 0x002C | W | 0x00000000 | GPIO1B IOMUX Select High bits |
| BUS_IOC_GPIO1C_IOMUX_SEL_L | 0x0030 | W | 0x00000000 | GPIO1C IOMUX Select Low bits |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| BUS_IOC_GPIO1C_IOMUX_SEL_H | 0x0034 | W | 0x00000000 | GPIO1C IOMUX Select High bits |
| BUS_IOC_GPIO1D_IOMUX_SEL_L | 0x0038 | W | 0x00000000 | GPIO1D IOMUX Select Low bits |
| BUS_IOC_GPIO1D_IOMUX_SEL_H | 0x003C | W | 0x00000000 | GPIO1D IOMUX Select High bits |
| BUS_IOC_GPIO2A_IOMUX_SEL_L | 0x0040 | W | 0x00000000 | GPIO2A IOMUX Select Low bits |
| BUS_IOC_GPIO2A_IOMUX_SEL_H | 0x0044 | W | 0x00000000 | GPIO2A IOMUX Select High bits |
| BUS_IOC_GPIO2B_IOMUX_SEL_L | 0x0048 | W | 0x00000000 | GPIO2B IOMUX Select Low bits |
| BUS_IOC_GPIO2B_IOMUX_SEL_H | 0x004C | W | 0x00000000 | GPIO2B IOMUX Select High bits |
| BUS_IOC_GPIO2C_IOMUX_SEL_L | 0x0050 | W | 0x00000000 | GPIO2C IOMUX Select Low bits |
| BUS_IOC_GPIO2C_IOMUX_SEL_H | 0x0054 | W | 0x00000000 | GPIO2C IOMUX Select High bits |
| BUS_IOC_GPIO2D_IOMUX_SEL_L | 0x0058 | W | 0x00000000 | GPIO2D IOMUX Select Low bits |
| BUS_IOC_GPIO2D_IOMUX_SEL_H | 0x005C | W | 0x00000000 | GPIO2D IOMUX Select High bits |
| BUS_IOC_GPIO3A_IOMUX_SEL_L | 0x0060 | W | 0x00000000 | GPIO3A IOMUX Select Low bits |
| BUS_IOC_GPIO3A_IOMUX_SEL_H | 0x0064 | W | 0x00000000 | GPIO3A IOMUX Select High bits |
| BUS_IOC_GPIO3B_IOMUX_SEL_L | 0x0068 | W | 0x00000000 | GPIO3B IOMUX Select Low bits |
| BUS_IOC_GPIO3B_IOMUX_SEL_H | 0x006C | W | 0x00000000 | GPIO3B IOMUX Select High bits |
| BUS_IOC_GPIO3C_IOMUX_SEL_L | 0x0070 | W | 0x00000000 | GPIO3C IOMUX Select Low bits |
| BUS_IOC_GPIO3C_IOMUX_SEL_H | 0x0074 | W | 0x00000000 | GPIO3C IOMUX Select High bits |
| BUS_IOC_GPIO3D_IOMUX_SEL_L | 0x0078 | W | 0x00000000 | GPIO3D IOMUX Select Low bits |
| BUS_IOC_GPIO3D_IOMUX_SEL_H | 0x007C | W | 0x00000000 | GPIO3D IOMUX Select High bits |
| BUS_IOC_GPIO4A_IOMUX_SEL_L | 0x0080 | W | 0x00000000 | GPIO4A IOMUX Select Low bits |
| BUS_IOC_GPIO4A_IOMUX_SEL_H | 0x0084 | W | 0x00000000 | GPIO4A IOMUX Select High bits |
| BUS_IOC_GPIO4B_IOMUX_SEL_L | 0x0088 | W | 0x00000000 | GPIO4B IOMUX Select Low bits |
| BUS_IOC_GPIO4B_IOMUX_SEL_H | 0x008C | W | 0x00000000 | GPIO4B IOMUX Select High bits |
| BUS_IOC_GPIO4C_IOMUX_SEL_L | 0x0090 | W | 0x00000000 | GPIO4C IOMUX Select Low bits |
| BUS_IOC_GPIO4C_IOMUX_SEL_H | 0x0094 | W | 0x00000000 | GPIO4C IOMUX Select High bits |
| BUS_IOC_GPIO4D_IOMUX_SEL_L | 0x0098 | W | 0x00005500 | GPIO4D IOMUX Select Low bits |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| BUS_IOC_GPIO4D_IOMUX_SEL_H | 0x009C | W | 0x00000000 | GPIO4D IOMUX Select High bits |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.27.2 Detail Registers Description

### BUS_IOC_GPIO0B_IOMUX_SEL_H

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio0b7_sel<br>4'h8: SPI0_CS1_M0<br>4'h9: I2C2_SCL_M0<br>4'hb: CAN0_TX_M0<br>4'hc: PCIE30X1_1_PERSTN_M0 |
| 11:8 | RW | 0x0 | gpio0b6_sel<br>4'h9: I2C1_SDA_M0<br>4'ha: UART2_RX_M0<br>4'hc: PCIE30X1_1_WAKEN_M0 |
| 7:4 | RW | 0x0 | gpio0b5_sel<br>4'h9: I2C1_SCL_M0<br>4'ha: UART2_TX_M0<br>4'hc: PCIE30X1_1_CLKREQN_M0 |
| 3:0 | RO | 0x0 | reserved |

### BUS_IOC_GPIO0C_IOMUX_SEL_L

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3:0 | RW | 0x0 | gpio0c0_sel<br>4'h8: SPI0_MOSI_M0<br>4'h9: I2C2_SDA_M0<br>4'hb: CAN0_RX_M0<br>4'hc: PCIE30X1_0_CLKREQN_M0 |

### BUS_IOC_GPIO0C_IOMUX_SEL_H

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:12 | RW | 0x0 | gpio0c7_sel<br>4'h8: SPI0_MISO_M0<br>4'h9: I2C6_SDA_M0<br>4'ha: UART1_RTSN_M2<br>4'hb: PWM6_M0<br>4'hc: PCIE30X4_WAKEN_M0 |
| 11:8 | RW | 0x0 | gpio0c6_sel<br>4'h8: SPI0_CLK_M0<br>4'hb: PWM5_M1<br>4'hc: PCIE30X4_CLKREQN_M0<br>4'hd: SATA_CP_POD |
| 7:4 | RW | 0x0 | gpio0c5_sel<br>4'h9: I2C4_SCL_M2<br>4'ha: DP1_HPDIN_M1<br>4'hb: PWM4_M0<br>4'hc: PCIE30X1_0_PERSTN_M0 |
| 3:0 | RW | 0x0 | gpio0c4_sel<br>4'h9: I2C4_SDA_M2<br>4'ha: DP0_HPDIN_M1<br>4'hc: PCIE30X1_0_WAKEN_M0 |

**BUS_IOC_GPIO0D_IOMUX_SEL_L**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio0d3_sel<br>4'h8: SPI3_CLK_M2 |
| 11:8 | RW | 0x0 | gpio0d2_sel<br>4'h8: SPI3_MOSI_M2<br>4'ha: UART1_RX_M2<br>4'hb: HDMI_RX_SCL_M0<br>4'hc: PCIE30X2_WAKEN_M0<br>4'hd: HDMI_TX1_CEC_M1 |
| 7:4 | RW | 0x0 | gpio0d1_sel<br>4'h8: SPI0_CS0_M0<br>4'ha: UART1_TX_M2<br>4'hb: HDMI_RX_SDA_M0<br>4'hc: PCIE30X2_CLKREQN_M0<br>4'hd: HDMI_TX0_CEC_M1 |
| 3:0 | RW | 0x0 | gpio0d0_sel<br>4'h8: SPI3_MISO_M2<br>4'h9: I2C6_SCL_M0<br>4'ha: UART1_CTSN_M2<br>4'hb: PWM7_IR_M0<br>4'hc: PCIE30X4_PERSTN_M0 |

**BUS_IOC_GPIO0D_IOMUX_SEL_H**

Address: Operational Base + offset (0x001C)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7:4 | RW | 0x0 | gpio0d5_sel<br>4'h8: SPI3_CS1_M2<br>4'h9: I2C1_SDA_M2<br>4'ha: CAN2_TX_M1<br>4'hb: HDMI_TX0_SCL_M1<br>4'hd: SATA_MP_SWITCH |
| 3:0 | RW | 0x0 | gpio0d4_sel<br>4'h8: SPI3_CS0_M2<br>4'h9: I2C1_SCL_M2<br>4'ha: CAN2_RX_M1<br>4'hb: HDMI_TX0_SDA_M1<br>4'hc: PCIE30X2_PERSTN_M0<br>4'hd: SATA_CPDET |

**BUS_IOC_GPIO1A_IOMUX_SEL_L**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio1a3_sel<br>4'h0: GPIO<br>4'h5: HDMI_TX1_SDA_M2<br>4'h8: SPI4_CS0_M2<br>4'h9: I2C4_SCL_M3<br>4'ha: UART6_CTSN_M1<br>4'hb: PWM1_M2 |
| 11:8 | RW | 0x0 | gpio1a2_sel<br>4'h0: GPIO<br>4'h1: VOP_POST_EMPTY<br>4'h8: SPI4_CLK_M2<br>4'h9: I2C4_SDA_M3<br>4'ha: UART6_RTSN_M1<br>4'hb: PWM0_M2 |
| 7:4 | RW | 0x0 | gpio1a1_sel<br>4'h0: GPIO<br>4'h4: PCIE30X1_1_WAKEN_M2<br>4'h5: DP1_HPDIN_M2<br>4'h6: SATA1_ACT_LED_M1<br>4'h8: SPI4_MOSI_M2<br>4'h9: I2C2_SCL_M4<br>4'ha: UART6_TX_M1 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RW | 0x0 | gpio1a0_sel<br>4'h0: GPIO<br>4'h4: PCIE30X1_1_CLKREQN_M2<br>4'h5: DP0_HPDIN_M2<br>4'h7: HDMI_DEBUG6<br>4'h8: SPI4_MISO_M2<br>4'h9: I2C2_SDA_M4<br>4'ha: UART6_RX_M1 |

**BUS_IOC_GPIO1A_IOMUX_SEL_H**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio1a7_sel<br>4'h0: GPIO<br>4'h2: PDM1_SDI0_M1<br>4'h4: PCIE30X1_1_PERSTN_M2<br>4'h7: HDMI_DEBUG0<br>4'h8: SPI2_CS0_M0<br>4'hb: PWM3_IR_M3 |
| 11:8 | RW | 0x0 | gpio1a6_sel<br>4'h0: GPIO<br>4'h5: HDMI_TX1_HPD_M0<br>4'h8: SPI2_CLK_M0 |
| 7:4 | RW | 0x0 | gpio1a5_sel<br>4'h0: GPIO<br>4'h5: HDMI_TX0_HPD_M0<br>4'h8: SPI2_MOSI_M0 |
| 3:0 | RW | 0x0 | gpio1a4_sel<br>4'h0: GPIO<br>4'h5: HDMI_TX1_SCL_M2<br>4'h8: SPI2_MISO_M0 |

**BUS_IOC_GPIO1B_IOMUX_SEL_L**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio1b3_sel<br>4'h0: GPIO<br>4'h2: PDM1_CLK1_M1<br>4'h4: PCIE30X1_0_WAKEN_M2<br>4'h6: SATA0_ACT_LED_M1<br>4'h7: HDMI_DEBUG4<br>4'h8: SPI0_CLK_M2<br>4'ha: UART4_TX_M2 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:8 | RW | 0x0 | gpio1b2_sel<br>4'h0: GPIO<br>4'h2: PDM1_SDI3_M1<br>4'h4: PCIE30X4_PERSTN_M3<br>4'h7: HDMI_DEBUG3<br>4'h8: SPI0_MOSI_M2<br>4'ha: UART4_RX_M2 |
| 7:4 | RW | 0x0 | gpio1b1_sel<br>4'h0: GPIO<br>4'h2: PDM1_SDI2_M1<br>4'h4: PCIE30X4_WAKEN_M3<br>4'h7: HDMI_DEBUG2<br>4'h8: SPI0_MISO_M2 |
| 3:0 | RW | 0x0 | gpio1b0_sel<br>4'h0: GPIO<br>4'h2: PDM1_SDI1_M1<br>4'h4: PCIE30X4_CLKREQN_M3<br>4'h7: HDMI_DEBUG1<br>4'h8: SPI2_CS1_M0 |

**BUS_IOC_GPIO1B_IOMUX_SEL_H**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio1b7_sel<br>4'h0: GPIO<br>4'h2: MIPI_CAMERA2_CLK_M0<br>4'h3: SPDIF1_TX_M0<br>4'h4: PCIE30X2_PERSTN_M3<br>4'h5: HDMI_RX_CEC_M2<br>4'h6: SATA2_ACT_LED_M1<br>4'h9: I2C5_SDA_M3<br>4'ha: UART1_RX_M1<br>4'hb: PWM13_M2 |
| 11:8 | RW | 0x0 | gpio1b6_sel<br>4'h0: GPIO<br>4'h2: MIPI_CAMERA1_CLK_M0<br>4'h3: SPDIF0_TX_M0<br>4'h4: PCIE30X2_WAKEN_M3<br>4'h5: HDMI_RX_HPDOUT_M2<br>4'h9: I2C5_SCL_M3<br>4'ha: UART1_TX_M1 |
| 7:4 | RW | 0x0 | gpio1b5_sel<br>4'h0: GPIO<br>4'h4: PCIE30X1_0_CLKREQN_M2<br>4'h8: SPI0_CS1_M2<br>4'ha: UART7_TX_M2 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RW | 0x0 | gpio1b4_sel<br>4'h0: GPIO<br>4'h2: PDM1_CLK0_M1<br>4'h4: PCIE30X1_0_PERSTN_M2<br>4'h7: HDMI_DEBUG5<br>4'h8: SPI0_CS0_M2<br>4'ha: UART7_RX_M2 |

**BUS_IOC_GPIO1C_IOMUX_SEL_L**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio1c3_sel<br>4'h0: GPIO<br>4'h1: I2S0_SCLK<br>4'h8: SPI4_CS0_M0<br>4'h9: I2C6_SCL_M1<br>4'ha: UART3_CTSN<br>4'hb: PWM7_IR_M2 |
| 11:8 | RW | 0x0 | gpio1c2_sel<br>4'h0: GPIO<br>4'h1: I2S0_MCLK<br>4'h8: SPI4_CLK_M0<br>4'h9: I2C6_SDA_M1<br>4'ha: UART3_RTSN<br>4'hb: PWM3_IR_M2 |
| 7:4 | RW | 0x0 | gpio1c1_sel<br>4'h0: GPIO<br>4'h8: SPI4_MOSI_M0<br>4'h9: I2C3_SCL_M0<br>4'ha: UART3_TX_M0 |
| 3:0 | RW | 0x0 | gpio1c0_sel<br>4'h0: GPIO<br>4'h8: SPI4_MISO_M0<br>4'h9: I2C3_SDA_M0<br>4'ha: UART3_RX_M0 |

**BUS_IOC_GPIO1C_IOMUX_SEL_H**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio1c7_sel<br>4'h0: GPIO<br>4'h1: I2S0_SDO0<br>4'h9: I2C4_SCL_M4<br>4'ha: UART4_CTSN |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:8 | RW | 0x0 | gpio1c6_sel<br>4'h0: GPIO<br>4'h3: PDM0_CLK0_M0<br>4'h9: I2C4_SDA_M4<br>4'hb: PWM15_IR_M2 |
| 7:4 | RW | 0x0 | gpio1c5_sel<br>4'h0: GPIO<br>4'h1: I2S0_LRCK<br>4'h9: I2C2_SCL_M3<br>4'ha: UART4_RTSN |
| 3:0 | RW | 0x0 | gpio1c4_sel<br>4'h0: GPIO<br>4'h3: PDM0_CLK1_M0<br>4'h4: PCIE30PHY_DTB0<br>4'h8: SPI4_CS1_M0<br>4'h9: I2C2_SDA_M3<br>4'hb: PWM11_IR_M2 |

**BUS_IOC_GPIO1D_IOMUX_SEL_L**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio1d3_sel<br>4'h0: GPIO<br>4'h2: I2S0_SDI1<br>4'h3: PDM0_SDI3_M0<br>4'h8: SPI1_CS0_M2<br>4'h9: I2C1_SDA_M4<br>4'ha: UART4_RX_M0<br>4'hb: PWM1_M1 |
| 11:8 | RW | 0x0 | gpio1d2_sel<br>4'h0: GPIO<br>4'h1: I2S0_SDO3<br>4'h2: I2S0_SDI2<br>4'h3: PDM0_SDI2_M0<br>4'h8: SPI1_CLK_M2<br>4'h9: I2C1_SCL_M4<br>4'ha: UART4_TX_M0<br>4'hb: PWM0_M1 |
| 7:4 | RW | 0x0 | gpio1d1_sel<br>4'h0: GPIO<br>4'h1: I2S0_SDO2<br>4'h2: I2S0_SDI3<br>4'h3: PDM0_SDI1_M0<br>4'h4: PCIE30PHY_DTB1<br>4'h8: SPI1_MOSI_M2<br>4'h9: I2C7_SDA_M0<br>4'ha: UART6_RX_M2 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RW | 0x0 | gpio1d0_sel<br>4'h0: GPIO<br>4'h1: I2S0_SDO1<br>4'h8: SPI1_MISO_M2<br>4'h9: I2C7_SCL_M0<br>4'ha: UART6_TX_M2 |

**BUS_IOC_GPIO1D_IOMUX_SEL_H**

Address: Operational Base + offset (0x003C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio1d7_sel<br>4'h0: GPIO<br>4'h2: MIPI_CAMERA4_CLK_M0<br>4'h4: PCIE30X2_CLKREQN_M3<br>4'h5: HDMI_RX_SDA_M2<br>4'h9: I2C8_SDA_M2<br>4'ha: UART1_CTSN_M1<br>4'hb: PWM15_IR_M3 |
| 11:8 | RW | 0x0 | gpio1d6_sel<br>4'h0: GPIO<br>4'h2: MIPI_CAMERA3_CLK_M0<br>4'h5: HDMI_RX_SCL_M2<br>4'h9: I2C8_SCL_M2<br>4'ha: UART1_RTSN_M1<br>4'hb: PWM14_M2 |
| 7:4 | RW | 0x0 | gpio1d5_sel<br>4'h0: GPIO<br>4'h3: PDM0_SDI0_M0<br>4'h8: SPI1_CS1_M2 |
| 3:0 | RW | 0x0 | gpio1d4_sel<br>4'h0: GPIO<br>4'h2: I2S0_SDI0 |

**BUS_IOC_GPIO2A_IOMUX_SEL_L**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio2a3_sel<br>4'h0: GPIO<br>4'h1: EMMC_RSTN<br>4'h9: I2C2_SCL_M2<br>4'ha: UART5_RTSN_M1 |
| 11:8 | RW | 0x0 | gpio2a2_sel<br>4'h0: GPIO<br>4'h1: EMMC_DATA_STROBE<br>4'h9: I2C2_SDA_M2<br>4'ha: UART5_CTSN_M1 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:4 | RW | 0x0 | gpio2a1_sel<br>4'h0: GPIO<br>4'h1: EMMC_CLKOUT |
| 3:0 | RW | 0x0 | gpio2a0_sel<br>4'h0: GPIO<br>4'h1: EMMC_CMD<br>4'h2: FSPI_CLK_M0 |

**BUS_IOC_GPIO2A_IOMUX_SEL_H**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio2a7_sel<br>4'h0: GPIO<br>4'h1: GMAC0_RXD3<br>4'h2: SDIO_D1_M0<br>4'h3: FSPI_D1_M1<br>4'ha: UART6_TX_M0 |
| 11:8 | RW | 0x0 | gpio2a6_sel<br>4'h0: GPIO<br>4'h1: GMAC0_RXD2<br>4'h2: SDIO_D0_M0<br>4'h3: FSPI_D0_M1<br>4'ha: UART6_RX_M0 |
| 7:0 | RO | 0x00 | reserved |

**BUS_IOC_GPIO2B_IOMUX_SEL_L**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio2b3_sel<br>4'h0: GPIO<br>4'h1: GMAC0_TXCLK<br>4'h2: SDIO_CLK_M0<br>4'h3: FSPI_CLK_M1<br>4'h9: I2C3_SDA_M3 |
| 11:8 | RW | 0x0 | gpio2b2_sel<br>4'h0: GPIO<br>4'h1: GMAC0_TXD3<br>4'h2: SDIO_CMD_M0<br>4'h9: I2C3_SCL_M3 |
| 7:4 | RW | 0x0 | gpio2b1_sel<br>4'h0: GPIO<br>4'h1: GMAC0_TXD2<br>4'h2: SDIO_D3_M0<br>4'h3: FSPI_D3_M1<br>4'h9: I2C8_SDA_M1<br>4'ha: UART6_CTSN_M0 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RW | 0x0 | gpio2b0_sel<br>4'h0: GPIO<br>4'h1: GMAC0_RXCLK<br>4'h2: SDIO_D2_M0<br>4'h3: FSPI_D2_M1<br>4'h9: I2C8_SCL_M1<br>4'ha: UART6_RTSN_M0 |

**BUS_IOC_GPIO2B_IOMUX_SEL_H**

Address: Operational Base + offset (0x004C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio2b7_sel<br>4'h0: GPIO<br>4'h1: GMAC0_TXD1<br>4'h2: I2S2_SCLK_M0<br>4'h9: I2C5_SDA_M4<br>4'ha: UART1_TX_M0 |
| 11:8 | RW | 0x0 | gpio2b6_sel<br>4'h0: GPIO<br>4'h1: GMAC0_TXD0<br>4'h2: I2S2_MCLK_M0<br>4'h9: I2C5_SCL_M4<br>4'ha: UART1_RX_M0 |
| 7:4 | RW | 0x0 | gpio2b5_sel<br>4'h0: GPIO<br>4'h1: GMAC0_PPSTRING<br>4'h3: FSPI_CS1N_M1<br>4'h4: HDMI_TX1_SCL_M0<br>4'h9: I2C4_SCL_M1<br>4'ha: UART7_TX_M0 |
| 3:0 | RW | 0x0 | gpio2b4_sel<br>4'h0: GPIO<br>4'h1: GMAC0_PTP_REFCLK<br>4'h3: FSPI_CS0N_M1<br>4'h4: HDMI_TX1_SDA_M0<br>4'h9: I2C4_SDA_M1<br>4'ha: UART7_RX_M0 |

**BUS_IOC_GPIO2C_IOMUX_SEL_L**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio2c3_sel<br>4'h0: GPIO<br>4'h1: ETH0_REFCLKO_25M<br>4'h2: I2S2_SDI_M0<br>4'h8: SPI1_CS0_M0<br>4'h9: I2C6_SCL_M2 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:8 | RW | 0x0 | gpio2c2_sel<br>4'h0: GPIO<br>4'h1: GMAC0_RXD1<br>4'h8: SPI1_MOSI_M0<br>4'h9: I2C6_SDA_M2<br>4'ha: UART9_TX_M0 |
| 7:4 | RW | 0x0 | gpio2c1_sel<br>4'h0: GPIO<br>4'h1: GMAC0_RXD0<br>4'h8: SPI1_MISO_M0<br>4'h9: I2C2_SCL_M1<br>4'ha: UART1_CTSN_M0 |
| 3:0 | RW | 0x0 | gpio2c0_sel<br>4'h0: GPIO<br>4'h1: GMAC0_TXEN<br>4'h2: I2S2_LRCK_M0<br>4'h8: SPI1_CLK_M0<br>4'h9: I2C2_SDA_M1<br>4'ha: UART1_RTSN_M0 |

**BUS_IOC_GPIO2C_IOMUX_SEL_H**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7:4 | RW | 0x0 | gpio2c5_sel<br>4'h0: GPIO<br>4'h1: CLK32K_OUT1 |
| 3:0 | RW | 0x0 | gpio2c4_sel<br>4'h0: GPIO<br>4'h1: GMAC0_PPSCLK<br>4'h3: TEST_CLKOUT_M1<br>4'h4: HDMI_TX1_CEC_M0<br>4'h8: SPI1_CS1_M0<br>4'ha: UART9_RX_M0 |

**BUS_IOC_GPIO2D_IOMUX_SEL_L**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio2d3_sel<br>4'h0: GPIO<br>4'h1: EMMC_D3<br>4'h2: FSPI_D3_M0 |
| 11:8 | RW | 0x0 | gpio2d2_sel<br>4'h0: GPIO<br>4'h1: EMMC_D2<br>4'h2: FSPI_D2_M0 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:4 | RW | 0x0 | gpio2d1_sel<br>4'h0: GPIO<br>4'h1: EMMC_D1<br>4'h2: FSPI_D1_M0 |
| 3:0 | RW | 0x0 | gpio2d0_sel<br>4'h0: GPIO<br>4'h1: EMMC_D0<br>4'h2: FSPI_D0_M0 |

**BUS_IOC_GPIO2D_IOMUX_SEL_H**

Address: Operational Base + offset (0x005C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio2d7_sel<br>4'h0: GPIO<br>4'h1: EMMC_D7<br>4'h2: FSPI_CS1N_M0 |
| 11:8 | RW | 0x0 | gpio2d6_sel<br>4'h0: GPIO<br>4'h1: EMMC_D6<br>4'h2: FSPI_CS0N_M0 |
| 7:4 | RW | 0x0 | gpio2d5_sel<br>4'h0: GPIO<br>4'h1: EMMC_D5<br>4'h9: I2C1_SDA_M3<br>4'ha: UART5_TX_M2 |
| 3:0 | RW | 0x0 | gpio2d4_sel<br>4'h0: GPIO<br>4'h1: EMMC_D4<br>4'h9: I2C1_SCL_M3<br>4'ha: UART5_RX_M2 |

**BUS_IOC_GPIO3A_IOMUX_SEL_L**

Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio3a3_sel<br>4'h0: GPIO<br>4'h1: GMAC1_RXD3<br>4'h2: SDIO_D3_M1<br>4'h3: I2S3_SDO<br>4'h4: AUDDSM_RN<br>4'h5: FSPI_D3_M2<br>4'h8: SPI4_CS0_M1<br>4'ha: UART8_RX_M1 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:8 | RW | 0x0 | gpio3a2_sel<br>4'h0: GPIO<br>4'h1: GMAC1_RXD2<br>4'h2: SDIO_D2_M1<br>4'h3: I2S3_LRCK<br>4'h4: AUDDSM_LP<br>4'h5: FSPI_D2_M2<br>4'h8: SPI4_CLK_M1<br>4'ha: UART8_TX_M1 |
| 7:4 | RW | 0x0 | gpio3a1_sel<br>4'h0: GPIO<br>4'h1: GMAC1_TXD3<br>4'h2: SDIO_D1_M1<br>4'h3: I2S3_SCLK<br>4'h4: AUDDSM_LN<br>4'h5: FSPI_D1_M2<br>4'h8: SPI4_MOSI_M1<br>4'h9: I2C6_SCL_M4<br>4'hb: PWM11_IR_M0 |
| 3:0 | RW | 0x0 | gpio3a0_sel<br>4'h0: GPIO<br>4'h1: GMAC1_TXD2<br>4'h2: SDIO_D0_M1<br>4'h3: I2S3_MCLK<br>4'h5: FSPI_D0_M2<br>4'h8: SPI4_MISO_M1<br>4'h9: I2C6_SDA_M4<br>4'hb: PWM10_M0 |

**BUS_IOC_GPIO3A_IOMUX_SEL_H**

Address: Operational Base + offset (0x0064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio3a7_sel<br>4'h0: GPIO<br>4'h1: GMAC1_RXD0<br>4'h4: MIPI_CAMERA2_CLK_M1<br>4'hb: PWM8_M0 |
| 11:8 | RW | 0x0 | gpio3a6_sel<br>4'h0: GPIO<br>4'h1: ETH1_REFCLKO_25M<br>4'h4: MIPI_CAMERA1_CLK_M1<br>4'h9: I2C4_SCL_M0 |
| 7:4 | RW | 0x0 | gpio3a5_sel<br>4'h0: GPIO<br>4'h1: GMAC1_RXCLK<br>4'h2: SDIO_CLK_M1<br>4'h4: MIPI_CAMERA0_CLK_M1<br>4'h5: FSPI_CLK_M2<br>4'h9: I2C4_SDA_M0<br>4'ha: UART8_CTSN_M1 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RW | 0x0 | gpio3a4_sel<br>4'h0: GPIO<br>4'h1: GMAC1_TXCLK<br>4'h2: SDIO_CMD_M1<br>4'h3: I2S3_SDI<br>4'h4: AUDDSM_RP<br>4'h8: SPI4_CS1_M1<br>4'ha: UART8_RTSN_M1 |

**BUS_IOC_GPIO3B_IOMUX_SEL_L**

Address: Operational Base + offset (0x0068)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio3b3_sel<br>4'h0: GPIO<br>4'h1: GMAC1_TXD0<br>4'h3: I2S2_SDO_M1<br>4'ha: UART2_RTSN |
| 11:8 | RW | 0x0 | gpio3b2_sel<br>4'h0: GPIO<br>4'h1: GMAC1_TXER<br>4'h3: I2S2_SDI_M1<br>4'ha: UART2_RX_M2<br>4'hb: PWM3_IR_M1 |
| 7:4 | RW | 0x0 | gpio3b1_sel<br>4'h0: GPIO<br>4'h1: GMAC1_RXDV_CRS<br>4'h4: MIPI_CAMERA4_CLK_M1<br>4'ha: UART2_TX_M2<br>4'hb: PWM2_M1 |
| 3:0 | RW | 0x0 | gpio3b0_sel<br>4'h0: GPIO<br>4'h1: GMAC1_RXD1<br>4'h4: MIPI_CAMERA3_CLK_M1<br>4'hb: PWM9_M0 |

**BUS_IOC_GPIO3B_IOMUX_SEL_H**

Address: Operational Base + offset (0x006C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio3b7_sel<br>4'h0: GPIO<br>4'h1: GMAC1_PTP_REF_CLK<br>4'h5: HDMI_TX1_HPD_M1<br>4'h8: SPI1_MOSI_M1<br>4'h9: I2C3_SCL_M1 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:8 | RW | 0x0 | gpio3b6_sel<br>4'h0: GPIO<br>4'h1: GMAC1_MCLKINOUT<br>4'h3: I2S2_LRCK_M1<br>4'h9: CAN1_TX_M0<br>4'ha: UART3_RX_M1<br>4'hb: PWM13_M0 |
| 7:4 | RW | 0x0 | gpio3b5_sel<br>4'h0: GPIO<br>4'h1: GMAC1_TXEN<br>4'h3: I2S2_SCLK_M1<br>4'h9: CAN1_RX_M0<br>4'ha: UART3_TX_M1<br>4'hb: PWM12_M0 |
| 3:0 | RW | 0x0 | gpio3b4_sel<br>4'h0: GPIO<br>4'h1: GMAC1_TXD1<br>4'h3: I2S2_MCLK_M1<br>4'ha: UART2_CTSN |

**BUS_IOC_GPIO3C_IOMUX_SEL_L**

Address: Operational Base + offset (0x0070)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio3c3_sel<br>4'h0: GPIO<br>4'h1: GMAC1_MDIO<br>4'h2: MIPI_TE1<br>4'h8: SPI1_CS1_M1<br>4'h9: I2C8_SDA_M4<br>4'ha: UART7_CTSN_M1<br>4'hb: PWM15_IR_M0 |
| 11:8 | RW | 0x0 | gpio3c2_sel<br>4'h0: GPIO<br>4'h1: GMAC1_MDC<br>4'h2: MIPI_TE0<br>4'h8: SPI1_CS0_M1<br>4'h9: I2C8_SCL_M4<br>4'ha: UART7_RTSN_M1<br>4'hb: PWM14_M0 |
| 7:4 | RW | 0x0 | gpio3c1_sel<br>4'h0: GPIO<br>4'h1: GMAC1_PPSCLK<br>4'h4: PCIE30X2_BUTTON_RSTN<br>4'h8: SPI1_CLK_M1<br>4'ha: UART7_RX_M1 |
| 3:0 | RW | 0x0 | gpio3c0_sel<br>4'h0: GPIO<br>4'h1: GMAC1_PPSTRIG<br>4'h8: SPI1_MISO_M1<br>4'h9: I2C3_SDA_M1<br>4'ha: UART7_TX_M1 |

Rockchip Confidencial

**BUS_IOC_GPIO3C_IOMUX_SEL_H**

Address: Operational Base + offset (0x0074)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio3c7_sel<br>4'h0: GPIO<br>4'h1: CIF_D11<br>4'h4: PCIE20X1_2_CLKREQN_M0<br>4'h5: HDMI_TX0_SCL_M2<br>4'h8: SPI3_MOSI_M3<br>4'h9: I2C5_SCL_M0 |
| 11:8 | RW | 0x0 | gpio3c6_sel<br>4'h0: GPIO<br>4'h1: CIF_D10<br>4'h4: PCIE30X4_PERSTN_M2<br>4'h5: HDMI_TX1_SCL_M1<br>4'h8: SPI3_MISO_M3 |
| 7:4 | RW | 0x0 | gpio3c5_sel<br>4'h0: GPIO<br>4'h1: CIF_D9<br>4'h2: FSPI_CS1N_M2<br>4'h4: PCIE30X4_WAKEN_M2<br>4'h5: HDMI_TX1_SDA_M1<br>4'h8: SPI3_CS1_M3<br>4'h9: CAN2_TX_M0<br>4'ha: UART5_RX_M1 |
| 3:0 | RW | 0x0 | gpio3c4_sel<br>4'h0: GPIO<br>4'h1: CIF_D8<br>4'h2: FSPI_CS0N_M2<br>4'h4: PCIE30X4_CLKREQN_M2<br>4'h5: HDMI_TX1_CEC_M2<br>4'h8: SPI3_CS0_M3<br>4'h9: CAN2_RX_M0<br>4'ha: UART5_TX_M1 |

**BUS_IOC_GPIO3D_IOMUX_SEL_L**

Address: Operational Base + offset (0x0078)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio3d3_sel<br>4'h0: GPIO<br>4'h1: CIF_D15<br>4'h4: PCIE30X2_WAKEN_M2<br>4'h5: HDMI_RX_SDA_M1<br>4'h8: SPI0_CLK_M3<br>4'h9: I2C7_SDA_M2<br>4'ha: UART9_CTSN_M2<br>4'hb: PWM10_M2 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:8 | RW | 0x0 | gpio3d2_sel<br>4'h0: GPIO<br>4'h1: CIF_D14<br>4'h4: PCIE30X2_CLKREQN_M2<br>4'h5: HDMI_RX_SCL_M1<br>4'h8: SPI0_MOSI_M3<br>4'h9: I2C7_SCL_M2<br>4'ha: UART9_RTSN_M2 |
| 7:4 | RW | 0x0 | gpio3d1_sel<br>4'h0: GPIO<br>4'h1: CIF_D13<br>4'h4: PCIE20X1_2_PERSTN_M0<br>4'h5: HDMI_RX_CEC_M1<br>4'h8: SPI0_MISO_M3<br>4'ha: UART4_TX_M1<br>4'hb: PWM9_M2 |
| 3:0 | RW | 0x0 | gpio3d0_sel<br>4'h0: GPIO<br>4'h1: CIF_D12<br>4'h4: PCIE20X1_2_WAKEN_M0<br>4'h5: HDMI_TX0_SDA_M2<br>4'h8: SPI3_CLK_M3<br>4'h9: I2C5_SDA_M0<br>4'ha: UART4_RX_M1<br>4'hb: PWM8_M2 |

**BUS_IOC_GPIO3D_IOMUX_SEL_H**

Address: Operational Base + offset (0x007C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7:4 | RW | 0x0 | gpio3d5_sel<br>4'h0: GPIO<br>4'h4: PCIE30X4_BUTTON_RSTN<br>4'h5: DP1_HPDIN_M0<br>4'h6: MCU_JTAG_TMS_M1<br>4'h8: SPI0_CS1_M3<br>4'ha: UART9_TX_M2<br>4'hb: PWM11_IR_M3 |
| 3:0 | RW | 0x0 | gpio3d4_sel<br>4'h0: GPIO<br>4'h3: HDMI_TX0_HPD_M1<br>4'h4: PCIE30X2_PERSTN_M2<br>4'h5: HDMI_RX_HPDOUT_M1<br>4'h6: MCU_JTAG_TCK_M1<br>4'h8: SPI0_CS0_M3<br>4'ha: UART9_RX_M2 |

**BUS_IOC_GPIO4A_IOMUX_SEL_L**

Address: Operational Base + offset (0x0080)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio4a3_sel<br>4'h0: GPIO<br>4'h1: CIF_D3<br>4'h2: BT1120_D3<br>4'h4: PCIE30X1_0_CLKREQN_M1<br>4'h7: DDRPHYCH0_DTB3<br>4'ha: UART0_TX_M2 |
| 11:8 | RW | 0x0 | gpio4a2_sel<br>4'h0: GPIO<br>4'h1: CIF_D2<br>4'h2: BT1120_D2<br>4'h3: I2S1_LRCK_M0<br>4'h4: PCIE30X1_1_PERSTN_M1<br>4'h7: DDRPHYCH0_DTB2<br>4'h8: SPI0_CLK_M1 |
| 7:4 | RW | 0x0 | gpio4a1_sel<br>4'h0: GPIO<br>4'h1: CIF_D1<br>4'h2: BT1120_D1<br>4'h3: I2S1_SCLK_M0<br>4'h4: PCIE30X1_1_WAKEN_M1<br>4'h7: DDRPHYCH0_DTB1<br>4'h8: SPI0_MOSI_M1<br>4'ha: UART9_CTSN_M1 |
| 3:0 | RW | 0x0 | gpio4a0_sel<br>4'h0: GPIO<br>4'h1: CIF_D0<br>4'h2: BT1120_D0<br>4'h3: I2S1_MCLK_M0<br>4'h4: PCIE30X1_1_CLKREQN_M1<br>4'h7: DDRPHYCH0_DTB0<br>4'h8: SPI0_MISO_M1<br>4'ha: UART9_RTSN_M1 |

**BUS_IOC_GPIO4A_IOMUX_SEL_H**

Address: Operational Base + offset (0x0084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio4a7_sel<br>4'h0: GPIO<br>4'h1: CIF_D7<br>4'h2: BT1120_D7<br>4'h3: I2S1_SDI2_M0<br>4'h4: PCIE30X2_WAKEN_M1<br>4'h7: DDRPHYCH1_DTB3<br>4'h8: SPI2_CS0_M1<br>4'h9: I2C5_SDA_M2 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:8 | RW | 0x0 | gpio4a6_sel<br>4'h0: GPIO<br>4'h1: CIF_D6<br>4'h2: BT1120_D6<br>4'h3: I2S1_SDI1_M0<br>4'h4: PCIE30X2_CLKREQN_M1<br>4'h7: DDRPHYCH1_DTB2<br>4'h8: SPI2_CLK_M1<br>4'h9: I2C5_SCL_M2<br>4'ha: UART3_RX_M2 |
| 7:4 | RW | 0x0 | gpio4a5_sel<br>4'h0: GPIO<br>4'h1: CIF_D5<br>4'h2: BT1120_D5<br>4'h3: I2S1_SDI0_M0<br>4'h4: PCIE30X1_0_PERSTN_M1<br>4'h7: DDRPHYCH1_DTB1<br>4'h8: SPI2_MOSI_M1<br>4'h9: I2C3_SDA_M2<br>4'ha: UART3_TX_M2 |
| 3:0 | RW | 0x0 | gpio4a4_sel<br>4'h0: GPIO<br>4'h1: CIF_D4<br>4'h2: BT1120_D4<br>4'h4: PCIE30X1_0_WAKEN_M1<br>4'h7: DDRPHYCH1_DTB0<br>4'h8: SPI2_MISO_M1<br>4'h9: I2C3_SCL_M2<br>4'ha: UART0_RX_M2 |

**BUS_IOC_GPIO4B_IOMUX_SEL_L**

Address: Operational Base + offset (0x0088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio4b3_sel<br>4'h0: GPIO<br>4'h1: CIF_VSYNC<br>4'h2: BT1120_D9<br>4'h3: I2S1_SDO2_M0<br>4'h4: PCIE20X1_2_BUTTON_RSTN<br>4'h7: DDRPHYCH2_DTB3<br>4'h9: I2C7_SDA_M3<br>4'ha: UART8_CTSN_M0<br>4'hb: PWM15_IR_M1<br>4'hc: CAN1_TX_M1 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:8 | RW | 0x0 | gpio4b2_sel<br>4'h0: GPIO<br>4'h1: CIF_HREF<br>4'h2: BT1120_D8<br>4'h3: I2S1_SDO1_M0<br>4'h4: PCIE30X1_1_BUTTON_RSTN<br>4'h7: DDRPHYCH2_DTB2<br>4'h8: SPI0_CS0_M1<br>4'h9: I2C7_SCL_M3<br>4'ha: UART8_RTSN_M0<br>4'hb: PWM14_M1<br>4'hc: CAN1_RX_M1 |
| 7:4 | RW | 0x0 | gpio4b1_sel<br>4'h0: GPIO<br>4'h1: MIPI_CAMERA0_CLK_M0<br>4'h2: SPDIF1_TX_M1<br>4'h3: I2S1_SDO0_M0<br>4'h4: PCIE30X1_0_BUTTON_RSTN<br>4'h6: SATA2_ACT_LED_M0<br>4'h7: DDRPHYCH2_DTB1<br>4'h8: SPI0_CS1_M1<br>4'h9: I2C6_SCL_M3<br>4'ha: UART8_RX_M0 |
| 3:0 | RW | 0x0 | gpio4b0_sel<br>4'h0: GPIO<br>4'h1: CIF_CLKIN<br>4'h2: BT1120_CLKOUT<br>4'h3: I2S1_SDI3_M0<br>4'h4: PCIE30X2_PERSTN_M1<br>4'h7: DDRPHYCH2_DTB0<br>4'h8: SPI2_CS1_M1<br>4'h9: I2C6_SDA_M3<br>4'ha: UART8_TX_M0 |

**BUS_IOC_GPIO4B_IOMUX_SEL_H**

Address: Operational Base + offset (0x008C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio4b7_sel<br>4'h0: GPIO<br>4'h2: BT1120_D13<br>4'h4: PCIE20X1_2_CLKREQN_M1<br>4'h5: HDMI_TX0_SCL_M0<br>4'h7: DDRPHYCH3_DTB3<br>4'h8: SPI3_CLK_M1<br>4'h9: I2C5_SDA_M1 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:8 | RW | 0x0 | gpio4b6_sel<br>4'h0: GPIO<br>4'h2: BT1120_D12<br>4'h4: PCIE30X4_PERSTN_M1<br>4'h5: HDMI_RX_HPDOUT_M0<br>4'h6: SATA0_ACT_LED_M0<br>4'h7: DDRPHYCH3_DTB2<br>4'h8: SPI3_MOSI_M1<br>4'h9: I2C5_SCL_M1<br>4'hb: PWM13_M1 |
| 7:4 | RW | 0x0 | gpio4b5_sel<br>4'h0: GPIO<br>4'h2: BT1120_D11<br>4'h4: PCIE30X4_WAKEN_M1<br>4'h5: HDMI_RX_CEC_M0<br>4'h6: SATA1_ACT_LED_M0<br>4'h7: DDRPHYCH3_DTB1<br>4'h8: SPI3_MISO_M1<br>4'ha: UART9_RX_M1<br>4'hb: PWM12_M1 |
| 3:0 | RW | 0x0 | gpio4b4_sel<br>4'h0: GPIO<br>4'h1: CIF_CLKOUT<br>4'h2: BT1120_D10<br>4'h3: I2S1_SDO3_M0<br>4'h4: PCIE30X4_CLKREQN_M1<br>4'h5: DP0_HPDIN_M0<br>4'h6: SPDIF0_TX_M1<br>4'h7: DDRPHYCH3_DTB0<br>4'ha: UART9_TX_M1<br>4'hb: PWM11_IR_M1 |

**BUS_IOC_GPIO4C_IOMUX_SEL_L**

Address: Operational Base + offset (0x0090)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | gpio4c3_sel<br>4'h0: GPIO<br>4'h1: GMAC0_MCLKINOUT<br>4'h2: I2S2_SDO_M0<br>4'h8: SPI3_CS1_M0<br>4'h9: I2C7_SCL_M1<br>4'hb: PWM4_M1 |
| 11:8 | RW | 0x0 | gpio4c2_sel<br>4'h0: GPIO<br>4'h1: GMAC0_RXDV_CRS<br>4'h8: SPI3_CS0_M0<br>4'ha: UART7_RTSN_M0<br>4'hb: PWM2_M2 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:4 | RW | 0x0 | gpio4c1_sel<br>4'h0: GPIO<br>4'h2: BT1120_D15<br>4'h3: SPDIF1_TX_M2<br>4'h4: PCIE20X1_2_PERSTN_M1<br>4'h5: HDMI_TX0_CEC_M0<br>4'h8: SPI3_CS1_M1<br>4'h9: I2C8_SDA_M3<br>4'hb: PWM6_M1 |
| 3:0 | RW | 0x0 | gpio4c0_sel<br>4'h0: GPIO<br>4'h2: BT1120_D14<br>4'h4: PCIE20X1_2_WAKEN_M1<br>4'h5: HDMI_TX0_SDA_M0<br>4'h8: SPI3_CS0_M1<br>4'h9: I2C8_SCL_M3 |

**BUS_IOC_GPIO4C_IOMUX_SEL_H**

Address: Operational Base + offset (0x0094)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11:8 | RW | 0x0 | gpio4c6_sel<br>4'h0: GPIO<br>4'h1: GMAC0_TXER<br>4'h8: SPI3_CLK_M0<br>4'h9: I2C0_SDA_M1<br>4'ha: UART7_CTSN_M0<br>4'hb: PWM7_IR_M3 |
| 7:4 | RW | 0x0 | gpio4c5_sel<br>4'h0: GPIO<br>4'h1: GMAC0_MDIO<br>4'h8: SPI3_MOSI_M0<br>4'h9: I2C0_SCL_M1<br>4'ha: UART9_CTSN_M0<br>4'hb: PWM6_M2 |
| 3:0 | RW | 0x0 | gpio4c4_sel<br>4'h0: GPIO<br>4'h1: GMAC0_MDC<br>4'h8: SPI3_MISO_M0<br>4'h9: I2C7_SDA_M1<br>4'ha: UART9_RTSN_M0<br>4'hb: PWM5_M2 |

**BUS_IOC_GPIO4D_IOMUX_SEL_L**

Address: Operational Base + offset (0x0098)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:12 | RW | 0x5 | gpio4d3_sel<br>4'h0: GPIO<br>4'h1: SDMMC_D3<br>4'h2: PDM1_SDI0_M0<br>4'h5: JTAG_TMS_M0<br>4'h9: I2C8_SDA_M0<br>4'ha: UART5_RTSN_M0<br>4'hb: PWM10_M1 |
| 11:8 | RW | 0x5 | gpio4d2_sel<br>4'h0: GPIO<br>4'h1: SDMMC_D2<br>4'h2: PDM1_SDI1_M0<br>4'h5: JTAG_TCK_M0<br>4'h9: I2C8_SCL_M0<br>4'ha: UART5_CTSN_M0 |
| 7:4 | RW | 0x0 | gpio4d1_sel<br>4'h0: GPIO<br>4'h1: SDMMC_D1<br>4'h2: PDM1_SDI2_M0<br>4'h5: JTAG_TMS_M1<br>4'h9: I2C3_SDA_M4<br>4'ha: UART2_RX_M1<br>4'hb: PWM9_M1 |
| 3:0 | RW | 0x0 | gpio4d0_sel<br>4'h0: GPIO<br>4'h1: SDMMC_D0<br>4'h2: PDM1_SDI3_M0<br>4'h5: JTAG_TCK_M1<br>4'h9: I2C3_SCL_M4<br>4'ha: UART2_TX_M1<br>4'hb: PWM8_M1 |

**BUS_IOC_GPIO4D_IOMUX_SEL_H**

Address: Operational Base + offset (0x009C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7:4 | RW | 0x0 | gpio4d5_sel<br>4'h0: GPIO<br>4'h1: SDMMC_CLK<br>4'h2: PDM1_CLK0_M0<br>4'h4: TEST_CLKOUT_M0<br>4'h5: MCU_JTAG_TMS_M0<br>4'h9: CAN0_RX_M1<br>4'ha: UART5_TX_M0 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RW | 0x0 | gpio4d4_sel<br>4'h0: GPIO<br>4'h1: SDMMC_CMD<br>4'h2: PDM1_CLK1_M0<br>4'h5: MCU_JTAG_TCK_M0<br>4'h9: CAN0_TX_M1<br>4'ha: UART5_RX_M0<br>4'hb: PWM7_IR_M1 |

# 6.28 VCCIO1_4_IOC Register Description

## 6.28.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VCCIO1_4_IOC_GPIO1A_DS_L | 0x0020 | W | 0x00006666 | GPIO1A Driver Strength Control Low bits |
| VCCIO1_4_IOC_GPIO1A_DS_H | 0x0024 | W | 0x00006666 | GPIO1A Driver Strength Control High bits |
| VCCIO1_4_IOC_GPIO1B_DS_L | 0x0028 | W | 0x00006666 | GPIO1B Driver Strength Control Low bits |
| VCCIO1_4_IOC_GPIO1B_DS_H | 0x002C | W | 0x00006666 | GPIO1B Driver Strength Control High bits |
| VCCIO1_4_IOC_GPIO1C_DS_L | 0x0030 | W | 0x00001111 | GPIO1C Driver Strength Control Low bits |
| VCCIO1_4_IOC_GPIO1C_DS_H | 0x0034 | W | 0x00001111 | GPIO1C Driver Strength Control High bits |
| VCCIO1_4_IOC_GPIO1D_DS_L | 0x0038 | W | 0x00001111 | GPIO1D Driver Strength Control Low bits |
| VCCIO1_4_IOC_GPIO1D_DS_H | 0x003C | W | 0x00006611 | GPIO1D Driver Strength Control High bits |
| VCCIO1_4_IOC_GPIO1A_P | 0x0110 | W | 0x0000D555 | GPIO1A Pull-up/down Control |
| VCCIO1_4_IOC_GPIO1B_P | 0x0114 | W | 0x0000FF57 | GPIO1B Pull-up/down Control |
| VCCIO1_4_IOC_GPIO1C_P | 0x0118 | W | 0x00005550 | GPIO1C Pull-up/down Control |
| VCCIO1_4_IOC_GPIO1D_P | 0x011C | W | 0x0000F555 | GPIO1D Pull-up/down Control |
| VCCIO1_4_IOC_GPIO1A_IE | 0x0180 | W | 0x000000FF | GPIO1A Input Enable Control |
| VCCIO1_4_IOC_GPIO1B_IE | 0x0184 | W | 0x000000FF | GPIO1B Input Enable Control |
| VCCIO1_4_IOC_GPIO1C_IE | 0x0188 | W | 0x000000FF | GPIO1C Input Enable Control |
| VCCIO1_4_IOC_GPIO1D_IE | 0x018C | W | 0x000000FF | GPIO1D Input Enable Control |
| VCCIO1_4_IOC_GPIO1A_SMT | 0x0210 | W | 0x00000000 | GPIO1A Schmitt Trigger Control |
| VCCIO1_4_IOC_GPIO1B_SMT | 0x0214 | W | 0x00000000 | GPIO1B Schmitt Trigger Control |
| VCCIO1_4_IOC_GPIO1C_SMT | 0x0218 | W | 0x00000000 | GPIO1C Schmitt Trigger Control |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VCCIO1_4_IOC_GPIO1D_SMT | 0x021C | W | 0x00000000 | GPIO1D Schmitt Trigger Control |
| VCCIO1_4_IOC_GPIO_PDIS | 0x0280 | W | 0x00000000 | Auto Pull-up/down disable Control |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.28.2 Detail Registers Description

### VCCIO1_4_IOC_GPIO1A_DS_L

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x6 | gpio1a3_ds<br>GPIO1A3 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x6 | gpio1a2_ds<br>GPIO1A2 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x6 | gpio1a1_ds<br>GPIO1A1 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio1a0_ds<br>GPIO1A0 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

Rockchip Confidencial

**VCCIO1_4_IOC_GPIO1A_DS_H**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x6 | gpio1a7_ds<br>GPIO1A7 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x6 | gpio1a6_ds<br>GPIO1A6 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x6 | gpio1a5_ds<br>GPIO1A5 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio1a4_ds<br>GPIO1A4 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**VCCIO1_4_IOC_GPIO1B_DS_L**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x6 | gpio1b3_ds<br>GPIO1B3 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x6 | gpio1b2_ds<br>GPIO1B2 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x6 | gpio1b1_ds<br>GPIO1B1 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio1b0_ds<br>GPIO1B0 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**VCCIO1_4_IOC_GPIO1B_DS_H**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14:12 | RW | 0x6 | gpio1b7_ds<br>GPIO1D7 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x6 | gpio1b6_ds<br>GPIO1D6 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x6 | gpio1b5_ds<br>GPIO1D5 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio1b4_ds<br>GPIO1D4 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**VCCIO1_4_IOC_GPIO1C_DS_L**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13:12 | RW | 0x1 | gpio1c3_ds<br>GPIO1C3 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:10 | RO | 0x0 | reserved |
| 9:8 | RW | 0x1 | gpio1c2_ds<br>GPIO1C2 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 7:6 | RO | 0x0 | reserved |
| 5:4 | RW | 0x1 | gpio1c1_ds<br>GPIO1C1 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 3:2 | RO | 0x0 | reserved |
| 1:0 | RW | 0x1 | gpio1c0_ds<br>GPIO1C0 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |

**VCCIO1_4_IOC_GPIO1C_DS_H**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13:12 | RW | 0x1 | gpio1c7_ds<br>GPIO1C7 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 11:10 | RO | 0x0 | reserved |
| 9:8 | RW | 0x1 | gpio1c6_ds<br>GPIO1C6 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 7:6 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5:4 | RW | 0x1 | gpio1c5_ds<br>GPIO1C5 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 3:2 | RO | 0x0 | reserved |
| 1:0 | RW | 0x1 | gpio1c4_ds<br>GPIO1C4 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |

**VCCIO1_4_IOC_GPIO1D_DS_L**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13:12 | RW | 0x1 | gpio1d3_ds<br>GPIO1D3 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 11:10 | RO | 0x0 | reserved |
| 9:8 | RW | 0x1 | gpio1d2_ds<br>GPIO1D2 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 7:6 | RO | 0x0 | reserved |
| 5:4 | RW | 0x1 | gpio1d1_ds<br>GPIO1D1 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 3:2 | RO | 0x0 | reserved |
| 1:0 | RW | 0x1 | gpio1d0_ds<br>GPIO1D0 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |

Rockchip Confidencial

**VCCIO1_4_IOC_GPIO1D_DS_H**

Address: Operational Base + offset (0x003C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x6 | gpio1d7_ds<br>GPIO1D7 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x6 | gpio1d6_ds<br>GPIO1D6 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7:6 | RO | 0x0 | reserved |
| 5:4 | RW | 0x1 | gpio1d5_ds<br>GPIO1D5 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 3:2 | RO | 0x0 | reserved |
| 1:0 | RW | 0x1 | gpio1d4_ds<br>GPIO1D4 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |

**VCCIO1_4_IOC_GPIO1A_P**

Address: Operational Base + offset (0x0110)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x1 | gpio1a7_ps<br>GPIO1A7 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 14 | RW | 0x1 | gpio1a7_pe<br>GPIO1A7 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 13 | RW | 0x0 | gpio1a6_ps<br>GPIO1A6 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 12 | RW | 0x1 | gpio1a6_pe<br>GPIO1A6 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 11 | RW | 0x0 | gpio1a5_ps<br>GPIO1A5 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 10 | RW | 0x1 | gpio1a5_pe<br>GPIO1A5 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 9 | RW | 0x0 | gpio1a4_ps<br>GPIO1A4 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 8 | RW | 0x1 | gpio1a4_pe<br>GPIO1A4 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 7 | RW | 0x0 | gpio1a3_ps<br>GPIO1A3 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 6 | RW | 0x1 | gpio1a3_pe<br>GPIO1A3 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 5 | RW | 0x0 | gpio1a2_ps<br>GPIO1A2 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x1 | gpio1a2_pe<br>GPIO1A2 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 3 | RW | 0x0 | gpio1a1_ps<br>GPIO1A1 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 2 | RW | 0x1 | gpio1a1_pe<br>GPIO1A1 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 1 | RW | 0x0 | gpio1a0_ps<br>GPIO1A0 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 0 | RW | 0x1 | gpio1a0_pe<br>GPIO1A0 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

**VCCIO1_4_IOC_GPIO1B_P**

Address: Operational Base + offset (0x0114)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | gpio1b7_ps<br>GPIO1B7 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 14 | RW | 0x1 | gpio1b7_pe<br>GPIO1B7 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 13 | RW | 0x1 | gpio1b6_ps<br>GPIO1B6 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 12 | RW | 0x1 | gpio1b6_pe<br>GPIO1B6 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11 | RW | 0x1 | gpio1b5_ps<br>GPIO1B5 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 10 | RW | 0x1 | gpio1b5_pe<br>GPIO1B5 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 9 | RW | 0x1 | gpio1b4_ps<br>GPIO1B4 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 8 | RW | 0x1 | gpio1b4_pe<br>GPIO1B4 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 7 | RW | 0x0 | gpio1b3_ps<br>GPIO1B3 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 6 | RW | 0x1 | gpio1b3_pe<br>GPIO1B3 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 5 | RW | 0x0 | gpio1b2_ps<br>GPIO1B2 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 4 | RW | 0x1 | gpio1b2_pe<br>GPIO1B2 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 3 | RW | 0x0 | gpio1b1_ps<br>GPIO1B1 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 2 | RW | 0x1 | gpio1b1_pe<br>GPIO1B1 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 1 | RW | 0x1 | gpio1b0_ps<br>GPIO1B0 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x1 | gpio1b0_pe<br>GPIO1B0 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

**VCCIO1_4_IOC_GPIO1C_P**

Address: Operational Base + offset (0x0118)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | gpio1c7_ps<br>GPIO1C7 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 14 | RW | 0x1 | gpio1c7_pe<br>GPIO1C7 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 13 | RW | 0x0 | gpio1c6_ps<br>GPIO1C6 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 12 | RW | 0x1 | gpio1c6_pe<br>GPIO1C6 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 11 | RW | 0x0 | gpio1c5_ps<br>GPIO1C5 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 10 | RW | 0x1 | gpio1c5_pe<br>GPIO1C5 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 9 | RW | 0x0 | gpio1c4_ps<br>GPIO1C4 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 8 | RW | 0x1 | gpio1c4_pe<br>GPIO1C4 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x0 | gpio1c3_ps<br>GPIO1C3 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 6 | RW | 0x1 | gpio1c3_pe<br>GPIO1C3 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 5 | RW | 0x0 | gpio1c2_ps<br>GPIO1C2 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 4 | RW | 0x1 | gpio1c2_pe<br>GPIO1C2 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 3 | RW | 0x0 | gpio1c1_ps<br>GPIO1C1 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 2 | RW | 0x0 | gpio1c1_pe<br>GPIO1C1 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 1 | RW | 0x0 | gpio1c0_ps<br>GPIO1C0 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 0 | RW | 0x0 | gpio1c0_pe<br>GPIO1C0 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

**VCCIO1_4_IOC_GPIO1D_P**

Address: Operational Base + offset (0x011C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | gpio1d7_ps<br>GPIO1D7 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14 | RW | 0x1 | gpio1d7_pe<br>GPIO1D7 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 13 | RW | 0x1 | gpio1d6_ps<br>GPIO1D6 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 12 | RW | 0x1 | gpio1d6_pe<br>GPIO1D6 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 11 | RW | 0x0 | gpio1d5_ps<br>GPIO1D5 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 10 | RW | 0x1 | gpio1d5_pe<br>GPIO1D5 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 9 | RW | 0x0 | gpio1d4_ps<br>GPIO1D4 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 8 | RW | 0x1 | gpio1d4_pe<br>GPIO1D4 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 7 | RW | 0x0 | gpio1d3_ps<br>GPIO1D3 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 6 | RW | 0x1 | gpio1d3_pe<br>GPIO1D3 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 5 | RW | 0x0 | gpio1d2_ps<br>GPIO1D2 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 4 | RW | 0x1 | gpio1d2_pe<br>GPIO1D2 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | gpio1d1_ps<br>GPIO1D1 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 2 | RW | 0x1 | gpio1d1_pe<br>GPIO1D1 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 1 | RW | 0x0 | gpio1d0_ps<br>GPIO1D0 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 0 | RW | 0x1 | gpio1d0_pe<br>GPIO1D0 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

**VCCIO1_4_IOC_GPIO1A_IE**

Address: Operational Base + offset (0x0180)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x1 | gpio1a7_ie<br>GPIO1A7 IE control<br>Active High input buffer enable |
| 6 | RW | 0x1 | gpio1a6_ie<br>GPIO1A6 IE control<br>Active High input buffer enable |
| 5 | RW | 0x1 | gpio1a5_ie<br>GPIO1A5 IE control<br>Active High input buffer enable |
| 4 | RW | 0x1 | gpio1a4_ie<br>GPIO1A4 IE control<br>Active High input buffer enable |
| 3 | RW | 0x1 | gpio1a3_ie<br>GPIO1A3 IE control<br>Active High input buffer enable |
| 2 | RW | 0x1 | gpio1a2_ie<br>GPIO1A2 IE control<br>Active High input buffer enable |
| 1 | RW | 0x1 | gpio1a1_ie<br>GPIO1A1 IE control<br>Active High input buffer enable |
| 0 | RW | 0x1 | gpio1a0_ie<br>GPIO1A0 IE control<br>Active High input buffer enable |

**VCCIO1_4_IOC_GPIO1B_IE**

Rockchip Confidencial

Address: Operational Base + offset (0x0184)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x1 | gpio1b7_ie<br>GPIO1B7 IE control<br>Active High input buffer enable |
| 6 | RW | 0x1 | gpio1b6_ie<br>GPIO1B6 IE control<br>Active High input buffer enable |
| 5 | RW | 0x1 | gpio1b5_ie<br>GPIO1B5 IE control<br>Active High input buffer enable |
| 4 | RW | 0x1 | gpio1b4_ie<br>GPIO1B4 IE control<br>Active High input buffer enable |
| 3 | RW | 0x1 | gpio1b3_ie<br>GPIO1B3 IE control<br>Active High input buffer enable |
| 2 | RW | 0x1 | gpio1b2_ie<br>GPIO1B2 IE control<br>Active High input buffer enable |
| 1 | RW | 0x1 | gpio1b1_ie<br>GPIO1B1 IE control<br>Active High input buffer enable |
| 0 | RW | 0x1 | gpio1b0_ie<br>GPIO1B0 IE control<br>Active High input buffer enable |

**VCCIO1_4_IOC_GPIO1C_IE**

Address: Operational Base + offset (0x0188)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x1 | gpio1c7_ie<br>GPIO1C7 IE control<br>Active High input buffer enable |
| 6 | RW | 0x1 | gpio1c6_ie<br>GPIO1C6 IE control<br>Active High input buffer enable |
| 5 | RW | 0x1 | gpio1c5_ie<br>GPIO1C5 IE control<br>Active High input buffer enable |
| 4 | RW | 0x1 | gpio1c4_ie<br>GPIO1C4 IE control<br>Active High input buffer enable |
| 3 | RW | 0x1 | gpio1c3_ie<br>GPIO1C3 IE control<br>Active High input buffer enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x1 | gpio1c2_ie<br>GPIO1C2 IE control<br>Active High input buffer enable |
| 1 | RW | 0x1 | gpio1c1_ie<br>GPIO1C1 IE control<br>Active High input buffer enable |
| 0 | RW | 0x1 | gpio1c0_ie<br>GPIO1C0 IE control<br>Active High input buffer enable |

**VCCIO1_4_IOC_GPIO1D_IE**

Address: Operational Base + offset (0x018C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x1 | gpio1d7_ie<br>GPIO1D7 IE control<br>Active High input buffer enable |
| 6 | RW | 0x1 | gpio1d6_ie<br>GPIO1D6 IE control<br>Active High input buffer enable |
| 5 | RW | 0x1 | gpio1d5_ie<br>GPIO1D5 IE control<br>Active High input buffer enable |
| 4 | RW | 0x1 | gpio1d4_ie<br>GPIO1D4 IE control<br>Active High input buffer enable |
| 3 | RW | 0x1 | gpio1d3_ie<br>GPIO1D3 IE control<br>Active High input buffer enable |
| 2 | RW | 0x1 | gpio1d2_ie<br>GPIO1D2 IE control<br>Active High input buffer enable |
| 1 | RW | 0x1 | gpio1d1_ie<br>GPIO1D1 IE control<br>Active High input buffer enable |
| 0 | RW | 0x1 | gpio1d0_ie<br>GPIO1D0 IE control<br>Active High input buffer enable |

**VCCIO1_4_IOC_GPIO1A_SMT**

Address: Operational Base + offset (0x0210)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x0 | gpio1a7_smt<br>GPIO1A7 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 6 | RW | 0x0 | gpio1a6_smt<br>GPIO1A6 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 5 | RW | 0x0 | gpio1a5_smt<br>GPIO1A5 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 4 | RW | 0x0 | gpio1a4_smt<br>GPIO1A4 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 3 | RW | 0x0 | gpio1a3_smt<br>GPIO1A3 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 2 | RW | 0x0 | gpio1a2_smt<br>GPIO1A2 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 1 | RW | 0x0 | gpio1a1_smt<br>GPIO1A1 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 0 | RW | 0x0 | gpio1a0_smt<br>GPIO1A0 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

**VCCIO1_4_IOC_GPIO1B_SMT**

Address: Operational Base + offset (0x0214)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | gpio1b7_smt<br>GPIO1B7 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | gpio1b6_smt<br>GPIO1B6 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 5 | RW | 0x0 | gpio1b5_smt<br>GPIO1B5 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 4 | RW | 0x0 | gpio1b4_smt<br>GPIO1B4 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 3 | RW | 0x0 | gpio1b3_smt<br>GPIO1B3 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 2 | RW | 0x0 | gpio1b2_smt<br>GPIO1B2 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 1 | RW | 0x0 | gpio1b1_smt<br>GPIO1B1 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 0 | RW | 0x0 | gpio1b0_smt<br>GPIO1B0 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

**VCCIO1_4_IOC_GPIO1C_SMT**

Address: Operational Base + offset (0x0218)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | gpio1c7_smt<br>GPIO1C7 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 6 | RW | 0x0 | gpio1c6_smt<br>GPIO1C6 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | gpio1c5_smt<br>GPIO1C5 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 4 | RW | 0x0 | gpio1c4_smt<br>GPIO1C4 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 3 | RW | 0x0 | gpio1c3_smt<br>GPIO1C3 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 2 | RW | 0x0 | gpio1c2_smt<br>GPIO1C2 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 1 | RW | 0x0 | gpio1c1_smt<br>GPIO1C1 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 0 | RW | 0x0 | gpio1c0_smt<br>GPIO1C0 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

**VCCIO1_4_IOC_GPIO1D_SMT**

Address: Operational Base + offset (0x021C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | gpio1d7_smt<br>GPIO1D7 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 6 | RW | 0x0 | gpio1d6_smt<br>GPIO1D6 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 5 | RW | 0x0 | gpio1d5_smt<br>GPIO1D5 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | gpio1d4_smt<br>GPIO1D4 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 3 | RW | 0x0 | gpio1d3_smt<br>GPIO1D3 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 2 | RW | 0x0 | gpio1d2_smt<br>GPIO1D2 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 1 | RW | 0x0 | gpio1d1_smt<br>GPIO1D1 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 0 | RW | 0x0 | gpio1d0_smt<br>GPIO1D0 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

**VCCIO1_4_IOC_GPIO_PDIS**

Address: Operational Base + offset (0x0280)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | vccio4_pull_dis<br>when 1'b1, disable VCCIO4 GPIO pull up/down when output enable |
| 0 | RW | 0x0 | vccio1_pull_dis<br>when 1'b1, disable VCCIO1 GPIO pull up/down when output enable |

# 6.29 VCCIO3_5_IOC Register Description

## 6.29.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VCCIO3_5_IOC_GPIO2A_DS_H | 0x0044 | W | 0x00001100 | GPIO2A Driver Strength Control High bits |
| VCCIO3_5_IOC_GPIO2B_DS_L | 0x0048 | W | 0x00001111 | GPIO2B Driver Strength Control Low bits |
| VCCIO3_5_IOC_GPIO2B_DS_H | 0x004C | W | 0x00001111 | GPIO2B Driver Strength Control High bits |

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VCCIO3_5_IOC_GPIO2C_DS_L | 0x0050 | W | 0x00001111 | GPIO2C Driver Strength Control Low bits |
| VCCIO3_5_IOC_GPIO2C_DS_H | 0x0054 | W | 0x00000011 | GPIO2C Driver Strength Control High bits |
| VCCIO3_5_IOC_GPIO3A_DS_L | 0x0060 | W | 0x00006666 | GPIO3A Driver Strength Control Low bits |
| VCCIO3_5_IOC_GPIO3A_DS_H | 0x0064 | W | 0x00006666 | GPIO3A Driver Strength Control High bits |
| VCCIO3_5_IOC_GPIO3B_DS_L | 0x0068 | W | 0x00006666 | GPIO3B Driver Strength Control Low bits |
| VCCIO3_5_IOC_GPIO3B_DS_H | 0x006C | W | 0x00006666 | GPIO3B Driver Strength Control High bits |
| VCCIO3_5_IOC_GPIO3C_DS_L | 0x0070 | W | 0x00006666 | GPIO3C Driver Strength Control Low bits |
| VCCIO3_5_IOC_GPIO3C_DS_H | 0x0074 | W | 0x00006666 | GPIO3C Driver Strength Control High bits |
| VCCIO3_5_IOC_GPIO3D_DS_L | 0x0078 | W | 0x00006666 | GPIO3D Driver Strength Control Low bits |
| VCCIO3_5_IOC_GPIO3D_DS_H | 0x007C | W | 0x00000066 | GPIO3D Driver Strength Control High bits |
| VCCIO3_5_IOC_GPIO4C_DS_L | 0x0090 | W | 0x00001100 | GPIO4C Driver Strength Control Low bits |
| VCCIO3_5_IOC_GPIO4C_DS_H | 0x0094 | W | 0x00000111 | GPIO4C Driver Strength Control High bits |
| VCCIO3_5_IOC_GPIO2A_P | 0x0120 | W | 0x0000F000 | GPIO2A Pull-up/down Control |
| VCCIO3_5_IOC_GPIO2B_P | 0x0124 | W | 0x00005F7F | GPIO2B Pull-up/down Control |
| VCCIO3_5_IOC_GPIO2C_P | 0x0128 | W | 0x00000555 | GPIO2C Pull-up/down Control |
| VCCIO3_5_IOC_GPIO3A_P | 0x0130 | W | 0x0000D5FF | GPIO3A Pull-up/down Control |
| VCCIO3_5_IOC_GPIO3B_P | 0x0134 | W | 0x00005FD7 | GPIO3B Pull-up/down Control |
| VCCIO3_5_IOC_GPIO3C_P | 0x0138 | W | 0x0000FF55 | GPIO3C Pull-up/down Control |
| VCCIO3_5_IOC_GPIO3D_P | 0x013C | W | 0x00000557 | GPIO3D Pull-up/down Control |
| VCCIO3_5_IOC_GPIO4C_P | 0x0148 | W | 0x00001550 | GPIO4C Pull-up/down Control |
| VCCIO3_5_IOC_GPIO2A_IE | 0x0190 | W | 0x000000C0 | GPIO2A Input Enable Control |
| VCCIO3_5_IOC_GPIO2B_IE | 0x0194 | W | 0x000000FF | GPIO2B Input Enable Control |
| VCCIO3_5_IOC_GPIO2C_IE | 0x0198 | W | 0x0000003F | GPIO2C Input Enable Control |
| VCCIO3_5_IOC_GPIO3A_IE | 0x01A0 | W | 0x000000FF | GPIO3A Input Enable Control |
| VCCIO3_5_IOC_GPIO3B_IE | 0x01A4 | W | 0x000000FF | GPIO3B Input Enable Control |
| VCCIO3_5_IOC_GPIO3C_IE | 0x01A8 | W | 0x000000FF | GPIO3C Input Enable Control |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VCCIO3_5_IOC_GPIO3D_IE | 0x01AC | W | 0x0000003F | GPIO3D Input Enable Control |
| VCCIO3_5_IOC_GPIO4C_IE | 0x01B8 | W | 0x0000007C | GPIO4C Input Enable Control |
| VCCIO3_5_IOC_GPIO2A_SMT | 0x0220 | W | 0x00000000 | GPIO2A Schmitt Trigger Control |
| VCCIO3_5_IOC_GPIO2B_SMT | 0x0224 | W | 0x00000000 | GPIO2B Schmitt Trigger Control |
| VCCIO3_5_IOC_GPIO2C_SMT | 0x0228 | W | 0x00000000 | GPIO2C Schmitt Trigger Control |
| VCCIO3_5_IOC_GPIO3A_SMT | 0x0230 | W | 0x00000000 | GPIO3A Schmitt Trigger Control |
| VCCIO3_5_IOC_GPIO3B_SMT | 0x0234 | W | 0x00000000 | GPIO3B Schmitt Trigger Control |
| VCCIO3_5_IOC_GPIO3C_SMT | 0x0238 | W | 0x00000000 | GPIO3C Schmitt Trigger Control |
| VCCIO3_5_IOC_GPIO3D_SMT | 0x023C | W | 0x00000000 | GPIO3D Schmitt Trigger Control |
| VCCIO3_5_IOC_GPIO4C_SMT | 0x0248 | W | 0x00000000 | GPIO4C Schmitt Trigger Control |
| VCCIO3_5_IOC_GPIO_PDIS | 0x0288 | W | 0x00000000 | Auto Pull-up/down disable Control |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.29.2 Detail Registers Description

**VCCIO3_5_IOC_GPIO2A_DS_H**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13:12 | RW | 0x1 | gpio2a7_ds<br>GPIO2A7 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 11:10 | RO | 0x0 | reserved |
| 9:8 | RW | 0x1 | gpio2a6_ds<br>GPIO2A6 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 7:0 | RO | 0x00 | reserved |

**VCCIO3_5_IOC_GPIO2B_DS_L**

Address: Operational Base + offset (0x0048)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13:12 | RW | 0x1 | gpio2b3_ds<br>GPIO2B3 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 11:10 | RO | 0x0 | reserved |
| 9:8 | RW | 0x1 | gpio2b2_ds<br>GPIO2B2 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 7:6 | RO | 0x0 | reserved |
| 5:4 | RW | 0x1 | gpio2b1_ds<br>GPIO2B1 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 3:2 | RO | 0x0 | reserved |
| 1:0 | RW | 0x1 | gpio2b0_ds<br>GPIO2B0 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |

**VCCIO3_5_IOC_GPIO2B_DS_H**

Address: Operational Base + offset (0x004C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13:12 | RW | 0x1 | gpio2b7_ds<br>GPIO2B7 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 11:10 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9:8 | RW | 0x1 | gpio2b6_ds<br>GPIO2B6 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 7:6 | RO | 0x0 | reserved |
| 5:4 | RW | 0x1 | gpio2b5_ds<br>GPIO2B5 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 3:2 | RO | 0x0 | reserved |
| 1:0 | RW | 0x1 | gpio2b4_ds<br>GPIO2B4 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |

**VCCIO3_5_IOC_GPIO2C_DS_L**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13:12 | RW | 0x1 | gpio2c3_ds<br>GPIO2C3 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 11:10 | RO | 0x0 | reserved |
| 9:8 | RW | 0x1 | gpio2c2_ds<br>GPIO2C2 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 7:6 | RO | 0x0 | reserved |
| 5:4 | RW | 0x1 | gpio2c1_ds<br>GPIO2C1 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:2 | RO | 0x0 | reserved |
| 1:0 | RW | 0x1 | gpio2c0_ds<br>GPIO2C0 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |

**VCCIO3_5_IOC_GPIO2C_DS_H**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5:4 | RW | 0x1 | gpio2c5_ds<br>GPIO2C5 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 3:2 | RO | 0x0 | reserved |
| 1:0 | RW | 0x1 | gpio2c4_ds<br>GPIO2C4 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |

**VCCIO3_5_IOC_GPIO3A_DS_L**

Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x6 | gpio3a3_ds<br>GPIO3A3 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10:8 | RW | 0x6 | gpio3a2_ds<br>GPIO3A2 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x6 | gpio3a1_ds<br>GPIO3A1 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio3a0_ds<br>GPIO3A0 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**VCCIO3_5_IOC_GPIO3A_DS_H**

Address: Operational Base + offset (0x0064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x6 | gpio3a7_ds<br>GPIO3A7 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10:8 | RW | 0x6 | gpio3a6_ds<br>GPIO3A6 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x6 | gpio3a5_ds<br>GPIO3A5 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio3a4_ds<br>GPIO3A4 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**VCCIO3_5_IOC_GPIO3B_DS_L**

Address: Operational Base + offset (0x0068)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x6 | gpio3b3_ds<br>GPIO3B3 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10:8 | RW | 0x6 | gpio3b2_ds<br>GPIO3B2 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x6 | gpio3b1_ds<br>GPIO3B1 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio3b0_ds<br>GPIO3B0 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**VCCIO3_5_IOC_GPIO3B_DS_H**

Address: Operational Base + offset (0x006C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x6 | gpio3b7_ds<br>GPIO3B7 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10:8 | RW | 0x6 | gpio3b6_ds<br>GPIO3B6 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x6 | gpio3b5_ds<br>GPIO3B5 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio3b4_ds<br>GPIO3B4 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**VCCIO3_5_IOC_GPIO3C_DS_L**

Address: Operational Base + offset (0x0070)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x6 | gpio3c3_ds<br>GPIO3C3 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10:8 | RW | 0x6 | gpio3c2_ds<br>GPIO3C2 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x6 | gpio3c1_ds<br>GPIO3C1 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio3c0_ds<br>GPIO3C0 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**VCCIO3_5_IOC_GPIO3C_DS_H**

Address: Operational Base + offset (0x0074)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x6 | gpio3c7_ds<br>GPIO3C7 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10:8 | RW | 0x6 | gpio3c6_ds<br>GPIO3C6 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x6 | gpio3c5_ds<br>GPIO3C5 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio3c4_ds<br>GPIO3C4 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**VCCIO3_5_IOC_GPIO3D_DS_L**

Address: Operational Base + offset (0x0078)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x6 | gpio3d3_ds<br>GPIO3D3 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10:8 | RW | 0x6 | gpio3d2_ds<br>GPIO3D2 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x6 | gpio3d1_ds<br>GPIO3D1 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio3d0_ds<br>GPIO3D0 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**VCCIO3_5_IOC_GPIO3D_DS_H**

Address: Operational Base + offset (0x007C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6:4 | RW | 0x6 | gpio3d5_ds<br>GPIO3D5 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2:0 | RW | 0x6 | gpio3d4_ds<br>GPIO3D4 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**VCCIO3_5_IOC_GPIO4C_DS_L**

Address: Operational Base + offset (0x0090)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13:12 | RW | 0x1 | gpio4c3_ds<br>GPIO4C3 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 11:10 | RO | 0x0 | reserved |
| 9:8 | RW | 0x1 | gpio4c2_ds<br>GPIO4C2 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 7:0 | RO | 0x00 | reserved |

**VCCIO3_5_IOC_GPIO4C_DS_H**

Address: Operational Base + offset (0x0094)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9:8 | RW | 0x1 | gpio4c6_ds<br>GPIO4C6 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 7:6 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5:4 | RW | 0x1 | gpio4c5_ds<br>GPIO4C5 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |
| 3:2 | RO | 0x0 | reserved |
| 1:0 | RW | 0x1 | gpio4c4_ds<br>GPIO4C4 DS control<br>Driver Strength Selection<br>2'b00: 2.5mA 100ohm<br>2'b10: 5mA 50ohm<br>2'b01: 7.5mA 33ohm<br>2'b11: 10mA 25ohm |

**VCCIO3_5_IOC_GPIO2A_P**

Address: Operational Base + offset (0x0120)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | gpio2a7_ps<br>GPIO2A7 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 14 | RW | 0x1 | gpio2a7_pe<br>GPIO2A7 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 13 | RW | 0x1 | gpio2a6_ps<br>GPIO2A6 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 12 | RW | 0x1 | gpio2a6_pe<br>GPIO2A6 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 11:0 | RO | 0x000 | reserved |

**VCCIO3_5_IOC_GPIO2B_P**

Address: Operational Base + offset (0x0124)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x0 | gpio2b7_ps<br>GPIO2B7 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 14 | RW | 0x1 | gpio2b7_pe<br>GPIO2B7 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 13 | RW | 0x0 | gpio2b6_ps<br>GPIO2B6 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 12 | RW | 0x1 | gpio2b6_pe<br>GPIO2B6 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 11 | RW | 0x1 | gpio2b5_ps<br>GPIO2B5 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 10 | RW | 0x1 | gpio2b5_pe<br>GPIO2B5 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 9 | RW | 0x1 | gpio2b4_ps<br>GPIO2B4 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 8 | RW | 0x1 | gpio2b4_pe<br>GPIO2B4 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 7 | RW | 0x0 | gpio2b3_ps<br>GPIO2B3 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 6 | RW | 0x1 | gpio2b3_pe<br>GPIO2B3 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 5 | RW | 0x1 | gpio2b2_ps<br>GPIO2B2 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x1 | gpio2b2_pe<br>GPIO2B2 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 3 | RW | 0x1 | gpio2b1_ps<br>GPIO2B1 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 2 | RW | 0x1 | gpio2b1_pe<br>GPIO2B1 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 1 | RW | 0x1 | gpio2b0_ps<br>GPIO2B0 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 0 | RW | 0x1 | gpio2b0_pe<br>GPIO2B0 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

**VCCIO3_5_IOC_GPIO2C_P**

Address: Operational Base + offset (0x0128)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | gpio2c5_ps<br>GPIO2C5 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 10 | RW | 0x1 | gpio2c5_pe<br>GPIO2C5 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 9 | RW | 0x0 | gpio2c4_ps<br>GPIO2C4 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 8 | RW | 0x1 | gpio2c4_pe<br>GPIO2C4 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x0 | gpio2c3_ps<br>GPIO2C3 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 6 | RW | 0x1 | gpio2c3_pe<br>GPIO2C3 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 5 | RW | 0x0 | gpio2c2_ps<br>GPIO2C2 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 4 | RW | 0x1 | gpio2c2_pe<br>GPIO2C2 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 3 | RW | 0x0 | gpio2c1_ps<br>GPIO2C1 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 2 | RW | 0x1 | gpio2c1_pe<br>GPIO2C1 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 1 | RW | 0x0 | gpio2c0_ps<br>GPIO2C0 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 0 | RW | 0x1 | gpio2c0_pe<br>GPIO2C0 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

**VCCIO3_5_IOC_GPIO3A_P**

Address: Operational Base + offset (0x0130)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | gpio3a7_ps<br>GPIO3A7 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14 | RW | 0x1 | gpio3a7_pe<br>GPIO3A7 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 13 | RW | 0x0 | gpio3a6_ps<br>GPIO3A6 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 12 | RW | 0x1 | gpio3a6_pe<br>GPIO3A6 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 11 | RW | 0x0 | gpio3a5_ps<br>GPIO3A5 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 10 | RW | 0x1 | gpio3a5_pe<br>GPIO3A5 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 9 | RW | 0x0 | gpio3a4_ps<br>GPIO3A4 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 8 | RW | 0x1 | gpio3a4_pe<br>GPIO3A4 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 7 | RW | 0x1 | gpio3a3_ps<br>GPIO3A3 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 6 | RW | 0x1 | gpio3a3_pe<br>GPIO3A3 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 5 | RW | 0x1 | gpio3a2_ps<br>GPIO3A2 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 4 | RW | 0x1 | gpio3a2_pe<br>GPIO3A2 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x1 | gpio3a1_ps<br>GPIO3A1 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 2 | RW | 0x1 | gpio3a1_pe<br>GPIO3A1 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 1 | RW | 0x1 | gpio3a0_ps<br>GPIO3A0 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 0 | RW | 0x1 | gpio3a0_pe<br>GPIO3A0 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

**VCCIO3_5_IOC_GPIO3B_P**

Address: Operational Base + offset (0x0134)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | gpio3b7_ps<br>GPIO3B7 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 14 | RW | 0x1 | gpio3b7_pe<br>GPIO3B7 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 13 | RW | 0x0 | gpio3b6_ps<br>GPIO3B6 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 12 | RW | 0x1 | gpio3b6_pe<br>GPIO3B6 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 11 | RW | 0x1 | gpio3b5_ps<br>GPIO3B5 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10 | RW | 0x1 | gpio3b5_pe<br>GPIO3B5 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 9 | RW | 0x1 | gpio3b4_ps<br>GPIO3B4 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 8 | RW | 0x1 | gpio3b4_pe<br>GPIO3B4 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 7 | RW | 0x1 | gpio3b3_ps<br>GPIO3B3 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 6 | RW | 0x1 | gpio3b3_pe<br>GPIO3B3 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 5 | RW | 0x0 | gpio3b2_ps<br>GPIO3B2 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 4 | RW | 0x1 | gpio3b2_pe<br>GPIO3B2 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 3 | RW | 0x0 | gpio3b1_ps<br>GPIO3B1 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 2 | RW | 0x1 | gpio3b1_pe<br>GPIO3B1 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 1 | RW | 0x1 | gpio3b0_ps<br>GPIO3B0 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 0 | RW | 0x1 | gpio3b0_pe<br>GPIO3B0 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

Rockchip Confidencial

**VCCIO3_5_IOC_GPIO3C_P**

Address: Operational Base + offset (0x0138)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | gpio3c7_ps<br>GPIO3C7 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 14 | RW | 0x1 | gpio3c7_pe<br>GPIO3C7 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 13 | RW | 0x1 | gpio3c6_ps<br>GPIO3C6 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 12 | RW | 0x1 | gpio3c6_pe<br>GPIO3C6 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 11 | RW | 0x1 | gpio3c5_ps<br>GPIO3C5 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 10 | RW | 0x1 | gpio3c5_pe<br>GPIO3C5 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 9 | RW | 0x1 | gpio3c4_ps<br>GPIO3C4 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 8 | RW | 0x1 | gpio3c4_pe<br>GPIO3C4 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 7 | RW | 0x0 | gpio3c3_ps<br>GPIO3C3 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x1 | gpio3c3_pe<br>GPIO3C3 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 5 | RW | 0x0 | gpio3c2_ps<br>GPIO3C2 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 4 | RW | 0x1 | gpio3c2_pe<br>GPIO3C2 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 3 | RW | 0x0 | gpio3c1_ps<br>GPIO3C1 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 2 | RW | 0x1 | gpio3c1_pe<br>GPIO3C1 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 1 | RW | 0x0 | gpio3c0_ps<br>GPIO3C0 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 0 | RW | 0x1 | gpio3c0_pe<br>GPIO3C0 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

**VCCIO3_5_IOC_GPIO3D_P**

Address: Operational Base + offset (0x013C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | gpio3d5_ps<br>GPIO3D5 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 10 | RW | 0x1 | gpio3d5_pe<br>GPIO3D5 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RW | 0x0 | gpio3d4_ps<br>GPIO3D4 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 8 | RW | 0x1 | gpio3d4_pe<br>GPIO3D4 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 7 | RW | 0x0 | gpio3d3_ps<br>GPIO3D3 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 6 | RW | 0x1 | gpio3d3_pe<br>GPIO3D3 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 5 | RW | 0x0 | gpio3d2_ps<br>GPIO3D2 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 4 | RW | 0x1 | gpio3d2_pe<br>GPIO3D2 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 3 | RW | 0x0 | gpio3d1_ps<br>GPIO3D1 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 2 | RW | 0x1 | gpio3d1_pe<br>GPIO3D1 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 1 | RW | 0x1 | gpio3d0_ps<br>GPIO3D0 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 0 | RW | 0x1 | gpio3d0_pe<br>GPIO3D0 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

**VCCIO3_5_IOC_GPIO4C_P**

Address: Operational Base + offset (0x0148)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | gpio4c6_ps<br>GPIO4C6 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 12 | RW | 0x1 | gpio4c6_pe<br>GPIO4C6 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 11 | RW | 0x0 | gpio4c5_ps<br>GPIO4C5 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 10 | RW | 0x1 | gpio4c5_pe<br>GPIO4C5 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 9 | RW | 0x0 | gpio4c4_ps<br>GPIO4C4 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 8 | RW | 0x1 | gpio4c4_pe<br>GPIO4C4 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 7 | RW | 0x0 | gpio4c3_ps<br>GPIO4C3 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 6 | RW | 0x1 | gpio4c3_pe<br>GPIO4C3 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 5 | RW | 0x0 | gpio4c2_ps<br>GPIO4C2 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 4 | RW | 0x1 | gpio4c2_pe<br>GPIO4C2 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RO | 0x0 | reserved |

**VCCIO3_5_IOC_GPIO2A_IE**

Address: Operational Base + offset (0x0190)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x1 | gpio2a7_ie<br>GPIO2A7 IE control<br>Active High input buffer enable |
| 6 | RW | 0x1 | gpio2a6_ie<br>GPIO2A6 IE control<br>Active High input buffer enable |
| 5:0 | RO | 0x00 | reserved |

**VCCIO3_5_IOC_GPIO2B_IE**

Address: Operational Base + offset (0x0194)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x1 | gpio2b7_ie<br>GPIO2B7 IE control<br>Active High input buffer enable |
| 6 | RW | 0x1 | gpio2b6_ie<br>GPIO2B6 IE control<br>Active High input buffer enable |
| 5 | RW | 0x1 | gpio2b5_ie<br>GPIO2B5 IE control<br>Active High input buffer enable |
| 4 | RW | 0x1 | gpio2b4_ie<br>GPIO2B4 IE control<br>Active High input buffer enable |
| 3 | RW | 0x1 | gpio2b3_ie<br>GPIO2B3 IE control<br>Active High input buffer enable |
| 2 | RW | 0x1 | gpio2b2_ie<br>GPIO2B2 IE control<br>Active High input buffer enable |
| 1 | RW | 0x1 | gpio2b1_ie<br>GPIO2B1 IE control<br>Active High input buffer enable |
| 0 | RW | 0x1 | gpio2b0_ie<br>GPIO2B0 IE control<br>Active High input buffer enable |

**VCCIO3_5_IOC_GPIO2C_IE**

Address: Operational Base + offset (0x0198)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x1 | gpio2c5_ie<br>GPIO2C5 IE control<br>Active High input buffer enable |
| 4 | RW | 0x1 | gpio2c4_ie<br>GPIO2C4 IE control<br>Active High input buffer enable |
| 3 | RW | 0x1 | gpio2c3_ie<br>GPIO2C3 IE control<br>Active High input buffer enable |
| 2 | RW | 0x1 | gpio2c2_ie<br>GPIO2C2 IE control<br>Active High input buffer enable |
| 1 | RW | 0x1 | gpio2c1_ie<br>GPIO2C1 IE control<br>Active High input buffer enable |
| 0 | RW | 0x1 | gpio2c0_ie<br>GPIO2C0 IE control<br>Active High input buffer enable |

**VCCIO3_5_IOC_GPIO3A_IE**

Address: Operational Base + offset (0x01A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x1 | gpio3a7_ie<br>GPIO3A7 IE control<br>Active High input buffer enable |
| 6 | RW | 0x1 | gpio3a6_ie<br>GPIO3A6 IE control<br>Active High input buffer enable |
| 5 | RW | 0x1 | gpio3a5_ie<br>GPIO3A5 IE control<br>Active High input buffer enable |
| 4 | RW | 0x1 | gpio3a4_ie<br>GPIO3A4 IE control<br>Active High input buffer enable |
| 3 | RW | 0x1 | gpio3a3_ie<br>GPIO3A3 IE control<br>Active High input buffer enable |
| 2 | RW | 0x1 | gpio3a2_ie<br>GPIO3A2 IE control<br>Active High input buffer enable |
| 1 | RW | 0x1 | gpio3a1_ie<br>GPIO3A1 IE control<br>Active High input buffer enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x1 | gpio3a0_ie<br>GPIO3A0 IE control<br>Active High input buffer enable |

**VCCIO3_5_IOC_GPIO3B_IE**

Address: Operational Base + offset (0x01A4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x1 | gpio3b7_ie<br>GPIO3B7 IE control<br>Active High input buffer enable |
| 6 | RW | 0x1 | gpio3b6_ie<br>GPIO3B6 IE control<br>Active High input buffer enable |
| 5 | RW | 0x1 | gpio3b5_ie<br>GPIO3B5 IE control<br>Active High input buffer enable |
| 4 | RW | 0x1 | gpio3b4_ie<br>GPIO3B4 IE control<br>Active High input buffer enable |
| 3 | RW | 0x1 | gpio3b3_ie<br>GPIO3B3 IE control<br>Active High input buffer enable |
| 2 | RW | 0x1 | gpio3b2_ie<br>GPIO3B2 IE control<br>Active High input buffer enable |
| 1 | RW | 0x1 | gpio3b1_ie<br>GPIO3B1 IE control<br>Active High input buffer enable |
| 0 | RW | 0x1 | gpio3b0_ie<br>GPIO3B0 IE control<br>Active High input buffer enable |

**VCCIO3_5_IOC_GPIO3C_IE**

Address: Operational Base + offset (0x01A8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x1 | gpio3c7_ie<br>GPIO3C7 IE control<br>Active High input buffer enable |
| 6 | RW | 0x1 | gpio3c6_ie<br>GPIO3C6 IE control<br>Active High input buffer enable |
| 5 | RW | 0x1 | gpio3c5_ie<br>GPIO3C5 IE control<br>Active High input buffer enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x1 | gpio3c4_ie<br>GPIO3C4 IE control<br>Active High input buffer enable |
| 3 | RW | 0x1 | gpio3c3_ie<br>GPIO3C3 IE control<br>Active High input buffer enable |
| 2 | RW | 0x1 | gpio3c2_ie<br>GPIO3C2 IE control<br>Active High input buffer enable |
| 1 | RW | 0x1 | gpio3c1_ie<br>GPIO3C1 IE control<br>Active High input buffer enable |
| 0 | RW | 0x1 | gpio3c0_ie<br>GPIO3C0 IE control<br>Active High input buffer enable |

**VCCIO3_5_IOC_GPIO3D_IE**

Address: Operational Base + offset (0x01AC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x1 | gpio3d5_ie<br>GPIO3D5 IE control<br>Active High input buffer enable |
| 4 | RW | 0x1 | gpio3d4_ie<br>GPIO3D4 IE control<br>Active High input buffer enable |
| 3 | RW | 0x1 | gpio3d3_ie<br>GPIO3D3 IE control<br>Active High input buffer enable |
| 2 | RW | 0x1 | gpio3d2_ie<br>GPIO3D2 IE control<br>Active High input buffer enable |
| 1 | RW | 0x1 | gpio3d1_ie<br>GPIO3D1 IE control<br>Active High input buffer enable |
| 0 | RW | 0x1 | gpio3d0_ie<br>GPIO3D0 IE control<br>Active High input buffer enable |

**VCCIO3_5_IOC_GPIO4C_IE**

Address: Operational Base + offset (0x01B8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x1 | gpio4c6_ie<br>GPIO4C6 IE control<br>Active High input buffer enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x1 | gpio4c5_ie<br>GPIO4C5 IE control<br>Active High input buffer enable |
| 4 | RW | 0x1 | gpio4c4_ie<br>GPIO4C4 IE control<br>Active High input buffer enable |
| 3 | RW | 0x1 | gpio4c3_ie<br>GPIO4C3 IE control<br>Active High input buffer enable |
| 2 | RW | 0x1 | gpio4c2_ie<br>GPIO4C2 IE control<br>Active High input buffer enable |
| 1:0 | RO | 0x0 | reserved |

**VCCIO3_5_IOC_GPIO2A_SMT**

Address: Operational Base + offset (0x0220)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | gpio2a7_smt<br>GPIO2A7 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 6 | RW | 0x0 | gpio2a6_smt<br>GPIO2A6 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 5:0 | RO | 0x00 | reserved |

**VCCIO3_5_IOC_GPIO2B_SMT**

Address: Operational Base + offset (0x0224)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | gpio2b7_smt<br>GPIO2B7 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 6 | RW | 0x0 | gpio2b6_smt<br>GPIO2B6 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | gpio2b5_smt<br>GPIO2B5 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 4 | RW | 0x0 | gpio2b4_smt<br>GPIO2B4 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 3 | RW | 0x0 | gpio2b3_smt<br>GPIO2B3 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 2 | RW | 0x0 | gpio2b2_smt<br>GPIO2B2 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 1 | RW | 0x0 | gpio2b1_smt<br>GPIO2B1 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 0 | RW | 0x0 | gpio2b0_smt<br>GPIO2B0 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

**VCCIO3_5_IOC_GPIO2C_SMT**

Address: Operational Base + offset (0x0228)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x0 | gpio2c5_smt<br>GPIO2C5 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 4 | RW | 0x0 | gpio2c4_smt<br>GPIO2C4 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 3 | RW | 0x0 | gpio2c3_smt<br>GPIO2C3 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | gpio2c2_smt<br>GPIO2C2 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 1 | RW | 0x0 | gpio2c1_smt<br>GPIO2C1 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 0 | RW | 0x0 | gpio2c0_smt<br>GPIO2C0 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

**VCCIO3_5_IOC_GPIO3A_SMT**

Address: Operational Base + offset (0x0230)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | gpio3a7_smt<br>GPIO3A7 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 6 | RW | 0x0 | gpio3a6_smt<br>GPIO3A6 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 5 | RW | 0x0 | gpio3a5_smt<br>GPIO3A5 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 4 | RW | 0x0 | gpio3a4_smt<br>GPIO3A4 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 3 | RW | 0x0 | gpio3a3_smt<br>GPIO3A3 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 2 | RW | 0x0 | gpio3a2_smt<br>GPIO3A2 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | gpio3a1_smt<br>GPIO3A1 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 0 | RW | 0x0 | gpio3a0_smt<br>GPIO3A0 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

**VCCIO3_5_IOC_GPIO3B_SMT**

Address: Operational Base + offset (0x0234)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | gpio3b7_smt<br>GPIO3B7 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 6 | RW | 0x0 | gpio3b6_smt<br>GPIO3B6 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 5 | RW | 0x0 | gpio3b5_smt<br>GPIO3B5 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 4 | RW | 0x0 | gpio3b4_smt<br>GPIO3B4 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 3 | RW | 0x0 | gpio3b3_smt<br>GPIO3B3 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 2 | RW | 0x0 | gpio3b2_smt<br>GPIO3B2 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 1 | RW | 0x0 | gpio3b1_smt<br>GPIO3B1 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | gpio3b0_smt<br>GPIO3B0 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

**VCCIO3_5_IOC_GPIO3C_SMT**

Address: Operational Base + offset (0x0238)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | gpio3c7_smt<br>GPIO3C7 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 6 | RW | 0x0 | gpio3c6_smt<br>GPIO3C6 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 5 | RW | 0x0 | gpio3c5_smt<br>GPIO3C5 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 4 | RW | 0x0 | gpio3c4_smt<br>GPIO3C4 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 3 | RW | 0x0 | gpio3c3_smt<br>GPIO3C3 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 2 | RW | 0x0 | gpio3c2_smt<br>GPIO3C2 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 1 | RW | 0x0 | gpio3c1_smt<br>GPIO3C1 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 0 | RW | 0x0 | gpio3c0_smt<br>GPIO3C0 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

Rockchip Confidencial

**VCCIO3_5_IOC_GPIO3D_SMT**

Address: Operational Base + offset (0x023C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x0 | gpio3d5_smt<br>GPIO3D5 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 4 | RW | 0x0 | gpio3d4_smt<br>GPIO3D4 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 3 | RW | 0x0 | gpio3d3_smt<br>GPIO3D3 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 2 | RW | 0x0 | gpio3d2_smt<br>GPIO3D2 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 1 | RW | 0x0 | gpio3d1_smt<br>GPIO3D1 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 0 | RW | 0x0 | gpio3d0_smt<br>GPIO3D0 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

**VCCIO3_5_IOC_GPIO4C_SMT**

Address: Operational Base + offset (0x0248)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x0 | gpio4c6_smt<br>GPIO4C6 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | gpio4c5_smt<br>GPIO4C5 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 4 | RW | 0x0 | gpio4c4_smt<br>GPIO4C4 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 3 | RW | 0x0 | gpio4c3_smt<br>GPIO4C3 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 2 | RW | 0x0 | gpio4c2_smt<br>GPIO4C2 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 1:0 | RO | 0x0 | reserved |

**VCCIO3_5_IOC_GPIO_PDIS**

Address: Operational Base + offset (0x0288)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | vccio5_pull_dis<br>when 1'b1, disable VCCIO5 GPIO pull up/down when output enable |
| 0 | RW | 0x0 | vccio3_pull_dis<br>when 1'b1, disable VCCIO3 GPIO pull up/down when output enable |

# 6.30 VCCIO2_IOC Register Description

## 6.30.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VCCIO2_IOC_GPIO4D_DS_L | 0x0098 | W | 0x00006666 | GPIO4D Driver Strength Control Low bits |
| VCCIO2_IOC_GPIO4D_DS_H | 0x009C | W | 0x00000066 | GPIO4D Driver Strength Control High bits |
| VCCIO2_IOC_GPIO4D_P | 0x014C | W | 0x000007FF | GPIO4D Pull-up/down Control |
| VCCIO2_IOC_GPIO4D_IE | 0x01BC | W | 0x0000003F | GPIO4D Input Enable Control |
| VCCIO2_IOC_GPIO4D_SMT | 0x024C | W | 0x00000000 | GPIO4D Schmitt Trigger Control |
| VCCIO2_IOC_GPIO_PDIS | 0x0284 | W | 0x00000000 | Auto Pull-up/down disable Control |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

Rockchip Confidencial

## 6.30.2 Detail Registers Description

**VCCIO2_IOC_GPIO4D_DS_L**

Address: Operational Base + offset (0x0098)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x6 | gpio4d3_ds<br>GPIO4D3 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x6 | gpio4d2_ds<br>GPIO4D2 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x6 | gpio4d1_ds<br>GPIO4D1 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio4d0_ds<br>GPIO4D0 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**VCCIO2_IOC_GPIO4D_DS_H**

Address: Operational Base + offset (0x009C)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6:4 | RW | 0x6 | gpio4d5_ds<br>GPIO4D5 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio4d4_ds<br>GPIO4D4 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**VCCIO2_IOC_GPIO4D_P**

Address: Operational Base + offset (0x014C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | gpio4d5_ps<br>GPIO4D5 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 10 | RW | 0x1 | gpio4d5_pe<br>GPIO4D5 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 9 | RW | 0x1 | gpio4d4_ps<br>GPIO4D4 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 8 | RW | 0x1 | gpio4d4_pe<br>GPIO4D4 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x1 | gpio4d3_ps<br>GPIO4D3 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 6 | RW | 0x1 | gpio4d3_pe<br>GPIO4D3 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 5 | RW | 0x1 | gpio4d2_ps<br>GPIO4D2 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 4 | RW | 0x1 | gpio4d2_pe<br>GPIO4D2 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 3 | RW | 0x1 | gpio4d1_ps<br>GPIO4D1 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 2 | RW | 0x1 | gpio4d1_pe<br>GPIO4D1 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 1 | RW | 0x1 | gpio4d0_ps<br>GPIO4D0 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 0 | RW | 0x1 | gpio4d0_pe<br>GPIO4D0 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

**VCCIO2_IOC_GPIO4D_IE**

Address: Operational Base + offset (0x01BC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x1 | gpio4d5_ie<br>GPIO4D5 IE control<br>Active High input buffer enable |
| 4 | RW | 0x1 | gpio4d4_ie<br>GPIO4D4 IE control<br>Active High input buffer enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x1 | gpio4d3_ie<br>GPIO4D3 IE control<br>Active High input buffer enable |
| 2 | RW | 0x1 | gpio4d2_ie<br>GPIO4D2 IE control<br>Active High input buffer enable |
| 1 | RW | 0x1 | gpio4d1_ie<br>GPIO4D1 IE control<br>Active High input buffer enable |
| 0 | RW | 0x1 | gpio4d0_ie<br>GPIO4D0 IE control<br>Active High input buffer enable |

**VCCIO2_IOC_GPIO4D_SMT**

Address: Operational Base + offset (0x024C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:6 | RO | 0x000 | reserved |
| 5 | RW | 0x0 | gpio4d5_smt<br>GPIO4D5 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 4 | RW | 0x0 | gpio4d4_smt<br>GPIO4D4 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 3 | RW | 0x0 | gpio4d3_smt<br>GPIO4D3 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 2 | RW | 0x0 | gpio4d2_smt<br>GPIO4D2 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 1 | RW | 0x0 | gpio4d1_smt<br>GPIO4D1 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 0 | RW | 0x0 | gpio4d0_smt<br>GPIO4D0 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

**VCCIO2_IOC_GPIO_PDIS**

Address: Operational Base + offset (0x0284)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | vccio2_pull_dis<br>when 1'b1, disable VCCIO2 GPIO pull up/down when output enable |

# 6.31 VCCIO6_IOC Register Description

## 6.31.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VCCIO6_IOC_GPIO4A_DS_L | 0x0080 | W | 0x00006666 | GPIO4A Driver Strength Control Low bits |
| VCCIO6_IOC_GPIO4A_DS_H | 0x0084 | W | 0x00006666 | GPIO4A Driver Strength Control High bits |
| VCCIO6_IOC_GPIO4B_DS_L | 0x0088 | W | 0x00006666 | GPIO4B Driver Strength Control Low bits |
| VCCIO6_IOC_GPIO4B_DS_H | 0x008C | W | 0x00006666 | GPIO4B Driver Strength Control High bits |
| VCCIO6_IOC_GPIO4C_DS_L | 0x0090 | W | 0x00000066 | GPIO4C Driver Strength Control Low bits |
| VCCIO6_IOC_GPIO4A_P | 0x0140 | W | 0x00005555 | GPIO4A Pull-up/down Control |
| VCCIO6_IOC_GPIO4B_P | 0x0144 | W | 0x0000D7FD | GPIO4B Pull-up/down Control |
| VCCIO6_IOC_GPIO4C_P | 0x0148 | W | 0x00000007 | GPIO4C Pull-up/down Control |
| VCCIO6_IOC_GPIO4A_IE | 0x01B0 | W | 0x000000FF | GPIO4A Input Enable Control |
| VCCIO6_IOC_GPIO4B_IE | 0x01B4 | W | 0x000000FF | GPIO4B Input Enable Control |
| VCCIO6_IOC_GPIO4C_IE | 0x01B8 | W | 0x00000003 | GPIO4C Input Enable Control |
| VCCIO6_IOC_GPIO4A_SMT | 0x0240 | W | 0x00000000 | GPIO4A Schmitt Trigger Control |
| VCCIO6_IOC_GPIO4B_SMT | 0x0244 | W | 0x00000000 | GPIO4B Schmitt Trigger Control |
| VCCIO6_IOC_GPIO4C_SMT | 0x0248 | W | 0x00000000 | GPIO4C Schmitt Trigger Control |
| VCCIO6_IOC_GPIO_PDIS | 0x028C | W | 0x00000000 | Auto Pull-up/down disable Control |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.31.2 Detail Registers Description

### VCCIO6_IOC_GPIO4A_DS_L

Address: Operational Base + offset (0x0080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14:12 | RW | 0x6 | gpio4a3_ds<br>GPIO4A3 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x6 | gpio4a2_ds<br>GPIO4A2 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x6 | gpio4a1_ds<br>GPIO4A1 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio4a0_ds<br>GPIO4A0 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**VCCIO6_IOC_GPIO4A_DS_H**

Address: Operational Base + offset (0x0084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14:12 | RW | 0x6 | gpio4a7_ds<br>GPIO4A7 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x6 | gpio4a6_ds<br>GPIO4A6 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x6 | gpio4a5_ds<br>GPIO4A5 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio4a4_ds<br>GPIO4A4 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**VCCIO6_IOC_GPIO4B_DS_L**

Address: Operational Base + offset (0x0088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14:12 | RW | 0x6 | gpio4b3_ds<br>GPIO4B3 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x6 | gpio4b2_ds<br>GPIO4B2 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x6 | gpio4b1_ds<br>GPIO4B1 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio4b0_ds<br>GPIO4B0 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**VCCIO6_IOC_GPIO4B_DS_H**

Address: Operational Base + offset (0x008C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14:12 | RW | 0x6 | gpio4b7_ds<br>GPIO4B7 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x6 | gpio4b6_ds<br>GPIO4B6 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x6 | gpio4b5_ds<br>GPIO4B5 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio4b4_ds<br>GPIO4B4 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**VCCIO6_IOC_GPIO4C_DS_L**

Address: Operational Base + offset (0x0090)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6:4 | RW | 0x6 | gpio4c1_ds<br>GPIO4C1 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio4c0_ds<br>GPIO4C0 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**VCCIO6_IOC_GPIO4A_P**

Address: Operational Base + offset (0x0140)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | gpio4a7_ps<br>GPIO4A7 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 14 | RW | 0x1 | gpio4a7_pe<br>GPIO4A7 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 13 | RW | 0x0 | gpio4a6_ps<br>GPIO4A6 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 12 | RW | 0x1 | gpio4a6_pe<br>GPIO4A6 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 11 | RW | 0x0 | gpio4a5_ps<br>GPIO4A5 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10 | RW | 0x1 | gpio4a5_pe<br>GPIO4A5 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 9 | RW | 0x0 | gpio4a4_ps<br>GPIO4A4 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 8 | RW | 0x1 | gpio4a4_pe<br>GPIO4A4 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 7 | RW | 0x0 | gpio4a3_ps<br>GPIO4A3 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 6 | RW | 0x1 | gpio4a3_pe<br>GPIO4A3 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 5 | RW | 0x0 | gpio4a2_ps<br>GPIO4A2 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 4 | RW | 0x1 | gpio4a2_pe<br>GPIO4A2 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 3 | RW | 0x0 | gpio4a1_ps<br>GPIO4A1 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 2 | RW | 0x1 | gpio4a1_pe<br>GPIO4A1 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 1 | RW | 0x0 | gpio4a0_ps<br>GPIO4A0 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 0 | RW | 0x1 | gpio4a0_pe<br>GPIO4A0 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

Rockchip Confidencial

**VCCIO6_IOC_GPIO4B_P**

Address: Operational Base + offset (0x0144)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | gpio4b7_ps<br>GPIO4B7 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 14 | RW | 0x1 | gpio4b7_pe<br>GPIO4B7 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 13 | RW | 0x0 | gpio4b6_ps<br>GPIO4B6 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 12 | RW | 0x1 | gpio4b6_pe<br>GPIO4B6 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 11 | RW | 0x0 | gpio4b5_ps<br>GPIO4B5 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 10 | RW | 0x1 | gpio4b5_pe<br>GPIO4B5 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 9 | RW | 0x1 | gpio4b4_ps<br>GPIO4B4 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 8 | RW | 0x1 | gpio4b4_pe<br>GPIO4B4 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 7 | RW | 0x1 | gpio4b3_ps<br>GPIO4B3 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x1 | gpio4b3_pe<br>GPIO4B3 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 5 | RW | 0x1 | gpio4b2_ps<br>GPIO4B2 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 4 | RW | 0x1 | gpio4b2_pe<br>GPIO4B2 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 3 | RW | 0x1 | gpio4b1_ps<br>GPIO4B1 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 2 | RW | 0x1 | gpio4b1_pe<br>GPIO4B1 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 1 | RW | 0x0 | gpio4b0_ps<br>GPIO4B0 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 0 | RW | 0x1 | gpio4b0_pe<br>GPIO4B0 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

**VCCIO6_IOC_GPIO4C_P**

Address: Operational Base + offset (0x0148)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | gpio4c1_ps<br>GPIO4C1 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 2 | RW | 0x1 | gpio4c1_pe<br>GPIO4C1 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x1 | gpio4c0_ps<br>GPIO4C0 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 0 | RW | 0x1 | gpio4c0_pe<br>GPIO4C0 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

**VCCIO6_IOC_GPIO4A_IE**

Address: Operational Base + offset (0x01B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x1 | gpio4a7_ie<br>GPIO4A7 IE control<br>Active High input buffer enable |
| 6 | RW | 0x1 | gpio4a6_ie<br>GPIO4A6 IE control<br>Active High input buffer enable |
| 5 | RW | 0x1 | gpio4a5_ie<br>GPIO4A5 IE control<br>Active High input buffer enable |
| 4 | RW | 0x1 | gpio4a4_ie<br>GPIO4A4 IE control<br>Active High input buffer enable |
| 3 | RW | 0x1 | gpio4a3_ie<br>GPIO4A3 IE control<br>Active High input buffer enable |
| 2 | RW | 0x1 | gpio4a2_ie<br>GPIO4A2 IE control<br>Active High input buffer enable |
| 1 | RW | 0x1 | gpio4a1_ie<br>GPIO4A1 IE control<br>Active High input buffer enable |
| 0 | RW | 0x1 | gpio4a0_ie<br>GPIO4A0 IE control<br>Active High input buffer enable |

**VCCIO6_IOC_GPIO4B_IE**

Address: Operational Base + offset (0x01B4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x1 | gpio4b7_ie<br>GPIO4B7 IE control<br>Active High input buffer enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x1 | gpio4b6_ie<br>GPIO4B6 IE control<br>Active High input buffer enable |
| 5 | RW | 0x1 | gpio4b5_ie<br>GPIO4B5 IE control<br>Active High input buffer enable |
| 4 | RW | 0x1 | gpio4b4_ie<br>GPIO4B4 IE control<br>Active High input buffer enable |
| 3 | RW | 0x1 | gpio4b3_ie<br>GPIO4B3 IE control<br>Active High input buffer enable |
| 2 | RW | 0x1 | gpio4b2_ie<br>GPIO4B2 IE control<br>Active High input buffer enable |
| 1 | RW | 0x1 | gpio4b1_ie<br>GPIO4B1 IE control<br>Active High input buffer enable |
| 0 | RW | 0x1 | gpio4b0_ie<br>GPIO4B0 IE control<br>Active High input buffer enable |

**VCCIO6_IOC_GPIO4C_IE**

Address: Operational Base + offset (0x01B8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x1 | gpio4c1_ie<br>GPIO4C1 IE control<br>Active High input buffer enable |
| 0 | RW | 0x1 | gpio4c0_ie<br>GPIO4C0 IE control<br>Active High input buffer enable |

**VCCIO6_IOC_GPIO4A_SMT**

Address: Operational Base + offset (0x0240)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | gpio4a7_smt<br>GPIO4A7 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 6 | RW | 0x0 | gpio4a6_smt<br>GPIO4A6 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | gpio4a5_smt<br>GPIO4A5 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 4 | RW | 0x0 | gpio4a4_smt<br>GPIO4A4 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 3 | RW | 0x0 | gpio4a3_smt<br>GPIO4A3 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 2 | RW | 0x0 | gpio4a2_smt<br>GPIO4A2 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 1 | RW | 0x0 | gpio4a1_smt<br>GPIO4A1 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 0 | RW | 0x0 | gpio4a0_smt<br>GPIO4A0 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

**VCCIO6_IOC_GPIO4B_SMT**

Address: Operational Base + offset (0x0244)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | gpio4b7_smt<br>GPIO4B7 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 6 | RW | 0x0 | gpio4b6_smt<br>GPIO4B6 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 5 | RW | 0x0 | gpio4b5_smt<br>GPIO4B5 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | gpio4b4_smt<br>GPIO4B4 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 3 | RW | 0x0 | gpio4b3_smt<br>GPIO4B3 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 2 | RW | 0x0 | gpio4b2_smt<br>GPIO4B2 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 1 | RW | 0x0 | gpio4b1_smt<br>GPIO4B1 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 0 | RW | 0x0 | gpio4b0_smt<br>GPIO4B0 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

**VCCIO6_IOC_GPIO4C_SMT**

Address: Operational Base + offset (0x0248)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | gpio4c1_smt<br>GPIO4C1 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 0 | RW | 0x0 | gpio4c0_smt<br>GPIO4C0 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

**VCCIO6_IOC_GPIO_PDIS**

Address: Operational Base + offset (0x028C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | vccio6_pull_dis<br>when 1'b1, disable VCCIO6 GPIO pull up/down when output enable |

# 6.32 EMMC_IOC Register Description

## 6.32.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| EMMC_IOC_GPIO2A_DS_L | 0x0040 | W | 0x00006666 | GPIO2A Driver Strength Control Low bits |
| EMMC_IOC_GPIO2D_DS_L | 0x0058 | W | 0x00006666 | GPIO2D Driver Strength Control Low bits |
| EMMC_IOC_GPIO2D_DS_H | 0x005C | W | 0x00006666 | GPIO2D Driver Strength Control High bits |
| EMMC_IOC_GPIO2A_P | 0x0120 | W | 0x00000057 | GPIO2A Pull-up/down Control |
| EMMC_IOC_GPIO2D_P | 0x012C | W | 0x0000FFFF | GPIO2D Pull-up/down Control |
| EMMC_IOC_GPIO2A_IE | 0x0190 | W | 0x0000000F | GPIO2A Input Enable Control |
| EMMC_IOC_GPIO2D_IE | 0x019C | W | 0x000000FF | GPIO2D Input Enable Control |
| EMMC_IOC_GPIO2A_SMT | 0x0220 | W | 0x00000000 | GPIO2A Schmitt Trigger Control |
| EMMC_IOC_GPIO2D_SMT | 0x022C | W | 0x00000000 | GPIO2D Schmitt Trigger Control |
| EMMC_IOC_GPIO_PDIS | 0x0290 | W | 0x00000000 | Auto Pull-up/down disable Control |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 6.32.2 Detail Registers Description

**EMMC_IOC_GPIO2A_DS_L**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x6 | gpio2a3_ds<br>GPIO2A3 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x6 | gpio2a2_ds<br>GPIO2A2 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x6 | gpio2a1_ds<br>GPIO2A1 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio2a0_ds<br>GPIO2A0 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**EMMC_IOC_GPIO2D_DS_L**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x6 | gpio2d3_ds<br>GPIO2D3 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x6 | gpio2d2_ds<br>GPIO2D2 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6:4 | RW | 0x6 | gpio2d1_ds<br>GPIO2D1 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio2d0_ds<br>GPIO2D0 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**EMMC_IOC_GPIO2D_DS_H**

Address: Operational Base + offset (0x005C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x6 | gpio2d7_ds<br>GPIO2D7 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x6 | gpio2d6_ds<br>GPIO2D6 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 7 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6:4 | RW | 0x6 | gpio2d5_ds<br>GPIO2D5 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x6 | gpio2d4_ds<br>GPIO2D4 DS control<br>Driver Strength Selection<br>3'b000: 100ohm<br>3'b100: 66ohm<br>3'b010: 50ohm<br>3'b110: 40ohm<br>3'b001: 33ohm<br>3'b101: 25ohm |

**EMMC_IOC_GPIO2A_P**

Address: Operational Base + offset (0x0120)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | gpio2a3_ps<br>GPIO2A3 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 6 | RW | 0x1 | gpio2a3_pe<br>GPIO2A3 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 5 | RW | 0x0 | gpio2a2_ps<br>GPIO2A2 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 4 | RW | 0x1 | gpio2a2_pe<br>GPIO2A2 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 3 | RW | 0x0 | gpio2a1_ps<br>GPIO2A1 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x1 | gpio2a1_pe<br>GPIO2A1 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 1 | RW | 0x1 | gpio2a0_ps<br>GPIO2A0 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 0 | RW | 0x1 | gpio2a0_pe<br>GPIO2A0 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

**EMMC_IOC_GPIO2D_P**

Address: Operational Base + offset (0x012C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | gpio2d7_ps<br>GPIO2D7 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 14 | RW | 0x1 | gpio2d7_pe<br>GPIO2D7 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 13 | RW | 0x1 | gpio2d6_ps<br>GPIO2D6 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 12 | RW | 0x1 | gpio2d6_pe<br>GPIO2D6 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 11 | RW | 0x1 | gpio2d5_ps<br>GPIO2D5 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 10 | RW | 0x1 | gpio2d5_pe<br>GPIO2D5 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RW | 0x1 | gpio2d4_ps<br>GPIO2D4 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 8 | RW | 0x1 | gpio2d4_pe<br>GPIO2D4 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 7 | RW | 0x1 | gpio2d3_ps<br>GPIO2D3 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 6 | RW | 0x1 | gpio2d3_pe<br>GPIO2D3 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 5 | RW | 0x1 | gpio2d2_ps<br>GPIO2D2 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 4 | RW | 0x1 | gpio2d2_pe<br>GPIO2D2 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 3 | RW | 0x1 | gpio2d1_ps<br>GPIO2D1 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 2 | RW | 0x1 | gpio2d1_pe<br>GPIO2D1 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |
| 1 | RW | 0x1 | gpio2d0_ps<br>GPIO2D0 PS control<br>Weak PU/PD Resistor Selection<br>1'b0: PD Selection<br>1'b1: PU Selection |
| 0 | RW | 0x1 | gpio2d0_pe<br>GPIO2D0 PE control<br>Active High Weak PU/PD Resistor Enable<br>1'b0: PU/PD Disable<br>1'b1: PU/PD Enable |

**EMMC_IOC_GPIO2A_IE**

Address: Operational Base + offset (0x0190)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x1 | gpio2a3_ie<br>GPIO2A3 IE control<br>Active High input buffer enable |
| 2 | RW | 0x1 | gpio2a2_ie<br>GPIO2A2 IE control<br>Active High input buffer enable |
| 1 | RW | 0x1 | gpio2a1_ie<br>GPIO2A1 IE control<br>Active High input buffer enable |
| 0 | RW | 0x1 | gpio2a0_ie<br>GPIO2A0 IE control<br>Active High input buffer enable |

**EMMC_IOC_GPIO2D_IE**

Address: Operational Base + offset (0x019C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x1 | gpio2d7_ie<br>GPIO2D7 IE control<br>Active High input buffer enable |
| 6 | RW | 0x1 | gpio2d6_ie<br>GPIO2D6 IE control<br>Active High input buffer enable |
| 5 | RW | 0x1 | gpio2d5_ie<br>GPIO2D5 IE control<br>Active High input buffer enable |
| 4 | RW | 0x1 | gpio2d4_ie<br>GPIO2D4 IE control<br>Active High input buffer enable |
| 3 | RW | 0x1 | gpio2d3_ie<br>GPIO2D3 IE control<br>Active High input buffer enable |
| 2 | RW | 0x1 | gpio2d2_ie<br>GPIO2D2 IE control<br>Active High input buffer enable |
| 1 | RW | 0x1 | gpio2d1_ie<br>GPIO2D1 IE control<br>Active High input buffer enable |
| 0 | RW | 0x1 | gpio2d0_ie<br>GPIO2D0 IE control<br>Active High input buffer enable |

**EMMC_IOC_GPIO2A_SMT**

Address: Operational Base + offset (0x0220)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | gpio2a3_smt<br>GPIO2A3 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 2 | RW | 0x0 | gpio2a2_smt<br>GPIO2A2 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 1 | RW | 0x0 | gpio2a1_smt<br>GPIO2A1 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 0 | RW | 0x0 | gpio2a0_smt<br>GPIO2A0 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

**EMMC_IOC_GPIO2D_SMT**

Address: Operational Base + offset (0x022C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | gpio2d7_smt<br>GPIO2D7 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 6 | RW | 0x0 | gpio2d6_smt<br>GPIO2D6 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 5 | RW | 0x0 | gpio2d5_smt<br>GPIO2D5 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 4 | RW | 0x0 | gpio2d4_smt<br>GPIO2D4 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | gpio2d3_smt<br>GPIO2D3 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 2 | RW | 0x0 | gpio2d2_smt<br>GPIO2D2 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 1 | RW | 0x0 | gpio2d1_smt<br>GPIO2D1 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |
| 0 | RW | 0x0 | gpio2d0_smt<br>GPIO2D0 SMT control<br>CMOS/Schmitt Trigger Selection<br>1'b0: CMOS Input<br>1'b1: Schmitt Trigger input |

**EMMC_IOC_GPIO_PDIS**

Address: Operational Base + offset (0x0290)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | emmcio_pull_dis<br>when 1'b1, disable VCCIO6 GPIO pull up/down when output enable |

# 6.33 Application Notes

## 6.33.1 Memory Configuration

**RM/RMA/RMB**

Read-Write margin Input. This input is used for setting the ReadWrite margin. It programs the sense amp differential setting and write time window which allows the trade off between speed and robustness.

**RA**

Read Assist Pins to control WL under-drive.

**WA**

WA[1] Write assist enable pin (Active High). WA[0:0] Write Assist pin to control negative voltage on SRAM bitline.

**WPULSE**

Write Assist Pulse pins. These pins control the start time of the bitline negative coupling.

**WMD/WMDA/WMDB**

Rockchip Confidencial

When enabled it is used to add more delay in the Write cycle for internal clock pulse. No change in the read cycle internal clock pulse.

**LS**
Light Sleep Input. When this pin is active then memory goes into low leakage mode, there is no change in the output state.

**TEST_RNM**
When this pin is high Memory will go in idle state and bit-lines are pre-charged high.

**TEST1**
Test pin to bypass self-timed circuit. The external clock controls the read and write control signals.

**TESTRWM**
Test mode for read write margin control.

Rockchip Confidencial

# Chapter 7 Power Management Unit (PMU)

## 7.1 Overview

In order to meet low power requirements, a power management unit (PMU) is designed for controlling power resources in RK3588. The RK3588 PMU is dedicated for managing the power of the whole chip.
PMU supports the following features:

- Support multi voltage domains: VD_BIGCORE0, VD_BIGCORE1, VD_LITDSU, VD_GPU, VD_NPU, VD_VCODEC, VD_DDR01, VD_DDR23, VD_LOGIC, VD_PMU
- Support multi power domains in VD_BIGCORE0: PD_CPU_4, PD_CPU_5
- Support multi power domains in VD_BIGCORE1: PD_CPU_6, PD_CPU_7
- Support multi power domains in VD_LITDSU: PD_CPU_0, PD_CPU_1, PD_CPU_2, PD_CPU_3
- Support multi power domains in VD_NPU: PD_NPUTOP, PD_NPU1, PD_NPU2
- Support multi power domains in VD_VCODEC: PD_RKVDEC0, PD_RKVDEC1, PD_VENC0, PD_VENC1
- Support multi power domains in VD_LOGIC: PD_VDPU, PD_RGA30, PD_AV1, PD_VI, PD_FEC, PD_ISP1, PD_RGA31, PD_VOP, PD_VO0, PD_VO1, PD_AUDIO, PD_PHP, PD_GMAC, PD_PCIE, PD_NVM, PD_NVM0, PD_SDIO, PD_USB, PD_SECURE, PD_SDMMC, PD_CRYPTO, PD_CENTER, PD_VOP_CLUSTER0, PD_VOP_CLUSTER1, PD_VOP_CLUSTER2, PD_VOP_CLUSTER3, PD_VOP_DSC8K, PD_VOP_DSC4K, PD_VOP_ESMART
- Support one power domain in VD_PMU: PD_PMU1
- Support BIU idle operations: BIU_BIGCORE0, BIU_BIGCORE1, BIU_DSU, BIU_LITDSU, BIU_GPU, BIU_NPUTOP, BIU_NPU1, BIU_NPU2, BIU_VENC0, BIU_VENC1, BIU_RKVDEC0, BIU_RKVDEC1, BIU_VDPU, BIU_AV1, BIU_ISP1, BIU_RGA31, BIU_VOP, BIU_VOP_CHANNEL, BIU_VO0, BIU_VO1, BIU_AUDIO, BIU_NVM, BIU_SDIO, BIU_USB, BIU_PHP, BIU_VO1USBTOP, BIU_SECURE, BIU_SECURE_CENTER_CHANNEL, BIU_SECURE_VO1USB_CHANNEL, BIU_CENTER, BIU_CENTER_CHANNEL, BIU_DDRSCH0, BIU_DDRSCH1, BIU_DDRSCH2, BIU_DDRSCH3, BIU_CENTER_DDRSCH, BIU_BUS, BIU_TOP, BIU_PMU1
- Support CPU auto power down and DSU auto power down
- Support power down/up all power domains by software or hardware
- Support power down/up all voltage domains by software or hardware
- Support to send idle request to BIU
- Support low frequency clock source from PMU_PVTM
- Support PMU clock switch to low frequency clock in low power mode
- Support PLLs power down/up by hardware in low power mode
- Support OSC enable/disable request in low power mode
- Support to clamp all VD_PMU input before power off VD_LOGIC in low power mode
- Support wakeup reset control in power off mode
- Support DDR self-refresh in low power mode
- Support DDR controller clock auto gating in low power mode
- Support varies configurable wakeup source for low power mode
- Support memory repair for all memory in system by software or hardware

## 7.2 Block Diagram

The following figure is the PMU block diagram. The PMU includes the 3 following sections:

- APB Interface and Register: Provide AMBA APB interface for register read and write
- System Power State Control: Provide power management for various low power modes
- Power Gating Control: Provide power gating control for power domains

Rockchip Confidential

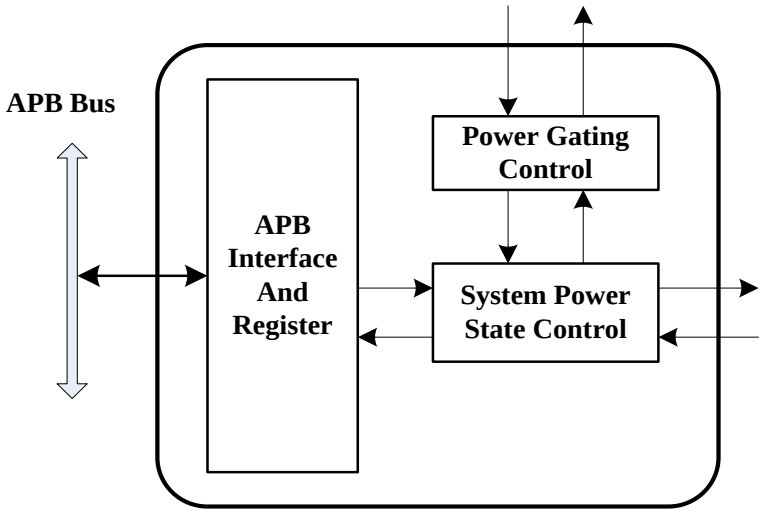



Fig. 7-1 PMU Bock Diagram

# 7.3 Function Description

## 7.3.1 Domain Description

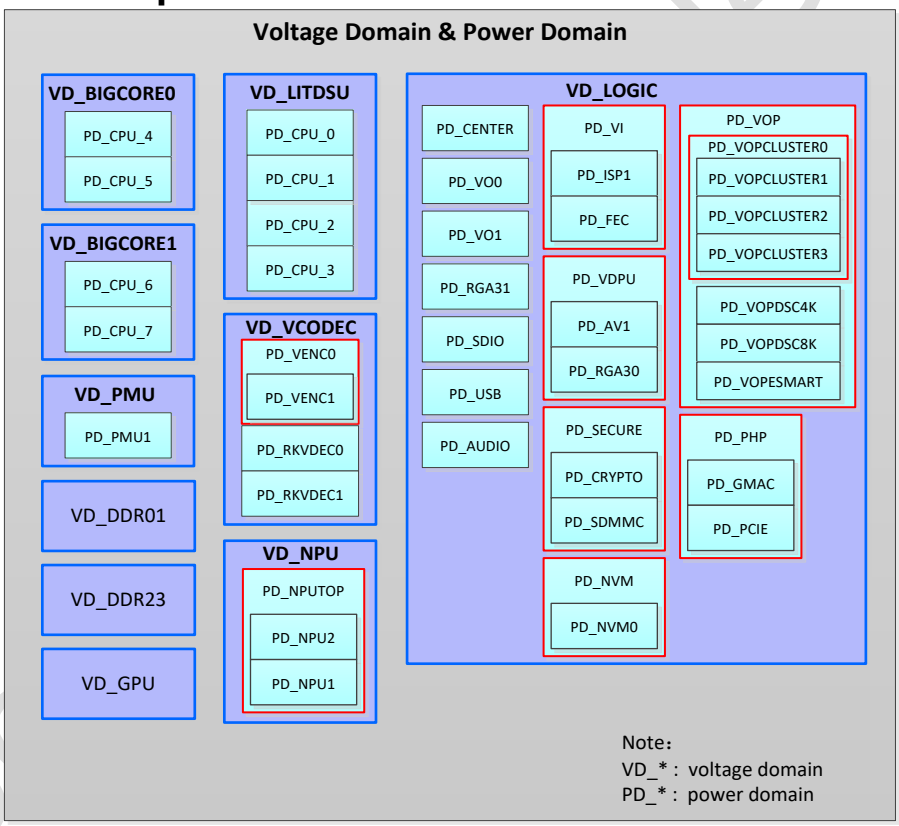



Fig. 7-2 RK3588 Voltage Domain and Power Domain Partition

The above diagram describes the power domain and voltage domain partition, and the following table lists IPs in every domain.

Table 7-1 RK3588 Voltage Domain and Power Domain Summary

| Voltage Domain | Power Domain | Description |
|---|---|---|
| VD_BIGCORE0 | PD_CPU_4 | A76_0 |
| | PD_CPU_5 | A76_1 |
| | ALIVE | BIU_BIGCORE0<br>PVTM_BIGCORE0<br>PVTPLL_BIGCORE0<br>BIGCORE0_CRU |

Rockchip Confidential

| Voltage Domain | Power Domain | Description |
|---|---|---|
| | | B0PLL<br>BIGCORE0_GRF |
| VD_BIGCORE 1 | PD_CPU_6 | A76_2 |
| | PD_CPU_7 | A76_3 |
| | ALIVE | BIU_BIGCORE1<br>PVTM_BIGCORE1<br>PVTPLL_BIGCORE1<br>BIGCORE1_CRU<br>B1PLL<br>BIGCORE1_GRF |
| VD_LITDSU | PD_CPU_0 | A55_0 |
| | PD_CPU_1 | A55_1 |
| | PD_CPU_2 | A55_2 |
| | PD_CPU_3 | A55_3 |
| | ALIVE | BIU_LITDSU<br>BIU_DSU<br>PVTM_LITDSU<br>PVTPLL_LITDSU<br>LITDSU_CRU<br>LPLL<br>LITDSU_GRF<br>LITDSU_SGRF<br>DSU/L3<br>DAP_LITE2<br>DEBUG_APB |
| VD_NPU | PD_NPUTOP | BIU_NPUTOP<br>MCU_NPU<br>PVTM_NPU<br>PVTPLL_NPU<br>WDT_NPU<br>TIMER_NPU<br>RKNN_CORE0 |
| | PD_NPU1 | BIU_NPU1<br>RKNN_CORE1 |
| | PD_NPU2 | BIU_NPU2<br>RKNN_CORE2 |
| VD_GPU | | BIU_GPU<br>Odin MP4<br>PVTM_GPU<br>PVTPLL_GPU<br>GPU_GRF |
| VD_VCODEC | PD_RKVDEC0 | BIU_RKVDEC0<br>RKVDEC0 & CCU |
| | PD_RKVDEC1 | BIU_RKVDEC1<br>RKVDEC1 |
| | PD_VENC0 | BIU_VENC0<br>RKVENC0 |
| | PD_VENC1 | BIU_VENC1<br>RKVENC1 |
| VD_DDR01 | | BIU_DDRSCH0<br>BIU_DDRSCH1<br>DDRCTRL_CH0<br>DDRCTRL_CH1<br>DDRPHY_CH0 |

Rockchip Confidencial

| Voltage Domain | Power Domain | Description |
|---|---|---|
| | | DDRPHY_CH1<br>DDR_SCRAMBLE_CH0<br>DDR_SCRAMBLE_CH1<br>DDR_MONITOR_CH0<br>DDR_MONITOR_CH1<br>DDR_CH01_GRF<br>DDR_CH01_CRU<br>D0APLL<br>D0BPLL<br>D1APLL<br>D1BPLL |
| VD_DDR23 | | BIU_DDRSCH2<br>BIU_DDRSCH3<br>DDRCTRL_CH2<br>DDRCTRL_CH3<br>DDRPHY_CH2<br>DDRPHY_CH3<br>DDR_SCRAMBLE_CH2<br>DDR_SCRAMBLE_CH3<br>DDR_MONITOR_CH2<br>DDR_MONITOR_CH3<br>DDR_CH23_GRF<br>DDR_CH23_CRU<br>D2APLL<br>D2BPLL<br>D3APLL<br>D3BPLL |
| VD_LOGIC | PD_CENTER | BIU_CENTER<br>BIU_CENTER_DDRSCH<br>BIU_CENTER_CHANNEL<br>SHARE_MEMORY<br>MCU_DDR<br>WDT_CENTER<br>TIMER_2CH_DDR<br>DMA2DDR<br>CENTER_GRF |
| | PD_VDPU | BIU_VDPU<br>VDPU<br>JPEG_ENC0<br>JPEG_ENC1<br>JPEG_ENC2<br>JPEG_ENC3<br>JPEG_DEC<br>RGA2<br>IEP |
| | PD_RGA30 | RGA3_0 |
| | PD_AV1 | BIU_AV1<br>AV1 |
| | PD_VOP | BIU_VOP<br>BIU_VOP_CHANNEL<br>VOP<br>DSIHOST0<br>DSIHOST1<br>VOP_GRF |
| | PD_VOPCLUSTE | VOP_CLUSTER0 |

Rockchip Confidencial

| Voltage Domain | Power Domain | Description |
|---|---|---|
| | R0 | |
| | PD_VOPCLUSTER1 | VOP_CLUSTER1 |
| | PD_VOPCLUSTER2 | VOP_CLUSTER2 |
| | PD_VOPCLUSTER3 | VOP_CLUSTER3 |
| | PD_VOPDSC8K | VOP_DSC8K |
| | PD_VOPDSC4K | VOP_DSC4K |
| | PD_VOPESMART | VOP_ESMART1<br>VOP_ESMART2<br>VOP_ESMART3 |
| | PD_VO0 | BIU_VO0<br>HDCP0<br>HDCP0_KEY<br>TRNG0<br>DP0<br>DP1<br>I2S4_8CH<br>I2S8_8CH<br>SPDIF2<br>SPDIF5<br>VO0_GRF |
| | PD_VO1 | BIU_VO1<br>HDCP1<br>HDCP1_KEY<br>TRNG1<br>eDP0<br>eDP1<br>HDMITX0<br>HDMITX1<br>HDMIRX<br>I2S5_8CH<br>I2S6_8CH<br>I2S7_8CH<br>I2S9_8CH<br>I2S10_8CH<br>SPDIF3<br>SPDIF4<br>SPDIF_RX0<br>SPDIF_RX1<br>SPDIF_RX2<br>VO1_GRF |
| | PD_VI | BIU_VI<br>VIPCAP<br>ISP0<br>CSIHOST0<br>CSIHOST1<br>CSIHOST2<br>CSIHOST3<br>CSIHOST4<br>CSIHOST5 |
| | PD_ISP1 | BIU_ISP1<br>ISP1 |

Rockchip Confidencial

| Voltage Domain | Power Domain | Description |
|---|---|---|
| | PD_FEC | FishEye0<br>FishEye1 |
| | PD_RGA31 | BIU_RGA31<br>RGA3_1 |
| | PD_USB | BIU_USB<br>USB2HOST_0<br>USB2HOST_1<br>USB3OTG_0<br>USB3OTG_1<br>USB_GRF |
| | PD_PHP | BIU_PHP<br>MMU600_PHP<br>MMU600_PCIE<br>GIC600(ITS)<br>USB3OTG_2<br>SATA_0<br>SATA_1<br>SATA_2<br>PCIE3_1L0<br>PCIE3_1L1<br>PCIE3_1L2<br>PHP_GRF |
| | PD_GMAC | GMAC_0<br>GMAC_1 |
| | PD_PCIE | PCIE3_2L<br>PCIE3_4L |
| | PD_NVM | BIU_NVN |
| | PD_NVM0 | FSPI<br>EMMC |
| | PD_SDIO | BIU_SDIO<br>SDIO |
| | PD_AUDIO | BIU_AUDIO<br>I2S0_8CH<br>I2S2_2CH<br>I2S3_2CH<br>PDM1<br>SPDIF0<br>SPDIF1<br>DSM_PWM |
| | PD_SECURE | BIU_SECURE |
| | PD_SDMMC | SDMMC |
| | PD_CRYPTO | SEC_SCRU<br>SEC_SGRF<br>DCF<br>OTP_S<br>TIMER_S<br>WDT_S<br>KEY_READER<br>TRNG_CHK0<br>TRNG_CHK1<br>TRNG_S<br>BOOTROM_S<br>KEYLADDER<br>CRYPTO_S |

Rockchip Confidencial

| Voltage Domain | Power Domain | Description |
|---|---|---|
| | | CRYPTO_NS<br>TRNG_NS<br>BOOTROM_NS<br>SDMMC_BUFFER |
| | ALIVE(PD_BUS) | BIU_TOP<br>BIU_BUS<br>BIU_SECURE_CENTER_CHANNEL<br>BIU_SECURE_VO1USB_CHANNEL<br>BIU_VO1USBTOP<br>PMU2<br>BUS_SCRU<br>BUS_SGRF<br>JDG_CHK0<br>JDG_CHK1<br>SPINLOCK<br>GIC600<br>DMAC0<br>DMAC1<br>DMAC2<br>TIMER_NS_0<br>TIMER_NS_1<br>WDT_NS<br>MAILBOX0<br>MAILBOX1<br>MAILBOX2<br>INT256MUX4<br>TSADC<br>SARADC<br>DECOM<br>OTP_TM<br>OTP_NS<br>SYS_GRF<br>BUS_IOC<br>CRU_NS<br>I2C1~I2C8<br>PWM1~PWM3<br>SPI0~SPI4<br>UART1~UART9<br>CAN0~CAN2<br>GPIO1~GPIO4<br>HDMI_DP_PHY0~HDMI_DP_PHY1<br>USB3_DP_PHY0~USB3_DP_PHY1<br>HDMI_DP_PHY0~HDMI_DP_PHY1<br>MIPI_DC_PHY0~MIPI_DC_PHY1<br>PCIE2_SATA_PHY0~ PCIE2_SATA_PHY2<br>USB2_PHY0~USB2_PHY3 HDMI_CSI_DPHY<br>PCIE3_PHY |
| VD_PMU | PD_PMU1 | BIU_PMU1<br>PMU1_CRU<br>PMU1_GRF<br>PMU1_SGRF<br>PMU1_IOC<br>PMU1<br>PMU_WDT<br>I2C0 |

Rockchip Confidencial

| Voltage Domain | Power Domain | Description |
|---|---|---|
| | | PWM0<br>PMU_TIMER<br>UART0<br>PMU_MEM<br>OSC_CHK<br>MCU_PMU<br>VAD<br>I2S1_8CH<br>PDM0<br>PMU1_PAD<br>PMU1_PMUX |
| | ALIVE | PMU0_CRU<br>PMU0_GRF<br>PMU0_SGRF<br>PMU0_IOC<br>PMU0<br>GPIO0<br>PVTM_PMU<br>SCRAMBLE_KEY<br>PMU0_PAD<br>PMU0_PMUX |

### 7.3.2 Operation Mode

We define two operation modes of PMU, software power mode and hardware power mode. When operating at software power mode, that means software can manage power sources directly by accessing PMU registers. For example, CPU or MCU_PMU can write PMU_PWR_GATE_CON0/1/2 registers to determine that power off/on which power domain independently.

When operating at hardware power mode, software manages power sources indirectly through FSM (Finite States Machine) in PMU and those settings always not take effect immediately. That means software also can configure PMU registers to power down/up some power resources, but these setting will not be executed immediately after configuration. They will be delayed to execute after FSM running in particular phase. And the specific power sources will be controlled during specific status in FSM. So the low power mode is a "delay affect" way to handle power sources inside the RK3588 chip.

### 7.3.3 Low Power Mode

There are 2 low power modes defined for RK3588: Power mode 0, Power mode 1.

Power mode 0: Ultra low power mode. In this power mode, all logic except ALIVE in VD_PMU0 can be power off or power down. Chip can be waked up by GPIO interrupt triggered by IO in PMUIO1 domain.

Power mode 1: Low power mode. In this power mode, all logic except ALIVE and PD_PMU1 in VD_PMU0 can be power off or power down. Chip can be waked up by GPIO interrupt triggered by IO in PMUIO1 and PMUIO2 domain or other wake up source from PD_PMU1 when in hardware power mode, or wake up by MCU_PMU when in hardware power mode.

## 7.4 Register Description

RK3588 PMU registers are divided into 3 parts for flexible applications:

- Offset = 0x0000~0x3FFF: registers defined in PMU0, in ALIVE of VD_PMU;
- Offset = 0x4000~0x7FFF: registers defined in PMU1, in PD_PMU1;
- Offset = 0x8000~0xBFFF: registers defined in PMU2, in ALIVE of VD_LOGIC.

Rockchip Confidencial

### 7.4.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PMU_PWR_CON0 | 0x0000 | W | 0x00000000 | PMU power control 0 register |
| PMU_WAKEUP_INT_CON_P0 | 0x0008 | W | 0x00000000 | PMU wake up interrupt control register for power mode 0 |
| PMU_WAKEUP_INT_STS_P0 | 0x000C | W | 0x00000000 | PMU wake up interrupt status register for power mode 0 |
| PMU_PMIC_STABLE_CNT_P0 | 0x0010 | W | 0x000FFFFF | PMIC stable count register for power mode 0 |
| PMU_WAKEUP_RST_CLR_CNT_P0 | 0x0014 | W | 0x000FFFFF | Wake up reset clear count register for power mode 0 |
| PMU_OSC_STABLE_CNT_P0 | 0x0018 | W | 0x000FFFFF | Oscillator stable count register for power mode 0 |
| PMU_PMU1_PWR_CHAIN_STABLE_CON | 0x001C | W | 0x00003E3F | PD_PMU1 power chain stable control register |
| PMU_DDR_RET_CON0_P0 | 0x0020 | W | 0x00000000 | DDR retention control register 0 for power mode 0 |
| PMU_DDR_RET_CON1_P0 | 0x0024 | W | 0x00000000 | DDR retention control register 1 for power mode 0 |
| PMU_INFO_TX_CON | 0x0030 | W | 0x00000000 | PMU debug information transmit control register |
| PMU_VERSION | 0x4000 | W | 0x00003588 | PMU version register |
| PMU_PWR_CON1 | 0x4004 | W | 0x00000000 | PMU power control 1 register |
| PMU_GLB_POWER_STS | 0x4008 | W | 0x00000000 | PMU global power status register |
| PMU_INT_MASK_CON | 0x400C | W | 0x00000000 | PMU interrupt mask control register |
| PMU_WAKEUP_INT_CON | 0x4010 | W | 0x00000000 | PMU wake up interrupt control register |
| PMU_WAKEUP_INT_STS | 0x4014 | W | 0x00000000 | PMU wake up interrupt status register |
| PMU_DDR_CH0_PWR_CON | 0x4020 | W | 0x00000000 | DDR channel 0 hardware power control register |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PMU_DDR_CH1_PWR_CON | 0x4024 | W | 0x00000000 | DDR channel 1 hardware power control register |
| PMU_DDR_CH2_PWR_CON | 0x4028 | W | 0x00000000 | DDR channel 2 hardware power control register |
| PMU_DDR_CH3_PWR_CON | 0x402C | W | 0x00000000 | DDR channel 3 hardware power control register |
| PMU_DDR_CH0_PWR_SFTCON | 0x4030 | W | 0x00000000 | DDR channel 0 software power control register |
| PMU_DDR_CH1_PWR_SFTCON | 0x4034 | W | 0x00000000 | DDR channel 1 software power control register |
| PMU_DDR_CH2_PWR_SFTCON | 0x4038 | W | 0x00000000 | DDR channel 2 software power control register |
| PMU_DDR_CH3_PWR_SFTCON | 0x403C | W | 0x00000000 | DDR channel 3 software power control register |
| PMU_DDR_POWER_STS | 0x4040 | W | 0x00000000 | DDR power state register |
| PMU_DDR_STS | 0x4044 | W | 0x00000000 | DDR state register |
| PMU_CRU_PWR_CON | 0x4050 | W | 0x00000000 | Clock and reset hardware power control register |
| PMU_CRU_PWR_SFTCON | 0x4054 | W | 0x00000000 | Clock and reset software power control register |
| PMU_CRU_POWER_STS | 0x4058 | W | 0x00000000 | Clock and reset power state register |
| PMU_PLLPD_CON0 | 0x4060 | W | 0x00000000 | PLL hardware power control register 0 |
| PMU_PLLPD_CON1 | 0x4064 | W | 0x00000000 | PLL hardware power control register 1 |
| PMU_PLLPD_SFTCON0 | 0x4068 | W | 0x00000000 | PLL software power control register 0 |
| PMU_PLLPD_SFTCON1 | 0x406C | W | 0x00000000 | PLL software power control register 1 |
| PMU_PMIC_STABLE_CNT | 0x4080 | W | 0x000FFFFF | PMIC stable count register |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PMU_OSC_STABLE_CNT | 0x4084 | W | 0x000FFFFF | Oscillator stable count register |
| PMU_WAKEUP_RST_CLR_CNT | 0x4088 | W | 0x000FFFFF | Wake up reset clear count register |
| PMU_PLL_LOCK_CNT | 0x408C | W | 0x000FFFFF | PLL lock count register |
| PMU_WAKEUP_TIMEOUT_CNT | 0x4094 | W | 0x00005DC0 | PMU wake up timeout count register |
| PMU_PWM_SWITCH_CNT | 0x4098 | W | 0x000FFFFF | PWM switch stable count register |
| PMU_SYS_REG0 | 0x4100 | W | 0x00000000 | PMU system register 0 |
| PMU_SYS_REG1 | 0x4104 | W | 0x00000000 | PMU system register 1 |
| PMU_SYS_REG2 | 0x4108 | W | 0x00000000 | PMU system register 2 |
| PMU_SYS_REG3 | 0x410C | W | 0x00000000 | PMU system register 3 |
| PMU_SYS_REG4 | 0x4110 | W | 0x00000000 | PMU system register 4 |
| PMU_SYS_REG5 | 0x4114 | W | 0x00000000 | PMU system register 5 |
| PMU_SYS_REG6 | 0x4118 | W | 0x00000000 | PMU system register 6 |
| PMU_SYS_REG7 | 0x411C | W | 0x00000000 | PMU system register 7 |
| PMU_PWR_CON2 | 0x8000 | W | 0x00000000 | PMU hardware power control 2 register |
| PMU_DSU_PWR_CON | 0x8004 | W | 0x00000000 | DSU hardware power control register |
| PMU_DSU_PWR_SFTCON | 0x8008 | W | 0x00000000 | DSU software power control register |
| PMU_DSU_AUTO_PWR_CON | 0x800C | W | 0x00000000 | DSU automatic power control register |
| PMU_CPU0_AUTO_PWR_CON | 0x8010 | W | 0x00000000 | CPU0 automatic power control register |
| PMU_CPU1_AUTO_PWR_CON | 0x8014 | W | 0x00000000 | CPU1 automatic power control register |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PMU_CPU2_AUTO_PWR_CON | 0x8018 | W | 0x00000000 | CPU2 automatic power control register |
| PMU_CPU3_AUTO_PWR_CON | 0x801C | W | 0x00000000 | CPU3 automatic power control register |
| PMU_CPU4_AUTO_PWR_CON | 0x8020 | W | 0x00000000 | CPU4 automatic power control register |
| PMU_CPU5_AUTO_PWR_CON | 0x8024 | W | 0x00000000 | CPU5 automatic power control register |
| PMU_CPU6_AUTO_PWR_CON | 0x8028 | W | 0x00000000 | CPU6 automatic power control register |
| PMU_CPU7_AUTO_PWR_CON | 0x802C | W | 0x00000000 | CPU7 automatic power control register |
| PMU_CPU0_PWR_SFTCON | 0x8030 | W | 0x000000C0 | CPU0 software power control register |
| PMU_CPU1_PWR_SFTCON | 0x8034 | W | 0x000000C0 | CPU1 software power control register |
| PMU_CPU2_PWR_SFTCON | 0x8038 | W | 0x000000C0 | CPU2 software power control register |
| PMU_CPU3_PWR_SFTCON | 0x803C | W | 0x000000C0 | CPU3 software power control register |
| PMU_CPU4_PWR_SFTCON | 0x8040 | W | 0x000000C0 | CPU4 software power control register |
| PMU_CPU5_PWR_SFTCON | 0x8044 | W | 0x000000C0 | CPU5 software power control register |
| PMU_CPU6_PWR_SFTCON | 0x8048 | W | 0x000000C0 | CPU6 software power control register |
| PMU_CPU7_PWR_SFTCON | 0x804C | W | 0x000000C0 | CPU7 software power control register |
| PMU_CORE0_PWR_CON | 0x8050 | W | 0x00000008 | BIGCORE0 hardware power control register |
| PMU_CORE1_PWR_CON | 0x8054 | W | 0x00000008 | BIGCORE1 hardware power control register |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PMU_CORE0_PWR_SFTCON | 0x8058 | W | 0x00000000 | BIGCORE0 software power control register |
| PMU_CORE1_PWR_SFTCON | 0x805C | W | 0x00000000 | BIGCORE1 software power control register |
| PMU_CORE0_AUTO_PWR_CON | 0x8060 | W | 0x00000000 | BIGCORE0 automatic power control register |
| PMU_CORE1_AUTO_PWR_CON | 0x8064 | W | 0x00000000 | BIGCORE1 automatic power control register |
| PMU_CLUSTER_BIU_AUTO_CON | 0x8068 | W | 0x00000000 | Cluster BIU automatic power control register |
| PMU_CLUSTER_BIU_IDLE_CON | 0x8070 | W | 0x00000000 | Cluster BIU idle request hardware control register |
| PMU_CLUSTER_BIU_IDLE_SFTCON | 0x8074 | W | 0x00000000 | Cluster BIU idle request software control register |
| PMU_CLUSTER_BIU_IDLE_ACK_STS | 0x8078 | W | 0x00000000 | Cluster BIU idle acknowledge status register |
| PMU_CLUSTER_BIU_IDLE_STS | 0x807C | W | 0x00000000 | Cluster BIU idle status register |
| PMU_CLUSTER_STS | 0x8080 | W | 0x00000000 | Cluster status register |
| PMU_CLUSTER_POWER_STS0 | 0x8084 | W | 0x00000000 | Cluster power status register 0 |
| PMU_CLUSTER_POWER_STS1 | 0x8088 | W | 0x00000000 | Cluster power status register 1 |
| PMU_CLUSTER_PCHANNEL_STS0 | 0x808C | W | 0x00000000 | Cluster P-Channel status register 0 |
| PMU_CLUSTER_PCHANNEL_STS1 | 0x8090 | W | 0x00000000 | Cluster P-Channel status register 1 |
| PMU_CLUSTER_PCHANNEL_STS2 | 0x8094 | W | 0x00000000 | Cluster P-Channel status register 2 |
| PMU_CPU_PWR_CHAIN_STABLE_CON | 0x8098 | W | 0x000000FF | CPU power chain stable control register |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PMU_DSU_MEM_PWR_CON | 0x809C | W | 0x00000000 | DSU memory power control register |
| PMU_DSU_STABLE_CNT | 0x80B0 | W | 0x000FFFFF | DSU power stable count register |
| PMU_DSU_PWRUP_CNT | 0x80B4 | W | 0x00005DC0 | DSU power up count register |
| PMU_DSU_PWRDN_CNT | 0x80B8 | W | 0x00005DC0 | DSU power down count register |
| PMU_CORE0_STABLE_CNT | 0x80BC | W | 0x000FFFFF | BIGCORE0 power stable count register |
| PMU_CORE0_PWRUP_CNT | 0x80C0 | W | 0x00005DC0 | BIGCORE0 power up count register |
| PMU_CORE0_PWRDN_CNT | 0x80C4 | W | 0x00005DC0 | BIGCORE0 power down count register |
| PMU_CORE1_STABLE_CNT | 0x80C8 | W | 0x000FFFFF | BIGCORE1 power stable count register |
| PMU_CORE1_PWRUP_CNT | 0x80CC | W | 0x00005DC0 | BIGCORE1 power up count register |
| PMU_CORE1_PWRDN_CNT | 0x80D0 | W | 0x00005DC0 | BIGCORE1 power down count register |
| PMU_CPU0_DBG_RST_CNT | 0x80D4 | W | 0x000FFFFF | CPU0 debug reset count register |
| PMU_CPU1_DBG_RST_CNT | 0x80D8 | W | 0x000FFFFF | CPU1 debug reset count register |
| PMU_CPU2_DBG_RST_CNT | 0x80DC | W | 0x000FFFFF | CPU2 debug reset count register |
| PMU_CPU3_DBG_RST_CNT | 0x80E0 | W | 0x000FFFFF | CPU3 debug reset count register |
| PMU_CPU4_DBG_RST_CNT | 0x80E4 | W | 0x000FFFFF | CPU4 debug reset count register |
| PMU_CPU5_DBG_RST_CNT | 0x80E8 | W | 0x000FFFFF | CPU5 debug reset count register |
| PMU_CPU6_DBG_RST_CNT | 0x80EC | W | 0x000FFFFF | CPU6 debug reset count register |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PMU_CPU7_DBG_RST_CNT | 0x80F0 | W | 0x000FFFFF | CPU7 debug reset count register |
| PMU_BIU_IDLE_CON0 | 0x8100 | W | 0x00000000 | BIU idle request hardware control register 0 |
| PMU_BIU_IDLE_CON1 | 0x8104 | W | 0x00000000 | BIU idle request hardware control register 1 |
| PMU_BIU_IDLE_CON2 | 0x8108 | W | 0x00000000 | BIU idle request hardware control register 2 |
| PMU_BIU_IDLE_SFTCON0 | 0x810C | W | 0x00000000 | BIU idle request software control register 0 |
| PMU_BIU_IDLE_SFTCON1 | 0x8110 | W | 0x00000000 | BIU idle request software control register 1 |
| PMU_BIU_IDLE_SFTCON2 | 0x8114 | W | 0x00000000 | BIU idle request software control register 2 |
| PMU_BIU_IDLE_ACK_STS0 | 0x8118 | W | 0x00000000 | BIU idle acknowledge status register 0 |
| PMU_BIU_IDLE_ACK_STS1 | 0x811C | W | 0x00000000 | BIU idle acknowledge status register 1 |
| PMU_BIU_IDLE_STS0 | 0x8120 | W | 0x00000000 | BIU idle status register 0 |
| PMU_BIU_IDLE_STS1 | 0x8124 | W | 0x00000000 | BIU idle status register 1 |
| PMU_BIU_AUTO_CON0 | 0x8128 | W | 0x00000000 | BIU automatic power control register 0 |
| PMU_BIU_AUTO_CON1 | 0x812C | W | 0x00000000 | BIU automatic power control register 1 |
| PMU_BIU_AUTO_CON2 | 0x8130 | W | 0x00000000 | BIU automatic power control register 2 |
| PMU_PWR_GATE_CON0 | 0x8140 | W | 0x00000000 | Power domain hardware power control register 0 |
| PMU_PWR_GATE_CON1 | 0x8144 | W | 0x00000000 | Power domain hardware power control register 1 |
| PMU_PWR_GATE_CON2 | 0x8148 | W | 0x00000000 | Power domain hardware power control register 2 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PMU_PWR_GATE_SFTCON0 | 0x814C | W | 0x0000FFF9 | Power domain software power control register 0 |
| PMU_PWR_GATE_SFTCON1 | 0x8150 | W | 0x000000FF | Power domain software power control register 1 |
| PMU_PWR_GATE_SFTCON2 | 0x8154 | W | 0x00000000 | Power domain software power control register 2 |
| PMU_VOL_GATE_CON0 | 0x8158 | W | 0x00000000 | Voltage domain power control register 0 |
| PMU_VOL_GATE_CON1 | 0x8160 | W | 0x00000000 | Voltage domain power control register 1 |
| PMU_PWR_CHAIN_PWRUP_CON0 | 0x8164 | W | 0x0000FFF8 | Power chain stable control register 0 for power up |
| PMU_PWR_CHAIN_PWRUP_CON1 | 0x8168 | W | 0x0000FFFF | Power chain stable control register 1 for power up |
| PMU_PWR_CHAIN_PWRDN_CON0 | 0x8170 | W | 0x00000000 | Power chain stable control register 0 for power down |
| PMU_PWR_CHAIN_PWRDN_CON1 | 0x8174 | W | 0x00000000 | Power chain stable control register 1 for power down |
| PMU_PWR_STABLE_CNT | 0x817C | W | 0x001F001F | Power chain stable count register |
| PMU_PWR_GATE_STS0 | 0x8180 | W | 0x00FFFFFF | Power domain power status register 0 |
| PMU_PWR_GATE_STS1 | 0x8184 | W | 0x00000000 | Power domain power status register 1 |
| PMU_PWR_GATE_POWER_STS | 0x8188 | W | 0x00000000 | Power gating status register |
| PMU_VOL_GATE_FAST_CON | 0x818C | W | 0x00000000 | Voltage domain fast power control register |
| PMU_GPU_PWRUP_CNT | 0x8190 | W | 0x000FFFFF | VD_GPU power up count register |
| PMU_GPU_PWRDN_CNT | 0x8194 | W | 0x000FFFFF | VD_GPU power down count register |
| PMU_NPU_PWRUP_CNT | 0x8198 | W | 0x000FFFFF | VD_NPU power up count register |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PMU_NPU_PWRDN_CNT | 0x819C | W | 0x000FFFFF | VD_NPU power down count register |
| PMU_MEM_PWR_GATE_SFTCON0 | 0x81A0 | W | 0x00000000 | Memory software power control register 0 |
| PMU_MEM_PWR_GATE_SFTCON1 | 0x81A4 | W | 0x00000000 | Memory software power control register 1 |
| PMU_MEM_PWR_GATE_SFTCON2 | 0x81A8 | W | 0x00000000 | Memory software power control register 2 |
| PMU_SUBMEM_PWR_GATE_SFTCON0 | 0x81B0 | W | 0x00000000 | Submodule memory software power control register 0 |
| PMU_SUBMEM_PWR_GATE_SFTCON1 | 0x81B4 | W | 0x00000000 | Submodule memory software power control register 1 |
| PMU_SUBMEM_PWR_GATE_SFTCON2 | 0x81B8 | W | 0x00000000 | Submodule memory software power control register 2 |
| PMU_SUBMEM_PWR_GATE_STS | 0x81BC | W | 0x00000000 | Submodule memory power status register |
| PMU_SUBMEM_PWR_ACK_BYPASS_CON0 | 0x81C0 | W | 0x00000000 | Submodule memory power acknowledge bypass control register 0 |
| PMU_SUBMEM_PWR_ACK_BYPASS_CON1 | 0x81C4 | W | 0x00000000 | Submodule memory power acknowledge bypass control register 1 |
| PMU_QCHANNEL_PWR_CON | 0x81D0 | W | 0x00000000 | Q-Channel hardware power control register |
| PMU_QCHANNEL_PWR_SFTCON | 0x81D4 | W | 0x00000000 | Q-Channel software power control register |
| PMU_QCHANNEL_PWR_STS | 0x81D8 | W | 0x00000000 | Q-Channel power status register |
| PMU_DEBUG_INFO_CON | 0x81E0 | W | 0x00000000 | PMU debug information control register |
| PMU_VOP_SUBPD_PWR_CHAIN_STS | 0x81E4 | W | 0x00049249 | VOP sub-domain power chain status register |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PMU_PWR_CHAIN0_STS0 | 0x81E8 | W | 0x000000FF | Power domain power chain 0 status register 0 |
| PMU_PWR_CHAIN0_STS1 | 0x81EC | W | 0x000000FF | Power domain power chain 0 status register 1 |
| PMU_PWR_CHAIN1_STS0 | 0x81F0 | W | 0x000000FF | Power domain power chain 1 status register 0 |
| PMU_PWR_CHAIN1_STS1 | 0x81F4 | W | 0x000000FF | Power domain power chain 1 status register 1 |
| PMU_PWR_MEM_STS0 | 0x81F8 | W | 0xFFFBF800 | Power domain memory power status register 0 |
| PMU_PWR_MEM_STS1 | 0x81FC | W | 0x00000000 | Power domain memory power status register 1 |
| PMU_BISR_CON0 | 0x8200 | W | 0x00000203 | Memory repair control register 0 |
| PMU_BISR_CON1 | 0x8204 | W | 0x00000000 | Memory repair control register 1 |
| PMU_BISR_CON2 | 0x8208 | W | 0x0000FF80 | Memory repair control register 2 |
| PMU_BISR_CON3 | 0x820C | W | 0x000001FF | Memory repair control register 3 |
| PMU_BISR_CON4 | 0x8210 | W | 0x00000000 | Memory repair control register 4 |
| PMU_BISR_CON5 | 0x8214 | W | 0x00000000 | Memory repair control register 5 |
| PMU_BISR_CON6 | 0x8218 | W | 0x00000000 | Memory repair control register 6 |
| PMU_BISR_CON7 | 0x821C | W | 0x00000000 | Memory repair control register 7 |
| PMU_BISR_CON8 | 0x8220 | W | 0x00000000 | Memory repair control register 8 |
| PMU_BISR_CON9 | 0x8224 | W | 0x00000000 | Memory repair control register 9 |
| PMU_BISR_CON10 | 0x8228 | W | 0x00000000 | Memory repair control register 10 |
| PMU_BISR_CON11 | 0x822C | W | 0x00000000 | Memory repair control register 11 |
| PMU_BISR_CON12 | 0x8230 | W | 0x00000000 | Memory repair control register 12 |
| PMU_BISR_CON13 | 0x8234 | W | 0x00000003 | Memory repair control register 13 |
| PMU_BISR_CON14 | 0x8238 | W | 0xFFFFFFFF | Memory repair control register 14 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PMU_BISR_STS0 | 0x8280 | W | 0x00000000 | Memory repair status register 0 |
| PMU_BISR_STS1 | 0x8284 | W | 0x00000000 | Memory repair status register 1 |
| PMU_BISR_STS2 | 0x8288 | W | 0x00000000 | Memory repair status register 2 |
| PMU_BISR_STS3 | 0x828C | W | 0x00000000 | Memory repair status register 3 |
| PMU_BISR_STS4 | 0x8290 | W | 0x00000000 | Memory repair status register 4 |
| PMU_BISR_STS5 | 0x8294 | W | 0x00000000 | Memory repair status register 5 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

## 7.4.2 Detail Register Description

### PMU_PWR_CON0

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | power_off_io_ena<br>Enable VCCIO enter low power mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | biu_auto_pmu1<br>When perform idle operation, BIU_PMU1 corresponding clock can be opened or gated automatically.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | pmu1_bus_idle_sftena<br>Enable sending idle request to BIU_PMU1 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | pmu1_bus_idle_ena<br>Enable sending idle request to BIU_PMU1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | pmu1_mempwr_gate_sftena<br>Enable power down PD_PMU1's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | pmu1_pwr_gate_sftena<br>Enable power down PD_PMU1 by software.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | pmu1_pwr_gate_ena<br>Enable power down PD_PMU1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | osc_dis_bypass<br>Bypass disable oscillator in power mode 0 procedure. If asserted, the oscillator cannot be disabled by FSM during power mode 0 procedure.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | freq_switch_bypass<br>Bypass frequency switch stability in power mode 0 procedure. If asserted, clk_pmu cannot be switched to 32KHz clock source during power mode 0 procedure.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | reset_bypass<br>Bypass wake up reset clear stability in power mode 0 procedure. If asserted, the FSM will enter next state not wait for reset counter, and chip will not be reset.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | pmic_bypass<br>Bypass waiting for PMIC stability in power mode 0 procedure. If asserted, the FSM will enter next state not wait until PMIC is stable.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | wakeup_bypass<br>Bypass waiting for wake up interrupt in power mode 0 procedure. If asserted, the FSM will exit sleep state without waiting for wake up source.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | pmu1_bus_bypass<br>Bypass BIU_PMU1 idle flow in power mode 0 procedure.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | pmu1_pwr_bypass<br>Bypass PD_PMU1 power gating flow in power mode 0 procedure. If asserted, PD_PMU1 is not power down or power up during power mode 0 procedure.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | R/WSC | 0x0 | powermode0_en<br>Power mode 0 enable. When controller enters power mode 0 procedure, this bit is automatically cleared.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_WAKEUP_INT_CON_P0**

Address: Operational Base + offset (0x0008)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | wakeup_int_en<br>Enable GPIO interrupt as wake up source to exit power mode 0 procedure.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_WAKEUP_INT_STS_P0**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RO | 0x0 | wakeup_int_st<br>Power mode 0 wake up source status.<br>1'b0: Inactive<br>1'b1: Active |

**PMU_PMIC_STABLE_CNT_P0**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfffff | pmic_stable_cnt<br>PMIC stable count for power mode 0 procedure. Number of clk_pmu used by counter logic. |

**PMU_WAKEUP_RST_CLR_CNT_P0**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfffff | wakeup_rst_clr_cnt<br>Wake up reset clear count for power mode 0 procedure. Number of clk_pmu used by counter logic. |

**PMU_OSC_STABLE_CNT_P0**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfffff | osc_stable_cnt<br>Oscillator stable count for power mode 0 procedure. Number of clk_pmu used by counter logic. |

**PMU_PMU1_PWR_CHAIN_STABLE_CON**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13:9 | RW | 0x1f | pmu1_pwr_dwn_stable_cnt<br>Stable count for PD_PMU1 power down flow. Number of clk_pmu used by counter logic. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | pmu1_pwr_dwn_stable_en<br>Enable stable counter between power chains for PD_PMU1 power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 7:6 | RO | 0x0 | reserved |
| 5:1 | RW | 0x1f | pmu1_pwr_up_stable_cnt<br>Stable count for PD_PMU1 power up flow. Number of clk_pmu used by counter logic. |
| 0 | RW | 0x1 | pmu1_pwr_up_stable_en<br>Enable stable counter between power chains for PD_PMU1 power up flow.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_DDR_RET_CON0_P0**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | ddrio_rstiov_exit_ena<br>Enable DDR exits retention mode through RST_IOV by hardware in power mode 0 procedure.<br>Bit[12] used for DDR channel 0.<br>Bit[13] used for DDR channel 1.<br>Bit[14] used for DDR channel 2.<br>Bit[15] used for DDR channel 3.<br>1'b0: Disable<br>1'b1: Enable |
| 11:8 | RW | 0x0 | ddrio_reton_exit_ena<br>Enable DDR exits retention mode through RETON/RETOFF by hardware in power mode 0 procedure.<br>Bit[8] used for DDR channel 0.<br>Bit[9] used for DDR channel 1.<br>Bit[10] used for DDR channel 2.<br>Bit[11] used for DDR channel 3.<br>1'b0: Disable<br>1'b1: Enable |
| 7:4 | RW | 0x0 | ddrio_rstiov_enter_ena<br>Enable DDR enters retention mode through RST_IOV by hardware in power mode 0 procedure.<br>Bit[4] used for DDR channel 0.<br>Bit[5] used for DDR channel 1.<br>Bit[6] used for DDR channel 2.<br>Bit[7] used for DDR channel 3.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RW | 0x0 | ddrio_reton_enter_ena<br>Enable DDR enters retention mode through RETON/RETOFF by hardware in power mode 0 procedure.<br>Bit[0] used for DDR channel 0.<br>Bit[1] used for DDR channel 1.<br>Bit[2] used for DDR channel 2.<br>Bit[3] used for DDR channel 3.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_DDR_RET_CON1_P0**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | ddrio_rstiov_exit_sftena<br>Enable DDR exits retention mode through RST_IOV by software.<br>Bit[12] used for DDR channel 0.<br>Bit[13] used for DDR channel 1.<br>Bit[14] used for DDR channel 2.<br>Bit[15] used for DDR channel 3.<br>1'b0: Disable<br>1'b1: Enable |
| 11:8 | RW | 0x0 | ddrio_reton_exit_sftena<br>Enable DDR exits retention mode through RETON/RETOFF by software.<br>Bit[8] used for DDR channel 0.<br>Bit[9] used for DDR channel 1.<br>Bit[10] used for DDR channel 2.<br>Bit[11] used for DDR channel 3.<br>1'b0: Disable<br>1'b1: Enable |
| 7:4 | RW | 0x0 | ddrio_rstiov_enter_sftena<br>Enable DDR enters retention mode through RST_IOV by software.<br>Bit[4] used for DDR channel 0.<br>Bit[5] used for DDR channel 1.<br>Bit[6] used for DDR channel 2.<br>Bit[7] used for DDR channel 3.<br>1'b0: Disable<br>1'b1: Enable |
| 3:0 | RW | 0x0 | ddrio_reton_enter_sftena<br>Enable DDR enters retention mode through RETON/RETOFF by software.<br>Bit[0] used for DDR channel 0.<br>Bit[1] used for DDR channel 1.<br>Bit[2] used for DDR channel 2.<br>Bit[3] used for DDR channel 3.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_INFO_TX_CON**

Address: Operational Base + offset (0x0030)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | info_tx_en<br>Enable PMU debug information transition.<br>1'b0: Disable<br>1'b1: Enable |
| 7:0 | RW | 0x00 | info_tx_intv_time<br>The interval time between the bytes of PMU debug information. |

**PMU_VERSION**

Address: Operational Base + offset (0x4000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00003588 | version<br>PMU version |

**PMU_PWR_CON1**

Address: Operational Base + offset (0x4004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | wfi_bypass<br>Bypass WFI in power mode 1 procedure.<br>If asserted, PMU FSM does not need to wait for CPU standbywfi state before entering low power flow.<br>1'b0: Disable<br>1'b1: Enable |
| 11:9 | RW | 0x0 | core_bypass<br>Bypass core low power flow in power mode 1 procedure.<br>Bit[9] used to bypass BIGCORE0 low power flow.<br>Bit[10] used to bypass BIGCORE1 low power flow.<br>Bit[11] used to bypass LITDSU low power flow.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | qch_bypass<br>Bypass power Q-Channel low power flow in power mode 1 procedure.<br>If asserted, PMU_QCHANNEL_PWR_CON cannot take effect for power Q-Channel low power flow. If you want to execute power Q-Channel low power flow, you can program PMU_QCHANNEL_PWR_SFTCON through software flow.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x0 | cru_bypass<br>Bypass clock and reset low power flow in power mode 1 procedure.<br>If asserted, PMU_CRU_PWR_CON cannot take effect for clock and reset low power flow. If you want to execute clock and reset low power flow, you can program PMU_CRU_PWR_SFTCON through software flow.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | pwrgate_bypass<br>Bypass power gating flow in power mode 1 procedure.<br>If asserted, PMU_PWR_GATE_CON0/1/2 cannot take effect for power gating flow. If you want to execute power gating flow, you can program PMU_PWR_GATE_SFTCON0/1/2 through software flow.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | ddr_bypass<br>Bypass DDR low power flow in power mode 1 procedure.<br>If asserted, PMU_DDR_CH0/1/2/3_PWR_CON cannot take effect for DDR low power flow. If you want to execute DDR low power flow, you can program PMU_DDR_CH0/1/2/3_PWR_SFTCON through software flow.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | bus_bypass<br>Bypass BIU idle request in power mode 1 procedure.<br>If asserted, PMU_BIU_IDLE_CON0/1/2 cannot take effect for BIU idle request. If you want to execute BIU idle request, you can program PMU_BIU_IDLE_SFTCON0/1/2 through software flow.<br>1'b0: Disable<br>1'b1: Enable |
| 3:2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | dsu_bypass<br>Bypass DSU low power flow in power mode 1 procedure.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | R/WSC | 0x0 | powermode1_en<br>Power mode 1 enable. When controller enters power mode 1 procedure. It is automatically cleared after PMU enters power mode 1 procedure.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_GLB_POWER_STS**

Address: Operational Base + offset (0x4008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RO | 0x0 | power_state<br>PMU1 global power state.<br>4'h0: Normal state<br>4'h1: Core low power state<br>4'h2: Cluster low power state<br>4'h3: Q-Channel low power state<br>4'h4: Bus low power state<br>4'h5: DDR low power state<br>4'h6: Power gating low power state<br>4'h7: Clock and reset low power state<br>4'h8: Sleep state<br>4'h9: Clock and reset active state<br>4'ha: Power gating active state<br>4'hb: DDR active state<br>4'hc: Bus active state<br>4'hd: Q-Channel active state<br>4'hd: Cluster active state<br>4'hf: Core active state |

**PMU_INT_MASK_CON**

Address: Operational Base + offset (0x400C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | R/WSC | 0x0 | glb_int_mask<br>Global interrupt mask during DSU sleep state.<br>1'b0: Interrupt is not mask<br>1'b1: Interrupt is mask |

**PMU_WAKEUP_INT_CON**

Address: Operational Base + offset (0x4010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16 | RW | 0x0 | wakeup_timeout_en<br>Enable PMU wake up timeout as wake up source to exit power mode 1 procedure.<br>1'b0: Disable<br>1'b1: Enable |
| 15 | RW | 0x0 | wakeup_sys_int_en<br>Enable system interrupt as wake up source to exit power mode 1 procedure.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | wakeup_timer_int_en<br>Enable PMU_TIMER interrupt as wake up source to exit power mode 1 procedure.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | wakeup_vad_int_en<br>Enable VAD interrupt as wake up source to exit power mode 1 procedure.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | wakeup_uart0_int_en<br>Enable UART0 interrupt as wake up source to exit power mode 1 procedure.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | wakeup_usb_int_en<br>Enable USB detect interrupt as wake up source to exit power mode 1 procedure.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | wakeup_sdio_int_en<br>Enable SDIO interrupt as wake up source to exit power mode 1 procedure.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | wakeup_sdmmc_int_en<br>Enable SDMMC detect interrupt as wake up source to exit power mode 1 procedure.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | wakeup_gpio0_int_en<br>Enable GPIO0 interrupt as wake up source to exit power mode 1 procedure.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | wakeup_cpu7_int_en<br>Enable CPU7 interrupt as wake up source to exit power mode 1 procedure.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | wakeup_cpu6_int_en<br>Enable CPU6 interrupt as wake up source to exit power mode 1 procedure.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | wakeup_cpu5_int_en<br>Enable CPU5 interrupt as wake up source to exit power mode 1 procedure.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | wakeup_cpu4_int_en<br>Enable CPU4 interrupt as wake up source to exit power mode 1 procedure.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | wakeup_cpu3_int_en<br>Enable CPU3 interrupt as wake up source to exit power mode 1 procedure.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | wakeup_cpu2_int_en<br>Enable CPU2 interrupt as wake up source to exit power mode 1 procedure.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | wakeup_cpu1_int_en<br>Enable CPU1 interrupt as wake up source to exit power mode 1 procedure.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | wakeup_cpu0_int_en<br>Enable CPU0 interrupt as wake up source to exit power mode 1 procedure.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_WAKEUP_INT_STS**

Address: Operational Base + offset (0x4014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16 | RO | 0x0 | wakeup_timeout_st<br>Wake up timeout as wake up source status.<br>1'b0: Inactive<br>1'b1: Active |
| 15 | RO | 0x0 | wakeup_sys_int_st<br>System interrupt as wake up source status.<br>1'b0: Inactive<br>1'b1: Active |
| 14 | RO | 0x0 | wakeup_timer_int_st<br>PMU_TIMER interrupt as wake up source status.<br>1'b0: Inactive<br>1'b1: Active |
| 13 | RO | 0x0 | wakeup_vad_int_st<br>VAD interrupt as wake up source status.<br>1'b0: Inactive<br>1'b1: Active |
| 12 | RO | 0x0 | wakeup_uart0_int_st<br>UART0 interrupt as wake up source status.<br>1'b0: Inactive<br>1'b1: Active |
| 11 | RO | 0x0 | wakeup_usb_int_st<br>USB detect interrupt as wake up source status.<br>1'b0: Inactive<br>1'b1: Active |
| 10 | RO | 0x0 | wakeup_sdio_int_st<br>SDIO interrupt as wake up source status.<br>1'b0: Inactive<br>1'b1: Active |
| 9 | RO | 0x0 | wakeup_sdmmc_int_st<br>SDMMC detect interrupt as wake up source status.<br>1'b0: Inactive<br>1'b1: Active |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RO | 0x0 | wakeup_gpio0_int_st<br>GPIO0 interrupt as wake up source status.<br>1'b0: Inactive<br>1'b1: Active |
| 7 | RO | 0x0 | wakeup_cpu7_int_st<br>CPU7 interrupt as wake up source status.<br>1'b0: Inactive<br>1'b1: Active |
| 6 | RO | 0x0 | wakeup_cpu6_int_st<br>CPU6 interrupt as wake up source status.<br>1'b0: Inactive<br>1'b1: Active |
| 5 | RO | 0x0 | wakeup_cpu5_int_st<br>CPU5 interrupt as wake up source status.<br>1'b0: Inactive<br>1'b1: Active |
| 4 | RO | 0x0 | wakeup_cpu4_int_st<br>CPU4 interrupt as wake up source status.<br>1'b0: Inactive<br>1'b1: Active |
| 3 | RO | 0x0 | wakeup_cpu3_int_st<br>CPU3 interrupt as wake up source status.<br>1'b0: Inactive<br>1'b1: Active |
| 2 | RO | 0x0 | wakeup_cpu2_int_st<br>CPU2 interrupt as wake up source status.<br>1'b0: Inactive<br>1'b1: Active |
| 1 | RO | 0x0 | wakeup_cpu1_int_st<br>CPU1 interrupt as wake up source status.<br>1'b0: Inactive<br>1'b1: Active |
| 0 | RO | 0x0 | wakeup_cpu0_int_st<br>CPU0 interrupt as wake up source status.<br>1'b0: Inactive<br>1'b1: Active |

**PMU_DDR_CH0_PWR_CON**

Address: Operational Base + offset (0x4020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | ddrphy_auto_gating_ena<br>Enable DDRPHY auto clock gating. DDRPHY's clock can be gated when in sleep mode.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | ddrctl_c_auto_gating_ena<br>Enable DDRCTRL's core-clock auto clock gating. Core-clock can be gated when in self-refresh mode.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | ddrctl_a_auto_gating_ena<br>Enable DDRCTRL's AXI-clock auto clock gating. AXI-clock can be gated when in self-refresh mode.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | ddrio_rstiov_exit_ena<br>Enable DDR exits retention mode through RST_IOV by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | ddrio_rstiov_enter_ena<br>Enable DDR enters retention mode through RST_IOV by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | ddrio_reton_exit_ena<br>Enable DDR exits retention mode through RETON/RETOFF by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 4:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | ddrio_reton_enter_ena<br>Enable DDR enters retention mode through RETON/RETOFF by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | ddr_sref_a_ena<br>Enable DDR self-refresh mode for AXI-clock domain by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | ddr_sref_c_ena<br>Enable DDR self-refresh mode for core-clock domain by hardware.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_DDR_CH1_PWR_CON**

Address: Operational Base + offset (0x4024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | ddrphy_auto_gating_ena<br>Enable DDRPHY auto clock gating. DDRPHY's clock can be gated when in sleep mode.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | ddrctl_c_auto_gating_ena<br>Enable DDRCTRL's core-clock auto clock gating. Core-clock can be gated when in self-refresh mode.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | ddrctl_a_auto_gating_ena<br>Enable DDRCTRL's AXI-clock auto clock gating. AXI-clock can be gated when in self-refresh mode.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | ddrio_rstiov_exit_ena<br>Enable DDR exits retention mode through RST_IOV by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | ddrio_rstiov_enter_ena<br>Enable DDR enters retention mode through RST_IOV by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | ddrio_reton_exit_ena<br>Enable DDR exits retention mode through RETON/RETOFF by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 4:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | ddrio_reton_enter_ena<br>Enable DDR enters retention mode through RETON/RETOFF by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | ddr_sref_a_ena<br>Enable DDR self-refresh mode for AXI-clock domain by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | ddr_sref_c_ena<br>Enable DDR self-refresh mode for core-clock domain by hardware.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_DDR_CH2_PWR_CON**

Address: Operational Base + offset (0x4028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | ddrphy_auto_gating_ena<br>Enable DDRPHY auto clock gating. DDRPHY's clock can be gated when in sleep mode.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | ddrctl_c_auto_gating_ena<br>Enable DDRCTRL's core-clock auto clock gating. Core-clock can be gated when in self-refresh mode.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | ddrctl_a_auto_gating_ena<br>Enable DDRCTRL's AXI-clock auto clock gating. AXI-clock can be gated when in self-refresh mode.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | ddrio_rstiov_exit_ena<br>Enable DDR exits retention mode through RST_IOV by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | ddrio_rstiov_enter_ena<br>Enable DDR enters retention mode through RST_IOV by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | ddrio_reton_exit_ena<br>Enable DDR exits retention mode through RETON/RETOFF by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 4:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | ddrio_reton_enter_ena<br>Enable DDR enters retention mode through RETON/RETOFF by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | ddr_sref_a_ena<br>Enable DDR self-refresh mode for AXI-clock domain by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | ddr_sref_c_ena<br>Enable DDR self-refresh mode for core-clock domain by hardware.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_DDR_CH3_PWR_CON**

Address: Operational Base + offset (0x402C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | ddrphy_auto_gating_ena<br>Enable DDRPHY auto clock gating. DDRPHY's clock can be gated when in sleep mode.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | ddrctl_c_auto_gating_ena<br>Enable DDRCTRL's core-clock auto clock gating. Core-clock can be gated when in self-refresh mode.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | ddrctl_a_auto_gating_ena<br>Enable DDRCTRL's AXI-clock auto clock gating. AXI-clock can be gated when in self-refresh mode.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | ddrio_rstiov_exit_ena<br>Enable DDR exits retention mode through RST_IOV by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | ddrio_rstiov_enter_ena<br>Enable DDR enters retention mode through RST_IOV by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | ddrio_reton_exit_ena<br>Enable DDR exits retention mode through RETON/RETOFF by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 4:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | ddrio_reton_enter_ena<br>Enable DDR enters retention mode through RETON/RETOFF by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | ddr_sref_a_ena<br>Enable DDR self-refresh mode for AXI-clock domain by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | ddr_sref_c_ena<br>Enable DDR self-refresh mode for core-clock domain by hardware.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_DDR_CH0_PWR_SFTCON**

Address: Operational Base + offset (0x4030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | ddrctl_c_active_wait_enter<br>1'b0: Not need to wait for ddrctl_c_active low before FSM enter self-refresh state<br>1'b1: Need to wait for ddrctl_c_active low before FSM enter self-refresh state |
| 10 | RW | 0x0 | ddrctl_a_active_wait_exit<br>1'b0: Not need to wait for ddrctl_a_active high before FSM exit self-refresh state<br>1'b1: Need to wait for ddrctl_a_active high before FSM exit self-refresh state |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RW | 0x0 | ddrctl_c_active_wait_exit<br>1'b0: Not need to wait for ddrctl_c_active high before FSM exit self-refresh state<br>1'b1: Need to wait for ddrctl_c_active high before FSM exit self-refresh state |
| 8 | RW | 0x0 | ddrctl_a_active_wait_enter<br>1'b0: Not need to wait for ddrctl_a_active low before FSM enter self-refresh state<br>1'b1: Need to wait for ddrctl_a_active low before FSM enter self-refresh state |
| 7 | R/WSC | 0x0 | ddrio_rstiov_exit_sftena<br>Enable DDR exits retention mode through RST_IOV by software. It is auto cleared after DDR exits retention mode.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | ddrio_rstiov_enter_sftena<br>Enable DDR enters retention mode through RST_IOV by software.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | R/WSC | 0x0 | ddrio_reton_exit_sftena<br>Enable DDR exits retention mode through RETON/RETOFF by software. It is auto cleared after DDR exits retention mode.<br>1'b0: Disable<br>1'b1: Enable |
| 4:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | ddrio_reton_enter_sftena<br>Enable DDR enters retention mode through RETON/RETOFF by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | ddr_sref_a_sftena<br>Enable DDR self-refresh mode for AXI-clock domain by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | ddr_sref_c_sftena<br>Enable DDR self-refresh mode for core-clock domain by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_DDR_CH1_PWR_SFTCON**

Address: Operational Base + offset (0x4034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | ddrctl_c_active_wait_enter<br>1'b0: Not need to wait for ddrctl_c_active low before FSM enter self-refresh state<br>1'b1: Need to wait for ddrctl_c_active low before FSM enter self-refresh state |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10 | RW | 0x0 | ddrctl_a_active_wait_exit<br>1'b0: Not need to wait for ddrctl_a_active high before FSM exit self-refresh state<br>1'b1: Need to wait for ddrctl_a_active high before FSM exit self-refresh state |
| 9 | RW | 0x0 | ddrctl_c_active_wait_exit<br>1'b0: Not need to wait for ddrctl_c_active high before FSM exit self-refresh state<br>1'b1: Need to wait for ddrctl_c_active high before FSM exit self-refresh state |
| 8 | RW | 0x0 | ddrctl_a_active_wait_enter<br>1'b0: Not need to wait for ddrctl_a_active low before FSM enter self-refresh state<br>1'b1: Need to wait for ddrctl_a_active low before FSM enter self-refresh state |
| 7 | R/W SC | 0x0 | ddrio_rstiov_exit_sftena<br>Enable DDR exits retention mode through RST_IOV by software. It is auto cleared after DDR exits retention mode.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | ddrio_rstiov_enter_sftena<br>Enable DDR enters retention mode through RST_IOV by software.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | R/W SC | 0x0 | ddrio_reton_exit_sftena<br>Enable DDR exits retention mode through RETON/RETOFF by software. It is auto cleared after DDR exits retention mode.<br>1'b0: Disable<br>1'b1: Enable |
| 4:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | ddrio_reton_enter_sftena<br>Enable DDR enters retention mode through RETON/RETOFF by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | ddr_sref_a_sftena<br>Enable DDR self-refresh mode for AXI-clock domain by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | ddr_sref_c_sftena<br>Enable DDR self-refresh mode for core-clock domain by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_DDR_CH2_PWR_SFTCON**

Address: Operational Base + offset (0x4038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11 | RW | 0x0 | ddrctl_c_active_wait_enter<br>1'b0: Not need to wait for ddrctl_c_active low before FSM enter self-refresh state<br>1'b1: Need to wait for ddrctl_c_active low before FSM enter self-refresh state |
| 10 | RW | 0x0 | ddrctl_a_active_wait_exit<br>1'b0: Not need to wait for ddrctl_a_active high before FSM exit self-refresh state<br>1'b1: Need to wait for ddrctl_a_active high before FSM exit self-refresh state |
| 9 | RW | 0x0 | ddrctl_c_active_wait_exit<br>1'b0: Not need to wait for ddrctl_c_active high before FSM exit self-refresh state<br>1'b1: Need to wait for ddrctl_c_active high before FSM exit self-refresh state |
| 8 | RW | 0x0 | ddrctl_a_active_wait_enter<br>1'b0: Not need to wait for ddrctl_a_active low before FSM enter self-refresh state<br>1'b1: Need to wait for ddrctl_a_active low before FSM enter self-refresh state |
| 7 | R/WSC | 0x0 | ddrio_rstiov_exit_sftena<br>Enable DDR exits retention mode through RST_IOV by software. It is auto cleared after DDR exits retention mode.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | ddrio_rstiov_enter_sftena<br>Enable DDR enters retention mode through RST_IOV by software.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | R/WSC | 0x0 | ddrio_reton_exit_sftena<br>Enable DDR exits retention mode through RETON/RETOFF by software. It is auto cleared after DDR exits retention mode.<br>1'b0: Disable<br>1'b1: Enable |
| 4:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | ddrio_reton_enter_sftena<br>Enable DDR enters retention mode through RETON/RETOFF by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | ddr_sref_a_sftena<br>Enable DDR self-refresh mode for AXI-clock domain by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | ddr_sref_c_sftena<br>Enable DDR self-refresh mode for core-clock domain by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_DDR_CH3_PWR_SFTCON**

Address: Operational Base + offset (0x403C)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | ddrctl_c_active_wait_enter<br>1'b0: Not need to wait for ddrctl_c_active low before FSM enter self-refresh state<br>1'b1: Need to wait for ddrctl_c_active low before FSM enter self-refresh state |
| 10 | RW | 0x0 | ddrctl_a_active_wait_exit<br>1'b0: Not need to wait for ddrctl_a_active high before FSM exit self-refresh state<br>1'b1: Need to wait for ddrctl_a_active high before FSM exit self-refresh state |
| 9 | RW | 0x0 | ddrctl_c_active_wait_exit<br>1'b0: Not need to wait for ddrctl_c_active high before FSM exit self-refresh state<br>1'b1: Need to wait for ddrctl_c_active high before FSM exit self-refresh state |
| 8 | RW | 0x0 | ddrctl_a_active_wait_enter<br>1'b0: Not need to wait for ddrctl_a_active low before FSM enter self-refresh state<br>1'b1: Need to wait for ddrctl_a_active low before FSM enter self-refresh state |
| 7 | R/WSC | 0x0 | ddrio_rstiov_exit_sftena<br>Enable DDR exits retention mode through RST_IOV by software. It is auto cleared after DDR exits retention mode.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | ddrio_rstiov_enter_sftena<br>Enable DDR enters retention mode through RST_IOV by software.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | R/WSC | 0x0 | ddrio_reton_exit_sftena<br>Enable DDR exits retention mode through RETON/RETOFF by software. It is auto cleared after DDR exits retention mode.<br>1'b0: Disable<br>1'b1: Enable |
| 4:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | ddrio_reton_enter_sftena<br>Enable DDR enters retention mode through RETON/RETOFF by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | ddr_sref_a_sftena<br>Enable DDR self-refresh mode for AXI-clock domain by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | ddr_sref_c_sftena<br>Enable DDR self-refresh mode for core-clock domain by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_DDR_POWER_STS**

Rockchip Confidential

Address: Operational Base + offset (0x4040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3:0 | RO | 0x0 | ddr_power_state<br>DDR power state.<br>4'h0: Normal state<br>4'h1: Enter self-refresh mode for AXI-clock state<br>4'h2: Enter self-refresh mode core-clock state<br>4'h3: Enter retention mode through RETON/RETOFF state<br>4'h4: Enter retention mode through RST_IOV state<br>4'h5: Sleep state<br>4'h6: Exit retention mode through RST_IOV state<br>4'h7: Exit retention mode through RETON/RETOFF state<br>4'h8: Exit self-refresh mode for core-clock state<br>4'h9: Exit self-refresh mode for AXI-clock state<br>Others: Reserved |

**PMU_DDR_STS**

Address: Operational Base + offset (0x4044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29 | RO | 0x0 | ddr_ch3_io_rstiov<br>DDR RST_IOV state for channel 3.<br>1'b0: Inactive<br>1'b1: Active |
| 28 | RO | 0x0 | ddrctrl_ch3_a_sysactive<br>DDRC AXI clock active for channel 3.<br>1'b0: Inactive<br>1'b1: Active |
| 27 | RO | 0x0 | ddrctrl_ch3_a_sysack<br>DDRC AXI hardware low-power request acknowledge for channel 3.<br>1'b0: Inactive<br>1'b1: Active |
| 26 | RO | 0x0 | ddr_ch3_io_reton<br>DDR RETON/RETOFF state for channel 3.<br>1'b0: Inactive<br>1'b1: Active |
| 25 | RO | 0x0 | ddrctrl_ch3_c_sysactive<br>DDRC hardware low-power clock active for channel 3.<br>1'b0: Inactive<br>1'b1: Active |
| 24 | RO | 0x0 | ddrctrl_ch3_c_sysack<br>DDRC hardware low-power request acknowledge for channel 3.<br>1'b0: Inactive<br>1'b1: Active |
| 23:22 | RO | 0x0 | reserved |
| 21 | RO | 0x0 | ddr_ch2_io_rstiov<br>DDR RST_IOV state for channel 2.<br>1'b0: Inactive<br>1'b1: Active |
| 20 | RO | 0x0 | ddrctrl_ch2_a_sysactive<br>DDRC AXI clock active for channel 2.<br>1'b0: Inactive<br>1'b1: Active |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19 | RO | 0x0 | ddrctrl_ch2_a_sysack<br>DDRC AXI hardware low-power request acknowledge for channel 2.<br>1'b0: Inactive<br>1'b1: Active |
| 18 | RO | 0x0 | ddr_ch2_io_reton<br>DDR RETON/RETOFF state for channel 2.<br>1'b0: Inactive<br>1'b1: Active |
| 17 | RO | 0x0 | ddrctrl_ch2_c_sysactive<br>DDRC hardware low-power clock active for channel 2.<br>1'b0: Inactive<br>1'b1: Active |
| 16 | RO | 0x0 | ddrctrl_ch2_c_sysack<br>DDRC hardware low-power request acknowledge for channel 2.<br>1'b0: Inactive<br>1'b1: Active |
| 15:14 | RO | 0x0 | reserved |
| 13 | RO | 0x0 | ddr_ch1_io_rstiov<br>DDR RST_IOV state for channel 1.<br>1'b0: Inactive<br>1'b1: Active |
| 12 | RO | 0x0 | ddrctrl_ch1_a_sysactive<br>DDRC AXI clock active for channel 1.<br>1'b0: Inactive<br>1'b1: Active |
| 11 | RO | 0x0 | ddrctrl_ch1_a_sysack<br>DDRC AXI hardware low-power request acknowledge for channel 1.<br>1'b0: Inactive<br>1'b1: Active |
| 10 | RO | 0x0 | ddr_ch1_io_reton<br>DDR RETON/RETOFF state for channel 1.<br>1'b0: Inactive<br>1'b1: Active |
| 9 | RO | 0x0 | ddrctrl_ch1_c_sysactive<br>DDRC hardware low-power clock active for channel 1.<br>1'b0: Inactive<br>1'b1: Active |
| 8 | RO | 0x0 | ddrctrl_ch1_c_sysack<br>DDRC hardware low-power request acknowledge for channel 1.<br>1'b0: Inactive<br>1'b1: Active |
| 7:6 | RO | 0x0 | reserved |
| 5 | RO | 0x0 | ddr_ch0_io_rstiov<br>DDR RST_IOV state for channel 0.<br>1'b0: Inactive<br>1'b1: Active |
| 4 | RO | 0x0 | ddrctrl_ch0_a_sysactive<br>DDRC AXI clock active for channel 0.<br>1'b0: Inactive<br>1'b1: Active |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RO | 0x0 | ddrctrl_ch0_a_sysack<br>DDRC AXI hardware low-power request acknowledge for channel 0.<br>1'b0: Inactive<br>1'b1: Active |
| 2 | RO | 0x0 | ddr_ch0_io_reton<br>DDR RETON/RETOFF state for channel 0.<br>1'b0: Inactive<br>1'b1: Active |
| 1 | RO | 0x0 | ddrctrl_ch0_c_sysactive<br>DDRC hardware low-power clock active for channel 0.<br>1'b0: Inactive<br>1'b1: Active |
| 0 | RO | 0x0 | ddrctrl_ch0_c_sysack<br>DDRC hardware low-power request acknowledge for channel 0.<br>1'b0: Inactive<br>1'b1: Active |

**PMU_CRU_PWR_CON**

Address: Operational Base + offset (0x4050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | power_off_io_ena<br>Enable VCCIO enter low power mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | pd_bus_clk_src_gate_ena<br>Gating BIU_BUS's clock source during clock low power mode.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | pwm_switch_iout<br>PWM output.<br>1'b0: Disable<br>1'b1: Enable<br>It is set 0 for RK3588. |
| 7 | RW | 0x0 | pwm_gpio_ioe_ena<br>PWM output enable.<br>1'b0: Disable<br>1'b1: Enable<br>It is set 0 for RK3588. |
| 6 | RW | 0x0 | pwm_switch_ena<br>PWM switch enable.<br>1'b0: Disable<br>1'b1: Enable<br>It is set 0 for RK3588. |
| 5 | RW | 0x0 | power_off_ena<br>Enable chip power off by hardware.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | alive_osc_ena<br>Enable clk_pmu/hclk_pmu/pclk_pmu switch to oscillator by hardware. When alive_32k_ena is asserted, this bit is ignored.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | input_clamp_ena<br>Enable VD_PMU input clamped by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | wakeup_rst_ena<br>Enable wake up reset by hardware.<br>If asserted, all registers without reset hold will be reset after chip wake up.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | osc_dis_ena<br>Disable oscillator by hardware.<br>1'b0: Enable<br>1'b1: Disable |
| 0 | RW | 0x0 | alive_32k_ena<br>Enable pclk_pmu and clk_pmu switch to 32KHz clock by hardware.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CRU_PWR_SFTCON**

Address: Operational Base + offset (0x4054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x0 | power_off_io_sftena<br>Enable VCCIO enter low power mode by software.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | power_off_sftena<br>Enable chip power off by software.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | alive_osc_sftena<br>Enable clk_pmu/hclk_pmu/pclk_pmu switch to oscillator by software. When alive_32k_ena is asserted, this bit is ignored.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | input_clamp_sftena<br>Enable VD_PMU input clamp by software.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | wakeup_rst_sftena<br>Enable wake up reset by software. If asserted, all digital except IP with reset hold will be reset.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | osc_dis_sftena<br>Disable oscillator by software.<br>1'b0: Enable<br>1'b1: Disable |
| 0 | RW | 0x0 | alive_32k_sftena<br>Enable pclk_pmu and clk_pmu switch to 32KHz clock by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CRU_POWER_STS**

Address: Operational Base + offset (0x4058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3:0 | RO | 0x0 | cru_power_state<br>Clock and reset power state.<br>4'h0: Normal state<br>4'h1: Clock low frequency state<br>4'h2: PLL power down state<br>4'h3: Input clamp state<br>4'h4: Oscillator disable state<br>4'h5: Sleep state<br>4'h6: Wake up state<br>4'h7: Input clamp release state<br>4'h8: Oscillator enable state<br>4'h9: Clock high frequency state<br>4'ha: Wake up reset clear state<br>4'hc: PLL power up state<br>Others: Reserved |

**PMU_PLLPD_CON0**

Address: Operational Base + offset (0x4060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | npll_pd_ena<br>Enable power down NPLL by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | cpll_pd_ena<br>Enable power down CPLL by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | gpll_pd_ena<br>Enable power down GPLL by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | aupll_pd_ena<br>Enable power down AUPLL by hardware.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11 | RW | 0x0 | v0pll_pd_ena<br>Enable power down V0PLL by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | d3bpll_pd_ena<br>Enable power down D3BPLL by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | d3apll_pd_ena<br>Enable power down D3APLL by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | d2bpll_pd_ena<br>Enable power down D2BPLL by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | d2apll_pd_ena<br>Enable power down D2APLL by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | d1bpll_pd_ena<br>Enable power down D1BPLL by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | d1apll_pd_ena<br>Enable power down D1APLL by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | d0bpll_pd_ena<br>Enable power down D0BPLL by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | d0apll_pd_ena<br>Enable power down D0APLL by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | lpll_pd_ena<br>Enable power down LPLL by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | b1pll_pd_ena<br>Enable power down B1PLL by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | b0pll_pd_ena<br>Enable power down B0PLL by hardware.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_PLLPD_CON1**

Address: Operational Base + offset (0x4064)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | spll_pd_ena<br>Enable power down SPLL by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | ppll_pd_ena<br>Enable power down PPLL by hardware.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_PLLPD_SFTCON0**

Address: Operational Base + offset (0x4068)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | npll_pd_sftena<br>Enable power down NPLL by software.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | cpll_pd_sftena<br>Enable power down CPLL by software.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | gpll_pd_sftena<br>Enable power down GPLL by software.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | aupll_pd_sftena<br>Enable power down AUPLL by software.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | v0pll_pd_sftena<br>Enable power down V0PLL by software.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | d3bpll_pd_sftena<br>Enable power down D3BPLL by software.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | d3apll_pd_sftena<br>Enable power down D3APLL by software.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | d2bpll_pd_sftena<br>Enable power down D2BPLL by software.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x0 | d2apll_pd_sftena<br>Enable power down D2APLL by software.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | d1bpll_pd_sftena<br>Enable power down D1BPLL by software.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | d1apll_pd_sftena<br>Enable power down D1APLL by software.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | d0bpll_pd_sftena<br>Enable power down D0BPLL by software.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | d0apll_pd_sftena<br>Enable power down D0APLL by software.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | lpll_pd_sftena<br>Enable power down LPLL by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | b1pll_pd_sftena<br>Enable power down B1PLL by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | b0pll_pd_sftena<br>Enable power down B0PLL by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_PLLPD_SFTCON1**

Address: Operational Base + offset (0x406C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | spll_pd_sftena<br>Enable power down SPLL by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | ppll_pd_sftena<br>Enable power down PPLL by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_PMIC_STABLE_CNT**

Address: Operational Base + offset (0x4080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19:0 | RW | 0xfffff | pmic_stable_cnt<br>PMIC stable count for mode 1 procedure. Number of clk_pmu used by counter logic. |

**PMU_OSC_STABLE_CNT**

Address: Operational Base + offset (0x4084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfffff | osc_stable_cnt<br>Oscillator stable count for mode 1 procedure. Number of clk_pmu used by counter logic. |

**PMU_WAKEUP_RST_CLR_CNT**

Address: Operational Base + offset (0x4088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfffff | wakeup_rst_clr_cnt<br>Wake up reset clear count for mode 1 procedure. Number of clk_pmu used by counter logic. |

**PMU_PLL_LOCK_CNT**

Address: Operational Base + offset (0x408C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfffff | pll_lock_cnt<br>Count for PLL from power up to lock. Number of clk_pmu used by counter logic. |

**PMU_WAKEUP_TIMEOUT_CNT**

Address: Operational Base + offset (0x4094)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x05dc0 | wakeup_timeout_cnt<br>Wake up timeout count. Number of clk_pmu used by counter logic. |

**PMU_PWM_SWITCH_CNT**

Address: Operational Base + offset (0x4098)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfffff | pwm_switch_cnt<br>PWM switch count. Number of clk_pmu used by counter logic. |

**PMU_SYS_REG0**

Address: Operational Base + offset (0x4100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sys_reg<br>System register. It cannot be reset by software. |

**PMU_SYS_REG1**

Address: Operational Base + offset (0x4104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sys_reg<br>System register. It cannot be reset by software. |

Rockchip Confidential

**PMU_SYS_REG2**

Address: Operational Base + offset (0x4108)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sys_reg<br>System register. It cannot be reset by software. |

**PMU_SYS_REG3**

Address: Operational Base + offset (0x410C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sys_reg<br>System register. It cannot be reset by software. |

**PMU_SYS_REG4**

Address: Operational Base + offset (0x4110)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sys_reg<br>System register. It cannot be reset by software. |

**PMU_SYS_REG5**

Address: Operational Base + offset (0x4114)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sys_reg<br>System register. It cannot be reset by software. |

**PMU_SYS_REG6**

Address: Operational Base + offset (0x4118)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sys_reg<br>System register. It cannot be reset by software. |

**PMU_SYS_REG7**

Address: Operational Base + offset (0x411C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sys_reg<br>System register. It cannot be reset by software. |

**PMU_PWR_CON2**

Address: Operational Base + offset (0x8000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | cpu7_lp_bypass<br>Bypass CPU7 low power flow.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | cpu6_lp_bypass<br>Bypass CPU6 low power flow.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | cpu5_lp_bypass<br>Bypass CPU5 low power flow.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | cpu4_lp_bypass<br>Bypass CPU4 low power flow.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | cpu3_lp_bypass<br>Bypass CPU3 low power flow.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | cpu2_lp_bypass<br>Bypass CPU2 low power flow.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | cpu1_lp_bypass<br>Bypass CPU1 low power flow.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | cpu0_lp_bypass<br>Bypass CPU0 low power flow.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_DSU_PWR_CON**

Address: Operational Base + offset (0x8004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | dsu_mem_dwn_ack_clamp_ena<br>Enable clamp for VD_DSU memory power down acknowledge.<br>This bit should be set to 1 if dsu_pwroff_ena=1 and VD_DSU will be power off.<br>1'b0: Disable<br>1'b1: Enable |
| 9:5 | RW | 0x00 | dsu_mem_dwn_ack_bypass<br>Bypass VD_DSU memory power down acknowledge.<br>Bit[5] used to bypass "Snoop filter and LTDB RAMs" memory power down acknowledge.<br>Bit[6] used to bypass "L3 Tag ways 0~3, L3 Data portion 0, and L3 Victim RAMs" memory power down acknowledge.<br>Bit[7] used to bypass "L3 Tag ways 4~7" memory power down acknowledge.<br>Bit[8] used to bypass "L3 Tag ways 8~11, L3 Data portion 1 RAMs" memory power down acknowledge.<br>Bit[9] used to bypass other memory power down acknowledge.<br>If memory is power down before DSU enter power down mode, you should set relative bypass bit high.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | dsu_funcret_ena<br>Enable DSU FUNC_RET mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | dsu_clusterpactive_bit_full_flag<br>CLUSTERPACTIVE bit full flag.<br>If DSU power mode wants to transfer from any mode to FULL ON or FULL FUNC_RET, this bit should be set to 1. Otherwise, this bit should be set to 0. |
| 1 | RW | 0x0 | dsu_pwroff_ena<br>Enable VD_LITDSU power off by hardware.<br>If you just power down VD_LITDSU memory but not power off VD_LITDSU, this bit should be set to 0.<br>If you want to power off VD_LITDSU by hardware, this bit should be set to 1.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | dsu_pwrdn_ena<br>Enable VD_LITDSU power down by hardware.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_DSU_PWR_SFTCON**

Address: Operational Base + offset (0x8008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | dsu_sft_clusterpactive_retsf<br>CLUSTERPACTIVE bit generated by software when requested mode is SFONLY FUNC_RET mode. High active.<br>It is auto cleared when CLUSTERPREQ is active.<br>It is used when DSU power mode transition is controlled by software. |
| 11 | RW | 0x0 | dsu_sft_clusterpactive_ret1p4<br>CLUSTERPACTIVE bit generated by software when requested mode is 1/4 FUNC_RET mode. High active.<br>It is auto cleared when CLUSTERPREQ is active.<br>It is used when DSU power mode transition is controlled by software. |
| 10 | RW | 0x0 | dsu_sft_clusterpactive_ret1p2<br>CLUSTERPACTIVE bit generated by software when requested mode is 1/2 FUNC_RET mode. High active.<br>It is auto cleared when CLUSTERPREQ is active.<br>It is used when DSU power mode transition is controlled by software. |
| 9 | RW | 0x0 | dsu_sft_clusterpactive_ret3p4<br>CLUSTERPACTIVE bit generated by software when requested mode is 3/4 FUNC_RET mode. High active.<br>It is auto cleared when CLUSTERPREQ is active.<br>It is used when DSU power mode transition is controlled by software. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | dsu_sft_clusterpactive_onsf<br>CLUSTERPACTIVE bit generated by software when requested mode is SFONLY ON mode. High active.<br>It is auto cleared when CLUSTERPREQ is active.<br>It is used when DSU power mode transition is controlled by software. |
| 7 | RW | 0x0 | dsu_sft_clusterpactive_on1p4<br>CLUSTERPACTIVE bit generated by software when requested mode is 1/4 ON mode. High active.<br>It is auto cleared when CLUSTERPREQ is active.<br>It is used when DSU power mode transition is controlled by software. |
| 6 | RW | 0x0 | dsu_sft_clusterpactive_on1p2<br>CLUSTERPACTIVE bit generated by software when requested mode is 1/2 ON mode. High active.<br>It is auto cleared when CLUSTERPREQ is active.<br>It is used when DSU power mode transition is controlled by software. |
| 5 | RW | 0x0 | dsu_sft_clusterpactive_on3p4<br>CLUSTERPACTIVE bit generated by software when requested mode is 3/4 ON mode. High active.<br>It is auto cleared when CLUSTERPREQ is active.<br>It is used when DSU power mode transition is controlled by software. |
| 4 | RW | 0x0 | dsu_sft_clusterpactive_funcret<br>CLUSTERPACTIVE bit generated by software when requested mode is FUNC_RET mode. High active.<br>It is auto cleared when CLUSTERPREQ is active.<br>It is used when DSU power mode transition is controlled by software. |
| 3 | RW | 0x0 | dsu_sft_clusterpactive_fullon<br>CLUSTERPACTIVE bit generated by software when requested mode is FULL ON mode. High active.<br>It is auto cleared when CLUSTERPREQ is active.<br>It is used when DSU power mode transition is controlled by software. |
| 2 | RW | 0x0 | dsu_sft_clusterpactive_off<br>CLUSTERPACTIVE bit generated by software when requested mode is OFF mode. High active.<br>It is auto cleared when CLUSTERPREQ is active.<br>It is used when DSU power mode transition is controlled by software. |
| 1 | RW | 0x0 | dsu_pwroff_sftena<br>Enable VD_LITDSU power off by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | dsu_pwrdn_sftena<br>Enable VD_LITDSU power down by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_DSU_AUTO_PWR_CON**

Address: Operational Base + offset (0x800C)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | dsu_auto_retsf_ena<br>Enable DSU enters SFONLY FUNC_RET mode automatically.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | dsu_auto_ret1p4_ena<br>Enable DSU enters 1/4 FUNC_RET mode automatically.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | dsu_auto_ret1p2_ena<br>Enable DSU enters 1/2 FUNC_RET mode automatically.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | dsu_auto_ret3p4_ena<br>Enable DSU enters 3/4 FUNC_RET mode automatically.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | dsu_auto_onsf_ena<br>Enable DSU enters SFONLY ON mode automatically.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | dsu_auto_on1p4_ena<br>Enable DSU enters 1/4 ON mode automatically.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | dsu_auto_on1p2_ena<br>Enable DSU enters 1/2 ON mode automatically.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | dsu_auto_on3p4_ena<br>Enable DSU enters 3/4 ON mode automatically.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | dsu_auto_fullon_ena<br>Enable DSU enters FULL ON mode automatically.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | dsu_auto_funcret_ena<br>Enable DSU enters FUNC_RET mode automatically.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | dsu_sft_wakeup_ena<br>Enable VD_LITDSU wake up by software.<br>1'b0: Wake up source inactive<br>1'b1: Wake up source active |
| 2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | dsu_int_wakeup_ena<br>Enable interrupt as VD_LITDSU wake up source.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | R/W SC | 0x0 | dsu_lp_en<br>Enable VD_LITDSU low power mode.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CPU0_AUTO_PWR_CON**

Address: Operational Base + offset (0x8010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | cpu_dbgrcv_ncpuporeset_ena<br>Enable CPU enters cold reset by assert ncpureset when CPU in debug recovery mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | cpu_dbgrcv_ncorereset_ena<br>Enable CPU enters warm reset by assert ncorereset when CPU in debug recovery mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | cpu_only_memoff_ena<br>Enable only power down CPU memory. i.e., just power down memory, but not other digital logic when CPU in OFF mode.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | cpu_auto_emuoff_ena<br>Enable CPU emulated off mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | cpu_mem_ls_ena<br>Enable CPU memory light sleep mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | R/W SC | 0x0 | cpu_dbgrcv_ena<br>Enable CPU debug recovery mode by hardware. It is auto cleared when FSM enters debug recovery state.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | cpu_auto_ret_ena<br>Enable CPU retention mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | cpu_sft_wakeup_ena<br>Enable CPU wake up by software.<br>1'b0: Wake up source inactive<br>1'b1: Wake up source active |
| 2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | cpu_int_wakeup_ena<br>Enable interrupt as CPU wake up source.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | cpu_auto_pwrdn_ena<br>Enable CPU power down automatically.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CPU1_AUTO_PWR_CON**

Address: Operational Base + offset (0x8014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | cpu_dbgrcv_ncpuporeset_ena<br>Enable CPU enters cold reset by assert ncpureset when CPU in debug recovery mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | cpu_dbgrcv_ncorereset_ena<br>Enable CPU enters warm reset by assert ncorereset when CPU in debug recovery mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | cpu_only_memoff_ena<br>Enable only power down CPU memory. i.e., just power down memory, but not other digital logic when CPU in OFF mode.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | cpu_auto_emu_ena<br>Enable CPU emulated off mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | cpu_mem_ls_ena<br>Enable CPU memory light sleep mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | R/WSC | 0x0 | cpu_dbgrcv_ena<br>Enable CPU debug recovery mode by hardware. It is auto cleared when FSM enters debug recovery state.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | cpu_auto_ret_ena<br>Enable CPU retention mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | cpu_sft_wakeup_ena<br>Enable CPU wake up by software.<br>1'b0: Wake up source inactive<br>1'b1: Wake up source active |
| 2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | cpu_int_wakeup_ena<br>Enable interrupt as CPU wake up source.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | cpu_auto_pwrdn_ena<br>Enable CPU power down automatically.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CPU2_AUTO_PWR_CON**

Address: Operational Base + offset (0x8018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | cpu_dbgrcv_ncpuporeset_ena<br>Enable CPU enters cold reset by assert ncpureset when CPU in debug recovery mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | cpu_dbgrcv_ncorereset_ena<br>Enable CPU enters warm reset by assert ncorereset when CPU in debug recovery mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | cpu_only_memoff_ena<br>Enable only power down CPU memory. i.e., just power down memory, but not other digital logic when CPU in OFF mode.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | cpu_auto_emu_ena<br>Enable CPU emulated off mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | cpu_mem_ls_ena<br>Enable CPU memory light sleep mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | R/WSC | 0x0 | cpu_dbgrcv_ena<br>Enable CPU debug recovery mode by hardware. It is auto cleared when FSM enters debug recovery state.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | cpu_auto_ret_ena<br>Enable CPU retention mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | cpu_sft_wakeup_ena<br>Enable CPU wake up by software.<br>1'b0: Wake up source inactive<br>1'b1: Wake up source active |
| 2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | cpu_int_wakeup_ena<br>Enable interrupt as CPU wake up source.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | cpu_auto_pwrdn_ena<br>Enable CPU power down automatically.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CPU3_AUTO_PWR_CON**

Address: Operational Base + offset (0x801C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | cpu_dbgrcv_ncpuporeset_ena<br>Enable CPU enters cold reset by assert ncpureset when CPU in debug recovery mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | cpu_dbgrcv_ncorereset_ena<br>Enable CPU enters warm reset by assert ncorereset when CPU in debug recovery mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | cpu_only_memoff_ena<br>Enable only power down CPU memory. i.e., just power down memory, but not other digital logic when CPU in OFF mode.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | cpu_auto_emu_ena<br>Enable CPU emulated off mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | cpu_mem_ls_ena<br>Enable CPU memory light sleep mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | R/WSC | 0x0 | cpu_dbgrcv_ena<br>Enable CPU debug recovery mode by hardware. It is auto cleared when FSM enters debug recovery state.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | cpu_auto_ret_ena<br>Enable CPU retention mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | cpu_sft_wakeup_ena<br>Enable CPU wake up by software.<br>1'b0: Wake up source inactive<br>1'b1: Wake up source active |
| 2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | cpu_int_wakeup_ena<br>Enable interrupt as CPU wake up source.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | cpu_auto_pwrdn_ena<br>Enable CPU power down automatically.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CPU4_AUTO_PWR_CON**

Address: Operational Base + offset (0x8020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | cpu_dbgrcv_ncpuporeset_ena<br>Enable CPU enters cold reset by assert ncpureset when CPU in debug recovery mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | cpu_dbgrcv_ncorereset_ena<br>Enable CPU enters warm reset by assert ncorereset when CPU in debug recovery mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | cpu_only_memoff_ena<br>Enable only power down CPU memory. i.e., just power down memory, but not other digital logic when CPU in OFF mode.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | cpu_auto_emu_ena<br>Enable CPU emulated off mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | cpu_mem_ls_ena<br>Enable CPU memory light sleep mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | R/WSC | 0x0 | cpu_dbgrcv_ena<br>Enable CPU debug recovery mode by hardware. It is auto cleared when FSM enters debug recovery state.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | cpu_auto_ret_ena<br>Enable CPU retention mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | cpu_sft_wakeup_ena<br>Enable CPU wake up by software.<br>1'b0: Wake up source inactive<br>1'b1: Wake up source active |
| 2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | cpu_int_wakeup_ena<br>Enable interrupt as CPU wake up source.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | cpu_auto_pwrdn_ena<br>Enable CPU power down automatically.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CPU5_AUTO_PWR_CON**

Address: Operational Base + offset (0x8024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | cpu_dbgrcv_ncpuporeset_ena<br>Enable CPU enters cold reset by assert ncpureset when CPU in debug recovery mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | cpu_dbgrcv_ncorereset_ena<br>Enable CPU enters warm reset by assert ncorereset when CPU in debug recovery mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | cpu_only_memoff_ena<br>Enable only power down CPU memory. i.e., just power down memory, but not other digital logic when CPU in OFF mode.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | cpu_auto_emu_ena<br>Enable CPU emulated off mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | cpu_mem_ls_ena<br>Enable CPU memory light sleep mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | R/WSC | 0x0 | cpu_dbgrcv_ena<br>Enable CPU debug recovery mode by hardware. It is auto cleared when FSM enters debug recovery state.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | cpu_auto_ret_ena<br>Enable CPU retention mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | cpu_sft_wakeup_ena<br>Enable CPU wake up by software.<br>1'b0: Wake up source inactive<br>1'b1: Wake up source active |
| 2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | cpu_int_wakeup_ena<br>Enable interrupt as CPU wake up source.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | cpu_auto_pwrdn_ena<br>Enable CPU power down automatically.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CPU6_AUTO_PWR_CON**

Address: Operational Base + offset (0x8028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | cpu_dbgrcv_ncpuporeset_ena<br>Enable CPU enters cold reset by assert ncpureset when CPU in debug recovery mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | cpu_dbgrcv_ncorereset_ena<br>Enable CPU enters warm reset by assert ncorereset when CPU in debug recovery mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | cpu_only_memoff_ena<br>Enable only power down CPU memory. i.e., just power down memory, but not other digital logic when CPU in OFF mode.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | cpu_auto_emu_ena<br>Enable CPU emulated off mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | cpu_mem_ls_ena<br>Enable CPU memory light sleep mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | R/WSC | 0x0 | cpu_dbgrcv_ena<br>Enable CPU debug recovery mode by hardware. It is auto cleared when FSM enters debug recovery state.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | cpu_auto_ret_ena<br>Enable CPU retention mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | cpu_sft_wakeup_ena<br>Enable CPU wake up by software.<br>1'b0: Wake up source inactive<br>1'b1: Wake up source active |
| 2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | cpu_int_wakeup_ena<br>Enable interrupt as CPU wake up source.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | cpu_auto_pwrdn_ena<br>Enable CPU power down automatically.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CPU7_AUTO_PWR_CON**

Address: Operational Base + offset (0x802C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | cpu_dbgrcv_ncpuporeset_ena<br>Enable CPU enters cold reset by assert ncpureset when CPU in debug recovery mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | cpu_dbgrcv_ncorereset_ena<br>Enable CPU enters warm reset by assert ncorereset when CPU in debug recovery mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | cpu_only_memoff_ena<br>Enable only power down CPU memory. i.e., just power down memory, but not other digital logic when CPU in OFF mode.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | cpu_auto_emu_ena<br>Enable CPU emulated off mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | cpu_mem_ls_ena<br>Enable CPU memory light sleep mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | R/WSC | 0x0 | cpu_dbgrcv_ena<br>Enable CPU debug recovery mode by hardware. It is auto cleared when FSM enters debug recovery state.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | cpu_auto_ret_ena<br>Enable CPU retention mode by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | cpu_sft_wakeup_ena<br>Enable CPU wake up by software.<br>1'b0: Wake up source inactive<br>1'b1: Wake up source active |
| 2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | cpu_int_wakeup_ena<br>Enable interrupt as CPU wake up source.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | cpu_auto_pwrdn_ena<br>Enable CPU power down automatically.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CPU0_PWR_SFTCON**

Address: Operational Base + offset (0x8030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | cpu_mem_ls_sftena<br>Enable CPU memory light sleep mode by software.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x1 | cpu_dbgrcv_ncpuporeset_sftena<br>Enable CPU enters cold reset by assert ncpureset when CPU in debug recovery mode by software.<br>1'b0: Enable<br>1'b1: Disable |
| 6 | RW | 0x1 | cpu_dbgrcv_ncorereset_sftena<br>Enable CPU enters warm reset by assert ncorereset when CPU in debug recovery mode by software.<br>1'b0: Enable<br>1'b1: Disable |
| 5 | RW | 0x0 | cpu_sft_pactive_dbgrcv<br>PACTIVE bit generated by software when requested mode is debug recovery mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 4 | RW | 0x0 | cpu_sft_pactive_emuoff<br>PACTIVE bit generated by software when requested mode is emulated off mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 3 | RW | 0x0 | cpu_sft_pactive_ret<br>PACTIVE bit generated by software when requested mode is retention mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 2 | RW | 0x0 | cpu_sft_pactive_on<br>PACTIVE bit generated by software when requested mode is ON mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | cpu_sft_pactive_off<br>PACTIVE bit generated by software when requested mode is OFF mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 0 | RW | 0x0 | cpu_pwrdn_sftena<br>Enable CPU power down by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CPU1_PWR_SFTCON**

Address: Operational Base + offset (0x8034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | cpu_mem_ls_sftena<br>Enable CPU memory light sleep mode by software.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x1 | cpu_dbgrcv_ncpuporeset_sftena<br>Enable CPU enters cold reset by assert ncpureset when CPU in debug recovery mode by software.<br>1'b0: Enable<br>1'b1: Disable |
| 6 | RW | 0x1 | cpu_dbgrcv_ncorereset_sftena<br>Enable CPU enters warm reset by assert ncorereset when CPU in debug recovery mode by software.<br>1'b0: Enable<br>1'b1: Disable |
| 5 | RW | 0x0 | cpu_sft_pactive_dbgrcv<br>PACTIVE bit generated by software when requested mode is debug recovery mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 4 | RW | 0x0 | cpu_sft_pactive_emuoff<br>PACTIVE bit generated by software when requested mode is emulated off mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 3 | RW | 0x0 | cpu_sft_pactive_ret<br>PACTIVE bit generated by software when requested mode is retention mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | cpu_sft_pactive_on<br>PACTIVE bit generated by software when requested mode is ON mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 1 | RW | 0x0 | cpu_sft_pactive_off<br>PACTIVE bit generated by software when requested mode is OFF mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 0 | RW | 0x0 | cpu_pwrdn_sftena<br>Enable CPU power down by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CPU2_PWR_SFTCON**

Address: Operational Base + offset (0x8038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | cpu_mem_ls_sftena<br>Enable CPU memory light sleep mode by software.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x1 | cpu_dbgrcv_ncpuporeset_sftena<br>Enable CPU enters cold reset by assert ncpureset when CPU in debug recovery mode by software.<br>1'b0: Enable<br>1'b1: Disable |
| 6 | RW | 0x1 | cpu_dbgrcv_ncorereset_sftena<br>Enable CPU enters warm reset by assert ncorereset when CPU in debug recovery mode by software.<br>1'b0: Enable<br>1'b1: Disable |
| 5 | RW | 0x0 | cpu_sft_pactive_dbgrcv<br>PACTIVE bit generated by software when requested mode is debug recovery mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 4 | RW | 0x0 | cpu_sft_pactive_emuoff<br>PACTIVE bit generated by software when requested mode is emulated off mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | cpu_sft_pactive_ret<br>PACTIVE bit generated by software when requested mode is retention mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 2 | RW | 0x0 | cpu_sft_pactive_on<br>PACTIVE bit generated by software when requested mode is ON mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 1 | RW | 0x0 | cpu_sft_pactive_off<br>PACTIVE bit generated by software when requested mode is OFF mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 0 | RW | 0x0 | cpu_pwrdn_sftena<br>Enable CPU power down by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CPU3_PWR_SFTCON**

Address: Operational Base + offset (0x803C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | cpu_mem_ls_sftena<br>Enable CPU memory light sleep mode by software.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x1 | cpu_dbgrcv_ncpuporeset_sftena<br>Enable CPU enters cold reset by assert ncpureset when CPU in debug recovery mode by software.<br>1'b0: Enable<br>1'b1: Disable |
| 6 | RW | 0x1 | cpu_dbgrcv_ncorereset_sftena<br>Enable CPU enters warm reset by assert ncorereset when CPU in debug recovery mode by software.<br>1'b0: Enable<br>1'b1: Disable |
| 5 | RW | 0x0 | cpu_sft_pactive_dbgrcv<br>PACTIVE bit generated by software when requested mode is debug recovery mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | cpu_sft_pactive_emuoff<br>PACTIVE bit generated by software when requested mode is emulated off mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 3 | RW | 0x0 | cpu_sft_pactive_ret<br>PACTIVE bit generated by software when requested mode is retention mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 2 | RW | 0x0 | cpu_sft_pactive_on<br>PACTIVE bit generated by software when requested mode is ON mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 1 | RW | 0x0 | cpu_sft_pactive_off<br>PACTIVE bit generated by software when requested mode is OFF mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 0 | RW | 0x0 | cpu_pwrdn_sftena<br>Enable CPU power down by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CPU4_PWR_SFTCON**

Address: Operational Base + offset (0x8040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | cpu_mem_ls_sftena<br>Enable CPU memory light sleep mode by software.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x1 | cpu_dbgrcv_ncpuporeset_sftena<br>Enable CPU enters cold reset by assert ncpureset when CPU in debug recovery mode by software.<br>1'b0: Enable<br>1'b1: Disable |
| 6 | RW | 0x1 | cpu_dbgrcv_ncorereset_sftena<br>Enable CPU enters warm reset by assert ncorereset when CPU in debug recovery mode by software.<br>1'b0: Enable<br>1'b1: Disable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | cpu_sft_pactive_dbgrcv<br>PACTIVE bit generated by software when requested mode is debug recovery mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 4 | RW | 0x0 | cpu_sft_pactive_emuoff<br>PACTIVE bit generated by software when requested mode is emulated off mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 3 | RW | 0x0 | cpu_sft_pactive_ret<br>PACTIVE bit generated by software when requested mode is retention mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 2 | RW | 0x0 | cpu_sft_pactive_on<br>PACTIVE bit generated by software when requested mode is ON mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 1 | RW | 0x0 | cpu_sft_pactive_off<br>PACTIVE bit generated by software when requested mode is OFF mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 0 | RW | 0x0 | cpu_pwrdn_sftena<br>Enable CPU power down by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CPU5_PWR_SFTCON**

Address: Operational Base + offset (0x8044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | cpu_mem_ls_sftena<br>Enable CPU memory light sleep mode by software.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x1 | cpu_dbgrcv_ncpuporeset_sftena<br>Enable CPU enters cold reset by assert ncpureset when CPU in debug recovery mode by software.<br>1'b0: Enable<br>1'b1: Disable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x1 | cpu_dbgrcv_ncorereset_sftena<br>Enable CPU enters warm reset by assert ncorereset when CPU in debug recovery mode by software.<br>1'b0: Enable<br>1'b1: Disable |
| 5 | RW | 0x0 | cpu_sft_pactive_dbgrcv<br>PACTIVE bit generated by software when requested mode is debug recovery mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 4 | RW | 0x0 | cpu_sft_pactive_emuoff<br>PACTIVE bit generated by software when requested mode is emulated off mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 3 | RW | 0x0 | cpu_sft_pactive_ret<br>PACTIVE bit generated by software when requested mode is retention mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 2 | RW | 0x0 | cpu_sft_pactive_on<br>PACTIVE bit generated by software when requested mode is ON mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 1 | RW | 0x0 | cpu_sft_pactive_off<br>PACTIVE bit generated by software when requested mode is OFF mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 0 | RW | 0x0 | cpu_pwrdn_sftena<br>Enable CPU power down by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CPU6_PWR_SFTCON**

Address: Operational Base + offset (0x8048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | cpu_mem_ls_sftena<br>Enable CPU memory light sleep mode by software.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x1 | cpu_dbgrcv_ncpuporeset_sftena<br>Enable CPU enters cold reset by assert ncpureset when CPU in debug recovery mode by software.<br>1'b0: Enable<br>1'b1: Disable |
| 6 | RW | 0x1 | cpu_dbgrcv_ncorereset_sftena<br>Enable CPU enters warm reset by assert ncorereset when CPU in debug recovery mode by software.<br>1'b0: Enable<br>1'b1: Disable |
| 5 | RW | 0x0 | cpu_sft_pactive_dbgrcv<br>PACTIVE bit generated by software when requested mode is debug recovery mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 4 | RW | 0x0 | cpu_sft_pactive_emuoff<br>PACTIVE bit generated by software when requested mode is emulated off mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 3 | RW | 0x0 | cpu_sft_pactive_ret<br>PACTIVE bit generated by software when requested mode is retention mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 2 | RW | 0x0 | cpu_sft_pactive_on<br>PACTIVE bit generated by software when requested mode is ON mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 1 | RW | 0x0 | cpu_sft_pactive_off<br>PACTIVE bit generated by software when requested mode is OFF mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 0 | RW | 0x0 | cpu_pwrdn_sftena<br>Enable CPU power down by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CPU7_PWR_SFTCON**

Address: Operational Base + offset (0x804C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | cpu_mem_ls_sftena<br>Enable CPU memory light sleep mode by software.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x1 | cpu_dbgrcv_ncpuporeset_sftena<br>Enable CPU enters cold reset by assert ncpureset when CPU in debug recovery mode by software.<br>1'b0: Enable<br>1'b1: Disable |
| 6 | RW | 0x1 | cpu_dbgrcv_ncorereset_sftena<br>Enable CPU enters warm reset by assert ncorereset when CPU in debug recovery mode by software.<br>1'b0: Enable<br>1'b1: Disable |
| 5 | RW | 0x0 | cpu_sft_pactive_dbgrcv<br>PACTIVE bit generated by software when requested mode is debug recovery mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 4 | RW | 0x0 | cpu_sft_pactive_emuoff<br>PACTIVE bit generated by software when requested mode is emulated off mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 3 | RW | 0x0 | cpu_sft_pactive_ret<br>PACTIVE bit generated by software when requested mode is retention mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 2 | RW | 0x0 | cpu_sft_pactive_on<br>PACTIVE bit generated by software when requested mode is ON mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 1 | RW | 0x0 | cpu_sft_pactive_off<br>PACTIVE bit generated by software when requested mode is OFF mode. High active.<br>It is auto cleared when PREQ is active.<br>It is used when CPU power mode transition is controlled by software. |
| 0 | RW | 0x0 | cpu_pwrdn_sftena<br>Enable CPU power down by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CORE0_PWR_CON**

Address: Operational Base + offset (0x8050)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x1 | core_pwr_cnt_ena<br>Enable counter to wait for VD_BIGCORE0 power on or power off stability.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | core_cpu_pwrdn_ena<br>Enable CPU power down when VD_BIGCORE0 power down by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | core_pwroff_ena<br>Enable VD_BIGCORE0 power off by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | core_pwrdn_ena<br>Enable VD_BIGCORE0 power down by hardware.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CORE1_PWR_CON**

Address: Operational Base + offset (0x8054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x1 | core_pwr_cnt_ena<br>Enable counter to wait for VD_BIGCORE1 power on or power off stability.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | core_cpu_pwrdn_ena<br>Enable CPU power down when VD_BIGCORE1 power down by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | core_pwroff_ena<br>Enable VD_BIGCORE1 power off by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | core_pwrdn_ena<br>Enable VD_BIGCORE1 power down by hardware.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CORE0_PWR_SFTCON**

Address: Operational Base + offset (0x8058)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | core_dwn_ack_clamp_ena<br>Enable clamp for VD_BIGCORE0 power down acknowledge. This bit should be set to 1 if VD_BIGCORE0 power off.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | core_cpu_pwrdn_sftena<br>Enable CPU power down when VD_BIGCORE0 power down by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | core_pwroff_sftena<br>Enable VD_BIGCORE0 power off by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | core_pwrdn_sftena<br>Enable VD_BIGCORE0 power down by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CORE1_PWR_SFTCON**

Address: Operational Base + offset (0x805C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | core_dwn_ack_clamp_ena<br>Enable clamp for VD_BIGCORE1 power down acknowledge. This bit should be set to 1 if VD_BIGCORE1 power off.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | core_cpu_pwrdn_sftena<br>Enable CPU power down when VD_BIGCORE1 power down by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | core_pwroff_sftena<br>Enable VD_BIGCORE1 power off by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | core_pwrdn_sftena<br>Enable VD_BIGCORE1 power down by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CORE0_AUTO_PWR_CON**

Address: Operational Base + offset (0x8060)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | core_int_wakeup_sftena<br>Enable VD_BIGCORE0 wake up by software.<br>1'b0: Wake up source inactive<br>1'b1: Wake up source active |
| 2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | core_int_wakeup_ena<br>Enable interrupt as VD_BIGCORE0 wake up source.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | core_lp_en<br>Enable VD_BIGCORE0 low power mode.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CORE1_AUTO_PWR_CON**

Address: Operational Base + offset (0x8064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | core_int_wakeup_sftena<br>Enable VD_BIGCORE1 wake up by software.<br>1'b0: Wake up source inactive<br>1'b1: Wake up source active |
| 2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | core_int_wakeup_ena<br>Enable interrupt as VD_BIGCORE1 wake up source.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | core_lp_en<br>Enable VD_BIGCORE1 low power mode.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CLUSTER_BIU_AUTO_CON**

Address: Operational Base + offset (0x8068)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | biu_auto_litdsu_ena<br>If enable, BIU_LITDSU corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | biu_auto_dsu_ena<br>If enable, BIU_DSU corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | biu_auto_bigcore1_ena<br>If enable, BIU_BIGCORE1 corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | biu_auto_bigcore0_ena<br>If enable, BIU_BIGCORE0 corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CLUSTER_BIU_IDLE_CON**

Address: Operational Base + offset (0x8070)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x0 | adb400_core_qch_ena<br>Enable core ADB400 Q-Channel power control by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | idle_req_litdsu_ena<br>Enable sending idle request to BIU_LITDSU by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | idle_req_dsu_ena<br>Enable sending idle request to BIU_DSU by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | idle_req_bigcore1_ena<br>Enable sending idle request to BIU_BIGCORE1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | idle_req_bigcore0_ena<br>Enable sending idle request to BIU_BIGCORE0 by hardware.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CLUSTER_BIU_IDLE_SFTCON**

Address: Operational Base + offset (0x8074)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | adb400_core_qch_sftena<br>Enable core ADB400 Q-Channel power control by software.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | idle_req_litdsu_sftena<br>Enable sending idle request to BIU_LITDSU by software.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | idle_req_dsu_sftena<br>Enable sending idle request to BIU_DSU by software.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | idle_req_bigcore1_sftena<br>Enable sending idle request to BIU_BIGCORE1 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | idle_req_bigcore0_sftena<br>Enable sending idle request to BIU_BIGCORE0 by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_CLUSTER_BIU_IDLE_ACK_STS**

Address: Operational Base + offset (0x8078)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4 | RO | 0x0 | adb400_core_paccept<br>PACCEPT state from core ADB400.<br>1'b0: Inactive<br>1'b1: Active |
| 3 | RO | 0x0 | idle_ack_litdsu<br>BIU_LITDSU idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 2 | RO | 0x0 | idle_ack_dsu<br>BIU_DSU idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 1 | RO | 0x0 | idle_ack_bigcore1<br>BIU_BIGCORE1 idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 0 | RO | 0x0 | idle_ack_bigcore0<br>BIU_BIGCORE0 idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |

**PMU_CLUSTER_BIU_IDLE_STS**

Address: Operational Base + offset (0x807C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RO | 0x0 | adb400_core_pactive<br>PACTIVE state from core ADB400.<br>1'b0: Inactive<br>1'b1: Active |
| 3 | RO | 0x0 | idle_litdsu<br>BIU_LITDSU idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 2 | RO | 0x0 | idle_dsu<br>BIU_DSU idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 1 | RO | 0x0 | idle_bigcore1<br>BIU_BIGCORE1 idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 0 | RO | 0x0 | idle_bigcore0<br>BIU_BIGCORE0 idle state.<br>1'b0: Not idle<br>1'b1: Idle |

**PMU_CLUSTER_STS**

Address: Operational Base + offset (0x8080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27 | RO | 0x0 | cpu7_standbywfi<br>CPU7 standbywfi state.<br>1'b0: Not standbywfi<br>1'b1: Standbywfi |
| 26 | RO | 0x0 | cpu6_standbywfi<br>CPU6 standbywfi state.<br>1'b0: Not standbywfi<br>1'b1: Standbywfi |
| 25 | RO | 0x0 | cpu5_standbywfi<br>CPU5 standbywfi state.<br>1'b0: Not standbywfi<br>1'b1: Standbywfi |
| 24 | RO | 0x0 | cpu4_standbywfi<br>CPU4 standbywfi state.<br>1'b0: Not standbywfi<br>1'b1: Standbywfi |
| 23 | RO | 0x0 | cpu3_standbywfi<br>CPU3 standbywfi state.<br>1'b0: Not standbywfi<br>1'b1: Standbywfi |
| 22 | RO | 0x0 | cpu2_standbywfi<br>CPU2 standbywfi state.<br>1'b0: Not standbywfi<br>1'b1: Standbywfi |
| 21 | RO | 0x0 | cpu1_standbywfi<br>CPU1 standbywfi state.<br>1'b0: Not standbywfi<br>1'b1: Standbywfi |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 20 | RO | 0x0 | cpu0_standbywfi<br>CPU0 standbywfi state.<br>1'b0: Not standbywfi<br>1'b1: Standbywfi |
| 19 | RO | 0x0 | dsu_handshake<br>DSU P-Channel hand shake state. If P-Channel request is accepted, it is set to 1; If P-Channel request is denied, it is set to 0.<br>1'b0: Not hand shake<br>1'b1: Hand shake |
| 18 | RO | 0x0 | cpu7_handshake<br>CPU7 P-Channel hand shake state. If P-Channel request is accepted, it is set to 1; If P-Channel request is denied, it is set to 0.<br>1'b0: Not hand shake<br>1'b1: Hand shake |
| 17 | RO | 0x0 | cpu6_handshake<br>CPU6 P-Channel hand shake state. If P-Channel request is accepted, it is set to 1; If P-Channel request is denied, it is set to 0.<br>1'b0: Not hand shake<br>1'b1: Hand shake |
| 16 | RO | 0x0 | cpu5_handshake<br>CPU5 P-Channel hand shake state. If P-Channel request is accepted, it is set to 1; If P-Channel request is denied, it is set to 0.<br>1'b0: Not hand shake<br>1'b1: Hand shake |
| 15 | RO | 0x0 | cpu4_handshake<br>CPU4 P-Channel hand shake state. If P-Channel request is accepted, it is set to 1; If P-Channel request is denied, it is set to 0.<br>1'b0: Not hand shake<br>1'b1: Hand shake |
| 14 | RO | 0x0 | cpu3_handshake<br>CPU3 P-Channel hand shake state. If P-Channel request is accepted, it is set to 1; If P-Channel request is denied, it is set to 0.<br>1'b0: Not hand shake<br>1'b1: Hand shake |
| 13 | RO | 0x0 | cpu2_handshake<br>CPU2 P-Channel hand shake state. If P-Channel request is accepted, it is set to 1; If P-Channel request is denied, it is set to 0.<br>1'b0: Not hand shake<br>1'b1: Hand shake |
| 12 | RO | 0x0 | cpu1_handshake<br>CPU1 P-Channel hand shake state. If P-Channel request is accepted, it is set to 1; If P-Channel request is denied, it is set to 0.<br>1'b0: Not hand shake<br>1'b1: Hand shake |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11 | RO | 0x0 | cpu0_handshake<br>CPU0 P-Channel hand shake state. If P-Channel request is accepted, it is set to 1; If P-Channel request is denied, it is set to 0.<br>1'b0: Not hand shake<br>1'b1: Hand shake |
| 10 | RO | 0x0 | pd_dsu_dwn_stat<br>VD_LITDSU power state.<br>1'b0: Power up<br>1'b1: Power down |
| 9 | RO | 0x0 | pd_core1_dwn_stat<br>VD_BIGCORE1 power state.<br>1'b0: Power up<br>1'b1: Power down |
| 8 | RO | 0x0 | pd_core0_dwn_stat<br>VD_BIGCORE0 power state.<br>1'b0: Power up<br>1'b1: Power down |
| 7 | RO | 0x0 | pd_cpu7_dwn_stat<br>PD_CPU7 power state.<br>1'b0: Power up<br>1'b1: Power down |
| 6 | RO | 0x0 | pd_cpu6_dwn_stat<br>PD_CPU6 power state.<br>1'b0: Power up<br>1'b1: Power down |
| 5 | RO | 0x0 | pd_cpu5_dwn_stat<br>PD_CPU5 power state.<br>1'b0: Power up<br>1'b1: Power down |
| 4 | RO | 0x0 | pd_cpu4_dwn_stat<br>PD_CPU4 power state.<br>1'b0: Power up<br>1'b1: Power down |
| 3 | RO | 0x0 | pd_cpu3_dwn_stat<br>PD_CPU3 power state.<br>1'b0: Power up<br>1'b1: Power down |
| 2 | RO | 0x0 | pd_cpu2_dwn_stat<br>PD_CPU2 power state.<br>1'b0: Power up<br>1'b1: Power down |
| 1 | RO | 0x0 | pd_cpu1_dwn_stat<br>PD_CPU1 power state.<br>1'b0: Power up<br>1'b1: Power down |
| 0 | RO | 0x0 | pd_cpu0_dwn_stat<br>PD_CPU0 power state.<br>1'b0: Power up<br>1'b1: Power down |

**PMU_CLUSTER_POWER_STS0**

Address: Operational Base + offset (0x8084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 30:28 | RO | 0x0 | cpu7_power_state<br>CPU7 power state.<br>3'h0: Normal state<br>3'h1: Off state<br>3'h2: Emulated off state<br>3'h3: Retention state<br>3'h4: Debug recovery state<br>Others: Reserved |
| 27 | RO | 0x0 | reserved |
| 26:24 | RO | 0x0 | cpu6_power_state<br>CPU6 power state.<br>3'h0: Normal state<br>3'h1: Off state<br>3'h2: Emulated off state<br>3'h3: Retention state<br>3'h4: Debug recovery state<br>Others: Reserved |
| 23 | RO | 0x0 | reserved |
| 22:20 | RO | 0x0 | cpu5_power_state<br>CPU5 power state.<br>3'h0: Normal state<br>3'h1: Off state<br>3'h2: Emulated off state<br>3'h3: Retention state<br>3'h4: Debug recovery state<br>Others: Reserved |
| 19 | RO | 0x0 | reserved |
| 18:16 | RO | 0x0 | cpu4_power_state<br>CPU4 power state.<br>3'h0: Normal state<br>3'h1: Off state<br>3'h2: Emulated off state<br>3'h3: Retention state<br>3'h4: Debug recovery state<br>Others: Reserved |
| 15 | RO | 0x0 | reserved |
| 14:12 | RO | 0x0 | cpu3_power_state<br>CPU3 power state.<br>3'h0: Normal state<br>3'h1: Off state<br>3'h2: Emulated off state<br>3'h3: Retention state<br>3'h4: Debug recovery state<br>Others: Reserved |
| 11 | RO | 0x0 | reserved |
| 10:8 | RO | 0x0 | cpu2_power_state<br>CPU2 power state.<br>3'h0: Normal state<br>3'h1: Off state<br>3'h2: Emulated off state<br>3'h3: Retention state<br>3'h4: Debug recovery state<br>Others: Reserved |
| 7 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6:4 | RO | 0x0 | cpu1_power_state<br>CPU1 power state.<br>3'h0: Normal state<br>3'h1: Off state<br>3'h2: Emulated off state<br>3'h3: Retention state<br>3'h4: Debug recovery state<br>Others: Reserved |
| 3 | RO | 0x0 | reserved |
| 2:0 | RO | 0x0 | cpu0_power_state<br>CPU0 power state.<br>3'h0: Normal state<br>3'h1: Off state<br>3'h2: Emulated off state<br>3'h3: Retention state<br>3'h4: Debug recovery state<br>Others: Reserved |

**PMU_CLUSTER_POWER_STS1**

Address: Operational Base + offset (0x8088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:8 | RO | 0x0 | dsu_power_state<br>DSU power state.<br>4'h0: Normal state<br>4'h1: DSU transfer idle state<br>4'h2: DSU power down state<br>4'h3: DSU sleep state<br>4'h4: DSU wake up state<br>4'h5: DSU power up state<br>4'h6: DSU transfer resume state<br>4'h7: DSU FUNC_RET state<br>4'h8: DSU 3/4 ON state<br>4'h9: DSU 1/2 ON state<br>4'ha: DSU 1/4 ON state<br>4'hb: DSU SFONLY ON state<br>4'hc: DSU 3/4 FUNC_RET state<br>4'hd: DSU 1/2 FUNC_RET state<br>4'he: DSU 1/4 FUNC_RET state<br>4'hf: DSU SFONLY FUNC_RET state |
| 7:4 | RO | 0x0 | core1_power_state<br>BIGCORE1 power state.<br>4'h0: Normal state<br>4'h1: CPU power down state<br>4'h2: Core transfer idle state<br>4'h3: Core power down state<br>4'h4: Core sleep state<br>4'h5: Core wake up state<br>4'h6: Core power up state<br>4'h7: Core transfer resume state<br>4'h8: CPU power up state<br>Others: Reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RO | 0x0 | core0_power_state<br>BIGCORE0 power state.<br>4'h0: Normal state<br>4'h1: CPU power down state<br>4'h2: Core transfer idle state<br>4'h3: Core power down state<br>4'h4: Core sleep state<br>4'h5: Core wake up state<br>4'h6: Core power up state<br>4'h7: Core transfer resume state<br>4'h8: CPU power up state<br>Others: Reserved |

**PMU_CLUSTER_PCHANNEL_STS0**

Address: Operational Base + offset (0x808C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:24 | RO | 0x00 | cpu3_pchannel_status<br>CPU3 P-Channel status. High active.<br>Bit[24]: PACTIVE bit [1]<br>Bit[25]: PACTIVE bit [5]<br>Bit[26]: PACTIVE bit [7]<br>Bit[27]: PACTIVE bit [8]<br>Bit[28]: PACCEPT<br>Bit[29]: PDENY |
| 23:22 | RO | 0x0 | reserved |
| 21:16 | RO | 0x00 | cpu2_pchannel_status<br>CPU2 P-Channel status. High active.<br>Bit[16]: PACTIVE bit [1]<br>Bit[17]: PACTIVE bit [5]<br>Bit[18]: PACTIVE bit [7]<br>Bit[19]: PACTIVE bit [8]<br>Bit[20]: PACCEPT<br>Bit[21]: PDENY |
| 15:14 | RO | 0x0 | reserved |
| 13:8 | RO | 0x00 | cpu1_pchannel_status<br>CPU1 P-Channel status. High active.<br>Bit[8]: PACTIVE bit [1]<br>Bit[9]: PACTIVE bit [5]<br>Bit[10]: PACTIVE bit [7]<br>Bit[11]: PACTIVE bit [8]<br>Bit[12]: PACCEPT<br>Bit[13]: PDENY |
| 7:6 | RO | 0x0 | reserved |
| 5:0 | RO | 0x00 | cpu0_pchannel_status<br>CPU0 P-Channel status. High active.<br>Bit[0]: PACTIVE bit [1]<br>Bit[1]: PACTIVE bit [5]<br>Bit[2]: PACTIVE bit [7]<br>Bit[3]: PACTIVE bit [8]<br>Bit[4]: PACCEPT<br>Bit[5]: PDENY |

**PMU_CLUSTER_PCHANNEL_STS1**

Address: Operational Base + offset (0x8090)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:24 | RO | 0x00 | cpu7_pchannel_status<br>CPU7 P-Channel status. High active.<br>Bit[24]: PACTIVE bit [1]<br>Bit[25]: PACTIVE bit [5]<br>Bit[26]: PACTIVE bit [7]<br>Bit[27]: PACTIVE bit [8]<br>Bit[28]: PACCEPT<br>Bit[29]: PDENY |
| 23:22 | RO | 0x0 | reserved |
| 21:16 | RO | 0x00 | cpu6_pchannel_status<br>CPU6 P-Channel status. High active.<br>Bit[16]: PACTIVE bit [1]<br>Bit[17]: PACTIVE bit [5]<br>Bit[18]: PACTIVE bit [7]<br>Bit[19]: PACTIVE bit [8]<br>Bit[20]: PACCEPT<br>Bit[21]: PDENY |
| 15:14 | RO | 0x0 | reserved |
| 13:8 | RO | 0x00 | cpu5_pchannel_status<br>CPU5 P-Channel status. High active.<br>Bit[8]: PACTIVE bit [1]<br>Bit[9]: PACTIVE bit [5]<br>Bit[10]: PACTIVE bit [7]<br>Bit[11]: PACTIVE bit [8]<br>Bit[12]: PACCEPT<br>Bit[13]: PDENY |
| 7:6 | RO | 0x0 | reserved |
| 5:0 | RO | 0x00 | cpu4_pchannel_status<br>CPU4 P-Channel status. High active.<br>Bit[0]: PACTIVE bit [1]<br>Bit[1]: PACTIVE bit [5]<br>Bit[2]: PACTIVE bit [7]<br>Bit[3]: PACTIVE bit [8]<br>Bit[4]: PACCEPT<br>Bit[5]: PDENY |

**PMU_CLUSTER_PCHANNEL_STS2**

Address: Operational Base + offset (0x8094)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:9 | RO | 0x000000 | reserved |
| 8:0 | RO | 0x000 | dsu_pchannel_status<br>DSU P-Channel status. High active.<br>Bit[0]: CLUSTERPACTIVE bit [2]<br>Bit[1]: CLUSTERPACTIVE bit [7]<br>Bit[2]: CLUSTERPACTIVE bit [8]<br>Bit[3]: CLUSTERPACTIVE bit [16]<br>Bit[4]: CLUSTERPACTIVE bit [17]<br>Bit[5]: CLUSTERPACTIVE bit [18]<br>Bit[6]: CLUSTERPACTIVE bit [19]<br>Bit[7]: CLUSTERPACCEPT<br>Bit[8]: CLUSTERPDENY |

**PMU_CPU_PWR_CHAIN_STABLE_CON**

Address: Operational Base + offset (0x8098)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | cpu7_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_CPU7 power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | cpu6_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_CPU6 power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | cpu5_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_CPU5 power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | cpu4_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_CPU4 power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | cpu3_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_CPU3 power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | cpu2_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_CPU2 power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | cpu1_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_CPU1 power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | cpu0_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_CPU0 power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x1 | cpu7_pwrup_stable_ena<br>Enable stable counter between power chains for PD_CPU7 power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x1 | cpu6_pwrup_stable_ena<br>Enable stable counter between power chains for PD_CPU6 power up flow.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x1 | cpu5_pwrup_stable_ena<br>Enable stable counter between power chains for PD_CPU5 power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x1 | cpu4_pwrup_stable_ena<br>Enable stable counter between power chains for PD_CPU4 power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x1 | cpu3_pwrup_stable_ena<br>Enable stable counter between power chains for PD_CPU3 power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x1 | cpu2_pwrup_stable_ena<br>Enable stable counter between power chains for PD_CPU2 power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x1 | cpu1_pwrup_stable_ena<br>Enable stable counter between power chains for PD_CPU1 power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x1 | cpu0_pwrup_stable_ena<br>Enable stable counter between power chains for PD_CPU0 power up flow.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_DSU_MEM_PWR_CON**

Address: Operational Base + offset (0x809C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RW | 0x0 | dsu_mem_ls_sftena<br>Enable DSU memory enters light sleep mode by software.<br>1'b0: Disable<br>1'b1: Enable<br>Bit[12] used to light sleep "Snoop filter and LTDB RAMs".<br>Bit[13] used to light sleep "L3 Tag ways 0~3, L3 Data portion 0, and L3 Victim RAMs".<br>Bit[14] used to light sleep "L3 Tag ways 4~7".<br>Bit[15] used to light sleep "L3 Tag ways 8~11, L3 Data portion 1 RAMs". |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:8 | RW | 0x0 | dsu_mem_sd_sftena<br>Enable DSU memory enters shutdown mode by software.<br>1'b0: Disable<br>1'b1: Enable<br>Bit[8] used to shutdown "Snoop filter and LTDB RAMs".<br>Bit[9] used to shutdown "L3 Tag ways 0~3, L3 Data portion 0, and L3 Victim RAMs".<br>Bit[10] used to shutdown "L3 Tag ways 4~7".<br>Bit[11] used to shutdown "L3 Tag ways 8~11, L3 Data portion 1 RAMs". |
| 7:4 | RW | 0x0 | dsu_mem_ls_ena<br>Enable DSU memory enters light sleep mode by hardware.<br>1'b0: Disable<br>1'b1: Enable<br>Bit[4] used to light sleep "Snoop filter and LTDB RAMs".<br>Bit[5] used to light sleep "L3 Tag ways 0~3, L3 Data portion 0, and L3 Victim RAMs".<br>Bit[6] used to light sleep "L3 Tag ways 4~7".<br>Bit[7] used to light sleep "L3 Tag ways 8~11, L3 Data portion 1 RAMs". |
| 3:0 | RW | 0x0 | dsu_mem_sd_ena<br>Enable DSU memory enters shutdown mode by hardware.<br>1'b0: Disable<br>1'b1: Enable<br>Bit[0] used to shutdown "Snoop filter and LTDB RAMs".<br>Bit[1] used to shutdown "L3 Tag ways 0~3, L3 Data portion 0, and L3 Victim RAMs".<br>Bit[2] used to shutdown "L3 Tag ways 4~7".<br>Bit[3] used to shutdown "L3 Tag ways 8~11, L3 Data portion 1 RAMs". |

**PMU_DSU_STABLE_CNT**

Address: Operational Base + offset (0x80B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfffff | dsu_stable_cnt<br>VD_DSU power stable count. Number of clk_pmu used by counter logic. |

**PMU_DSU_PWRUP_CNT**

Address: Operational Base + offset (0x80B4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x05dc0 | dsu_pwrup_cnt<br>VD_DSU power up count. Number of clk_pmu used by counter logic. |

**PMU_DSU_PWRDN_CNT**

Address: Operational Base + offset (0x80B8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x05dc0 | dsu_pwrdn_cnt<br>VD_DSU power down count. Number of clk_pmu used by counter logic. |

Rockchip Confidential

**PMU_CORE0_STABLE_CNT**

Address: Operational Base + offset (0x80BC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfffff | core0_stable_cnt<br>VD_BIGCORE0 power stable count. Number of clk_pmu used by counter logic. |

**PMU_CORE0_PWRUP_CNT**

Address: Operational Base + offset (0x80C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x05dc0 | core0_pwrup_cnt<br>VD_BIGCORE0 power up count. Number of clk_pmu used by counter logic. |

**PMU_CORE0_PWRDN_CNT**

Address: Operational Base + offset (0x80C4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x05dc0 | core0_pwrdn_cnt<br>VD_BIGCORE0 power down count. Number of clk_pmu used by counter logic. |

**PMU_CORE1_STABLE_CNT**

Address: Operational Base + offset (0x80C8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfffff | core1_stable_cnt<br>VD_BIGCORE1 power stable count. Number of clk_pmu used by counter logic. |

**PMU_CORE1_PWRUP_CNT**

Address: Operational Base + offset (0x80CC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x05dc0 | core1_pwrup_cnt<br>VD_BIGCORE1 power up count. Number of clk_pmu used by counter logic. |

**PMU_CORE1_PWRDN_CNT**

Address: Operational Base + offset (0x80D0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x05dc0 | core1_pwrdn_cnt<br>VD_BIGCORE1 power down count. Number of clk_pmu used by counter logic. |

**PMU_CPU0_DBG_RST_CNT**

Address: Operational Base + offset (0x80D4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19:0 | RW | 0xfffff | cpu0_dbg_rst_cnt<br>CPU0 debug reset count. Number of clk_pmu used by counter logic.<br>The CPU reset holds low until counter to zero in debug recovery mode. |

**PMU_CPU1_DBG_RST_CNT**

Address: Operational Base + offset (0x80D8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfffff | cpu1_dbg_rst_cnt<br>CPU1 debug reset count. Number of clk_pmu used by counter logic.<br>The CPU reset holds low until counter to zero in debug recovery mode. |

**PMU_CPU2_DBG_RST_CNT**

Address: Operational Base + offset (0x80DC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfffff | cpu2_dbg_rst_cnt<br>CPU2 debug reset count. Number of clk_pmu used by counter logic.<br>The CPU reset holds low until counter to zero in debug recovery mode. |

**PMU_CPU3_DBG_RST_CNT**

Address: Operational Base + offset (0x80E0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfffff | cpu3_dbg_rst_cnt<br>CPU3 debug reset count. Number of clk_pmu used by counter logic.<br>The CPU reset holds low until counter to zero in debug recovery mode. |

**PMU_CPU4_DBG_RST_CNT**

Address: Operational Base + offset (0x80E4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfffff | cpu4_dbg_rst_cnt<br>CPU4 debug reset count. Number of clk_pmu used by counter logic.<br>The CPU reset holds low until counter to zero in debug recovery mode. |

**PMU_CPU5_DBG_RST_CNT**

Address: Operational Base + offset (0x80E8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfffff | cpu5_dbg_rst_cnt<br>CPU5 debug reset count. Number of clk_pmu used by counter logic.<br>The CPU reset holds low until counter to zero in debug recovery mode. |

Rockchip Confidential

**PMU_CPU6_DBG_RST_CNT**

Address: Operational Base + offset (0x80EC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfffff | cpu6_dbg_rst_cnt<br>CPU6 debug reset count. Number of clk_pmu used by counter logic.<br>The CPU reset holds low until counter to zero in debug recovery mode. |

**PMU_CPU7_DBG_RST_CNT**

Address: Operational Base + offset (0x80F0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfffff | cpu7_dbg_rst_cnt<br>CPU7 debug reset count. Number of clk_pmu used by counter logic.<br>The CPU reset holds low until counter to zero in debug recovery mode. |

**PMU_BIU_IDLE_CON0**

Address: Operational Base + offset (0x8100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | idle_req_vo0_ena<br>Enable sending idle request to BIU_VO0 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | idle_req_vop_channel_ena<br>Enable sending idle request to BIU_VOP_CHANNEL by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | idle_req_vop_ena<br>Enable sending idle request to BIU_VOP by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | idle_req_rga31_ena<br>Enable sending idle request to BIU_RGA31 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | idle_req_isp1_ena<br>Enable sending idle request to BIU_ISP1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | idle_req_vi_ena<br>Enable sending idle request to BIU_VI by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | idle_req_av1_ena<br>Enable sending idle request to BIU_AV1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | idle_req_vdpu_ena<br>Enable sending idle request to BIU_VDPU by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | idle_req_rkvdec1_ena<br>Enable sending idle request to BIU_RKVDEC1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | idle_req_rkvdec0_ena<br>Enable sending idle request to BIU_RKVDEC0 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | idle_req_venc1_ena<br>Enable sending idle request to BIU_VENC1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | idle_req_venc0_ena<br>Enable sending idle request to BIU_VENC0 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | idle_req_npu2_ena<br>Enable sending idle request to BIU_NPU2 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | idle_req_npu1_ena<br>Enable sending idle request to BIU_NPU1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | idle_req_nputop_ena<br>Enable sending idle request to BIU_NPUTOP by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | idle_req_gpu_ena<br>Enable sending idle request to BIU_GPU by hardware.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_BIU_IDLE_CON1**

Address: Operational Base + offset (0x8104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | idle_req_ddrsch3_ena<br>Enable sending idle request to BIU_DDRSCH3 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | idle_req_ddrsch2_ena<br>Enable sending idle request to BIU_DDRSCH2 by hardware.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | idle_req_ddrsch1_ena<br>Enable sending idle request to BIU_DDRSCH1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | idle_req_ddrsch0_ena<br>Enable sending idle request to BIU_DDRSCH0 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | idle_req_center_channel_ena<br>Enable sending idle request to BIU_CENTER_CHANNEL by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | idle_req_center_ena<br>Enable sending idle request to BIU_CENTER by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | idle_req_secure_vo1usb_channel_ena<br>Enable sending idle request to BIU_SECURE_VO1USB_CHANNEL by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | idle_req_secure_center_channel_ena<br>Enable sending idle request to BIU_SECURE_CENTER_CHANNEL by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | idle_req_secure_ena<br>Enable sending idle request to BIU_SECURE by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | idle_req_vo1usbtop_ena<br>Enable sending idle request to BIU_VO1USBTOP by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | idle_req_php_ena<br>Enable sending idle request to BIU_PHP by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | idle_req_usb_ena<br>Enable sending idle request to BIU_USB by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | idle_req_sdio_ena<br>Enable sending idle request to BIU_SDIO by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | idle_req_nvm_ena<br>Enable sending idle request to BIU_NVM by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | idle_req_audio_ena<br>Enable sending idle request to BIU_AUDIO by hardware.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | idle_req_vo1_ena<br>Enable sending idle request to BIU_VO1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_BIU_IDLE_CON2**

Address: Operational Base + offset (0x8108)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:3 | RO | 0x0000 | reserved |
| 2 | RW | 0x0 | idle_req_top_ena<br>Enable sending idle request to BIU_TOP by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | idle_req_bus_ena<br>Enable sending idle request to BIU_BUS by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | idle_req_center_ddrsch_ena<br>Enable sending idle request to BIU_CENTER_DDRSCH by hardware.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_BIU_IDLE_SFTCON0**

Address: Operational Base + offset (0x810C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | idle_req_vo0_sftena<br>Enable sending idle request to BIU_VO0 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | idle_req_vop_channel_sftena<br>Enable sending idle request to BIU_VOP_CHANNEL by software.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | idle_req_vop_sftena<br>Enable sending idle request to BIU_VOP by software.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | idle_req_rga31_sftena<br>Enable sending idle request to BIU_RGA31 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | idle_req_isp1_sftena<br>Enable sending idle request to BIU_ISP1 by software.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10 | RW | 0x0 | idle_req_vi_sftena<br>Enable sending idle request to BIU_VI by software.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | idle_req_av1_sftena<br>Enable sending idle request to BIU_AV1 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | idle_req_vdpu_sftena<br>Enable sending idle request to BIU_VDPU by software.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | idle_req_rkvdec1_sftena<br>Enable sending idle request to BIU_RKVDEC1 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | idle_req_rkvdec0_sftena<br>Enable sending idle request to BIU_RKVDEC0 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | idle_req_venc1_sftena<br>Enable sending idle request to BIU_VENC1 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | idle_req_venc0_sftena<br>Enable sending idle request to BIU_VENC0 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | idle_req_npu2_sftena<br>Enable sending idle request to BIU_NPU2 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | idle_req_npu1_sftena<br>Enable sending idle request to BIU_NPU1 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | idle_req_nputop_sftena<br>Enable sending idle request to BIU_NPUTOP by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | idle_req_gpu_sftena<br>Enable sending idle request to BIU_GPU by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_BIU_IDLE_SFTCON1**

Address: Operational Base + offset (0x8110)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x0 | idle_req_ddrsch3_sftena<br>Enable sending idle request to BIU_DDRSCH3 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | idle_req_ddrsch2_sftena<br>Enable sending idle request to BIU_DDRSCH2 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | idle_req_ddrsch1_sftena<br>Enable sending idle request to BIU_DDRSCH1 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | idle_req_ddrsch0_sftena<br>Enable sending idle request to BIU_DDRSCH0 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | idle_req_center_channel_sftena<br>Enable sending idle request to BIU_CENTER_CHANNEL by software.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | idle_req_center_sftena<br>Enable sending idle request to BIU_CENTER by software.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | idle_req_secure_vo1usb_channel_sftena<br>Enable sending idle request to BIU_SECURE_VO1USB_CHANNEL by software.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | idle_req_secure_center_channel_sftena<br>Enable sending idle request to BIU_SECURE_CENTER_CHANNEL by software.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | idle_req_secure_sftena<br>Enable sending idle request to BIU_SECURE by software.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | idle_req_vo1usbtop_sftena<br>Enable sending idle request to BIU_VO1USBTOP by software.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | idle_req_php_sftena<br>Enable sending idle request to BIU_PHP by software.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | idle_req_usb_sftena<br>Enable sending idle request to BIU_USB by software.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | idle_req_sdio_sftena<br>Enable sending idle request to BIU_SDIO by software.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | idle_req_nvm_sftena<br>Enable sending idle request to BIU_NVM by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | idle_req_audio_sftena<br>Enable sending idle request to BIU_AUDIO by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | idle_req_vo1_sftena<br>Enable sending idle request to BIU_VO1 by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_BIU_IDLE_SFTCON2**

Address: Operational Base + offset (0x8114)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:3 | RO | 0x0000 | reserved |
| 2 | RW | 0x0 | idle_req_top_sftena<br>Enable sending idle request to BIU_TOP by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | idle_req_bus_sftena<br>Enable sending idle request to BIU_BUS by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | idle_req_center_ddrsch_sftena<br>Enable sending idle request to BIU_CENTER_DDRSCH by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_BIU_IDLE_ACK_STS0**

Address: Operational Base + offset (0x8118)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | idle_ack_ddrsch3<br>BIU_DDRSCH3 idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 30 | RO | 0x0 | idle_ack_ddrsch2<br>BIU_DDRSCH2 idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 29 | RO | 0x0 | idle_ack_ddrsch1<br>BIU_DDRSCH1 idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 28 | RO | 0x0 | idle_ack_ddrsch0<br>BIU_DDRSCH0 idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 27 | RO | 0x0 | idle_ack_center_channel<br>BIU_CENTER_CHANNEL idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 26 | RO | 0x0 | idle_ack_center<br>BIU_CENTER idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 25 | RO | 0x0 | idle_ack_secure_vo1usb_channel<br>BIU_SECURE_VO1USB_CHANNEL idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 24 | RO | 0x0 | idle_ack_secure_center_channel<br>BIU_SECURE_CENTER_CHANNEL idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 23 | RO | 0x0 | idle_ack_secure<br>BIU_SECURE idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 22 | RO | 0x0 | idle_ack_vo1usbtop<br>BIU_VO1USBTOP idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 21 | RO | 0x0 | idle_ack_php<br>BIU_PHP idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 20 | RO | 0x0 | idle_ack_usb<br>BIU_USB idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 19 | RO | 0x0 | idle_ack_sdio<br>BIU_SDIO idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 18 | RO | 0x0 | idle_ack_nvm<br>BIU_NVM idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 17 | RO | 0x0 | idle_ack_audio<br>BIU_AUDIO idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 16 | RO | 0x0 | idle_ack_vo1<br>BIU_VO1 idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 15 | RO | 0x0 | idle_ack_vo0<br>BIU_VO0 idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14 | RO | 0x0 | idle_ack_vop_channel<br>BIU_VOP_CHANNEL idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 13 | RO | 0x0 | idle_ack_vop<br>BIU_VOP idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 12 | RO | 0x0 | idle_ack_rga31<br>BIU_RGA31 idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 11 | RO | 0x0 | idle_ack_isp1<br>BIU_ISP1 idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 10 | RO | 0x0 | idle_ack_vi<br>BIU_VI idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 9 | RO | 0x0 | idle_ack_av1<br>BIU_AV1 idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 8 | RO | 0x0 | idle_ack_vdpu<br>BIU_VDPU idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 7 | RO | 0x0 | idle_ack_rkvdec1<br>BIU_RKVDEC1 idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 6 | RO | 0x0 | idle_ack_rkvdec0<br>BIU_RKVDEC0 idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 5 | RO | 0x0 | idle_ack_venc1<br>BIU_VENC1 idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 4 | RO | 0x0 | idle_ack_venc0<br>BIU_VENC0 idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 3 | RO | 0x0 | idle_ack_npu2<br>BIU_NPU2 idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 2 | RO | 0x0 | idle_ack_npu1<br>BIU_NPU1 idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RO | 0x0 | idle_ack_nputop<br>BIU_NPUTOP idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 0 | RO | 0x0 | idle_ack_gpu<br>BIU_GPU idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |

**PMU_BIU_IDLE_ACK_STS1**

Address: Operational Base + offset (0x811C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2 | RO | 0x0 | idle_ack_top<br>BIU_TOP idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 1 | RO | 0x0 | idle_ack_bus<br>BIU_BUS idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |
| 0 | RO | 0x0 | idle_ack_center_ddrsch<br>BIU_CENTER_DDRSCH idle acknowledge state.<br>1'b0: Not acknowledge<br>1'b1: Acknowledge |

**PMU_BIU_IDLE_STS0**

Address: Operational Base + offset (0x8120)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | idle_ddrsch3<br>BIU_DDRSCH3 idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 30 | RO | 0x0 | idle_ddrsch2<br>BIU_DDRSCH2 idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 29 | RO | 0x0 | idle_ddrsch1<br>BIU_DDRSCH1 idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 28 | RO | 0x0 | idle_ddrsch0<br>BIU_DDRSCH0 idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 27 | RO | 0x0 | idle_center_channel<br>BIU_CENTER_CHANNEL idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 26 | RO | 0x0 | idle_center<br>BIU_CENTER idle state.<br>1'b0: Not idle<br>1'b1: Idle |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 25 | RO | 0x0 | idle_secure_vo1usb_channel<br>BIU_SECURE_VO1USB_CHANNEL idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 24 | RO | 0x0 | idle_secure_center_channel<br>BIU_SECURE_CENTER_CHANNEL idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 23 | RO | 0x0 | idle_secure<br>BIU_SECURE idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 22 | RO | 0x0 | idle_vo1usbtop<br>BIU_VO1USBTOP idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 21 | RO | 0x0 | idle_php<br>BIU_PHP idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 20 | RO | 0x0 | idle_usb<br>BIU_USB idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 19 | RO | 0x0 | idle_sdio<br>BIU_SDIO idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 18 | RO | 0x0 | idle_nvm<br>BIU_NVM idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 17 | RO | 0x0 | idle_audio<br>BIU_AUDIO idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 16 | RO | 0x0 | idle_vo1<br>BIU_VO1 idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 15 | RO | 0x0 | idle_vo0<br>BIU_VO0 idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 14 | RO | 0x0 | idle_vop_channel<br>BIU_VOP_CHANNEL idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 13 | RO | 0x0 | idle_vop<br>BIU_VOP idle state.<br>1'b0: Not idle<br>1'b1: Idle |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RO | 0x0 | idle_rga31<br>BIU_RGA31 idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 11 | RO | 0x0 | idle_isp1<br>BIU_ISP1 idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 10 | RO | 0x0 | idle_vi<br>BIU_VI idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 9 | RO | 0x0 | idle_av1<br>BIU_AV1 idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 8 | RO | 0x0 | idle_vdpu<br>BIU_VDPU idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 7 | RO | 0x0 | idle_rkvdec1<br>BIU_RKVDEC1 idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 6 | RO | 0x0 | idle_rkvdec0<br>BIU_RKVDEC0 idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 5 | RO | 0x0 | idle_venc1<br>BIU_VENC1 idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 4 | RO | 0x0 | idle_venc0<br>BIU_VENC0 idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 3 | RO | 0x0 | idle_npu2<br>BIU_NPU2 idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 2 | RO | 0x0 | idle_npu1<br>BIU_NPU1 idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 1 | RO | 0x0 | idle_nputop<br>BIU_NPUTOP idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 0 | RO | 0x0 | idle_gpu<br>BIU_GPU idle state.<br>1'b0: Not idle<br>1'b1: Idle |

**PMU_BIU_IDLE_STS1**

Address: Operational Base + offset (0x8124)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2 | RO | 0x0 | idle_top<br>BIU_TOP idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 1 | RO | 0x0 | idle_bus<br>BIU_BUS idle state.<br>1'b0: Not idle<br>1'b1: Idle |
| 0 | RO | 0x0 | idle_center_ddrsch<br>BIU_CENTER_DDRSCH idle state.<br>1'b0: Not idle<br>1'b1: Idle |

**PMU_BIU_AUTO_CON0**

Address: Operational Base + offset (0x8128)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | idle_auto_vo0_ena<br>If enable, BIU_VO0 corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | idle_auto_vop_channel_ena<br>If enable, BIU_VOP_CHANNEL corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | idle_auto_vop_ena<br>If enable, BIU_VOP corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | idle_auto_rga31_ena<br>If enable, BIU_RGA31 corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | idle_auto_isp1_ena<br>If enable, BIU_ISP1 corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | idle_auto_vi_ena<br>If enable, BIU_VI corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RW | 0x0 | idle_auto_av1_ena<br>If enable, BIU_AV1 corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | idle_auto_vdpu_ena<br>If enable, BIU_VDPU corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | idle_auto_rkvdec1_ena<br>If enable, BIU_RKVDEC1 corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | idle_auto_rkvdec0_ena<br>If enable, BIU_RKVDEC0 corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | idle_auto_venc1_ena<br>If enable, BIU_VENC1 corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | idle_auto_venc0_ena<br>If enable, BIU_VENC0 corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | idle_auto_npu2_ena<br>If enable, BIU_NPU2 corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | idle_auto_npu1_ena<br>If enable, BIU_NPU1 corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | idle_auto_nputop_ena<br>If enable, BIU_NPUTOP corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | biu_auto_gpu_ena<br>If enable, BIU_GPU corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_BIU_AUTO_CON1**

Address: Operational Base + offset (0x812C)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | idle_auto_ddrsch3_ena<br>If enable, BIU_DDRSCH3 corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | idle_auto_ddrsch2_ena<br>If enable, BIU_DDRSCH2 corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | idle_auto_ddrsch1_ena<br>If enable, BIU_DDRSCH1 corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | idle_auto_ddrsch0_ena<br>If enable, BIU_DDRSCH0 corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | idle_auto_center_channel_ena<br>If enable, BIU_CENTER_CHANNEL corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | idle_auto_center_ena<br>If enable, BIU_CENTER corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | idle_auto_secure_vo1usb_channel_ena<br>If enable, BIU_SECURE_VO1USB_CHANNEL corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | idle_auto_secure_center_channel_ena<br>If enable, BIU_SECURE_CENTER_CHANNEL corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | idle_auto_secure_ena<br>If enable, BIU_SECURE corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | idle_auto_vo1usbtop_ena<br>If enable, BIU_VO1USBTOP corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | idle_auto_php_ena<br>If enable, BIU_PHP corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | idle_auto_usb_ena<br>If enable, BIU_USB corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | idle_auto_sdio_ena<br>If enable, BIU_SDIO corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | idle_auto_nvm_ena<br>If enable, BIU_NVM corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | idle_auto_audio_ena<br>If enable, BIU_AUDIO corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | idle_auto_vo1_ena<br>If enable, BIU_VO1 corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_BIU_AUTO_CON2**

Address: Operational Base + offset (0x8130)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:3 | RO | 0x0000 | reserved |
| 2 | RW | 0x0 | idle_auto_top_ena<br>If enable, BIU_TOP corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | idle_auto_bus_ena<br>If enable, BIU_BUS corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | idle_auto_center_ddrsch_ena<br>If enable, BIU_CENTER_DDRSCH corresponding clock can be opened or gated automatically when idle operation.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

**PMU_PWR_GATE_CON0**

Address: Operational Base + offset (0x8140)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pd_isp1_dwn_ena<br>Enable power down PD_ISP1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | pd_fec_dwn_ena<br>Enable power down PD_FEC by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | pd_vi_dwn_ena<br>Enable power down PD_VI by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | pd_av1_dwn_ena<br>Enable power down PD_AV1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | pd_rga30_dwn_ena<br>Enable power down PD_RGA30 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | pd_vdpu_dwn_ena<br>Enable power down PD_VDPU by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | pd_rkvdec1_dwn_ena<br>Enable power down PD_RKVDEC1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | pd_rkvdec0_dwn_ena<br>Enable power down PD_RKVDEC0 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | pd_venc1_dwn_ena<br>Enable power down PD_VENC1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | pd_venc0_dwn_ena<br>Enable power down PD_VENC0 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | pd_npu2_dwn_ena<br>Enable power down PD_NPU2 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | pd_npu1_dwn_ena<br>Enable power down PD_NPU1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | pd_nputop_dwn_ena<br>Enable power down PD_NPUTOP by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | pd_vcodec_dwn_ena<br>Enable power down VD_VCODEC by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | pd_npu_dwn_ena<br>Enable power down VD_NPU by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | pd_gpu_dwn_ena<br>Enable power down VD_GPU by hardware.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_PWR_GATE_CON1**

Address: Operational Base + offset (0x8144)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pd_center_dwn_ena<br>Enable power down PD_CENTER by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | pd_crypto_dwn_ena<br>Enable power down PD_CRYPTO by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | pd_sdmmc_dwn_ena<br>Enable power down PD_SDMMC by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | pd_secure_dwn_ena<br>Enable power down PD_SECURE by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | pd_usb_dwn_ena<br>Enable power down PD_USB by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | pd_sdio_dwn_ena<br>Enable power down PD_SDIO by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | pd_nvm0_dwn_ena<br>Enable power down PD_NVM0 by hardware.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | pd_nvm_dwn_ena<br>Enable power down PD_NVM by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | pd_pcie_dwn_ena<br>Enable power down PD_PCIE by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | pd_gmac_dwn_ena<br>Enable power down PD_GMAC by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | pd_php_dwn_ena<br>Enable power down PD_PHP by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | pd_audio_dwn_ena<br>Enable power down PD_AUDIO by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | pd_vo1_dwn_ena<br>Enable power down PD_VO1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | pd_vo0_dwn_ena<br>Enable power down PD_VO0 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | pd_vop_dwn_ena<br>Enable power down PD_VOP by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | pd_rga31_dwn_ena<br>Enable power down PD_RGA31 by hardware.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_PWR_GATE_CON2**

Address: Operational Base + offset (0x8148)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | pd_ddr23_dwn_ena<br>Enable power down VD_DDR23 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | pd_ddr01_dwn_ena<br>Enable power down VD_DDR01 by hardware.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_PWR_GATE_SFTCON0**

Rockchip Confidencial

Address: Operational Base + offset (0x814C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | pd_isp1_dwn_sftena<br>Enable power down PD_ISP1 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x1 | pd_fec_dwn_sftena<br>Enable power down PD_FEC by software.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x1 | pd_vi_dwn_sftena<br>Enable power down PD_VI by software.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x1 | pd_av1_dwn_sftena<br>Enable power down PD_AV1 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x1 | pd_rga30_dwn_sftena<br>Enable power down PD_RGA30 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x1 | pd_vdpu_dwn_sftena<br>Enable power down PD_VDPU by software.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x1 | pd_rkvdec1_dwn_sftena<br>Enable power down PD_RKVDEC1 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x1 | pd_rkvdec0_dwn_sftena<br>Enable power down PD_RKVDEC0 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x1 | pd_venc1_dwn_sftena<br>Enable power down PD_VENC1 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x1 | pd_venc0_dwn_sftena<br>Enable power down PD_VENC0 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x1 | pd_npu2_dwn_sftena<br>Enable power down PD_NPU2 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x1 | pd_npu1_dwn_sftena<br>Enable power down PD_NPU1 by software.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x1 | pd_nputop_dwn_sftena<br>Enable power down PD_NPUTOP by software.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | pd_vcodec_dwn_sftena<br>Enable power down VD_VCODEC by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | pd_npu_dwn_sftena<br>Enable power down VD_NPU by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x1 | pd_gpu_dwn_sftena<br>Enable power down VD_GPU by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_PWR_GATE_SFTCON1**

Address: Operational Base + offset (0x8150)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pd_center_dwn_sftena<br>Enable power down PD_CENTER by software.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | pd_crypto_dwn_sftena<br>Enable power down PD_CRYPTO by software.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | pd_sdmmc_dwn_sftena<br>Enable power down PD_SDMMC by software.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | pd_secure_dwn_sftena<br>Enable power down PD_SECURE by software.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | pd_usb_dwn_sftena<br>Enable power down PD_USB by software.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | pd_sdio_dwn_sftena<br>Enable power down PD_SDIO by software.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | pd_nvm0_dwn_sftena<br>Enable power down PD_NVM0 by software.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | pd_nvm_dwn_sftena<br>Enable power down PD_NVM by software.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x1 | pd_pcie_dwn_sftena<br>Enable power down PD_PCIE by software.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x1 | pd_gmac_dwn_sftena<br>Enable power down PD_GMAC by software.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x1 | pd_php_dwn_sftena<br>Enable power down PD_PHP by software.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x1 | pd_audio_dwn_sftena<br>Enable power down PD_AUDIO by software.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x1 | pd_vo1_dwn_sftena<br>Enable power down PD_VO1 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x1 | pd_vo0_dwn_sftena<br>Enable power down PD_VO0 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x1 | pd_vop_dwn_sftena<br>Enable power down PD_VOP by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x1 | pd_rga31_dwn_sftena<br>Enable power down PD_RGA31 by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_PWR_GATE_SFTCON2**

Address: Operational Base + offset (0x8154)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | pd_ddr23_dwn_sftena<br>Enable power down VD_DDR23 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | pd_ddr01_dwn_sftena<br>Enable power down VD_DDR01 by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_VOL_GATE_CON0**

Rockchip Confidencial

Address: Operational Base + offset (0x8158)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:3 | RO | 0x0000 | reserved |
| 2 | RW | 0x0 | vd_vcodec_off_ena<br>Enable power off VD_VCODEC.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | vd_npu_off_ena<br>Enable power off VD_NPU.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | vd_gpu_off_ena<br>Enable power off VD_GPU.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_VOL_GATE_CON1**

Address: Operational Base + offset (0x8160)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | vd_ddr23_off_ena<br>Enable power off VD_DDR23.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | vd_ddr01_off_ena<br>Enable power off VD_DDR01.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_PWR_CHAIN_PWRUP_CON0**

Address: Operational Base + offset (0x8164)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | pd_isp1_pwrup_stable_ena<br>Enable stable counter between power chains for PD_ISP1 power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x1 | pd_fec_pwrup_stable_ena<br>Enable stable counter between power chains for PD_FEC power up flow.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x1 | pd_vi_pwrup_stable_ena<br>Enable stable counter between power chains for PD_VI power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x1 | pd_av1_pwrup_stable_ena<br>Enable stable counter between power chains for PD_AV1 power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x1 | pd_rga30_pwrup_stable_ena<br>Enable stable counter between power chains for PD_RGA30 power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x1 | pd_vdpu_pwrup_stable_ena<br>Enable stable counter between power chains for PD_VDPU power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x1 | pd_rkvdec1_pwrup_stable_ena<br>Enable stable counter between power chains for PD_RKVDEC1 power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x1 | pd_rkvdec0_pwrup_stable_ena<br>Enable stable counter between power chains for PD_RKVDEC0 power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x1 | pd_venc1_pwrup_stable_ena<br>Enable stable counter between power chains for PD_VENC1 power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x1 | pd_venc0_pwrup_stable_ena<br>Enable stable counter between power chains for PD_VENC0 power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x1 | pd_npu2_pwrup_stable_ena<br>Enable stable counter between power chains for PD_NPU2 power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x1 | pd_npu1_pwrup_stable_ena<br>Enable stable counter between power chains for PD_NPU1 power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x1 | pd_nputop_pwrup_stable_ena<br>Enable stable counter between power chains for PD_NPUTOP power up flow.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2:0 | RO | 0x0 | reserved |

**PMU_PWR_CHAIN_PWRUP_CON1**

Address: Operational Base + offset (0x8168)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | pd_center_pwrup_stable_ena<br>Enable stable counter between power chains for PD_CENTER power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x1 | pd_crypto_pwrup_stable_ena<br>Enable stable counter between power chains for PD_CRYPTO power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x1 | pd_sdmmc_pwrup_stable_ena<br>Enable stable counter between power chains for PD_SDMMC power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x1 | pd_secure_pwrup_stable_ena<br>Enable stable counter between power chains for PD_SECURE power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x1 | pd_usb_pwrup_stable_ena<br>Enable stable counter between power chains for PD_USB power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x1 | pd_sdio_pwrup_stable_ena<br>Enable stable counter between power chains for PD_SDIO power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x1 | pd_nvm0_pwrup_stable_ena<br>Enable stable counter between power chains for PD_NVM0 power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x1 | pd_nvm_pwrup_stable_ena<br>Enable stable counter between power chains for PD_NVM power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x1 | pd_pcie_pwrup_stable_ena<br>Enable stable counter between power chains for PD_PCIE power up flow.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x1 | pd_gmac_pwrup_stable_ena<br>Enable stable counter between power chains for PD_GMAC power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x1 | pd_php_pwrup_stable_ena<br>Enable stable counter between power chains for PD_PHP power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x1 | pd_audio_pwrup_stable_ena<br>Enable stable counter between power chains for PD_AUDIO power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x1 | pd_vo1_pwrup_stable_ena<br>Enable stable counter between power chains for PD_VO1 power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x1 | pd_vo0_pwrup_stable_ena<br>Enable stable counter between power chains for PD_VO0 power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x1 | pd_vop_pwrup_stable_ena<br>Enable stable counter between power chains for PD_VOP power up flow.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x1 | pd_rga31_pwrup_stable_ena<br>Enable stable counter between power chains for PD_RGA31 power up flow.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_PWR_CHAIN_PWRDN_CON0**

Address: Operational Base + offset (0x8170)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pd_isp1_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_ISP1 power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | pd_fec_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_FEC power down flow.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | pd_vi_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_VI power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | pd_av1_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_AV1 power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | pd_rga30_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_RGA30 power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | pd_vdpu_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_VDPU power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | pd_rkvdec1_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_RKVDEC1 power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | pd_rkvdec0_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_RKVDEC0 power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | pd_venc1_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_VENC1 power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | pd_venc0_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_VENC0 power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | pd_npu2_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_NPU2 power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | pd_npu1_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_NPU1 power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | pd_nputop_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_NPUTOP power down flow.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2:0 | RO | 0x0 | reserved |

**PMU_PWR_CHAIN_PWRDN_CON1**

Address: Operational Base + offset (0x8174)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pd_center_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_CENTER power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | pd_crypto_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_CRYPTO power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | pd_sdmmc_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_SDMMC power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | pd_secure_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_SECURE power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | pd_usb_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_USB power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | pd_sdio_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_SDIO power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | pd_nvm0_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_NVM0 power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | pd_nvm_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_NVM power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | pd_pcie_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_PCIE power down flow.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | pd_gmac_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_GMAC power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | pd_php_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_PHP power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | pd_audio_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_AUDIO power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | pd_vo1_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_VO1 power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | pd_vo0_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_VO0 power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | pd_vop_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_VOP power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | pd_rga31_pwrdn_stable_ena<br>Enable stable counter between power chains for PD_RGA31 power down flow.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_PWR_STABLE_CNT**

Address: Operational Base + offset (0x817C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x000 | reserved |
| 20:16 | RW | 0x1f | pwrdn_stable_cnt<br>Count for power chain power down stability. Number of clk_pmu used by counter logic. |
| 15:5 | RO | 0x000 | reserved |
| 4:0 | RW | 0x1f | pwrup_stable_cnt<br>Count for power chain power up stability. Number of clk_pmu used by counter logic. |

**PMU_PWR_GATE_STS0**

Address: Operational Base + offset (0x8180)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | pd_center_dwn_stat<br>The power state of PD_CENTER.<br>1'b0: Power up<br>1'b1: Power down |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 30 | RO | 0x0 | pd_crypto_dwn_stat<br>The power state of PD_CRYPTO.<br>1'b0: Power up<br>1'b1: Power down |
| 29 | RO | 0x0 | pd_sdmmc_dwn_stat<br>The power state of PD_SDMMC.<br>1'b0: Power up<br>1'b1: Power down |
| 28 | RO | 0x0 | pd_secure_dwn_stat<br>The power state of PD_SECURE.<br>1'b0: Power up<br>1'b1: Power down |
| 27 | RO | 0x0 | pd_usb_dwn_stat<br>The power state of PD_USB.<br>1'b0: Power up<br>1'b1: Power down |
| 26 | RO | 0x0 | pd_sdio_dwn_stat<br>The power state of PD_SDIO.<br>1'b0: Power up<br>1'b1: Power down |
| 25 | RO | 0x0 | pd_nvm0_dwn_stat<br>The power state of PD_NVM0.<br>1'b0: Power up<br>1'b1: Power down |
| 24 | RO | 0x0 | pd_nvm_dwn_stat<br>The power state of PD_NVM.<br>1'b0: Power up<br>1'b1: Power down |
| 23 | RO | 0x1 | pd_pcie_dwn_stat<br>The power state of PD_PCIE.<br>1'b0: Power up<br>1'b1: Power down |
| 22 | RO | 0x1 | pd_gmac_dwn_stat<br>The power state of PD_GMAC.<br>1'b0: Power up<br>1'b1: Power down |
| 21 | RO | 0x1 | pd_php_dwn_stat<br>The power state of PD_PHP.<br>1'b0: Power up<br>1'b1: Power down |
| 20 | RO | 0x1 | pd_audio_dwn_stat<br>The power state of PD_AUDIO.<br>1'b0: Power up<br>1'b1: Power down |
| 19 | RO | 0x1 | pd_vo1_dwn_stat<br>The power state of PD_VO1.<br>1'b0: Power up<br>1'b1: Power down |
| 18 | RO | 0x1 | pd_vo0_dwn_stat<br>The power state of PD_VO0.<br>1'b0: Power up<br>1'b1: Power down |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17 | RO | 0x1 | pd_vop_dwn_stat<br>The power state of PD_VOP.<br>1'b0: Power up<br>1'b1: Power down |
| 16 | RO | 0x1 | pd_rga31_dwn_stat<br>The power state of PD_RGA31.<br>1'b0: Power up<br>1'b1: Power down |
| 15 | RO | 0x1 | pd_isp1_dwn_stat<br>The power state of PD_ISP1.<br>1'b0: Power up<br>1'b1: Power down |
| 14 | RO | 0x1 | pd_fec_dwn_stat<br>The power state of PD_FEC.<br>1'b0: Power up<br>1'b1: Power down |
| 13 | RO | 0x1 | pd_vi_dwn_stat<br>The power state of PD_VI.<br>1'b0: Power up<br>1'b1: Power down |
| 12 | RO | 0x1 | pd_av1_dwn_stat<br>The power state of PD_AV1.<br>1'b0: Power up<br>1'b1: Power down |
| 11 | RO | 0x1 | pd_rga30_dwn_stat<br>The power state of PD_RGA30.<br>1'b0: Power up<br>1'b1: Power down |
| 10 | RO | 0x1 | pd_vdpu_dwn_stat<br>The power state of PD_VDPU.<br>1'b0: Power up<br>1'b1: Power down |
| 9 | RO | 0x1 | pd_rkvdec1_dwn_stat<br>The power state of PD_RKVDEC1.<br>1'b0: Power up<br>1'b1: Power down |
| 8 | RO | 0x1 | pd_rkvdec0_dwn_stat<br>The power state of PD_RKVDEC0.<br>1'b0: Power up<br>1'b1: Power down |
| 7 | RO | 0x1 | pd_venc1_dwn_stat<br>The power state of PD_VENC1.<br>1'b0: Power up<br>1'b1: Power down |
| 6 | RO | 0x1 | pd_venc0_dwn_stat<br>The power state of PD_VENC0.<br>1'b0: Power up<br>1'b1: Power down |
| 5 | RO | 0x1 | pd_npu2_dwn_stat<br>The power state of PD_NPU2.<br>1'b0: Power up<br>1'b1: Power down |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RO | 0x1 | pd_npu1_dwn_stat<br>The power state of PD_NPU1.<br>1'b0: Power up<br>1'b1: Power down |
| 3 | RO | 0x1 | pd_nputop_dwn_stat<br>The power state of PD_NPUTOP.<br>1'b0: Power up<br>1'b1: Power down |
| 2 | RO | 0x0 | pd_vcodec_dwn_stat<br>The power state of VD_VCODEC.<br>1'b0: Power up<br>1'b1: Power down |
| 1 | RO | 0x0 | pd_npu_dwn_stat<br>The power state of VD_NPU.<br>1'b0: Power up<br>1'b1: Power down |
| 0 | RO | 0x1 | pd_gpu_dwn_stat<br>The power state of VD_GPU.<br>1'b0: Power up<br>1'b1: Power down |

**PMU_PWR_GATE_STS1**

Address: Operational Base + offset (0x8184)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RO | 0x0 | pd_ddr23_dwn_stat<br>The power state of VD_DDR23.<br>1'b0: Power up<br>1'b1: Power down |
| 0 | RO | 0x0 | pd_ddr01_dwn_stat<br>The power state of VD_DDR01.<br>1'b0: Power up<br>1'b1: Power down |

**PMU_PWR_GATE_POWER_STS**

Address: Operational Base + offset (0x8188)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2:0 | RO | 0x0 | power_gate_state<br>Power gating state.<br>3'h0: Normal state<br>3'h1: Power down start state<br>3'h2: Power down running state<br>3'h3: Wait for power up state<br>3'h4: Power up start state<br>3'h5: Power up running state<br>Others: Reserved |

**PMU_VOL_GATE_FAST_CON**

Address: Operational Base + offset (0x818C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | vd_npu_fast_ena<br>Enable VD_NPU fast power control.<br>When asserted, it means that VD_NPU will power up completely if VD_NPU power up count from npu_pwrup_cnt (defined in PMU_NPU_PWRUP_CNT) to zero when VD_NPU power up request active, or VD_NPU will power down completely if VD_NPU power down count from npu_pwrdn_cnt (defined in PMU_NPU_PWRDN_CNT) to zero when VD_NPU power down request active.<br>Otherwise, it means that VD_NPU will power up completely as soon as VD_NPU power up request active, or power down completely as soon as VD_NPU power down request active.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | vd_gpu_fast_ena<br>Enable VD_GPU fast power control.<br>When asserted, it means that VD_GPU will power up completely if VD_GPU power up count from gpu_pwrup_cnt (defined in PMU_GPU_PWRUP_CNT) to zero when VD_GPU power up request active, or VD_GPU will power down completely if VD_GPU power down count from gpu_pwrdn_cnt (defined in PMU_GPU_PWRDN_CNT) to zero when VD_GPU power down request active.<br>Otherwise, it means that VD_GPU will power up completely as soon as VD_GPU power up request active, or power down completely as soon as VD_GPU power down request active.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_GPU_PWRUP_CNT**

Address: Operational Base + offset (0x8190)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfffff | gpu_pwrup_cnt<br>VD_GPU power up count. Number of clk_pmu used by counter logic. |

**PMU_GPU_PWRDN_CNT**

Address: Operational Base + offset (0x8194)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfffff | gpu_pwrdn_cnt<br>VD_GPU power down count. Number of clk_pmu used by counter logic. |

**PMU_NPU_PWRUP_CNT**

Address: Operational Base + offset (0x8198)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfffff | npu_pwrup_cnt<br>VD_NPU power up count. Number of clk_pmu used by counter logic. |

**PMU_NPU_PWRDN_CNT**

Rockchip Confidential

Address: Operational Base + offset (0x819C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0xfffff | npu_pwrdn_cnt<br>VD_NPU power down count. Number of clk_pmu used by counter logic. |

**PMU_MEM_PWR_GATE_SFTCON0**

Address: Operational Base + offset (0x81A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pd_isp1_mem_dwn_sftena<br>Enable power down PD_ISP1's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | pd_fec_mem_dwn_sftena<br>Enable power down PD_FEC's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | pd_vi_mem_dwn_sftena<br>Enable power down PD_VI's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | pd_av1_mem_dwn_sftena<br>Enable power down PD_AV1's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | pd_rga30_mem_dwn_sftena<br>Enable power down PD_RGA30's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RO | 0x0 | reserved |
| 9 | RW | 0x0 | pd_rkvdec1_mem_dwn_sftena<br>Enable power down PD_RKVDEC1's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | pd_rkvdec0_mem_dwn_sftena<br>Enable power down PD_RKVDEC0's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | pd_venc1_mem_dwn_sftena<br>Enable power down PD_VENC1's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | pd_venc0_mem_dwn_sftena<br>Enable power down PD_VENC0's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | pd_npu2_mem_dwn_sftena<br>Enable power down PD_NPU2's memory by software.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | pd_npu1_mem_dwn_sftena<br>Enable power down PD_NPU1's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | pd_nputop_mem_dwn_sftena<br>Enable power down PD_NPUTOP's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 2:0 | RO | 0x0 | reserved |

**PMU_MEM_PWR_GATE_SFTCON1**

Address: Operational Base + offset (0x81A4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pd_center_mem_dwn_sftena<br>Enable power down PD_CENTER's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | pd_crypto_mem_dwn_sftena<br>Enable power down PD_CRYPTO's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | pd_sdmmc_mem_dwn_sftena<br>Enable power down PD_SDMMC's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | pd_usb_mem_dwn_sftena<br>Enable power down PD_USB's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | pd_sdio_mem_dwn_sftena<br>Enable power down PD_SDIO's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | pd_nvm0_mem_dwn_sftena<br>Enable power down PD_NVM0's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RO | 0x0 | reserved |
| 7 | RW | 0x0 | pd_pcie_mem_dwn_sftena<br>Enable power down PD_PCIE's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | pd_gmac_mem_dwn_sftena<br>Enable power down PD_GMAC's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | pd_php_mem_dwn_sftena<br>Enable power down PD_PHP's memory by software.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | pd_audio_mem_dwn_sftena<br>Enable power down PD_AUDIO's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | pd_vo1_mem_dwn_sftena<br>Enable power down PD_VO1's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | pd_vo0_mem_dwn_sftena<br>Enable power down PD_VO0's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | pd_vop_mem_dwn_sftena<br>Enable power down PD_VOP's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | pd_rga31_mem_dwn_sftena<br>Enable power down PD_RGA31's memory by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_MEM_PWR_GATE_SFTCON2**

Address: Operational Base + offset (0x81A8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | pd_ddr23_mem_dwn_sftena<br>Enable power down VD_DDR23's memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | pd_ddr01_mem_dwn_sftena<br>Enable power down VD_DDR01's memory by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_SUBMEM_PWR_GATE_SFTCON0**

Address: Operational Base + offset (0x81B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | shrm_blk3_ds_ctrl<br>Control share memory block 3 deep sleep mode by software.<br>1'b0: Invalid<br>1'b1: Valid |
| 14 | RW | 0x0 | shrm_blk2_ds_ctrl<br>Control share memory block 2 deep sleep mode by software.<br>1'b0: Invalid<br>1'b1: Valid |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | shrm_blk1_ds_ctrl<br>Control share memory block 1 deep sleep mode by software.<br>1'b0: Invalid<br>1'b1: Valid |
| 12 | RW | 0x0 | shrm_blk0_ds_ctrl<br>Control share memory block 0 deep sleep mode by software.<br>1'b0: Invalid<br>1'b1: Valid |
| 11 | RW | 0x0 | shrm_blk3_sd_ctrl<br>Control share memory block 3 shutdown mode by software.<br>1'b0: Invalid<br>1'b1: Valid |
| 10 | RW | 0x0 | shrm_blk2_sd_ctrl<br>Control share memory block 2 shutdown mode by software.<br>1'b0: Invalid<br>1'b1: Valid |
| 9 | RW | 0x0 | shrm_blk1_sd_ctrl<br>Control share memory block 1 shutdown mode by software.<br>1'b0: Invalid<br>1'b1: Valid |
| 8 | RW | 0x0 | shrm_blk0_sd_ctrl<br>Control share memory block 0 shutdown mode by software.<br>1'b0: Invalid<br>1'b1: Valid |
| 7 | RW | 0x0 | shrm_blk3_ds_ena<br>Enable share memory block 3 deep sleep mode by software.<br>1'b0: Disable<br>1'b1: Enable<br>It should be set to 1 before shrm_blk3_ds_ctrl set to 1, and set to 0 after shrm_blk3_ds_ctrl set to 0. |
| 6 | RW | 0x0 | shrm_blk2_ds_ena<br>Enable share memory block 2 deep sleep mode by software.<br>1'b0: Disable<br>1'b1: Enable<br>It should be set to 1 before shrm_blk2_ds_ctrl set to 1, and set to 0 after shrm_blk2_ds_ctrl set to 0. |
| 5 | RW | 0x0 | shrm_blk1_ds_ena<br>Enable share memory block 1 deep sleep mode by software.<br>1'b0: Disable<br>1'b1: Enable<br>It should be set to 1 before shrm_blk1_ds_ctrl set to 1, and set to 0 after shrm_blk1_ds_ctrl set to 0. |
| 4 | RW | 0x0 | shrm_blk0_ds_ena<br>Enable share memory block 0 deep sleep mode by software.<br>1'b0: Disable<br>1'b1: Enable<br>It should be set to 1 before shrm_blk0_ds_ctrl set to 1, and set to 0 after shrm_blk0_ds_ctrl set to 0. |
| 3 | RW | 0x0 | shrm_blk3_sd_ena<br>Enable share memory block 3 shutdown mode by software.<br>1'b0: Disable<br>1'b1: Enable<br>It should be set to 1 before shrm_blk3_sd_ctrl set to 1, and set to 0 after shrm_blk3_sd_ctrl set to 0. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | shrm_blk2_sd_ena<br>Enable share memory block 2 shutdown mode by software.<br>1'b0: Disable<br>1'b1: Enable<br>It should be set to 1 before shrm_blk2_sd_ctrl set to 1, and set to 0 after shrm_blk2_sd_ctrl set to 0. |
| 1 | RW | 0x0 | shrm_blk1_sd_ena<br>Enable share memory block 1 shutdown mode by software.<br>1'b0: Disable<br>1'b1: Enable<br>It should be set to 1 before shrm_blk1_sd_ctrl set to 1, and set to 0 after shrm_blk1_sd_ctrl set to 0. |
| 0 | RW | 0x0 | shrm_blk0_sd_ena<br>Enable share memory block 0 shutdown mode by software.<br>1'b0: Disable<br>1'b1: Enable<br>It should be set to 1 before shrm_blk0_sd_ctrl set to 1, and set to 0 after shrm_blk0_sd_ctrl set to 0. |

**PMU_SUBMEM_PWR_GATE_SFTCON1**

Address: Operational Base + offset (0x81B4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | voppost0_mem_dwn_sftena<br>Enable shutdown VOPPOST0 memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | jpegenc3_mem_dwn_sftena<br>Enable shutdown JPEGENC3 memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | jpegenc2_mem_dwn_sftena<br>Enable shutdown JPEGENC2 memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | jpegenc1_mem_dwn_sftena<br>Enable shutdown JPEGENC1 memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | jpegenc0_mem_dwn_sftena<br>Enable shutdown JPEGENC0 memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | jpegdec_mem_dwn_sftena<br>Enable shutdown JPEGDEC memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | iep_mem_dwn_sftena<br>Enable shutdown IEP memory by software.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | rga2_mem_dwn_sftena<br>Enable shutdown RGA2 memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | vdpu_mem_dwn_sftena<br>Enable shutdown VDPU memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | usb3_mem_dwn_sftena<br>Enable shutdown USB3OTG_2 memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | sata_mem_dwn_sftena<br>Enable shutdown SATA_0/1/2 memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | phpmmu_mem_dwn_sftena<br>Enable shutdown PHPMMU memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | pciemmu_mem_dwn_sftena<br>Enable shutdown PCIEMMU memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | pcie1l2_mem_dwn_sftena<br>Enable shutdown PCIE3_1L2 memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | pcie1l1_mem_dwn_sftena<br>Enable shutdown PCIE3_1L1 memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | pcie1l0_mem_dwn_sftena<br>Enable shutdown PCIE3_1L0 memory by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_SUBMEM_PWR_GATE_SFTCON2**

Address: Operational Base + offset (0x81B8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | dsihost1_mem_dwn_sftena<br>Enable shutdown DSIHOST1 memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | dsihost0_mem_dwn_sftena<br>Enable shutdown DSIHOST0 memory by software.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | vopwb_mem_dwn_sftena<br>Enable shutdown VOPWB memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | vopdolby3_mem_dwn_sftena<br>Enable shutdown VOPDOLBY3 memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | vopdolby2_mem_dwn_sftena<br>Enable shutdown VOPDOLBY2 memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | vopdolby1_mem_dwn_sftena<br>Enable shutdown VOPDOLBY1 memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | voppost3_mem_dwn_sftena<br>Enable shutdown VOPPOST3 memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | voppost2_mem_dwn_sftena<br>Enable shutdown VOPPOST2 memory by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | voppost1_mem_dwn_sftena<br>Enable shutdown VOPPOST1 memory by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_SUBMEM_PWR_GATE_STS**

Address: Operational Base + offset (0x81BC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28 | RO | 0x0 | dsihost1_mem_dwn_stat<br>DSIHOST1 memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 27 | RO | 0x0 | dsihost0_mem_dwn_stat<br>DSIHOST0 memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 26 | RO | 0x0 | vopwb_mem_dwn_stat<br>VOPWB memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 25 | RO | 0x0 | vopdolby3_mem_dwn_stat<br>VOPDOLBY3 memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 24 | RO | 0x0 | vopdolby2_mem_dwn_stat<br>VOPDOLBY2 memory power status.<br>1'b0: Power up<br>1'b1: Power down |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23 | RO | 0x0 | vopdolby1_mem_dwn_stat<br>VOPDOLBY1 memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 22 | RO | 0x0 | voppost3_mem_dwn_stat<br>VOPPOST3 memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 21 | RO | 0x0 | voppost2_mem_dwn_stat<br>VOPPOST2 memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 20 | RO | 0x0 | voppost1_mem_dwn_stat<br>VOPPOST1 memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 19 | RO | 0x0 | voppost0_mem_dwn_stat<br>VOPPOST0 memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 18 | RO | 0x0 | jpegenc3_mem_dwn_stat<br>JPEGENC3 memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 17 | RO | 0x0 | jpegenc2_mem_dwn_stat<br>JPEGENC2 memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 16 | RO | 0x0 | jpegenc1_mem_dwn_stat<br>JPEGENC1 memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 15 | RO | 0x0 | jpegenc0_mem_dwn_stat<br>JPEGENC0 memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 14 | RO | 0x0 | jpegdec_mem_dwn_stat<br>JPEGDEC memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 13 | RO | 0x0 | iep_mem_dwn_stat<br>IEP memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 12 | RO | 0x0 | rga2_mem_dwn_stat<br>RGA2 memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 11 | RO | 0x0 | vdpu_mem_dwn_stat<br>VDPU memory power status.<br>1'b0: Power up<br>1'b1: Power down |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10 | RO | 0x0 | usb3_mem_dwn_stat<br>USB3OTG_2 memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 9 | RO | 0x0 | sata_mem_dwn_stat<br>SATA_0/1/2 memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 8 | RO | 0x0 | phpmmu_mem_dwn_stat<br>PHPMMU memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 7 | RO | 0x0 | pciemmu_mem_dwn_stat<br>PCIEMMU memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 6 | RO | 0x0 | pcie1l2_mem_dwn_stat<br>PCIE3_1L2 memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 5 | RO | 0x0 | pcie1l1_mem_dwn_stat<br>PCIE3_1L1 memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 4 | RO | 0x0 | pcie1l0_mem_pwr_stat<br>PCIE3_1L0 memory power status.<br>1'b0: Power up<br>1'b1: Power down |
| 3 | RO | 0x0 | shrm_blk3_pwr_stat<br>Share memory block 3 power status.<br>1'b0: Power up<br>1'b1: Power down |
| 2 | RO | 0x0 | shrm_blk2_pwr_stat<br>Share memory block 2 power status.<br>1'b0: Power up<br>1'b1: Power down |
| 1 | RO | 0x0 | shrm_blk1_pwr_stat<br>Share memory block 1 power status.<br>1'b0: Power up<br>1'b1: Power down |
| 0 | RO | 0x0 | shrm_blk0_pwr_stat<br>Share memory block 0 power status.<br>1'b0: Power up<br>1'b1: Power down |

**PMU_SUBMEM_PWR_ACK_BYPASS_CON0**

Address: Operational Base + offset (0x81C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x0 | voppost0_mem_pwr_ack_bypass_ena<br>Enable bypass VOPPOST0 memory power up or power down acknowledge. If asserted, it does not need to wait for VOPPOST0 memory power up or power down acknowledge for PD_VOP power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | jpegenc3_mem_pwr_ack_bypass_ena<br>Enable bypass JPEGENC3 memory power up or power down acknowledge. If asserted, it does not need to wait for JPEGENC3 memory power up or power down acknowledge for PD_VDPU power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | jpegenc2_mem_pwr_ack_bypass_ena<br>Enable bypass JPEGENC2 memory power up or power down acknowledge. If asserted, it does not need to wait for JPEGENC2 memory power up or power down acknowledge for PD_VDPU power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | jpegenc1_mem_pwr_ack_bypass_ena<br>Enable bypass JPEGENC1 memory power up or power down acknowledge. If asserted, it does not need to wait for JPEGENC1 memory power up or power down acknowledge for PD_VDPU power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | jpegenc0_mem_pwr_ack_bypass_ena<br>Enable bypass JPEGENC0 memory power up or power down acknowledge. If asserted, it does not need to wait for JPEGENC0 memory power up or power down acknowledge for PD_VDPU power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | jpegdec_mem_pwr_ack_bypass_ena<br>Enable bypass JPEGDEC memory power up or power down acknowledge. If asserted, it does not need to wait for JPEGDEC memory power up or power down acknowledge for PD_VDPU power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | iep_mem_pwr_ack_bypass_ena<br>Enable bypass IEP memory power up or power down acknowledge. If asserted, it does not need to wait for IEP memory power up or power down acknowledge for PD_VDPU power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | rga2_mem_pwr_ack_bypass_ena<br>Enable bypass RGA2 memory power up or power down acknowledge. If asserted, it does not need to wait for RGA2 memory power up or power down acknowledge for PD_VDPU power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | vdpu_mem_pwr_ack_bypass_ena<br>Enable bypass VDPU memory power up or power down acknowledge. If asserted, it does not need to wait for VDPU memory power up or power down acknowledge for PD_VDPU power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | usb3_mem_pwr_ack_bypass_ena<br>Enable bypass USB3OTG_2 memory power up or power down acknowledge. If asserted, it does not need to wait for USB3OTG_2 memory power up or power down acknowledge for PD_PHP power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | sata_mem_pwr_ack_bypass_ena<br>Enable bypass SATA_0/1/2 memory power up or power down acknowledge. If asserted, it does not need to wait for SATA_0/1/2 memory power up or power down acknowledge for PD_PHP power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | phpmmu_mem_pwr_ack_bypass_ena<br>Enable bypass PHPMMU memory power up or power down acknowledge. If asserted, it does not need to wait for PHPMMU memory power up or power down acknowledge for PD_PHP power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | pciemmu_mem_pwr_ack_bypass_ena<br>Enable bypass PCIEMMU memory power up or power down acknowledge. If asserted, it does not need to wait for PCIEMMU memory power up or power down acknowledge for PD_PHP power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | pcie1l2_mem_pwr_ack_bypass_ena<br>Enable bypass PCIE3_1L2 memory power up or power down acknowledge. If asserted, it does not need to wait for PCIE3_1L2 memory power up or power down acknowledge for PD_PHP power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | pcie1l1_mem_pwr_ack_bypass_ena<br>Enable bypass PCIE3_1L1 memory power up or power down acknowledge. If asserted, it does not need to wait for PCIE3_1L1 memory power up or power down acknowledge for PD_PHP power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | pcie1l0_mem_pwr_ack_bypass_ena<br>Enable bypass PCIE3_1L0 memory power up or power down acknowledge. If asserted, it does not need to wait for PCIE3_1L0 memory power up or power down acknowledge for PD_PHP power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_SUBMEM_PWR_ACK_BYPASS_CON1**

Address: Operational Base + offset (0x81C4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | shrm_blk3_dwn_ack_bypass_ena<br>Enable bypass share memory block3 memory power up or power down acknowledge. If asserted, it does not need to wait for share memory block3 memory power up or power down acknowledge for PD_CENTER power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | shrm_blk2_dwn_ack_bypass_ena<br>Enable bypass share memory block2 memory power up or power down acknowledge. If asserted, it does not need to wait for share memory block2 memory power up or power down acknowledge for PD_CENTER power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | shrm_blk1_dwn_ack_bypass_ena<br>Enable bypass share memory block1 memory power up or power down acknowledge. If asserted, it does not need to wait for share memory block1 memory power up or power down acknowledge for PD_CENTER power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | shrm_blk0_dwn_ack_bypass_ena<br>Enable bypass share memory block0 memory power up or power down acknowledge. If asserted, it does not need to wait for share memory block0 memory power up or power down acknowledge for PD_CENTER power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | dsihost1_mem_pwr_ack_bypass_ena<br>Enable bypass DSIHOST1 memory power up or power down acknowledge. If asserted, it does not need to wait for DSIHOST1 memory power up or power down acknowledge for PD_VOP power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | dsihost0_mem_pwr_ack_bypass_ena<br>Enable bypass DSIHOST0 memory power up or power down acknowledge. If asserted, it does not need to wait for DSIHOST0 memory power up or power down acknowledge for PD_VOP power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | vopwb_mem_pwr_ack_bypass_ena<br>Enable bypass VOPWB memory power up or power down acknowledge. If asserted, it does not need to wait for VOPWB memory power up or power down acknowledge for PD_VOP power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | vopdolby3_mem_pwr_ack_bypass_ena<br>Enable bypass VOPDOLBY3 memory power up or power down acknowledge. If asserted, it does not need to wait for VOPDOLBY3 memory power up or power down acknowledge for PD_VOP power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | vopdolby2_mem_pwr_ack_bypass_ena<br>Enable bypass VOPDOLBY2 memory power up or power down acknowledge. If asserted, it does not need to wait for VOPDOLBY2 memory power up or power down acknowledge for PD_VOP power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | vopdolby1_mem_pwr_ack_bypass_ena<br>Enable bypass VOPDOLBY1 memory power up or power down acknowledge. If asserted, it does not need to wait for VOPDOLBY1 memory power up or power down acknowledge for PD_VOP power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | voppost3_mem_pwr_ack_bypass_ena<br>Enable bypass VOPPOST3 memory power up or power down acknowledge. If asserted, it does not need to wait for VOPPOST3 memory power up or power down acknowledge for PD_VOP power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | voppost2_mem_pwr_ack_bypass_ena<br>Enable bypass VOPPOST2 memory power up or power down acknowledge. If asserted, it does not need to wait for VOPPOST2 memory power up or power down acknowledge for PD_VOP power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | voppost1_dwn_ack_bypass_ena<br>Enable bypass VOPPOST1 memory power up or power down acknowledge. If asserted, it does not need to wait for VOPPOST1 memory power up or power down acknowledge for PD_VOP power up or power down flow.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_QCHANNEL_PWR_CON**

Address: Operational Base + offset (0x81D0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x0 | busgic_its1_qch_ena<br>Enable BUSGIC-ITS1 Q-Channel power control by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | busgic_its0_qch_ena<br>Enable BUSGIC-ITS0 Q-Channel power control by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | phpgic_its_qch_ena<br>Enable PHPGIC-ITS Q-Channel power control by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | pciemmu_tcu_qch_ena<br>Enable PCIEMMU-TCU Q-Channel power control by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | pciemmu_tbu_qch_ena<br>Enable PCIEMMU-TBU Q-Channel power control by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | phpmmu_tcu_qch_ena<br>Enable PHPMMU-TCU Q-Channel power control by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | phpmmu_tbu_qch_ena<br>Enable PHPMMU-TBU Q-Channel power control by hardware.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_QCHANNEL_PWR_SFTCON**

Address: Operational Base + offset (0x81D4)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:7 | RO | 0x000 | reserved |
| 6 | RW | 0x0 | busgic_its1_qch_sftena<br>Enable BUSGIC-ITS1 Q-Channel power control by software.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | busgic_its0_qch_sftena<br>Enable BUSGIC-ITS0 Q-Channel power control by software.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | phpgic_its_qch_sftena<br>Enable PHPGIC-ITS Q-Channel power control by software.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | pciemmu_tcu_qch_sftena<br>Enable PCIEMMU-TCU Q-Channel power control by software.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | pciemmu_tbu_qch_sftena<br>Enable PCIEMMU-TBU Q-Channel power control by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | phpmmu_tcu_qch_sftena<br>Enable PHPMMU-TCU Q-Channel power control by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | phpmmu_tbu_qch_sftena<br>Enable PHPMMU-TBU Q-Channel power control by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_QCHANNEL_PWR_STS**

Address: Operational Base + offset (0x81D8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27 | RO | 0x0 | busgic_its1_qch_req<br>Request status for BUSGIC-ITS1 Q-Channel power control.<br>1'b0: Not valid request<br>1'b1: Valid request |
| 26 | RO | 0x0 | busgic_its0_qch_req<br>Request status for BUSGIC-ITS0 Q-Channel power control.<br>1'b0: Not valid request<br>1'b1: Valid request |
| 25 | RO | 0x0 | phpgic_its_qch_req<br>Request status for PHPGIC-ITS Q-Channel power control.<br>1'b0: Not valid request<br>1'b1: Valid request |
| 24 | RO | 0x0 | pciemmu_tcu_qch_req<br>Request status for PCIEMMU-TCU Q-Channel power control.<br>1'b0: Not valid request<br>1'b1: Valid request |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23 | RO | 0x0 | pciemmu_tbu_qch_req<br>Request status for PCIEMMU-TBU Q-Channel power control.<br>1'b0: Not valid request<br>1'b1: Valid request |
| 22 | RO | 0x0 | phpmmu_tcu_qch_req<br>Request status for PHPMMU-TCU Q-Channel power control.<br>1'b0: Not valid request<br>1'b1: Valid request |
| 21 | RO | 0x0 | phpmmu_tbu_qch_req<br>Request status for PHPMMU-TBU Q-Channel power control.<br>1'b0: Not valid request<br>1'b1: Valid request |
| 20 | RO | 0x0 | busgic_its1_qch_active<br>Active status for PHPBUS-ITS1 Q-Channel power control.<br>1'b0: Inactive<br>1'b1: Active |
| 19 | RO | 0x0 | busgic_its0_qch_active<br>Active status for PHPBUS-ITS0 Q-Channel power control.<br>1'b0: Inactive<br>1'b1: Active |
| 18 | RO | 0x0 | phpgic_its_qch_active<br>Active status for PHPGIC-ITS Q-Channel power control.<br>1'b0: Inactive<br>1'b1: Active |
| 17 | RO | 0x0 | pciemmu_tcu_qch_active<br>Active status for PCIEMMU-TCU Q-Channel power control.<br>1'b0: Inactive<br>1'b1: Active |
| 16 | RO | 0x0 | pciemmu_tbu_qch_active<br>Active status for PCIEMMU-TBU Q-Channel power control.<br>1'b0: Inactive<br>1'b1: Active |
| 15 | RO | 0x0 | phpmmu_tcu_qch_active<br>Active status for PHPMMU-TCU Q-Channel power control.<br>1'b0: Inactive<br>1'b1: Active |
| 14 | RO | 0x0 | phpmmu_tbu_qch_active<br>Active status for PHPMMU-TBU Q-Channel power control.<br>1'b0: Inactive<br>1'b1: Active |
| 13 | RO | 0x0 | busgic_its1_qch_deny<br>Deny status for PBUSGIC-ITS1 Q-Channel power control.<br>1'b0: Not deny<br>1'b1: Deny |
| 12 | RO | 0x0 | busgic_its0_qch_deny<br>Deny status for BUSGIC-ITS0 Q-Channel power control.<br>1'b0: Not deny<br>1'b1: Deny |
| 11 | RO | 0x0 | phpgic_its_qch_deny<br>Deny status for PHPGIC-ITS Q-Channel power control.<br>1'b0: Not deny<br>1'b1: Deny |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10 | RO | 0x0 | pciemmu_tcu_qch_deny<br>Deny status for PCIEMMU-TCU Q-Channel power control.<br>1'b0: Not deny<br>1'b1: Deny |
| 9 | RO | 0x0 | pciemmu_tbu_qch_deny<br>Deny status for PCIEMMU-TBU Q-Channel power control.<br>1'b0: Not deny<br>1'b1: Deny |
| 8 | RO | 0x0 | phpmmu_tcu_qch_deny<br>Deny status for PHPMMU-TCU Q-Channel power control.<br>1'b0: Not deny<br>1'b1: Deny |
| 7 | RO | 0x0 | phpmmu_tbu_qch_deny<br>Deny status for PHPMMU-TBU Q-Channel power control.<br>1'b0: Not deny<br>1'b1: Deny |
| 6 | RO | 0x0 | busgic_its1_qch_accept<br>Accept status for BUSGIC-ITS1 Q-Channel power control.<br>1'b0: Not accept<br>1'b1: Accept |
| 5 | RO | 0x0 | busgic_its0_qch_accept<br>Accept status for BUSGIC-ITS0 Q-Channel power control.<br>1'b0: Not accept<br>1'b1: Accept |
| 4 | RO | 0x0 | phpgic_its_qch_accept<br>Accept status for PHPGIC-ITS Q-Channel power control.<br>1'b0: Not accept<br>1'b1: Accept |
| 3 | RO | 0x0 | pciemmu_tcu_qch_accept<br>Accept status for PCIEMMU-TCU Q-Channel power control.<br>1'b0: Not accept<br>1'b1: Accept |
| 2 | RO | 0x0 | pciemmu_tbu_qch_accept<br>Accept status for PCIEMMU-TBU Q-Channel power control.<br>1'b0: Not accept<br>1'b1: Accept |
| 1 | RO | 0x0 | phpmmu_tcu_qch_accept<br>Accept status for PHPMMU-TCU Q-Channel power control.<br>1'b0: Not accept<br>1'b1: Accept |
| 0 | RO | 0x0 | phpmmu_tbu_qch_accept<br>Accept status for PHPMMU-TBU Q-Channel power control.<br>1'b0: Not accept<br>1'b1: Accept |

**PMU_DEBUG_INFO_CON**

Address: Operational Base + offset (0x81E0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:11 | RO | 0x00 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10 | RW | 0x0 | cpu_power_state_sel<br>Select CPU power state as debug information output to IO.<br>1'b0: Not select<br>1'b1: Select |
| 9 | RW | 0x0 | core1_power_state_sel<br>Select BIGCORE1 power state as debug information output to IO.<br>1'b0: Not select<br>1'b1: Select |
| 8 | RW | 0x0 | core0_power_state_sel<br>Select BIGCORE0 power state as debug information output to IO.<br>1'b0: Not select<br>1'b1: Select |
| 7 | RW | 0x0 | cpu7_power_state_sel<br>Select CPU7 power state as CPU power state.<br>1'b0: Not select<br>1'b1: Select |
| 6 | RW | 0x0 | cpu6_power_state_sel<br>Select CPU6 power state as CPU power state.<br>1'b0: Not select<br>1'b1: Select |
| 5 | RW | 0x0 | cpu5_power_state_sel<br>Select CPU5 power state as CPU power state.<br>1'b0: Not select<br>1'b1: Select |
| 4 | RW | 0x0 | cpu4_power_state_sel<br>Select CPU4 power state as CPU power state.<br>1'b0: Not select<br>1'b1: Select |
| 3 | RW | 0x0 | cpu3_power_state_sel<br>Select CPU3 power state as CPU power state.<br>1'b0: Not select<br>1'b1: Select |
| 2 | RW | 0x0 | cpu2_power_state_sel<br>Select CPU2 power state as CPU power state.<br>1'b0: Not select<br>1'b1: Select |
| 1 | RW | 0x0 | cpu1_power_state_sel<br>Select CPU1 power state as CPU power state.<br>1'b0: Not select<br>1'b1: Select |
| 0 | RW | 0x0 | cpu0_power_state_sel<br>Select CPU0 power state as CPU power state.<br>1'b0: Not select<br>1'b1: Select |

**PMU_VOP_SUBPD_PWR_CHAIN_STS**

Address: Operational Base + offset (0x81E4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x000 | reserved |
| 20 | RO | 0x0 | vop_dsc8k_c0_pwr_stat<br>PD_VOPDSC8K power chain 0 power state.<br>1'b0: Power down<br>1'b1: Power up |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19 | RO | 0x0 | vop_dsc8k_c1_pwr_stat<br>PD_VOPDSC8K power chain 1 power state.<br>1'b0: Power down<br>1'b1: Power up |
| 18 | RO | 0x1 | vop_dsc8k_mem_pwr_stat<br>PD_VOPDSC8K memory power state.<br>1'b0: Power up<br>1'b1: Power down |
| 17 | RO | 0x0 | vop_dsc4k_c0_pwr_stat<br>PD_VOPDSC4K power chain 0 power state.<br>1'b0: Power down<br>1'b1: Power up |
| 16 | RO | 0x0 | vop_dsc4k_c1_pwr_stat<br>PD_VOPDSC4K power chain 1 power state.<br>1'b0: Power down<br>1'b1: Power up |
| 15 | RO | 0x1 | vop_dsc4k_mem_pwr_stat<br>PD_VOPDSC4K memory power state.<br>1'b0: Power up<br>1'b1: Power down |
| 14 | RO | 0x0 | vop_esmart_c0_pwr_stat<br>PD_VOPESMART power chain 0 power state.<br>1'b0: Power down<br>1'b1: Power up |
| 13 | RO | 0x0 | vop_esmart_c1_pwr_stat<br>PD_VOPESMART power chain 1 power state.<br>1'b0: Power down<br>1'b1: Power up |
| 12 | RO | 0x1 | vop_esmart_mem_pwr_stat<br>PD_VOPESMART memory power state.<br>1'b0: Power up<br>1'b1: Power down |
| 11 | RO | 0x0 | vop_cluster3_c0_pwr_stat<br>PD_VOPCLUSTER3 power chain 0 power state.<br>1'b0: Power down<br>1'b1: Power up |
| 10 | RO | 0x0 | vop_cluster3_c1_pwr_stat<br>PD_VOPCLUSTER3 power chain 1 power state.<br>1'b0: Power down<br>1'b1: Power up |
| 9 | RO | 0x1 | vop_cluster3_mem_pwr_stat<br>PD_VOPCLUSTER3 memory power state.<br>1'b0: Power up<br>1'b1: Power down |
| 8 | RO | 0x0 | vop_cluster2_c0_pwr_stat<br>PD_VOPCLUSTER2 power chain 0 power state.<br>1'b0: Power down<br>1'b1: Power up |
| 7 | RO | 0x0 | vop_cluster2_c1_pwr_stat<br>PD_VOPCLUSTER2 power chain 1 power state.<br>1'b0: Power down<br>1'b1: Power up |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RO | 0x1 | vop_cluster2_mem_pwr_stat<br>PD_VOPCLUSTER2 memory power state.<br>1'b0: Power up<br>1'b1: Power down |
| 5 | RO | 0x0 | vop_cluster1_c0_pwr_stat<br>PD_VOPCLUSTER1 power chain 0 power state.<br>1'b0: Power down<br>1'b1: Power up |
| 4 | RO | 0x0 | vop_cluster1_c1_pwr_stat<br>PD_VOPCLUSTER1 power chain 1 power state.<br>1'b0: Power down<br>1'b1: Power up |
| 3 | RO | 0x1 | vop_cluster1_mem_pwr_stat<br>PD_VOPCLUSTER1 memory power state.<br>1'b0: Power up<br>1'b1: Power down |
| 2 | RO | 0x0 | vop_cluster0_c0_pwr_stat<br>PD_VOPCLUSTER0 power chain 0 power state.<br>1'b0: Power down<br>1'b1: Power up |
| 1 | RO | 0x0 | vop_cluster0_c1_pwr_stat<br>PD_VOPCLUSTER0 power chain 1 power state.<br>1'b0: Power down<br>1'b1: Power up |
| 0 | RO | 0x1 | vop_cluster0_mem_pwr_stat<br>PD_VOPCLUSTER0 memory power state.<br>1'b0: Power up<br>1'b1: Power down |

**PMU_PWR_CHAIN0_STS0**

Address: Operational Base + offset (0x81E8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | pd_pcie_c0_pwr_stat<br>The power state of PD_PCIE power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 30 | RO | 0x0 | pd_gmac_c0_pwr_stat<br>The power state of PD_GMAC power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 29 | RO | 0x0 | pd_php_c0_pwr_stat<br>The power state of PD_PHP power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 28 | RO | 0x0 | pd_audio_c0_pwr_stat<br>The power state of PD_AUDIO power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 27 | RO | 0x0 | pd_vo1_c0_pwr_stat<br>The power state of PD_VO1 power chain 0.<br>1'b0: Power down<br>1'b1: Power up |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 26 | RO | 0x0 | pd_vo0_c0_pwr_stat<br>The power state of PD_VO0 power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 25 | RO | 0x0 | pd_vop_c0_pwr_stat<br>The power state of PD_VOP power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 24 | RO | 0x0 | pd_rga31_c0_pwr_stat<br>The power state of PD_RGA31 power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 23 | RO | 0x0 | pd_isp1_c0_pwr_stat<br>The power state of PD_ISP1 power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 22 | RO | 0x0 | pd_fec_c0_pwr_stat<br>The power state of PD_FEC power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 21 | RO | 0x0 | pd_vi_c0_pwr_stat<br>The power state of PD_VI power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 20 | RO | 0x0 | pd_av1_c0_pwr_stat<br>The power state of PD_AV1 power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 19 | RO | 0x0 | pd_rga30_c0_pwr_stat<br>The power state of PD_RGA30.<br>1'b0: Power down<br>1'b1: Power up |
| 18 | RO | 0x0 | pd_vdpu_c0_pwr_stat<br>The power state of PD_VDPU power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 17 | RO | 0x0 | pd_rkvdec1_c0_pwr_stat<br>The power state of PD_RKVDEC1 power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 16 | RO | 0x0 | pd_rkvdec0_c0_pwr_stat<br>The power state of PD_RKVDEC0 power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 15 | RO | 0x0 | pd_venc1_c0_pwr_stat<br>The power state of PD_VENC1 power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 14 | RO | 0x0 | pd_venc0_c0_pwr_stat<br>The power state of PD_VENC0 power chain 0.<br>1'b0: Power down<br>1'b1: Power up |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RO | 0x0 | pd_npu2_c0_pwr_stat<br>The power state of PD_NPU2 power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 12 | RO | 0x0 | pd_npu1_c0_pwr_stat<br>The power state of PD_NPU1 power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 11 | RO | 0x0 | pd_nputop_c0_pwr_stat<br>The power state of PD_NPUTOP power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 10:8 | RO | 0x0 | reserved |
| 7 | RO | 0x1 | pd_cpu_7_c0_pwr_stat<br>The power state of PD_CPU_7 power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 6 | RO | 0x1 | pd_cpu_6_c0_pwr_stat<br>The power state of PD_CPU_6 power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 5 | RO | 0x1 | pd_cpu_5_c0_pwr_stat<br>The power state of PD_CPU_5 power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 4 | RO | 0x1 | pd_cpu_4_c0_pwr_stat<br>The power state of PD_CPU_4 power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 3 | RO | 0x1 | pd_cpu_3_c0_pwr_stat<br>The power state of PD_CPU_3 power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 2 | RO | 0x1 | pd_cpu_2_c0_pwr_stat<br>The power state of PD_CPU_2 power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 1 | RO | 0x1 | pd_cpu_1_c0_pwr_stat<br>The power state of PD_CPU_1 power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 0 | RO | 0x1 | pd_cpu_0_c0_pwr_stat<br>The power state of PD_CPU_0 power chain 0.<br>1'b0: Power down<br>1'b1: Power up |

**PMU_PWR_CHAIN0_STS1**

Address: Operational Base + offset (0x81EC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RO | 0x1 | pd_center_c0_pwr_stat<br>The power state of PD_CENTER power chain 0.<br>1'b0: Power down<br>1'b1: Power up |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RO | 0x1 | pd_crypto_c0_pwr_stat<br>The power state of PD_CRYPTO power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 5 | RO | 0x1 | pd_sdmmc_c0_pwr_stat<br>The power state of PD_SDMMC power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 4 | RO | 0x1 | pd_secure_c0_pwr_stat<br>The power state of PD_SECURE power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 3 | RO | 0x1 | pd_usb_c0_pwr_stat<br>The power state of PD_USB power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 2 | RO | 0x1 | pd_sdio_c0_pwr_stat<br>The power state of PD_SDIO power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 1 | RO | 0x1 | pd_nvm0_c0_pwr_stat<br>The power state of PD_NVM0 power chain 0.<br>1'b0: Power down<br>1'b1: Power up |
| 0 | RO | 0x1 | pd_nvm_c0_pwr_stat<br>The power state of PD_NVM power chain 0.<br>1'b0: Power down<br>1'b1: Power up |

**PMU_PWR_CHAIN1_STS0**

Address: Operational Base + offset (0x81F0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | pd_pcie_c1_pwr_stat<br>The power state of PD_PCIE power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 30 | RO | 0x0 | pd_gmac_c1_pwr_stat<br>The power state of PD_GMAC power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 29 | RO | 0x0 | pd_php_c1_pwr_stat<br>The power state of PD_PHP power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 28 | RO | 0x0 | pd_audio_c1_pwr_stat<br>The power state of PD_AUDIO power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 27 | RO | 0x0 | pd_vo1_c1_pwr_stat<br>The power state of PD_VO1 power chain 1.<br>1'b0: Power down<br>1'b1: Power up |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 26 | RO | 0x0 | pd_vo0_c1_pwr_stat<br>The power state of PD_VO0 power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 25 | RO | 0x0 | pd_vop_c1_pwr_stat<br>The power state of PD_VOP power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 24 | RO | 0x0 | pd_rga31_c1_pwr_stat<br>The power state of PD_RGA31 power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 23 | RO | 0x0 | pd_isp1_c1_pwr_stat<br>The power state of PD_ISP1 power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 22 | RO | 0x0 | pd_fec_c1_pwr_stat<br>The power state of PD_FEC power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 21 | RO | 0x0 | pd_vi_c1_pwr_stat<br>The power state of PD_VI power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 20 | RO | 0x0 | pd_av1_c1_pwr_stat<br>The power state of PD_AV1 power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 19 | RO | 0x0 | pd_rga30_c1_pwr_stat<br>The power state of PD_RGA30.<br>1'b0: Power down<br>1'b1: Power up |
| 18 | RO | 0x0 | pd_vdpu_c1_pwr_stat<br>The power state of PD_VDPU power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 17 | RO | 0x0 | pd_rkvdec1_c1_pwr_stat<br>The power state of PD_RKVDEC1 power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 16 | RO | 0x0 | pd_rkvdec0_c1_pwr_stat<br>The power state of PD_RKVDEC0 power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 15 | RO | 0x0 | pd_venc1_c1_pwr_stat<br>The power state of PD_VENC1 power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 14 | RO | 0x0 | pd_venc0_c1_pwr_stat<br>The power state of PD_VENC0 power chain 1.<br>1'b0: Power down<br>1'b1: Power up |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RO | 0x0 | pd_npu2_c1_pwr_stat<br>The power state of PD_NPU2 power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 12 | RO | 0x0 | pd_npu1_c1_pwr_stat<br>The power state of PD_NPU1 power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 11 | RO | 0x0 | pd_nputop_c1_pwr_stat<br>The power state of PD_NPUTOP power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 10:8 | RO | 0x0 | reserved |
| 7 | RO | 0x1 | pd_cpu_7_c1_pwr_stat<br>The power state of PD_CPU_7 power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 6 | RO | 0x1 | pd_cpu_6_c1_pwr_stat<br>The power state of PD_CPU_6 power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 5 | RO | 0x1 | pd_cpu_5_c1_pwr_stat<br>The power state of PD_CPU_5 power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 4 | RO | 0x1 | pd_cpu_4_c1_pwr_stat<br>The power state of PD_CPU_4 power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 3 | RO | 0x1 | pd_cpu_3_c1_pwr_stat<br>The power state of PD_CPU_3 power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 2 | RO | 0x1 | pd_cpu_2_c1_pwr_stat<br>The power state of PD_CPU_2 power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 1 | RO | 0x1 | pd_cpu_1_c1_pwr_stat<br>The power state of PD_CPU_1 power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 0 | RO | 0x1 | pd_cpu_0_c1_pwr_stat<br>The power state of PD_CPU_0 power chain 1.<br>1'b0: Power down<br>1'b1: Power up |

**PMU_PWR_CHAIN1_STS1**

Address: Operational Base + offset (0x81F4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RO | 0x1 | pd_center_c1_pwr_stat<br>The power state of PD_CENTER power chain 1.<br>1'b0: Power down<br>1'b1: Power up |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RO | 0x1 | pd_crypto_c1_pwr_stat<br>The power state of PD_CRYPTO power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 5 | RO | 0x1 | pd_sdmmc_c1_pwr_stat<br>The power state of PD_SDMMC power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 4 | RO | 0x1 | pd_secure_c1_pwr_stat<br>The power state of PD_SECURE power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 3 | RO | 0x1 | pd_usb_c1_pwr_stat<br>The power state of PD_USB power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 2 | RO | 0x1 | pd_sdio_c1_pwr_stat<br>The power state of PD_SDIO power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 1 | RO | 0x1 | pd_nvm0_c1_pwr_stat<br>The power state of PD_NVM0 power chain 1.<br>1'b0: Power down<br>1'b1: Power up |
| 0 | RO | 0x1 | pd_nvm_c1_pwr_stat<br>The power state of PD_NVM power chain 1.<br>1'b0: Power down<br>1'b1: Power up |

**PMU_PWR_MEM_STS0**

Address: Operational Base + offset (0x81F8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x1 | pd_pcie_mem_pwr_stat<br>The power state of PD_PCIE memory.<br>1'b0: Power up<br>1'b1: Power down |
| 30 | RO | 0x1 | pd_gmac_mem_pwr_stat<br>The power state of PD_GMAC memory.<br>1'b0: Power up<br>1'b1: Power down |
| 29 | RO | 0x1 | pd_php_mem_pwr_stat<br>The power state of PD_PHP memory.<br>1'b0: Power up<br>1'b1: Power down |
| 28 | RO | 0x1 | pd_audio_mem_pwr_stat<br>The power state of PD_AUDIO memory.<br>1'b0: Power up<br>1'b1: Power down |
| 27 | RO | 0x1 | pd_vo1_mem_pwr_stat<br>The power state of PD_VO1 memory.<br>1'b0: Power up<br>1'b1: Power down |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 26 | RO | 0x1 | pd_vo0_mem_pwr_stat<br>The power state of PD_VO0 memory.<br>1'b0: Power up<br>1'b1: Power down |
| 25 | RO | 0x1 | pd_vop_mem_pwr_stat<br>The power state of PD_VOP memory.<br>1'b0: Power up<br>1'b1: Power down |
| 24 | RO | 0x1 | pd_rga31_mem_pwr_stat<br>The power state of PD_RGA31 memory.<br>1'b0: Power up<br>1'b1: Power down |
| 23 | RO | 0x1 | pd_isp1_mem_pwr_stat<br>The power state of PD_ISP1 memory.<br>1'b0: Power up<br>1'b1: Power down |
| 22 | RO | 0x1 | pd_fec_mem_pwr_stat<br>The power state of PD_FEC memory.<br>1'b0: Power up<br>1'b1: Power down |
| 21 | RO | 0x1 | pd_vi_mem_pwr_stat<br>The power state of PD_VI memory.<br>1'b0: Power up<br>1'b1: Power down |
| 20 | RO | 0x1 | pd_av1_mem_pwr_stat<br>The power state of PD_AV1 memory.<br>1'b0: Power up<br>1'b1: Power down |
| 19 | RO | 0x1 | pd_rga30_mem_pwr_stat<br>The power state of PD_RGA30 memory.<br>1'b0: Power up<br>1'b1: Power down |
| 18 | RO | 0x0 | reserved |
| 17 | RO | 0x1 | pd_rkvdec1_mem_pwr_stat<br>The power state of PD_RKVDEC1 memory.<br>1'b0: Power up<br>1'b1: Power down |
| 16 | RO | 0x1 | pd_rkvdec0_mem_pwr_stat<br>The power state of PD_RKVDEC0 memory.<br>1'b0: Power up<br>1'b1: Power down |
| 15 | RO | 0x1 | pd_venc1_mem_pwr_stat<br>The power state of PD_VENC1 memory.<br>1'b0: Power up<br>1'b1: Power down |
| 14 | RO | 0x1 | pd_venc0_mem_pwr_stat<br>The power state of PD_VENC0 memory.<br>1'b0: Power up<br>1'b1: Power down |
| 13 | RO | 0x1 | pd_npu2_mem_pwr_stat<br>The power state of PD_NPU2 memory.<br>1'b0: Power up<br>1'b1: Power down |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RO | 0x1 | pd_npu1_mem_pwr_stat<br>The power state of PD_NPU1 memory.<br>1'b0: Power up<br>1'b1: Power down |
| 11 | RO | 0x1 | pd_nputop_mem_pwr_stat<br>The power state of PD_NPUTOP memory.<br>1'b0: Power up<br>1'b1: Power down |
| 10:8 | RO | 0x0 | reserved |
| 7 | RO | 0x0 | pd_cpu_7_mem_pwr_stat<br>The power state of PD_CPU_7 memory.<br>1'b0: Power up<br>1'b1: Power down |
| 6 | RO | 0x0 | pd_cpu_6_mem_pwr_stat<br>The power state of PD_CPU_6 memory.<br>1'b0: Power up<br>1'b1: Power down |
| 5 | RO | 0x0 | pd_cpu_5_mem_pwr_stat<br>The power state of PD_CPU_5 memory.<br>1'b0: Power up<br>1'b1: Power down |
| 4 | RO | 0x0 | pd_cpu_4_mem_pwr_stat<br>The power state of PD_CPU_4 memory.<br>1'b0: Power up<br>1'b1: Power down |
| 3 | RO | 0x0 | pd_cpu_3_mem_pwr_stat<br>The power state of PD_CPU_3 memory.<br>1'b0: Power up<br>1'b1: Power down |
| 2 | RO | 0x0 | pd_cpu_2_mem_pwr_stat<br>The power state of PD_CPU_2 memory.<br>1'b0: Power up<br>1'b1: Power down |
| 1 | RO | 0x0 | pd_cpu_1_mem_pwr_stat<br>The power state of PD_CPU_1 memory.<br>1'b0: Power up<br>1'b1: Power down |
| 0 | RO | 0x0 | pd_cpu_0_mem_pwr_stat<br>The power state of PD_CPU_0 memory.<br>1'b0: Power up<br>1'b1: Power down |

**PMU_PWR_MEM_STS1**

Address: Operational Base + offset (0x81FC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:15 | RO | 0x00000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14:10 | RO | 0x00 | pd_dsu_mem_pwr_stat<br>The power state of VD_LITDSU memory.<br>1'b0: Power up<br>1'b1: Power down<br>Bit[10] used to indicate "Snoop filter and LTDB RAMs" memory power state.<br>Bit[11] used to indicate "L3 Tag ways 0~3, L3 Data portion 0, and L3 Victim RAMs" memory state.<br>Bit[12] used to indicate "L3 Tag ways 4~7" memory power state.<br>Bit[13] used to indicate "L3 Tag ways 8~11, L3 Data portion 1 RAMs" memory power state.<br>Bit[14] used to indicate other memory power state. |
| 9 | RO | 0x0 | pd_ddr23_mem_pwr_stat<br>The power state of VD_DDR23 memory.<br>1'b0: Power up<br>1'b1: Power down |
| 8 | RO | 0x0 | pd_ddr01_mem_pwr_stat<br>The power state of VD_DDR01 memory.<br>1'b0: Power up<br>1'b1: Power down |
| 7 | RO | 0x0 | pd_center_mem_pwr_stat<br>The power state of PD_CENTER memory.<br>1'b0: Power up<br>1'b1: Power down |
| 6 | RO | 0x0 | pd_crypto_mem_pwr_stat<br>The power state of PD_CRYPTO memory.<br>1'b0: Power up<br>1'b1: Power down |
| 5 | RO | 0x0 | pd_sdmmc_mem_pwr_stat<br>The power state of PD_SDMMC memory.<br>1'b0: Power up<br>1'b1: Power down |
| 4 | RO | 0x0 | reserved |
| 3 | RO | 0x0 | pd_usb_mem_pwr_stat<br>The power state of PD_USB memory.<br>1'b0: Power up<br>1'b1: Power down |
| 2 | RO | 0x0 | pd_sdio_mem_pwr_stat<br>The power state of PD_SDIO memory.<br>1'b0: Power up<br>1'b1: Power down |
| 1 | RO | 0x0 | pd_nvm0_mem_pwr_stat<br>The power state of PD_NVM0 memory.<br>1'b0: Power up<br>1'b1: Power down |
| 0 | RO | 0x0 | reserved |

**PMU_BISR_CON0**

Address: Operational Base + offset (0x8200)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:12 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11 | RW | 0x0 | bisr_initrstn_dis<br>Disable initial reset for memory repair logic.<br>1'b0: Enable<br>1'b1: Disable |
| 10 | RW | 0x0 | bisr_sft_ena<br>Enable memory repair control by software.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x1 | bisr_resetn_sft<br>Generate bisr_resetN by software. |
| 8 | RW | 0x0 | bisr_repair_mode<br>Memory repair mode.<br>1'b0: Serial repair mode. In this mode, memory repair will start after power domain is power up, not need to wait for other domain power up. If multi domains are power up at the same time, the repair is executed according to the repair group order.<br>1'b1: Parallel repair mode. In this mode, memory repair will not start until all specified power domains are power up. |
| 7 | RW | 0x0 | bisr_timeout_ena<br>Enable memory repair timeout counter.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | bisr_clkgate_sftena<br>Enable memory repair clock gating by software. If asserted, memory repair clock is gated.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | bisr_clkgate_ena<br>Enable memory repair auto clock gating by hardware. If asserted, memory repair clock is auto gated when memory repair is idle.<br>1'b0: Disable<br>1'b1: Enable |
| 4:1 | RW | 0x1 | bisr_pdgdone_sel<br>PDGDone source selection.<br>If bit[1]=1, PDGDone come from bisr_PDGDone, controlled by hardware.<br>If bit[2]=1, PDGDone come from sft_PDGDone (pd_xx_pdgdone_sftena), controlled by software.<br>If bit[3]=1, PDGDone come from bisr_Done, controlled by hardware.<br>If bit[4]=1, PDGDone come from bisr_timeout, controlled by hardware.<br>Only one bit can be set to 1 at a time. |
| 0 | RW | 0x1 | bisr_init<br>Enable memory repair initialization.<br>When asserted, the chip will startup memory repair for memory of power on if external memory repair information is ready. It should be set to 0 if chip is reset by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_BISR_CON1**

Address: Operational Base + offset (0x8204)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pd_rga31_repair_ena<br>Enable memory repair for PD_RGA31 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | pd_isp1_repair_ena<br>Enable memory repair for PD_ISP1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | pd_fec_repair_ena<br>Enable memory repair for PD_FEC by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | pd_vi_repair_ena<br>Enable memory repair for PD_VI by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | pd_av1_repair_ena<br>Enable memory repair for PD_AV1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | pd_rga30_repair_ena<br>Enable memory repair for PD_RGA30 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | pd_vdpu_repair_ena<br>Enable memory repair for PD_VDPU by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | pd_rkvdec1_repair_ena<br>Enable memory repair for PD_RKVDEC1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | pd_rkvdec0_repair_ena<br>Enable memory repair for PD_RKVDEC0 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | pd_venc1_repair_ena<br>Enable memory repair for PD_VENC1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | pd_venc0_repair_ena<br>Enable memory repair for PD_VENC0 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | pd_npu2_repair_ena<br>Enable memory repair for PD_NPU2 by hardware.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | pd_npu1_repair_ena<br>Enable memory repair for PD_NPU1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | pd_nputop_repair_ena<br>Enable memory repair for PD_NPUTOP by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | pd_gpu_bisr_ena<br>Enable memory repair for VD_GPU by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RO | 0x0 | reserved |

**PMU_BISR_CON2**

Address: Operational Base + offset (0x8208)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x1 | pd_bus_repair_ena<br>Enable memory repair for PD_BUS by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x1 | pd_ddr23_repair_ena<br>Enable memory repair for VD_DDR23 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x1 | pd_ddr01_repair_ena<br>Enable memory repair for VD_DDR01 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x1 | pd_center_repair_ena<br>Enable memory repair for PD_CENTER by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x1 | pd_crypto_repair_ena<br>Enable memory repair for PD_CRYPTO by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x1 | pd_sdmmc_repair_ena<br>Enable memory repair for PD_SDMMC by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x1 | pd_usb_repair_ena<br>Enable memory repair for PD_USB by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x1 | pd_sdio_repair_ena<br>Enable memory repair for PD_SDIO by hardware.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x1 | pd_nvm0_repair_ena<br>Enable memory repair for PD_NVM0 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | pd_pcie_repair_ena<br>Enable memory repair for PD_PCIE by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | pd_gmac_repair_ena<br>Enable memory repair for PD_GMAC by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | pd_php_repair_ena<br>Enable memory repair for PD_PHP by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | pd_audio_repair_ena<br>Enable memory repair for PD_AUDIO by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | pd_vo1_repair_ena<br>Enable memory repair for PD_VO1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | pd_vo0_repair_ena<br>Enable memory repair for PD_VO0 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | pd_vop_repair_ena<br>Enable memory repair for PD_VOP by hardware.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_BISR_CON3**

Address: Operational Base + offset (0x820C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pd_vopesmart_repair_ena<br>Enable memory repair for PD_VOPESMART by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | pd_vopdsc4k_repair_ena<br>Enable memory repair for PD_VOPDSC4K by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | pd_vopdsc8k_repair_ena<br>Enable memory repair for PD_VOPDSC8K by hardware.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | pd_vopcluster3_repair_ena<br>Enable memory repair for PD_VOPCLUSTER3 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | pd_vopcluster2_repair_ena<br>Enable memory repair for PD_VOPCLUSTER2 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | pd_vopcluster1_repair_ena<br>Enable memory repair for PD_VOPCLUSTER1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | pd_vopcluster0_repair_ena<br>Enable memory repair for PD_VOPCLUSTER0 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x1 | pd_cpu0_repair_ena<br>Enable memory repair for PD_CPU0 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x1 | pd_cpu1_repair_ena<br>Enable memory repair for PD_CPU1 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x1 | pd_cpu2_repair_ena<br>Enable memory repair for PD_CPU2 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x1 | pd_cpu3_repair_ena<br>Enable memory repair for PD_CPU3 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x1 | pd_cpu4_repair_ena<br>Enable memory repair for PD_CPU4 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x1 | pd_cpu5_repair_ena<br>Enable memory repair for PD_CPU5 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x1 | pd_cpu6_repair_ena<br>Enable memory repair for PD_CPU6 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x1 | pd_cpu7_repair_ena<br>Enable memory repair for PD_CPU7 by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x1 | pd_dsu_repair_ena<br>Enable memory repair for PD_DSU by hardware.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_BISR_CON4**

Address: Operational Base + offset (0x8210)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pd_rga31_repair_sftena<br>Enable memory repair for PD_RGA31 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | pd_isp1_repair_sftena<br>Enable memory repair for PD_ISP1 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | pd_fec_repair_sftena<br>Enable memory repair for PD_FEC by software.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | pd_vi_repair_sftena<br>Enable memory repair for PD_VI by software.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | pd_av1_repair_sftena<br>Enable memory repair for PD_AV1 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | pd_rga30_repair_sftena<br>Enable memory repair for PD_RGA30 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | pd_vdpu_repair_sftena<br>Enable memory repair for PD_VDPU by software.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | pd_rkvdec1_repair_sftena<br>Enable memory repair for PD_RKVDEC1 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | pd_rkvdec0_repair_sftena<br>Enable memory repair for PD_RKVDEC0 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | pd_venc1_repair_sftena<br>Enable memory repair for PD_VENC1 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | pd_venc0_repair_sftena<br>Enable memory repair for PD_VENC0 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | pd_npu2_repair_sftena<br>Enable memory repair for PD_NPU2 by software.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | pd_npu1_repair_sftena<br>Enable memory repair for PD_NPU1 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | pd_nputop_repair_sftena<br>Enable memory repair for PD_NPUTOP by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | pd_gpu_bisr_sftena<br>Enable memory repair for VD_GPU by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | pd_pmu1_repair_sftena<br>Enable memory repair for PD_PMU1 by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_BISR_CON5**

Address: Operational Base + offset (0x8214)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pd_bus_repair_sftena<br>Enable memory repair for PD_BUS by software.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | pd_ddr23_repair_sftena<br>Enable memory repair for VD_DDR23 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | pd_ddr01_repair_sftena<br>Enable memory repair for VD_DDR01 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | pd_center_repair_sftena<br>Enable memory repair for PD_CENTER by software.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | pd_crypto_repair_sftena<br>Enable memory repair for PD_CRYPTO by software.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | pd_sdmmc_repair_sftena<br>Enable memory repair for PD_SDMMC by software.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | pd_usb_repair_sftena<br>Enable memory repair for PD_USB by software.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | pd_sdio_repair_sftena<br>Enable memory repair for PD_SDIO by software.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | pd_nvm0_repair_sftena<br>Enable memory repair for PD_NVM0 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | pd_pcie_repair_sftena<br>Enable memory repair for PD_PCIE by software.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | pd_gmac_repair_sftena<br>Enable memory repair for PD_GMAC by software.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | pd_php_repair_sftena<br>Enable memory repair for PD_PHP by software.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | pd_audio_repair_sftena<br>Enable memory repair for PD_AUDIO by software.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | pd_vo1_repair_sftena<br>Enable memory repair for PD_VO1 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | pd_vo0_repair_sftena<br>Enable memory repair for PD_VO0 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | pd_vop_repair_sftena<br>Enable memory repair for PD_VOP by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_BISR_CON6**

Address: Operational Base + offset (0x8218)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pd_vopesmart_repair_sftena<br>Enable memory repair for PD_VOPESMART by software.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | pd_vopdsc4k_repair_sftena<br>Enable memory repair for PD_VOPDSC4K by software.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | pd_vopdsc8k_repair_sftena<br>Enable memory repair for PD_VOPDSC8K by software.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | pd_vopcluster3_repair_sftena<br>Enable memory repair for PD_VOPCLUSTER3 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | pd_vopcluster2_repair_sftena<br>Enable memory repair for PD_VOPCLUSTER2 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | pd_vopcluster1_repair_sftena<br>Enable memory repair for PD_VOPCLUSTER1 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | pd_vopcluster0_repair_sftena<br>Enable memory repair for PD_VOPCLUSTER0 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | pd_cpu0_repair_sftena<br>Enable memory repair for PD_CPU0 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | pd_cpu1_repair_sftena<br>Enable memory repair for PD_CPU1 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | pd_cpu2_repair_sftena<br>Enable memory repair for PD_CPU2 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | pd_cpu3_repair_sftena<br>Enable memory repair for PD_CPU3 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | pd_cpu4_repair_sftena<br>Enable memory repair for PD_CPU4 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | pd_cpu5_repair_sftena<br>Enable memory repair for PD_CPU5 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | pd_cpu6_repair_sftena<br>Enable memory repair for PD_CPU6 by software.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | pd_cpu7_repair_sftena<br>Enable memory repair for PD_CPU7 by software.<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | pd_dsu_repair_sftena<br>Enable memory repair for PD_DSU by software.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_BISR_CON7**

Address: Operational Base + offset (0x821C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pd_rga31_pdgdone_sftena<br>Configure repair done for PD_RGA31 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 14 | RW | 0x0 | pd_isp1_pdgdone_sftena<br>Configure repair done for PD_ISP1 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 13 | RW | 0x0 | pd_fec_pdgdone_sftena<br>Configure repair done for PD_FEC by software.<br>1'b0: Inactive<br>1'b1: Active |
| 12 | RW | 0x0 | pd_vi_pdgdone_sftena<br>Configure repair done for PD_VI by software.<br>1'b0: Inactive<br>1'b1: Active |
| 11 | RW | 0x0 | pd_av1_pdgdone_sftena<br>Configure repair done for PD_AV1 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 10 | RW | 0x0 | pd_rga30_pdgdone_sftena<br>Configure repair done for PD_RGA30 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 9 | RW | 0x0 | pd_vdpu_pdgdone_sftena<br>Configure repair done for PD_VDPU by software.<br>1'b0: Inactive<br>1'b1: Active |
| 8 | RW | 0x0 | pd_rkvdec1_pdgdone_sftena<br>Configure repair done for PD_RKVDEC1 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 7 | RW | 0x0 | pd_rkvdec0_pdgdone_sftena<br>Configure repair done for PD_RKVDEC0 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 6 | RW | 0x0 | pd_venc1_pdgdone_sftena<br>Configure repair done for PD_VENC1 by software.<br>1'b0: Inactive<br>1'b1: Active |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | pd_venc0_pdgdone_sftena<br>Configure repair done for PD_VENC0 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 4 | RW | 0x0 | pd_npu2_pdgdone_sftena<br>Configure repair done for PD_NPU2 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 3 | RW | 0x0 | pd_npu1_pdgdone_sftena<br>Configure repair done for PD_NPU1 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 2 | RW | 0x0 | pd_nputop_pdgdone_sftena<br>Configure repair done for PD_NPUTOP by software.<br>1'b0: Inactive<br>1'b1: Active |
| 1 | RW | 0x0 | pd_gpu_pdgdone_sftena<br>Configure repair done for VD_GPU by software.<br>1'b0: Inactive<br>1'b1: Active |
| 0 | RW | 0x0 | pd_pmu1_pdgdone_sftena<br>Configure repair done for PD_PMU1 by software.<br>1'b0: Inactive<br>1'b1: Active |

**PMU_BISR_CON8**

Address: Operational Base + offset (0x8220)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pd_bus_pdgdone_sftena<br>Configure repair done for PD_BUS by software.<br>1'b0: Inactive<br>1'b1: Active |
| 14 | RW | 0x0 | pd_ddr23_pdgdone_sftena<br>Configure repair done for VD_DDR23 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 13 | RW | 0x0 | pd_ddr01_pdgdone_sftena<br>Configure repair done for VD_DDR01 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 12 | RW | 0x0 | pd_center_pdgdone_sftena<br>Configure repair done for PD_CENTER by software.<br>1'b0: Inactive<br>1'b1: Active |
| 11 | RW | 0x0 | pd_crypto_pdgdone_sftena<br>Configure repair done for PD_CRYPTO by software.<br>1'b0: Inactive<br>1'b1: Active |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10 | RW | 0x0 | pd_sdmmc_pdgdone_sftena<br>Configure repair done for PD_SDMMC by software.<br>1'b0: Inactive<br>1'b1: Active |
| 9 | RW | 0x0 | pd_usb_pdgdone_sftena<br>Configure repair done for PD_USB by software.<br>1'b0: Inactive<br>1'b1: Active |
| 8 | RW | 0x0 | pd_sdio_pdgdone_sftena<br>Configure repair done for PD_SDIO by software.<br>1'b0: Inactive<br>1'b1: Active |
| 7 | RW | 0x0 | pd_nvm0_pdgdone_sftena<br>Configure repair done for PD_NVM0 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 6 | RW | 0x0 | pd_pcie_pdgdone_sftena<br>Configure repair done for PD_PCIE by software.<br>1'b0: Inactive<br>1'b1: Active |
| 5 | RW | 0x0 | pd_gmac_pdgdone_sftena<br>Configure repair done for PD_GMAC by software.<br>1'b0: Inactive<br>1'b1: Active |
| 4 | RW | 0x0 | pd_php_pdgdone_sftena<br>Configure repair done for PD_PHP by software.<br>1'b0: Inactive<br>1'b1: Active |
| 3 | RW | 0x0 | pd_audio_pdgdone_sftena<br>Configure repair done for PD_AUDIO by software.<br>1'b0: Inactive<br>1'b1: Active |
| 2 | RW | 0x0 | pd_vo1_pdgdone_sftena<br>Configure repair done for PD_VO1 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 1 | RW | 0x0 | pd_vo0_pdgdone_sftena<br>Configure repair done for PD_VO0 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 0 | RW | 0x0 | pd_vop_pdgdone_sftena<br>Active repair PD_VOP by software.<br>1'b0: Inactive<br>1'b1: Active |

**PMU_BISR_CON9**

Address: Operational Base + offset (0x8224)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x0 | pd_vopesmart_pdgdone_sftena<br>Configure repair done for PD_VOPESMART by software.<br>1'b0: Inactive<br>1'b1: Active |
| 14 | RW | 0x0 | pd_vopdsc4k_pdgdone_sftena<br>Configure repair done for PD_VOPDSC4K by software.<br>1'b0: Inactive<br>1'b1: Active |
| 13 | RW | 0x0 | pd_vopdsc8k_pdgdone_sftena<br>Configure repair done for PD_VOPDSC8K by software.<br>1'b0: Inactive<br>1'b1: Active |
| 12 | RW | 0x0 | pd_vopcluster3_pdgdone_sftena<br>Configure repair done for PD_VOPCLUSTER3 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 11 | RW | 0x0 | pd_vopcluster2_pdgdone_sftena<br>Configure repair done for PD_VOPCLUSTER2 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 10 | RW | 0x0 | pd_vopcluster1_pdgdone_sftena<br>Configure repair done for PD_VOPCLUSTER1 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 9 | RW | 0x0 | pd_vopcluster0_pdgdone_sftena<br>Configure repair done for PD_VOPCLUSTER0 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 8 | RW | 0x0 | pd_cpu0_pdgdone_sftena<br>Configure repair done for PD_CPU0 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 7 | RW | 0x0 | pd_cpu1_pdgdone_sftena<br>Configure repair done for PD_CPU1 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 6 | RW | 0x0 | pd_cpu2_pdgdone_sftena<br>Configure repair done for PD_CPU2 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 5 | RW | 0x0 | pd_cpu3_pdgdone_sftena<br>Configure repair done for PD_CPU3 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 4 | RW | 0x0 | pd_cpu4_pdgdone_sftena<br>Configure repair done for PD_CPU4 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 3 | RW | 0x0 | pd_cpu5_pdgdone_sftena<br>Configure repair done for PD_CPU5 by software.<br>1'b0: Inactive<br>1'b1: Active |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | pd_cpu6_pdgdone_sftena<br>Configure repair done for PD_CPU6 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 1 | RW | 0x0 | pd_cpu7_pdgdone_sftena<br>Configure repair done for PD_CPU7 by software.<br>1'b0: Inactive<br>1'b1: Active |
| 0 | RW | 0x0 | pd_dsu_pdgdone_sftena<br>Configure repair done for PD_DSU by software.<br>1'b0: Inactive<br>1'b1: Active |

**PMU_BISR_CON10**

Address: Operational Base + offset (0x8228)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write Inactive for lower 16 bits, each bit is individual.<br>1'b0: Write access Active<br>1'b1: Write access Inactive |
| 15 | RW | 0x0 | pd_rga31_initrstn_sftena<br>Configure initial reset for PD_RGA31 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 14 | RW | 0x0 | pd_isp1_initrstn_sftena<br>Configure initial reset for PD_ISP1 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 13 | RW | 0x0 | pd_fec_initrstn_sftena<br>Configure initial reset for PD_FEC by software.<br>1'b0: Active<br>1'b1: Inactive |
| 12 | RW | 0x0 | pd_vi_initrstn_sftena<br>Configure initial reset for PD_VI by software.<br>1'b0: Active<br>1'b1: Inactive |
| 11 | RW | 0x0 | pd_av1_initrstn_sftena<br>Configure initial reset for PD_AV1 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 10 | RW | 0x0 | pd_rga30_initrstn_sftena<br>Configure initial reset for PD_RGA30 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 9 | RW | 0x0 | pd_vdpu_initrstn_sftena<br>Configure initial reset for PD_VDPU by software.<br>1'b0: Active<br>1'b1: Inactive |
| 8 | RW | 0x0 | pd_rkvdec1_initrstn_sftena<br>Configure initial reset for PD_RKVDEC1 by software.<br>1'b0: Active<br>1'b1: Inactive |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x0 | pd_rkvdec0_initrstn_sftena<br>Configure initial reset for PD_RKVDEC0 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 6 | RW | 0x0 | pd_venc1_initrstn_sftena<br>Configure initial reset for PD_VENC1 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 5 | RW | 0x0 | pd_venc0_initrstn_sftena<br>Configure initial reset for PD_VENC0 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 4 | RW | 0x0 | pd_npu2_initrstn_sftena<br>Configure initial reset for PD_NPU2 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 3 | RW | 0x0 | pd_npu1_initrstn_sftena<br>Configure initial reset for PD_NPU1 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 2 | RW | 0x0 | pd_nputop_initrstn_sftena<br>Configure initial reset for PD_NPUTOP by software.<br>1'b0: Active<br>1'b1: Inactive |
| 1 | RW | 0x0 | pd_gpu_initrstn_sftena<br>Configure initial reset for PD_PMU1 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 0 | RW | 0x0 | pd_pmu1_initrstn_sftena<br>Configure initial reset for PD_PMU1 by software.<br>1'b0: Active<br>1'b1: Inactive |

**PMU_BISR_CON11**

Address: Operational Base + offset (0x822C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write Inactive for lower 16 bits, each bit is individual.<br>1'b0: Write access Active<br>1'b1: Write access Inactive |
| 15 | RW | 0x0 | pd_bus_initrstn_sftena<br>Configure initial reset for PD_BUS by software.<br>1'b0: Active<br>1'b1: Inactive |
| 14 | RW | 0x0 | pd_ddr23_initrstn_sftena<br>Configure initial reset for VD_DDR23 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 13 | RW | 0x0 | pd_ddr01_initrstn_sftena<br>Configure initial reset for VD_DDR01 by software.<br>1'b0: Active<br>1'b1: Inactive |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | pd_center_initrstn_sftena<br>Configure initial reset for PD_CENTER by software.<br>1'b0: Active<br>1'b1: Inactive |
| 11 | RW | 0x0 | pd_crypto_initrstn_sftena<br>Configure initial reset for PD_CRYPTO by software.<br>1'b0: Active<br>1'b1: Inactive |
| 10 | RW | 0x0 | pd_sdmmc_initrstn_sftena<br>Configure initial reset for PD_SDMMC by software.<br>1'b0: Active<br>1'b1: Inactive |
| 9 | RW | 0x0 | pd_usb_initrstn_sftena<br>Configure initial reset for PD_USB by software.<br>1'b0: Active<br>1'b1: Inactive |
| 8 | RW | 0x0 | pd_sdio_initrstn_sftena<br>Configure initial reset for PD_SDIO by software.<br>1'b0: Active<br>1'b1: Inactive |
| 7 | RW | 0x0 | pd_nvm0_initrstn_sftena<br>Configure initial reset for PD_NVM0 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 6 | RW | 0x0 | pd_pcie_initrstn_sftena<br>Configure initial reset for PD_PCIE by software.<br>1'b0: Active<br>1'b1: Inactive |
| 5 | RW | 0x0 | pd_gmac_initrstn_sftena<br>Configure initial reset for PD_GMAC by software.<br>1'b0: Active<br>1'b1: Inactive |
| 4 | RW | 0x0 | pd_php_initrstn_sftena<br>Configure initial reset for PD_PHP by software.<br>1'b0: Active<br>1'b1: Inactive |
| 3 | RW | 0x0 | pd_audio_initrstn_sftena<br>Configure initial reset for PD_AUDIO by software.<br>1'b0: Active<br>1'b1: Inactive |
| 2 | RW | 0x0 | pd_vo1_initrstn_sftena<br>Configure initial reset for PD_VO1 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 1 | RW | 0x0 | pd_vo0_initrstn_sftena<br>Configure initial reset for PD_VO0 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 0 | RW | 0x0 | pd_vop_initrstn_sftena<br>Configure initial reset for PD_VOP by software.<br>1'b0: Active<br>1'b1: Inactive |

**PMU_BISR_CON12**

Address: Operational Base + offset (0x8230)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | pd_vopesmart_initrstn_sftena<br>Configure initial reset for PD_VOPESMART by software.<br>1'b0: Active<br>1'b1: Inactive |
| 14 | RW | 0x0 | pd_vopdsc4k_initrstn_sftena<br>Configure initial reset for PD_VOPDSC4K by software.<br>1'b0: Active<br>1'b1: Inactive |
| 13 | RW | 0x0 | pd_vopdsc8k_initrstn_sftena<br>Configure initial reset for PD_VOPDSC8K by software.<br>1'b0: Active<br>1'b1: Inactive |
| 12 | RW | 0x0 | pd_vopcluster3_initrstn_sftena<br>Configure initial reset for PD_VOPCLUSTER3 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 11 | RW | 0x0 | pd_vopcluster2_initrstn_sftena<br>Configure initial reset for PD_VOPCLUSTER2 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 10 | RW | 0x0 | pd_vopcluster1_initrstn_sftena<br>Configure initial reset for PD_VOPCLUSTER1 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 9 | RW | 0x0 | pd_vopcluster0_initrstn_sftena<br>Configure initial reset for PD_VOPCLUSTER0 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 8 | RW | 0x0 | pd_cpu0_initrstn_sftena<br>Configure initial reset for PD_CPU0 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 7 | RW | 0x0 | pd_cpu1_initrstn_sftena<br>Configure initial reset for PD_CPU1 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 6 | RW | 0x0 | pd_cpu2_initrstn_sftena<br>Configure initial reset for PD_CPU2 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 5 | RW | 0x0 | pd_cpu3_initrstn_sftena<br>Configure initial reset for PD_CPU3 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 4 | RW | 0x0 | pd_cpu4_initrstn_sftena<br>Configure initial reset for PD_CPU4 by software.<br>1'b0: Active<br>1'b1: Inactive |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | pd_cpu5_initrstn_sftena<br>Configure initial reset for PD_CPU5 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 2 | RW | 0x0 | pd_cpu6_initrstn_sftena<br>Configure initial reset for PD_CPU6 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 1 | RW | 0x0 | pd_cpu7_initrstn_sftena<br>Configure initial reset for PD_CPU7 by software.<br>1'b0: Active<br>1'b1: Inactive |
| 0 | RW | 0x0 | pd_dsu_initrstn_sftena<br>Configure initial reset for PD_DSU by software.<br>1'b0: Active<br>1'b1: Inactive |

**PMU_BISR_CON13**

Address: Operational Base + offset (0x8234)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | pciephy_initrstn_sftena<br>Configure repair initial reset for PCIEPHY by software.<br>1'b0: Active<br>1'b1: Inactive |
| 12 | RW | 0x0 | hdmirxphy_initrstn_sftena<br>Configure repair initial reset for HDMIRXPHY by software.<br>1'b0: Active<br>1'b1: Inactive |
| 11:10 | RO | 0x0 | reserved |
| 9 | RW | 0x0 | pciephy_pdgdone_sftena<br>Configure repair done for PCIEPHY by software.<br>1'b0: Inactive<br>1'b1: Active |
| 8 | RW | 0x0 | hdmirxphy_pdgdone_sftena<br>Configure repair done for HDMIRXPHY by software.<br>1'b0: Inactive<br>1'b1: Active |
| 7:6 | RO | 0x0 | reserved |
| 5 | RW | 0x0 | pciephy_repair_sftena<br>Enable memory repair for PCIEPHY by software.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | hdmirxphy_repair_sftena<br>Enable memory repair for HDMIRXPHY by software.<br>1'b0: Disable<br>1'b1: Enable |
| 3:2 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x1 | pciephy_repair_ena<br>Enable memory repair for PCIEPHY by hardware.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x1 | hdmirxphy_repair_ena<br>Enable memory repair for HDMIRXPHY by hardware.<br>1'b0: Disable<br>1'b1: Enable |

**PMU_BISR_CON14**

Address: Operational Base + offset (0x8238)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0xffffffff | bisr_timeout_cnt<br>BISR timeout count for PDGDone. Number of repair clock used by counter logic. |

**PMU_BISR_STS0**

Address: Operational Base + offset (0x8280)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | pd_bus_dwn_pdgdone<br>PDGDone status for PD_BUS repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 30 | RO | 0x0 | pd_ddr23_dwn_pdgdone<br>PDGDone status for VD_DDR23 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 29 | RO | 0x0 | pd_ddr01_dwn_pdgdone<br>PDGDone status for VD_DDR01 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 28 | RO | 0x0 | pd_center_dwn_pdgdone<br>PDGDone status for PD_CENTER repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 27 | RO | 0x0 | pd_crypto_dwn_pdgdone<br>PDGDone status for PD_CRYPTO repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 26 | RO | 0x0 | pd_sdmmc_dwn_pdgdone<br>PDGDone status for PD_SDMMC repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 25 | RO | 0x0 | pd_usb_dwn_pdgdone<br>PDGDone status for PD_USB repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 24 | RO | 0x0 | pd_sdio_dwn_pdgdone<br>PDGDone status for PD_SDIO repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 23 | RO | 0x0 | pd_nvm0_dwn_pdgdone<br>PDGDone status for PD_NVM0 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 22 | RO | 0x0 | pd_pcie_dwn_pdgdone<br>PDGDone status for PD_PCIE repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 21 | RO | 0x0 | pd_gmac_dwn_pdgdone<br>PDGDone status for PD_GMAC repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 20 | RO | 0x0 | pd_php_dwn_pdgdone<br>PDGDone status for PD_PHP repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 19 | RO | 0x0 | pd_audio_dwn_pdgdone<br>PDGDone status for PD_AUDIO repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 18 | RO | 0x0 | pd_vo1_dwn_pdgdone<br>PDGDone status for PD_VO1 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 17 | RO | 0x0 | pd_vo0_dwn_pdgdone<br>PDGDone status for PD_VO0 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 16 | RO | 0x0 | pd_vop_dwn_pdgdone<br>PDGDone status for PD_VOP repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 15 | RO | 0x0 | pd_rga31_dwn_pdgdone<br>PDGDone status for PD_RGA31 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 14 | RO | 0x0 | pd_isp1_dwn_pdgdone<br>PDGDone status for PD_ISP1 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 13 | RO | 0x0 | pd_fec_dwn_pdgdone<br>PDGDone status for PD_FEC repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 12 | RO | 0x0 | pd_vi_dwn_pdgdone<br>PDGDone status for PD_VI repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 11 | RO | 0x0 | pd_av1_dwn_pdgdone<br>PDGDone status for PD_AV1 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 10 | RO | 0x0 | pd_rga30_dwn_pdgdone<br>PDGDone status for PD_RGA30 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RO | 0x0 | pd_vdpu_dwn_pdgdone<br>PDGDone status for PD_VDPU repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 8 | RO | 0x0 | pd_rkvdec1_dwn_pdgdone<br>PDGDone status for PD_RKVDEC1 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 7 | RO | 0x0 | pd_rkvdec0_dwn_pdgdone<br>PDGDone status for PD_RKVDEC0 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 6 | RO | 0x0 | pd_venc1_dwn_pdgdone<br>PDGDone status for PD_VENC1 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 5 | RO | 0x0 | pd_venc0_dwn_pdgdone<br>PDGDone status for PD_VENC0 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 4 | RO | 0x0 | pd_npu2_dwn_pdgdone<br>PDGDone status for PD_NPU2 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 3 | RO | 0x0 | pd_npu1_dwn_pdgdone<br>PDGDone status for PD_NPU1 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 2 | RO | 0x0 | pd_nputop_dwn_pdgdone<br>PDGDone status for PD_NPUTOP repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 1 | RO | 0x0 | pd_gpu_bisr_pdgdone<br>PDGDone status for VD_GPU repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 0 | RO | 0x0 | pd_pmu1_repair_pdgdone<br>PDGDone status for PD_PMU1 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |

**PMU_BISR_STS1**

Address: Operational Base + offset (0x8284)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17 | RO | 0x0 | pciephy_repair_pdgdone<br>PDGDone status for PCIEPHY repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 16 | RO | 0x0 | hdmirxphy_repair_pdgdone<br>PDGDone status for HDMIRXPHY repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RO | 0x0 | pd_vopesmart_repair_pdgdone<br>PDGDone status for PD_VOPESMAKRT repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 14 | RO | 0x0 | pd_vopdsc4k_repair_pdgdone<br>PDGDone status for PD_VOPDSC4K repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 13 | RO | 0x0 | pd_vopdsc8k_repair_pdgdone<br>PDGDone status for PD_VOPDSC8K repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 12 | RO | 0x0 | pd_vopcluster3_repair_pdgdone<br>PDGDone status for PD_VOPCLUSTER3 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 11 | RO | 0x0 | pd_vopcluster2_repair_pdgdone<br>PDGDone status for PD_VOPCLUSTER2 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 10 | RO | 0x0 | pd_vopcluster1_repair_pdgdone<br>PDGDone status for PD_VOPCLUSTER1 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 9 | RO | 0x0 | pd_vopcluster0_repair_pdgdone<br>PDGDone status for PD_VOPCLUSTER0 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 8 | RO | 0x0 | pd_cpu0_repair_pdgdone<br>PDGDone status for PD_CPU0 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 7 | RO | 0x0 | pd_cpu1_repair_pdgdone<br>PDGDone status for PD_CPU1 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 6 | RO | 0x0 | pd_cpu2_repair_pdgdone<br>PDGDone status for PD_CPU3 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 5 | RO | 0x0 | pd_cpu3_repair_pdgdone<br>PDGDone status for PD_CPU3 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 4 | RO | 0x0 | pd_cpu4_repair_pdgdone<br>PDGDone status for PD_CPU4 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 3 | RO | 0x0 | pd_cpu5_repair_pdgdone<br>PDGDone status for PD_CPU5 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RO | 0x0 | pd_cpu6_repair_pdgdone<br>PDGDone status for PD_CPU6 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 1 | RO | 0x0 | pd_cpu7_repair_pdgdone<br>PDGDone status for PD_CPU7 repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |
| 0 | RO | 0x0 | pd_dsu_repair_pdgdone<br>PDGDone status for PD_DSU repair.<br>1'b0: Repair not complete<br>1'b1: Repair complete |

**PMU_BISR_STS2**

Address: Operational Base + offset (0x8288)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | pd_bus_repair_cedis<br>CEDis status for PD_BUS repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 30 | RO | 0x0 | pd_ddr23_repair_cedis<br>CEDis status for VD_DDR23 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 29 | RO | 0x0 | pd_ddr01_repair_cedis<br>CEDis status for VD_DDR01 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 28 | RO | 0x0 | pd_center_repair_cedis<br>CEDis status for PD_CENTER repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 27 | RO | 0x0 | pd_crypto_repair_cedis<br>CEDis status for PD_CRYPTO repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 26 | RO | 0x0 | pd_sdmmc_repair_cedis<br>CEDis status for PD_SDMMC repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 25 | RO | 0x0 | pd_usb_repair_cedis<br>CEDis status for PD_USB repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 24 | RO | 0x0 | pd_sdio_repair_cedis<br>CEDis status for PD_SDIO repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 23 | RO | 0x0 | pd_nvm0_repair_cedis<br>CEDis status for PD_NVM0 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 22 | RO | 0x0 | pd_pcie_repair_cedis<br>CEDis status for PD_PCIE repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 21 | RO | 0x0 | pd_gmac_repair_cedis<br>CEDis status for PD_GMAC repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 20 | RO | 0x0 | pd_php_repair_cedis<br>CEDis status for PD_PHP repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 19 | RO | 0x0 | pd_audio_repair_cedis<br>CEDis status for PD_AUDIO repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 18 | RO | 0x0 | pd_vo1_repair_cedis<br>CEDis status for PD_VO1 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 17 | RO | 0x0 | pd_vo0_repair_cedis<br>CEDis status for PD_VO0 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 16 | RO | 0x0 | pd_vop_repair_cedis<br>CEDis status for PD_VOP repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 15 | RO | 0x0 | pd_rga31_repair_cedis<br>CEDis status for PD_RGA31 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 14 | RO | 0x0 | pd_isp1_repair_cedis<br>CEDis status for PD_ISP1 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 13 | RO | 0x0 | pd_fec_repair_cedis<br>CEDis status for PD_FEC repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 12 | RO | 0x0 | pd_vi_repair_cedis<br>CEDis status for PD_VI repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 11 | RO | 0x0 | pd_av1_repair_cedis<br>CEDis status for PD_AV1 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 10 | RO | 0x0 | pd_rga30_repair_cedis<br>CEDis status for PD_RGA30 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RO | 0x0 | pd_vdpu_repair_cedis<br>CEDis status for PD_VDPU repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 8 | RO | 0x0 | pd_rkvdec1_repair_cedis<br>CEDis status for PD_RKVDEC1 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 7 | RO | 0x0 | pd_rkvdec0_repair_cedis<br>CEDis status for PD_RKVDEC0 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 6 | RO | 0x0 | pd_venc1_repair_cedis<br>CEDis status for PD_VENC1 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 5 | RO | 0x0 | pd_venc0_repair_cedis<br>CEDis status for PD_VENC0 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 4 | RO | 0x0 | pd_npu2_repair_cedis<br>CEDis status for PD_NPU2 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 3 | RO | 0x0 | pd_npu1_repair_cedis<br>CEDis status for PD_NPU1 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 2 | RO | 0x0 | pd_nputop_repair_cedis<br>CEDis status for PD_NPUTOP repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 1 | RO | 0x0 | pd_gpu_bisr_cedis<br>CEDis status for VD_GPU repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 0 | RO | 0x0 | pd_pmu1_repair_cedis<br>CEDis status for PD_PMU1 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |

**PMU_BISR_STS3**

Address: Operational Base + offset (0x828C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17 | RO | 0x0 | pciephy_repair_cedis<br>CEDis status for PCIEPHY repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 16 | RO | 0x0 | hdmirxphy_repair_cedis<br>CEDis status for HDMIRXPHY repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RO | 0x0 | pd_vopesmart_repair_cedis<br>CEDis status for PD_VOPESMAKRT repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 14 | RO | 0x0 | pd_vopdsc4k_repair_cedis<br>CEDis status for PD_VOPDSC4K repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 13 | RO | 0x0 | pd_vopdsc8k_repair_cedis<br>CEDis status for PD_VOPDSC8K repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 12 | RO | 0x0 | pd_vopcluster3_repair_cedis<br>CEDis status for PD_VOPCLUSTER3 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 11 | RO | 0x0 | pd_vopcluster2_repair_cedis<br>CEDis status for PD_VOPCLUSTER2 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 10 | RO | 0x0 | pd_vopcluster1_repair_cedis<br>CEDis status for PD_VOPCLUSTER1 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 9 | RO | 0x0 | pd_vopcluster0_repair_cedis<br>CEDis status for PD_VOPCLUSTER0 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 8 | RO | 0x0 | pd_cpu0_repair_cedis<br>CEDis status for PD_CPU0 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 7 | RO | 0x0 | pd_cpu1_repair_cedis<br>CEDis status for PD_CPU1 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 6 | RO | 0x0 | pd_cpu2_repair_cedis<br>CEDis status for PD_CPU3 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 5 | RO | 0x0 | pd_cpu3_repair_cedis<br>CEDis status for PD_CPU3 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 4 | RO | 0x0 | pd_cpu4_repair_cedis<br>CEDis status for PD_CPU4 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 3 | RO | 0x0 | pd_cpu5_repair_cedis<br>CEDis status for PD_CPU5 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RO | 0x0 | pd_cpu6_repair_cedis<br>CEDis status for PD_CPU6 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 1 | RO | 0x0 | pd_cpu7_repair_cedis<br>CEDis status for PD_CPU7 repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |
| 0 | RO | 0x0 | pd_dsu_repair_cedis<br>CEDis status for PD_DSU repair.<br>1'b0: Repair ready<br>1'b1: Repair busy |

**PMU_BISR_STS4**

Address: Operational Base + offset (0x8290)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | pd_bus_dwn_pwr_repair_stat<br>Power and repair status for PD_BUS repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 30 | RO | 0x0 | pd_ddr23_dwn_pwr_repair_stat<br>Power and repair status for VD_DDR23 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 29 | RO | 0x0 | pd_ddr01_dwn_pwr_repair_stat<br>Power and repair status for VD_DDR01 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 28 | RO | 0x0 | pd_center_dwn_pwr_repair_stat<br>Power and repair status for PD_CENTER repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 27 | RO | 0x0 | pd_crypto_dwn_pwr_repair_stat<br>Power and repair status for PD_CRYPTO repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 26 | RO | 0x0 | pd_sdmmc_dwn_pwr_repair_stat<br>Power and repair status for PD_SDMMC repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 25 | RO | 0x0 | pd_usb_dwn_pwr_repair_stat<br>Power and repair status for PD_USB repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 24 | RO | 0x0 | pd_sdio_dwn_pwr_repair_stat<br>Power and repair status for PD_SDIO repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 23 | RO | 0x0 | pd_nvm0_dwn_pwr_repair_stat<br>Power and repair status for PD_NVM0 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 22 | RO | 0x0 | pd_pcie_dwn_pwr_repair_stat<br>Power and repair status for PD_PCIE repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 21 | RO | 0x0 | pd_gmac_dwn_pwr_repair_stat<br>Power and repair status for PD_GMAC repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 20 | RO | 0x0 | pd_php_dwn_pwr_repair_stat<br>Power and repair status for PD_PHP repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 19 | RO | 0x0 | pd_audio_dwn_pwr_repair_stat<br>Power and repair status for PD_AUDIO repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 18 | RO | 0x0 | pd_vo1_dwn_pwr_repair_stat<br>Power and repair status for PD_VO1 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 17 | RO | 0x0 | pd_vo0_dwn_pwr_repair_stat<br>Power and repair status for PD_VO0 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 16 | RO | 0x0 | pd_vop_dwn_pwr_repair_stat<br>Power and repair status for PD_VOP repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 15 | RO | 0x0 | pd_rga31_dwn_pwr_repair_stat<br>Power and repair status for PD_RGA31 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 14 | RO | 0x0 | pd_isp1_dwn_pwr_repair_stat<br>Power and repair status for PD_ISP1 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 13 | RO | 0x0 | pd_fec_dwn_pwr_repair_stat<br>Power and repair status for PD_FEC repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 12 | RO | 0x0 | pd_vi_dwn_pwr_repair_stat<br>Power and repair status for PD_VI repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 11 | RO | 0x0 | pd_av1_dwn_pwr_repair_stat<br>Power and repair status for PD_AV1 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 10 | RO | 0x0 | pd_rga30_dwn_pwr_repair_stat<br>Power and repair status for PD_RGA30 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RO | 0x0 | pd_vdpu_dwn_pwr_repair_stat<br>Power and repair status for PD_VDPU repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 8 | RO | 0x0 | pd_rkvdec1_dwn_pwr_repair_stat<br>Power and repair status for PD_RKVDEC1 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 7 | RO | 0x0 | pd_rkvdec0_dwn_pwr_repair_stat<br>Power and repair status for PD_RKVDEC0 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 6 | RO | 0x0 | pd_venc1_dwn_pwr_repair_stat<br>Power and repair status for PD_VENC1 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 5 | RO | 0x0 | pd_venc0_dwn_pwr_repair_stat<br>Power and repair status for PD_VENC0 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 4 | RO | 0x0 | pd_npu2_dwn_pwr_repair_stat<br>Power and repair status for PD_NPU2 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 3 | RO | 0x0 | pd_npu1_dwn_pwr_repair_stat<br>Power and repair status for PD_NPU1 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 2 | RO | 0x0 | pd_nputop_dwn_pwr_repair_stat<br>Power and repair status for PD_NPUTOP repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 1 | RO | 0x0 | pd_gpu_bisr_pwr_repair_stat<br>Power and repair status for VD_GPU repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 0 | RO | 0x0 | pd_pmu1_pwr_repair_stat<br>Power and repair status for PD_PMU1.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |

**PMU_BISR_STS5**

Address: Operational Base + offset (0x8294)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17 | RO | 0x0 | pciephy_repair_pwr_repair_stat<br>Power and repair status for PCIEPHY repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 16 | RO | 0x0 | hdmirxphy_repair_pwr_repair_stat<br>Power and repair status for HDMIRXPHY repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RO | 0x0 | pd_vopesmart_repair_pwr_repair_stat<br>Power and repair status for PD_VOPESMAKRT repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 14 | RO | 0x0 | pd_vopdsc4k_repair_pwr_repair_stat<br>Power and repair status for PD_VOPDSC4K repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 13 | RO | 0x0 | pd_vopdsc8k_repair_pwr_repair_stat<br>Power and repair status for PD_VOPDSC8K repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 12 | RO | 0x0 | pd_vopcluster3_repair_pwr_repair_stat<br>Power and repair status for PD_VOPCLUSTER3 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 11 | RO | 0x0 | pd_vopcluster2_repair_pwr_repair_stat<br>Power and repair status for PD_VOPCLUSTER2 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 10 | RO | 0x0 | pd_vopcluster1_repair_pwr_repair_stat<br>Power and repair status for PD_VOPCLUSTER1 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 9 | RO | 0x0 | pd_vopcluster0_repair_pwr_repair_stat<br>Power and repair status for PD_VOPCLUSTER0 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 8 | RO | 0x0 | pd_cpu0_repair_pwr_repair_stat<br>Power and repair status for PD_CPU0 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 7 | RO | 0x0 | pd_cpu1_repair_pwr_repair_stat<br>Power and repair status for PD_CPU1 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 6 | RO | 0x0 | pd_cpu2_repair_pwr_repair_stat<br>Power and repair status for PD_CPU3 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 5 | RO | 0x0 | pd_cpu3_repair_pwr_repair_stat<br>Power and repair status for PD_CPU3 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 4 | RO | 0x0 | pd_cpu4_repair_pwr_repair_stat<br>Power and repair status for PD_CPU4 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 3 | RO | 0x0 | pd_cpu5_repair_pwr_repair_stat<br>Power and repair status for PD_CPU5 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RO | 0x0 | pd_cpu6_repair_pwr_repair_stat<br>Power and repair status for PD_CPU6 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 1 | RO | 0x0 | pd_cpu7_repair_pwr_repair_stat<br>Power and repair status for PD_CPU7 repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |
| 0 | RO | 0x0 | pd_dsu_repair_pwr_repair_stat<br>Power and repair status for PD_DSU repair.<br>1'b0: Power down or repair not complete<br>1'b1: Power up and repair complete |

## 7.5 Application Notes

### 7.5.1 Low Power Mode

PMU can work in power mode 1 by setting bit[0] in PMU_PWR_CON1 register. After setting this bit and all CPUs enter standbywfi state, PMU power mode 1 FSM will start to run. In this low power mode, PMU will manage power resources by hardware or software, such as send idle request or resume transfer to specified BIU interface, power down or power up the specified power domain, DDR enters or exits retention mode, shut down or power up PLL, disable or enable oscillator, and so on. All of above are configurable by setting corresponding registers.

PMU can work in power mode 0 by setting bit[0] in PMU_PWR_CON0 register. After setting this bit and PMU enters power mode 1, PMU power mode 0 FSM will start to run. In this low power mode, PMU will manage PD_PMU1 power resource and idle request, manage DDR retention mode, VCCIO retention mode, disable oscillator, etc. All of above are configurable by setting corresponding registers.

There are similar control bits for bit[0]/[1]/[2]/[3]/[10] in PMU_CRU_PWR_CON and bit[5]/[6]/[7]/[14] in PMU_PWR_CON0. If chip is planned to enter power mode 0, these bits in PMU_CRU_PWR_CON are not need to configure since those low power flow are controlled by PMU_PWR_CON0.

### 7.5.2 Nested Power Domain

There are nested power domains in RK3588, denoted by red-frame and black-frame in "RK3588 Voltage Domain and Power Domain Partition": red-frame used for external power domain, black-frame used for internal power domain. For these power domains, external power domain should not be power down before internal power domain power down, external power domain should be power up before internal power domain power up. These domains are shown below.

Table 7-2 Nested Power Domain 1

| Group ID | External Power Domain | Internal Power Domain |
|---|---|---|
| 1 | PD_VENC0 | PD_VENC1 |
| 2 | PD_NPUTOP | PD_NPU1 |
| 3 | | PD_NPU2 |
| 4 | PD_VI | PD_ISP1 |
| 5 | | PD_FEC |
| 6 | PD_VDPU | PD_AV1 |
| 7 | | PD_RGA30 |
| 8 | PD_SECURE | PD_CRYPTO |
| 9 | | PD_SDMMC |
| 10 | PD_NVM | PD_NVM0 |
| 11 | PD_PHP | PD_GMAC |
| 12 | | PD_PCIE |

Rockchip Confidential

| Group ID | External Power Domain | Internal Power Domain |
|---|---|---|
| 13 | PD_VOP | PD_VOPCLUSTER0 |
| 14 | | PD_VOPDSC4K |
| 15 | | PD_VOPDSC8K |
| 16 | | PD_VOPESMART |
| 17 | PD_VOPCLUSTER0 | PD_VOPCLUSTER1 |
| 18 | | PD_VOPCLUSTER2 |
| 19 | | PD_VOPCLUSTER3 |

It should be noted that the internal power domains in PD_VOP are controlled by VOP internal registers. Moreover, if PD_VOP is power down, both internal power domains in PD_VOP and internal power domains in PD_VOPCLUSTER0 are power down meanwhile.
Incorrect power order may cause power leakage.

Moreover, because of the signal relationship, "Level 0 Power Domain" should be power up and corresponding BIU clock is active if any IP in "Level 1 Power Domain" want to work. Details of corresponding BIU clock please refers to CRU chapter.

Table 7-3 Nested Power Domain 2

| Group ID | Level 0 Power Domain | Level 1 Power Domain |
|---|---|---|
| 1 | PD_SECURE | PD_VO1 |
| 2 | | PD_USB |
| 3 | PD_VDPU | PD_RKVDEC0 |
| 4 | | PD_RKVDEC1 |
| 5 | PD_NVM | PD_SDIO |
| 6 | PD_VOP | PD_VO0 |

### 7.5.3 Software Power Down and Power Up flow

In order to power down the power domains which are managed by software correctly, the software should obey the flow bellow.

**1. Software power down flow**

(1) Send BIU idle request if BIU interface exists in specific power domain that you want to power down by configure the corresponding bit in PMU_IDLE_SFTCON0/1/2 register. If BIU interface does not exist, skip this step;
(2) Query PMU_IDLE_ACK_STS0/1 register to wait for the corresponding BIU idle acknowledge state; Query PMU_IDLE_STS0/1 register to wait for the corresponding BIU in idle state. If BIU interface does not exist, skip this step;
(3) Enable power down to the specific power domain by setting corresponding bit to 1 in PMU_PWR_GATE_SFTCON0/1/2 register;
(4) Query PMU_PWR_GATE_STS0/1 register to wait for the specific power domain power down;

**2. Software power up without repair flow**

(1) Enable power up to the specific power domain by setting corresponding bit to 0 in PMU_PWR_GATE_SFTCON0/1/2 register;
(2) Query PMU_PWR_GATE_STS0/1 register to wait for the specific power domain power up;
(3) Send BIU resume request to the BIU in specific power domain that you want to power down by configure the corresponding bit in PMU_IDLE_SFTCON0/1/2 register; If BIU interface does not exist, skip this step;
(4) Query PMU_IDLE_ACK_STS0/1 register to wait for the corresponding BIU idle acknowledge state; Query PMU_IDLE_STS0/1 register to wait for the corresponding BIU in idle state; If BIU interface does not exist, skip this step.

**3. Software power up with hardware repair flow**

(1) Enable memory repair to the specific power domain by setting corresponding bit to 1 in PMU_BISR_CON1/2/3/13 register;
(2) Enable power up to the specific power domain by setting corresponding bit to 0 in PMU_PWR_GATE_SFTCON0/1/2 register;
(3) Query PMU_BISR_STS4/5 register to wait for the specific power domain power up and repair done;
(4) Send BIU request to the BIU in specific power domain that you want to power up by configure the corresponding bit in PMU_IDLE_SFTCON0/1/2 register; If BIU interface

Rockchip Confidential

does not exist, skip this step;
(5) Query PMU_IDLE_ACK_STS0/1 register to wait for the corresponding BIU exiting idle acknowledgement state; Query PMU_IDLE_STS0/1 register to wait for the corresponding BIU exit idle state; If BIU interface does not exist, skip this step.

**4. Software power up with software repair flow**

(1) Enable memory repair to the specific power domain by setting corresponding bit to 1 in PMU_BISR_CON4/5/6/13 register;
(2) Set PMU_BISR_CON0[10] to 1 to select software repair mode;
(3) Enable power up to the specific power domain by setting corresponding bit to 0 in PMU_PWR_GATE_SFTCON0/1/2 register;
(4) Query PMU_PWR_GATE_STS0/1 register to wait for the specific power domain power up;
(5) Disable software repair clock gating by set PMU_BISR_CON0[6] to 0;
(6) Enable software memory repair reset to the specific power domain by setting corresponding bit to 1 in PMU_BISR_CON10/11/12/13 register;
(7) Set PMU_BISR_CON0[9] to 1 to initial repair global reset signal high; wait for some time and then set PMU_BISR_CON0[9] to 0 to set repair global reset signal low; wait for some time and then set PMU_BISR_CON0[9] to 1 to set repair global reset signal high;
(8) Query PMU_BISR_STS0/1 register to wait for the specific power domain repair done;
(9) Enable software repair clock gating by set PMU_BISR_CON0[6] to 1;
(10) Send BIU request to the BIU in specific power domain that you want to power up by configure the corresponding bit in PMU_IDLE_SFTCON0/1/2 register; If BIU interface does not exist, skip this step.
(11) Query PMU_IDLE_ACK_STS0/1 register to wait for the corresponding BIU exiting idle acknowledgement state; Query PMU_IDLE_STS0/1 register to wait for the corresponding BIU exit idle state; If BIU interface does not exist, skip this step.

### 7.5.4 Memory Power Control

In RK3588, memory powers are independent of logic powers in the power domain. These memory powers can be controlled by software independently through setting specified bit in PMU_MEM_PWR_GATE_SFTCON0/1/2. They can be power down to reduce power consumption if these memories are not work.
Moreover, some module's memory powers are independent of power domain's memory power in the power domain. In this case, these memory powers can be controlled by software independently through setting specified bit in PMU_SUBMEM_PWR_GATE_SFTCON0/1/2. They can be power down to reduce power consumption if the module is not work. If these memories are pre-power down before its power domain enters power down flow, the memory power acknowledgement should be bypassed through setting specified bit in PMU_SUBMEM_PWR_ACK_BYPASS_CON0/1/2.

### 7.5.5 Power Management IO Usage

There are independent power supplies for different voltage domain. You can communicate with external PMIC (Power Management Integrated Circuits) through I2C interface, or through IO interface.

There are 6 IOs designed for purpose, corresponding Module Pin names are pmic_sleep_1~ pmic_sleep_6. The IO interface configuration is as below.

Table 7-4 Power Management IO Interface

| Module Pin | Direction | Pin Name | IOMUX Setting |
|---|---|---|---|
| pmic_sleep_1 | O | PMIC_SLEEP1/GPIO0_A2_d | PMU1_IOC_GPIO0A_IOMUX_SEL_L[11:8]=1 |
| pmic_sleep_2 | O | PMIC_SLEEP2/GPIO0_A3_d | PMU1_IOC_GPIO0A_IOMUX_SEL_L[15:12]=1 |
| pmic_sleep_3 | O | PMIC_SLEEP3/GPIO0_C1_d | PMU2_IOC_GPIO0C_IOMUX_SEL_L[7:4]=1 |
| pmic_sleep_4 | O | PMIC_SLEEP4/GPIO0_C2_d | PMU2_IOC_GPIO0C_IOMUX_SEL_L[11:8]=1 |
| pmic_sleep_5 | O | PMIC_SLEEP5/GPIO0_C3_d | PMU2_IOC_GPIO0C_IOMUX_SEL_L[15:12]=1 |
| pmic_sleep_6 | O | PMIC_SLEEP6/PDM0_SDI3_M1/ | PMU2_IOC_GPIO0D_IOMUX_ |

Rockchip Confidential

| Module Pin | Direction | Pin Name | IOMUX Setting |
|---|---|---|---|
| | | GPIO0_D6_d | SEL_H[11:8]=1 |

Each pmic_sleep_i(i=0~6) has multi power off requests and you can only choose one at a time. Detail refers to PMU0_GRF_SOC_CON3 and PMU1_GRF_SOC_CON2.

Each voltage domain can generate one power off request. The voltage domain power off request can be generated as below:

(1) Enable power off control bit: Set corresponding bit to 1 in PMU_VOL_GATE_CON0/1;
(2) Power down internal power domain: If there is power domain included in the voltage domain, the power domain should be power down firstly. Else, skip this step;
(3) Power down voltage domain: Set corresponding bit to 1 in PMU_PWR_GATE_CON0/2 by hardware power gating or set corresponding bit to 1 in PMU_PWR_GATE_SFTCON0/2 by software power gating.

### 7.5.6 Debug Information

The PMU internal power states could be monitored through debug IO.
The IO interface configuration is as below.

Table 7-5 PMU Debug IO Interface

| Module Pin | Direction | Pin Name | IOMUX Setting |
|---|---|---|---|
| pmu_debug | O | SPI2_CLK_M2/SDMMC_PWREN/ PMU_DEBUG/GPIO0_A5_d | PMU1_IOC_GPIO0A_IOMUX_ SEL_H[7:4]=3 |

The PMU internal power states are transmitted in 8-bit UART interface mode. If PMU does not enter power mode 0, the debug information is decoded as below.

Table 7-6 PMU Debug Information Decode Before Enter Power Mode 0

| Decode Value | PMU State | Register Description |
|---|---|---|
| 2 | CPU (one CPU of CPU0~CPU7)power down state | PMU_CLUSTER_POWER_STS1[3:0] or [7:4]=4'h1 |
| 3 | Core (BIGCORE0 or BIGCORE1) transfer idle state | PMU_CLUSTER_POWER_STS1[3:0] or [7:4]=4'h2 |
| 4 | Core (BIGCORE0 or BIGCORE1) power down state | PMU_CLUSTER_POWER_STS1[3:0] or [7:4]=4'h3 |
| 5 | DSU transfer idle state | PMU_CLUSTER_POWER_STS1[11:8]= 4'h1 |
| 6 | DSU power down state | PMU_CLUSTER_POWER_STS1[11:8]= 4'h2 |
| 7 | Q-Channel low power state | PMU_GLB_POWER_STS=4'h3 |
| 8 | Bus low power state | PMU_GLB_POWER_STS=4'h4 |
| 9 | DDR enters self-refresh mode for core-clock state | PMU_DDR_POWER_STS=4'h2 |
| 10 | DDR enters retention mode through RETON/RETOFF state | PMU_DDR_POWER_STS=4'h3 |
| 11 | Power domain power down start state | PMU_PWR_GATE_POWER_STS=3'h1 |
| 12 | Power domain power down running state | PMU_PWR_GATE_POWER_STS=3'h2 |
| 13 | Clock low frequency state | PMU_CRU_POWER_STS=4'h1 |
| 14 | PLL power down state | PMU_CRU_POWER_STS=4'h2 |
| 15 | Input clamp state | PMU_CRU_POWER_STS=4'h3 |
| 16 | Oscillator disable state | PMU_CRU_POWER_STS=4'h4 |
| 17 | Sleep state | PMU_GLB_POWER_STS=4'h8 |
| 18 | Wake up state | PMU_CRU_POWER_STS=4'h6 |
| 19 | Input clamp release state | PMU_CRU_POWER_STS=4'h7 |
| 20 | Oscillator enable state | PMU_CRU_POWER_STS=4'h8 |
| 21 | Clock high frequency state | PMU_CRU_POWER_STS=4'h9 |
| 22 | Wake up reset clear state | PMU_CRU_POWER_STS=4'ha |
| 24 | PLL power up state | PMU_CRU_POWER_STS=4'hc |

Rockchip Confidential

| Decode Value | PMU State | Register Description |
|---|---|---|
| 26 | Power domain power up start state | PMU_PWR_GATE_POWER_STS=3'h4 |
| 27 | Power domain power up running state | PMU_PWR_GATE_POWER_STS=3'h5 |
| 28 | DDR exits retention mode through RETON/RETOFF state | PMU_DDR_POWER_STS=4'h7 |
| 29 | DDR exits self-refresh mode for core-clock state | PMU_DDR_POWER_STS=4'h8 |
| 30 | Bus active state | PMU_GLB_POWER_STS=4'hc |
| 31 | Q-Channel active state | PMU_GLB_POWER_STS=4'hd |
| 32 | DSU wake up state | PMU_CLUSTER_POWER_STS1[11:8]= 4'h4 |
| 33 | DSU power up state | PMU_CLUSTER_POWER_STS1[11:8]= 4'h5 |
| 34 | DSU transfer resume state | PMU_CLUSTER_POWER_STS1[11:8]= 4'h6 |
| 35 | Core wake up state | PMU_CLUSTER_POWER_STS1[3:0] or [7:4]=4'h5 |
| 36 | Core power up state | PMU_CLUSTER_POWER_STS1[3:0] or [7:4]=4'h6 |
| 37 | Core transfer resume state | PMU_CLUSTER_POWER_STS1[3:0] or [7:4]=4'h7 |
| 38 | CPU power up state | PMU_CLUSTER_POWER_STS1[3:0] or [7:4]=4'h8 |
| 39 | DDR enters self-refresh mode for AXI-clock state | PMU_DDR_POWER_STS=4'h1 |
| 40 | DDR enters retention mode through RST_IOV state | PMU_DDR_POWER_STS=4'h4 |
| 41 | DDR exits retention mode through RST_IOV state | PMU_DDR_POWER_STS=4'h6 |
| 42 | DDR exits self-refresh mode for AXI-clock state | PMU_DDR_POWER_STS=4'h9 |

If PMU enters power mode 0, the debug information is decoded as below.

Table 7-7 PMU Debug Information Decode After Enter Power Mode 0

| Decode Value | PMU State |
|---|---|
| 1 | PD_PMU1 bus idle state |
| 2 | PD_PMU1 power down state |
| 3 | Clock low frequency state |
| 4 | Oscillator disable state |
| 5 | Sleep state |
| 6 | Wake up state |
| 7 | Oscillator enable state |
| 8 | Clock high frequency state |
| 9 | PD_PMU1 power up state |
| 10 | PD_PMU1 bus normal state |
| 11 | Wake up reset clear state |
| 12 | DDR exits retention mode through RST_IOV state |
| 13 | DDR exits retention mode through RETON/RETOFF state |

### 7.5.7 System Register

PMU support 8 system registers: PMU_SYS_REG0~PMU_SYS_REG7. These registers are placed on PD_PMU1. Software can use these registers to retain some information which is useful after wakeup from any mode. It is used for any mode when PD_PMU1 is power on.

Rockchip Confidential

# Chapter 8 MMU600

## 8.1 Overview

The MMU600 is a System-level Memory Management Unit (SMMU) that translates an input address to an output address. This translation is based on address mapping and memory attribute information that is available in the MMU600 internal registers and translation tables. The MMU600 implements the Arm SMMU architecture version 3.1, SMMUv3.1, as the *Arm® System Memory Management Unit Architecture Specification, SMMU architecture version 3.0 and version 3.1* defines.
The version of MMU600 is r2p2-00rel0. There are two MMU600 instances in RK3588, MMU600_PCIE and MMU600_PHP respectively. Their configurations are shown below:

Table 8-1 MMU600_PCIE Configuration

| Configuration Parameters | Value |
|---|---|
| TOPCFG_NO_OF_TBU | 2 |
| TCUCFG_QTW_ADDR_WIDTH | 48 |
| TCUCFG_QTW_DATA_WIDTH | 128 |
| TCUCFG_XLATE_SLOTS | 64 |
| TCUCFG_PTW_SLOTS | 16 |
| TCUCFG_CTW_SLOTS | 4 |
| TCUCFG_WCS1L0_DEPTH | 64 |
| TCUCFG_WCS1L1_DEPTH | 64 |
| TCUCFG_WCS1L2_DEPTH | 256 |
| TCUCFG_WCS1L3_DEPTH | 256 |
| TCUCFG_WCS2L0_DEPTH | 64 |
| TCUCFG_WCS2L1_DEPTH | 64 |
| TCUCFG_WCS2L2_DEPTH | 256 |
| TCUCFG_WCS2L3_DEPTH | 256 |
| TCUCFG_CC_DEPTH | 64 |
| TBUCFG_TBS_ADDR_WIDTH | 64 |
| TBUCFG_TBM_ADDR_WIDTH | 48 |
| TBUCFG_DATA_WIDTH | 128 |
| TBUCFG_UTLB_DEPTH | 32 |
| TBUCFG_MTLB_DEPTH | 256 |
| TBUCFG_MTLB_PARTS | 4 |
| TBUCFG_WOT_DEPTH | 16 |
| TBUCFG_ROT_DEPTH | 16 |
| TBUCFG_XLATE_SLOTS | 16 |
| TBUCFG_SID_WIDTH | 16 |
| TBUCFG_SSID_WIDTH | 20 |
| TBUCFG_LFIFO_DEPTH | 4 |
| TBUCFG_WBUF_DEPTH | 32 |

Table 8-2 MMU600_PHP Configuration

| Configuration Parameters | Value |
|---|---|
| TOPCFG_NO_OF_TBU | 1 |
| TCUCFG_QTW_ADDR_WIDTH | 48 |
| TCUCFG_QTW_DATA_WIDTH | 128 |
| TCUCFG_XLATE_SLOTS | 64 |
| TCUCFG_PTW_SLOTS | 16 |
| TCUCFG_CTW_SLOTS | 4 |
| TCUCFG_WCS1L0_DEPTH | 64 |
| TCUCFG_WCS1L1_DEPTH | 64 |
| TCUCFG_WCS1L2_DEPTH | 256 |
| TCUCFG_WCS1L3_DEPTH | 256 |

Rockchip Confidential

| Configuration Parameters | Value |
|---|---|
| TCUCFG_WCS2L0_DEPTH | 64 |
| TCUCFG_WCS2L1_DEPTH | 64 |
| TCUCFG_WCS2L2_DEPTH | 256 |
| TCUCFG_WCS2L3_DEPTH | 256 |
| TCUCFG_CC_DEPTH | 64 |
| TBUCFG_TBS_ADDR_WIDTH | 64 |
| TBUCFG_TBM_ADDR_WIDTH | 48 |
| TBUCFG_DATA_WIDTH | 128 |
| TBUCFG_UTLB_DEPTH | 32 |
| TBUCFG_MTLB_DEPTH | 256 |
| TBUCFG_MTLB_PARTS | 4 |
| TBUCFG_WOT_DEPTH | 16 |
| TBUCFG_ROT_DEPTH | 16 |
| TBUCFG_XLATE_SLOTS | 16 |
| TBUCFG_SID_WIDTH | 16 |
| TBUCFG_SSID_WIDTH | 20 |
| TBUCFG_LFIFO_DEPTH | 4 |
| TBUCFG_WBUF_DEPTH | 32 |

The MMU600 in RK3588 supports following feature:

- Compliance with the SMMUv3.1 architecture:
  - Support for Stage 1 translation, Stage 2 translation, and Stage 1 followed by stage 2 translation
  - Support for ARMv8 AArch32 and AArch64 translation table formats
  - Support for 4KB, 16KB and 64KB granule sizes in AArch64 format
  - Masters can be stalled while a processor handles translation faults, enabling software support for demand paging
  - Configuration tables in memory can support millions of active translation contexts
  - Queues in memory perform MMU600 management, no requirement to stall a processor when it accesses the MMU600
  - A Performance Monitoring Unit (PMU) in each TBU and TCU that enables MMU600 performance to be investigated
  - Reliability, Serviceability, and Availability (RAS) features for cache corruption detection and correction
- Support for AMBA interfaces, including:
  - AMBA DTI communication between the TCU and TBUs, enabling masters to request translations and implement TBU functionality internally
  - Support for the AMBA Low-Power Interface (LPI) Q-Channel so that standard controllers can control power and clock gating
  - AXI5 WAKEUP signaling on all interfaces, including DTI and APB interfaces
- Support for flexible integration:
  - You can place a configurable number of TBUs close to the masters being translated
  - Communication between TBU and TCU over AXI4-Stream, supported using the supplied DTI interconnect components, or any other AXI4-Stream interconnect
- Support for high-performance translation:
  - Scalable configurable micro TLB and Main TLB (MTLB) in the TBU can reduce the number of translation requests to the TCU
  - MTLB partitioning enable the use of MTLB entries to be managed outside the TBU, improving real-time translation performance
  - Optimization to store all architecturally defined page and block sizes, including contiguous page and block entries, as a single entry in the TBU and TCU TLBs
  - Per-TBU prioritization in the TCU enables high-priority transaction streams to be translated
  - TCU prefetch of translation tables, which can be enabled on a per-context basis, improving translation performance for real-time masters that access memory

Rockchip Confidential

linearly

- Hit-Under-Miss (HUM) support in the TBU enables transactions with different AXI IDs to be propagated out of order, when a translation is available
- TBU detection of multiple transactions that require the same translation so that only one TBU request to the TCU is required
- TCU detection of multiple translations that require the same table in memory so that only one TCU memory request is required
- Multi-level, multi-stage walk caches in the TCU reduce translation cost by performing only part of the table walk process on a miss
- A configurable number of concurrent translations in the TBU and TCU promotes high translation throughput

## 8.2 Block Diagram

The MMU600_PCIE is connected with five PCIe controllers and the MMU600_PHP is connected with USB3/GMAC/SATA controller. The Bridge_PCIe/Bridge_PHP will arbiter requests from various masters under first in first out method. As shown below:

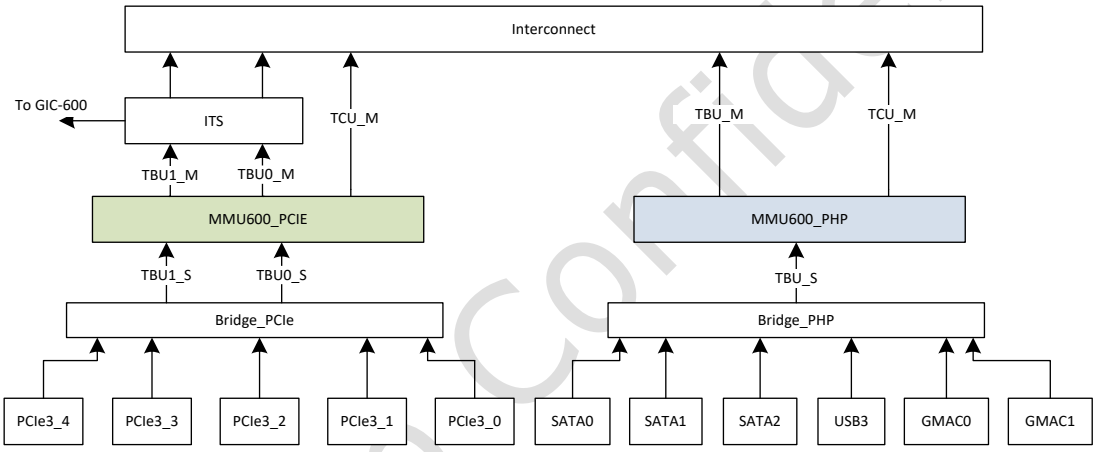



Fig. 8-1 Block Diagram

## 8.3 Function Description

Please refer to the document corelink_mmu600_system_memory_management_unit_technical_reference_manual_100310_0202_00_en.pdf for the detail function description.

Rockchip Confidential

# Chapter 9 MCU Subsystem

## 9.1 Overview

The MCU Subsystem embedded one MCU processor(Cortex-M0,r0p0-03rel0), a 16KB unified I/D cache, a tightly-coupled memory(TCM) and interrupt multiplexer(INTMUX). It allowed fast & efficient data exchange. And the Level 1 Instruction/Data Cache designed for MCU can improve the memory access performance significantly.
The following features may or may not be present in the actual product. Please contact Rockchip for the actual feature configurations and the third-party licensing requirements.
The MCU features and benefits are:

- One MCU processor
- Tightly-coupled memory(TCM)
- Optional debug support
  - Two hardware breakpoints
  - One watch points
  - Support Serial Wire debug connection
- Interrupt multiplexer(INTMUX)
  - Mux 8 interrupts from 512 interrupt sources using round-robin algorithm
  - Each 8 adjacent interrupts are seen as a group which share same INTMUX_INT_ENABLE_GROUPx and INTMUX_INT_FLAG_GROUPx register
- 16KB unified I/D Cache
  - Support 2-way set-associative with 32Byte cache line size
  - Support one 128bit AHB-Lite bus master interface to SoC interconnect
  - Support memory cacheable access and peripheral bypass access
  - Support Write-Through with No-Write-Allocate and Read-Allocate
  - Support Write-Back with Write-Allocate and Read-Allocate
  - Support cache maintenance operations (clean/invalidate/clean & invalidate) by address
  - Support cache invalidate/clean & invalidate operations for all cache lines
  - Support cache initialization by software configuration
  - Support RAM debug mode for tag RAM and data RAM
  - Support one interrupt source

There are three MCU subsystem in RK3588, PMU_M0, NPU_M0 and DDR_M0 respectively. Their main configurations are different, As shown below.

Table 9-1 MCU Subsystem Configurations

| | PMU_M0 | NPU_M0 | DDR_M0 |
|---|---|---|---|
| TCM | 16KB | 64KB | 32KB |
| CACHE | 16KB | 16KB | NA |
| IRQ_NUM | 32 | 16 | 8 |
| INTMUX | YES | NA | YES |

## 9.2 Block Diagram

The Int_in[511:0] will connect with all interrupt source of RK3588, and please refer to "Chapter System Overview" for the detail interrupt number. MCU Subsystem are shown below.

Rockchip Confidential

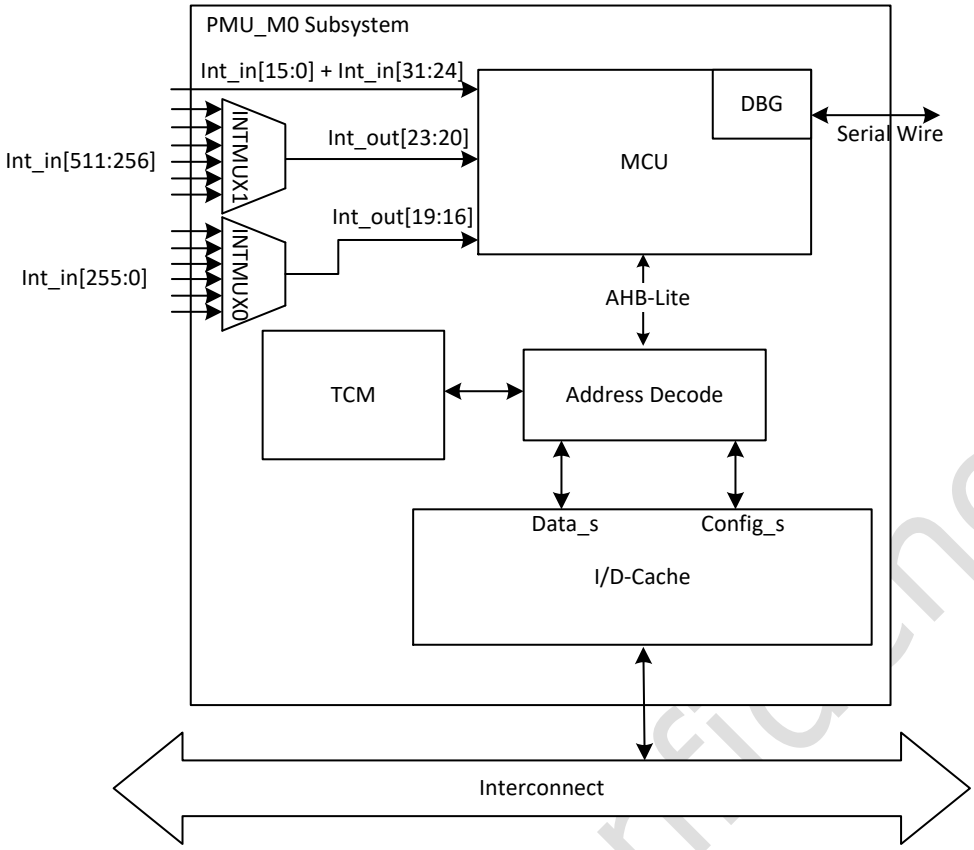
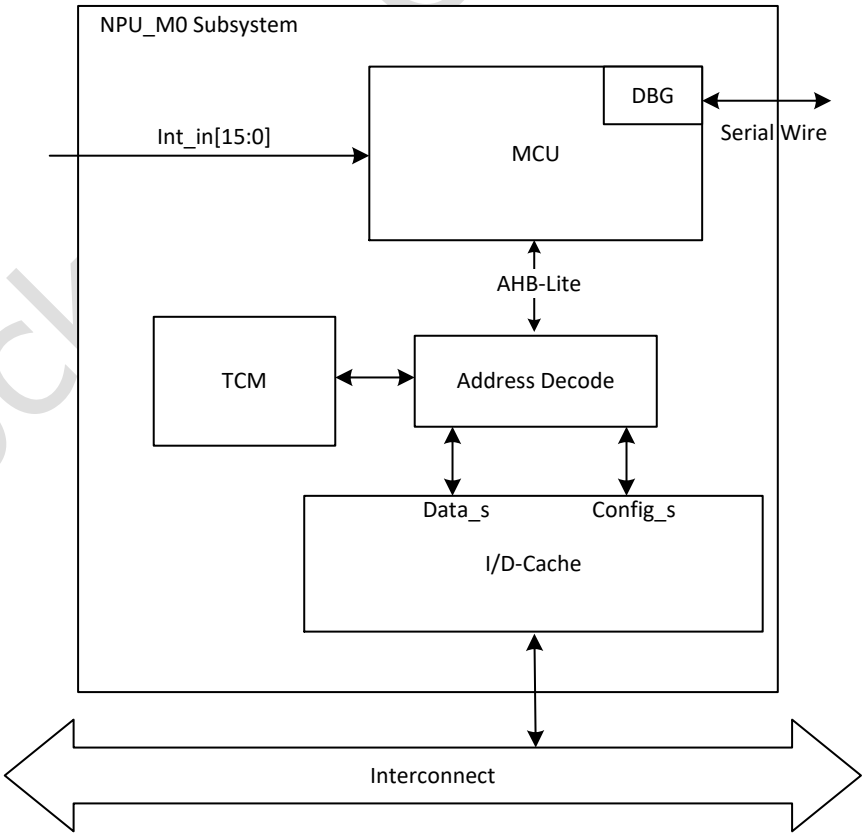



Fig. 9-1 Block Diagram of PMU_M0 Subsystem




Rockchip Confidential

Fig. 9-2 Block Diagram of NPU_M0 Subsystem

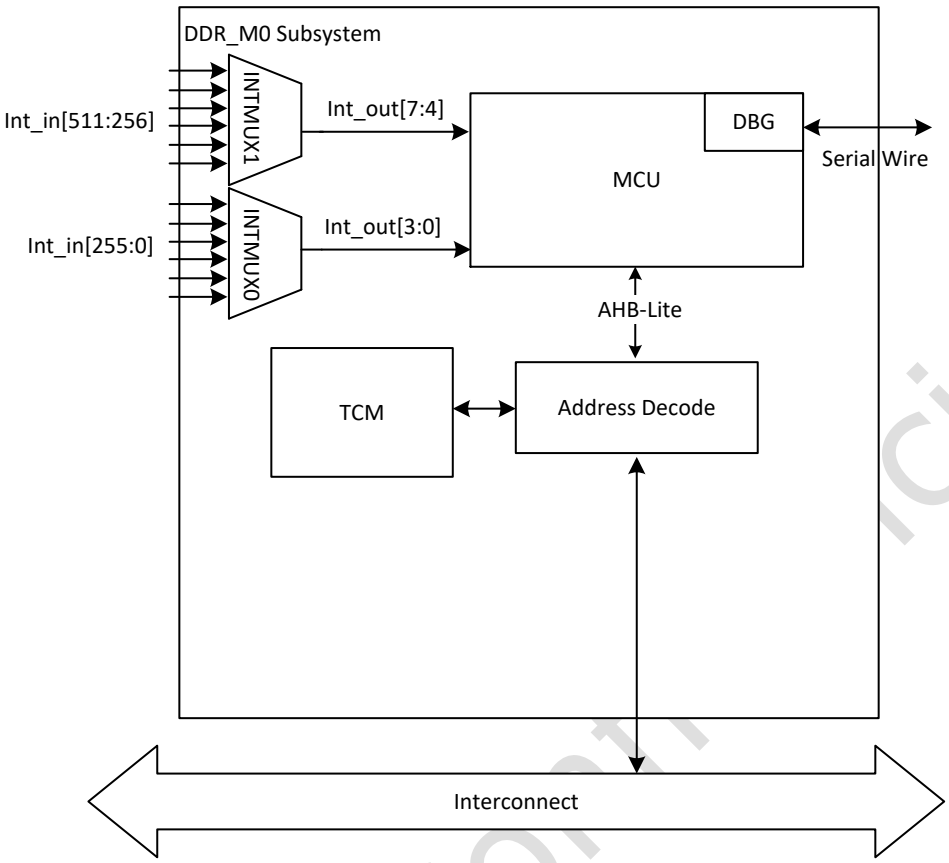



Fig. 9-3 Block Diagram of DDR_M0 Subsystem

## 9.3 Register Description

Software should read and write these registers using 32-bits accesses. Please note that the INTMUX0 and INTMUX1 are same instance, so they have same register list, but the base address of INTMUX0_PMU/INTMUX1_PMU/INTMUX0_DDR/INTMUX1_DDR are 0xFECF0000/0xFECF4000/0xFECF8000/0xFECFC0000 respectively. Every 64 interrupts as a group will be multiplexed into one INT to MCU in order.

### 9.3.1 Registers Summary(cache)

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CACHE_CACHE_CTRL | 0x0000 | W | 0x000006cc | Cache Control Register |
| CACHE_MAINTAIN0 | 0x0004 | W | 0x00000000 | Cache Maintain 0 Register |
| CACHE_MAINTAIN1 | 0x0008 | W | 0x00000000 | Cache Maintain 1 Register |
| CACHE_STB_TIMEOUT_CTRL | 0x000c | W | 0x4000000c | Store Buffer Timeout Control Register |
| CACHE_RAM_DEBUG | 0x0010 | W | 0x00000000 | Cache RAM Debug Register |
| CACHE_CACHE_INT_EN | 0x0020 | W | 0x00000000 | Cache Interrupt Enable Register |
| CACHE_CACHE_INT_ST | 0x0024 | W | 0x00000000 | Cache Interrupt Status Register |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CACHE_CACHE_ERR_HADDR | 0x0028 | W | 0x00000000 | Cache Error Address Register |
| CACHE_CACHE_STATUS | 0x0030 | W | 0x00000000 | Cache Status Register |
| CACHE_PMU_RD_NUM_CNT | 0x0040 | W | 0x00000000 | PMU Read Number Count Register |
| CACHE_PMU_WR_NUM_CNT | 0x0044 | W | 0x00000000 | PMU Write Number Count Register |
| CACHE_PMU_SRAM_RD_HIT_CNT | 0x0048 | W | 0x00000000 | PMU RAM Read Hit Count Register |
| CACHE_PMU_HB_RD_HIT_CNT | 0x004c | W | 0x00000000 | PMU Hot Buffer Read Hit Count Register |
| CACHE_PMU_STB_RD_HIT_CNT | 0x0050 | W | 0x00000000 | PMU Store Buffer Read Hit Count Register |
| CACHE_PMU_RD_HIT_CNT | 0x0054 | W | 0x00000000 | PMU Read Hit Count Register |
| CACHE_PMU_WR_HIT_CNT | 0x0058 | W | 0x00000000 | PMU Write Hit Count Register |
| CACHE_PMU_RD_MISS_PENALTY_CNT | 0x005c | W | 0x00000000 | PMU Read Miss Penalty Count Register |
| CACHE_PMU_WR_MISS_PENALTY_CNT | 0x0060 | W | 0x00000000 | PMU Write Miss Penalty Count Register |
| CACHE_PMU_RD_LAT_CNT | 0x0064 | W | 0x00000000 | PMU Read Latency Count Register |
| CACHE_PMU_WR_LAT_CNT | 0x0068 | W | 0x00000000 | PMU Write Latency Count Register |
| CACHE_REVISION | 0x00f0 | W | 0x00000100 | Cache Design Revision Register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

## 9.3.2 Detail Registers Description

**CACHE_CACHE_CTRL**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RO | 0x00000 | reserved |
| 13 | RW | 0x0 | cache_pf_en<br>Cache prefetch enable register.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | cache_mpu_mode<br>Cache MPU mode enable register. When this bit is set to 1, the cacheability policy is determined by MPU of Cortex-M4.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x6 | stb_entry_thresh<br>Store buffer entry threshold control register. The depth of the store buffer entry is 8. When the number of the used data entries is greater than or equal to threshold value, the write data will be written to Cache RAM. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x1 | stb_timeout_en<br>Store buffer timeout enable register. When this bit is set to 1, the data in the store buffer must be flushed to Cache RAM if the counter value is equal to the timeout value.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x1 | cache_bypass<br>Cache bypass mode enable register. When this bit is set to 1, data will bypass the Cache.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | cache_pmu_en<br>Cache Performance Monitor Unit enable register.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | cache_flush<br>Cache flush enable register. When this bit is set to 1, the dirty data is flushed to external memory and the cache line are invalidated.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x1 | cache_stb_en<br>Cache store buffer enable register. This bit must be set to 0 when Write-Through mode is selected and must be set to 1 when Write-Back mode is selected.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x1 | cache_hb_en<br>Cache hot buffer enable register.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | cache_wt_en<br>Cache mode control register.<br>1'b0: Write-Back<br>1'b1: Write-Through |
| 0 | RW | 0x0 | cache_en<br>Cache initialization enable register.<br>1'b0: Disable<br>1'b1: Enable |

**CACHE_MAINTAIN0**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RW | 0x0000000 | cache_m_addr<br>Cache maintain start address. This address is 32Byte cache line aligned, that is, the bits[4:0] are always 0. |
| 4:3 | RO | 0x0 | reserved |
| 2:1 | RW | 0x0 | cache_m_cmd<br>Cache maintain command register.<br>2'b00: Clean by address<br>2'b01: Invalidate by address<br>2'b10: Clean and Invalidate by address<br>2'b11: Invalidate all |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | WO | 0x0 | cache_m_valid<br>Cache maintain valid register. The maintenance operation is valid only when this bit is set to 1. |

**CACHE_MAINTAIN1**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:27 | RO | 0x00 | reserved |
| 26:0 | RW | 0x0000000 | cache_m_offset<br>Cache maintain offset. This bit field indicates the end offset of cache line, that is, the value plus 1 determines the number of cache line to be maintained. The bit field of cache_m_addr is treated as the start offset of cache line, so the maintain address range is from (cache_m_addr * 32) to (cache_m_addr * 32 + 31 + cache_m_offset * 32). |

**CACHE_STB_TIMEOUT_CTRL**

Address: Operational Base + offset (0x000c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x4000000c | stb_timeout_value<br>Store buffer timeout value. |

**CACHE_RAM_DEBUG**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | ram_debug_en<br>Cache RAM debug mode enable register.<br>1'b0: Disable<br>1'b1: Enable |

**CACHE_CACHE_INT_EN**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | err_record_en<br>AHB master bus error record enable.<br>1'b0: Disable<br>1'b1: Enable |

**CACHE_CACHE_INT_ST**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | ahb_error_status<br>Error status bit for AHB master bus.<br>1'b0: Nothing<br>1'b1: Bus error |

**CACHE_CACHE_ERR_HADDR**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RO | 0x0 | status_haddr<br>Recent record of AHB bus error address. |

Rockchip Confidential

**CACHE_CACHE_STATUS**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2 | RO | 0x0 | cache_flush_done<br>Cache flush done status register.<br>1'b0: Nothing<br>1'b1: Flush done |
| 1 | RO | 0x0 | cache_m_busy<br>Cache maintain busy status register.<br>1'b0: Idle<br>1'b1: Busy |
| 0 | RO | 0x0 | cache_init_finish<br>Cache initialization finish status register.<br>1'b0: Cache is uninitialized<br>1'b1: Cache is initialized |

**CACHE_PMU_RD_NUM_CNT**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | pmu_rd_num_cnt<br>Total count of read transfers. |

**CACHE_PMU_WR_NUM_CNT**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | pmu_wr_num_cnt<br>Total count of write transfers. |

**CACHE_PMU_SRAM_RD_HIT_CNT**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | pmu_ram_rd_hit_cnt<br>Count of read hits on Cache RAM. |

**CACHE_PMU_HB_RD_HIT_CNT**

Address: Operational Base + offset (0x004c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | pmu_hb_rd_hit_cnt<br>Count of read hits on hot buffer. |

**CACHE_PMU_STB_RD_HIT_CNT**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | pmu_stb_rd_hit_cnt<br>Count of read hits on store buffer. |

**CACHE_PMU_RD_HIT_CNT**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | pmu_rd_hit_cnt<br>Total count of read hits. |

**CACHE_PMU_WR_HIT_CNT**

Address: Operational Base + offset (0x0058)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | pmu_wr_hit_cnt<br>Total count of write hits. |

**CACHE_PMU_RD_MISS_PENALTY_CNT**

Address: Operational Base + offset (0x005c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | pmu_rd_miss_penalty_cnt<br>Total count of read miss penalty (in clock cycles). |

**CACHE_PMU_WR_MISS_PENALTY_CNT**

Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | pmu_wr_miss_penalty_cnt<br>Total count of write miss penalty (in clock cycles). |

**CACHE_PMU_RD_LAT_CNT**

Address: Operational Base + offset (0x0064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | pmu_rd_lat_cnt<br>Total count of read latency (in clock cycles). |

**CACHE_PMU_WR_LAT_CNT**

Address: Operational Base + offset (0x0068)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | pmu_wr_lat_cnt<br>Total count of write latency (in clock cycles). |

**CACHE_REVISION**

Address: Operational Base + offset (0x00f0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000100 | revision<br>Cache revision number. |

## 9.3.3 Registers Summary (INTMUX)

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| INTMUX_INT_ENABLE_GROUP0 | 0x0000 | W | 0x00000000 | Interrupt Group0 Enable Register |
| INTMUX_INT_ENABLE_GROUP1 | 0x0004 | W | 0x00000000 | Interrupt Group1 Enable Register |
| INTMUX_INT_ENABLE_GROUP2 | 0x0008 | W | 0x00000000 | Interrupt Group2 Enable Register |
| INTMUX_INT_ENABLE_GROUP3 | 0x000c | W | 0x00000000 | Interrupt Group3 Enable Register |
| INTMUX_INT_ENABLE_GROUP4 | 0x0010 | W | 0x00000000 | Interrupt Group4 Enable Register |
| INTMUX_INT_ENABLE_GROUP5 | 0x0014 | W | 0x00000000 | Interrupt Group5 Enable Register |
| INTMUX_INT_ENABLE_GROUP6 | 0x0018 | W | 0x00000000 | Interrupt Group6 Enable Register |
| INTMUX_INT_ENABLE_GROUP7 | 0x001c | W | 0x00000000 | Interrupt Group7 Enable Register |
| INTMUX_INT_ENABLE_GROUP8 | 0x0020 | W | 0x00000000 | Interrupt Group8 Enable Register |

Rockchip Confidencial

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| INTMUX_INT_ENABLE_GROUP9 | 0x0024 | W | 0x00000000 | Interrupt Group9 Enable Register |
| INTMUX_INT_ENABLE_GROUP10 | 0x0028 | W | 0x00000000 | Interrupt Group10 Enable Register |
| INTMUX_INT_ENABLE_GROUP11 | 0x002c | W | 0x00000000 | Interrupt Group11 Enable Register |
| INTMUX_INT_ENABLE_GROUP12 | 0x0030 | W | 0x00000000 | Interrupt Group12 Enable Register |
| INTMUX_INT_ENABLE_GROUP13 | 0x0034 | W | 0x00000000 | Interrupt Group13 Enable Register |
| INTMUX_INT_ENABLE_GROUP14 | 0x0038 | W | 0x00000000 | Interrupt Group14 Enable Register |
| INTMUX_INT_ENABLE_GROUP15 | 0x003c | W | 0x00000000 | Interrupt Group15 Enable Register |
| INTMUX_INT_ENABLE_GROUP16 | 0x0040 | W | 0x00000000 | Interrupt Group16 Enable Register |
| INTMUX_INT_ENABLE_GROUP17 | 0x0044 | W | 0x00000000 | Interrupt Group17 Enable Register |
| INTMUX_INT_ENABLE_GROUP18 | 0x0048 | W | 0x00000000 | Interrupt Group18 Enable Register |
| INTMUX_INT_ENABLE_GROUP19 | 0x004c | W | 0x00000000 | Interrupt Group19 Enable Register |
| INTMUX_INT_ENABLE_GROUP20 | 0x0050 | W | 0x00000000 | Interrupt Group20 Enable Register |
| INTMUX_INT_ENABLE_GROUP21 | 0x0054 | W | 0x00000000 | Interrupt Group21 Enable Register |
| INTMUX_INT_ENABLE_GROUP22 | 0x0058 | W | 0x00000000 | Interrupt Group22 Enable Register |
| INTMUX_INT_ENABLE_GROUP23 | 0x005c | W | 0x00000000 | Interrupt Group23 Enable Register |
| INTMUX_INT_ENABLE_GROUP24 | 0x0060 | W | 0x00000000 | Interrupt Group24 Enable Register |
| INTMUX_INT_ENABLE_GROUP25 | 0x0064 | W | 0x00000000 | Interrupt Group25 Enable Register |
| INTMUX_INT_ENABLE_GROUP26 | 0x0068 | W | 0x00000000 | Interrupt Group26 Enable Register |
| INTMUX_INT_ENABLE_GROUP27 | 0x006c | W | 0x00000000 | Interrupt Group27 Enable Register |
| INTMUX_INT_ENABLE_GROUP28 | 0x0070 | W | 0x00000000 | Interrupt Group28 Enable Register |
| INTMUX_INT_ENABLE_GROUP29 | 0x0074 | W | 0x00000000 | Interrupt Group29 Enable Register |
| INTMUX_INT_ENABLE_GROUP30 | 0x0078 | W | 0x00000000 | Interrupt Group30 Enable Register |
| INTMUX_INT_ENABLE_GROUP31 | 0x007c | W | 0x00000000 | Interrupt Group31 Enable Register |
| INTMUX_INT_FLAG_GROUP0 | 0x0080 | W | 0x00000000 | Interrupt Group0 Flag Register |
| INTMUX_INT_FLAG_GROUP1 | 0x0084 | W | 0x00000000 | Interrupt Group1 Flag Register |
| INTMUX_INT_FLAG_GROUP2 | 0x0088 | W | 0x00000000 | Interrupt Group2 Flag Register |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| INTMUX_INT_FLAG_GROUP3 | 0x008c | W | 0x00000000 | Interrupt Group3 Flag Register |
| INTMUX_INT_FLAG_GROUP4 | 0x0090 | W | 0x00000000 | Interrupt Group4 Flag Register |
| INTMUX_INT_FLAG_GROUP5 | 0x0094 | W | 0x00000000 | Interrupt Group5 Flag Register |
| INTMUX_INT_FLAG_GROUP6 | 0x0098 | W | 0x00000000 | Interrupt Group6 Flag Register |
| INTMUX_INT_FLAG_GROUP7 | 0x009c | W | 0x00000000 | Interrupt Group7 Flag Register |
| INTMUX_INT_FLAG_GROUP8 | 0x00a0 | W | 0x00000000 | Interrupt Group8 Flag Register |
| INTMUX_INT_FLAG_GROUP9 | 0x00a4 | W | 0x00000000 | Interrupt Group9 Flag Register |
| INTMUX_INT_FLAG_GROUP10 | 0x00a8 | W | 0x00000000 | Interrupt Group10 Flag Register |
| INTMUX_INT_FLAG_GROUP11 | 0x00ac | W | 0x00000000 | Interrupt Group11 Flag Register |
| INTMUX_INT_FLAG_GROUP12 | 0x00b0 | W | 0x00000000 | Interrupt Group12 Flag Register |
| INTMUX_INT_FLAG_GROUP13 | 0x00b4 | W | 0x00000000 | Interrupt Group13 Flag Register |
| INTMUX_INT_FLAG_GROUP14 | 0x00b8 | W | 0x00000000 | Interrupt Group14 Flag Register |
| INTMUX_INT_FLAG_GROUP15 | 0x00bc | W | 0x00000000 | Interrupt Group15 Flag Register |
| INTMUX_INT_FLAG_GROUP16 | 0x00c0 | W | 0x00000000 | Interrupt Group16 Flag Register |
| INTMUX_INT_FLAG_GROUP17 | 0x00c4 | W | 0x00000000 | Interrupt Group17 Flag Register |
| INTMUX_INT_FLAG_GROUP18 | 0x00c8 | W | 0x00000000 | Interrupt Group18 Flag Register |
| INTMUX_INT_FLAG_GROUP19 | 0x00cc | W | 0x00000000 | Interrupt Group19 Flag Register |
| INTMUX_INT_FLAG_GROUP20 | 0x00d0 | W | 0x00000000 | Interrupt Group20 Flag Register |
| INTMUX_INT_FLAG_GROUP21 | 0x00d4 | W | 0x00000000 | Interrupt Group21 Flag Register |
| INTMUX_INT_FLAG_GROUP22 | 0x00d8 | W | 0x00000000 | Interrupt Group22 Flag Register |
| INTMUX_INT_FLAG_GROUP23 | 0x00dc | W | 0x00000000 | Interrupt Group23 Flag Register |
| INTMUX_INT_FLAG_GROUP24 | 0x00e0 | W | 0x00000000 | Interrupt Group24 Flag Register |
| INTMUX_INT_FLAG_GROUP25 | 0x00e4 | W | 0x00000000 | Interrupt Group25 Flag Register |
| INTMUX_INT_FLAG_GROUP26 | 0x00e8 | W | 0x00000000 | Interrupt Group26 Flag Register |
| INTMUX_INT_FLAG_GROUP27 | 0x00ec | W | 0x00000000 | Interrupt Group27 Flag Register |
| INTMUX_INT_FLAG_GROUP28 | 0x00f0 | W | 0x00000000 | Interrupt Group28 Flag Register |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| INTMUX_INT_FLAG_GROUP29 | 0x00f4 | W | 0x00000000 | Interrupt Group29 Flag Register |
| INTMUX_INT_FLAG_GROUP30 | 0x00f8 | W | 0x00000000 | Interrupt Group30 Flag Register |
| INTMUX_INT_FLAG_GROUP31 | 0x00fc | W | 0x00000000 | Interrupt Group31 Flag Register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

## 9.3.4 Detail Registers Description

### INTMUX_INT_ENABLE_GROUP0

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

### INTMUX_INT_ENABLE_GROUP1

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

### INTMUX_INT_ENABLE_GROUP2

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

### INTMUX_INT_ENABLE_GROUP3

Address: Operational Base + offset (0x000c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

### INTMUX_INT_ENABLE_GROUP4

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

Rockchip Confidential

**INTMUX_INT_ENABLE_GROUP5**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP6**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP7**

Address: Operational Base + offset (0x001c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP8**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP9**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP10**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP11**

Rockchip Confidencial

Address: Operational Base + offset (0x002c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP12**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP13**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP14**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP15**

Address: Operational Base + offset (0x003c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP16**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP17**

Address: Operational Base + offset (0x0044)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP18**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP19**

Address: Operational Base + offset (0x004c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP20**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP21**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP22**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP23**

Address: Operational Base + offset (0x005c)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP24**

Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP25**

Address: Operational Base + offset (0x0064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP26**

Address: Operational Base + offset (0x0068)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP27**

Address: Operational Base + offset (0x006c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP28**

Address: Operational Base + offset (0x0070)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP29**

Address: Operational Base + offset (0x0074)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP30**

Address: Operational Base + offset (0x0078)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_ENABLE_GROUP31**

Address: Operational Base + offset (0x007c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | enable<br>Each bit represents one interrupt enable bit.<br>1'b0: Interrupt disabled<br>1'b1: Interrupt enabled |

**INTMUX_INT_FLAG_GROUP0**

Address: Operational Base + offset (0x0080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP1**

Address: Operational Base + offset (0x0084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP2**

Address: Operational Base + offset (0x0088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP3**

Address: Operational Base + offset (0x008c)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP4**

Address: Operational Base + offset (0x0090)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP5**

Address: Operational Base + offset (0x0094)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP6**

Address: Operational Base + offset (0x0098)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP7**

Address: Operational Base + offset (0x009c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP8**

Address: Operational Base + offset (0x00a0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP9**

Address: Operational Base + offset (0x00a4)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP10**

Address: Operational Base + offset (0x00a8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP11**

Address: Operational Base + offset (0x00ac)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP12**

Address: Operational Base + offset (0x00b0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP13**

Address: Operational Base + offset (0x00b4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP14**

Address: Operational Base + offset (0x00b8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP15**

Address: Operational Base + offset (0x00bc)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP16**

Address: Operational Base + offset (0x00c0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP17**

Address: Operational Base + offset (0x00c4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP18**

Address: Operational Base + offset (0x00c8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP19**

Address: Operational Base + offset (0x00cc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP20**

Address: Operational Base + offset (0x00d0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP21**

Address: Operational Base + offset (0x00d4)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP22**

Address: Operational Base + offset (0x00d8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP23**

Address: Operational Base + offset (0x00dc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP24**

Address: Operational Base + offset (0x00e0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP25**

Address: Operational Base + offset (0x00e4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP26**

Address: Operational Base + offset (0x00e8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP27**

Address: Operational Base + offset (0x00ec)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP28**

Address: Operational Base + offset (0x00f0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP29**

Address: Operational Base + offset (0x00f4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP30**

Address: Operational Base + offset (0x00f8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

**INTMUX_INT_FLAG_GROUP31**

Address: Operational Base + offset (0x00fc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | flag<br>Each bit represents one interrupt is in service.<br>1'b0: Interrupt in service<br>1'b1: Interrupt out of service |

## 9.4 Interface Description

There are two sets of serial debug interface for the three MCUs. When we debug using serial wire, not only set IOMUX, but also configure the bit[11:10] of SYS_GRF_SOC_CON10 to select the MCU that you want to debug.

Rockchip Confidencial

Table 9-2 MCU Serial Wire Debug Interface Description

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| mcujtag_tckm0 | I | SDMMC_CMD/PDM1_CLK1_M0/MCU_JTAG_TCK_M0/CAN0_TX_M1/UART5_RX_M0/PWM7_IR_M1/GPIO4_D4_u | BUS_IOC_GPIO4D_IOMUX_SEL_H[3:0] = 4'h5 |
| mcujtag_tmsm0 | I/O | SDMMC_CLK/PDM1_CLK0_M0/TEST_CLKOUT_M0/MCU_JTAG_TMS_M0/CAN0_RX_M1/UART5_TX_M0/GPIO4_D5_d | BUS_IOC_GPIO4D_IOMUX_SEL_H[7:4] = 4'h5 |
| mcujtag_tckm1 | I | HDMI_TX0_HPD_M1/PCIE30X2_PERSTN_M2/HDMI_RX_HPDOUT_M1/MCU_JTAG_TCK_M1/UART9_RX_M2/SPI0_CS0_M3/GPIO3_D4_d | BUS_IOC_GPIO3D_IOMUX_SEL_H[3:0] = 4'h6 |
| mcujtag_tmsm1 | I/O | PCIE30X4_BUTTON_RSTN/DP1_HPDIN_M0/MCU_JTAG_TMS_M1/UART9_TX_M2/PWM11_IR_M3/SPI0_CS1_M3/GPIO3_D5_d | BUS_IOC_GPIO3D_IOMUX_SEL_H[7:4] = 4'h6 |

*Notes: I=input, O=output, I/O=input/output, bidirectional*

# 9.5 Application Notes

## 9.5.1 Clock and Reset Generation

Please refer to "Chapter CRU" for more detailed information.

## 9.5.2 Memory Remap

The memory map is divided into different memory types for different usage.
To avoid the memory map conflict between different processors, the source space can be remap to another. In addition, these remap operation could not take effect until the MCU soft reset.

Table 9-3 PMU_M0 Address Remap

| Before Remap | Memory Type | Usage | After Remap |
|---|---|---|---|
| 0xA0000000 - 0xDFFFFFFF | Device XN | Peripherals | Before Remap - 0xA0000000 + {pmu1_sgrf_soc_con12[15:0],16'h0} |
| 0x80000000 - 0x9FFFFFFF | Normal WT | Off chip RAM | Before Remap - 0x60000000 + {pmu1_sgrf_soc_con11[15:0],16'h0} |
| 0x60000000 - 0x7FFFFFFF | Normal WBWA | Off chip RAM | Before Remap - 0x60000000 + {pmu1_sgrf_soc_con11[15:0],16'h0} |
| 0x40000000 - 0x5FFFFFFF | Device XN | Peripherals | Before Remap - 0x40000000 + 0xF0000000 |
| 0x20000000 - 0x3FFFFFFF | Normal WBWA | On chip RAM | Before Remap - 0x20000000 + {pmu1_sgrf_soc_con10[15:0],16'h0} |
| 0x00000000 - 0x1FFFFFFF | Normal WT | ROM or flash | Before Remap - 0x0000000 + {pmu1_sgrf_soc_con9[15:0],16'h0} |

Table 9-4 NPU_M0 Address Remap

| Before Remap | Memory Type | Usage | After Remap |
|---|---|---|---|
| 0xA0000000 - 0xDFFFFFFF | Device XN | Peripherals | Before Remap - 0xA0000000 + {bus_sgrf_mcu_con1[15:0],16'h0} |
| 0x80000000 - 0x9FFFFFFF | Normal WT | Off chip RAM | Before Remap - 0x60000000 + {bus_sgrf_mcu_con2[15:0],16'h0} |
| 0x60000000 - 0x7FFFFFFF | Normal WBWA | Off chip RAM | Before Remap - 0x60000000 + {bus_sgrf_mcu_con2[15:0],16'h0} |
| 0x40000000 - 0x5FFFFFFF | Device XN | Peripherals | Before Remap - 0x40000000 + 0xF0000000 |
| 0x20000000 - 0x3FFFFFFF | Normal WBWA | On chip RAM | Before Remap - 0x20000000 + {bus_sgrf_mcu_con3[15:0],16'h0} |
| 0x00000000 - 0x1FFFFFFF | Normal WT | ROM or flash | Before Remap - 0x0000000 + {bus_sgrf_mcu_con0[15:0],16'h0} |

Table 9-5 DDR_M0 Address Remap

| Before Remap | Memory Type | Usage | After Remap |
|---|---|---|---|
| 0xA0000000 - 0xDFFFFFFF | Device XN | Peripherals | Before Remap - 0xA0000000 + {bus_sgrf_mcu_con6[15:0],16'h0} |
| 0x80000000 - 0x9FFFFFFF | Normal WT | Off chip RAM | Before Remap - 0x60000000 + {bus_sgrf_mcu_con7[15:0],16'h0} |

Rockchip Confidential

| | | | |
|---|---|---|---|
| 0x60000000 - 0x7FFFFFFF | Normal WBWA | Off chip RAM | Before Remap - 0x60000000 + {bus_sgrf_mcu_con7[15:0],16'h0} |
| 0x40000000 - 0x5FFFFFFF | Device XN | Peripherals | Before Remap - 0x40000000 + 0xF0000000 |
| 0x20000000 - 0x3FFFFFFF | Normal WBWA | On chip RAM | Before Remap - 0x20000000 + {bus_sgrf_mcu_con8[15:0],16'h0} |
| 0x00000000 - 0x1FFFFFFF | Normal WT | ROM or flash | Before Remap - 0x0000000 + {bus_sgrf_mcu_con5[15:0],16'h0} |

*Notes:*

- XN means execute-never.
- WT means write-through.
- WBWA means write-back-write-allocate.
- WT means write-through

## 9.5.3 Interrupt for MCU

Table 9-6 DDR_M0 Interrupt

| IRQ ID | IRQ Source | IRQ ID | IRQ Source |
|---|---|---|---|
| 0 | Int_in[63:0] | 4 | Int_in[319:256] |
| 1 | Int_in[127:64] | 5 | Int_in[383:320] |
| 2 | Int_in[191:128] | 6 | Int_in[447:384] |
| 3 | Int_in[255:192] | 7 | Int_in[511:448] |

The Int_in[511:0] are system interrupts, and each 64 interrupts will multiplexed into one interrupt which connect to one DDR_M0 IRQ lines. Please refer to "Chapter System Overview" for the detail interrupt number.

Table 9-7 PMU_M0 Interrupt

| IRQ ID | IRQ Source | IRQ ID | IRQ Source |
|---|---|---|---|
| 0 | PMIC | 11 | PWM0 |
| 1 | SDMMC_DETECTN | 12 | WDT_PMU |
| 2 | UART0 | 13 | TIMER1_PMU |
| 3 | GPIO0 | 14 | TIMER0_PMU |
| 4 | GPIO0_EXP | 15 | CRC_CHK_RST_REQ_PMU0_SGRF\| CRC_CHK_RST_REQ_PMU1SGRF |
| 5 | I2C0 | 16-23 | INTMUX_OUT |
| 6 | VAD | 24 | HPTIMER_PMU0 |
| 7 | PDM0 | 25 | OSC_CHK_RST_REQ |
| 8 | I2S1_8CH | 26 | CACHE_PMU |
| 9 | PVTM_PMU | 27-31 | RESERVED |
| 10 | PWM0_PWR | | |

The INTMUX_OUT are multiplexed from 512 system interrupts.

Table 9-8 NPU_M0 Interrupt

| IRQ ID | IRQ Source | IRQ ID | IRQ Source |
|---|---|---|---|
| 0 | Timer0_NPU | 5 | C1_RKNN |
| 1 | Timer1_NPU | 6 | C2_RKNN |
| 2 | PVTM_NPU | 7 | CACHE_NPU |
| 3 | WDT_NPU | 8-11 | MAILBOX2_AP |
| 4 | C0_RKNN | 12-15 | MAILBOX2_BB |

The 16 interrupts are connected to NPU_M0 without INTMUX directly.

## 9.5.4 Cache Initialization

The Cache is bypassed after reset and need to be initialized by the MCU. The basic initialization flow is:

1. Configure to Write-Back or Write-Through mode by setting CACHE_CTRL.cache_wt_en

Rockchip Confidential

and start initialization by configuring CACHE_CTRL.cache_en to high while keeping the Cache in bypass mode (CACHE_CTRL.cache_bypass is high). The store buffer must and only can be enabled for Write-Back mode, so you must disable the store buffer when Write-Through mode is selected. You can also enable the hot buffer for better performance. It is recommended that configure the I-Cache to Write-Through mode and configure the D-Cache to Write-Back mode.

2. Wait for cache initialization to be finished by polling CACHE_STATUS.cache_init_finish.
3. Disable cache bypass mode by configuring CACHE_CTRL.cache_bypass to low. Now that the Cache is enabled.
4. Simply configure CACHE_CTRL.cache_bypass to bypass or enable the Cache again after the initialization flow.

### 9.5.5 Cache Maintenance

The Cache Controller support the following cache maintenance operations:

- Clean by address: push the specified cache line data to external memory if it is valid and dirty.
- Invalidate by address: unconditionally clear the valid and dirty data of the specified cache lines.
- Clean and invalidate by address: clean and then invalidate the specified cache lines.
- Invalidate all: unconditionally clear the valid and dirty data for all the cache lines.
- Clean and invalidate all (Flush): clean and then invalidate all the cache lines.

  For the operation of cache clean and invalidate all, configure CACHE_CTRL.cache_flush to high first, and then wait for flush to be done by polling CACHE_STATUS.cache_flush_done. Finally, if the flush is done, you should configure CACHE_CTRL.cache_flush to low.

For the other four maintenance operations, you should set the maintenance command and the address range of the cache lines by configuring CACHE_MAINTAIN0 and CACHE_MAINTAIN1, then start by configuring CACHE_MAINTAIN0.cache_m_valid to high. When the operation is finished, CACHE_MAINTAIN0.cache_m_valid will be automatically cleared to low. You can also poll CACHE_STATUS.cache_m_busy to judge whether the operation is done.

### 9.5.6 Cache RAM Debug Mode

When the Cache is enabled and not in the bypass mode, you can enter the cache RAM debug mode by configuring CACHE_RAM_DEBUG.ram_debug_en to high. In the RAM debug mode, the cache RAM can be accessed directly by the specific address, and all the other cacheable memory accesses are bypassed because the cache core is disabled.

The following table shows the address map for the cache RAM debug.

Table 9-6 Address Map for the Cache RAM Debug

| RAM Access Type | RAM Access Size | Address Range for Cache RAM Debug |
|---|---|---|
| Reserved | 7KB | 0xF6F26400 ~ 0xF6F27FFF |
| TAG RAM1 | 1KB | 0xF6F26000 ~ 0xF6F263FF |
| Reserved | 7KB | 0xF6F24400 ~ 0xF6F25FFF |
| TAG RAMCU | 1KB | 0xF6F24000 ~ 0xF6F243FF |
| DATA RAM1 | 8KB | 0xF6F22000 ~ 0xF6F23FFF |
| DATA RAMCU | 8KB | 0xF6F20000 ~ 0xF6F21FFF |

As shown in the above table, there are 2 ways for each cache, and the size of one DATA RAM is 8KB. The following explanation may help you use the RAM debug method:

- Using the word-aligned address to access the TAG RAM.
- The bits[9:2] of the TAG RAM address are acted as the bits[12:5] of the corresponding memory address.
- Only the bits[20:0] of the TAG RAM data are available, and the bits[31:21] are always zero.

Rockchip Confidential

  - The bit[20] is the valid flag bit.
  - The bit[19] is the dirty flag bit.
  - The bits[18:0] are acted as the bits[31:13] of the corresponding memory address.
- The bits[12:0] of the DATA RAM address are acted as the bits[12:0] of the corresponding memory address.
- In order to get the cache line data at the wanted address, you should read the both of the TAG RAMs to find the matched address, and then read data from the corresponding DATA RAM.
- If write data to the DATA RAM, 8 copies of the 32bit data on the AHB bus will be written to the 32Byte cache line.

### 9.5.7 TCM

All MCU Subsystem implement data/instructions tightly-coupled memory to speed up code execute, but only MCU can access TCM. In addition, the base address of TCM are configurable to ease software. Refer to pmu1_sgrf_soc_con13/bus_sgrf_mcu_con4/bus_sgrf_mcu_con9 for more detail.

### 9.5.8 Other Hints

One interrupt request source is supported for the I/D-Cache, so you can query the interrupt register in the ISR if it is enabled. When CACHE_INT_EN.err_record_en is high, the Cache will generate a bus error interrupt if access to a wrong address. You can read CACHE_INT_ST.ahb_error_status for the cache interrupt status and get the recent error address information from CACHE_ERR_HADDR.status_haddr.

Rockchip Confidential

# Chapter 10 Timer

## 10.1 Overview

TIMER is a programmable timer peripheral. This component is an APB slave device. In RK3588, there are three types of TIMER according to the count type, which are normal decrement count TIMER, normal increment count TIMER and special function increment count TIMER. The normal decrement count TIMER is called NDCTIMER. The normal increment count TIMER is called NICTIMER. The special function increment count TIMER is called HPTIMER(High Precision TIMER).

5 normal decrement count TIMERs and 1 normal increment count TIMER constitute a 6-channel TIMER. In 6-channel TIMER, TIMER5 is the normal increment count TIMER, and the other channel TIMER is the normal decrement count TIMER.

2 normal increment count TIMERs form a 2-channel TIMER.

HPTIMER has calibration function and provides count value for CPU.

Timer supports the following features:

- All three kinds of counter support 32 bits APB slave.
- All three kinds of counter loading count value support configurable.
- All three kinds of counter support two counting modes: free-running and user-defined count.
- All three kinds of counters support maskable interrupts.
- HPTIMER with three timer mode: Normal, Hardware adjust, Software adjust.
- Hardware adjust mode HPTIMER can be calibrated back to the exact count value without software calculation.
- Software adjust mode HPTIMER can be calibrated back to the exact count value with software-aided calculation.
- Common multiples of slow and fast clock cycles are configurable.

## 10.2 Block Diagram

### 10.2.1 Normal count TIMER block diagram

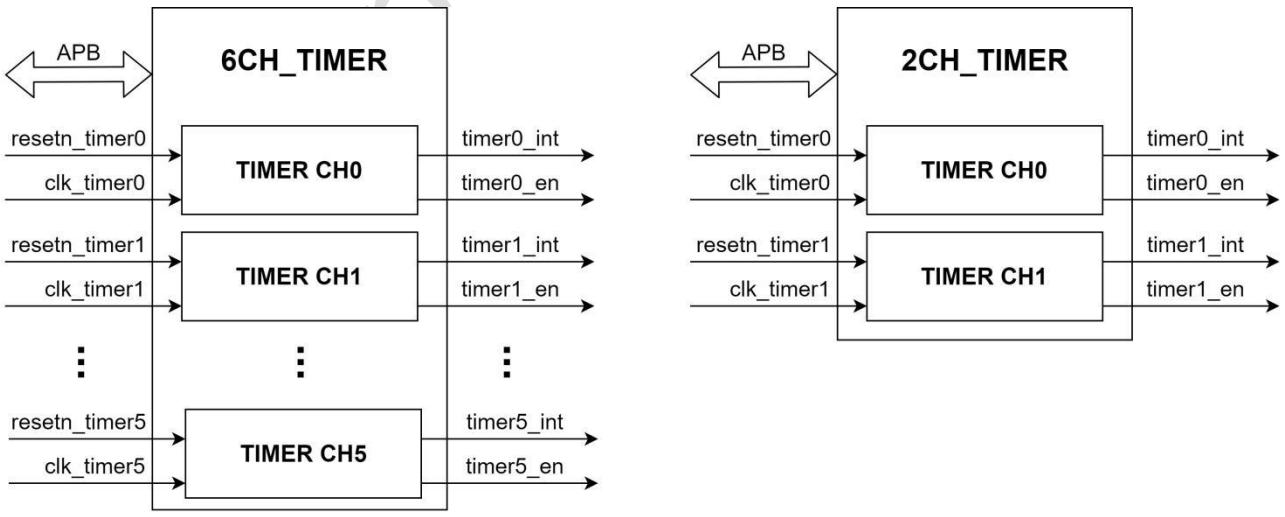



Fig. 10-1 Normal Timer Block Diagram

Fig. 10-1 show 6-channel TIMER and 2-channel TIMER. At 6CH_TIMER, the TIMER ch0~ch4 are the normal decrement count TIMER and ch5 is the normal increment count TIMER. At 2CH_TIMER, ch0 and ch1 are common normal increment count TIMER. APB is the read and write interface of timer register. reset_timern and clk_timern are reset and count clock for each channel timer. Timern_int and timern_en are interrupt and clock enable for each channel timer respectively. (timern is the signal corresponding to TIMER CHn)

Rockchip Confidential

### 10.2.2 HPTIMER block diagram

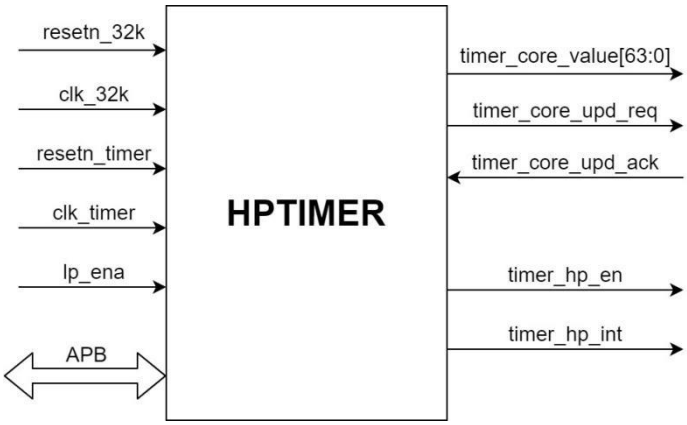



Fig. 10-2 HPTIMER Block Diagram

Fig. 10-2 shows the block diagram of HPTIMER.
HPTIMER has a set of APB interfaces for reading and writing registers.
lp_ena is the low power enable signal sent by PMU to HPTIMER, and it is also the indication signal of clk_timer frequency switching.
timer_core_value[63:0], timer_core_upd_req, timer_core_upd_ack is the interaction signal with core. timer_core_value[63:0] is the count update value, timer_core_upd_req is the update count request signal, timer_core_upd_ack is the update count response signal.
timer_hp_en is the enabling signal of clk_32k and clk_timer clocks. timer_hp_int is the interrupt output of HPTIMER.

## 10.3 Function Description

### 10.3.1 TIMER clock

The clock frequency of the counting clock source of NICTIMER and NDCTIMER is 24MHz. The clock source clock of clk_32k of HPTIMER is 32KHz, and the clock frequency of clk_timer clock source is switched between 24MHz and 32KHz.

### 10.3.2 Programming sequence

#### 10.3.2.1 NDCTIMER and NICTIMER programming sequence

1. Initialize the TIMER by the TIMER_TIMERn_CONTROLREG (0≤n≤5) register:
   1) Disable the timer by writing a "0" to the timer enable bit (bit 0). Accordingly, the timer_en output signal is de-asserted.
   2) Program the timer mode—free-running or user-defined—by writing a "0" or "1" respectively, to the timer mode bit (bit 1).
   3) Set the interrupt mask as either masked or not masked by writing a "0" or "1" respectively, to the timer interrupt mask bit (bit 2).
2. Load the timer count value into the TIMER_TIMERn_LOAD_COUNT1 (0≤n≤5) and TIMER_TIMERn_LOAD_COUNT0 (0≤n≤5) register.
3. Enable the TIMER by writing a "1" to bit 0 of TIMER_TIMERn_CONTROLREG (0≤n≤5).

Rockchip Confidential

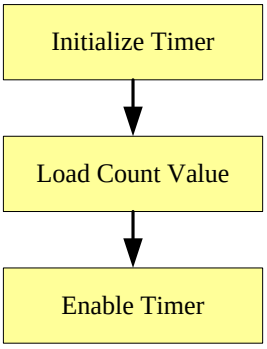



Fig. 10-3 Timer Usage Flow

### 10.3.2.2 HPTIMER programming sequence

- **Normal mode**

1. Initialize the HPTIMER by the TIMER_HP_CTRL register:
   (1) Disable the HPTIMER by writing a '0' to the timer enable bit (bit 0). Accordingly, the timer_hp_en output signal is de-asserted.
   (2) Program the timer mode, normal mode by writing a 0x0 to the timer mode bits (bit 1 to bit 2).
   (3) Program the count mode, free-running or user-defined by writing a '0' or '1' to the count mode bit (bit 3).
2. Load the HPTIMER count value into the TIMER_HP_LOAD_COUNT1 and TIMER_HP_LOAD_COUNT0 register.
3. Enable the HPTIMER by writing a '1' to bit 0 of TIMER_HP_CTRL.

If you want to do another count, repeat steps 1 to 3.

- **Hardware adjust mode**

1. Initialize the HPTIMER by the TIMER_HP_CTRL register:
   (1)Disable the HPTIMER by writing a '0' to the timer enable bit (bit 0). Accordingly, the timer_hp_en output signal is de-asserted.
   (2) Program the timer mode, normal mode by writing a 0x1 to the timer mode bits (bit 1 to bit 2).
   (3) Program the count mode, free-running or user-defined by writing a '0' or '1' to the count mode bit (bit 3).
2. Initialize the HPTIMER by the TIMER_HP_INTR_STATUS register. Write 0x7 to TIMER_HP_INTR_STATUS register to clear TIMER_HP_INTR_STATUS register.
3. Load the HPTIMER count value into the TIMER_HP_LOAD_COUNT1 and TIMER_HP_LOAD_COUNT0 register.
4. Configure the HPTIMER GCD register.
   (1) Divide the least common multiple of clk_timer and clk_32k clock cycle by clk_timer clock cycle and configure it in TIMER_HP_T24_GCD register.
   (2) Divide the least common multiple of clk_timer and clk_32k clock cycle by clk_32k clock cycle and configure it in TIMER_HP_T32_GCD register.
5. Enable the HPTIMER by writing a '1' to bit 0 of TIMER_HP_CTRL.
6. Read out the INTR_STATUS register until the ini_adj_done bit segment (bit 1) is '1', which means that the HPTIMER 32K count is initially adjusted. The low power mode can only be entered after the initial adjustment is completed.
7. The chip enters and exits the low power consumption mode at any time in between.
8. Read out the INTR_STATUS register until the sync_done bit segment (bit 2) is '1', indicating that the HPTIMER count is adjusted.
9. Write 0x7 to TIMER_HP_ INTR_STATUS register to clear TIMER_HP_INTR_STATUS register.

If the chip enters and exits the low power consumption mode again, repeat steps 7 to 9.

- **Software adjust mode**

1. Initialize the HPTIMER by the TIMER_HP_CTRL register:
   (1) Disable the HPTIMER by writing a '0' to the timer enable bit (bit 0). Accordingly, the timer_hp_en output signal is de-asserted.
   (2) Program the timer mode, normal mode by writing a 0x2 to the timer mode bits (bit 1 to bit 2).

Rockchip Confidencial

(3) Program the count mode, free-running or user-defined by writing a '0' or '1' to the count mode bit (bit 3).

2. Initialize the HPTIMER by the TIMER_HP_INTR_STATUS and BEGIN_END_VALID register. Write 0x7 to TIMER_HP_ INTR_STATUS register to clear TIMER_HP_INTR_STATUS register. write 0x3 to BEGIN_END_VALID register to clear BEGIN_END_VALID register.
3. Load the HPTIMER count value into the TIMER_HP_LOAD_COUNT1 and TIMER_HP_LOAD_ COUNT0 register.
4. Enable the HPTIMER by writing a '1' to bit 0 of TIMER_HP_CTRL.
5. The chip enters and exits the low power consumption mode at any time in between.
6. Read out BEGIN_END_VALID register until the value of it is 0x3, which indicates that the chip has entered and exited the low power consumption mode, then you can adjust the timer count value. Then write 0x3 to BEGIN_END_VALID register to clear the register.
7. The count value of HPTIMER compensation.
   (1) Read out TIMER_HP_T24_32BEGIN1, TIMER_ HP_T24_32BEGIN0, TIMER_HP_T32_ 24END1 and TIMER_HP_T32_24END0 register.
   (2) configure TIMER_HP_T24_DELAT_COUNT1 and TIMER_HP_T24_DELAT_COUNT0 registers to compensate for the count values according to the values of these registers read out above.
   (3) Write 0x1 to TIMER_HP_SYNC_REQ register to start compensation counting.
   (4) Read out the INTR_STATUS register until the sync_done bit segment (bit 2) is '1', indicating that the compensation count is completed.
8. Write 0x7 to TIMER_HP_ INTR_STATUS register to clear TIMER_HP_INTR_STATUS register.

If the chip enters and exits the low power consumption mode again, repeat steps 5 to 8.

### 10.3.3 Loading a timer count value

For the descending TIMER(that is, the value from which it counts down). The initial value for each TIMER is loaded into the TIMER using the load count register (TIMER_TIMERn_LOAD_ COUNT1 and TIMER_TIMERn_ LOAD_COUNT0). Two events can cause a TIMER to load the initial value from its load count register:

- TIMER is enabled after reset or disabled.
- TIMER counts down to 0, when TIMER is configured into free-running mode.

For the incremental TIMER(that is, the value from which it counts up). The initial value for each timer is zero. The count register will count up to the value loaded in the register TIMER_ TIMERn_LOAD_COUNT1 and TIMER_TIMERn_ LOAD_COUNT0. Two events can cause a TIMER to load zero:

- TIMER is enabled after reset or disabled.
- TIMER counts up to the value stored in TIMER_TIMERn_LOAD_COUNT1 and TIMER_ TIMERn_LOAD_COUNT0, when timer is configured into free-running mode.

### 10.3.4 Timer mode selection

- User-defined count mode – TIMER loads TIMER_TIMERn_LOAD_COUNT1 and TIMER_ TIMERn_LOAD_ COUNT0 registers (for descending TIMER) or zero (for incremental TIMER) as initial value. When the TIMER counts down to 0 (for descending TIMER) or counts up to the value in TIMER_TIMERn_LOAD_COUNT1 and TIMER_TIMERn_ LOAD_ COUNT0 (for incremental TIMER), it will not automatically reload the count register. User need to disable timer firstly and follow the programming sequence to make timer work again.
- Free-running mode – TIMER loads the TIMER_TIMERn_LOAD_COUNT1 and TIMER_ TIMERn_LOAD_COUNT0(for descending TIMER) or zero(for incremental TIMER) register as initial value. TIMER will automatically reload the count register, when timer counts down to 0(for descending TIMER) or counts up to the value in TIMER_TIMERn_LOAD_ COUNT1 and TIMER_TIMERn_LOAD_COUNT0 (for incremental TIMER).

Rockchip Confidential

# 10.4 Register Description

## 10.4.1 Registers Summary

### 10.4.1.1 Normal Count TIMER Register Summary

For 2-channel normal count TIMER, the base address of channel 1 is greater than that of channel 0 by 0x20. For 6-channel normal count TIMER, the base address of channel 1 is greater than that of channel 0 by 0x20, the base address of channel 2 is greater than that of channel 1 by 0x20, and so on. The revision register offset of 2-channel / 6-channel normal count TIMER is 0xf0.
If you want to know that each TIMER is 2-channel or 6-channel, please refer to the "TIMER attributes" section at the end of "Chapter TIMER".

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| TIMER_TIMERn_LOAD_COUNT0 | 0x0000 +n*0x20 | W | 0x00000000 | Timern Load Count Register 0 |
| TIMER_TIMERn_LOAD_COUNT1 | 0x0004 +n*0x20 | W | 0x00000000 | Timern Load Count Register 1.Higher 32 bits Value to be loaded into Timer n. This is the value from which counting commences |
| TIMER_TIMERn_CURRENT_VALUE0 | 0x0008 +n*0x20 | W | 0x00000000 | Timern Current Value Register 0 |
| TIMER_TIMERn_CURRENT_VALUE1 | 0x000c +n*0x20 | W | 0x00000000 | Timern Current Value Register 1.High 32 bits of Current Value of Timer n |
| TIMER_TIMERn_CONTROLREG | 0x0010 +n*0x20 | W | 0x00000000 | Timern Control Register |
| TIMER_TIMERn_INTSTATUS | 0x0018 +n*0x20 | W | 0x00000000 | Timern Interrupt Status Register |
| TIMER_2CH_REVISION | 0x00F0 | W | 0x15650302 | 2-channel TIMER version |
| TIMER_6CH_REVISION | 0x00F0 | W | 0x11972006 | 6-channel TIMER version |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

### 1.4.1.2 HPTIMER Register Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| TIMER_HP_REVISION | 0x0000 | W | 0x13D10201 | HPTIMER version |
| TIMER_HP_CTRL | 0x0004 | W | 0x00000000 | HPTIMER control |
| TIMER_HP_INTR_EN | 0x0008 | W | 0x00000000 | Interrupt musk |
| TIMER_HP_T24_GCD | 0x000C | W | 0x00000000 | Common multiple div 24M |
| TIMER_HP_T32_GCD | 0x0010 | W | 0x00000000 | Common multiple div 32K |
| TIMER_HP_LOAD_COUNT0 | 0x0014 | W | 0x00000000 | Low 32bits of load count value |
| TIMER_HP_LOAD_COUNT1 | 0x0018 | W | 0x00000000 | High 32bits of load count value |
| TIMER_HP_T24_DELAT_COUNT0 | 0x001C | W | 0x00000000 | Low 32bits of 24M clock delay time count value |
| TIMER_HP_T24_DELAT_COUNT1 | 0x0020 | W | 0x00000000 | High 32bits of 24M clock delay time count value |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| TIMER_HP_CURR_32K_VALUE0 | 0x0024 | W | 0x00000000 | Low 32bits of current cnt_32k value |
| TIMER_HP_CURR_32K_VALUE1 | 0x0028 | W | 0x00000000 | High 32bits of current cnt_32k value |
| TIMER_HP_CURR_TIMER_VALUE0 | 0x002C | W | 0x00000000 | Low 32bits of current timer_cnt value |
| TIMER_HP_CURR_TIMER_VALUE1 | 0x0030 | W | 0x00000000 | High 32bits of current timer_cnt value |
| TIMER_HP_T24_32BEGIN0 | 0x0034 | W | 0x00000000 | Low 32 bits of low power begin |
| TIMER_HP_T24_32BEGIN1 | 0x0038 | W | 0x00000000 | High 32 bits of low power begin |
| TIMER_HP_T32_24END0 | 0x003C | W | 0x00000000 | Low 32 bits of low power end |
| TIMER_HP_T32_24END1 | 0x0040 | W | 0x00000000 | High 32 bits of low power end |
| TIMER_HP_BEGIN_END_VALID | 0x0044 | W | 0x00000000 | Low power count value valid |
| TIMER_HP_SYNC_REQ | 0x0048 | W | 0x00000000 | Synchronize request |
| TIMER_HP_INTR_STATUS | 0x004C | W | 0x00000000 | Interrupt status |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

### **10.4.2** Detail Register Description

#### 10.4.2.1 Normal Count TIMER Detail Register Description

**TIMER_TIMERn_LOAD_COUNT0**

Address: Operational Base + offset (0x0000+n*0x20)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | load_count_0<br>Lower 32 bits Value to be loaded into Timer n. This is the value from which counting commences. |

**TIMER_TIMERn_LOAD_COUNT1**

Address: Operational Base + offset (0x0004+n*0x20)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | load_count_1<br>Higher 32 bits Value to be loaded into Timer n. This is the value from which counting commences. |

**TIMER_TIMERn_CURRENT_VALUE0**

Address: Operational Base + offset (0x0008+n*0x20)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | timern_current_value0<br>Lower 32 bits of Current Value of Timer n. |

**TIMER_TIMERn_CURRENT_VALUE1**

Address: Operational Base + offset (0x000c+n*0x20)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | timern_current_value1<br>Higher 32 bits of Current Value of Timer n. |

**TIMER_TIMERn_CONTROLREG**

Rockchip Confidential

Address: Operational Base + offset (0x0010+n*0x20)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x0 | Reserved |
| 2 | RW | 0x0 | timer_int_en<br>Timer interrupt enable<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | timer_mode<br>Timer mode<br>1'b0: Free-running mode<br>1'b1: User-defined count mode |
| 0 | RW | 0x0 | timer_en<br>Timer enable<br>1'b0: Disable<br>1'b1: Enable |

**TIMER_TIMERn_INTSTATUS**

Address: Operational Base + offset (0x0018+n*0x20)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x0 | Reserved |
| 0 | RO | 0x0 | timern_int<br>This register contains the interrupt status for timern. |

**TIMER_2CH_REVISION**

Address: Operational Base + offset (0x00F0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x1565 | svn_revision<br>SVN revision: 16'd5477. |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x1 | ch1_type<br>Channel 1 is a count up counter. |
| 8 | RW | 0x1 | ch0_type<br>Channel 0 is a count up counter. |
| 7:0 | RO | 0x02 | ip_function<br>IP function: 16'd2. |

**TIMER_6CH_REVISION**

Address: Operational Base + offset (0x00F0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x1197 | svn_revision<br>SVN revision: 16'd4503. |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x1 | ch5_type<br>Channel 5 is a count up counter. |
| 12 | RW | 0x0 | ch4_type<br>Channel 4 is a count down counter. |
| 11 | RW | 0x0 | ch3_type<br>Channel 3 is a count down counter. |
| 10 | RW | 0x0 | ch2_type<br>Channel 2 is a count down counter. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RW | 0x0 | ch1_type<br>Channel 1 is a count down counter. |
| 8 | RW | 0x0 | ch0_type<br>Channel 0 is a count down counter. |
| 7:0 | RW | 0x06 | ip_function<br>IP function: 16'd6. |

### 10.4.2.2 HPTIMER Detail Register Description

**TIMER_HP_REVISION**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x13d1 | svn_revision<br>SVN revision: 16'd5073. |
| 15:10 | RO | 0x00 | reserved |
| 9:8 | RW | 0x2 | ch_type<br>Channel 0 is a low power recovery self-correction count up counter. |
| 7:0 | RO | 0x01 | ip_function<br>IP function: 16'd1. |

**TIMER_HP_CTRL**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3 | RW | 0x0 | count_mode<br>Timer count mode<br>1'b0: Free-running mode<br>1'b1: User-defined count mode |
| 2:1 | RW | 0x0 | timer_mode<br>Select timer as which timer<br>2'b00: Normal timer<br>2'b01: Adjust timer with hardware adjust<br>2'b10: Adjust timer with software adjust |
| 0 | RW | 0x0 | timer_en<br>Timer enable<br>1'b0: Disable<br>1'b1: Enable |

**TIMER_HP_INTR_EN**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2 | RW | 0x0 | sync_done_intr_en<br>Synchronization done interrupt enable<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | ini_adj_done_intr_en<br>Initial adjust done interrupt enable<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | count_reach_intr_en<br>Timer count reach load_count interrupt enable<br>1'b0: Disable<br>1'b1: Enable |

Rockchip Confidential

**TIMER_HP_T24_GCD**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | t24_gcd<br>The least common multiple of 24M and 32K clock cycles divided by 24M clock cycles. |

**TIMER_HP_T32_GCD**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | t32_gcd<br>The least common multiple of 24M and 32K clock cycles divided by 32K clock cycles. |

**TIMER_HP_LOAD_COUNT0**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | load_count0<br>Low 32bits of load count value. |

**TIMER_HP_LOAD_COUNT1**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | load_count1<br>High 32bits of load count value. |

**TIMER_HP_T24_DELAT_COUNT0**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | t24_delay_time_count0<br>Low 32bits of 24M clock delay time count value. |

**TIMER_HP_T24_DELAT_COUNT1**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | t24_delay_time_count1<br>High 32bits of 24M clock delay time count value. |

**TIMER_HP_CURR_32K_VALUE0**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | current_32k_value0<br>Low 32bits of current cnt_32k value. |

**TIMER_HP_CURR_32K_VALUE1**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | current_32k_value1<br>High 32bits of current cnt_32k value. |

**TIMER_HP_CURR_TIMER_VALUE0**

Address: Operational Base + offset (0x002C)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | current_value0<br>Low 32bits of current timer_cnt value. |

**TIMER_HP_CURR_TIMER_VALUE1**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | current_value1<br>High 32bits of current timer_cnt value. |

**TIMER_HP_T24_32BEGIN0**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | t24_32begin0<br>24M switches to 32K clock, with a low 32 bits of timer_cnt value. |

**TIMER_HP_T24_32BEGIN1**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | t24_32begin1<br>24M switches to 32K clock, with a high 32 bits of timer_cnt value. |

**TIMER_HP_T32_24END0**

Address: Operational Base + offset (0x003C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | t32_24end0<br>32K switches to 24M clock, with a low 32 bits of timer_cnt value. |

**TIMER_HP_T32_24END1**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | t32_24end1<br>32K switches to 24M clock, with a high 32 bits of timer_cnt value. |

**TIMER_HP_BEGIN_END_VALID**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | W1C | 0x0 | t32_24end_valid<br>T32_24END value valid<br>1'b0: Invalid<br>1'b1: Valid |
| 0 | W1C | 0x0 | t24_32begin_valid<br>T24_32BEGIN value valid<br>1'b0: Invalid<br>1'b1: Valid |

**TIMER_HP_SYNC_REQ**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | R/WSC | 0x0 | sync_request<br>Timer_cnt synchronize request. |

**TIMER_HP_INTR_STATUS**

Rockchip Confidential

Address: Operational Base + offset (0x004C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2 | W1C | 0x0 | sync_done<br>Timer_cnt synchronization done. |
| 1 | W1C | 0x0 | ini_adj_done<br>Cnt_32k initial adjust done. |
| 0 | W1C | 0x0 | count_reach<br>Normal counter: timer_cnt reach load_count value. |

## 10.5 Application Notes

### 10.5.1 Clock and Enable

In the chip, the timer_clk is from 24MHz XIN_OSC, asynchronous to the pclk. When user disables the timer enables bit (bit 0 of TIMERn_CONTROLREG (0≤n≤5)), the timer en output signal is de-asserted, and timer_clk will stop. When user enables the timer, the timer_en signal is asserted and timer_clk will start running.
The application is only allowed to re-config registers when timer_en is low.

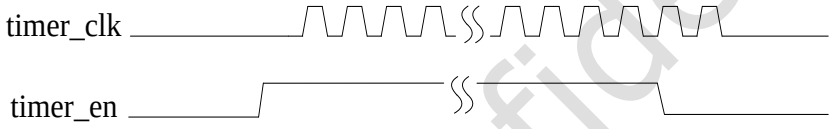



Fig. 10-4 Timing between timer_en and timer_clk

Please refer to function description section for the timer usage flow.

### 10.5.2 HPTIMER application notes

- Initial adjustment, synchronous counting adjustment time is about 2ms.
- When HPTIMER is used as software / hardware adjustment count, the count reaches the TIMER_HP_LOAD_COUNT value, the interrupt status bit will be set, but the count will not stop and continue to count.
- The timer_en of the CTRL register will output as a reference signal for timer clock gating. When timer_en is '0', it will gate the 24M and 32K clocks of the input timer. The application is only allowed to re-config registers when timer_en is low.

### 10.5.3 TIMER attributes

Table 10-1 shows the TIMER name corresponding to each TIMER, the total number of channels and their PD. It also shows the base address of each TIMER, in which the difference of TIMER address offset between adjacent channels in each TIMER is 0x20.

Table 10-1 TIMER attribute

| TIMER Name | CH NUM | PD | Base Address |
|---|---|---|---|
| TIMER_PMU | 2 | pd_pmu1 | 0xfd8f0000 |
| TIMER_NPU | 2 | pd_npu | 0xfdb00000 |
| TIMER_DDR | 2 | pd_center | 0xfe118000 |
| TIMER_S_0 | 6 | pd_secure | 0xfe3d0000 |
| TIMER_S_1 | 6 | pd_bus | 0xfed30000 |
| TIMER_NS_0 | 6 | pd_bus | 0xfeae0000 |
| TIMER_NS_1 | 6 | pd_bus | 0xfeae8000 |
| HP_TIMER | 1 | pd_pmu0 | 0xfd8c8000 |

Rockchip Confidential

# Chapter 11 GIC600

## 11.1 Overview

The GIC600 is a generic interrupt controller that handles interrupts from peripherals to the cores and between cores.
The GIC600 supports the GICv3 architecture, refer to the *Arm® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*.
The version of GIC600 is r1p6-00rel0. The configuration of GIC600 is shown below:

Table 11-1 GIC600 Configuration

| Configuration item | Value |
|---|---|
| num_clusters | 1 |
| cpus_per_clsuter_0 | 8 |
| num_spis | 480 |
| disable_security | false |
| lpi_support | true |
| monolithic | 0 |
| ppi_count | 1 |
| its_count | 2 |
| bypass_port | 1 |
| lpi_ram_depth | 128 |
| did_width | 16 |
| vid_width | 16 |
| col_width | 4 |
| axis_rid_width(GICD) | 10 |
| axis_wid_width(GICD) | 10 |
| axim_addr_width(GICD) | 35 |
| axim_data_width(GICD) | 64 |
| axis_addr_width(GICD) | 32 |
| axis_data_width(GICD) | 64 |
| axis_rid_width(ITS) | 8 |
| axis_wid_width(ITS) | 8 |
| axim_addr_width(ITS) | 35 |
| axim_data_width(ITS) | 128 |
| axis_addr_width(ITS) | 35 |
| axis_data_width(ITS) | 128 |

The GIC600 in RK3588 supports following feature:
- Support 1 cluster
- Support cluster 0 with 8 CPUs
- Support 0-32GB address space access by ITS and GICD
- According to the design of SOC, only support Non-shareable attribute of accesses to the LPI tables
- The following interrupt types:
  - Locality-specific Peripheral Interrupts (LPIs). These interrupts are generated by a peripheral writing to a memory-mapped register in the ITS
  - 480 Shared Peripheral Interrupts (SPIs)
  - 12 Private Peripheral Interrupts (PPIs), that are independent for each core and can be programmed to support either edge-triggered or level-sensitive interrupts
  - 16 SGIs, that are generated either by using software to write to GICD_SGIR or through the GIC CPU interface of a core
- Interrupt Translation Service (ITS). This provides device isolation and ID translation for message-based interrupts, which allows virtual machines to program devices directly
- Memory-mapped access to all registers
- Interrupt masking and prioritization
- Programmable interrupt routing that is based on affinity

Rockchip Confidential

- Three different interrupt groups, which allow interrupts to target different Exception levels:
  - Group 0
  - Non-secure Group 1
  - Secure Group 1
- A global Disable Security (DS) bit. This allows support for systems with and without security
- 32 priority values, five bits for each interrupt

## 11.2 Block Diagram

The GIC600 in the RK3588 is connected with CPU cluster through AXI Stream bus. As we can see, ITS is a separate component outside of the Distributor(GICD), since the monolithic configuration is 0. What's more, the GIC Domain and ITS Domain are placed in different power domain which are pd_bus and pd_php power domain respectively. As shown below:

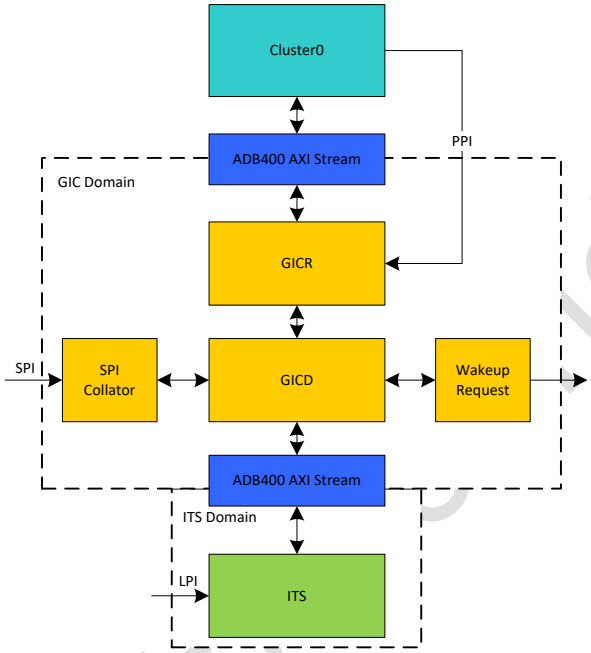



Fig. 11-1 Block Diagram

## 11.3 Function Description

Please refer to the document ARM_GIC-600_r1p6-00rel0_Technical_Reference_Manual.pdf for the detail function description. When we use Q-Channel for clock gating the GIC600 Distributor, remember to configure the bit[1] of SYS_GRF_GIC_CON0 to 1'b0.

Rockchip Confidential

# Chapter 12 DMA Controller (DMAC)

## 12.1 Overview

This device supports 3 Direct Memory Access (DMA) Controller. DMAC0/1/2 support transfers between memory and memory, peripheral and memory. DMAC0/1/2 is under Non-secure state after reset, and the Secure state can be changed by configurable SGRF module.
DMAC supports the following features:

- DMAC0 Supports 24 peripheral requests
- DMAC1 Supports 23 peripheral requests
- DMAC2 Supports 21 peripheral requests
- Up to 64 bits data size
- 8 channel at the same time
- Up to burst 16
- 16 interrupts output and 1 abort output
- Supports 128 MFIFO depth

Following table shows the DMAC request mapping scheme.

Table 12-1 DMAC Request Mapping Table

| DMAC0 | | |
|---|---|---|
| **Req number** | **Source** | **Polarity** |
| 0 | I2S0_8CH_TX | High level |
| 1 | I2S0_8CH_RX | High level |
| 2 | I2S1_8CH_TX | High level |
| 3 | I2S1_8CH_RX | High level |
| 4 | PDM0 | High level |
| 5 | SPDIF0 | High level |
| 6 | UART0_TX | High level |
| 7 | UART0_RX | High level |
| 8 | UART1_TX | High level |
| 9 | UART1_RX | High level |
| 10 | UART2_TX | High level |
| 11 | UART2_RX | High level |
| 12 | UART3_TX | High level |
| 13 | UART3_RX | High level |
| 14 | SPI0_TX | High level |
| 15 | SPI0_RX | High level |
| 16 | SPI1_TX | High level |
| 17 | SPI1_RX | High level |
| 18 | PWM_PMU | High level |
| 19 | CAN0_TX | High level |
| 20 | CAN0_RX | High level |
| 21 | SPDIF_RX0 | High level |
| 22 | SPDIF_RX1 | High level |
| 23 | SPDIF_RX2 | High level |
| **DMAC1** | | |
| **Req number** | **Source** | **Polarity** |
| 0 | I2S2_2CH_TX | High level |
| 1 | I2S2_2CH_RX | High level |
| 2 | I2S3_2CH_TX | High level |
| 3 | I2S3_2CH_RX | High level |
| 4 | PDM1 | High level |
| 5 | SPDIF1 | High level |
| 6 | SPDIF2 | High level |
| 7 | SPDIF3 | High level |
| 8 | SPDIF4 | High level |

Rockchip Confidential

| | | |
|---|---|---|
| 9 | UART4_TX | High level |
| 10 | UART4_RX | High level |
| 11 | UART5_TX | High level |
| 12 | UART5_RX | High level |
| 13 | UART6_TX | High level |
| 14 | UART6_RX | High level |
| 15 | SPI2_TX | High level |
| 16 | SPI2_RX | High level |
| 17 | SPI3_TX | High level |
| 18 | SPI3_RX | High level |
| 19 | PWM1 | High level |
| 20 | CAN1_TX | High level |
| 21 | CAN1_RX | High level |
| 22 | SPDIF5 | High level |
| **DMAC2** | | |
| **Req number** | **Source** | **Polarity** |
| 0 | I2S4_8CH_TX | High level |
| 2 | I2S5_8CH_TX | High level |
| 4 | I2S6_8CH_TX | High level |
| 7 | UART7_TX | High level |
| 8 | UART7_RX | High level |
| 9 | UART8_TX | High level |
| 10 | UART8_RX | High level |
| 11 | UART9_TX | High level |
| 12 | UART9_RX | High level |
| 13 | SPI4_TX | High level |
| 14 | SPI4_RX | High level |
| 15 | PWM2 | High level |
| 16 | PWM3 | High level |
| 17 | CAN2_TX | High level |
| 18 | CAN2_RX | High level |
| 19 | SDMMC_BUFFER | High level |
| 21 | I2S7_8CH_RX | High level |
| 22 | I2S8_8CH_TX | High level |
| 23 | I2S9_8CH_RX | High level |
| 24 | I2S10_8CH_RX | High level |

DMAC supports incrementing-address burst and fixed-address burst. But in the case of access to SPI and UART at byte or half word size, DMAC only supports fixed-address burst and the address must be aligned to word.

## 12.2 Block Diagram

Following figure shows the block diagram of DMAC.

Rockchip Confidential

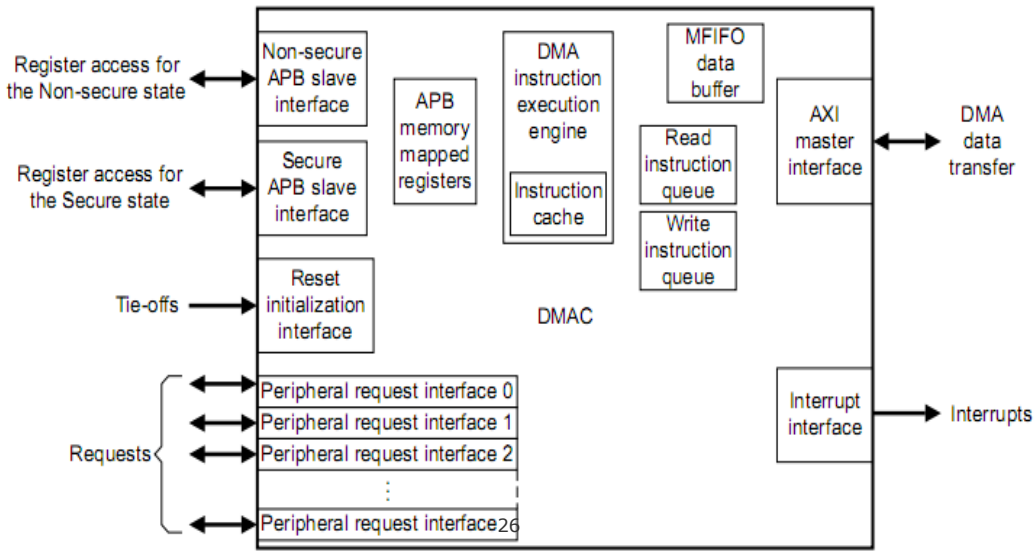



Fig. 12-1 Block Diagram of DMAC

As the DMAC supports TrustZone technology, so dual APB interfaces enable the operation of the DMAC to be partitioned into the Secure state and Non-secure state. You can use the APB interfaces to access status registers and also directly execute instructions in the DMAC. The default interface after reset is Non-secure APB interface.

# 12.3 Function Description

## 12.3.1 Introduction

The DMAC contains an instruction processing block that enables it to process program code that controls a DMA transfer. The program code is stored in a region of system memory that the DMAC accesses using its AXI interface. The DMAC stores instructions temporarily in a cache. It supports 8 channels, each channel capable of supporting a single concurrent thread of DMA operation. In addition, a single DMA manager thread exists, and you can use it to initialize the DMA channel threads. The DMAC executes up to one instruction for each AXI clock cycle. To ensure that it regularly executes each active thread, it alternates by processing the DMA manager thread and then a DMA channel thread. It uses a round-robin process when selecting the next active DMA channel thread to execute.

The DMAC uses variable-length instructions that consist of one to six bytes. It provides a separate Program Counter (PC) register for each DMA channel. When a thread requests an instruction from an address, the cache performs a look-up. If a cache hit occurs, then the cache immediately provides the data. Otherwise, the thread is stalled while the DMAC uses the AXI interface to perform a cache line fill. If an instruction is greater than 4 bytes, or spans the end of a cache line, the DMAC performs multiple cache accesses to fetch the instruction.

When a cache line fill is in progress, the DMAC enables other threads to access the cache, but if another cache miss occurs, this stalls the pipeline until the first line fill is complete. When a DMA channel thread executes a load or store instruction, the DMAC adds the instruction to the relevant read or write queue. The DMAC uses these queues as an instruction storage buffer prior to it issuing the instructions on the AXI bus. The DMAC also contains a Multi First-In-First-Out (MFIFO) data buffer that it uses to store data that it reads, or writes, during a DMA transfer.

## 12.3.2 Operating states

Following figure shows the operating states for the DMA manager thread and DMA channel threads.

Rockchip Confidential

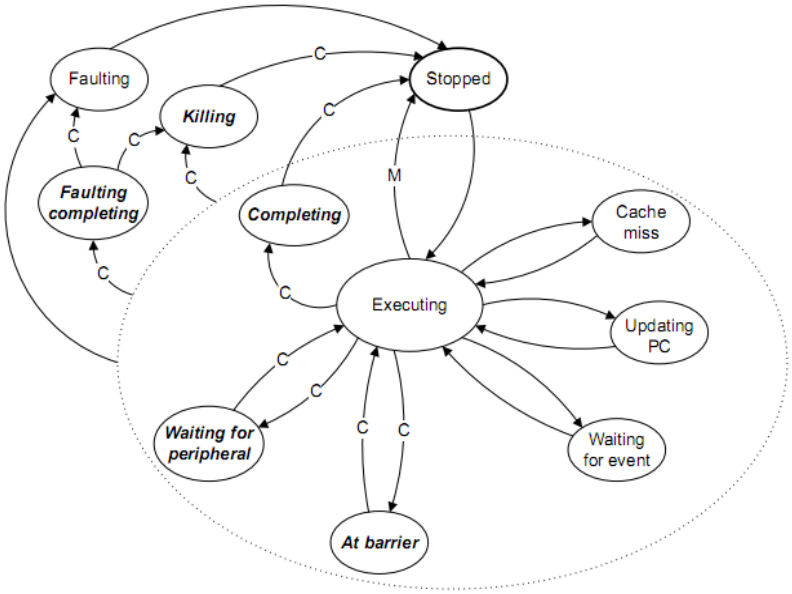



Fig. 12-2 DMAC Operation State

*Notes: arcs with no letter designator indicate state transitions for the DMA manager and DMA channel threads, otherwise use is restricted as follows:*
*C DMA channel threads only.*
*M DMA manager thread only.*

After the DMAC exits from reset, it sets all DMA channel threads to the stopped state, and DMA manager thread moves to the Stopped state.

## 12.4 Register Description

### 12.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

### 12.4.2 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| DMAC_DSR | 0x0000 | W | 0x00000000 | DMA Manager Status Register |
| DMAC_DPC | 0x0004 | W | 0x00000000 | DMA Program Counter Register |
| DMAC_INTEN | 0x0020 | W | 0x00000000 | Interrupt Enable Register |
| DMAC_EVENT_RIS | 0x0024 | W | 0x00000000 | Event-Interrupt Raw Status Register |
| DMAC_INTMIS | 0x0028 | W | 0x00000000 | Interrupt Status Register |
| DMAC_INTCLR | 0x002c | W | 0x00000000 | Interrupt Clear Register |
| DMAC_FSRD | 0x0030 | W | 0x00000000 | Fault Status DMA Manager Register |
| DMAC_FSRC | 0x0034 | W | 0x00000000 | Fault Status DMA Channel Register |
| DMAC_FTRD | 0x0038 | W | 0x00000000 | Fault Type DMA Manager Register |
| DMAC_FTR0 | 0x0040 | W | 0x00000000 | Fault Type DMA Channel 0 Register |
| DMAC_FTR1 | 0x0044 | W | 0x00000000 | Fault Type DMA Channel 1 Register |
| DMAC_FTR2 | 0x0048 | W | 0x00000000 | Fault Type DMA Channel 2 Register |
| DMAC_FTR3 | 0x004c | W | 0x00000000 | Fault Type DMA Channel 3 Register |
| DMAC_FTR4 | 0x0050 | W | 0x00000000 | Fault Type DMA Channel 4 Register |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| DMAC_FTR5 | 0x0054 | W | 0x00000000 | Fault Type DMA Channel 5 Register |
| DMAC_FTR6 | 0x0058 | W | 0x00000000 | Fault Type DMA Channel 6 Register |
| DMAC_FTR7 | 0x005c | W | 0x00000000 | Fault Type DMA Channel 7 Register |
| DMAC_CSR0 | 0x0100 | W | 0x00000000 | Channel 0 Status Register |
| DMAC_CPC0 | 0x0104 | W | 0x00000000 | Channel 0 Program Counter Register |
| DMAC_CSR1 | 0x0108 | W | 0x00000000 | Channel 1 Status Register |
| DMAC_CPC1 | 0x010c | W | 0x00000000 | Channel 1 Program Counter Register |
| DMAC_CSR2 | 0x0110 | W | 0x00000000 | Channel 2 Status Register |
| DMAC_CPC2 | 0x0114 | W | 0x00000000 | Channel 2 Program Counter Register |
| DMAC_CSR3 | 0x0118 | W | 0x00000000 | Channel 3 Status Register |
| DMAC_CPC3 | 0x011c | W | 0x00000000 | Channel 3 Program Counter Register |
| DMAC_CSR4 | 0x0120 | W | 0x00000000 | Channel 4 Status Register |
| DMAC_CPC4 | 0x0124 | W | 0x00000000 | Channel 4 Program Counter Register |
| DMAC_CSR5 | 0x0128 | W | 0x00000000 | Channel 5 Status Register |
| DMAC_CPC5 | 0x012c | W | 0x00000000 | Channel 5 Program Counter Register |
| DMAC_CSR6 | 0x0130 | W | 0x00000000 | Channel 6 Status Register |
| DMAC_CPC6 | 0x0134 | W | 0x00000000 | Channel 6 Program Counter Register |
| DMAC_CSR7 | 0x0138 | W | 0x00000000 | Channel 7 Status Register |
| DMAC_CPC7 | 0x013c | W | 0x00000000 | Channel 7 Program Counter Register |
| DMAC_SAR0 | 0x0400 | W | 0x00000000 | Channel 0 Source Address Register |
| DMAC_DAR0 | 0x0404 | W | 0x00000000 | Channel 0 Destination Address Register |
| DMAC_CCR0 | 0x0408 | W | 0x00000000 | Channel 0 Channel Control Register |
| DMAC_LC0_0 | 0x040c | W | 0x00000000 | Channel 0 Loop Counter 0 Register |
| DMAC_LC1_0 | 0x0410 | W | 0x00000000 | Channel 0 Loop Counter 1 Register |
| DMAC_SAR1 | 0x0420 | W | 0x00000000 | Channel 1 Source Address Register |
| DMAC_DAR1 | 0x0424 | W | 0x00000000 | Channel 1 Destination Address Register |
| DMAC_CCR1 | 0x0428 | W | 0x00000000 | Channel 1 Channel Control Register |
| DMAC_LC0_1 | 0x042c | W | 0x00000000 | Channel 1 Loop Counter 0 Register |
| DMAC_LC1_1 | 0x0430 | W | 0x00000000 | Channel 1 Loop Counter 1 Register |
| DMAC_SAR2 | 0x0440 | W | 0x00000000 | Channel 2 Source Address Register |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| DMAC_DAR2 | 0x0444 | W | 0x00000000 | Channel 2 Destination Address Register |
| DMAC_CCR2 | 0x0448 | W | 0x00000000 | Channel 2 Channel Control Register |
| DMAC_LC0_2 | 0x044c | W | 0x00000000 | Channel 2 Loop Counter 0 Register |
| DMAC_LC1_2 | 0x0450 | W | 0x00000000 | Channel 2 Loop Counter 1 Register |
| DMAC_SAR3 | 0x0460 | W | 0x00000000 | Channel 3 Source Address Register |
| DMAC_DAR3 | 0x0464 | W | 0x00000000 | Channel 3 Destination Address Register |
| DMAC_CCR3 | 0x0468 | W | 0x00000000 | Channel 3 Channel Control Register |
| DMAC_LC0_3 | 0x046c | W | 0x00000000 | Channel 3 Loop Counter 0 Register |
| DMAC_LC1_3 | 0x0470 | W | 0x00000000 | Channel 3 Loop Counter 1 Register |
| DMAC_SAR4 | 0x0480 | W | 0x00000000 | Channel 4 Address Register |
| DMAC_DAR4 | 0x0484 | W | 0x00000000 | Channel 4 Destination Address Register |
| DMAC_CCR4 | 0x0488 | W | 0x00000000 | Channel 4 Channel Control Register |
| DMAC_LC0_4 | 0x048c | W | 0x00000000 | Channel 4 Loop Counter 0 Register |
| DMAC_LC1_4 | 0x0490 | W | 0x00000000 | Channel 4 Loop Counter 1 Register |
| DMAC_SAR5 | 0x04a0 | W | 0x00000000 | Channel 5 Address Register |
| DMAC_DAR5 | 0x04a4 | W | 0x00000000 | Channel 5 Destination Address Register |
| DMAC_CCR5 | 0x04a8 | W | 0x00000000 | Channel 5 Channel Control Register |
| DMAC_LC0_5 | 0x04ac | W | 0x00000000 | Channel 5 Loop Counter 0 Register |
| DMAC_LC1_5 | 0x04b0 | W | 0x00000000 | Channel 5 Loop Counter 1 Register |
| DMAC_SAR6 | 0x04c0 | W | 0x00000000 | Channel 6 Source Address Register |
| DMAC_DAR6 | 0x04c4 | W | 0x00000000 | Channel 6 Destination Address Register |
| DMAC_CCR6 | 0x04c8 | W | 0x00000000 | Channel 6 Channel Control Register |
| DMAC_LC0_6 | 0x04cc | W | 0x00000000 | Channel 6 Loop Counter 0 Register |
| DMAC_LC1_6 | 0x04d0 | W | 0x00000000 | Channel 6 Loop Counter 1 Register |
| DMAC_SAR7 | 0x04e0 | W | 0x00000000 | Channel 7 Source Address Register |
| DMAC_DAR7 | 0x04e4 | W | 0x00000000 | Channel 7 Destination Address Register |
| DMAC_CCR7 | 0x04e8 | W | 0x00000000 | Channel 7 Channel Control Register |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| DMAC_LC0_7 | 0x04ec | W | 0x00000000 | Channel 7 Loop Counter 0 Register |
| DMAC_LC1_7 | 0x04f0 | W | 0x00000000 | Channel 7 Loop Counter 1 Register |
| DMAC_DBGSTATUS | 0x0d00 | W | 0x00000000 | Debug Status Register |
| DMAC_DBGCMD | 0x0d04 | W | 0x00000000 | Debug Command Register |
| DMAC_DBGINST0 | 0x0d08 | W | 0x00000000 | Debug Instruction-0 Register |
| DMAC_DBGINST1 | 0x0d0c | W | 0x00000000 | Debug Instruction-1 Register |
| DMAC_CR0 | 0x0e00 | W | 0x001f3075 | Configuration Register 0 |
| DMAC_CR1 | 0x0e04 | W | 0x000000b5 | Configuration Register 1 |
| DMAC_CR2 | 0x0e08 | W | 0x00000000 | Configuration Register 2 |
| DMAC_CR3 | 0x0e0c | W | 0x0000ffff | Configuration Register 3 |
| DMAC_CR4 | 0x0e10 | W | 0x000fffff | Configuration Register 4 |
| DMAC_CRDn | 0x0e14 | W | 0x07ff7f73 | Configuration Register |
| DMAC_WD | 0x0e80 | W | 0x00000000 | DMA Watchdog Register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

### 12.4.3 Detail Register Description

**DMAC_DSR**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x0 | reserved |
| 9 | RO | 0x0 | dns<br>1'b0: DMA manager operates in the Secure state<br>1'b1: DMA manager operates in the Non-secure state |
| 8:4 | RO | 0x00 | wakeup_event<br>5'h0: event[0]<br>5'h1: event[1]<br>5'h2: event[2]<br>…<br>5'h1f: event[31] |
| 3:0 | RO | 0x0 | dma_status<br>4'h0: Stopped<br>4'h1: Executing<br>4'h2: Cache miss<br>4'h3: Updating PC<br>4'h4: Waiting for event<br>4'hf: Faulting<br>Others: Reserved |

**DMAC_DPC**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | pc_mgr<br>Program counter for the DMA manager thread |

**DMAC_INTEN**

Address: Operational Base + offset (0x0020)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | event_irq_select<br>Bit [N]<br>1'b0: If the DMAC executes DMASEV for the event-interrupt resource N then the DMAC signals event N to all of the threads. Set bit [N] to 0 if your system design does not use irq[N] to signal an interrupt request.<br>1'b1: If the DMAC executes DMASEV for the event-interrupt resource N then the DMAC sets irq[N] HIGH. Set bit [N] to 1 if your system designer requires irq[N] to signal an interrupt request. |

**DMAC_EVENT_RIS**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | dmasev_active<br>Bit [N]<br>1'b0: Event N is inactive or irq[N] is LOW<br>1'b1: Event N is active or irq[N] is HIGH |

**DMAC_INTMIS**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | irq_status<br>Bit [N]<br>1'b0: Interrupt N is inactive and therefore irq[N] is LOW<br>1'b1: Interrupt N is active and therefore irq[N] is HIGH |

**DMAC_INTCLR**

Address: Operational Base + offset (0x002c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | WO | 0x00000000 | irq_clr<br>Bit [N]<br>1'b0: The status of irq[N] does not change<br>1'b1: The DMAC sets irq[N] LOW if the DMAC_INTEN Register programs the DMAC to signal an interrupt. Otherwise, the status of irq[N] does not change. |

**DMAC_FSRD**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x0 | reserved |
| 0 | RO | 0x0 | fs_mgr<br>1'b0: The DMA manager thread is not in the Faulting state<br>1'b1: The DMA manager thread is in the Faulting state |

**DMAC_FSRC**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0 | reserved |
| 7:0 | RO | 0x00 | fault_status<br>Bit [N]<br>1'b0: No fault is present on DMA channel N<br>1'b1: DMA channel N is in the Faulting or Faulting completing state |

Rockchip Confidencial

**DMAC_FTRD**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |
| 30 | RO | 0x0 | dbg_instr<br>Memory or from the debug interface.<br>1'b0: Instruction that generated an abort was read from system memory<br>1'b1: Instruction that generated an abort was read from the debug interface |
| 29:17 | RO | 0x0 | reserved |
| 16 | RO | 0x0 | instr_fetch_err<br>Performs an instruction fetch.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response |
| 15:6 | RO | 0x0 | reserved |
| 5 | RO | 0x0 | mgr_evnt_err<br>1'b0: DMA manager has appropriate security to execute DMAWFE or DMASEV<br>1'b1: DMA manager thread in the Non-secure state attempted to execute either:<br>a. DMAWFE to wait for a secure event<br>b. DMASEV to create a secure event or secure interrupt |
| 4 | RO | 0x0 | dmago_err<br>1'b0: DMA manager has appropriate security to execute DMAGO<br>1'b1: DMA manager thread in the Non-secure state attempted to execute DMAGO to create a DMA channel operating in the Secure state |
| 3:2 | RO | 0x0 | reserved |
| 1 | RO | 0x0 | operand_invalid<br>The configuration of the DMAC.<br>1'b0: Valid operand<br>1'b1: Invalid operand |
| 0 | RW | 0x0 | undef_instr<br>1'b0: Defined instruction<br>1'b1: Undefined instruction |

**DMAC_FTR0**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | lockup_err<br>1'b0: DMA channel has adequate resources<br>1'b1: DMA channel has locked-up because of insufficient resources<br>This fault is an imprecise abort. |
| 30 | RO | 0x0 | dbg_instr<br>Memory or from the debug interface.<br>1'b0: Instruction that generated an abort was read from system memory<br>1'b1: Instruction that generated an abort was read from the debug interface<br>This fault is an imprecise abort but the bit is only valid when a precise abort occurs. |
| 29:19 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 18 | RO | 0x0 | data_read_err<br>Thread performs a data read.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is an imprecise abort. |
| 17 | RO | 0x0 | data_write_err<br>Thread performs a data write.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is an imprecise abort. |
| 16 | RO | 0x0 | instr_fetch_err<br>Thread performs an instruction fetch.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is a precise abort. |
| 15:14 | RO | 0x0 | reserved |
| 13 | RO | 0x0 | st_data_unavailable<br>1'b0: MFIFO contains all the data to enable the DMAST to complete<br>1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete<br>This fault is a precise abort. |
| 12 | RO | 0x0 | mfifo_err<br>DMALD<br>1'b0: MFIFO contains sufficient space<br>1'b1: MFIFO is too small to hold the data that DMALD requires<br>DMAST<br>1'b0: MFIFO contains sufficient data<br>1'b1: MFIFO is too small to store the data to enable DMAST to complete<br>This fault is an imprecise abort. |
| 11:8 | RO | 0x0 | reserved |
| 7 | RO | 0x0 | ch_rdwr_err<br>To perform a secure read or secure write.<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write<br>This fault is a precise abort. |
| 6 | RO | 0x0 | ch_periph_err<br>DMASTP, or DMAFLUSHP with inappropriate security permissions.<br>1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: a DMA channel thread in the Non-secure state attempted to execute either:<br>a. DMAWFP to wait for a secure peripheral<br>b. DMALDP or DMASTP to notify a secure peripheral<br>c. DMAFLUSHP to flush a secure peripheral<br>This fault is a precise abort. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RO | 0x0 | ch_event_err<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to execute either:<br>a. DMAWFE to wait for a secure event<br>b. DMASEV to create a secure event or secure interrupt<br>This fault is a precise abort. |
| 4:2 | RO | 0x0 | reserved |
| 1 | RO | 0x0 | operand_invalid<br>Valid for the configuration of the DMAC.<br>1'b0: Valid operand<br>1'b1: Invalid operand<br>This fault is a precise abort. |
| 0 | RO | 0x0 | undef_instr<br>1'b0: Defined instruction<br>1'b1: Undefined instruction<br>This fault is a precise abort. |

**DMAC_FTR1**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | lockup_err<br>1'b0: DMA channel has adequate resources<br>1'b1: DMA channel has locked-up because of insufficient resources<br>This fault is an imprecise abort. |
| 30 | RO | 0x0 | dbg_instr<br>Memory or from the debug interface.<br>1'b0: Instruction that generated an abort was read from system memory<br>1'b1: Instruction that generated an abort was read from the debug interface<br>This fault is an imprecise abort but the bit is only valid when a precise abort occurs. |
| 29:19 | RO | 0x0 | reserved |
| 18 | RO | 0x0 | data_read_err<br>Thread performs a data read.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is an imprecise abort. |
| 17 | RO | 0x0 | data_write_err<br>Thread performs a data write.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is an imprecise abort. |
| 16 | RO | 0x0 | instr_fetch_err<br>Thread performs an instruction fetch.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is a precise abort. |
| 15:14 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RO | 0x0 | st_data_unavailable<br>1'b0: MFIFO contains all the data to enable the DMAST to complete<br>1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete<br>This fault is a precise abort. |
| 12 | RO | 0x0 | mfifo_err<br>DMALD<br>1'b0: MFIFO contains sufficient space<br>1'b1: MFIFO is too small to hold the data that DMALD requires<br>DMAST<br>1'b0: MFIFO contains sufficient data<br>1'b1: MFIFO is too small to store the data to enable DMAST to complete<br>This fault is an imprecise abort. |
| 11:8 | RO | 0x0 | reserved |
| 7 | RO | 0x0 | ch_rdwr_err<br>To perform a secure read or secure write.<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write<br>This fault is a precise abort. |
| 6 | RO | 0x0 | ch_periph_err<br>DMASTP, or DMAFLUSHP with inappropriate security permissions.<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to execute either:<br>a. DMAWFP to wait for a secure peripheral<br>b. DMALDP or DMASTP to notify a secure peripheral<br>c. DMAFLUSHP to flush a secure peripheral<br>This fault is a precise abort. |
| 5 | RO | 0x0 | ch_event_err<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to execute either:<br>a. DMAWFE to wait for a secure event<br>b. DMASEV to create a secure event or secure interrupt<br>This fault is a precise abort. |
| 4:2 | RO | 0x0 | reserved |
| 1 | RO | 0x0 | operand_invalid<br>Valid for the configuration of the DMAC.<br>1'b0: Valid operand<br>1'b1: Invalid operand<br>This fault is a precise abort. |
| 0 | RO | 0x0 | undef_instr<br>1'b0: Defined instruction<br>1'b1: Undefined instruction<br>This fault is a precise abort. |

**DMAC_FTR2**

Address: Operational Base + offset (0x0048)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | lockup_err<br>1'b0: DMA channel has adequate resources<br>1'b1: DMA channel has locked-up because of insufficient resources<br>This fault is an imprecise abort. |
| 30 | RO | 0x0 | dbg_instr<br>Memory or from the debug interface.<br>1'b0: Instruction that generated an abort was read from system memory<br>1'b1: Instruction that generated an abort was read from the debug interface<br>This fault is an imprecise abort but the bit is only valid when a precise abort occurs. |
| 29:19 | RO | 0x0 | reserved |
| 18 | RO | 0x0 | data_read_err<br>Thread performs a data read.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is an imprecise abort. |
| 17 | RO | 0x0 | data_write_err<br>Thread performs a data write.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is an imprecise abort. |
| 16 | RO | 0x0 | instr_fetch_err<br>Thread performs an instruction fetch.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is a precise abort. |
| 15:14 | RO | 0x0 | reserved |
| 13 | RO | 0x0 | st_data_unavailable<br>1'b0: MFIFO contains all the data to enable the DMAST to complete<br>1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete<br>This fault is a precise abort. |
| 12 | RO | 0x0 | mfifo_err<br>DMALD<br>1'b0: MFIFO contains sufficient space<br>1'b1: MFIFO is too small to hold the data that DMALD requires<br>DMAST<br>1'b0: MFIFO contains sufficient data<br>1'b1: MFIFO is too small to store the data to enable DMAST to complete<br>This fault is an imprecise abort. |
| 11:8 | RO | 0x0 | reserved |
| 7 | RO | 0x0 | ch_rdwr_err<br>To perform a secure read or secure write.<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write<br>This fault is a precise abort. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RO | 0x0 | ch_periph_err<br>DMASTP, or DMAFLUSHP with inappropriate security permissions.<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to execute either:<br>a. DMAWFP to wait for a secure peripheral<br>b. DMALDP or DMASTP to notify a secure peripheral<br>c. DMAFLUSHP to flush a secure peripheral<br>This fault is a precise abort. |
| 5 | RO | 0x0 | ch_event_err<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to execute either:<br>a. DMAWFE to wait for a secure event<br>b. DMASEV to create a secure event or secure interrupt<br>This fault is a precise abort. |
| 4:2 | RO | 0x0 | reserved |
| 1 | RO | 0x0 | operand_invalid<br>Valid for the configuration of the DMAC.<br>1'b0: Valid operand<br>1'b1: Invalid operand<br>This fault is a precise abort. |
| 0 | RO | 0x0 | undef_instr<br>1'b0: Defined instruction<br>1'b1: Undefined instruction<br>This fault is a precise abort. |

**DMAC_FTR3**

Address: Operational Base + offset (0x004c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | lockup_err<br>1'b0: DMA channel has adequate resources<br>1'b1: DMA channel has locked-up because of insufficient resources<br>This fault is an imprecise abort. |
| 30 | RO | 0x0 | dbg_instr<br>Memory or from the debug interface.<br>1'b0: Instruction that generated an abort was read from system memory<br>1'b1: Instruction that generated an abort was read from the debug interface<br>This fault is an imprecise abort but the bit is only valid when a precise abort occurs. |
| 29:19 | RO | 0x0 | reserved |
| 18 | RO | 0x0 | data_read_err<br>Thread performs a data read.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is an imprecise abort. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17 | RO | 0x0 | data_write_err<br>Thread performs a data write.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is an imprecise abort. |
| 16 | RO | 0x0 | instr_fetch_err<br>Thread performs an instruction fetch.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is a precise abort. |
| 15:14 | RO | 0x0 | reserved |
| 13 | RO | 0x0 | st_data_unavailable<br>1'b0: MFIFO contains all the data to enable the DMAST to complete<br>1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete<br>This fault is a precise abort. |
| 12 | RO | 0x0 | mfifo_err<br>DMALD<br>1'b0: MFIFO contains sufficient space<br>1'b1: MFIFO is too small to hold the data that DMALD requires<br>DMAST<br>1'b0: MFIFO contains sufficient data<br>1'b1: MFIFO is too small to store the data to enable DMAST to complete<br>This fault is an imprecise abort. |
| 11:8 | RO | 0x0 | reserved |
| 7 | RO | 0x0 | ch_rdwr_err<br>To perform a secure read or secure write.<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write<br>This fault is a precise abort. |
| 6 | RO | 0x0 | ch_periph_err<br>DMASTP, or DMAFLUSHP with inappropriate security permissions.<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to execute either:<br>a. DMAWFP to wait for a secure peripheral<br>b. DMALDP or DMASTP to notify a secure peripheral<br>c. DMAFLUSHP to flush a secure peripheral<br>This fault is a precise abort. |
| 5 | RO | 0x0 | ch_event_err<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to execute either:<br>a. DMAWFE to wait for a secure event<br>b. DMASEV to create a secure event or secure interrupt<br>This fault is a precise abort. |
| 4:2 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RO | 0x0 | operand_invalid<br>Valid for the configuration of the DMAC.<br>1'b0: Valid operand<br>1'b1: Invalid operand<br>This fault is a precise abort. |
| 0 | RO | 0x0 | undef_instr<br>1'b0: Defined instruction<br>1'b1: Undefined instruction<br>This fault is a precise abort. |

**DMAC_FTR4**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | lockup_err<br>1'b0: DMA channel has adequate resources<br>1'b1: DMA channel has locked-up because of insufficient resources<br>This fault is an imprecise abort. |
| 30 | RO | 0x0 | dbg_instr<br>Memory or from the debug interface.<br>1'b0: Instruction that generated an abort was read from system memory<br>1'b1: Instruction that generated an abort was read from the debug interface<br>This fault is an imprecise abort but the bit is only valid when a precise abort occurs. |
| 29:19 | RO | 0x0 | reserved |
| 18 | RO | 0x0 | data_read_err<br>Thread performs a data read.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is an imprecise abort. |
| 17 | RO | 0x0 | data_write_err<br>Thread performs a data write.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is an imprecise abort. |
| 16 | RO | 0x0 | instr_fetch_err<br>Thread performs an instruction fetch.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is a precise abort. |
| 15:14 | RO | 0x0 | reserved |
| 13 | RO | 0x0 | st_data_unavailable<br>1'b0: MFIFO contains all the data to enable the DMAST to complete<br>1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete<br>This fault is a precise abort. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RO | 0x0 | mfifo_err<br>DMALD<br>1'b0: MFIFO contains sufficient space<br>1'b1: MFIFO is too small to hold the data that DMALD requires<br>DMAST<br>1'b0: MFIFO contains sufficient data<br>1'b1: MFIFO is too small to store the data to enable DMAST to complete<br>This fault is an imprecise abort. |
| 11:8 | RO | 0x0 | reserved |
| 7 | RO | 0x0 | ch_rdwr_err<br>To perform a secure read or secure write.<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write<br>This fault is a precise abort. |
| 6 | RO | 0x0 | ch_periph_err<br>DMASTP, or DMAFLUSHP with inappropriate security permissions.<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to execute either:<br>a. DMAWFP to wait for a secure peripheral<br>b. DMALDP or DMASTP to notify a secure peripheral<br>c. DMAFLUSHP to flush a secure peripheral<br>This fault is a precise abort. |
| 5 | RO | 0x0 | ch_event_err<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to execute either:<br>a. DMAWFE to wait for a secure event<br>b. DMASEV to create a secure event or secure interrupt<br>This fault is a precise abort. |
| 4:2 | RO | 0x0 | reserved |
| 1 | RO | 0x0 | operand_invalid<br>Valid for the configuration of the DMAC.<br>1'b0: Valid operand<br>1'b1: Invalid operand<br>This fault is a precise abort. |
| 0 | RO | 0x0 | undef_instr<br>1'b0: Defined instruction<br>1'b1: Undefined instruction<br>This fault is a precise abort. |

**DMAC_FTR5**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | lockup_err<br>1'b0: DMA channel has adequate resources<br>1'b1: DMA channel has locked-up because of insufficient resources<br>This fault is an imprecise abort. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 30 | RO | 0x0 | dbg_instr<br>Memory or from the debug interface.<br>1'b0: Instruction that generated an abort was read from system memory<br>1'b1: Instruction that generated an abort was read from the debug interface<br>This fault is an imprecise abort but the bit is only valid when a precise abort occurs. |
| 29:19 | RO | 0x0 | reserved |
| 18 | RO | 0x0 | data_read_err<br>Thread performs a data read.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is an imprecise abort. |
| 17 | RO | 0x0 | data_write_err<br>Thread performs a data write.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is an imprecise abort. |
| 16 | RO | 0x0 | instr_fetch_err<br>Thread performs an instruction fetch.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is a precise abort. |
| 15:14 | RO | 0x0 | reserved |
| 13 | RO | 0x0 | st_data_unavailable<br>1'b0: MFIFO contains all the data to enable the DMAST to complete<br>1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete<br>This fault is a precise abort. |
| 12 | RO | 0x0 | mfifo_err<br>DMALD<br>1'b0: MFIFO contains sufficient space<br>1'b1: MFIFO is too small to hold the data that DMALD requires<br>DMAST<br>1'b0: MFIFO contains sufficient data<br>1'b1: MFIFO is too small to store the data to enable DMAST to complete<br>This fault is an imprecise abort. |
| 11:8 | RO | 0x0 | reserved |
| 7 | RO | 0x0 | ch_rdwr_err<br>To perform a secure read or secure write.<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write<br>This fault is a precise abort. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RO | 0x0 | ch_periph_err<br>DMASTP, or DMAFLUSHP with inappropriate security permissions.<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to execute either:<br>a. DMAWFP to wait for a secure peripheral<br>b. DMALDP or DMASTP to notify a secure peripheral<br>c. DMAFLUSHP to flush a secure peripheral<br>This fault is a precise abort. |
| 5 | RO | 0x0 | ch_event_err<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to execute either:<br>a. DMAWFE to wait for a secure event<br>b. DMASEV to create a secure event or secure interrupt<br>This fault is a precise abort. |
| 4:2 | RO | 0x0 | reserved |
| 1 | RO | 0x0 | operand_invalid<br>Valid for the configuration of the DMAC.<br>1'b0: Valid operand<br>1'b1: Invalid operand<br>This fault is a precise abort. |
| 0 | RO | 0x0 | undef_instr<br>1'b0: Defined instruction<br>1'b1: Undefined instruction<br>This fault is a precise abort. |

**DMAC_FTR6**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | lockup_err<br>1'b0: DMA channel has adequate resources<br>1'b1: DMA channel has locked-up because of insufficient resources<br>This fault is an imprecise abort. |
| 30 | RO | 0x0 | dbg_instr<br>Memory or from the debug interface.<br>1'b0: Instruction that generated an abort was read from system memory<br>1'b1: Instruction that generated an abort was read from the debug interface<br>This fault is an imprecise abort but the bit is only valid when a precise abort occurs. |
| 29:19 | RO | 0x0 | reserved |
| 18 | RO | 0x0 | data_read_err<br>Thread performs a data read.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is an imprecise abort. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17 | RO | 0x0 | data_write_err<br>Thread performs a data write.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is an imprecise abort. |
| 16 | RO | 0x0 | instr_fetch_err<br>Thread performs an instruction fetch.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is a precise abort. |
| 15:14 | RO | 0x0 | reserved |
| 13 | RO | 0x0 | st_data_unavailable<br>1'b0: MFIFO contains all the data to enable the DMAST to complete<br>1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete<br>This fault is a precise abort. |
| 12 | RO | 0x0 | mfifo_err<br>DMALD<br>1'b0: MFIFO contains sufficient space<br>1'b1: MFIFO is too small to hold the data that DMALD requires<br>DMAST<br>1'b0: MFIFO contains sufficient data<br>1'b1: MFIFO is too small to store the data to enable DMAST to complete<br>This fault is an imprecise abort. |
| 11:8 | RO | 0x0 | reserved |
| 7 | RO | 0x0 | ch_rdwr_err<br>To perform a secure read or secure write.<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write<br>This fault is a precise abort. |
| 6 | RO | 0x0 | ch_periph_err<br>DMASTP, or DMAFLUSHP with inappropriate security permissions.<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to execute either:<br>a. DMAWFP to wait for a secure peripheral<br>b. DMALDP or DMASTP to notify a secure peripheral<br>c. DMAFLUSHP to flush a secure peripheral<br>This fault is a precise abort. |
| 5 | RO | 0x0 | ch_event_err<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to execute either:<br>a. DMAWFE to wait for a secure event<br>b. DMASEV to create a secure event or secure interrupt<br>This fault is a precise abort. |
| 4:2 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RO | 0x0 | operand_invalid<br>Valid for the configuration of the DMAC.<br>1'b0: Valid operand<br>1'b1: Invalid operand<br>This fault is a precise abort. |
| 0 | RO | 0x0 | undef_instr<br>1'b0: Defined instruction<br>1'b1: Undefined instruction<br>This fault is a precise abort. |

**DMAC_FTR7**

Address: Operational Base + offset (0x005c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | lockup_err<br>1'b0: DMA channel has adequate resources<br>1'b1: DMA channel has locked-up because of insufficient resources<br>This fault is an imprecise abort. |
| 30 | RO | 0x0 | dbg_instr<br>Memory or from the debug interface.<br>1'b0: Instruction that generated an abort was read from system memory<br>1'b1: Instruction that generated an abort was read from the debug interface<br>This fault is an imprecise abort but the bit is only valid when a precise abort occurs. |
| 29:19 | RO | 0x0 | reserved |
| 18 | RO | 0x0 | data_read_err<br>Thread performs a data read.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is an imprecise abort. |
| 17 | RO | 0x0 | data_write_err<br>Thread performs a data write.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is an imprecise abort. |
| 16 | RO | 0x0 | instr_fetch_err<br>Thread performs an instruction fetch.<br>1'b0: OKAY response<br>1'b1: EXOKAY, SLVERR, or DECERR response<br>This fault is a precise abort. |
| 15:14 | RO | 0x0 | reserved |
| 13 | RO | 0x0 | st_data_unavailable<br>1'b0: MFIFO contains all the data to enable the DMAST to complete<br>1'b1: Previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete<br>This fault is a precise abort. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RO | 0x0 | mfifo_err<br>DMALD<br>1'b0: MFIFO contains sufficient space<br>1'b1: MFIFO is too small to hold the data that DMALD requires<br>DMAST<br>1'b0: MFIFO contains sufficient data<br>1'b1: MFIFO is too small to store the data to enable DMAST to complete<br>This fault is an imprecise abort. |
| 11:8 | RO | 0x0 | reserved |
| 7 | RO | 0x0 | ch_rdwr_err<br>To perform a secure read or secure write.<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to perform a secure read or secure write<br>This fault is a precise abort. |
| 6 | RO | 0x0 | ch_periph_err<br>DMASTP, or DMAFLUSHP with inappropriate security permissions.<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to execute either:<br>a. DMAWFP to wait for a secure peripheral<br>b. DMALDP or DMASTP to notify a secure peripheral<br>c. DMAFLUSHP to flush a secure peripheral<br>This fault is a precise abort. |
| 5 | RO | 0x0 | ch_event_err<br>1'b0: A DMA channel thread in the Non-secure state is not violating the security permissions<br>1'b1: A DMA channel thread in the Non-secure state attempted to execute either:<br>a. DMAWFE to wait for a secure event<br>b. DMASEV to create a secure event or secure interrupt<br>This fault is a precise abort. |
| 4:2 | RO | 0x0 | reserved |
| 1 | RO | 0x0 | operand_invalid<br>Valid for the configuration of the DMAC.<br>1'b0: Valid operand<br>1'b1: Invalid operand<br>This fault is a precise abort. |
| 0 | RO | 0x0 | undef_instr<br>1'b0: Defined instruction<br>1'b1: Undefined instruction<br>This fault is a precise abort. |

**DMAC_CSR0**

Address: Operational Base + offset (0x0100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x0 | reserved |
| 21 | RO | 0x0 | cns<br>1'b0: DMA channel operates in the Secure state<br>1'b1: DMA channel operates in the Non-secure state |
| 20:16 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RO | 0x0 | dmawfp_periph<br>1'b0: DMAWFP executed with the periph operand not set<br>1'b1: DMAWFP executed with the periph operand set |
| 14 | RO | 0x0 | dmawfp_b_ns<br>1'b0: DMAWFP executed with the single operand set<br>1'b1: DMAWFP executed with the burst operand set |
| 13:9 | RO | 0x0 | reserved |
| 8:4 | RO | 0x00 | wakeup_number<br>Indicate the event or peripheral number that the channel is waiting for.<br>5'h0: DMA channel is waiting for event, or peripheral, 0<br>5'h1: DMA channel is waiting for event, or peripheral, 1<br>5'h2: DMA channel is waiting for event, or peripheral, 2<br>…<br>5'h1f: DMA channel is waiting for event, or peripheral, 31 |
| 3:0 | RO | 0x0 | channel_status<br>Channel 0 status.<br>4'h0: Stopped<br>4'h1: Executing<br>4'h2: Cache miss<br>4'h3: Updating PC<br>4'h4: Waiting for event<br>4'h5: At barrier<br>4'h7: Waiting for peripheral<br>4'h8: Killing<br>4'h9: Completing<br>4'he: Faulting completing<br>4'hf: Faulting<br>Others: Reserved |

**DMAC_CPC0**

Address: Operational Base + offset (0x0104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | pc_chnl<br>Program counter for the DMA channel 0 thread |

**DMAC_CSR1**

Address: Operational Base + offset (0x0108)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x0 | reserved |
| 21 | RO | 0x0 | cns<br>1'b0: DMA channel operates in the Secure state<br>1'b1: DMA channel operates in the Non-secure state |
| 20:16 | RO | 0x0 | reserved |
| 15 | RO | 0x0 | dmawfp_periph<br>1'b0: DMAWFP executed with the periph operand not set<br>1'b1: DMAWFP executed with the periph operand set |
| 14 | RO | 0x0 | dmawfp_b_ns<br>1'b0: DMAWFP executed with the single operand set<br>1'b1: DMAWFP executed with the burst operand set |
| 13:9 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8:4 | RO | 0x00 | wakeup_number<br>Indicate the event or peripheral number that the channel is waiting for.<br>5'h0: DMA channel is waiting for event, or peripheral, 0<br>5'h1: DMA channel is waiting for event, or peripheral, 1<br>5'h2: DMA channel is waiting for event, or peripheral, 2<br>…<br>5'h1f: DMA channel is waiting for event, or peripheral, 31 |
| 3:0 | RO | 0x0 | channel_status<br>Channel 1 status.<br>4'h0: Stopped<br>4'h1: Executing<br>4'h2: Cache miss<br>4'h3: Updating PC<br>4'h4: Waiting for event<br>4'h5: At barrier<br>4'h7: Waiting for peripheral<br>4'h8: Killing<br>4'h9: Completing<br>4'he: Faulting completing<br>4'hf: Faulting<br>Others: Reserved |

**DMAC_CPC1**

Address: Operational Base + offset (0x010c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | pc_chnl<br>Program counter for the DMA channel 1 thread |

**DMAC_CSR2**

Address: Operational Base + offset (0x0110)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x0 | reserved |
| 21 | RO | 0x0 | cns<br>1'b0: DMA channel operates in the Secure state<br>1'b1: DMA channel operates in the Non-secure state |
| 20:16 | RO | 0x0 | reserved |
| 15 | RO | 0x0 | dmawfp_periph<br>1'b0: DMAWFP executed with the periph operand not set<br>1'b1: DMAWFP executed with the periph operand set |
| 14 | RO | 0x0 | dmawfp_b_ns<br>1'b0: DMAWFP executed with the single operand set<br>1'b1: DMAWFP executed with the burst operand set |
| 13:9 | RO | 0x0 | reserved |
| 8:4 | RO | 0x00 | wakeup_number<br>Indicate the event or peripheral number that the channel is waiting for.<br>5'h0: DMA channel is waiting for event, or peripheral, 0<br>5'h1: DMA channel is waiting for event, or peripheral, 1<br>5'h2: DMA channel is waiting for event, or peripheral, 2<br>…<br>5'h1f: DMA channel is waiting for event, or peripheral, 31 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RO | 0x0 | channel_status<br>Channel 2 status.<br>4'h0: Stopped<br>4'h1: Executing<br>4'h2: Cache miss<br>4'h3: Updating PC<br>4'h4: Waiting for event<br>4'h5: At barrier<br>4'h7: Waiting for peripheral<br>4'h8: Killing<br>4'h9: Completing<br>4'he: Faulting completing<br>4'hf: Faulting<br>Others: Reserved |

**DMAC_CPC2**

Address: Operational Base + offset (0x0114)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | pc_chnl<br>Program counter for the DMA channel 2 thread |

**DMAC_CSR3**

Address: Operational Base + offset (0x0118)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x0 | reserved |
| 21 | RO | 0x0 | cns<br>1'b0: DMA channel operates in the Secure state<br>1'b1: DMA channel operates in the Non-secure state |
| 20:16 | RO | 0x0 | reserved |
| 15 | RO | 0x0 | dmawfp_periph<br>1'b0: DMAWFP executed with the periph operand not set<br>1'b1: DMAWFP executed with the periph operand set |
| 14 | RO | 0x0 | dmawfp_b_ns<br>1'b0: DMAWFP executed with the single operand set<br>1'b1: DMAWFP executed with the burst operand set |
| 13:9 | RO | 0x0 | reserved |
| 8:4 | RO | 0x00 | wakeup_number<br>Indicate the event or peripheral number that the channel is waiting for.<br>5'h0: DMA channel is waiting for event, or peripheral, 0<br>5'h1: DMA channel is waiting for event, or peripheral, 1<br>5'h2: DMA channel is waiting for event, or peripheral, 2<br>…<br>5'h1f: DMA channel is waiting for event, or peripheral, 31 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RO | 0x0 | channel_status<br>Channel 3 status.<br>4'h0: Stopped<br>4'h1: Executing<br>4'h2: Cache miss<br>4'h3: Updating PC<br>4'h4: Waiting for event<br>4'h5: At barrier<br>4'h7: Waiting for peripheral<br>4'h8: Killing<br>4'h9: Completing<br>4'he: Faulting completing<br>4'hf: Faulting<br>Others: Reserved |

**DMAC_CPC3**

Address: Operational Base + offset (0x011c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | pc_chnl<br>Program counter for the DMA channel 3 thread |

**DMAC_CSR4**

Address: Operational Base + offset (0x0120)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x0 | reserved |
| 21 | RO | 0x0 | cns<br>1'b0: DMA channel operates in the Secure state<br>1'b1: DMA channel operates in the Non-secure state |
| 20:16 | RO | 0x0 | reserved |
| 15 | RO | 0x0 | dmawfp_periph<br>1'b0: DMAWFP executed with the periph operand not set<br>1'b1: DMAWFP executed with the periph operand set |
| 14 | RO | 0x0 | dmawfp_b_ns<br>1'b0: DMAWFP executed with the single operand set<br>1'b1: DMAWFP executed with the burst operand set |
| 13:9 | RO | 0x0 | reserved |
| 8:4 | RO | 0x00 | wakeup_number<br>Indicate the event or peripheral number that the channel is waiting for.<br>5'h0: DMA channel is waiting for event, or peripheral, 0<br>5'h1: DMA channel is waiting for event, or peripheral, 1<br>5'h2: DMA channel is waiting for event, or peripheral, 2<br>…<br>5'h1f: DMA channel is waiting for event, or peripheral, 31 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RO | 0x0 | channel_status<br>Channel 4 status.<br>4'h0: Stopped<br>4'h1: Executing<br>4'h2: Cache miss<br>4'h3: Updating PC<br>4'h4: Waiting for event<br>4'h5: At barrier<br>4'h7: Waiting for peripheral<br>4'h8: Killing<br>4'h9: Completing<br>4'he: Faulting completing<br>4'hf: Faulting<br>Others: Reserved |

**DMAC_CPC4**

Address: Operational Base + offset (0x0124)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | pc_chnl<br>Program counter for the DMA channel 4 thread |

**DMAC_CSR5**

Address: Operational Base + offset (0x0128)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x0 | reserved |
| 21 | RO | 0x0 | cns<br>1'b0: DMA channel operates in the Secure state<br>1'b1: DMA channel operates in the Non-secure state |
| 20:16 | RO | 0x0 | reserved |
| 15 | RO | 0x0 | dmawfp_periph<br>1'b0: DMAWFP executed with the periph operand not set<br>1'b1: DMAWFP executed with the periph operand set |
| 14 | RO | 0x0 | dmawfp_b_ns<br>1'b0: DMAWFP executed with the single operand set<br>1'b1: DMAWFP executed with the burst operand set |
| 13:9 | RO | 0x0 | reserved |
| 8:4 | RO | 0x00 | wakeup_number<br>Indicate the event or peripheral number that the channel is waiting for.<br>5'h0: DMA channel is waiting for event, or peripheral, 0<br>5'h1: DMA channel is waiting for event, or peripheral, 1<br>5'h2: DMA channel is waiting for event, or peripheral, 2<br>…<br>5'h1f: DMA channel is waiting for event, or peripheral, 31 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RO | 0x0 | channel_status<br>Channel 5 status.<br>4'h0: Stopped<br>4'h1: Executing<br>4'h2: Cache miss<br>4'h3: Updating PC<br>4'h4: Waiting for event<br>4'h5: At barrier<br>4'h7: Waiting for peripheral<br>4'h8: Killing<br>4'h9: Completing<br>4'he: Faulting completing<br>4'hf: Faulting<br>Others: Reserved |

**DMAC_CPC5**

Address: Operational Base + offset (0x012c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | pc_chnl<br>Program counter for the DMA channel 5 thread |

**DMAC_CSR6**

Address: Operational Base + offset (0x0130)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x0 | reserved |
| 21 | RO | 0x0 | cns<br>1'b0: DMA channel operates in the Secure state<br>1'b1: DMA channel operates in the Non-secure state |
| 20:16 | RO | 0x0 | reserved |
| 15 | RO | 0x0 | dmawfp_periph<br>1'b0: DMAWFP executed with the periph operand not set<br>1'b1: DMAWFP executed with the periph operand set |
| 14 | RO | 0x0 | dmawfp_b_ns<br>1'b0: DMAWFP executed with the single operand set<br>1'b1: DMAWFP executed with the burst operand set |
| 13:9 | RO | 0x0 | reserved |
| 8:4 | RO | 0x00 | wakeup_number<br>Indicate the event or peripheral number that the channel is waiting for.<br>5'h0: DMA channel is waiting for event, or peripheral, 0<br>5'h1: DMA channel is waiting for event, or peripheral, 1<br>5'h2: DMA channel is waiting for event, or peripheral, 2<br>…<br>5'h1f: DMA channel is waiting for event, or peripheral, 31 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RO | 0x0 | channel_status<br>Channel 6 status.<br>4'h0: Stopped<br>4'h1: Executing<br>4'h2: Cache miss<br>4'h3: Updating PC<br>4'h4: Waiting for event<br>4'h5: At barrier<br>4'h7: Waiting for peripheral<br>4'h8: Killing<br>4'h9: Completing<br>4'he: Faulting completing<br>4'hf: Faulting<br>Others: Reserved |

**DMAC_CPC6**

Address: Operational Base + offset (0x0134)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | pc_chnl<br>Program counter for the DMA channel 6 thread |

**DMAC_CSR7**

Address: Operational Base + offset (0x0138)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x0 | reserved |
| 21 | RO | 0x0 | cns<br>1'b0: DMA channel operates in the Secure state<br>1'b1: DMA channel operates in the Non-secure state |
| 20:16 | RO | 0x0 | reserved |
| 15 | RO | 0x0 | dmawfp_periph<br>1'b0: DMAWFP executed with the periph operand not set<br>1'b1: DMAWFP executed with the periph operand set |
| 14 | RO | 0x0 | dmawfp_b_ns<br>1'b0: DMAWFP executed with the single operand set<br>1'b1: DMAWFP executed with the burst operand set |
| 13:9 | RO | 0x0 | reserved |
| 8:4 | RO | 0x00 | wakeup_number<br>Indicate the event or peripheral number that the channel is waiting for.<br>5'h0: DMA channel is waiting for event, or peripheral, 0<br>5'h1: DMA channel is waiting for event, or peripheral, 1<br>5'h2: DMA channel is waiting for event, or peripheral, 2<br>…<br>5'h1f: DMA channel is waiting for event, or peripheral, 31 |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RO | 0x0 | channel_status<br>Channel 7 status.<br>4'h0: Stopped<br>4'h1: Executing<br>4'h2: Cache miss<br>4'h3: Updating PC<br>4'h4: Waiting for event<br>4'h5: At barrier<br>4'h7: Waiting for peripheral<br>4'h8: Killing<br>4'h9: Completing<br>4'he: Faulting completing<br>4'hf: Faulting<br>Others: Reserved |

**DMAC_CPC7**

Address: Operational Base + offset (0x013c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | pc_chnl<br>Program counter for the DMA channel 7 thread |

**DMAC_SAR0**

Address: Operational Base + offset (0x0400)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | src_addr<br>Address of the source data for DMA channel 0 |

**DMAC_DAR0**

Address: Operational Base + offset (0x0404)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | dst_addr<br>Address of the Destination data for DMA channel 0 |

**DMAC_CCR0**

Address: Operational Base + offset (0x0408)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27:25 | RO | 0x0 | dst_cache_ctrl<br>Bit [27]<br>1'b0: AWCACHE[3] is LOW<br>1'b1: AWCACHE[3] is HIGH<br>Bit [26]<br>1'b0: AWCACHE[1] is LOW<br>1'b1: AWCACHE[1] is HIGH<br>Bit [25]<br>1'b0: AWCACHE[0] is LOW<br>1'b1: AWCACHE[0] is HIGH |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 24:22 | RO | 0x0 | dst_prot_ctrl<br>Bit [24]<br>1'b0: AWPROT[2] is LOW<br>1'b1: AWPROT[2] is HIGH<br>Bit [23]<br>1'b0: AWPROT[1] is LOW<br>1'b1: AWPROT[1] is HIGH<br>Bit [22]<br>1'b0: AWPROT[0] is LOW<br>1'b1: AWPROT[0] is HIGH |
| 21:18 | RO | 0x0 | dst_burst_len<br>the destination data:<br>4'h0: 1 data transfer<br>4'h1: 2 data transfers<br>4'h2: 3 data transfers<br>…<br>4'hf: 16 data transfers<br>The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size. |
| 17:15 | RO | 0x0 | dst_burst_size<br>3'h0: Writes 1 byte per beat<br>3'h1: Writes 2 bytes per beat<br>3'h2: Writes 4 bytes per beat<br>3'h3: Writes 8 bytes per beat<br>3'h4: Writes 16 bytes per beat<br>Others: Reserved<br>The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size. |
| 14 | RO | 0x0 | dst_inc<br>1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW.<br>1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH. |
| 13:11 | RO | 0x0 | src_cache_ctrl<br>Bit [13]<br>1'b0: ARCACHE[2] is LOW<br>1'b1: ARCACHE[2] is HIGH<br>Bit [12]<br>1'b0: ARCACHE[1] is LOW<br>1'b1: ARCACHE[1] is HIGH<br>Bit [11]<br>1'b0: ARCACHE[0] is LOW<br>1'b1: ARCACHE[0] is HIGH |
| 10:8 | RO | 0x0 | src_prot_ctrl<br>Bit [10]<br>1'b0: ARPROT[2] is LOW<br>1'b1: ARPROT[2] is HIGH<br>Bit [9]<br>1'b0: ARPROT[1] is LOW<br>1'b1: ARPROT[1] is HIGH<br>Bit [8]<br>1'b0: ARPROT[0] is LOW<br>1'b1: ARPROT[0] is HIGH |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:4 | RO | 0x0 | src_burst_len<br>4'h0: 1 data transfer<br>4'h1: 2 data transfers<br>4'h2: 3 data transfers<br>…<br>4'hf: 16 data transfers<br>The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size. |
| 3:1 | RO | 0x0 | src_burst_size<br>3'h0: Reads 1 byte per beat<br>3'h1: Reads 2 bytes per beat<br>3'h2: Reads 4 bytes per beat<br>3'h3: Reads 8 bytes per beat<br>3'h4: Reads 16 bytes per beat<br>Others: Reserved<br>The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size. |
| 0 | RO | 0x0 | src_inc<br>1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW.<br>1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH. |

**DMAC_LC0_0**

Address: Operational Base + offset (0x040c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0 | reserved |
| 7:0 | RO | 0x00 | loop_counter_iterations<br>Loop counter 0 iterations |

**DMAC_LC1_0**

Address: Operational Base + offset (0x0410)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0 | reserved |
| 7:0 | RO | 0x00 | loop_counter_iterations<br>Loop counter 1 iterations |

**DMAC_SAR1**

Address: Operational Base + offset (0x0420)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | src_addr<br>Address of the source data for DMA channel 1 |

**DMAC_DAR1**

Address: Operational Base + offset (0x0424)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | dst_addr<br>Address of the Destination data for DMA channel 1 |

**DMAC_CCR1**

Address: Operational Base + offset (0x0428)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 27:25 | RO | 0x0 | dst_cache_ctrl<br>Bit [27]<br>1'b0: AWCACHE[3] is LOW<br>1'b1: AWCACHE[3] is HIGH<br>Bit [26]<br>1'b0: AWCACHE[1] is LOW<br>1'b1: AWCACHE[1] is HIGH<br>Bit [25]<br>1'b0: AWCACHE[0] is LOW<br>1'b1: AWCACHE[0] is HIGH |
| 24:22 | RO | 0x0 | dst_prot_ctrl<br>Bit [24]<br>1'b0: AWPROT[2] is LOW<br>1'b1: AWPROT[2] is HIGH<br>Bit [23]<br>1'b0: AWPROT[1] is LOW<br>1'b1: AWPROT[1] is HIGH<br>Bit [22]<br>1'b0: AWPROT[0] is LOW<br>1'b1: AWPROT[0] is HIGH |
| 21:18 | RO | 0x0 | dst_burst_len<br>the destination data:<br>4'h0: 1 data transfer<br>4'h1: 2 data transfers<br>4'h2: 3 data transfers<br>…<br>4'hf: 16 data transfers<br>The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size. |
| 17:15 | RO | 0x0 | dst_burst_size<br>3'h0: Writes 1 byte per beat<br>3'h1: Writes 2 bytes per beat<br>3'h2: Writes 4 bytes per beat<br>3'h3: Writes 8 bytes per beat<br>3'h4: Writes 16 bytes per beat<br>Others: Reserved<br>The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size. |
| 14 | RO | 0x0 | dst_inc<br>1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW.<br>1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH. |
| 13:11 | RO | 0x0 | src_cache_ctrl<br>Bit [13]<br>1'b0: ARCACHE[2] is LOW<br>1'b1: ARCACHE[2] is HIGH<br>Bit [12]<br>1'b0: ARCACHE[1] is LOW<br>1'b1: ARCACHE[1] is HIGH<br>Bit [11]<br>1'b0: ARCACHE[0] is LOW<br>1'b1: ARCACHE[0] is HIGH |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10:8 | RO | 0x0 | src_prot_ctrl<br>Bit [10]<br>1'b0: ARPROT[2] is LOW<br>1'b1: ARPROT[2] is HIGH<br>Bit [9]<br>1'b0: ARPROT[1] is LOW<br>1'b1: ARPROT[1] is HIGH<br>Bit [8]<br>1'b0: ARPROT[0] is LOW<br>1'b1: ARPROT[0] is HIGH |
| 7:4 | RO | 0x0 | src_burst_len<br>4'h0: 1 data transfer<br>4'h1: 2 data transfers<br>4'h2: 3 data transfers<br>…<br>4'hf: 16 data transfers<br>The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size. |
| 3:1 | RO | 0x0 | src_burst_size<br>3'h0: Reads 1 byte per beat<br>3'h1: Reads 2 bytes per beat<br>3'h2: Reads 4 bytes per beat<br>3'h3: Reads 8 bytes per beat<br>3'h4: Reads 16 bytes per beat<br>Others: Reserved<br>The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size. |
| 0 | RO | 0x0 | src_inc<br>1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW.<br>1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH. |

**DMAC_LC0_1**

Address: Operational Base + offset (0x042c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0 | reserved |
| 7:0 | RO | 0x00 | loop_counter_iterations<br>Loop counter 0 iterations |

**DMAC_LC1_1**

Address: Operational Base + offset (0x0430)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0 | reserved |
| 7:0 | RO | 0x00 | loop_counter_iterations<br>Loop counter 1 iterations |

**DMAC_SAR2**

Address: Operational Base + offset (0x0440)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | src_addr<br>Address of the source data for DMA channel 2 |

**DMAC_DAR2**

Rockchip Confidencial

Address: Operational Base + offset (0x0444)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | dst_addr<br>Address of the Destination data for DMA channel 2 |

**DMAC_CCR2**

Address: Operational Base + offset (0x0448)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27:25 | RO | 0x0 | dst_cache_ctrl<br>Bit [27]<br>1'b0: AWCACHE[3] is LOW<br>1'b1: AWCACHE[3] is HIGH<br>Bit [26]<br>1'b0: AWCACHE[1] is LOW<br>1'b1: AWCACHE[1] is HIGH<br>Bit [25]<br>1'b0: AWCACHE[0] is LOW<br>1'b1: AWCACHE[0] is HIGH |
| 24:22 | RO | 0x0 | dst_prot_ctrl<br>Bit [24]<br>1'b0: AWPROT[2] is LOW<br>1'b1: AWPROT[2] is HIGH<br>Bit [23]<br>1'b0: AWPROT[1] is LOW<br>1'b1: AWPROT[1] is HIGH<br>Bit [22]<br>1'b0: AWPROT[0] is LOW<br>1'b1: AWPROT[0] is HIGH |
| 21:18 | RO | 0x0 | dst_burst_len<br>the destination data:<br>4'h0: 1 data transfer<br>4'h1: 2 data transfers<br>4'h2: 3 data transfers<br>…<br>4'hf: 16 data transfers<br>The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size. |
| 17:15 | RO | 0x0 | dst_burst_size<br>3'h0: Writes 1 byte per beat<br>3'h1: Writes 2 bytes per beat<br>3'h2: Writes 4 bytes per beat<br>3'h3: Writes 8 bytes per beat<br>3'h4: Writes 16 bytes per beat<br>Others: Reserved<br>The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size. |
| 14 | RO | 0x0 | dst_inc<br>1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW.<br>1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:11 | RO | 0x0 | src_cache_ctrl<br>Bit [13]<br>1'b0: ARCACHE[2] is LOW<br>1'b1: ARCACHE[2] is HIGH<br>Bit [12]<br>1'b0: ARCACHE[1] is LOW<br>1'b1: ARCACHE[1] is HIGH<br>Bit [11]<br>1'b0: ARCACHE[0] is LOW<br>1'b1: ARCACHE[0] is HIGH |
| 10:8 | RO | 0x0 | src_prot_ctrl<br>Bit [10]<br>1'b0: ARPROT[2] is LOW<br>1'b1: ARPROT[2] is HIGH<br>Bit [9]<br>1'b0: ARPROT[1] is LOW<br>1'b1: ARPROT[1] is HIGH<br>Bit [8]<br>1'b0: ARPROT[0] is LOW<br>1'b1: ARPROT[0] is HIGH |
| 7:4 | RO | 0x0 | src_burst_len<br>4'h0: 1 data transfer<br>4'h1: 2 data transfers<br>4'h2: 3 data transfers<br>…<br>4'hf: 16 data transfers<br>The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size. |
| 3:1 | RO | 0x0 | src_burst_size<br>3'h0: Reads 1 byte per beat<br>3'h1: Reads 2 bytes per beat<br>3'h2: Reads 4 bytes per beat<br>3'h3: Reads 8 bytes per beat<br>3'h4: Reads 16 bytes per beat<br>Others: Reserved<br>The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size. |
| 0 | RO | 0x0 | src_inc<br>1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW.<br>1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH. |

**DMAC_LC0_2**

Address: Operational Base + offset (0x044c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0 | reserved |
| 7:0 | RO | 0x00 | loop_counter_iterations<br>Loop counter 0 iterations |

**DMAC_LC1_2**

Address: Operational Base + offset (0x0450)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0 | reserved |
| 7:0 | RO | 0x00 | loop_counter_iterations<br>Loop counter 1 iterations |

**DMAC_SAR3**

Address: Operational Base + offset (0x0460)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | src_addr<br>Address of the source data for DMA channel 3 |

**DMAC_DAR3**

Address: Operational Base + offset (0x0464)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | dst_addr<br>Address of the Destination data for DMA channel 3 |

**DMAC_CCR3**

Address: Operational Base + offset (0x0468)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27:25 | RO | 0x0 | dst_cache_ctrl<br>Bit [27]<br>1'b0: AWCACHE[3] is LOW<br>1'b1: AWCACHE[3] is HIGH<br>Bit [26]<br>1'b0: AWCACHE[1] is LOW<br>1'b1: AWCACHE[1] is HIGH<br>Bit [25]<br>1'b0: AWCACHE[0] is LOW<br>1'b1: AWCACHE[0] is HIGH |
| 24:22 | RO | 0x0 | dst_prot_ctrl<br>Bit [24]<br>1'b0: AWPROT[2] is LOW<br>1'b1: AWPROT[2] is HIGH<br>Bit [23]<br>1'b0: AWPROT[1] is LOW<br>1'b1: AWPROT[1] is HIGH<br>Bit [22]<br>1'b0: AWPROT[0] is LOW<br>1'b1: AWPROT[0] is HIGH |
| 21:18 | RO | 0x0 | dst_burst_len<br>the destination data:<br>4'h0: 1 data transfer<br>4'h1: 2 data transfers<br>4'h2: 3 data transfers<br>…<br>4'hf: 16 data transfers<br>The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17:15 | RO | 0x0 | dst_burst_size<br>3'h0: Writes 1 byte per beat<br>3'h1: Writes 2 bytes per beat<br>3'h2: Writes 4 bytes per beat<br>3'h3: Writes 8 bytes per beat<br>3'h4: Writes 16 bytes per beat<br>Others: Reserved<br>The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size. |
| 14 | RO | 0x0 | dst_inc<br>1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW.<br>1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH. |
| 13:11 | RO | 0x0 | src_cache_ctrl<br>Bit [13]<br>1'b0: ARCACHE[2] is LOW<br>1'b1: ARCACHE[2] is HIGH<br>Bit [12]<br>1'b0: ARCACHE[1] is LOW<br>1'b1: ARCACHE[1] is HIGH<br>Bit [11]<br>1'b0: ARCACHE[0] is LOW<br>1'b1: ARCACHE[0] is HIGH |
| 10:8 | RO | 0x0 | src_prot_ctrl<br>Bit [10]<br>1'b0: ARPROT[2] is LOW<br>1'b1: ARPROT[2] is HIGH<br>Bit [9]<br>1'b0: ARPROT[1] is LOW<br>1'b1: ARPROT[1] is HIGH<br>Bit [8]<br>1'b0: ARPROT[0] is LOW<br>1'b1: ARPROT[0] is HIGH |
| 7:4 | RO | 0x0 | src_burst_len<br>4'h0: 1 data transfer<br>4'h1: 2 data transfers<br>4'h2: 3 data transfers<br>…<br>4'hf: 16 data transfers<br>The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size. |
| 3:1 | RO | 0x0 | src_burst_size<br>3'h0: Reads 1 byte per beat<br>3'h1: Reads 2 bytes per beat<br>3'h2: Reads 4 bytes per beat<br>3'h3: Reads 8 bytes per beat<br>3'h4: Reads 16 bytes per beat<br>Others: Reserved<br>The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RO | 0x0 | src_inc<br>1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW.<br>1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH. |

**DMAC_LC0_3**

Address: Operational Base + offset (0x046c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0 | reserved |
| 7:0 | RO | 0x00 | loop_counter_iterations<br>Loop counter 0 iterations |

**DMAC_LC1_3**

Address: Operational Base + offset (0x0470)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0 | reserved |
| 7:0 | RO | 0x00 | loop_counter_iterations<br>Loop counter 1 iterations |

**DMAC_SAR4**

Address: Operational Base + offset (0x0480)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | src_addr<br>Address of the source data for DMA channel 4 |

**DMAC_DAR4**

Address: Operational Base + offset (0x0484)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | dst_addr<br>Address of the Destination data for DMA channel 4 |

**DMAC_CCR4**

Address: Operational Base + offset (0x0488)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27:25 | RO | 0x0 | dst_cache_ctrl<br>Bit [27]<br>1'b0: AWCACHE[3] is LOW<br>1'b1: AWCACHE[3] is HIGH<br>Bit [26]<br>1'b0: AWCACHE[1] is LOW<br>1'b1: AWCACHE[1] is HIGH<br>Bit [25]<br>1'b0: AWCACHE[0] is LOW<br>1'b1: AWCACHE[0] is HIGH |
| 24:22 | RO | 0x0 | dst_prot_ctrl<br>Bit [24]<br>1'b0: AWPROT[2] is LOW<br>1'b1: AWPROT[2] is HIGH<br>Bit [23]<br>1'b0: AWPROT[1] is LOW<br>1'b1: AWPROT[1] is HIGH<br>Bit [22]<br>1'b0: AWPROT[0] is LOW<br>1'b1: AWPROT[0] is HIGH |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 21:18 | RO | 0x0 | dst_burst_len<br>the destination data:<br>4'h0: 1 data transfer<br>4'h1: 2 data transfers<br>4'h2: 3 data transfers<br>…<br>4'hf: 16 data transfers<br>The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size. |
| 17:15 | RO | 0x0 | dst_burst_size<br>3'h0: Writes 1 byte per beat<br>3'h1: Writes 2 bytes per beat<br>3'h2: Writes 4 bytes per beat<br>3'h3: Writes 8 bytes per beat<br>3'h4: Writes 16 bytes per beat<br>Others: Reserved<br>The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size. |
| 14 | RO | 0x0 | dst_inc<br>1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW.<br>1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH. |
| 13:11 | RO | 0x0 | src_cache_ctrl<br>Bit [13]<br>1'b0: ARCACHE[2] is LOW<br>1'b1: ARCACHE[2] is HIGH<br>Bit [12]<br>1'b0: ARCACHE[1] is LOW<br>1'b1: ARCACHE[1] is HIGH<br>Bit [11]<br>1'b0: ARCACHE[0] is LOW<br>1'b1: ARCACHE[0] is HIGH |
| 10:8 | RO | 0x0 | src_prot_ctrl<br>Bit [10]<br>1'b0: ARPROT[2] is LOW<br>1'b1: ARPROT[2] is HIGH<br>Bit [9]<br>1'b0: ARPROT[1] is LOW<br>1'b1: ARPROT[1] is HIGH<br>Bit [8]<br>1'b0: ARPROT[0] is LOW<br>1'b1: ARPROT[0] is HIGH |
| 7:4 | RO | 0x0 | src_burst_len<br>4'h0: 1 data transfer<br>4'h1: 2 data transfers<br>4'h2: 3 data transfers<br>…<br>4'hf: 16 data transfers<br>The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:1 | RO | 0x0 | src_burst_size<br>3'h0: Reads 1 byte per beat<br>3'h1: Reads 2 bytes per beat<br>3'h2: Reads 4 bytes per beat<br>3'h3: Reads 8 bytes per beat<br>3'h4: Reads 16 bytes per beat<br>Others: Reserved<br>The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size. |
| 0 | RO | 0x0 | src_inc<br>1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW.<br>1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH. |

**DMAC_LC0_4**

Address: Operational Base + offset (0x048c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0 | reserved |
| 7:0 | RO | 0x00 | loop_counter_iterations<br>Loop counter 0 iterations |

**DMAC_LC1_4**

Address: Operational Base + offset (0x0490)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0 | reserved |
| 7:0 | RO | 0x00 | loop_counter_iterations<br>Loop counter 1 iterations |

**DMAC_SAR5**

Address: Operational Base + offset (0x04a0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | src_addr<br>Address of the source data for DMA channel 5 |

**DMAC_DAR5**

Address: Operational Base + offset (0x04a4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | dst_addr<br>Address of the Destination data for DMA channel 5 |

**DMAC_CCR5**

Address: Operational Base + offset (0x04a8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27:25 | RO | 0x0 | dst_cache_ctrl<br>Bit [27]<br>1'b0: AWCACHE[3] is LOW<br>1'b1: AWCACHE[3] is HIGH<br>Bit [26]<br>1'b0: AWCACHE[1] is LOW<br>1'b1: AWCACHE[1] is HIGH<br>Bit [25]<br>1'b0: AWCACHE[0] is LOW<br>1'b1: AWCACHE[0] is HIGH |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 24:22 | RO | 0x0 | dst_prot_ctrl<br>Bit [24]<br>1'b0: AWPROT[2] is LOW<br>1'b1: AWPROT[2] is HIGH<br>Bit [23]<br>1'b0: AWPROT[1] is LOW<br>1'b1: AWPROT[1] is HIGH<br>Bit [22]<br>1'b0: AWPROT[0] is LOW<br>1'b1: AWPROT[0] is HIGH |
| 21:18 | RO | 0x0 | dst_burst_len<br>the destination data:<br>4'h0: 1 data transfer<br>4'h1: 2 data transfers<br>4'h2: 3 data transfers<br>…<br>4'hf: 16 data transfers<br>The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size. |
| 17:15 | RO | 0x0 | dst_burst_size<br>3'h0: Writes 1 byte per beat<br>3'h1: Writes 2 bytes per beat<br>3'h2: Writes 4 bytes per beat<br>3'h3: Writes 8 bytes per beat<br>3'h4: Writes 16 bytes per beat<br>Others: Reserved<br>The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size. |
| 14 | RO | 0x0 | dst_inc<br>1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW.<br>1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH. |
| 13:11 | RO | 0x0 | src_cache_ctrl<br>Bit [13]<br>1'b0: ARCACHE[2] is LOW<br>1'b1: ARCACHE[2] is HIGH<br>Bit [12]<br>1'b0: ARCACHE[1] is LOW<br>1'b1: ARCACHE[1] is HIGH<br>Bit [11]<br>1'b0: ARCACHE[0] is LOW<br>1'b1: ARCACHE[0] is HIGH |
| 10:8 | RO | 0x0 | src_prot_ctrl<br>Bit [10]<br>1'b0: ARPROT[2] is LOW<br>1'b1: ARPROT[2] is HIGH<br>Bit [9]<br>1'b0: ARPROT[1] is LOW<br>1'b1: ARPROT[1] is HIGH<br>Bit [8]<br>1'b0: ARPROT[0] is LOW<br>1'b1: ARPROT[0] is HIGH |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:4 | RO | 0x0 | src_burst_len<br>4'h0: 1 data transfer<br>4'h1: 2 data transfers<br>4'h2: 3 data transfers<br>…<br>4'hf: 16 data transfers<br>The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size. |
| 3:1 | RO | 0x0 | src_burst_size<br>3'h0: Reads 1 byte per beat<br>3'h1: Reads 2 bytes per beat<br>3'h2: Reads 4 bytes per beat<br>3'h3: Reads 8 bytes per beat<br>3'h4: Reads 16 bytes per beat<br>Others: Reserved<br>The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size. |
| 0 | RO | 0x0 | src_inc<br>1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW.<br>1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH. |

**DMAC_LC0_5**

Address: Operational Base + offset (0x04ac)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0 | reserved |
| 7:0 | RO | 0x00 | loop_counter_iterations<br>Loop counter 0 iterations |

**DMAC_LC1_5**

Address: Operational Base + offset (0x04b0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0 | reserved |
| 7:0 | RO | 0x00 | loop_counter_iterations<br>Loop counter 1 iterations |

**DMAC_SAR6**

Address: Operational Base + offset (0x04c0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | src_addr<br>Address of the source data for DMA channel 6 |

**DMAC_DAR6**

Address: Operational Base + offset (0x04c4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | dst_addr<br>Address of the Destination data for DMA channel 6 |

**DMAC_CCR6**

Address: Operational Base + offset (0x04c8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 27:25 | RO | 0x0 | dst_cache_ctrl<br>Bit [27]<br>1'b0: AWCACHE[3] is LOW<br>1'b1: AWCACHE[3] is HIGH<br>Bit [26]<br>1'b0: AWCACHE[1] is LOW<br>1'b1: AWCACHE[1] is HIGH<br>Bit [25]<br>1'b0: AWCACHE[0] is LOW<br>1'b1: AWCACHE[0] is HIGH |
| 24:22 | RO | 0x0 | dst_prot_ctrl<br>Bit [24]<br>1'b0: AWPROT[2] is LOW<br>1'b1: AWPROT[2] is HIGH<br>Bit [23]<br>1'b0: AWPROT[1] is LOW<br>1'b1: AWPROT[1] is HIGH<br>Bit [22]<br>1'b0: AWPROT[0] is LOW<br>1'b1: AWPROT[0] is HIGH |
| 21:18 | RO | 0x0 | dst_burst_len<br>the destination data:<br>4'h0: 1 data transfer<br>4'h1: 2 data transfers<br>4'h2: 3 data transfers<br>…<br>4'hf: 16 data transfers<br>The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size. |
| 17:15 | RO | 0x0 | dst_burst_size<br>3'h0: Writes 1 byte per beat<br>3'h1: Writes 2 bytes per beat<br>3'h2: Writes 4 bytes per beat<br>3'h3: Writes 8 bytes per beat<br>3'h4: Writes 16 bytes per beat<br>Others: Reserved<br>The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size. |
| 14 | RO | 0x0 | dst_inc<br>1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW.<br>1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH. |
| 13:11 | RO | 0x0 | src_cache_ctrl<br>Bit [13]<br>1'b0: ARCACHE[2] is LOW<br>1'b1: ARCACHE[2] is HIGH<br>Bit [12]<br>1'b0: ARCACHE[1] is LOW<br>1'b1: ARCACHE[1] is HIGH<br>Bit [11]<br>1'b0: ARCACHE[0] is LOW<br>1'b1: ARCACHE[0] is HIGH |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10:8 | RO | 0x0 | src_prot_ctrl<br>Bit [10]<br>1'b0: ARPROT[2] is LOW<br>1'b1: ARPROT[2] is HIGH<br>Bit [9]<br>1'b0: ARPROT[1] is LOW<br>1'b1: ARPROT[1] is HIGH<br>Bit [8]<br>1'b0: ARPROT[0] is LOW<br>1'b1: ARPROT[0] is HIGH |
| 7:4 | RO | 0x0 | src_burst_len<br>4'h0: 1 data transfer<br>4'h1: 2 data transfers<br>4'h2: 3 data transfers<br>…<br>4'hf: 16 data transfers<br>The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size. |
| 3:1 | RO | 0x0 | src_burst_size<br>3'h0: Reads 1 byte per beat<br>3'h1: Reads 2 bytes per beat<br>3'h2: Reads 4 bytes per beat<br>3'h3: Reads 8 bytes per beat<br>3'h4: Reads 16 bytes per beat<br>Others: Reserved<br>The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size. |
| 0 | RO | 0x0 | src_inc<br>1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW.<br>1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH. |

**DMAC_LC0_6**

Address: Operational Base + offset (0x04cc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0 | reserved |
| 7:0 | RO | 0x00 | loop_counter_iterations<br>Loop counter 0 iterations |

**DMAC_LC1_6**

Address: Operational Base + offset (0x04d0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0 | reserved |
| 7:0 | RO | 0x00 | loop_counter_iterations<br>Loop counter 1 iterations |

**DMAC_SAR7**

Address: Operational Base + offset (0x04e0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | src_addr<br>Address of the source data for DMA channel 7 |

**DMAC_DAR7**

Rockchip Confidencial

Address: Operational Base + offset (0x04e4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | dst_addr<br>Address of the Destination data for DMA channel 7 |

**DMAC_CCR7**

Address: Operational Base + offset (0x04e8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27:25 | RO | 0x0 | dst_cache_ctrl<br>Bit [27]<br>1'b0: AWCACHE[3] is LOW<br>1'b1: AWCACHE[3] is HIGH<br>Bit [26]<br>1'b0: AWCACHE[1] is LOW<br>1'b1: AWCACHE[1] is HIGH<br>Bit [25]<br>1'b0: AWCACHE[0] is LOW<br>1'b1: AWCACHE[0] is HIGH |
| 24:22 | RO | 0x0 | dst_prot_ctrl<br>Bit [24]<br>1'b0: AWPROT[2] is LOW<br>1'b1: AWPROT[2] is HIGH<br>Bit [23]<br>1'b0: AWPROT[1] is LOW<br>1'b1: AWPROT[1] is HIGH<br>Bit [22]<br>1'b0: AWPROT[0] is LOW<br>1'b1: AWPROT[0] is HIGH |
| 21:18 | RO | 0x0 | dst_burst_len<br>the destination data:<br>4'h0: 1 data transfer<br>4'h1: 2 data transfers<br>4'h2: 3 data transfers<br>…<br>4'hf: 16 data transfers<br>The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size. |
| 17:15 | RO | 0x0 | dst_burst_size<br>3'h0: Writes 1 byte per beat<br>3'h1: Writes 2 bytes per beat<br>3'h2: Writes 4 bytes per beat<br>3'h3: Writes 8 bytes per beat<br>3'h4: Writes 16 bytes per beat<br>Others: Reserved<br>The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size. |
| 14 | RO | 0x0 | dst_inc<br>1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW.<br>1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:11 | RO | 0x0 | src_cache_ctrl<br>Bit [13]<br>1'b0: ARCACHE[2] is LOW<br>1'b1: ARCACHE[2] is HIGH<br>Bit [12]<br>1'b0: ARCACHE[1] is LOW<br>1'b1: ARCACHE[1] is HIGH<br>Bit [11]<br>1'b0: ARCACHE[0] is LOW<br>1'b1: ARCACHE[0] is HIGH |
| 10:8 | RO | 0x0 | src_prot_ctrl<br>Bit [10]<br>1'b0: ARPROT[2] is LOW<br>1'b1: ARPROT[2] is HIGH<br>Bit [9]<br>1'b0: ARPROT[1] is LOW<br>1'b1: ARPROT[1] is HIGH<br>Bit [8]<br>1'b0: ARPROT[0] is LOW<br>1'b1: ARPROT[0] is HIGH |
| 7:4 | RO | 0x0 | src_burst_len<br>4'h0: 1 data transfer<br>4'h1: 2 data transfers<br>4'h2: 3 data transfers<br>…<br>4'hf: 16 data transfers<br>The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size. |
| 3:1 | RO | 0x0 | src_burst_size<br>3'h0: Reads 1 byte per beat<br>3'h1: Reads 2 bytes per beat<br>3'h2: Reads 4 bytes per beat<br>3'h3: Reads 8 bytes per beat<br>3'h4: Reads 16 bytes per beat<br>Others: Reserved<br>The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size. |
| 0 | RO | 0x0 | src_inc<br>1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW.<br>1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH. |

**DMAC_LC0_7**

Address: Operational Base + offset (0x04ec)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0 | reserved |
| 7:0 | RO | 0x00 | loop_counter_iterations<br>Loop counter 0 iterations |

**DMAC_LC1_7**

Address: Operational Base + offset (0x04f0)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0 | reserved |
| 7:0 | RO | 0x00 | loop_counter_iterations<br>Loop counter 1 iterations |

**DMAC_DBGSTATUS**

Address: Operational Base + offset (0x0d00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x0 | reserved |
| 0 | RO | 0x0 | dbgstatus<br>1'b0: Idle<br>1'b1: Busy |

**DMAC_DBGCMD**

Address: Operational Base + offset (0x0d04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x0 | reserved |
| 1:0 | WO | 0x0 | dbgcmd<br>2'b00: Execute the instruction that the DMAC_DBGINST [1:0] Registers contain<br>Others: Reserved |

**DMAC_DBGINST0**

Address: Operational Base + offset (0x0d08)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | WO | 0x00 | instruction_byte1<br>Instruction byte 1 |
| 23:16 | WO | 0x00 | instruction_byte0<br>Instruction byte 0 |
| 15:11 | RO | 0x0 | reserved |
| 10:8 | WO | 0x0 | channel_number<br>3'b000: DMA channel 0<br>3'b001: DMA channel 1<br>3'b010: DMA channel 2<br>…<br>3'b111: DMA channel 7 |
| 7:1 | RO | 0x0 | reserved |
| 0 | WO | 0x0 | debug_thread<br>1'b0: DMA manager thread<br>1'b1: DMA channel |

**DMAC_DBGINST1**

Address: Operational Base + offset (0x0d0c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | WO | 0x00 | instruction_byte5<br>Instruction byte 5 |
| 23:16 | WO | 0x00 | instruction_byte4<br>Instruction byte 4 |
| 15:8 | WO | 0x00 | instruction_byte3<br>Instruction byte 3 |
| 7:0 | WO | 0x00 | instruction_byte2<br>Instruction byte 2 |

**DMAC_CR0**

Address: Operational Base + offset (0x0e00)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x0 | reserved |
| 21:17 | RO | 0x0f | num_events<br>5'h0: 1 interrupt output, irq[0]<br>5'h1: 2 interrupt outputs, irq[1:0]<br>5'h2: 3 interrupt outputs, irq[2:0]<br>…<br>5'h1f: 32 interrupt outputs, irq[31:0] |
| 16:12 | RO | 0x13 | num_periph_req<br>5'h0: 1 peripheral request interface<br>5'h1: 2 peripheral request interfaces<br>5'h2: 3 peripheral request interfaces<br>…<br>5'h1f: 32 peripheral request interfaces |
| 11:7 | RO | 0x0 | reserved |
| 6:4 | RO | 0x7 | num_chnls<br>3'b000: 1 DMA channel<br>3'b001: 2 DMA channels<br>3'b010: 3 DMA channels<br>…<br>3'b111: 8 DMA channels |
| 3 | RO | 0x0 | reserved |
| 2 | RO | 0x1 | mgr_ns_at_rst<br>1'b0: boot_manager_ns was LOW<br>1'b1: boot_manager_ns was HIGH |
| 1 | RO | 0x0 | boot_en<br>1'b0: boot_from_pc was LOW<br>1'b1: boot_from_pc was HIGH |
| 0 | RO | 0x1 | periph_req<br>1'b0: The DMAC does not provide a peripheral request interface<br>1'b1: The DMAC provides the number of peripheral request interfaces that the num_periph_req field specifies |

**DMAC_CR1**

Address: Operational Base + offset (0x0e04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0 | reserved |
| 7:4 | RO | 0xb | num_i_cache_lines<br>4'b0000: 1 i-cache line<br>4'b0001: 2 i-cache lines<br>4'b0010: 3 i-cache lines<br>…<br>4'b1111: 16 i-cache lines |
| 3 | RO | 0x0 | reserved |
| 2:0 | RO | 0x5 | i_cache_len<br>3'b010: 4 bytes<br>3'b011: 8 bytes<br>3'b100: 16 bytes<br>3'b101: 32 bytes<br>Others: Reserved |

**DMAC_CR2**

Address: Operational Base + offset (0x0e08)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | boot_addr<br>Provides the value of boot_addr[31:0] when the DMAC exited from reset |

**DMAC_CR3**

Address: Operational Base + offset (0x0e0c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x0000ffff | ins<br>Bit [N]<br>1'b0: Assigns event<N> or irq[N] to the Secure state<br>1'b1: Assigns event<N> or irq[N] to the Non-secure state |

**DMAC_CR4**

Address: Operational Base + offset (0x0e10)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x000fffff | pns<br>Bit [N]<br>1'b0: Assigns peripheral request interface N to the Secure state<br>1'b1: Assigns peripheral request interface N to the Non-secure state |

**DMAC_CRDn**

Address: Operational Base + offset (0x0e14)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:20 | RO | 0x07f | data_buffer_dep<br>10'b000000000: 1 line<br>10'b000000001: 2 lines<br>…<br>10'b111111111: 1024 lines |
| 19:16 | RO | 0xf | rd_q_dep<br>4'b0000: 1 line<br>4'b0001: 2 lines<br>…<br>4'b1111: 16 lines |
| 15 | RO | 0x0 | reserved |
| 14:12 | RO | 0x7 | rd_cap<br>3'b000: 1<br>3'b001: 2<br>…<br>3'b111: 8 |
| 11:8 | RO | 0xf | wr_q_dep<br>4'b0000: 1 line<br>4'b0001: 2 lines<br>…<br>4'b1111: 16 lines |
| 7 | RO | 0x0 | reserved |
| 6:4 | RO | 0x7 | wr_cap<br>3'b000: 1<br>3'b001: 2<br>…<br>3'b111: 8 |
| 3 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2:0 | RO | 0x3 | data_width<br>3'b010: 32-bit<br>3'b011: 64-bit<br>3'b100: 128-bit<br>Others:Reserved |

**DMAC_WD**

Address: Operational Base + offset (0x0e80)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | wd_irq_only<br>1'b0: The DMAC aborts all of the contributing DMA channels and sets irq_abort HIGH<br>1'b1: The DMAC sets irq_abort HIGH |

## 12.5 Timing Diagram

Following picture shows the relationship between dma_req and dma_ack.

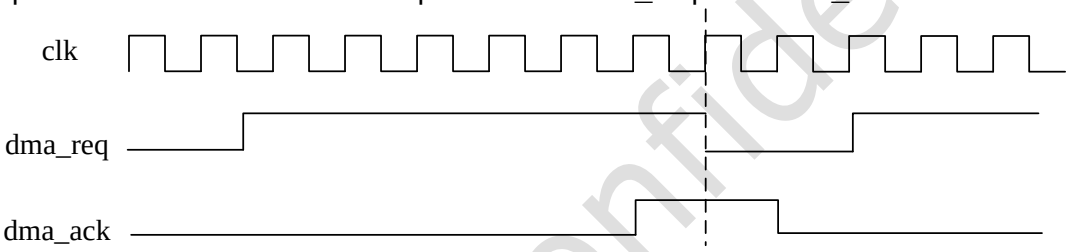



Fig. 12-3 DMAC Request and Acknowledge Timing

## 12.6 Application Notes

### 12.6.1 Using the APB Slave Interfaces

You must ensure that you use the appropriate APB interface, depending on the security state in which the boot_manager_ns initializes the DMAC to operate. For example, if the DMAC is in the secure state, you must issue the instruction using the secure APB interface, otherwise the DMAC ignores the instruction. You can use the secure APB interface, or the non-secure APB interface, to start or restart a DMA channel when the DMAC is in the Non-secure state.

The necessary steps to start a DMA channel thread using the debug instruction registers as following:

1. Create a program for the DMA channel.
2. Store the program in a region of system memory.
3. Poll the DMAC_DBGSTATUS Register to ensure that debug is idle, that is, the dbgstatus bit is 0.
4. Write to the DMAC_DBGINST0 Register and enter the:
- Instruction byte 0 encoding for DMAGO.
- Instruction byte 1 encoding for DMAGO.
- Debug thread bit to 0. This selects the DMA manager thread.

5. Write to the DBGINST1 Register with the DMAGO instruction byte [5:2] data, see Debug Instruction-1 Register o. You must set these four bytes to the address of the first instruction in the program that was written to system memory in step 2.
6. Writing zero to the DMAC_DBGCMD Register. The DMAC starts the DMA channel thread and sets the dbgstatus bit to 1.

### 12.6.2 Security Usage

**DMA manager thread is in the secure state**

If the DNS bit is 0, the DMA manager thread operates in the secure state and it only

Rockchip Confidencial

performs secure instruction fetches. When a DMA manager thread in the secure state processes:

**DMAGO**
It uses the status of the ns bit, to set the security state of the DMA channel thread by writing to the CNS bit for that channel.

**DMAWFE**
It halts execution of the thread until the event occurs. When the event occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding INS bit.

**DMASEV**
It sets the corresponding bit in the INT_EVENT_RIS Register, irrespective of the security state of the corresponding INS bit.

**DMA manager thread is in the Non-secure state**
If the DNS bit is 1, the DMA manager thread operates in the Non-secure state, and it only performs non-secure instruction fetches. When a DMA manager thread in the Non-secure state processes:

**DMAGO**
The DMAC uses the status of the ns bit, to control if it starts a DMA channel thread. If:
ns = 0
The DMAC does not start a DMA channel thread and instead it:
1. Executes a NOP.
2. Sets the DMAC_FSRD Register, see Fault Status DMA Manager
3. Sets the dmago_err bit in the DMAC_FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.
ns = 1
The DMAC starts a DMA channel thread in the Non-secure state and programs the CNS bit to be non-secure.

**DMAWFE**
The DMAC uses the status of the corresponding INS bit, in the DMAC_CR3 Register, to control if it waits for the event. If:
INS = 0
The event is in the Secure state. The DMAC:
1. Executes a NOP.
2. Sets the DMAC_FSRD Register, see Fault Status DMA Manager Register.
3. Sets the mgr_evnt_err bit in the DMAC_FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.
INS = 1
The event is in the Non-secure state. The DMAC halts execution of the thread and waits for the event to occur.

**DMASEV**
The DMAC uses the status of the corresponding INS bit, in the CR3Register, to control if it creates the event-interrupt. If:
INS = 0
The event-interrupt resource is in the secure state. The DMAC:
1. Executes a NOP.
2. Sets the DMAC_FSRD Register, see Fault Status DMA Manager Register.
3. Sets the mgr_evnt_err bit in the DMAC_FTRD Register, see Fault Type DMA Manager Register.

Rockchip Confidencial

4. Moves the DMA manager to the Faulting state.
INS = 1
The event-interrupt resource is in the Non-secure state. The DMAC creates the event-interrupt.

**DMA channel thread is in the secure state**
When the CNS bit is 0, the DMA channel thread is programmed to operate in the Secure state and it only performs secure instruction fetches.
When a DMA channel thread in the secure state processes the following instructions:

**DMAWFE**
The DMAC halts execution of the thread until the event occurs. When the event occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding INS bit, in the DMAC_CR3 Register.

**DMASEV**
The DMAC creates the event-interrupt, irrespective of the security state of the corresponding INS bit, in the DMAC_CR3 Register.

**DMAWFP**
The DMAC halts execution of the thread until the peripheral signals a DMA request. When this occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding PNS bit, in the DMAC_CR4 Register.

**DMALDP, DMASTP**
The DMAC sends a message to the peripheral to communicate that data transfer is complete, irrespective of the security state of the corresponding PNS bit, in the DMAC_CR4 Register.

**DMAFLUSHP**
The DMAC clears the state of the peripheral and sends a message to the peripheral to resend its level status, irrespective of the security state of the corresponding PNS bit, in the DMAC_CR4 Register.
When a DMA channel thread is in the Secure state, it enables the DMAC to perform secure and non-secure AXI accesses.

**DMA channel thread is in the Non-secure state**
When the CNS bit is 1, the DMA channel thread is programmed to operate in the Non-secure state and it only performs non-secure instruction fetches.
When a DMA channel thread in the Non-secure state processes the following instructions:

**DMAWFE**
The DMAC uses the status of the corresponding INS bit, in the DMAC_CR3 Register, to control if it waits for the event. If:
INS = 0
The event is in the Secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_evnt_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
INS = 1
The event is in the Non-secure state. The DMAC halts execution of the thread and waits for the event to occur.

**DMASEV**

Rockchip Confidencial

The DMAC uses the status of the corresponding INS bit, in the DMAC_CR3 Register, to control if it creates the event. If:
INS = 0
The event-interrupt resource is in the Secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_evnt_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
INS = 1
The event-interrupt resource is in the Non-secure state. The DMAC creates the event-interrupt.

**DMAWFP**
The DMAC uses the status of the corresponding PNS bit, in the DMAC_CR4 Register, to control if it waits for the peripheral to signal a request. If:
PNS = 0
The peripheral is in the Secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
PNS = 1
The peripheral is in the Non-secure state. The DMAC halts execution of the thread and waits for the peripheral to signal a request.

**DMALDP, DMASTP**
The DMAC uses the status of the corresponding PNS bit, in the DMAC_CR4 Register, to control if it sends an acknowledgement to the peripheral. If:
PNS = 0
The peripheral is in the secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
PNS = 1
The peripheral is in the Non-secure state. The DMAC sends a message to the peripheral to communicate when the data transfer is complete.

**DMAFLUSHP**
The DMAC uses the status of the corresponding PNS bit, in the DMAC_CR4 Register, to control if it sends a flush request to the peripheral. If:
PNS = 0
The peripheral is in the secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
PNS = 1
The peripheral is in the Non-secure state. The DMAC clears the state of the peripheral and

Rockchip Confidential

sends a message to the peripheral to resend its level status.
When a DMA channel thread is in the Non-secure state, and a DMAMOV CCR instruction attempts to program the channel to perform a secure AXI transaction, the DMAC:
1. Executes a DMANOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_rdwr_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel thread to the Faulting completing state.

## 12.6.3 Programming Restrictions

**Fixed unaligned bursts**

The DMAC does not support fixed unaligned bursts. If you program the following conditions, the DMAC treats this as a programming error:
Unaligned read

- src_inc field is 0 in the DMAC_CCRn(n=0~7) Register
- the DMAC_SARn(n=0~7) Register contains an address that is not aligned to the size of data that the src_burst_size field contain

Unaligned write

- dst_inc field is 0 in the DMAC_CCRn(n=0~7) Register
- the DMAC_DARn(n=0~7) Register contains an address that is not aligned to the size of data that the dst_burst_size field contains

**Endian swap size restrictions**

If you program the endian_swap_size field in the DMAC_CCRn(n=0~7) Register, to enable a DMA channel to perform an endian swap then you must set the corresponding DMAC_SARn(n=0~7) Register and the corresponding DMAC_DARn(n=0~7) Register to contain an address that is aligned to the value that the endian_swap_size field contains.

**Updating DMA channel control registers during a DMA cycle restrictions**

Prior to the DMAC executing a sequence of DMALD and DMAST instructions, the values you program in to the DMAC_CCRn(n=0~7) Register, DMAC_SARn(n=0~7) Register, and DMAC_DARn(n=0~7) Register control the data byte lane manipulation that the DMAC performs when it transfers the data from the source address to the destination address. You'd better not update these registers during a DMA cycle.

**Resource sharing between DMA channels**

DMA channel programs share the MFIFO data storage resource. You must not start a set of concurrently running DMA channel programs with a resource requirement that exceeds the configured size of the MFIFO. If you exceed this limit then the DMAC might lock up and generate a Watchdog abort.

## 12.6.4 Unaligned Transfers

For a configuration with more than one channel, if any of channels 1 to 7 is performing transfers between certain types of misaligned source and destination addresses, then the output data may be corrupted by the action of channel 0.

Data corruption might occur if all of the following are true:
1. Two beats of AXI read data are received for one of channels 1 to 7.
2. Source and destination address alignments mean that each read data beat is split across two lines in the data buffer (see Splitting data, below).
3. There is one idle cycle between the two read data beats.
4. Channel 0 performs an operation that updates channel control information during this idle cycle (see Updates to channel control information, below).

**Splitting data**

Depending upon the programmed values for the DMA transfer, one beat of read data from

Rockchip Confidencial

the AXI interface need to be split across two lines in the internal data buffer. This occurs when the read data beat contains data bytes which will be written to addresses that wrap around at the AXI interface data width, so that these bytes could not be transferred by a single AXI write data beat of the full interface width.

Most applications of DMA do not split data in this way, so are NOT vulnerable to data corruption from this defect.

The following cases are NOT vulnerable to data corruption because they do not split data:

- Byte lane offset between source and destination addresses is 0 when source and destination addresses have the same byte lane alignment, the offset is 0 and a wrap operation that splits data cannot occur.
- Byte lane offset between source and destination addresses is a multiple of source size.

Table 12-3 Source Size in DMAC_CCRn

| Source size in DMAC_CCRn | Allowed offset between DMAC_SARn and DMAC_DARn |
|---|---|
| SS8 | any offset allowed. |
| SS16 | 0,2,4,6,8,10,12,14 |
| SS32 | 0,4,8,12 |
| SS64 | 0,8 |

### 12.6.5 Interrupt Sharing between Channels

As the DMAC does not record which channel (or list of channels) have asserted an interrupt. So it will depend on your program and whether any of the visible information for that program can be used to determine progress, and help identify the interrupt source.
There are 4 likely information sources that can be used to determine the progress made by a program:
- Program counter (PC)
- Source address
- Destination address
- Loop counters (LC)

For example, a program might emit an interrupt each time that it iterates around a loop. In this case, the interrupt service routine (ISR) would need to store the loop value of each channel when it is called, and then compare against the new value when it is next called. A change in value would indicate that the program has progressed.
The ISR must be carefully written to ensure that no interrupts are lost. The sequence of operations is as follows:
1. Disable interrupts
2. Immediately clear the interrupt in DMA-330
3. Check the relevant registers for both channels to determine which must be serviced
4. Take appropriate action for the channels
5. Re-enable interrupts and exit ISR

### 12.6.6 Instruction Sets

Table 12-4 DMAC Instruction Sets

| Mnemonic | Instruction | Thread Usage |
|---|---|---|
| DMAADDH | Add Halfword | C |
| DMAEND | End | M/C |
| DMAFLUSHP | Flush and notify Peripheral | C |
| DMAGO | Go | M |
| DMAKILL | Kill | C |
| DMALD | Load | C |
| DMALDP | Load Peripheral | C |
| DMALP | Loop | C |
| DMALPEND | Loop End | C |
| DMALPFE | Loop Forever | C |

Rockchip Confidential

| | | |
|---|---|---|
| DMAMOV | Move | C |
| DMANOP | No operation | M/C |
| DMARMB | Read Memory Barrier | C |
| DMASEV | Send Event | M/C |
| DMAST | Store | C |
| DMASTP | Store and notify Peripheral | C |
| DMASTZ | Store Zero | C |
| DMAWFE | Wait For Event M | M/C |
| DMAWFP | Wait For Peripheral | C |
| DMAWMB | Write Memory Barrier | C |
| DMAADNH | Add Negative Halfword | C |

*Notes: Thread usage: C=DMA channel, M=DMA manager*

## 12.6.7 Assembler Directives

In this document, only DMMADNH instruction is took as an example to show the way the instruction assembled. For the other instructions, please refer to pl330_trm.pdf.

**DMAADNH**

Add Negative Halfword adds an immediate negative 16-bit value to the DMAC_SARn(n=0~7) Register or DMAC_DARn(n=0~7) Register, for the DMA channel thread. This enables the DMAC to support 2D DMA operations, or reading or writing an area of memory in a different order to naturally incrementing addresses. See Source Address Registers and Destination Address Registers.

The immediate unsigned 16-bit value is one-extended to 32 bits, to create a value that is the two's complement representation of a negative number between -65536 and -1, before the DMAC adds it to the address using 32-bit addition. The DMAC discards the carry bit so that addresses wrap from 0xFFFFFFFF to 0x00000000. The net effect is to subtract between 65536 and 1 from the current value in the Source or Destination Address Register.

Following table shows the instruction encoding.

Table 12-5 DMAC Instruction Encoding

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Imm[15:8] | Imm[7:0] | 0 | 1 | 0 | 1 | 1 | 1 | ra | 0 |

**Assembler syntax**

DMAADNH <address_register>, <16-bit immediate>

where:

<address_register>

Selects the address register to use. It must be either:

SAR

DMAC_SARn(n=0~7) Register and sets ra to 0.

DAR

DMAC_DARn(n=0~7) Register and sets ra to 1.

<16-bit immediate>

The immediate value to be added to the <address_register>.

You should specify the 16-bit immediate as the number that is to be represented in the instruction encoding. For example, DMAADNH DAR, 0xFFF0 causes the value 0xFFFFFFF0 to be added to the current value of the Destination Address Register, effectively subtracting 16 from the DAR.

You can only use this instruction in a DMA channel thread.

Rockchip Confidential

# Chapter 13 SDMMC_BUFFER

## 13.1 Overview

The SDMMC_BUFFER is a data buffer, which transfer data from system DMA to chip external through the SDMMC IOs. The following features are supported by SDMMC_BUFFER

- Support 4 bits data out
- Support 1 bit clock out
- Support DMA hardware handshaking interface
- Support AHB Slave interface
- Support 32x32 fifo

## 13.2 Block Diagram

This section provides a description of SDMMC_BUFFER components.

- AHB slave interface
- DATA FIFO
- DATA IO interface

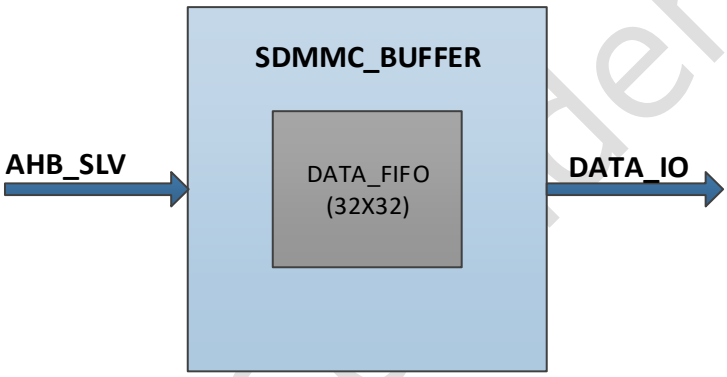



Fig. 13-1 SDMMC_BUFFER Architecture

## 13.3 Function Description

The main block of SDMMC_BUFFER is a 32x32 FIFO, when SDMMC_BUFFER is enable, the DMA handshaking interface is asserted to the system DMA, then the system DMA write data to SDMMC_BUFFER. If the FIFO in SDMMC_BUFFER is not empty, the FIFO data will be transfer to IO

## 13.4 Interface Description

The following table is the interface mapping of between SDMMC_BUF and SDMMC IP.

Table 13-1 SDMMC_BUFFER interface mapping

| SDMMC_BUFFER | SDMMC |
|---|---|
| sdmmc_cclk | sdmmc_cclk |
| sdmmc_cdata0 | sdmmc_cdata0 |
| sdmmc_cdata1 | sdmmc_cdata1 |
| sdmmc_cdata2 | sdmmc_cdata2 |
| sdmmc_cdata3 | sdmmc_cdata3 |

## 13.5 Application Notes

The configuration sequence of enable SDMMC_BUFFER is described as below.

- Set iomux to select sdmmc clock and data io
- Enable IO mux to SDMMC_BUFFER by setting SYS_GRF_SOC_CON10[0]
- Configure write FIFO threshold by setting SYS_GRF_SOC_CON10[7:3]
- Enable SDMMC buffer by setting SYS_GRF_SOC_CON10[1]
- Configure DMA to enable hardware handshaking

Rockchip Confidential

# Chapter 14 Temperature-Sensor ADC (TS-ADC)

## 14.1 Overview

TS-ADC Controller is used to control and get the temperature information. TS-ADC will convert for each enable channel in loop after initial setting and can be stopped by software. If you find that the temperature High in a period of time, an interrupt is generated to the processor down-measures taken; if the temperature over a period of time High, the resulting TSHUT gave CRU module, let it reset the entire chip, or via GPIO give PMIC. Also, if you find that the temperature Low in a period of time, an interrupt can be generated.
TS-ADC Controller supports the following features:

- Support to 7 channel TS-ADC (near chip center, A76_0/1, A76_2/3, DSU and A55_0/1/2/3, PD_CENTER, NPU, GPU)
- The temperature for High and Low interrupt can be configurable
- The temperature of system reset can be configurable
- The time interval of temperature detection can be configurable
- When detecting a high temperature, the time interval of temperature detection can be configurable
- High temperature debounce can be configurable
- An interrupt can be generated after TS-ADC converts all setting channel
- -40~125°C temperature range and 1°C temperature resolution

## 14.2 Block Diagram

TS-ADC controller comprises with:

- APB Interface
- TS-ADC control logic

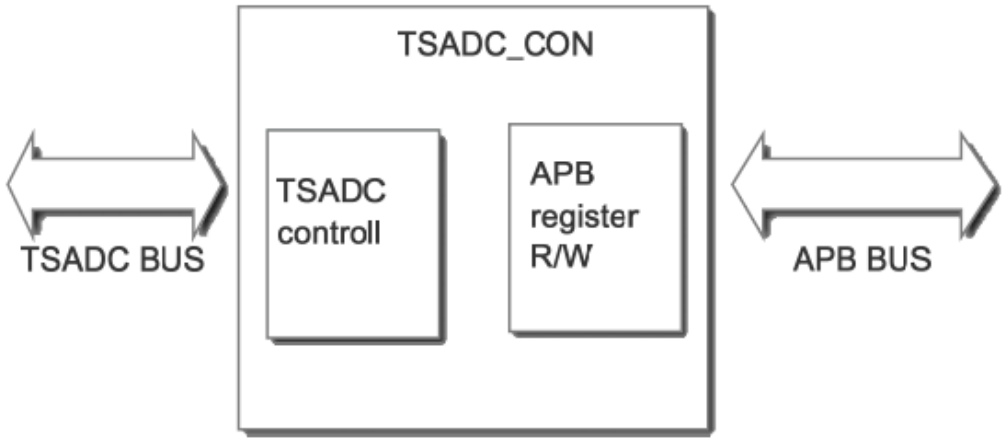



Fig. 14-1 TS-ADC Controller Block Diagram

## 14.3 Function Description

### 14.3.1 APB Interface

There is an APB Slave interface in TS-ADC Controller, which is used to configure the TS-ADC Controller registers and look up the temperature from the temperature sensor.

### 14.3.2 TS-ADC Controller

This block is used to control the TS-ADC PHY to meet the conversion timing and receive the temperature information from TS-ADC PHY.

Rockchip Confidential

## 14.4 Register Description

### 14.4.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| TSADC_USER_CON | 0x0000 | W | 0x00000000 | User control |
| TSADC_AUTO_CON | 0x0004 | W | 0x00000000 | Auto control |
| TSADC_AUTO_STATUS | 0x0008 | W | 0x00000000 | Status used in auto mode |
| TSADC_AUTO_SRC | 0x000C | W | 0x00000000 | Channel select for TSADC in auto mode |
| TSADC_LT_EN | 0x0010 | W | 0x00000000 | Low temperature check logic enable |
| TSADC_HT_INT_EN | 0x0014 | W | 0x00000000 | High temperature interrupt enable |
| TSADC_GPIO_EN | 0x0018 | W | 0x00000000 | Temperature violation to gpio enable |
| TSADC_CRU_EN | 0x001C | W | 0x00000000 | Temperature violation to cru enable |
| TSADC_LT_INT_EN | 0x0020 | W | 0x00000000 | Low temperature interrupt enable |
| TSADC_HLT_INT_PD | 0x0024 | W | 0x00000000 | High and low temperature interrupt status |
| TSADC_EOC_HSHUT_PD | 0x0028 | W | 0x00000000 | High temperature shut and round int status |
| TSADC_DATA0 | 0x002C | W | 0x00000000 | Channel0 data |
| TSADC_DATA1 | 0x0030 | W | 0x00000000 | Channel1 data |
| TSADC_DATA2 | 0x0034 | W | 0x00000000 | Channel2 data |
| TSADC_DATA3 | 0x0038 | W | 0x00000000 | Channel3 data |
| TSADC_DATA4 | 0x003C | W | 0x00000000 | Channel4 data |
| TSADC_DATA5 | 0x0040 | W | 0x00000000 | Channel5 data |
| TSADC_DATA6 | 0x0044 | W | 0x00000000 | Channel6 data |
| TSADC_DATA7 | 0x0048 | W | 0x00000000 | Channel7 data |
| TSADC_DATA8 | 0x004C | W | 0x00000000 | Channel8 data |
| TSADC_DATA9 | 0x0050 | W | 0x00000000 | Channel9 data |
| TSADC_DATA10 | 0x0054 | W | 0x00000000 | Channel10 data |
| TSADC_DATA11 | 0x0058 | W | 0x00000000 | Channel11 data |
| TSADC_DATA12 | 0x005C | W | 0x00000000 | Channel12 data |
| TSADC_DATA13 | 0x0060 | W | 0x00000000 | Channel13 data |
| TSADC_DATA14 | 0x0064 | W | 0x00000000 | Channel14 data |
| TSADC_DATA15 | 0x0068 | W | 0x00000000 | Channel15 data |
| TSADC_COMP0_INT | 0x006C | W | 0x00000000 | High temperature interrupt threshold for channel0 |
| TSADC_COMP1_INT | 0x0070 | W | 0x00000000 | High temperature interrupt threshold for channel1 |
| TSADC_COMP2_INT | 0x0074 | W | 0x00000000 | High temperature interrupt threshold for channel2 |
| TSADC_COMP3_INT | 0x0078 | W | 0x00000000 | High temperature interrupt threshold for channel3 |
| TSADC_COMP4_INT | 0x007C | W | 0x00000000 | High temperature interrupt threshold for channel4 |
| TSADC_COMP5_INT | 0x0080 | W | 0x00000000 | High temperature interrupt threshold for channel5 |
| TSADC_COMP6_INT | 0x0084 | W | 0x00000000 | High temperature interrupt threshold for channel6 |
| TSADC_COMP7_INT | 0x0088 | W | 0x00000000 | High temperature interrupt threshold for channel7 |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| TSADC_COMP8_INT | 0x008C | W | 0x00000000 | High temperature interrupt threshold for channel8 |
| TSADC_COMP9_INT | 0x0090 | W | 0x00000000 | High temperature interrupt threshold for channel9 |
| TSADC_COMP10_INT | 0x0094 | W | 0x00000000 | High temperature interrupt threshold for channel10 |
| TSADC_COMP11_INT | 0x0098 | W | 0x00000000 | High temperature interrupt threshold for channel11 |
| TSADC_COMP12_INT | 0x009C | W | 0x00000000 | High temperature interrupt threshold for channel12 |
| TSADC_COMP13_INT | 0x0100 | W | 0x00000000 | High temperature interrupt threshold for channel13 |
| TSADC_COMP14_INT | 0x0104 | W | 0x00000000 | High temperature interrupt threshold for channel14 |
| TSADC_COMP15_INT | 0x0108 | W | 0x00000000 | High temperature interrupt threshold for channel15 |
| TSADC_COMP0_SHUT | 0x010C | W | 0x00000000 | High temperature shut threshold for channel0 |
| TSADC_COMP1_SHUT | 0x0110 | W | 0x00000000 | High temperature shut threshold for channel1 |
| TSADC_COMP2_SHUT | 0x0114 | W | 0x00000000 | High temperature shut threshold for channel2 |
| TSADC_COMP3_SHUT | 0x0118 | W | 0x00000000 | High temperature shut threshold for channel3 |
| TSADC_COMP4_SHUT | 0x011C | W | 0x00000000 | High temperature shut threshold for channel4 |
| TSADC_COMP5_SHUT | 0x0120 | W | 0x00000000 | High temperature shut threshold for channel5 |
| TSADC_COMP6_SHUT | 0x0124 | W | 0x00000000 | High temperature shut threshold for channel6 |
| TSADC_COMP7_SHUT | 0x0128 | W | 0x00000000 | High temperature shut threshold for channel7 |
| TSADC_COMP8_SHUT | 0x012C | W | 0x00000000 | High temperature shut threshold for channel8 |
| TSADC_COMP9_SHUT | 0x0130 | W | 0x00000000 | High temperature shut threshold for channel9 |
| TSADC_COMP10_SHUT | 0x0134 | W | 0x00000000 | High temperature shut threshold for channel10 |
| TSADC_COMP11_SHUT | 0x0138 | W | 0x00000000 | High temperature shut threshold for channel11 |
| TSADC_COMP12_SHUT | 0x013C | W | 0x00000000 | High temperature shut threshold for channel12 |
| TSADC_COMP13_SHUT | 0x0140 | W | 0x00000000 | High temperature shut threshold for channel13 |
| TSADC_COMP14_SHUT | 0x0144 | W | 0x00000000 | High temperature shut threshold for channel14 |
| TSADC_COMP15_SHUT | 0x0148 | W | 0x00000000 | High temperature shut threshold for channel15 |
| TSADC_HIGH_INT_DEBOUNCE | 0x014C | W | 0x00000003 | High interrupt debounce |
| TSADC_HIGHT_TSHUT_DEBOUNCE | 0x0150 | W | 0x00000003 | High shut debounce |
| TSADC_AUTO_PERIOD | 0x0154 | W | 0x00010000 | Auto conversion period |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| TSADC_AUTO_PERIOD_HT | 0x0158 | W | 0x00010000 | Auto conversion period for high temperature |
| TSADC_COMP0_LOW_INT | 0x015C | W | 0x00000000 | Low temperature threshold for channel0 |
| TSADC_COMP1_LOW_INT | 0x0160 | W | 0x00000000 | Low temperature threshold for channel1 |
| TSADC_COMP2_LOW_INT | 0x0164 | W | 0x00000000 | Low temperature threshold for channel2 |
| TSADC_COMP3_LOW_INT | 0x0168 | W | 0x00000000 | Low temperature threshold for channel3 |
| TSADC_COMP4_LOW_INT | 0x016C | W | 0x00000000 | Low temperature threshold for channel4 |
| TSADC_COMP5_LOW_INT | 0x0170 | W | 0x00000000 | Low temperature threshold for channel5 |
| TSADC_COMP6_LOW_INT | 0x0174 | W | 0x00000000 | Low temperature threshold for channel6 |
| TSADC_COMP7_LOW_INT | 0x0178 | W | 0x00000000 | Low temperature threshold for channel7 |
| TSADC_COMP8_LOW_INT | 0x017C | W | 0x00000000 | Low temperature threshold for channel8 |
| TSADC_COMP9_LOW_INT | 0x0180 | W | 0x00000000 | Low temperature threshold for channel9 |
| TSADC_COMP10_LOW_INT | 0x0184 | W | 0x00000000 | Low temperature threshold for channel10 |
| TSADC_COMP11_LOW_INT | 0x0188 | W | 0x00000000 | Low temperature threshold for channel11 |
| TSADC_COMP12_LOW_INT | 0x018C | W | 0x00000000 | Low temperature threshold for channel12 |
| TSADC_COMP13_LOW_INT | 0x0190 | W | 0x00000000 | Low temperature threshold for channel13 |
| TSADC_COMP14_LOW_INT | 0x0194 | W | 0x00000000 | Low temperature threshold for channel14 |
| TSADC_COMP15_LOW_INT | 0x0198 | W | 0x00000000 | Low temperature threshold for channel15 |
| TSADC_T_SETUP | 0x019C | W | 0x0000002F | Timing for setup |
| TSADC_T_PW_EN | 0x0200 | W | 0x00000027 | Timing for pw_en |
| TSADC_T_EN_CLK | 0x0204 | W | 0x00000001 | Timing for en_clk |
| TSADC_T_NON_OV | 0x0208 | W | 0x00000002 | Timing for non_ov |
| TSADC_T_HOLD | 0x020C | W | 0x00000013 | Timing for hold |
| TSADC_Q_MAX | 0x0210 | W | 0x00000200 | Max data used for data inversion |
| TSADC_STATIC_CON | 0x0214 | W | 0x0280001B | Static control signal |
| TSADC_FLOW_CON | 0x0218 | W | 0x00000000 | Flow control |
| TSADC_CLK_CH_PERIOD | 0x021C | W | 0x0000012B | CLK_CH_TS period control |
| TSADC_T_PW_CLK | 0x0220 | W | 0x00000030 | Timing for pw_clk |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 14.4.2 Detail Register Description

### TSADC_USER_CON

Address: Operational Base + offset (0x0000)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b1: Write access enable<br>1'b0: Write access disable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RO | 0x0 | adc_status<br>1'b0: ADC stop<br>1'b1: Conversion in progress |
| 7 | R/WSC | 0x0 | start<br>When software writes 1 to this bit, start-of-conversion will be asserted.<br>This bit will be cleared after TSADC access finishing.<br>Only when TSADC_USER_CON[5] = 1'b1, this bit takes effect. |
| 6 | RW | 0x0 | eoc_inten<br>Enable eoc interrupt for each conversion.<br>1'b1: Enable<br>1'b0: Disable |
| 5 | RW | 0x0 | start_mode<br>Start mode.<br>1'b0: TSADC controller will assert start_of_conversion after power up.<br>1'b1: The start_of_conversion will be controlled by TSADC_USER_CON[7]. |
| 4 | RW | 0x0 | power_control<br>ADC power control<br>1'b0: power down<br>1'b1: power up<br>This bit is not enable when TSADC_AUTO_CON[0] is set to 1. |
| 3:0 | RW | 0x0 | input_src_sel<br>ADC input source select in user mode.<br>Can be changed from 0 - 6. |

**TSADC_AUTO_CON**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b1: Write access enable<br>1'b0: Write access disable |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | tshut_polarity<br>This bit is used to control the output signal polarity to GPIO when the temperature is higher than threshold.<br>1'b0: Low active<br>1'b1: High active |
| 7:3 | RO | 0x00 | reserved |
| 2 | RW | 0x0 | round_int_en<br>Int enable for round mode. Used for auto mode all channel set is sampled.<br>1'b1: Enable<br>1'b0: Disable |
| 1 | RW | 0x0 | q_sel<br>1'b0: Use tsadc_q as output (positive temperature coefficient)<br>1'b1: Use (q_max - tsadc_q) as output (negative temperature coefficient) |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | auto_en<br>Auto conversion enable<br>1'b0: TSADC controller works at user-define mode<br>1'b1: TSADC controller works at auto mode |

**TSADC_AUTO_STATUS**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3 | RW | 0x0 | ht_wram<br>High temperature status<br>1'b0: TSADC data is not higher than ht shut temperature<br>1'b1: TSADC data is higher than ht shut temperature |
| 2 | RW | 0x0 | auto_status<br>TSADC auto mode status<br>1'b0: Auto mode stop<br>1'b1: Auto mode in progress |
| 1 | W0C | 0x0 | last_tshut_cru<br>Status for cru reset latest tshut, write 1 to clear. |
| 0 | W1C | 0x0 | last_tshut_gpio<br>Status for gpio latest tshut, write 1 to clear. |

**TSADC_AUTO_SRC**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b1: Write access enable<br>1'b0: Write access disable |
| 15:0 | RW | 0x0000 | auto_src<br>Enable channel for TSADC in auto mode. Each bit can enable for one channel from 0 - 6. |

**TSADC_LT_EN**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b1: Write access enable<br>1'b0: Write access disable |
| 15:0 | RW | 0x0000 | low_temperature_vio_en<br>Low temperature violation logic enable, each bit enables one channel.<br>1'b1: Enable<br>1'b0: Disable |

**TSADC_HT_INT_EN**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b1: Write access enable<br>1'b0: Write access disable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0000 | high_temperature_int_en<br>High temperature interrupt enable, each bit enables one channel.<br>1'b1: Enable<br>1'b0: Disable |

**TSADC_GPIO_EN**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b1: Write access enable<br>1'b0: Write access disable |
| 15:0 | RW | 0x0000 | gpio_en<br>Temperature violation to gpio enable, each bit enables one channel.<br>1'b1: Enable<br>1'b0: Disable |

**TSADC_CRU_EN**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b1: Write access enable<br>1'b0: Write access disable |
| 15:0 | RW | 0x0000 | cru_en<br>Temperature violation to cru reset enable, each bit enables one channel.<br>1'b1: Enable<br>1'b0: Disable |

**TSADC_LT_INT_EN**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b1: Write access enable<br>1'b0: Write access disable |
| 15:0 | RW | 0x0000 | low_Temperature_int_en<br>Low temperature interrupt enable, each bit enables one channel.<br>1'b1: Enable<br>1'b0: Disable |

**TSADC_HLT_INT_PD**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | W1C | 0x0000 | lt_int_status<br>Low temperature interrupt status for each channel. |
| 15:0 | W1C | 0x0000 | ht_int_status<br>High temperature interrupt status for each channel. |

**TSADC_EOC_HSHUT_PD**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17 | W1C | 0x0 | round_int_pd<br>Auto mode interrupt for each round of all set channel. |
| 16 | W1C | 0x0 | usr_eoc_irq_pd<br>User mode end interrupt status. |
| 15:0 | W1C | 0x0000 | ht_shut_pd<br>High temperature shut down status for each channel. |

**TSADC_DATA0**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | adc_data<br>A/D value of the channel 0 last conversion. |

**TSADC_DATA1**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | adc_data<br>A/D value of the channel 1 last conversion. |

**TSADC_DATA2**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | adc_data<br>A/D value of the channel 2 last conversion. |

**TSADC_DATA3**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | adc_data<br>A/D value of the channel 3 last conversion. |

**TSADC_DATA4**

Address: Operational Base + offset (0x003C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | adc_data<br>A/D value of the channel 4 last conversion. |

**TSADC_DATA5**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | adc_data<br>A/D value of the channel 5 last conversion. |

**TSADC_DATA6**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:0 | RO | 0x000 | adc_data<br>A/D value of the channel 6 last conversion. |

**TSADC_DATA7**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | adc_data<br>A/D value of the channel 7 last conversion. |

**TSADC_DATA8**

Address: Operational Base + offset (0x004C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | adc_data<br>A/D value of the channel 8 last conversion. |

**TSADC_DATA9**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | adc_data<br>A/D value of the channel 9 last conversion. |

**TSADC_DATA10**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | adc_data<br>A/D value of the channel 10 last conversion. |

**TSADC_DATA11**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | adc_data<br>A/D value of the channel 11 last conversion. |

**TSADC_DATA12**

Address: Operational Base + offset (0x005C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | adc_data<br>A/D value of the channel 12 last conversion. |

**TSADC_DATA13**

Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | adc_data<br>A/D value of the channel 13 last conversion. |

**TSADC_DATA14**

Address: Operational Base + offset (0x0064)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | adc_data<br>A/D value of the channel 14 last conversion. |

**TSADC_DATA15**

Address: Operational Base + offset (0x0068)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | adc_data<br>A/D value of the channel 15 last conversion. |

**TSADC_COMP0_INT**

Address: Operational Base + offset (0x006C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src0<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is high.<br>TSADC_INT will be valid. |

**TSADC_COMP1_INT**

Address: Operational Base + offset (0x0070)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src1<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is high.<br>TSADC_INT will be valid. |

**TSADC_COMP2_INT**

Address: Operational Base + offset (0x0074)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src2<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is high.<br>TSADC_INT will be valid. |

**TSADC_COMP3_INT**

Address: Operational Base + offset (0x0078)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src3<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is high.<br>TSADC_INT will be valid. |

**TSADC_COMP4_INT**

Address: Operational Base + offset (0x007C)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src4<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is high.<br>TSADC_INT will be valid. |

**TSADC_COMP5_INT**

Address: Operational Base + offset (0x0080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src5<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is high.<br>TSADC_INT will be valid. |

**TSADC_COMP6_INT**

Address: Operational Base + offset (0x0084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src6<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is high.<br>TSADC_INT will be valid. |

**TSADC_COMP7_INT**

Address: Operational Base + offset (0x0088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src7<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is high.<br>TSADC_INT will be valid. |

**TSADC_COMP8_INT**

Address: Operational Base + offset (0x008C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src8<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is high.<br>TSADC_INT will be valid. |

**TSADC_COMP9_INT**

Address: Operational Base + offset (0x0090)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:0 | RW | 0x000 | tsadc_comp_src9<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is high.<br>TSADC_INT will be valid. |

**TSADC_COMP10_INT**

Address: Operational Base + offset (0x0094)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src10<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is high.<br>TSADC_INT will be valid. |

**TSADC_COMP11_INT**

Address: Operational Base + offset (0x0098)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src11<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is high.<br>TSADC_INT will be valid. |

**TSADC_COMP12_INT**

Address: Operational Base + offset (0x009C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src12<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is high.<br>TSADC_INT will be valid. |

**TSADC_COMP13_INT**

Address: Operational Base + offset (0x0100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src13<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is high.<br>TSADC_INT will be valid. |

**TSADC_COMP14_INT**

Address: Operational Base + offset (0x0104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:0 | RW | 0x000 | tsadc_comp_src14<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is high.<br>TSADC_INT will be valid. |

**TSADC_COMP15_INT**

Address: Operational Base + offset (0x0108)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src15<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is high.<br>TSADC_INT will be valid. |

**TSADC_COMP0_SHUT**

Address: Operational Base + offset (0x010C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src0<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is too high.<br>TSHUT will be valid. |

**TSADC_COMP1_SHUT**

Address: Operational Base + offset (0x0110)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src1<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is too high.<br>TSHUT will be valid. |

**TSADC_COMP2_SHUT**

Address: Operational Base + offset (0x0114)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src2<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is too high.<br>TSHUT will be valid. |

**TSADC_COMP3_SHUT**

Address: Operational Base + offset (0x0118)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:0 | RW | 0x000 | tsadc_comp_src3<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is too high.<br>TSHUT will be valid. |

**TSADC_COMP4_SHUT**

Address: Operational Base + offset (0x011C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src4<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is too high.<br>TSHUT will be valid. |

**TSADC_COMP5_SHUT**

Address: Operational Base + offset (0x0120)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src5<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is too high.<br>TSHUT will be valid. |

**TSADC_COMP6_SHUT**

Address: Operational Base + offset (0x0124)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src6<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is too high.<br>TSHUT will be valid. |

**TSADC_COMP7_SHUT**

Address: Operational Base + offset (0x0128)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src7<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is too high.<br>TSHUT will be valid. |

**TSADC_COMP8_SHUT**

Address: Operational Base + offset (0x012C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:0 | RW | 0x000 | tsadc_comp_src8<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is too high.<br>TSHUT will be valid. |

**TSADC_COMP9_SHUT**

Address: Operational Base + offset (0x0130)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src9<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is too high.<br>TSHUT will be valid. |

**TSADC_COMP10_SHUT**

Address: Operational Base + offset (0x0134)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src10<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is too high.<br>TSHUT will be valid. |

**TSADC_COMP11_SHUT**

Address: Operational Base + offset (0x0138)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src11<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is too high.<br>TSHUT will be valid. |

**TSADC_COMP12_SHUT**

Address: Operational Base + offset (0x013C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src12<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is too high.<br>TSHUT will be valid. |

**TSADC_COMP13_SHUT**

Address: Operational Base + offset (0x0140)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:0 | RW | 0x000 | tsadc_comp_src13<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is too high.<br>TSHUT will be valid. |

**TSADC_COMP14_SHUT**

Address: Operational Base + offset (0x0144)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src14<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is too high.<br>TSHUT will be valid. |

**TSADC_COMP15_SHUT**

Address: Operational Base + offset (0x0148)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src15<br>TSADC high temperature level.<br>TSADC output is bigger than tsadc_comp, means the temperature is too high.<br>TSHUT will be valid. |

**TSADC_HIGH_INT_DEBOUNCE**

Address: Operational Base + offset (0x014C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x03 | debounce<br>TSADC controller will only generate interrupt or TSHUT when temperature is higher than COMP_INT for "debounce" times. |

**TSADC_HIGHT_TSHUT_DEBOUNCE**

Address: Operational Base + offset (0x0150)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x03 | debounce<br>TSADC controller will only generate interrupt or TSHUT when temperature is higher than COMP_SHUT for "debounce" times. |

**TSADC_AUTO_PERIOD**

Address: Operational Base + offset (0x0154)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00010000 | auto_period<br>When auto mode is enabled, this register controls the interleave between every conversion for all channel enabled of TSADC. |

**TSADC_AUTO_PERIOD_HT**

Address: Operational Base + offset (0x0158)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00010000 | auto_period<br>This register controls the interleave between every conversion for all channel enabled of TSADC after the temperature is higher than COMP_SHUT or COMP_INT. |

**TSADC_COMP0_LOW_INT**

Address: Operational Base + offset (0x015C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src0<br>TSADC low temperature level.<br>TSADC output is lower than tsadc_comp, means the temperature is low.<br>TSADC_LOW_INT will be valid. |

**TSADC_COMP1_LOW_INT**

Address: Operational Base + offset (0x0160)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src1<br>TSADC low temperature level.<br>TSADC output is lower than tsadc_comp, means the temperature is low.<br>TSADC_LOW_INT will be valid. |

**TSADC_COMP2_LOW_INT**

Address: Operational Base + offset (0x0164)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src2<br>TSADC low temperature level.<br>TSADC output is lower than tsadc_comp, means the temperature is low.<br>TSADC_LOW_INT will be valid. |

**TSADC_COMP3_LOW_INT**

Address: Operational Base + offset (0x0168)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src3<br>TSADC low temperature level.<br>TSADC output is lower than tsadc_comp, means the temperature is low.<br>TSADC_LOW_INT will be valid. |

**TSADC_COMP4_LOW_INT**

Address: Operational Base + offset (0x016C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src4<br>TSADC low temperature level.<br>TSADC output is lower than tsadc_comp, means the temperature is low.<br>TSADC_LOW_INT will be valid. |

Rockchip Confidencial

**TSADC_COMP5_LOW_INT**

Address: Operational Base + offset (0x0170)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src5<br>TSADC low temperature level.<br>TSADC output is lower than tsadc_comp, means the temperature is low.<br>TSADC_LOW_INT will be valid. |

**TSADC_COMP6_LOW_INT**

Address: Operational Base + offset (0x0174)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src6<br>TSADC low temperature level.<br>TSADC output is lower than tsadc_comp, means the temperature is low.<br>TSADC_LOW_INT will be valid. |

**TSADC_COMP7_LOW_INT**

Address: Operational Base + offset (0x0178)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src7<br>TSADC low temperature level.<br>TSADC output is lower than tsadc_comp, means the temperature is low.<br>TSADC_LOW_INT will be valid. |

**TSADC_COMP8_LOW_INT**

Address: Operational Base + offset (0x017C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src8<br>TSADC low temperature level.<br>TSADC output is lower than tsadc_comp, means the temperature is low.<br>TSADC_LOW_INT will be valid. |

**TSADC_COMP9_LOW_INT**

Address: Operational Base + offset (0x0180)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src9<br>TSADC low temperature level.<br>TSADC output is lower than tsadc_comp, means the temperature is low.<br>TSADC_LOW_INT will be valid. |

**TSADC_COMP10_LOW_INT**

Address: Operational Base + offset (0x0184)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:0 | RW | 0x000 | tsadc_comp_src10<br>TSADC low temperature level.<br>TSADC output is lower than tsadc_comp, means the temperature is low.<br>TSADC_LOW_INT will be valid. |

**TSADC_COMP11_LOW_INT**

Address: Operational Base + offset (0x0188)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src11<br>TSADC low temperature level.<br>TSADC output is lower than tsadc_comp, means the temperature is low.<br>TSADC_LOW_INT will be valid. |

**TSADC_COMP12_LOW_INT**

Address: Operational Base + offset (0x018C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src12<br>TSADC low temperature level.<br>TSADC output is lower than tsadc_comp, means the temperature is low.<br>TSADC_LOW_INT will be valid. |

**TSADC_COMP13_LOW_INT**

Address: Operational Base + offset (0x0190)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src13<br>TSADC low temperature level.<br>TSADC output is lower than tsadc_comp, means the temperature is low.<br>TSADC_LOW_INT will be valid. |

**TSADC_COMP14_LOW_INT**

Address: Operational Base + offset (0x0194)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | tsadc_comp_src14<br>TSADC low temperature level.<br>TSADC output is lower than tsadc_comp, means the temperature is low.<br>TSADC_LOW_INT will be valid. |

**TSADC_COMP15_LOW_INT**

Address: Operational Base + offset (0x0198)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:0 | RW | 0x000 | tsadc_comp_src15<br>TSADC low temperature level.<br>TSADC output is lower than tsadc_comp, means the temperature is low.<br>TSADC_LOW_INT will be valid. |

**TSADC_T_SETUP**

Address: Operational Base + offset (0x019C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x002f | t_setup<br>The timing between TSADC power up and start conversion. |

**TSADC_T_PW_EN**

Address: Operational Base + offset (0x0200)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0027 | t_pw_en<br>The timing assert start conversion signal (EN_TEMP_SEN_TS). |

**TSADC_T_EN_CLK**

Address: Operational Base + offset (0x0204)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x01 | t_en_clk<br>The timing between dis-assert start conversion signal (EN_TEMP_SEN_TS) and assert CLK_SEN_TS[8]. |

**TSADC_T_NON_OV**

Address: Operational Base + offset (0x0208)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x02 | t_non_ov<br>The timing between each bit assertion of CLK_SENSE_TS. |

**TSADC_T_HOLD**

Address: Operational Base + offset (0x020C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0013 | t_hold<br>The timing between dis-assert CLK_SENSE_TS and TSADC data valid. |

**TSADC_Q_MAX**

Address: Operational Base + offset (0x0210)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |
| 12:0 | RW | 0x0200 | q_max<br>This register used for TSADC_AUTO_CON[1] for inversion output data. |

**TSADC_STATIC_CON**

Address: Operational Base + offset (0x0214)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:27 | RW | 0x00 | buf_vref_sel<br>Offset control for temperature output code. |
| 26:23 | RW | 0x5 | buf_slope_sel<br>Slope control for temperature output code. |
| 22:21 | RW | 0x0 | comp_i_trim<br>Comparator current timing ports. |
| 20:17 | RW | 0x0 | vbe_i_trm<br>Current timing ports for VBE in PTAT generator. |
| 16:13 | RW | 0x0 | verf_trim<br>Reference voltage trimming ports for reference generator. |
| 12:9 | RW | 0x0 | bgr_r_trim<br>BGR control ports in reference generator. |
| 8:5 | RW | 0x0 | bgr_i_trim<br>BJT emitter current control ports in reference generator. |
| 4:2 | RW | 0x6 | avg_mode<br>Average mode control ports for digital filter. |
| 1 | RW | 0x1 | en_dem<br>Dynamic element matching enable port. |
| 0 | RW | 0x1 | en_ch<br>Digital offset cancellation enable port. |

**TSADC_FLOW_CON**

Address: Operational Base + offset (0x0218)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b1: Write access enable<br>1'b0: Write access disable |
| 15:6 | RO | 0x000 | reserved |
| 5 | W1T | 0x0 | usr_clk_ch_start<br>User to toggle clk_ch in user mode, write 1'b1 to toggle the it will be clear by internal logic. |
| 4 | RW | 0x0 | as_pd_mode<br>If this bit set to one, at the end of each round in auto mode, PD pin for temperature will be asserted for saving power. |
| 3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | single_d_mode<br>If this bit set to 1, average data output is not used. |
| 1 | RW | 0x0 | pd_soc_mode<br>If this bit set to 1, CLK_SENSE_TS is not used. |
| 0 | RW | 0x0 | eoc_mode<br>Use eoc to end conversion. |

**TSADC_CLK_CH_PERIOD**

Address: Operational Base + offset (0x021C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x0000012b | clk_ch_period<br>Control the period of CLK_CH_TS. |

**TSADC_T_PW_CLK**

Address: Operational Base + offset (0x0220)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0030 | t_pw_clk<br>The timing for assertion of each bit of CLK_SENSE_TS. |

# 14.5 Application Notes

## 14.5.1 Conversion Flow

The system works as following

1) Set the conversion channel in register TSADC_AUTO_SRC, jump channel is not suggested.
2) Temperature violation and other configuration may be set.
3) Set the bit[0] in register TSADC_AUTO_CON, then TS-ADC will work.
4) Then temperature information can be read from APB interface.
5) If TS-ADC needs to be closed, set bit[0] in register TSADC_AUTO_CON to 1'b0.

## 14.5.2 Timing Diagram

When TS-ADC start to work, the timing will follow the Fig.1-2

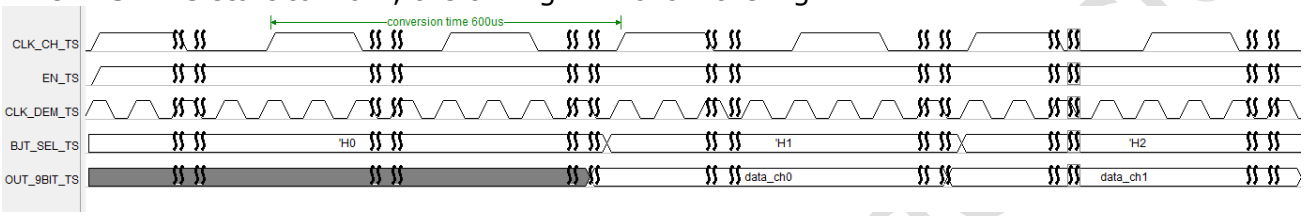



Fig. 14-2 Timing diagram for TS-ADC

When TS-ADC start to work, EN_TS comes to high. Every two CLK_CH_TS cycle, the conversion of one channel is done and channel will change to next one showing as BJT_SEL_TS. Output data from TS-ADC PHY will be kept until next time this channel conversion is done.

CLK_DEM_TS is the main clock for TS-ADC, this clock frequency should be set to 2MHz which can be divided from 24MHz OSC clock. About this please refer to CRU section.

## 14.5.3 Temperature-to-Code Mapping

Table 14-1 Temperature Code Mapping

| Temperature (℃) | ADC Output Data | | |
|---|---|---|---|
| | Min | Typ(Dec) | Max |
| -40 | - | 220 | - |
| 25 | - | 285 | - |
| 85 | - | 345 | - |
| 125 | - | 385 | - |

Note:

Code to Temperature mapping of the Temperature sensor is a linear curve. Any temperature, code falling between to 2 given temperatures can be linearly interpolated.

Code to Temperature mapping should be updated based on silicon results.

Rockchip Confidential

# Chapter 15 Debug

## 15.1 Overview

The chip uses the DAP-LITE2 Technology to support Cortex-A55/Cortex-A76 real-time debug.

### 15.1.1 Features

- Invasive debug with core halted
- SW-DP

### 15.1.2 Debug components address map

The following table shows the debug components address in debug memory map:

| Module | Base Address |
|---|---|
| DAP_ROM | 0x00000 |

## 15.2 Block Diagram

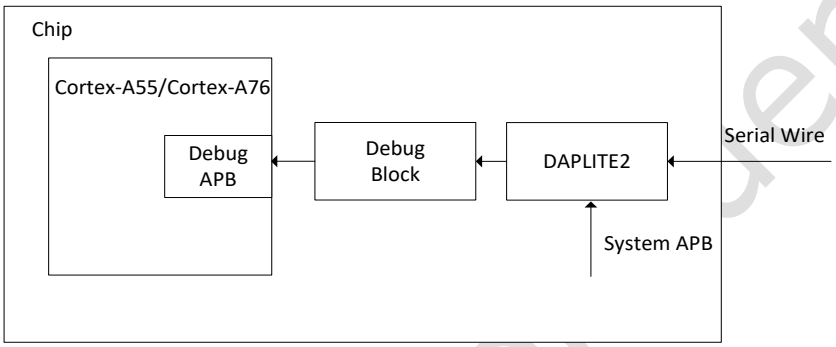



Fig. 15-1 Debug System Structure

## 15.3 Function Description

1.1
2.1
3.1
4.1
5.1

### 15.3.1 DAP

The DAP has following components:

- Serial Wire JTAG Debug Port(SWJ-DP)
- APB Access Port(APB-AP)
- ROM table

The debug port is the host tools interface to access the DAP-Lite2. This interface controls any access ports provided within the DAP-Lite2. The DAP-Lite2 supports a combined debug port which includes both JTAG and Serial Wire Debug(SWD), with a mechanism that supports switching between them.

The APB-AP acts as a bridge between SWJ-DP and APB bus which translate the Debug request to APB bus.

The DAP provides an internal ROM table connected to the master Debug APB port of the APB-Mux. The Debug ROM table is loaded at address 0x00000000 and 0x80000000 of this bus and is accessible from both APB-AP and the system APB input. Bit[31] of the address bus is not connected to the ROM Table, ensuring that both views read the same value. The ROM table stores the locations of the components on the Debug APB.

Please refer to the document CoreSight_DAPLite2_TRM_r0p0.pdf for the debug detail description.

## 15.4 Register Description

Please refer to the document CoreSight_DAPLite2_TRM_r0p0.pdf for the debug detail

Rockchip Confidential

description.

# 15.5 Interface Description

## 15.5.1 DAP SWJ-DP Interface

The following figure is the DAP SWJ-DP interface, the SWJ-DP is a combined JTAG-DP and SW-DP that enable you connect either a Serial Wire Debug(SWJ) to JTAG probe to a target.

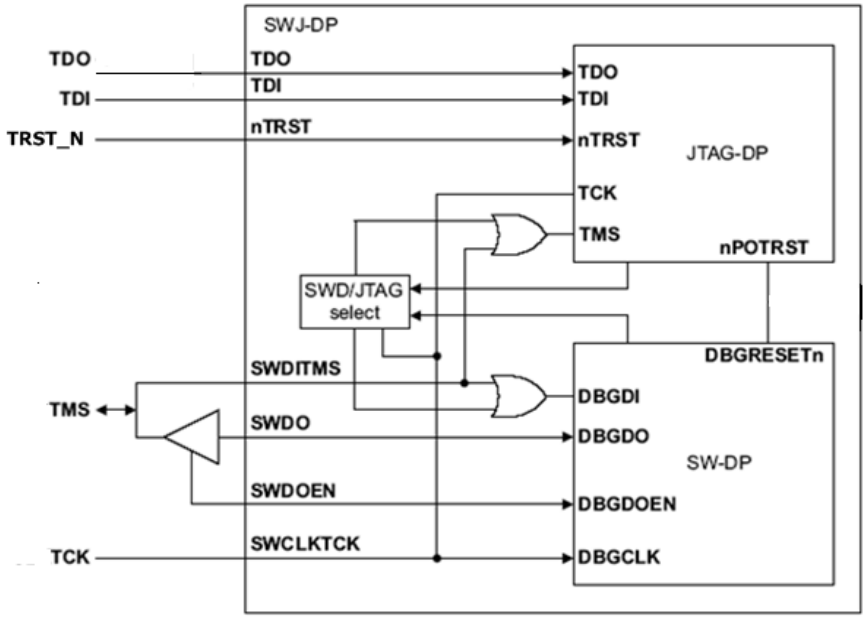



Fig. 15-2 DAP SWJ Interface

## 15.5.2 DAP SW-DP Interface

This implementation is taken from ADIv5.1 and operates with a synchronous serial interface. This uses a single bidirectional data signal, and a clock signal.

The figure below describes the interaction between the timing of transactions on the serial wire interface, and the DAP internal bus transfers. It shows when the target responds with a WAIT acknowledgement.

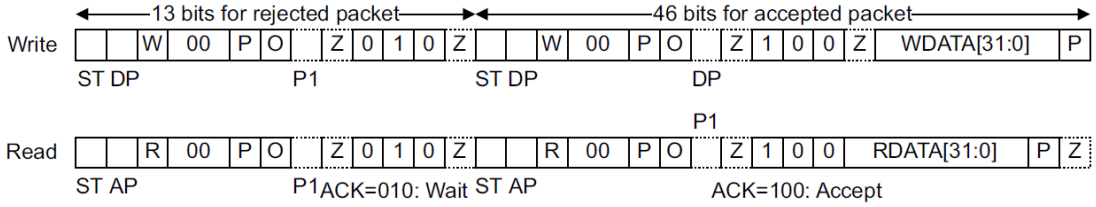



Fig. 15-3 SW-DP Acknowledgement Timing

There are three sets of serial debug interface to debug. By default, jtag_tckm0 and jtag_tmsm0 are connected to corresponding IO pad.

Table 15-1 SW-DP Interface Description

| le pin | Direction | Pad name | IOMUX |
|---|---|---|---|
| jtag_tckm0 | I | SDMMC_D2/PDM1_SDI1_M0/JTAG_TCK_M0/I2C8_SCL_M0/UART5_CTSN_M0/GPIO4_D2_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[11:8]=4'b0101 |
| jtag_tmsm0 | I/O | SDMMC_D3/PDM1_SDI0_M0/JTAG_TMS_M0/I2C8_SDA_M0/UART5_RTSN_M0/PWM10_M1/GPIO4_D3_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[15:12]=4'b0101 |

Rockchip Confidential

| **le pin** | **Direction** | **Pad name** | **IOMUX** |
|---|---|---|---|
| jtag_tck m1 | I | SDMMC_D0/PDM1_SDI3_M0/JTAG_TCK_M1/I2C3_SCL_M4/UART2_TX_M1/PWM8_M1/GPIO4_D0_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[3:0]=4'b0101 |
| jtag_tms m1 | I/O | SDMMC_D1/PDM1_SDI2_M0/JTAG_TMS_M1/I2C3_SDA_M4/UART2_RX_M1/PWM9_M1/GPIO4_D1_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[7:4]=4'b0101 |
| jtag_tck m2 | I | I2S1_MCLK_M1/JTAG_TCK_M2/I2C1_SCL_M0/UART2_TX_M0/PCIE30X1_1_CLKREQN_M0/GPIO0_B5_d | PMU2_IOC_GPIO0B_IOMUX_SEL_H[7:4]=4'b0010 |
| jtag_tms m2 | I/O | I2S1_SCLK_M1/JTAG_TMS_M2/I2C1_SDA_M0/UART2_RX_M0/PCIE30X1_1_WAKEN_M0/GPIO0_B6_d | PMU2_IOC_GPIO0B_IOMUX_SEL_H[11:8]=4'b0010 |

Notes: I=input, O=output, I/O=input/output, bidirectional.

Rockchip Confidencial

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

# Chapter 16 Mailbox

## 16.1 Overview

The Mailbox module is a simple APB peripheral that allows CPU, MCU core to communicate with each other by writing operation to generate interrupt. The registers are accessible via APB interface.
There are three mailbox controllers in RK3588.
The Mailbox has the following main features:

- Support APB interface
- Support four mailbox elements, each element includes one data word, one command word register and one flag bit that can represent one interrupt
- Support interrupts to CPU, and MCU core
- Provide 32 lock registers for software to use to indicate whether mailbox is occupied

## 16.2 Block Diagram

The figure below shows Mailbox block diagram:

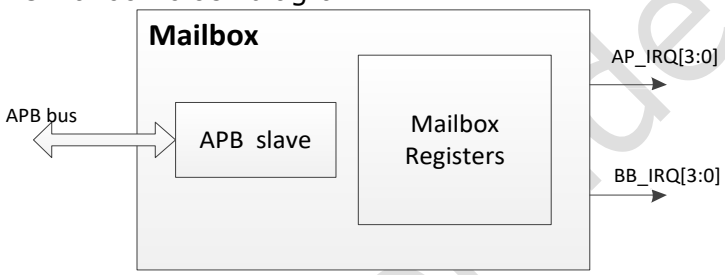



Fig. 16-1 Mailbox Block Diagram

## 16.3 Function Description

### 16.3.1 Mailbox

- Regard CPU as the "AP" side of the Mailbox. The four elements interrupt to CPU is:
  - Enabled when MAILBOX_B2A_INTEN[i] is set to 1 (i=0~3) and the responding IRQs is enabled in GIC.
  - Generated when there are writing operation to corresponding MAILBOX_B2A_CMD_i and MAILBOX_B2A_DAT_i orderly.
  - Cleared when writing 1 to corresponding MAILBOX_B2A_STATUS[i].
- Regard MCU core as the "BB" side of the Mailbox. The four elements interrupt to MCU core is:
  - Enabled when MAILBOX_A2B_INTEN[i] is set to 1 (i=0~3) and the responding IRQs is enabled in INTC of MCU.
  - Generated when there are writing operation to corresponding MAILBOX_A2B_CMD_i and MAILBOX_A2B_DAT_i orderly.
  - Cleared when writing 1 to corresponding MAILBOX_A2B_STATUS[i].
- You can also regard CPU as the "BB" side of the Mailbox and regard MCU core as the "AP" side of the Mailbox. The configuration flow is similar.

## 16.4 Register Description

### 16.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

### 16.4.2 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| MAILBOX_A2B_INTEN | 0x0000 | W | 0x00000000 | AP to BB Interrupt Enable Register |
| MAILBOX_A2B_STATUS | 0x0004 | W | 0x00000000 | AP to BB Interrupt Status Register |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| MAILBOX_A2B_CMD_0 | 0x0008 | W | 0x00000000 | AP to BB Command 0 Register |
| MAILBOX_A2B_DAT_0 | 0x000C | W | 0x00000000 | AP to BB Data 0 Register |
| MAILBOX_A2B_CMD_1 | 0x0010 | W | 0x00000000 | AP to BB Command 1 Register |
| MAILBOX_A2B_DAT_1 | 0x0014 | W | 0x00000000 | AP to BB Data 1 Register |
| MAILBOX_A2B_CMD_2 | 0x0018 | W | 0x00000000 | AP to BB Command 2 Register |
| MAILBOX_A2B_DAT_2 | 0x001C | W | 0x00000000 | AP to BB Data 2 Register |
| MAILBOX_A2B_CMD_3 | 0x0020 | W | 0x00000000 | AP to BB Command 3 Register |
| MAILBOX_A2B_DAT_3 | 0x0024 | W | 0x00000000 | AP to BB Data 3 Register |
| MAILBOX_B2A_INTEN | 0x0028 | W | 0x00000000 | BB to AP Interrupt Enable Register |
| MAILBOX_B2A_STATUS | 0x002C | W | 0x00000000 | BB to AP Interrupt Status Register |
| MAILBOX_B2A_CMD_0 | 0x0030 | W | 0x00000000 | BB to AP Command 0 Register |
| MAILBOX_B2A_DAT_0 | 0x0034 | W | 0x00000000 | BB to AP Data 0 Register |
| MAILBOX_B2A_CMD_1 | 0x0038 | W | 0x00000000 | BB to AP Command 1 Register |
| MAILBOX_B2A_DAT_1 | 0x003C | W | 0x00000000 | BB to AP Data 1 Register |
| MAILBOX_B2A_CMD_2 | 0x0040 | W | 0x00000000 | BB to AP Command 2 Register |
| MAILBOX_B2A_DAT_2 | 0x0044 | W | 0x00000000 | BB to AP Data 2 Register |
| MAILBOX_B2A_CMD_3 | 0x0048 | W | 0x00000000 | BB to AP Command 3 Register |
| MAILBOX_B2A_DAT_3 | 0x004C | W | 0x00000000 | BB to AP Data 3 Register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

### 16.4.3 Detail Registers Description

**MAILBOX_A2B_INTEN**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3 | RW | 0x0 | int3<br>Interrupt enable for int3.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | int2<br>Interrupt enable for int2.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | int1<br>Interrupt enable for int1.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | int0<br>Interrupt enable for int0.<br>1'b0: Disable<br>1'b1: Enable |

**MAILBOX_A2B_STATUS**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3 | W1C | 0x0 | int3<br>Interrupt status for int3.<br>Clear the interrupt by writing 1 to this bit.<br>1'b0: Interrupt is inactive<br>1'b1: Interrupt is active |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | W1C | 0x0 | int2<br>Interrupt status for int2.<br>Clear the interrupt by writing 1 to this bit.<br>1'b0: Interrupt is inactive<br>1'b1: Interrupt is active |
| 1 | W1C | 0x0 | int1<br>Interrupt status for int1.<br>Clear the interrupt by writing 1 to this bit.<br>1'b0: Interrupt is inactive<br>1'b1: Interrupt is active |
| 0 | W1C | 0x0 | int0<br>Interrupt status for int0.<br>Clear the interrupt by writing 1 to this bit.<br>1'b0: Interrupt is inactive<br>1'b1: Interrupt is active |

**MAILBOX_A2B_CMD_0**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | command<br>Command register. |

**MAILBOX_A2B_DAT_0**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | data<br>Data register. |

**MAILBOX_A2B_CMD_1**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | command<br>Command register. |

**MAILBOX_A2B_DAT_1**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | data<br>Data register. |

**MAILBOX_A2B_CMD_2**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | command<br>Command register. |

**MAILBOX_A2B_DAT_2**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | data<br>Data register. |

**MAILBOX_A2B_CMD_3**

Address: Operational Base + offset (0x0020)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | command<br>Command register. |

**MAILBOX_A2B_DAT_3**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | data<br>Data register. |

**MAILBOX_B2A_INTEN**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3 | RW | 0x0 | int3<br>Interrupt enable for int3.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | int2<br>Interrupt enable for int2.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | int1<br>Interrupt enable for int1.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | int0<br>Interrupt enable for int0.<br>1'b0: Disable<br>1'b1: Enable |

**MAILBOX_B2A_STATUS**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3 | W1C | 0x0 | int3<br>Interrupt status for int3.<br>Clear the interrupt by writing 1 to this bit.<br>1'b0: Interrupt is inactive<br>1'b1: Interrupt is active |
| 2 | W1C | 0x0 | int2<br>Interrupt status for int2.<br>Clear the interrupt by writing 1 to this bit.<br>1'b0: Interrupt is inactive<br>1'b1: Interrupt is active |
| 1 | W1C | 0x0 | int1<br>Interrupt status for int1.<br>Clear the interrupt by writing 1 to this bit.<br>1'b0: Interrupt is inactive<br>1'b1: Interrupt is active |
| 0 | W1C | 0x0 | int0<br>Interrupt status for int0.<br>Clear the interrupt by writing 1 to this bit.<br>1'b0: Interrupt is inactive<br>1'b1: Interrupt is active |

Rockchip Confidencial

**MAILBOX_B2A_CMD_0**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | command<br>Command register. |

**MAILBOX_B2A_DAT_0**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | data<br>Data register. |

**MAILBOX_B2A_CMD_1**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | command<br>Command register. |

**MAILBOX_B2A_DAT_1**

Address: Operational Base + offset (0x003C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | data<br>Data register. |

**MAILBOX_B2A_CMD_2**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | command<br>Command register. |

**MAILBOX_B2A_DAT_2**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | data<br>Data register. |

**MAILBOX_B2A_CMD_3**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | command<br>Command register. |

**MAILBOX_B2A_DAT_3**

Address: Operational Base + offset (0x004C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | data<br>Data register. |

## 16.5 Application Notes

- It is recommended to read one ATOMIC_LOCK register first when using the Mailbox. The read value is 0 means it is available, and 1 means it has been automatically locked. Writing to the ATOMIC_LOCK register will clear this bit.
- Write to the CMD register before writing to the DAT register. If wrong order is used, then

Rockchip Confidencial

the interrupt cannot be generated successfully.

- If you want to clear the interrupt, you can read out the STATUS register and writing 1 to corresponding bit.
- MAILBOX0 is suggested to use for communication between MCU in PD_PMU and CPU. MAILBOX1 is suggested to use for communication between MCU in PD_CENTER and CPU. MAILBOX2 is suggested to use for communication between MCU in PD_NPU and CPU.

Rockchip Confidencial

# Chapter 17 Watchdog Timer(WDT)

## 17.1 Overview

Watchdog Timer (WDT) is an APB slave peripheral that can be used to prevent system lockup that caused by conflicting parts or programs in a SOC. The WDT would generate interrupt or reset signal when its counter reaches zero, then a reset controller would reset the system.

WDT supports the following features:

- 32 bits APB bus width
- WDT counter's clock can be chosen from 24MHz or 32KHz clock
- 32 bits WDT counter width
- Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
- WDT can perform two types of operations when timeout occurs:
  - Generate a system reset
  - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
- Programmable reset pulse length
- Total 16 defined-ranges of main timeout period
- There are five WDTs : WDT_PMU,WDT_NPU,WDT_DDR,WDT_S,WDT_NS
- All the five WDTs can drive CRU to generate global software reset

## 17.2 Block Diagram

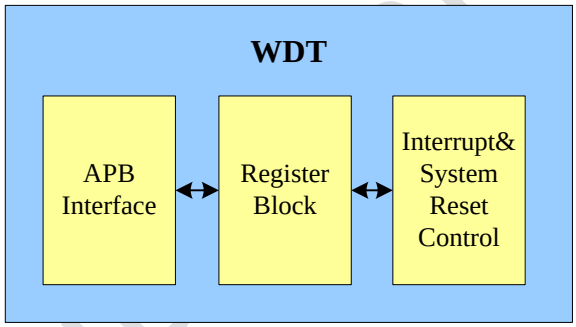



Fig. 17-1 WDT Block Diagram

WDT comprises with:

- APB Interface

The APB Interface implements the APB slave operation. Its data bus width is 32 bits.

- Register Block

A register block that read coherence for the current count register.

- Interrupt & System Reset Control

An interrupt/system reset generation block is comprised of a decrementing counter and control logic.

## 17.3 Function Description

### 17.3.1 Operation

**Counter**

The WDT counts from a preset (timeout) value in descending order to zero. When the counter reaches zero, depending on the output response mode selected, either a system reset or an interrupt occurs. When the counter reaches zero, it wraps to the selected timeout value and continues decrementing. The user can restart the counter to its initial value. This is programmed by writing to the restart register at any time. The process of restarting the watchdog counter is sometimes referred as kicking the dog. As a safety feature to prevent accidental restarts, the value 0x76 must be written to the Current Counter Value Register (WDT_CRR).

Rockchip Confidential

Copyright 2022 © Rockchip Electronics Co., Ltd. 

**Interrupts**

The WDT can be programmed to generate an interrupt (and then a system reset) when a timeout occurs. When a 1 is written to the response mode field (RMOD, bit 1) of the Watchdog Timer Control Register (WDT_CR), the WDT generates an interrupt. If it is not cleared by the time a second timeout occurs, then it generates a system reset. If a restart occurs at the same time the watchdog counter reaches zero, an interrupt is not generated.

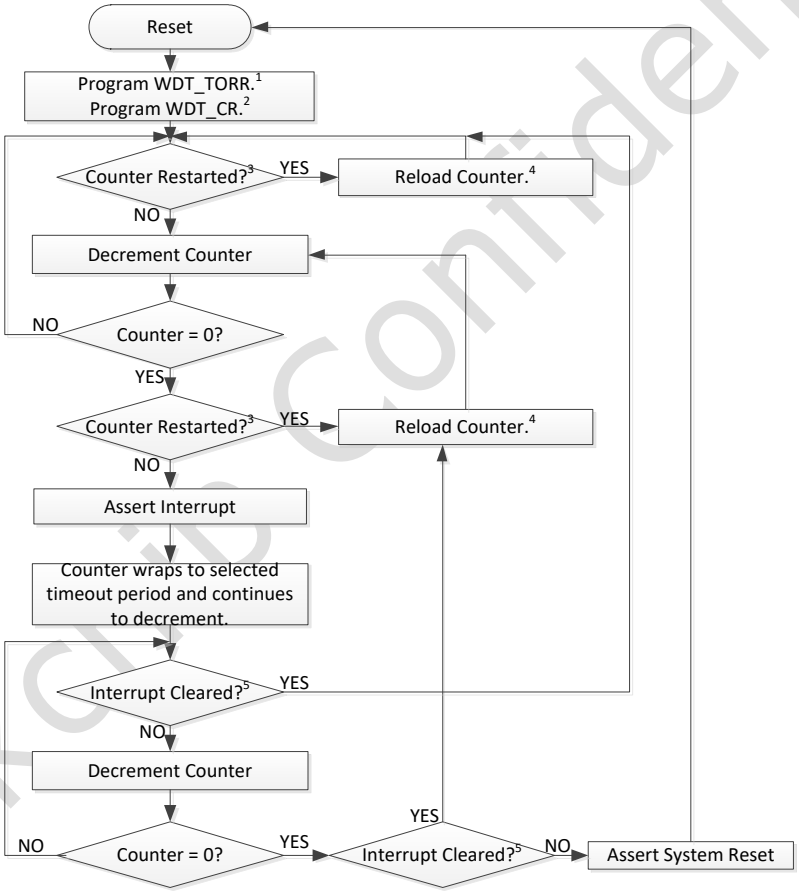
**System Resets**

When a 0 is written to the output response mode field (RMOD, bit 1) of the Watchdog Timer Control Register (WDT_CR), the WDT generates a system reset when a timeout occurs.

**Reset Pulse Length**

The reset pulse length is the number of pclk cycles for which a system reset is asserted. When a system reset is generated, it remains asserted for the number of cycles specified by the reset pulse length or until the system is reset. A counter restart has no effect on the system reset once it has been asserted.

### 17.3.2 Programming Sequence




1. Select required timeout period.
2. Set reset pulse length, response mode, and enable WDT.
3. Write 0x76 to WDT_CRR.
4. Starts back to selected timeout period.
5. Can clear by reading WDT_EOI or restarting (kicking) the counter by writing 0x76 to WDT_CRR.

Fig. 17-2 WDT Operation Flow (RMOD=1)

## 17.4 Register Description

This section describes the control/status registers of the design. Software should read and write these registers using 32-bits accesses. There are five WDTs , and each of them has same register group. Therefore, five WDTs' register groups have five different base addresses.

Rockchip Confidential

### 17.4.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| WDT_CR | 0x0000 | W | 0x00000008 | Control Register |
| WDT_TORR | 0x0004 | W | 0x00000000 | Timeout Range Register |
| WDT_CCVR | 0x0008 | W | 0x0000FFFF | Current Counter Value Register |
| WDT_CRR | 0x000C | W | 0x00000000 | Counter Restart Register |
| WDT_STAT | 0x0010 | W | 0x00000000 | Interrupt Status Register |
| WDT_EOI | 0x0014 | W | 0x00000000 | Interrupt Clear Register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

### 17.4.2 Detail Registers Description

**WDT_CR**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4:2 | RW | 0x2 | rst_pluse_length<br>This is used to select the number of pclk cycles<br>for which the system reset stays asserted.<br>3'b000: 2 pclk cycles<br>3'b001: 4 pclk cycles<br>3'b010: 8 pclk cycles<br>3'b011: 16 pclk cycles<br>3'b100: 32 pclk cycles<br>3'b101: 64 pclk cycles<br>3'b110: 128 pclk cycles<br>3'b111: 256 pclk cycles |
| 1 | RW | 0x0 | resp_mode<br>Selects the output response generated to a timeout.<br>1'b0: Generate a system reset.<br>1'b1: First generate an interrupt and if it is not cleared by the time a second timeout occurs then generate a system reset. |
| 0 | RW | 0x0 | en<br>This bit is used to enable and disable the WDT.When disabled, the counter dose not decrement .Thus, no interrupt or system reset are generated. Once this bit has been enabled, it can be cleared only by a system reset.<br>1'b0: WDT disabled.<br>1'b1: WDT enabled. |

**WDT_TORR**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RW | 0x0 | timeout_period<br>This field is used to select the timeout period from which the watchdog counter restarts. A change of the timeout period takes effect only after the next counter restart (kick).<br>The range of values available for a 32-bit watchdog counter are:<br>4'b0000: 0x0000ffff<br>4'b0001: 0x0001ffff<br>4'b0010: 0x0003ffff<br>4'b0011: 0x0007ffff<br>4'b0100: 0x000fffff<br>4'b0101: 0x001fffff<br>4'b0110: 0x003fffff<br>4'b0111: 0x007fffff<br>4'b1000: 0x00ffffff<br>4'b1001: 0x01ffffff<br>4'b1010: 0x03ffffff<br>4'b1011: 0x07ffffff<br>4'b1100: 0x0fffffff<br>4'b1101: 0x1fffffff<br>4'b1110: 0x3fffffff<br>4'b1111: 0x7fffffff |

**WDT_CCVR**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x0000ffff | cur_cnt<br>This register, when read, is the current value of the internal counter. This value is read coherently whenever it is read. |

**WDT_CRR**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | WO | 0x00 | cnt_restart<br>This register is used to restart the WDT counter. As a safety feature to prevent accidental restarts, the value 0x76 must be written. A restart also clears the WDT interrupt. Reading this register returns zero. |

**WDT_STAT**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RO | 0x0 | status<br>This register shows the interrupt status of the WDT.<br>1'b1: Interrupt is active regardless of polarity.<br>1'b0: Interrupt is inactive. |

**WDT_EOI**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RO | 0x0 | int_clr<br>This can be used to clear the interrupt without restarting the watchdog counter. |

Rockchip Confidencial

## 17.5 Application Notes

- WDTs can trigger global software reset. Please refer to Chapter 3 for more information.

Rockchip Confidencial

Copyright 2022 © Rockchip Electronics Co., Ltd. 

# Chapter 18 Pulse Width Modulation (PWM)

## 18.1 Overview

The pulse-width modulator (PWM) feature is very common in embedded systems. It provides a way to generate a pulse periodic waveform for motor control or can act as a digital-to-analog converter with some external components.
The PWM module supports the following features:

- 4-built-in PWM channels
- Support capture mode
  - Measures the high/low polarity effective cycles of the input waveform
  - Generates a single interrupt at the transition of input waveform polarity
  - 32-bit high polarity capture register
  - 32-bit low polarity capture register
  - 32-bit current value register
  - The capture result can be stored in a FIFO, and the depth of FIFO is 8. The data of FIFO can be read by CPU or DMA
  - Channel 3 support 32-bits power key capture mode
  - Support switch channel IO between channel 3 and channel0/1/2
  - Support a input filter to remove glitch
- Support continuous mode or one-shot mode
  - 32-bit period counter
  - 32-bit duty register
  - 32-bit current value register
  - PWM output polarity in inactive state and duty cycle polarity can be configured
  - Period and duty cycle are shadow buffered. Change takes effect when the end of the effective period is reached or when the channel is disabled
  - Programmable center or left aligned outputs, and change takes effect when the end of the effective period is reached or when the channel is disabled
  - 8-bit repeat counter for one-shot operation. One-shot operation will produce N + 1 periods of the waveform, where N is the repeat counter value, and generates a single interrupt at the end of operation
  - Continuous mode generates the waveform continuously, and does not generates any interrupts
- Support 2 main clock input, one is from crystal oscillator and the frequency is fixed, the other one is from PLL and the frequency can be configured. Each channel can select one of the clocks according to requirement.
- Support two-level frequency division.
- Available low-power mode to reduce power consumption when the channel is inactive.

Rockchip Confidencial

Copyright 2022 © Rockchip Electronics Co., Ltd. 

## 18.2 Block Diagram

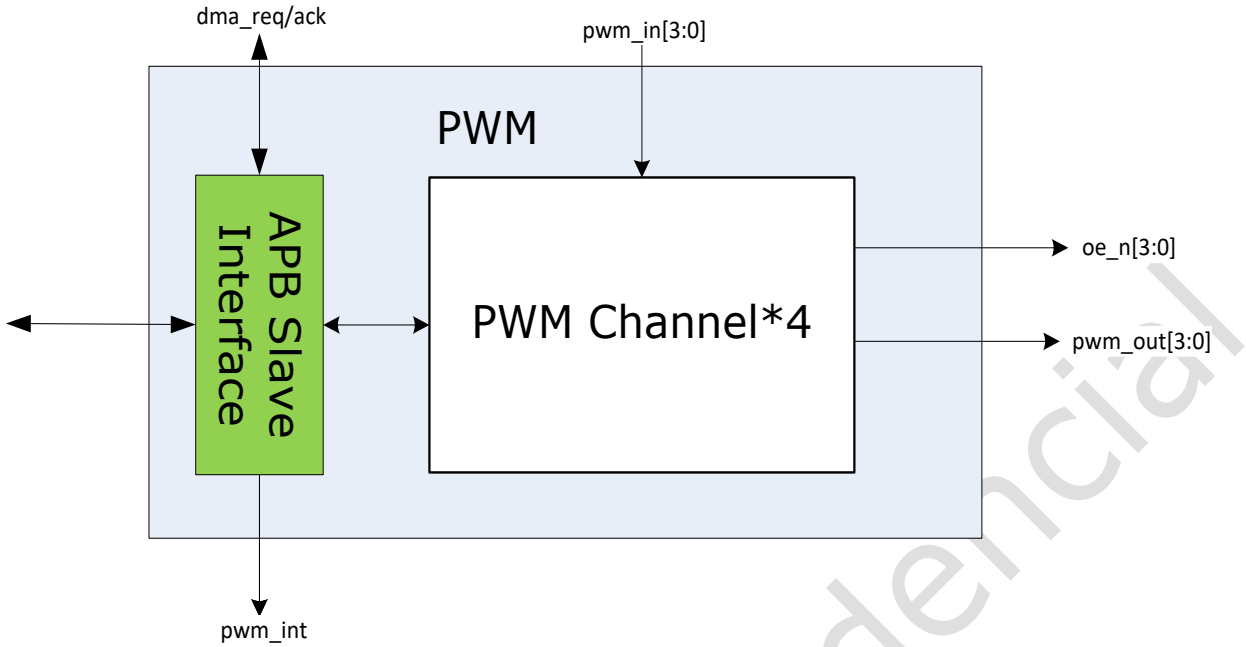



Fig. 18-1 PWM Block Diagram

The host processor gets access to PWM Register Block through the APB slave interface with 32-bit bus width, and asserts the active-high level interrupt. PWM only supports one interrupt output, please refer to interrupt register to know the raw interrupt status when an interrupt is asserted.

PWM Channel is the control logic of PWM module, and controls the operation of PWM module according to the configured working mode.

## 18.3 Function Description

The PWM supports three operation modes: capture mode, one-shot mode and continuous mode. For the one-shot mode and the continuous mode, the PWM output can be configured as the left-aligned mode or the center-aligned mode.

### 18.3.1 Capture mode

The capture mode is used to measure the PWM channel input waveform high/low effective cycles with the PWM channel clock, and asserts an interrupt when the polarity of the input waveform changes. The number of the high effective cycles is recorded in the PWMx_PERIOD_HPC register, while the number of the low effective cycles is recorded in the PWMx_DUTY_LPC register.

*Notes: the PWM input waveform is doubled buffered when the PWM channel is working in order to filter unexpected shot-time polarity transition, and therefore the interrupt is asserted several cycles after the input waveform polarity changes, and so does the change of the values of PWMx_PERIOD_HPC and PWMx_DUTY_LPC.*

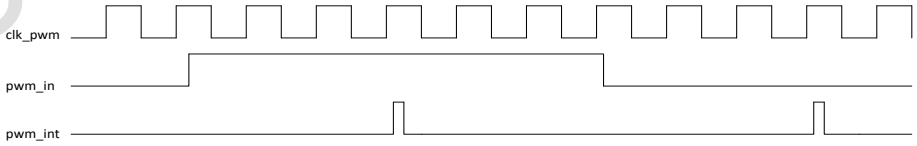



Fig. 18-2 PWM Capture Mode

The capture result can also be stored in a FIFO. The FIFO has an almost full indicator. The indicator can chose to use as an interrupt or DMA request. When it is used as an interrupt, the data in FIFO can be read by CPU. When it is used as a DMA request, the data in FIFO can be read through DMA. It also supports timeout interrupt when the data in FIFO has not been read in a time threshold.

The PWM (only channel 3) support 32-bits power key capture mode. User can configure 10 power key to match, user can poll the status to judge whether a power key access.

Rockchip Confidential

### 18.3.2 Continuous mode

The PWM channel generates a series of the pulses continuously as expected once the channel is enabled with continuous mode.

In the continuous mode, the PWM output waveforms can be in one form of the two output mode: left-aligned mode or center-aligned mode.

For the left-aligned output mode, the PWM channel firstly starts the duty cycle with the configured duty polarity (PWMx_CTRL.duty_pol). Once duty cycle number (PWMx_DUTY_LPC) is reached, the output is switched to the opposite polarity. After the period number (PWMx_PERIOD_HPC) is reached, the output is again switched to the opposite polarity to start another period of desired pulse.

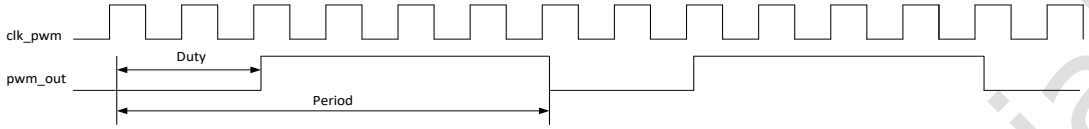



Fig. 18-3 PWM Continuous Left-aligned Output Mode

For the center-aligned output mode, the PWM channel firstly starts the duty cycle with the configured duty polarity (PWMx_CTRL.duty_pol). Once one half of duty cycle number (PWMx_DUTY_LPC) is reached, the output is switched to the opposite polarity. Then if there is one half of duty cycle left for the whole period, the output is again switched to the opposite polarity. Finally after the period number (PWMx_PERIOD_HPC) is reached, the output starts another period of desired pulse.

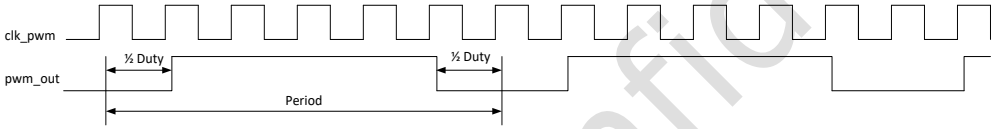



Fig. 18-4 PWM Continuous Center-aligned Output Mode

Once disable the PWM channel, the channel stops generating the output waveforms and output polarity is fixed as the configured inactive polarity (PWMx_CTRL.inactive_pol).

### 18.3.3 One-shot mode

Unlike the continuous mode, the PWM channel generates the output waveforms within the configured periods (PWM_CTRL.rpt + 1), and then stops. At the same times, an interrupt is asserted to inform that the operation has been finished.

There are also two output modes for the one-shot mode: the left-aligned mode and the center-aligned mode.

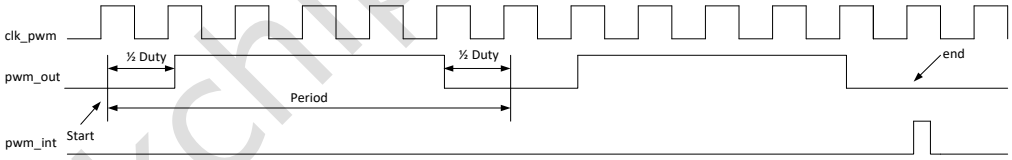



Fig. 18-5 PWM One-shot Center-aligned Output Mode

## 18.4 Register Description

### 18.4.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PWM_PWM0_CNT | 0x0000 | W | 0x00000000 | PWM Channel 0 Counter Register |
| PWM_PWM0_PERIOD_HPR | 0x0004 | W | 0x00000000 | PWM Channel 0 Period Register/High Polarity Capture Register |
| PWM_PWM0_DUTY_LPR | 0x0008 | W | 0x00000000 | PWM Channel 0 Duty Register/Low Polarity Capture Register |
| PWM_PWM0_CTRL | 0x000C | W | 0x00000000 | PWM Channel 0 Control Register |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PWM_PWM1_CNT | 0x0010 | W | 0x00000000 | PWM Channel 1 Counter Register |
| PWM_PWM1_PERIOD_HPR | 0x0014 | W | 0x00000000 | PWM Channel 1 Period Register/High Polarity Capture Register |
| PWM_PWM1_DUTY_LPR | 0x0018 | W | 0x00000000 | PWM Channel 1 Duty Register/Low Polarity Capture Register |
| PWM_PWM1_CTRL | 0x001C | W | 0x00000000 | PWM Channel 1 Control Register |
| PWM_PWM2_CNT | 0x0020 | W | 0x00000000 | PWM Channel 2 Counter Register |
| PWM_PWM2_PERIOD_HPR | 0x0024 | W | 0x00000000 | PWM Channel 2 Period Register/High Polarity Capture Register |
| PWM_PWM2_DUTY_LPR | 0x0028 | W | 0x00000000 | PWM Channel 2 Duty Register/Low Polarity Capture Register |
| PWM_PWM2_CTRL | 0x002C | W | 0x00000000 | PWM Channel 2 Control Register |
| PWM_PWM3_CNT | 0x0030 | W | 0x00000000 | PWM Channel 3 Counter Register |
| PWM_PWM3_PERIOD_HPR | 0x0034 | W | 0x00000000 | PWM Channel 3 Period Register/High Polarity Capture Register |
| PWM_PWM3_DUTY_LPR | 0x0038 | W | 0x00000000 | PWM Channel 3 Duty Register/Low Polarity Capture Register |
| PWM_PWM3_CTRL | 0x003C | W | 0x00000000 | PWM Channel 3 Control Register |
| PWM_INTSTS | 0x0040 | W | 0x00000000 | Interrupt Status Register |
| PWM_INT_EN | 0x0044 | W | 0x00000000 | Interrupt Enable Register |
| PWM_FIFO_CTRL | 0x0050 | W | 0x00000000 | PWM Channel 3 FIFO Mode Control Register |
| PWM_FIFO_INTSTS | 0x0054 | W | 0x00000010 | FIFO Interrupts Status Register |
| PWM_FIFO_TOUTTHR | 0x0058 | W | 0x00000000 | FIFO Timeout Threshold Register |
| PWM_VERSION_ID | 0x005C | W | 0x02120B34 | PWM Version ID Register |
| PWM_FIFO | 0x0060 | W | 0x00000000 | FIFO Register |
| PWM_PWRMATCH_CTRL | 0x0080 | W | 0x00000000 | Power Key Match Control Register |
| PWM_PWRMATCH_LPRE | 0x0084 | W | 0x238C22C4 | Power Key Match Of Low Preload Register |
| PWM_PWRMATCH_HPRE | 0x0088 | W | 0x11F81130 | Power Key Match Of High Preload Register |
| PWM_PWRMATCH_LD | 0x008C | W | 0x029401CC | Power Key Match Of Low Data Register |
| PWM_PWRMATCH_HD_ZERO | 0x0090 | W | 0x029401CC | Power Key Match Of High Data For Zero Register |
| PWM_PWRMATCH_HD_ONE | 0x0094 | W | 0x06FE0636 | Power Key Match Of High Data For One Register |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PWM_PWRMATCH_VALUE_0 | 0x0098 | W | 0x00000000 | Power Key Match Value 0 Register |
| PWM_PWRMATCH_VALUE_1 | 0x009C | W | 0x00000000 | Power Key Match Value 1 Register |
| PWM_PWRMATCH_VALUE_2 | 0x00A0 | W | 0x00000000 | Power Key Match Value 2 Register |
| PWM_PWRMATCH_VALUE_3 | 0x00A4 | W | 0x00000000 | Power Key Match Value 3 Register |
| PWM_PWRMATCH_VALUE_4 | 0x00A8 | W | 0x00000000 | Power Key Match Value 4 Register |
| PWM_PWRMATCH_VALUE_5 | 0x00AC | W | 0x00000000 | Power Key Match Value 5 Register |
| PWM_PWRMATCH_VALUE_6 | 0x00B0 | W | 0x00000000 | Power Key Match Value 6 Register |
| PWM_PWRMATCH_VALUE_7 | 0x00B4 | W | 0x00000000 | Power Key Match Value 7 Register |
| PWM_PWRMATCH_VALUE_8 | 0x00B8 | W | 0x00000000 | Power Key Match Value 8 Register |
| PWM_PWRMATCH_VALUE_9 | 0x00BC | W | 0x00000000 | Power Key Match Value 9 Register |
| PWM_PWM3_PWRCAPTURE_VALUE | 0x00CC | W | 0x00000000 | Channel 3 Power Key Capture Value Register |
| PWM_CHANNEL_IO_CTRL | 0x00D0 | W | 0x00000000 | Channel IO Control Register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 18.4.2 Detail Registers Description

**PWM_PWM0_CNT**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | cnt<br>The 32-bit indicates current value of PWM Channel 0 counter. The counter runs at the rate of PWM clock.<br>The value ranges from 0 to (2^32-1). |

**PWM_PWM0_PERIOD_HPR**

Address: Operational Base + offset (0x0004)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | period_hpr<br>If PWM is operated at the continuous mode or one-shot mode, this value defines the period of the output waveform. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is taken into account and bit [0] always considered as 0.<br>If PWM is operated at the capture mode, this value indicates the effective high polarity cycles of input waveform. This value is based on the PWM clock.<br>The value ranges from 0 to (2^32-1). |

**PWM_PWM0_DUTY_LPR**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | duty_lpr<br>If PWM is operated at the continuous mode or one-shot mode, this value defines the duty cycle of the output waveform. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is taken into account.<br>If PWM is operated at the capture mode, this value indicates the effective low polarity cycles of input waveform.<br>This value is based on the PWM clock. The value ranges from 0 to (2^32-1). |

**PWM_PWM0_CTRL**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | rpt<br>This field defines the repeated effective periods of output waveform in one-shot mode. The value N means N+1 repeated effective periods. |
| 23:16 | RW | 0x00 | scale<br>This field defines the scale factor applied to prescaled clock. The value N means the clock is divided by 2*N. If N is 0, it means that the clock is divided by 512(2*256). |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x0 | prescale<br>This field defines the prescale factor applied to input clock. The value N means that the input clock is divided by 2^N. |
| 11 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10 | RW | 0x0 | clk_src_sel<br>1'b0: Select clk_pwm as root clock source. Clock is from PLL and the frequency can be configured.<br>1'b1: Select clk_pwm_capture as root clock source. Clock is from crystal oscillator and the frequency is fixed. |
| 9 | RW | 0x0 | clk_sel<br>1'b0: Non-scaled clock is selected as PWM clock source. It means that the prescaled clock is directly used as the PWM clock source.<br>1'b1: Scaled clock is selected as PWM clock source. |
| 8 | RW | 0x0 | force_clk_en<br>1'b0: Disabled. When PWM channel is inactive state, the clk_pwm to PWM clock prescale module is blocked to reduce power consumption.<br>1'b1: Enabled. The clk_pwm to PWM Clock prescale module is always enabled. |
| 7 | RW | 0x0 | ch_cnt_en<br>1'b0: Disabled<br>1'b1: Enabled |
| 6 | RW | 0x0 | conlock<br>PWM period and duty lock to previous configuration<br>1'b0: Disable lock<br>1'b1: Enable lock |
| 5 | RW | 0x0 | output_mode<br>1'b0: Left aligned mode<br>1'b1: Center aligned mode |
| 4 | RW | 0x0 | inactive_pol<br>This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled.<br>1'b0: Negative<br>1'b1: Positive |
| 3 | RW | 0x0 | duty_pol<br>This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle.<br>1'b0: Negative<br>1'b1: Positive |
| 2:1 | RW | 0x0 | pwm_mode<br>2'b00: One shot mode. PWM produces the waveform within the repeated times defined by PWM0_CTRL.rpt.<br>2'b01: Continuous mode. PWM produces the waveform continuously.<br>2'b10: Capture mode. PWM measures the cycles of high/low polarity of input waveform.<br>2'b11: Reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | pwm_en<br>1'b0: Disabled<br>1'b1: Enabled<br>If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation. |

**PWM_PWM1_CNT**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | cnt<br>The 32-bit indicates current value of PWM Channel 1 counter. The counter runs at the rate of PWM clock.<br>The value ranges from 0 to (2^32-1). |

**PWM_PWM1_PERIOD_HPR**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | period_hpr<br>If PWM is operated at the continuous mode or one-shot mode, this value defines the period of the output waveform. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is taken into account and bit [0] always considered as 0.<br>If PWM is operated at the capture mode, this value indicates the effective high polarity cycles of input waveform. This value is based on the PWM clock.<br>The value ranges from 0 to (2^32-1). |

**PWM_PWM1_DUTY_LPR**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | duty_lpr<br>If PWM is operated at the continuous mode or one-shot mode, this value defines the duty cycle of the output waveform. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is taken into account.<br>If PWM is operated at the capture mode, this value indicates the effective low polarity cycles of input waveform.<br>This value is based on the PWM clock. The value ranges from 0 to (2^32-1). |

**PWM_PWM1_CTRL**

Address: Operational Base + offset (0x001C)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | rpt<br>This field defines the repeated effective periods of output waveform in one-shot mode. The value N means N+1 repeated effective periods. |
| 23:16 | RW | 0x00 | scale<br>This field defines the scale factor applied to prescaled clock. The value N means the clock is divided by 2*N. If N is 0, it means that the clock is divided by 512(2*256). |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x0 | prescale<br>This field defines the prescale factor applied to input clock. The value N means that the input clock is divided by 2^N. |
| 11 | RO | 0x0 | reserved |
| 10 | RW | 0x0 | clk_src_sel<br>1'b0: Select clk_pwm as root clock source. Clock is from PLL and the frequency can be configured.<br>1'b1: Select clk_pwm_capture as root clock source. Clock is from crystal oscillator and the frequency is fixed. |
| 9 | RW | 0x0 | clk_sel<br>1'b0: Non-scaled clock is selected as PWM clock source. It means that the prescaled clock is directly used as the PWM clock source.<br>1'b1: Scaled clock is selected as PWM clock source. |
| 8 | RW | 0x0 | force_clk_en<br>1'b0: Disabled. When PWM channel is inactive state, the clk_pwm to PWM clock prescale module is blocked to reduce power consumption.<br>1'b1: Enabled. The clk_pwm to PWM Clock prescale module is always enabled. |
| 7 | RW | 0x0 | ch_cnt_en<br>1'b0: Disabled<br>1'b1: Enabled |
| 6 | RW | 0x0 | conlock<br>PWM period and duty lock to previous configuration<br>1'b0: Disable lock<br>1'b1: Enable lock |
| 5 | RW | 0x0 | output_mode<br>1'b0: Left aligned mode<br>1'b1: Center aligned mode |
| 4 | RW | 0x0 | inactive_pol<br>This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled.<br>1'b0: Negative<br>1'b1: Positive |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | duty_pol<br>This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle.<br>1'b0: Negative<br>1'b1: Positive |
| 2:1 | RW | 0x0 | pwm_mode<br>2'b00: One shot mode. PWM produces the waveform within the repeated times defined by PWM1_CTRL.rpt.<br>2'b01: Continuous mode. PWM produces the waveform continuously.<br>2'b10: Capture mode. PWM measures the cycles of high/low polarity of input waveform.<br>2'b11: Reserved |
| 0 | RW | 0x0 | pwm_en<br>1'b0: Disabled<br>1'b1: Enabled<br>If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation. |

**PWM_PWM2_CNT**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | cnt<br>The 32-bit indicates current value of PWM Channel 2 counter. The counter runs at the rate of PWM clock.<br>The value ranges from 0 to (2^32-1). |

**PWM_PWM2_PERIOD_HPR**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | period_hpr<br>If PWM is operated at the continuous mode or one-shot mode, this value defines the period of the output waveform. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is taken into account and bit [0] always considered as 0.<br>If PWM is operated at the capture mode, this value indicates the effective high polarity cycles of input waveform. This value is based on the PWM clock.<br>The value ranges from 0 to (2^32-1). |

**PWM_PWM2_DUTY_LPR**

Address: Operational Base + offset (0x0028)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | duty_lpr<br>If PWM is operated at the continuous mode or one-shot mode, this value defines the duty cycle of the output waveform. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is taken into account.<br>If PWM is operated at the capture mode, this value indicates the effective low polarity cycles of input waveform.<br>This value is based on the PWM clock. The value ranges from 0 to (2^32-1). |

**PWM_PWM2_CTRL**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | rpt<br>This field defines the repeated effective periods of output waveform in one-shot mode. The value N means N+1 repeated effective periods. |
| 23:16 | RW | 0x00 | scale<br>This field defines the scale factor applied to prescaled clock. The value N means the clock is divided by 2*N. If N is 0, it means that the clock is divided by 512(2*256). |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x0 | prescale<br>This field defines the prescale factor applied to input clock. The value N means that the input clock is divided by 2^N. |
| 11 | RO | 0x0 | reserved |
| 10 | RW | 0x0 | clk_src_sel<br>1'b0: Select clk_pwm as root clock source. Clock is from PLL and the frequency can be configured.<br>1'b1: Select clk_pwm_capture as root clock source. Clock is from crystal oscillator and the frequency is fixed. |
| 9 | RW | 0x0 | clk_sel<br>1'b0: Non-scaled clock is selected as PWM clock source. It means that the prescaled clock is directly used as the PWM clock source.<br>1'b1: Scaled clock is selected as PWM clock source. |
| 8 | RW | 0x0 | force_clk_en<br>1'b0: Disabled. When PWM channel is inactive state, the clk_pwm to PWM clock prescale module is blocked to reduce power consumption.<br>1'b1: Enabled. The clk_pwm to PWM Clock prescale module is always enabled. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x0 | ch_cnt_en<br>1'b0: Disabled<br>1'b1: Enabled |
| 6 | RW | 0x0 | conlock<br>PWM period and duty lock to previous configuration<br>1'b0: Disable lock<br>1'b1: Enable lock |
| 5 | RW | 0x0 | output_mode<br>1'b0: Left aligned mode<br>1'b1: Center aligned mode |
| 4 | RW | 0x0 | inactive_pol<br>This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled.<br>1'b0: Negative<br>1'b1: Positive |
| 3 | RW | 0x0 | duty_pol<br>This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle.<br>1'b0: Negative<br>1'b1: Positive |
| 2:1 | RW | 0x0 | pwm_mode<br>2'b00: One shot mode. PWM produces the waveform within the repeated times defined by PWM2_CTRL.rpt.<br>2'b01: Continuous mode. PWM produces the waveform continuously.<br>2'b10: Capture mode. PWM measures the cycles of high/low polarity of input waveform.<br>2'b11: Reserved |
| 0 | RW | 0x0 | pwm_en<br>1'b0: Disabled<br>1'b1: Enabled<br>If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation. |

**PWM_PWM3_CNT**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | cnt<br>The 32-bit indicates current value of PWM Channel 3 counter. The counter runs at the rate of PWM clock.<br>The value ranges from 0 to (2^32-1). |

**PWM_PWM3_PERIOD_HPR**

Rockchip Confidential

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | period_hpr<br>If PWM is operated at the continuous mode or one-shot mode, this value defines the period of the output waveform. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is taken into account and bit [0] always considered as 0.<br>If PWM is operated at the capture mode, this value indicates the effective high polarity cycles of input waveform. This value is based on the PWM clock.<br>The value ranges from 0 to (2^32-1). |

**PWM_PWM3_DUTY_LPR**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | duty_lpr<br>If PWM is operated at the continuous mode or one-shot mode, this value defines the duty cycle of the output waveform. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is taken into account.<br>If PWM is operated at the capture mode, this value indicates the effective low polarity cycles of input waveform.<br>This value is based on the PWM clock. The value ranges from 0 to (2^32-1). |

**PWM_PWM3_CTRL**

Address: Operational Base + offset (0x003C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | rpt<br>This field defines the repeated effective periods of output waveform in one-shot mode. The value N means N+1 repeated effective periods. |
| 23:16 | RW | 0x00 | scale<br>This field defines the scale factor applied to prescaled clock. The value N means the clock is divided by 2*N. If N is 0, it means that the clock is divided by 512(2*256). |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x0 | prescale<br>This field defines the prescale factor applied to input clock. The value N means that the input clock is divided by 2^N. |
| 11 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10 | RW | 0x0 | clk_src_sel<br>1'b0: Select clk_pwm as root clock source. Clock is from PLL and the frequency can be configured.<br>1'b1: Select clk_pwm_capture as root clock source. Clock is from crystal oscillator and the frequency is fixed. |
| 9 | RW | 0x0 | clk_sel<br>1'b0: Non-scaled clock is selected as PWM clock source. It means that the prescaled clock is directly used as the PWM clock source.<br>1'b1: Scaled clock is selected as PWM clock source. |
| 8 | RW | 0x0 | force_clk_en<br>1'b0: Disabled. When PWM channel is inactive state, the clk_pwm to PWM clock prescale module is blocked to reduce power consumption.<br>1'b1: Enabled. The clk_pwm to PWM Clock prescale module is always enabled. |
| 7 | RW | 0x0 | ch_cnt_en<br>1'b0: Disabled<br>1'b1: Enabled |
| 6 | RW | 0x0 | conlock<br>PWM period and duty lock to previous configuration<br>1'b0: Disable lock<br>1'b1: Enable lock |
| 5 | RW | 0x0 | output_mode<br>1'b0: Left aligned mode<br>1'b1: Center aligned mode |
| 4 | RW | 0x0 | inactive_pol<br>This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled.<br>1'b0: Negative<br>1'b1: Positive |
| 3 | RW | 0x0 | duty_pol<br>This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle.<br>1'b0: Negative<br>1'b1: Positive |
| 2:1 | RW | 0x0 | pwm_mode<br>2'b00: One shot mode. PWM produces the waveform within the repeated times defined by PWM3_CTRL.rpt.<br>2'b01: Continuous mode. PWM produces the waveform continuously.<br>2'b10: Capture mode. PWM measures the cycles of high/low polarity of input waveform.<br>2'b11: Reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | pwm_en<br>1'b0: Disabled<br>1'b1: Enabled<br>If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation. |

**PWM_INTSTS**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11 | RO | 0x0 | CH3_Pol<br>This bit is used in capture mode in order to identify the transition of the input waveform when interrupt is generated. When bit is 1, please refer to PWM3_PERIOD_HPR to know the effective high cycle of Channel 3 input waveform. Otherwise, please refer to PWM3_PERIOD_LPR to know the effective low cycle of Channel 3 input waveform. Write 1 to CH3_IntSts will clear this bit. |
| 10 | RO | 0x0 | CH2_Pol<br>This bit is used in capture mode in order to identify the transition of the input waveform when interrupt is generated. When bit is 1, please refer to PWM2_PERIOD_HPR to know the effective high cycle of Channel 2 input waveform. Otherwise, please refer to PWM2_PERIOD_LPR to know the effective low cycle of Channel 2 input waveform. Write 1 to CH2_IntSts will clear this bit. |
| 9 | RO | 0x0 | CH1_Pol<br>This bit is used in capture mode in order to identify the transition of the input waveform when interrupt is generated. When bit is 1, please refer to PWM1_PERIOD_HPR to know the effective high cycle of Channel 1 input waveform. Otherwise, please refer to PWM1_PERIOD_LPR to know the effective low cycle of Channel 1 input waveform. Write 1 to CH1_IntSts will clear this bit. |
| 8 | RO | 0x0 | CH0_Pol<br>This bit is used in capture mode in order to identify the transition of the input waveform when interrupt is generated. When bit is 1, please refer to PWM0_PERIOD_HPR to know the effective high cycle of Channel 0 input waveform. Otherwise, please refer to PWM0_PERIOD_LPR to know the effective low cycle of Channel 0 input waveform. Write 1 to CH0_IntSts will clear this bit. |
| 7 | W1C | 0x0 | CH3_pwr_IntSts<br>1'b0: Channel 3 power key Interrupt not generated<br>1'b1: Channel 3 power key Interrupt generated |
| 6:4 | RO | 0x0 | reserved |
| 3 | W1C | 0x0 | CH3_IntSts<br>1'b0: Channel 3 Interrupt not generated<br>1'b1: Channel 3 Interrupt generated |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | W1C | 0x0 | CH2_IntSts<br>1'b0: Channel 2 Interrupt not generated<br>1'b1: Channel 2 Interrupt generated |
| 1 | W1C | 0x0 | CH1_IntSts<br>1'b0: Channel 1 Interrupt not generated<br>1'b1: Channel 1 Interrupt generated |
| 0 | W1C | 0x0 | CH0_IntSts<br>1'b0: Channel 0 Interrupt not generated<br>1'b1: Channel 0 Interrupt generated |

**PWM_INT_EN**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RW | 0x0 | CH3_pwr_Int_en<br>1'b0: Channel 3 power key Interrupt disabled<br>1'b1: Channel 3 power key Interrupt enabled |
| 6:4 | RO | 0x0 | reserved |
| 3 | RW | 0x0 | CH3_Int_en<br>1'b0: Channel 3 Interrupt disabled<br>1'b1: Channel 3 Interrupt enabled |
| 2 | RW | 0x0 | CH2_Int_en<br>1'b0: Channel 2 Interrupt disabled<br>1'b1: Channel 2 Interrupt enabled |
| 1 | RW | 0x0 | CH1_Int_en<br>1'b0: Channel 1 Interrupt disabled<br>1'b1: Channel 1 Interrupt enabled |
| 0 | RW | 0x0 | CH0_Int_en<br>1'b0: Channel 0 Interrupt disabled<br>1'b1: Channel 0 Interrupt enabled |

**PWM_FIFO_CTRL**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RO | 0x00000 | reserved |
| 13:12 | RW | 0x0 | dma_ch_sel<br>2'b00: Select PWM0<br>2'b01: Select PWM1<br>2'b10: Select PWM2<br>2'b11: Select PWM3 |
| 11 | RO | 0x0 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10 | RW | 0x0 | dma_ch_sel_en<br>1'b0: Disabled. Select the channel PWM3 to FIFO mode and DMA mode.<br>1'b1: Enabled. Use dma_ch_sel to select the channel to FIFO mode and DMA mode. |
| 9 | RW | 0x0 | timeout_en<br>FIFO timeout enable. |
| 8 | RW | 0x0 | dma_mode_en<br>1'b1: Enabled<br>1'b0: Disabled |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x0 | almost_full_watermark<br>Almost full Watermark level. |
| 3 | RW | 0x0 | watermark_int_en<br>Watermark full interrupt. |
| 2 | RW | 0x0 | overflow_int_en<br>When high, an interrupt asserts when the FIFO overflow. |
| 1 | RW | 0x0 | full_int_en<br>When high, an interrupt asserts when the FIFO is full. |
| 0 | RW | 0x0 | fifo_mode_sel<br>When high, PWM FIFO mode is activated. |

**PWM_FIFO_INTSTS**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4 | RO | 0x1 | fifo_empty_status<br>This bit indicates the FIFO is empty. |
| 3 | W1C | 0x0 | timieout_intsts<br>Timeout interrupt. |
| 2 | W1C | 0x0 | fifo_watermark_full_intsts<br>This bit indicates the FIFO is Watermark full. |
| 1 | W1C | 0x0 | fifo_overflow_intsts<br>This bit indicates the FIFO is overflow. |
| 0 | W1C | 0x0 | fifo_full_intsts<br>This bit indicates the FIFO is full. |

**PWM_FIFO_TOUTTHR**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | timeout_threshold<br>FIFO timeout value (Unit: pwm clock). |

**PWM_VERSION_ID**

Rockchip Confidencial

Address: Operational Base + offset (0x005C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x02 | main_version<br>Main version<br>8'h0: Base version<br>8'h1: Support DMA mode<br>8'h2: Support DMA mode and Power key mode |
| 23:16 | RW | 0x13 | minor_version<br>Minor version |
| 15:0 | RW | 0x11B6 | svn_version<br>SVN version |

**PWM_FIFO**

Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | pol<br>This bit indicates the polarity of the lower 31-bit counter.<br>1'b0: Low<br>1'b1: High |
| 30:0 | RO | 0x00000000 | cycle_cnt<br>This 31-bit counter indicates the effective cycles of high/low waveform. |

**PWM_PWRMATCH_CTRL**

Address: Operational Base + offset (0x0080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15 | RW | 0x0 | CH3_pwrkey_int_ctrl<br>1'b0: Assert interrupt after key capture with power key match<br>1'b1: Assert interrupt after key capture without power key match |
| 14:12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | CH3_pwrkey_capture_ctrl<br>1'b0: Capture the value after interrupt<br>1'b1: Capture the value directly |
| 10:8 | RO | 0x0 | reserved |
| 7 | RW | 0x0 | CH3_pwrkey_polarity<br>1'b0: PWM in polarity is positive<br>1'b1: PWM in polarity is negative |
| 6:4 | RO | 0x0 | reserved |
| 3 | RW | 0x0 | CH3_pwrkey_enable<br>1'b0: Disabled<br>1'b1: Enabled |
| 2:0 | RO | 0x0 | reserved |

**PWM_PWRMATCH_LPRE**

Address: Operational Base + offset (0x0084)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x238c | cnt_max<br>The maximum counter value. |
| 15:0 | RW | 0x22c4 | cnt_min<br>The minimum counter value. |

**PWM_PWRMATCH_HPRE**

Address: Operational Base + offset (0x0088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x11f8 | cnt_max<br>The maximum counter value. |
| 15:0 | RW | 0x1130 | cnt_min<br>The minimum counter value. |

**PWM_PWRMATCH_LD**

Address: Operational Base + offset (0x008C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0294 | cnt_max<br>The maximum counter value. |
| 15:0 | RW | 0x01cc | cnt_min<br>The minimum counter value. |

**PWM_PWRMATCH_HD_ZERO**

Address: Operational Base + offset (0x0090)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0294 | cnt_max<br>The maximum counter value. |
| 15:0 | RW | 0x01cc | cnt_min<br>The minimum counter value. |

**PWM_PWRMATCH_HD_ONE**

Address: Operational Base + offset (0x0094)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x06fe | cnt_max<br>The maximum counter value. |
| 15:0 | RW | 0x0636 | cnt_min<br>The minimum counter value. |

**PWM_PWRMATCH_VALUE0**

Address: Operational Base + offset (0x0098)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | pwrkey_match_value<br>Power key match value 0. |

**PWM_PWRMATCH_VALUE1**

Address: Operational Base + offset (0x009C)

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | pwrkey_match_value<br>Power key match value 1. |

**PWM_PWRMATCH_VALUE2**

Address: Operational Base + offset (0x00A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | pwrkey_match_value<br>Power key match value 2. |

**PWM_PWRMATCH_VALUE3**

Address: Operational Base + offset (0x00A4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | pwrkey_match_value<br>Power key match value 3. |

**PWM_PWRMATCH_VALUE4**

Address: Operational Base + offset (0x00A8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | pwrkey_match_value<br>Power key match value 4. |

**PWM_PWRMATCH_VALUE5**

Address: Operational Base + offset (0x00AC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | pwrkey_match_value<br>Power key match value 5. |

**PWM_PWRMATCH_VALUE6**

Address: Operational Base + offset (0x00B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | pwrkey_match_value<br>Power key match value 6. |

**PWM_PWRMATCH_VALUE7**

Address: Operational Base + offset (0x00B4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | pwrkey_match_value<br>Power key match value 7. |

**PWM_PWRMATCH_VALUE8**

Address: Operational Base + offset (0x00B8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | pwrkey_match_value<br>Power key match value 8. |

Rockchip Confidencial

**PWM_PWRMATCH_VALUE9**

Address: Operational Base + offset (0x00BC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | pwrkey_match_value<br>Power key match value 9. |

**PWM_PWM3_PWRCAPTURE_VALUE**

Address: Operational Base + offset (0x00CC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | pwrkey_capture_value<br>Power key capture value. |

**PWM_CHANNEL_IO_CTRL**

Address: Operational Base + offset (0x00D0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:19 | RO | 0x0000 | reserved |
| 18 | RW | 0x0 | CH2_and_CH3_switch_en<br>1'b0: Disabled<br>1'b1: Enabled |
| 17 | RW | 0x0 | CH1_and_CH3_switch_en<br>1'b0: Disabled<br>1'b1: Enabled |
| 16 | RW | 0x0 | CH0_and_CH3_switch_en<br>1'b0: Disabled<br>1'b1: Enabled |
| 15:13 | RO | 0x0 | reserved |
| 12:4 | RW | 0x000 | filter_number<br>Filter window number |
| 3 | RW | 0x0 | CH3_input_filter_enable<br>1'b0: Disabled<br>1'b1: Enabled |
| 2 | RW | 0x0 | CH2_input_filter_enable<br>1'b0: Disabled<br>1'b1: Enabled |
| 1 | RW | 0x0 | CH1_input_filter_enable<br>1'b0: Disabled<br>1'b1: Enabled |
| 0 | RW | 0x0 | CH0_input_filter_enable<br>1'b0: Disabled<br>1'b1: Enabled |

Rockchip Confidencial

## 18.5 Interface Description

Table 18-1 PWM Interface Description

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| PWM0CH0 | I/O | I2S1_LRCK_M1/PWM0_M0/I2C2_SCL_M0/CAN0_TX_M0/SPI0_CS1_M0/PCIE30X1_1_PERSTN_M0/GPIO0_B7_d | PMU2_IOC_GPIO0B_IOMUX_SEL_H[15:12]=4'h3 |
| | | I2S0_SDO3/I2S0_SDI2/PDM0_SDI2_M0/I2C1_SCL_M4/UART4_TX_M0/PWM0_M1/SPI1_CLK_M2/GPIO1_D2_d | BUS_BUS_IOC_GPIO1D_IOMUX_SEL_l[11:8]=4'hb |
| | | VOP_POST_EMPTY/I2C4_SDA_M3/UART6_RTSN_M1/PWM0_M2/SPI4_CLK_M2/GPIO1_A2_d | BUS_IOC_GPIO1A_IOMUX_SEL_L[11:8]=4'hb |
| PWM0CH1 | I/O | PDM0_CLK0_M1/PWM1_M0/I2C2_SDA_M0/CAN0_RX_M0/SPI0_MOSI_M0/PCIE30X1_0_CLKREQN_M0/GPIO0_C0_d | PMU2_IOC_GPIO0C_IOMUX_SEL_L[3:0]=4'h3 |
| | | I2S0_SDI1/PDM0_SDI3_M0/I2C1_SDA_M4/UART4_RX_M0/PWM1_M1/SPI1_CS0_M2/GPIO1_D3_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[15:12]=4'hb |
| | | HDMI_TX1_SDA_M2/I2C4_SCL_M3/UART6_CTSN_M1/PWM1_M2/SPI4_CS0_M2/GPIO1_A3_d | BUS_IOC_GPIO1A_IOMUX_SEL_L[15:12]=4'hb |
| PWM0CH2 | I/O | PDM0_CLK1_M1/PWM2_M0/UART0_RX_M0/I2C4_SDA_M2/DP0_HPDIN_M1/PCIE30X1_0_WAKEN_M0/GPIO0_C4_d | PMU2_IOC_GPIO0C_IOMUX_SEL_H[3:0]=4'h3 |
| | | GMAC1_RXDV_CRS/MIPI_CAMERA4_CLK_M1/UART2_TX_M2/PWM2_M1/GPIO3_B1_d | BUS_IOC_GPIO3B_IOMUX_SEL_L[7:4]=4'hb |
| | | GMAC0_MDC/I2C7_SDA_M1/UART9_RTSN_M0/PWM5_M2/SPI3_MISO_M0/GPIO4_C4_d | BUS_IOC_GPIO4C_IOMUX_SEL_L[11:8]=4'hb |
| PWM0CH3 | I/O | I2S1_SDO2_M1/PDM0_SDI2_M1/PWM3_IR_M0/I2C1_SCL_M2/CAN2_RX_M1/HDMI_TX0_SDA_M1/SPI3_CS0_M2/PCIE30X2_PERSTN_M0/SATA_CPDET/GPIO0_D4_u | PMU2_IOC_GPIO0D_IOMUX_SEL_H[3:0]=4'h3 |
| | | GMAC1_RXDV_CRS/MIPI_CAMERA4_CLK_M1/UART2_TX_M2/PWM2_M1/GPIO3_B1_d | BUS_IOC_GPIO3B_IOMUX_SEL_L[11:8]=4'hb |
| | | I2S0_MCLK/I2C6_SDA_M1/UART3_RTSN/PWM3_IR_M2/SPI4_CLK_M0/GPIO1_C2_d | BUS_IOC_GPIO1C_IOMUX_SEL_L[11:8]=4'hb |
| | | PDM1_SDI0_M1/PCIE30X1_1_PERSTN_M2/PWM3_IR_M3/SPI2_CS0_M0/GPIO1_A7_u | BUS_IOC_GPIO1A_IOMUX_SEL_H=[15:12]=4'hb |

Rockchip Confidential

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| PWM1CH0 | I/O | I2S1_SDI0_M1/GPU_AVS/UART0_TX_M0/I2C4_SCL_M2/DP1_HPDIN_M1/PWM4_M0/PCIE30X1_0_PERSTN_M0/GPIO0_C5_u | BUS_BUS_IOC_GPIO0C_IOMUX_SEL_H[7:4]=4'hb |
| | | GMAC0_MCLKINOUT/I2S2_SDO_M0/I2C7_SCL_M1/PWM4_M1/SPI3_CS1_M0/GPIO4_C3_d | BUS_IOC_GPIO4C_IOMUX_SEL_L[15:12]=4'hb |
| PWM1CH1 | I/O | SPI2_CS0_M2/I2C1_SDA_M1/PWM5_M0/UART0_TX_M1/GPIO0_B1_z | PMU1_IOC_GPIO0B_IOMUX_SEL_L[7:4]=4'h3 |
| | | I2S1_SDI1_M1/NPU_AVS/UART0_RTSN/PWM5_M1/SPI0_CLK_M0/PCIE30X4_CLKREQN_M0/SATA_CP_POD/GPIO0_C6_u | BUS_BUS_IOC_GPIO0C_IOMUX_SEL_H[11:8]=4'hb |
| | | GMAC0_MDC/I2C7_SDA_M1/UART9_RTSN_M0/PWM5_M2/SPI3_MISO_M0/GPIO4_C4_d | BUS_IOC_GPIO4C_IOMUX_SEL_H[3:0]=4'hb |
| PWM1CH2 | I/O | I2S1_SDI2_M1/PDM0_SDI0_M1/I2C6_SDA_M0/UART1_RTSN_M2/PWM6_M0/SPI0_MISO_M0/PCIE30X4_WAKEN_M0/GPIO0_C7_d | BUS_BUS_IOC_GPIO0C_IOMUX_SEL_H[15:12]=4'hb |
| | | BT1120_D15/SPDIF1_TX_M2/PCIE20X1_2_PERSTN_M1/HDMI_TX0_CEC_M0/I2C8_SDA_M3/PWM6_M1/SPI3_CS1_M1/GPIO4_C1_d | BUS_IOC_GPIO4C_IOMUX_SEL_L[7:4]=4'hb |
| | | GMAC0_MDIO/I2C0_SCL_M1/UART9_CTSN_M0/PWM6_M2/SPI3_MOSI_M0/GPIO4_C5_d | BUS_IOC_GPIO4C_IOMUX_SEL_H[7:4]=4'hb |
| PWM1CH3 | I/O | I2S1_SDI3_M1/PDM0_SDI1_M1/I2C6_SCL_M0/UART1_CTSN_M2/PWM7_IR_M0/SPI3_MISO_M2/PCIE30X4_PERSTN_M0/GPIO0_D0_d | BUS_BUS_IOC_GPIO0D_IOMUX_SEL_L[3:0]=4'hb |
| | | SDMMC_CMD/PDM1_CLK1_M0/MCU_JTAG_TCK_M0/CAN0_TX_M1/UART5_RX_M0/PWM7_IR_M1/GPIO4_D4_u | BUS_IOC_GPIO4D_IOMUX_SEL_H[3:0]=4'hb |
| | | I2S0_SCLK/I2C6_SCL_M1/UART3_CTSN/PWM7_IR_M2/SPI4_CS0_M0/GPIO1_C3_d | BUS_IOC_GPIO1C_IOMUX_SEL_L[15:12]=4'hb |
| | | GMAC0_TXER/I2C0_SDA_M1/UART7_CTSN_M0/PWM7_IR_M3/SPI3_CLK_M0/GPIO4_C6_d | BUS_IOC_GPIO4C_IOMUX_SEL_H[11:8]=4'hb |
| PWM2CH0 | I/O | GMAC1_RXD0/MIPI_CAMERA2_CLK_M1/PWM8_M0/GPIO3_A7_u | BUS_IOC_GPIO3A_IOMUX_SEL_H[15:12]=4'hb |
| | | SDMMC_D0/PDM1_SDI3_M0/JTAG_TCK_M1/I2C3_SCL_M4/UART2_TX_M1/PWM8_M1/GPIO4_D0_u | BUS_IOC_GPIO3D_IOMUX_SEL_L[3:0]=4'hb |

Rockchip Confidential

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| | | CIF_D12/PCIE20X1_2_WAKEN_M0/HDMI_TX0_SDA_M2/I2C5_SDA_M0/UART4_RX_M1/PWM8_M2/SPI3_CLK_M3/GPIO3_D0_u | BUS_IOC_GPIO3D_IOMUX_SEL_L[3:0]=4'hb |
| PWM2CH1 | I/O | GMAC1_RXD1/MIPI_CAMERA3_CLK_M1/PWM9_M0/GPIO3_B0_u | BUS_IOC_GPIO3B_IOMUX_SEL_L[3:0]=4'hb |
| | | SDMMC_D1/PDM1_SDI2_M0/JTAG_TMS_M1/I2C3_SDA_M4/UART2_RX_M1/PWM9_M1/GPIO4_D1_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[7:4]=4'hb |
| | | CIF_D13/PCIE20X1_2_PERSTN_M0/HDMI_RX_CEC_M1/UART4_TX_M1/PWM9_M2/SPI0_MISO_M3/GPIO3_D1_d | BUS_IOC_GPIO3D_IOMUX_SEL_L[7:4]=4'hb |
| PWM2CH2 | I/O | GMAC1_TXD2/SDIO_D0_M1/I2S3_MCLK/FSPI_D0_M2/I2C6_SDA_M4/PWM10_M0/SPI4_MISO_M1/GPIO3_A0_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[3:0]=4'hb |
| | | SDMMC_D3/PDM1_SDI0_M0/JTAG_TMS_M0/I2C8_SDA_M0/UART5_RTSN_M0/PWM10_M1/GPIO4_D3_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[15:12]=4'hb |
| | | CIF_D15/PCIE30X2_WAKEN_M2/HDMI_RX_SDA_M1/I2C7_SDA_M2/UART9_CTSN_M2/PWM10_M2/SPI0_CLK_M3/GPIO3_D3_d | BUS_IOC_GPIO3D_IOMUX_SEL_L[15:12]=4'hb |
| PWM2CH3 | I/O | GMAC1_TXD3/SDIO_D1_M1/I2S3_SCLK/AUDDSM_LN/FSPI_D1_M2/I2C6_SCL_M4/PWM11_IR_M0/SPI4_MOSI_M1/GPIO3_A1_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[7:4]=4'hb |
| | | CIF_CLKOUT/BT1120_D10/I2S1_SDO3_M0/PCIE30X4_CLKREQN_M1/DP0_HPDIN_M0/SPDIF0_TX_M1/UART9_TX_M1/PWM11_IR_M1/GPIO4_B4_u | BUS_IOC_GPIO4B_IOMUX_SEL_H[3:0]=4'hb |
| | | PDM0_CLK1_M0/I2C2_SDA_M3/PWM11_IR_M2/SPI4_CS1_M0/GPIO1_C4_d | BUS_IOC_GPIO1C_IOMUX_SEL_H[3:0]=4'hb |
| | | PCIE30X4_BUTTON_RSTN/DP1_HPDIN_M0/MCU_JTAG_TMS_M1/UART9_TX_M2/PWM11_IR_M3/SPI0_CS1_M3/GPIO3_D5_d | BUS_IOC_GPIO3D_IOMUX_SEL_H[7:4]=4'hb |
| PWM3CH0 | I/O | GMAC1_TXEN/I2S2_SCLK_M1/CAN1_RX_M0/UART3_TX_M1/PWM12_M0/GPIO3_B5_u | BUS_IOC_GPIO3B_IOMUX_SEL_H[7:4]=4'hb |
| | | BT1120_D11/PCIE30X4_WAKEN_M1/HDMI_RX_CEC_M0/SATA1_ACT_LED_M0/UART9_RX_M1/PWM12_M1/SPI3_MISO_M1/GPIO4_B5_d | BUS_IOC_GPIO4B_IOMUX_SEL_H[7:4]=4'hb |

Rockchip Confidential

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| PWM3CH1 | I/O | GMAC1_MCLKINOUT/II2S2_LRCK_M1/CAN1_TX_M0/UART3_RX_M1/PWM13_M0/GPIO3_B6_d | BUS_IOC_GPIO3B_IOMUX_SEL_H[11:8]=4'hb |
| | | BT1120_D12/PCIE30X4_PERSTN_M1/HDMI_RX_HPDOUT_M0/SATA0_ACT_LED_M0/I2C5_SCL_M1/PWM13_M1/SPI3_MOSI_M1/GPIO4_B6_d | BUS_IOC_GPIO4B_IOMUX_SEL_H[11:8]=4'hb |
| | | GMAC0_TXD1/I2S2_SCLK_M0/I2C5_SDA_M4/UART1_TX_M0/GPIO2_B7_d | BUS_IOC_GPIO1B_IOMUX_SEL_H[15:12]=4'hb |
| PWM3CH2 | I/O | GMAC1_MDC/MIPI_TE0/I2C8_SCL_M4/UART7_RTSN_M1/PWM14_M0/SPI1_CS0_M1/GPIO3_C2_d | BUS_IOC_GPIO3C_IOMUX_SEL_L[11:8]=4'hb |
| | | CIF_HREF/BT1120_D8/I2S1_SDO1_M0/PCIE30X1_1_BUTTON_RSTN/I2C7_SCL_M3/UART8_RTSN_M0/PWM14_M1/SPI0_CS0_M1/CAN1_RX_M1/GPIO4_B2_u | BUS_IOC_GPIO4B_IOMUX_SEL_L[11:8]=4'hb |
| | | MIPI_CAMERA3_CLK_M0/HDMI_RX_SCL_M2/I2C8_SCL_M2/UART1_RTSN_M1/PWM14_M2/GPIO1_D6_u | BUS_IOC_GPIO1D_IOMUX_SEL_H[11:8]=4'hb |
| PWM3CH3 | I/O | GMAC1_MDIO/MIPI_TE1/I2C8_SDA_M4/UART7_CTSN_M1/PWM15_IR_M0/SPI1_CS1_M1/GPIO3_C3_d | BUS_IOC_GPIO3C_IOMUX_SEL_L[15:12]=4'hb |
| | | CIF_VSYNC/BT1120_D9/I2S1_SDO2_M0/PCIE20X1_2_BUTTON_RSTN/I2C7_SDA_M3/UART8_CTSN_M0/PWM15_IR_M1/CAN1_TX_M1/GPIO4_B3_u | BUS_IOC_GPIO4B_IOMUX_SEL_L[15:12]=4'hb |
| | | PDM0_CLK0_M0/I2C4_SDA_M4/PWM15_IR_M2/GPIO1_C6_d | BUS_IOC_GPIO1C_IOMUX_SEL_H[11:8]=4'hb |
| | | MIPI_CAMERA4_CLK_M0/PCIE30X2_CLKREQN_M3/HDMI_RX_SDA_M2/I2C8_SDA_M2/UART1_CTSN_M1/PWM15_IR_M3/GPIO1_D7_u | BUS_IOC_GPIO1D_IOMUX_SEL_H[15:12]=4'hb |

*Notes: Unused Module Pin is tied to zero! I=input, O=output, I/O=input/output, bidirectional*

# 18.6 Application Notes

## 18.6.1 PWM Capture Mode Standard Usage Flow

1. Set PWM_PWMx_CTRL.pwm_en to '0' to disable the PWM channel.
2. Choose the prescale factor and the scale factor for clk_pwm by programming PWM_PWMx_CTRL.prescale and PWM_PWMx_CTRL.scale, and select the clock needed by setting PWM_PWMx_CTRL.clk_sel and PWM_PWMx_CTRL.clk_src_sel.
3. Configure the channel to work in the capture mode.
4. Enable the PWM_INT_EN.chx_int_en to enable the interrupt generation.
5. Set PWM_CHANNEL_IO_CTRL. filter_number, then Enable the PWM_CHANNEL_IO_CTRL. CHx_input_filter_enable(Optional).
6. Enable the channel by writing '1' to PWM_PWMx_CTRL.pwm_en bit to start the channel.
7. When an interrupt is asserted, refer to INTSTS register to know the raw interrupt status. If the corresponding polarity flag is set, turn to PWM_PWMx_PERIOD_HPC register to know

Rockchip Confidential

the effective high cycles of input waveforms, otherwise turn to PWM_PWMx_DUTY_LPC register to know the effective low cycles.
8. Write '0' to PWM_PWMx_CTRL.pwm_en to disable the channel.

### 18.6.2 PWM Capture DMA Mode Standard Usage Flow

1. Set PWM_PWMx_CTRL.pwm_en to '0' to disable the PWM channel.
2. Choose the prescale factor and the scale factor for clk_pwm by programming PWM_PWMx_CTRL.prescale and PWM_PWMx_CTRL.scale, and select the clock needed by setting PWM_PWMx_CTRL.clk_sel and PWM_PWMx_CTRL.clk_src_sel.
3. Configure the channel 3 to work in the capture mode.
4. Configure the PWM_FIFO_CTRL.dma_mode_en and PWM_FIFO_CTRL.fifo_mode_sel to enable the DMA mode. Configure PWM_FIFO_CTRL.almost_full_watermark at appropriate value.
5. Configure DMAC_BUS to transfer data from PWM to DDR.
6. Set PWM_CHANNEL_IO_CTRL.filter_number, then Enable the PWM_CHANNEL_IO_CTRL. CHx_input_filter_enable(Optional).
7. Enable the channel by writing '1' to PWM_PWMx_CTRL.pwm_en bit to start the channel.
8. When a dma_req is asserted, DMAC_BUS transfer the data of effective high cycles and low cycles of input waveforms to DDR.
9. Write '0' to PWM_PWMx_CTRL.pwm_en to disable the channel.

### 18.6.3 PWM Power key Capture Mode Standard Usage Flow

1. Set PWM_PWM3_CTRL.pwm_en to '0' to disable the PWM channel.
2. Choose the prescale factor and the scale factor for clk_pwm by programming PWM_PWM3_CTRL.prescale and PWM_PWM3_CTRL.scale, and select the clock needed by setting PWM_PWM3_CTRL.clk_sel. The clock should be 1 MHz after division.
3. Configure the channel to work in the capture mode.
4. Enable the PWM_INT_EN.CH3_int_pwr to enable the interrupt generation.
5. Set the PWM_PWRMATCH_VALUE0~9 registers for the 10 power key match value.
6. Set max_cnt and min_cnt of follow register: PWM_PWRMATCH_LPRE, PWM_PWRMATCH_HPRE, PWM_PWRMATCH_LD, PWM_PWRMATCH_HD_ZERO, PWM_PWRMATCH_HD_ONE. It doesn't need to set these registers when the default value can meet the requirement.
7.Set PWM_PWRMATCH_CTRL.CH3_pwrkey_polarity for the polarity of power key signal, the default value is 0. Enable the PWM_PWRMATCH_CTRL.CH3_pwrkey_enable.
8. Set PWM_CHANNEL_IO_CTRL.filter_number, then Enable the PWM_CHANNEL_IO_CTRL. CH3_input_filter_enable(Optional).
9. Enable the channel by writing '1' to PWM_PWM3_CTRL.pwm_en bit to start the channel.
10. Poll INTSTS. CH3_pwr_IntSts ==1, and refer to PWM_PWM3_PWRCAPTURE_VALUE to know the power key capture value.
11. Write '0' to PWM_PWM3_CTRL.pwm_en to disable the channel.

### 18.6.4 PWM One-shot Mode/Continuous Standard Usage Flow

1. Set PWM_PWMx_CTRL.pwm_en to '0' to disable the PWM channel.
2. Choose the prescale factor and the scale factor for pclk by programming PWM_PWMx_CTRL.prescale and PWM_PWMx_CTRL.scale, and select the clock needed by setting PWM_PWMx_CTRL.clk_sel.
3. Choose the output mode by setting PWM_PWMx_CTRL.output_mode, and set the duty polarity and inactive polarity by programming PWM_PWMx_CTRL.duty_pol and PWM_PWMx_CTRL.inactive_pol.
4. Set the PWM_PWMx_CTRL.rpt if the channel is desired to work in the one-shot mode.
5. Configure the channel to work in the one-shot mode or the continuous mode.
6. Enable the PWM_INT_EN.chx_int_en to enable the interrupt generation if the channel is desired to work in the one-shot mode.
7. If the channel is working in the one-shot mode, an interrupt is asserted after the end of operation, and the PWM_PWMx_CTRL.pwm_en is automatically cleared. Whatever mode the channel is working in, write '0' to PWM_PWMx_CTRL.pwm_en bit to disable the PWM channel.

Rockchip Confidential

### 18.6.5 Low-power Usage Flow

The default value of PWM_PWMx_CTRL.force_clk_en is '0' which make the channel enter the low-power mode. In low-power mode, When the PWM channel is inactive, the clk_pwm to the clock prescale module is gated in order to reduce the power consumption. User can set PWM_PWMx_CTRL.force_clk_en to '1' which will make the channel quit the low-power mode. After the setting, the clk_pwm to the clock prescale module is always enable.

### 18.6.6 Other notes

When the channel is active to produce waveforms, it is free to program the PWM_PWMx_PERIOD_HPC and PWM_PWMx_DUTY_LPC register. User can use PWM_PWMx_CTRL.conlock to take period and duty effect at the same time. The usage flow is as follow:

1. Set PWM_PWMx_CTRL.conlock to '1'.
2. Set PWM_PWMx_PERIOD_HPC and PWM_PWMx_DUTY_LPC.
3. Set PWM_PWMx_CTRL.conlock to '0', others bits in PWM_PWMx_CTRL should be appropriate.

After above configuration, the change will not take effect immediately until the current period ends.

An active channel can be changed to another operation mode without disable the PWM channel. However, during the transition of the operation mode there may be some irregular output waveforms. So does changing the clock division factor when the channel is active.

Rockchip Confidential

# Chapter 19 UART

## 19.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

UART Controller supports the following features:

- Support 10 independent UART controller: UART0-UART9
- All contain two 64 Bytes FIFOs for data receive and transmit
- All support auto flow-control
- Support bit rates 115.2Kbps, 460.8Kbps, 921.6Kbps, 1.5Mbps, 3Mbps, 4Mbps
- Support programmable baud rates, even with non-integer clock divider
- Standard asynchronous communication bits (start, stop and parity)
- Support interrupt-based or DMA-based mode
- Support 5-8 bits width transfer

## 19.2 Block Diagram

This section provides a description about the functions and behavior under various conditions. The UART Controller comprises with:

- AMBA APB interface
- FIFO controllers
- Register block
- Modem synchronization block and baud clock generation block
- Serial receiver and serial transmitter

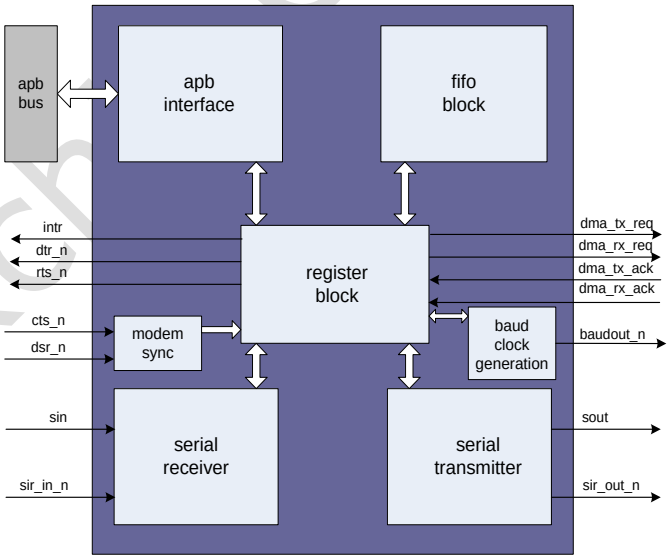



Fig. 19-1 UART Architecture

**APB INTERFACE**

The host processor accesses data, control, and status information on the UART through the APB interface. The UART supports APB data bus widths of 8, 16, and 32 bits.

**Register block**

Be responsible for the main UART functionality including control, status and interrupt generation.

Rockchip Confidential

**Modem Synchronization block**
Synchronizes the modem input signal.

**FIFO block**
Be responsible for FIFO control and storage (when using internal RAM) or signaling to control external RAM (when used).

**Baud Clock Generator**
Generates the transmitter and receiver baud clock along with the output reference clock signal (baudout_n).

**Serial Transmitter**
Converts the parallel data, written to the UART, into serial form and adds all additional bits, as specified by the control register, for transmission.

**Serial Receiver**
Converts the serial data character (as specified by the control register) received to parallel form. Parity error detection, framing error detection and line break detection is carried out in this block.

## 19.3 Function Description

**UART (RS232) Serial Protocol**
Because the serial communication is asynchronous, additional bits (start and stop) are added to the serial data to indicate the beginning and end. An additional parity bit may be added to the serial character. This bit appears after the last data bit and before the stop bit(s) in the character structure to perform simple error checking on the received data, as shown in Figure.

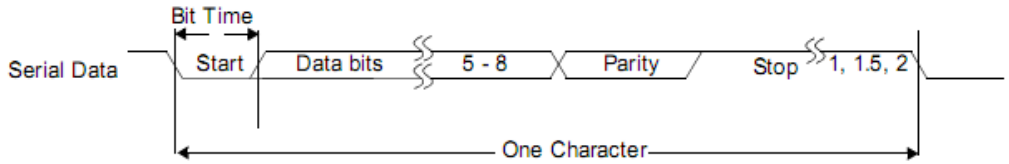



Fig. 19-2 UART Serial protocol

**Baud Clock**
The baud rate is controlled by the serial clock (sclk or pclk in a single clock implementation) and the Divisor Latch Register (DLH and DLL). As the exact number of baud clocks that each bit was transmitted for is known, calculating the mid-point for sampling is not difficult, that is every 16 baud clocks after the mid-point sample of the start bit.

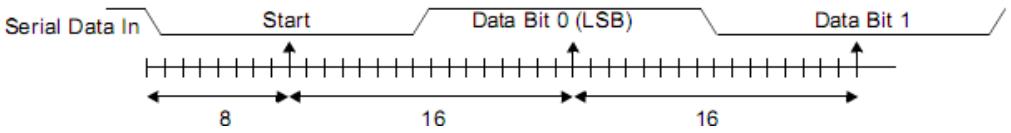



Fig. 19-3 UART baud rate

**FIFO Support**
**1. NONE FIFO MODE**
If FIFO support is not selected, then no FIFOs are implemented and only a single receive data byte and transmit data byte can be stored at a time in the RBR and THR.

**2. FIFO MODE**
The FIFO depth of is 64bytes. The FIFO mode of all the UART is enabled by register FCR[0].

**Interrupts**

Rockchip Confidential

The following interrupt types can be enabled with the IER register.

- Receiver Error
- Receiver Data Available
- Character Timeout (in FIFO mode only)
- Transmitter Holding Register Empty at/below threshold (in Programmable THRE Interrupt mode)
- Modem Status

**DMA Support**

The UART supports DMA signaling with the use of two output signals (dma_tx_req_n and dma_rx_req_n) to indicate when data is ready to be read or when the transmit FIFO is empty.

The dma_tx_req_n signal is asserted under the following conditions:

- When the Transmitter Holding Register is empty in non-FIFO mode.
- When the transmitter FIFO is empty in FIFO mode with Programmable THRE interrupt mode disabled.
- When the transmitter FIFO is at, or below the programmed threshold with Programmable THRE interrupt mode enabled.

The dma_rx_req_n signal is asserted under the following conditions:

- When there is a single character available in the Receive Buffer Register in non-FIFO mode.
- When the Receiver FIFO is at or above the programmed trigger level in FIFO mode.

**Auto Flow Control**

The UART can be configured to have a 16750-compatible Auto RTS and Auto CTS serial data flow control mode available. If FIFOs are not implemented, then this mode cannot be selected. When Auto Flow Control mode has been selected, it can be enabled with the Modem Control Register (MCR[5]). Following figure shows a block diagram of the Auto Flow Control functionality.

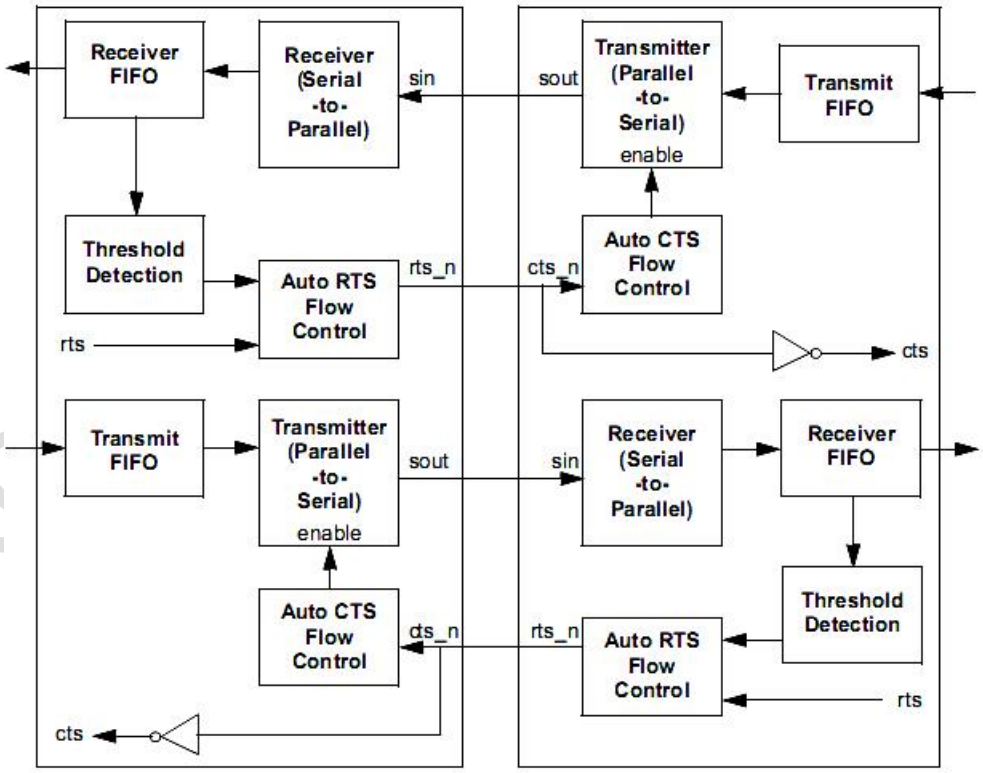



Fig. 19-4 UART Auto flow control block diagram

Auto RTS – Becomes active when the following occurs:

- Auto Flow Control is selected during configuration

Rockchip Confidential

- FIFOs are implemented
- RTS (MCR[1] bit and MCR[5]bit are both set)
- FIFOs are enabled (FCR[0]) bit is set)
- SIR mode is disabled (MCR[6] bit is not set)

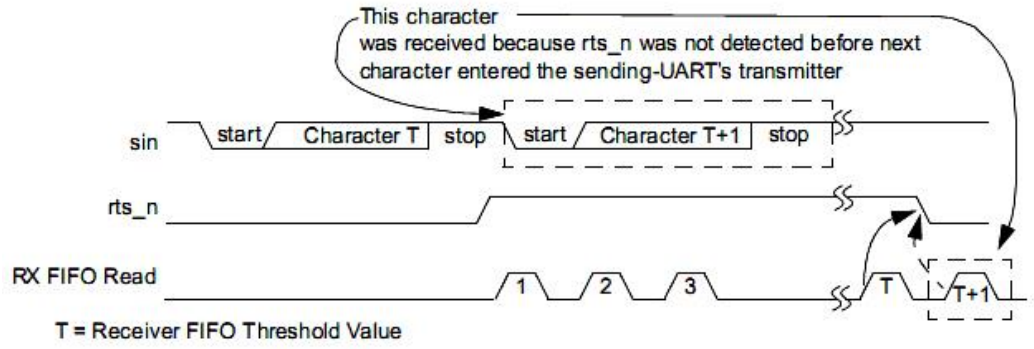



Fig. 19-5 UART AUTO RTS TIMING

Auto CTS – becomes active when the following occurs:

- Auto Flow Control is selected during configuration
- FIFOs are implemented
- AFCE (MCR[5] bit is set)
- FIFOs are enabled through FIFO Control Register FCR[0] bit
- SIR mode is disabled (MCR[6] bit is not set)

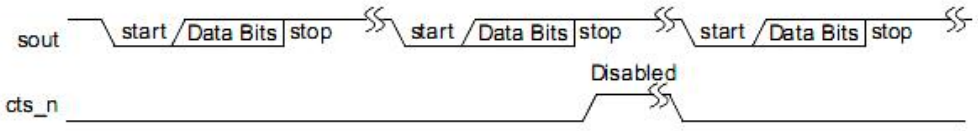



Fig. 19-6 UART AUTO CTS TIMING

# 19.4 Register Description

## 19.4.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| UART_RBR | 0x0000 | W | 0x00000000 | Receive Buffer Register |
| UART_DLL | 0x0000 | W | 0x00000000 | Divisor Latch Low |
| UART_THR | 0x0000 | W | 0x00000000 | Transmit Buffer Register |
| UART_DLH | 0x0004 | W | 0x00000000 | Divisor Latch High |
| UART_IER | 0x0004 | W | 0x00000000 | Interrupt Enable Register |
| UART_FCR | 0x0008 | W | 0x00000000 | FIFO Enable |
| UART_IIR | 0x0008 | W | 0x00000001 | Interrupt Identity Register |
| UART_LCR | 0x000C | W | 0x00000000 | Line Control Register |
| UART_MCR | 0x0010 | W | 0x00000000 | Modem Control Register |
| UART_LSR | 0x0014 | W | 0x00000060 | Line Status Register |
| UART_MSR | 0x0018 | W | 0x00000000 | Modem Status Register |
| UART_SCR | 0x001C | W | 0x00000000 | Scratchpad Register |
| UART_SRBR | 0x0030 | W | 0x00000000 | Shadow Receive Buffer Register |
| UART_STHR | 0x0030 | W | 0x00000000 | Shadow Transmit Holding Register |
| UART_FAR | 0x0070 | W | 0x00000000 | FIFO Access Register |
| UART_TFR | 0x0074 | W | 0x00000000 | Transmit FIFO Read |
| UART_RFW | 0x0078 | W | 0x00000000 | Receive FIFO write |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| UART_USR | 0x007C | W | 0x00000006 | UART Status Register |
| UART_TFL | 0x0080 | W | 0x00000000 | Transmit FIFO level |
| UART_RFL | 0x0084 | W | 0x00000000 | Receive FIFO level |
| UART_SRR | 0x0088 | W | 0x00000000 | Software Reset Register |
| UART_SRTS | 0x008C | W | 0x00000000 | Shadow Request to Send |
| UART_SBCR | 0x0090 | W | 0x00000000 | Shadow Break Control Register |
| UART_SDMAM | 0x0094 | W | 0x00000000 | Shadow DMA Mode |
| UART_SFE | 0x0098 | W | 0x00000000 | Shadow FIFO enable |
| UART_SRT | 0x009C | W | 0x00000000 | Shadow RCVR Trigger |
| UART_STET | 0x00A0 | W | 0x00000000 | Shadow TX Empty Trigger |
| UART_HTX | 0x00A4 | W | 0x00000000 | Halt TX |
| UART_DMASA | 0x00A8 | W | 0x00000000 | DMA Software Acknowledge |
| UART_CPR | 0x00F4 | W | 0x00043FF2 | Component Parameter Register |
| UART_UCV | 0x00F8 | W | 0x3430322A | UART Component Version |
| UART_CTR | 0x00FC | W | 0x44570110 | Component Type Register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 19.4.2 Detail Registers Description

**UART_RBR**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | data_input<br>Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an over-run error.<br>If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an over-run error occurs. |

**UART_DLL**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:0 | RW | 0x00 | baud_rate_divisor_l<br>Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (pclk if one clock design, sclk if two clock design (CLOCK_MODE == Enabled)) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor).<br>Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data. |

**UART_THR**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | WO | 0x00 | data_output<br>Data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in non-FIFO mode or FIFOs are disabled (FCR[0] = 0) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten.<br>If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, 64 characters of data may be written to the THR before the FIFO is full. Any attempt to write data when the FIFO is full results in the write data being lost. |

**UART_DLH**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | baud_rate_divisor_h<br>Upper 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (pclk if one clock design, sclk if two clock design CLOCK_MODE == Enabled)) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor).<br>Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data. |

**UART_IER**

Address: Operational Base + offset (0x0004)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RW | 0x0 | prog_thre_int_en<br>Programmable THRE Interrupt Mode Enable that can be written to only when THRE_MODE_USER == Enabled, always readable. This is used to enable/disable the generation of THRE Interrupt.<br>1'b0: Disabled<br>1'b1: Enabled |
| 6:4 | RO | 0x0 | reserved |
| 3 | RW | 0x0 | modem_status_int_en<br>Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt.<br>1'b0: Disabled<br>1'b1: Enabled |
| 2 | RW | 0x0 | receive_line_status_int_en<br>Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority<br>interrupt.<br>1'b0: Disabled<br>1'b1: Enabled |
| 1 | RW | 0x0 | trans_hold_empty_int_en<br>Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt.<br>1'b0: Disabled<br>1'b1: Enabled |
| 0 | RW | 0x0 | receive_data_available_int_en<br>Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts.<br>1'b0: Disabled<br>1'b1: Enabled |

**UART_FCR**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:6 | WO | 0x0 | rcvr_trigger<br>At which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. For details on DMA support, refer to "DMA Support". The following trigger levels are supported:<br>2'b00: 1 character in the FIFO<br>2'b01: FIFO 1/4 full<br>2'b10: FIFO 1/2 full<br>2'b11: FIFO 2 less than full |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5:4 | WO | 0x0 | tx_empty_trigger<br>TX Empty Trigger. Writes have no effect when THRE_MODE_USER == Disabled. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. For details on DMA support, refer to "DMA Support" . The following trigger levels are supported:<br>2'b00: FIFO empty<br>2'b01: 2 characters in the FIFO<br>2'b10: FIFO 1/4 full<br>2'b11: FIFO 1/2 full |
| 3 | WO | 0x0 | dma_mode<br>DMA Mode. This determines the DMA signaling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == No). For details on DMA support, refer to DMA Support.<br>1'b0: Mode 0<br>1'b1: Mode 1 |
| 2 | WO | 0x0 | xmit_fifo_reset<br>XMIT FIFO Reset. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. |
| 1 | WO | 0x0 | rcvr_fifo_reset<br>RCVR FIFO Reset. This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. |
| 0 | WO | 0x0 | fifo_en<br>FIFO Enable. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset. |

**UART_IIR**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:6 | RO | 0x0 | fifos_en<br>FIFOs Enabled. This is used to indicate whether the FIFOs are enabled or disabled.<br>2'b00: Disabled<br>2'b11: Enabled |
| 5:4 | RO | 0x0 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RO | 0x1 | int_id<br>Interrupt ID. This indicates the highest priority pending interrupt which can be one of the following types:<br>4'b0000: Modem status<br>4'b0001: No interrupt pending<br>4'b0010: THR empty<br>4'b0100: Received data available<br>4'b0110: Receiver line status<br>4'b0111: Busy detect<br>4'b1100: Character timeout<br>The interrupt priorities are split into four levels that are detailed in Table X.<br>Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt. |

**UART_LCR**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RW | 0x0 | div_lat_access<br>Divisor Latch Access Bit. Writable only when UART is not busy (USR[0] is zero), always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. |
| 6 | RW | 0x0 | break_ctrl<br>Break Control Bit. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low. |
| 5 | RW | 0x0 | stick_parity<br>If UART_16550_COMPATIBLE = NO, then writable only when UART is not busy (USR[0] is 0); otherwise always writable and always readable. This bit is used to force parity value. When PEN, EPS and Stick Parity are set to 1, the parity bit is transmitted and checked as logic 0. If PEN and Stick Parity are set to 1 and EPS is a logic 0, then parity bit is transmitted and checked as a logic 1. If this bit is set to 0, Stick Parity is disabled. |
| 4 | RW | 0x0 | even_parity_sel<br>Even Parity Select. Writable only when UART is not busy (USR[0] is zero), always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | parity_en<br>Parity Enable. Writable only when UART is not busy (USR[0] is zero), always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively.<br>1'b0: Parity disabled<br>1'b1: Parity enabled |
| 2 | RW | 0x0 | stop_bits_num<br>Number of stop bits. Writable only when UART is not busy (USR[0] is zero), always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit.<br>1'b0: 1 stop bit<br>1'b1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit. |
| 1:0 | RW | 0x0 | data_length_sel<br>Data Length Select. Writable only when UART is not busy (USR[0] is zero), always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows:<br>2'b00: 5 bits<br>2'b01: 6 bits<br>2'b10: 7 bits<br>2'b11: 8 bits |

**UART_MCR**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6 | RW | 0x0 | reserved |
| 5 | RW | 0x0 | auto_flow_ctrl_en<br>Auto Flow Control Enable. Writable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled as described in "Auto Flow Control".<br>1'b0: Auto Flow Control Mode disabled<br>1'b1: Auto Flow Control Mode enabled |
| 4 | RW | 0x0 | loopback<br>LoopBack Bit. This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | out2<br>OUT2. This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n, that is:<br>1'b0: Out2_n de-asserted (logic 1)<br>1'b1: Out2_n asserted (logic 0)<br>Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input. |
| 2 | RW | 0x0 | out1<br>OUT1. This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n, that is:<br>1'b0: Out1_n de-asserted (logic 1)<br>1'b1: Out1_n asserted (logic 0)<br>Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input. |
| 1 | RW | 0x0 | req_to_send<br>Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input. |
| 0 | RW | 0x0 | data_terminal_ready<br>Data Terminal Ready. This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n, that is:<br>1'b0: dtr_n de-asserted (logic 1)<br>1'b1: dtr_n asserted (logic 0)<br>The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive |

**UART_LSR**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RO | 0x0 | receiver_fifo_error<br>Receiver FIFO Error bit. This bit is only relevant when FIFO_MODE != NONE AND FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO.<br>1'b0: No error in RX FIFO<br>1'b1: Error in RX FIFO<br>This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO. |
| 6 | RO | 0x1 | trans_empty<br>Transmitter Empty bit. If in FIFO mode (FIFO_MODE != NONE) and FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in non-FIFO mode or FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty. |
| 5 | RO | 0x1 | trans_hold_reg_empty<br>Transmit Holding Register Empty bit. If THRE_MODE_USER == Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty.<br>This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting. |
| 4 | RO | 0x0 | break_int<br>Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RO | 0x0 | framing_error<br>Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to re-synchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]).<br>1'b0: No framing error<br>1'b1: Framing error<br>Reading the LSR clears the FE bit. |
| 2 | RO | 0x0 | parity_error<br>Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]).<br>1'b0: No parity error<br>1'b1: Parity error<br>Reading the LSR clears the PE bit. |
| 1 | RO | 0x0 | overrun_error<br>Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost.<br>1'b0: No overrun error<br>1'b1: Overrun error<br>Reading the LSR clears the OE bit. |
| 0 | RO | 0x0 | data_ready<br>Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO.<br>1'b0: No data ready<br>1'b1: Data ready<br>This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode. |

**UART_MSR**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RO | 0x0 | data_carrior_detect<br>Data Carrier Detect. This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set.<br>1'b0: dcd_n input is de-asserted (logic 1)<br>1'b1: dcd_n input is asserted (logic 0)<br>In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2). |
| 6 | RO | 0x0 | ring_indicator<br>Ring Indicator. This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set.<br>1'b0: ri_n input is de-asserted (logic 1)<br>1'b1: ri_n input is asserted (logic 0)<br>In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1). |
| 5 | RO | 0x0 | data_set_ready<br>Data Set Ready. This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the UART.<br>1'b0: dsr_n input is de-asserted (logic 1)<br>1'b1: dsr_n input is asserted (logic 0)<br>In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR). |
| 4 | RO | 0x0 | clear_to_send<br>Clear to Send. This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the UART.<br>1'b0: cts_n input is de-asserted (logic 1)<br>1'b1: cts_n input is asserted (logic 0)<br>In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS). |
| 3 | RO | 0x0 | delta_data_carrier_detect<br>Delta Data Carrier Detect. This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read.<br>1'b0: No change on dcd_n since last read of MSR<br>1'b1: Change on dcd_n since last read of MSR<br>Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] = 1), DDCD reflects changes on MCR[3] (Out2).<br>Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RO | 0x0 | trailing_edge_ring_indicator<br>Trailing Edge of Ring Indicator. This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read.<br>1'b0: No change on ri_n since last read of MSR<br>1'b1: Change on ri_n since last read of MSR<br>Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] = 1), TERI reflects when MCR[2] (Out1) has changed state from a high to a low. |
| 1 | RO | 0x0 | delta_data_set_ready<br>Delta Data Set Ready. This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read.<br>1'b0: No change on dsr_n since last read of MSR<br>1'b1: Change on dsr_n since last read of MSR<br>Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR).<br>Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted. |
| 0 | RO | 0x0 | delta_clear_to_send<br>Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read.<br>1'b0: No change on ctsdsr_n since last read of MSR<br>1'b1: Change on ctsdsr_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted. |

**UART_SCR**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | temp_store_space<br>Scratchpad register. This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART. |

**UART_SRBR**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:0 | RO | 0x00 | shadow_rbr<br>This is a shadow register for the RBR and has been allocated sixteen 32-bit locations (0x30-0x6c) so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. |

**UART_STHR**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | WO | 0x00 | shadow_thr<br>This is a shadow register for the THR and has been allocated sixteen 32-bit locations(0x30-0x6c) so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in non-FIFO mode or FIFOs are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If in FIFO mode and FIFOs are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost. |

**UART_FAR**

Address: Operational Base + offset (0x0070)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | fifo_access_test_en<br>Writes have no effect when FIFO_ACCESS == No, always readable. This register is use to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFOs are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master.<br>1'b0: FIFO access mode disabled<br>1'b1: FIFO access mode enabled<br>Note that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFOs are treated as empty. |

**UART_TFR**

Address: Operational Base + offset (0x0074)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | trans_fifo_read<br>Transmit FIFO Read. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO.<br>When FIFOs are not implemented or not enabled, reading this register gives the data in the THR. |

**UART_RFW**

Address: Operational Base + offset (0x0078)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9 | WO | 0x0 | receive_fifo_framing_error<br>Receive FIFO Framing Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write framing error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write framing error detection information to the RBR. |
| 8 | WO | 0x0 | receive_fifo_parity_error<br>Receive FIFO Parity Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write parity error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write parity error detection information to the RBR. |
| 7:0 | WO | 0x00 | receive_fifo_write<br>Receive FIFO Write Data. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs are not implemented or not enabled, the data that is written to the RFWD is pushed into the RBR. |

Rockchip Confidential

**UART_USR**

Address: Operational Base + offset (0x007C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4 | RO | 0x0 | receive_fifo_full<br>Receive FIFO Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full.<br>1'b0: Receive FIFO not full<br>1'b1: Receive FIFO full<br>This bit is cleared when the RX FIFO is no longer full. |
| 3 | RO | 0x0 | receive_fifo_not_empty<br>Receive FIFO Not Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries.<br>1'b0: Receive FIFO is empty<br>1'b1: Receive FIFO is not empty<br>This bit is cleared when the RX FIFO is empty. |
| 2 | RO | 0x1 | trasn_fifo_empty<br>Transmit FIFO Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty.<br>1'b0: Transmit FIFO is not empty<br>1'b1: Transmit FIFO is empty<br>This bit is cleared when the TX FIFO is no longer empty. |
| 1 | RO | 0x1 | trans_fifo_not_full<br>Transmit FIFO Not Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO in not full.<br>1'b0: Transmit FIFO is full<br>1'b1: Transmit FIFO is not full<br>This bit is cleared when the TX FIFO is full. |
| 0 | RO | 0x0 | uart_busy<br>UART Busy. This is indicates that a serial transfer is in progress, when cleared indicates that the UART is idle or inactive.<br>1'b0: UART is idle or inactive<br>1'b1: UART is busy (actively transferring data)<br>Note that it is possible for the UART Busy bit to be cleared even though a new character may have been sent from another device. That is, if the UART has no data in THR and RBR and there is no transmission in progress and a start bit of a new character has just reached the UART. This is due to the fact that a valid start is not seen until the middle of the bit period and this duration is dependent on the baud divisor that has been programmed. If a second system clock has been implemented (CLOCK_MODE == Enabled), the assertion of this bit is also delayed by several cycles of the slower clock. |

**UART_TFL**

Address: Operational Base + offset (0x0080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5:0 | RO | 0x00 | trans_fifo_level<br>Transmit FIFO Level. This is indicates the number of data entries in the transmit FIFO. |

**UART_RFL**

Address: Operational Base + offset (0x0084)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5:0 | RO | 0x00 | receive_fifo_level<br>Receive FIFO Level. This is indicates the number of data entries in the receive FIFO. |

**UART_SRR**

Address: Operational Base + offset (0x0088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2 | WO | 0x0 | xmit_fifo_reset<br>XMIT FIFO Reset. This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. |
| 1 | WO | 0x0 | rcvr_fifo_reset<br>RCVR FIFO Reset. This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES).<br>Note that this bit is 'self-clearing'. It is not necessary to clear this bit. |
| 0 | WO | 0x0 | uart_reset<br>UART Reset. This asynchronously resets the UART and synchronously removes the reset assertion. For a two clock implementation both pclk and sclk domains are reset. |

**UART_SRTS**

Address: Operational Base + offset (0x008C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | shadow_req_to_send<br>Shadow Request to Send. This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read-modify-write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] = 0), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] = 1) and FIFOs enable (FCR[0] = 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold).<br>Note that in Loopback mode (MCR[4] = 1), the rts_n output is held inactive-high while the value of this location is internally looped back to an input. |

Rockchip Confidential

**UART_SBCR**

Address: Operational Base + offset (0x0090)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | shadow_break_ctrl<br>Shadow Break Control Bit. This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] = 1) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver. |

**UART_SDMAM**

Address: Operational Base + offset (0x0094)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | shadow_dma_mode<br>Shadow DMA Mode. This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. This determines the DMA signaling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == NO).<br>1'b0: Mode 0<br>1'b1: Mode 1 |

**UART_SFE**

Address: Operational Base + offset (0x0098)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | shadow_fifo_en<br>Shadow FIFO Enable. This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset. |

**UART_SRT**

Address: Operational Base + offset (0x009C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1:0 | RW | 0x0 | shadow_rcvr_trigger<br>Shadow RCVR Trigger. This is a shadow register for the RCVR trigger bits (FCR[7:6]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the RCVR trigger bit gets updated. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. It also determines when the dma_rx_req_n signal is asserted when DMA Mode (FCR[3]) = 1. The following trigger levels are supported:<br>2'b00: 1 character in the FIFO<br>2'b01: FIFO 1/4 full<br>2'b10: FIFO 1/2 full<br>2'b11: FIFO 2 less than full |

**UART_STET**

Address: Operational Base + offset (0x00A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1:0 | RW | 0x0 | shadow_tx_empty_trigger<br>Shadow TX Empty Trigger. This is a shadow register for the TX empty trigger bits (FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported:<br>2'b00: FIFO empty<br>2'b01: 2 characters in the FIFO<br>2'b10: FIFO 1/4 full<br>2'b11: FIFO 1/2 full |

**UART_HTX**

Address: Operational Base + offset (0x00A4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | halt_tx_en<br>This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled.<br>1'b0: Halt TX disabled<br>1'b1: Halt TX enabled<br>Note, if FIFOs are implemented and not enabled, the setting of the halt TX register has no effect on operation. |

**UART_DMASA**

Address: Operational Base + offset (0x00A8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | WO | 0x0 | dma_software_ack<br>This register is use to perform a DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the UART should clear its request. This causes the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing'. It is not necessary to clear this bit. |

**UART_CPR**

Address: Operational Base + offset (0x00F4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23:16 | RO | 0x04 | fifo_mode<br>8'h4 means FIFO mode is 64. |
| 15:14 | RO | 0x0 | reserved |
| 13 | RO | 0x1 | dma_extra<br>1'b1 means DMA_EXTRA enabled. |
| 12 | RO | 0x1 | uart_add_encoded_params<br>1'b1 means UART_ADD_ENCODED_PARAMS enabled. |
| 11 | RO | 0x1 | shadow<br>1'b1 means SHADOW mode enabled. |
| 10 | RO | 0x1 | fifo_stat<br>1'b1 means FIFO_STAT enabled. |
| 9 | RO | 0x1 | fifo_access<br>1'b1 means FIFO ACCESS enabled. |
| 8 | RO | 0x1 | new_feat<br>1'b1 means Additional features enabled. |
| 7 | RO | 0x1 | sir_lp_mode<br>1'b1 means SIR_LP mode enabled. |
| 6 | RO | 0x1 | sir_mode<br>1'b1 means SIR mode enabled. |
| 5 | RO | 0x1 | thre_mode<br>1'b1 means THRE mode enabled. |
| 4 | RO | 0x1 | afce_mode<br>1'b1 means AFCE mode enabled. |
| 3:2 | RO | 0x0 | reserved |
| 1:0 | RO | 0x2 | apb_data_width<br>2'b10 means APB data width is 32bit. |

**UART_UCV**

Address: Operational Base + offset (0x00F8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x3430322a | ver<br>ASCII value for each number in the version. |

**UART_CTR**

Address: Operational Base + offset (0x00FC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x44570110 | peripheral_id<br>This register contains the peripherals identification code. |

Rockchip Confidencial

## 19.5 Interface Description

Table 19-1 UART0 Interface Description

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| **IOMUX0** | | | |
| uart_rx | I | PDM0_CLK1_M1/PWM2_M0/UART0_RX_M0/I2C4_SDA_M2/DP0_HPDIN_M1/PCIE30X1_0_WAKEN_M0/GPIO0_C4_d | PMU2_IOC_GPIO0C_IOMUX_SEL_H[3:0] = 4'h4 |
| uart_tx | O | I2S1_SDI0_M1/GPU_AVS/UART0_TX_M0/I2C4_SCL_M2/DP1_HPDIN_M1/PWM4_M0/PCIE30X1_0_PERSTN_M0/GPIO0_C5_u | PMU2_IOC_GPIO0C_IOMUX_SEL_H[7:4] = 4'h4 |
| uart_cts_n | I | I2S1_SDO0_M1/CPU_BIG0_AVS/I2C0_SCL_M2/UART0_CTSN/UART1_TX_M2/HDMI_RX_SDA_M0/SPI0_CS0_M0/PCIE30X2_CLKREQN_M0/HDMI_TX0_CEC_M1/GPIO0_D1_u | PMU2_IOC_GPIO0D_IOMUX_SEL_L[7:4] = 4'h4 |
| uart_rts_n | O | I2S1_SDI1_M1/NPU_AVS/UART0_RTSN/PWM5_M1/SPI0_CLK_M0/PCIE30X4_CLKREQN_M0/SATA_CP_POD/GPIO0_C6_u | PMU2_IOC_GPIO0C_IOMUX_SEL_H[11:8] = 4'h4 |
| **IOMUX1** | | | |
| uart_rx | I | SPI2_CS1_M2/I2C1_SCL_M1/UART0_RX_M1/GPIO0_B0_z | PMU1_IOC_GPIO0B_IOMUX_SEL_L[3:0] = 4'h4 |
| uart_tx | O | SPI2_CS0_M2/I2C1_SDA_M1/PWM5_M0/UART0_TX_M1/GPIO0_B1_z | PMU1_IOC_GPIO0B_IOMUX_SEL_L[7:4] = 4'h4 |
| **IOMUX2** | | | |
| uart_rx | I | CIF_D4/BT1120_D4/PCIE30X1_0_WAKEN_M1/I2C3_SCL_M2/UART0_RX_M2/SPI2_MISO_M1/GPIO4_A4_d | BUS_IOC_GPIO4A_IOMUX_SEL_H[3:0] = 4'ha |
| uart_tx | O | CIF_D3/BT1120_D3/PCIE30X1_0_CLKREQN_M1/UART0_TX_M2/GPIO4_A3_d | BUS_IOC_GPIO4A_IOMUX_SEL_L[15:12] = 4'ha |

Table 19-2 UART1 Interface Description

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| **IOMUX0** | | | |
| uart_rx | I | GMAC0_TXD0/I2S2_MCLK_M0/I2C5_SCL_M4/UART1_RX_M0/GPIO2_B6_d | BUS_IOC_GPIO2B_IOMUX_SEL_H[11:8] = 4'ha |
| uart_tx | O | GMAC0_TXD1/I2S2_SCLK_M0/I2C5_SDA_M4/UART1_TX_M0/GPIO2_B7_d | BUS_IOC_GPIO2B_IOMUX_SEL_H[15:12] = 4'ha |
| uart_cts_n | I | GMAC0_RXD0/I2C2_SCL_M1/UART1_CTSN_M0/SPI1_MISO_M0/GPIO2_C1_d | BUS_IOC_GPIO2C_IOMUX_SEL_L[7:4] = 4'ha |
| uart_rts_n | O | GMAC0_TXEN/I2S2_LRCK_M0/I2C2_SDA_M1/UART1_RTSN_M0/SPI1_CLK_M0/GPIO2_C0_d | BUS_IOC_GPIO2C_IOMUX_SEL_L[3:0] = 4'ha |
| **IOMUX1** | | | |

Rockchip Confidential

| | | | |
|---|---|---|---|
| uart_rx | I | MIPI_CAMERA2_CLK_M0/SPDIF1_TX_M0/PCIE30X2_PERSTN_M3/HDMI_RX_CEC_M2/SATA2_ACT_LED_M1/I2C5_SDA_M3/UART1_RX_M1/PWM13_M2/GPIO1_B7_u | BUS_IOC_GPIO1B_IOMUX_SEL_H[15:12] = 4'ha |
| uart_tx | O | MIPI_CAMERA1_CLK_M0/SPDIF0_TX_M0/PCIE30X2_WAKEN_M3/HDMI_RX_HPDOUT_M2/I2C5_SCL_M3/UART1_TX_M1/GPIO1_B6_d | BUS_IOC_GPIO1B_IOMUX_SEL_H[11:8] = 4'ha |
| uart_cts_n | I | MIPI_CAMERA4_CLK_M0/PCIE30X2_CLKREQN_M3/HDMI_RX_SDA_M2/I2C8_SDA_M2/UART1_CTSN_M1/PWM15_IR_M3/GPIO1_D7_u | BUS_IOC_GPIO1D_IOMUX_SEL_H[15:12] = 4'ha |
| uart_rts_n | O | MIPI_CAMERA3_CLK_M0/HDMI_RX_SCL_M2/I2C8_SCL_M2/UART1_RTSN_M1/PWM14_M2/GPIO1_D6_u | BUS_IOC_GPIO1D_IOMUX_SEL_H[11:8] = 4'ha |
| **IOMUX2** | | | |
| uart_rx | I | I2S1_SDO1_M1/I2C0_SDA_M2/UART1_RX_M2/HDMI_RX_SCL_M0/SPI3_MOSI_M2/PCIE30X2_WAKEN_M0/HDMI_TX1_CEC_M1/GPIO0_D2_u | BUS_IOC_GPIO0D_IOMUX_SEL_L[11:8] = 4'ha<br>PMU2_IOC_GPIO0D_IOMUX_SEL_L[11:8] = 4'h8 |
| uart_tx | O | I2S1_SDO0_M1/CPU_BIG0_AVS/I2C0_SCL_M2/UART0_CTSN/UART1_TX_M2/HDMI_RX_SDA_M0/SPI0_CS0_M0/PCIE30X2_CLKREQN_M0/HDMI_TX0_CEC_M1/GPIO0_D1_u | BUS_IOC_GPIO0D_IOMUX_SEL_L[7:4] = 4'ha<br>PMU2_IOC_GPIO0D_IOMUX_SEL_L[7:4] = 4'h8 |
| uart_cts_n | I | I2S1_SDI3_M1/PDM0_SDI1_M1/I2C6_SCL_M0/UART1_CTSN_M2/PWM7_IR_M0/SPI3_MISO_M2/PCIE30X4_PERSTN_M0/GPIO0_D0_d | BUS_IOC_GPIO0D_IOMUX_SEL_L[3:0] = 4'ha<br>PMU2_IOC_GPIO0D_IOMUX_SEL_L[3:0] = 4'h8 |
| uart_rts_n | O | I2S1_SDI2_M1/PDM0_SDI0_M1/I2C6_SDA_M0/UART1_RTSN_M2/PWM6_M0/SPI0_MISO_M0/PCIE30X4_WAKEN_M0/GPIO0_C7_d | BUS_IOC_GPIO0C_IOMUX_SEL_H[15:12] = 4'ha<br>PMU2_IOC_GPIO0C_IOMUX_SEL_H[15:12] = 4'h8 |

Table 19-3 UART2 Interface Description

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| **IOMUX0** | | | |
| uart_rx | I | I2S1_SCLK_M1/JTAG_TMS_M2/I2C1_SDA_M0/UART2_RX_M0/PCIE30X1_1_WAKEN_M0/GPIO0_B6_d | BUS_IOC_GPIO0B_IOMUX_SEL_H[11:8] = 4'ha<br>PMU2_IOC_GPIO0B_IOMUX_SEL_H[11:8] = 4'h8 |
| uart_tx | O | I2S1_MCLK_M1/JTAG_TCK_M2/I2C1_SCL_M0/UART2_TX_M0/PCIE30X1_1_CLKREQN_M0/GPIO0_B5_d | BUS_IOC_GPIO0B_IOMUX_SEL_H[7:4] = 4'ha<br>PMU2_IOC_GPIO0B_IOMUX_SEL_H[7:4] = 4'ha |
| uart_cts_n | I | GMAC1_TXD1/I2S2_MCLK_M1/UART2_CTSN/GPIO3_B4_u | BUS_IOC_GPIO3B_IOMUX_SEL_H[3:0] = 4'ha |
| uart_rts_n | O | GMAC1_TXD0/I2S2_SDO_M1/UART2 | BUS_IOC_GPIO3B_IOM |

Rockchip Confidential

| | | | |
|---|---|---|---|
| | | _RTSN/GPIO3_B3_u | UX_SEL_L[15:12] = 4'ha |
| **IOMUX1** | | | |
| uart_rx | I | SDMMC_D1/PDM1_SDI2_M0/JTAG_TMS_M1/I2C3_SDA_M4/UART2_RX_M1/PWM9_M1/GPIO4_D1_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[7:4] = 4'ha |
| uart_tx | O | SDMMC_D0/PDM1_SDI3_M0/JTAG_TCK_M1/I2C3_SCL_M4/UART2_TX_M1/PWM8_M1/GPIO4_D0_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[3:0] = 4'ha |
| **IOMUX2** | | | |
| uart_rx | I | GMAC1_TXER/I2S2_SDI_M1/UART2_RX_M2/PWM3_IR_M1/GPIO3_B2_d | BUS_IOC_GPIO3B_IOMUX_SEL_L[11:8] = 4'ha |
| uart_tx | O | GMAC1_RXDV_CRS/MIPI_CAMERA4_CLK_M1/UART2_TX_M2/PWM2_M1/GPIO3_B1_d | BUS_IOC_GPIO3B_IOMUX_SEL_L[7:4] = 4'ha |

Table 19-4 UART3 Interface Description

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| **IOMUX0** | | | |
| uart_rx | I | I2C3_SDA_M0/UART3_RX_M0/SPI4_MISO_M0/GPIO1_C0_z | BUS_IOC_GPIO1C_IOMUX_SEL_L[3:0] = 4'ha |
| uart_tx | O | I2C3_SCL_M0/UART3_TX_M0/SPI4_MOSI_M0/GPIO1_C1_z | BUS_IOC_GPIO1C_IOMUX_SEL_L[7:4] = 4'ha |
| uart_cts_n | I | I2S0_SCLK/I2C6_SCL_M1/UART3_CTSN/PWM7_IR_M2/SPI4_CS0_M0/GPIO1_C3_d | BUS_IOC_GPIO1C_IOMUX_SEL_L[15:12] = 4'ha |
| uart_rts_n | O | I2S0_MCLK/I2C6_SDA_M1/UART3_RTSN/PWM3_IR_M2/SPI4_CLK_M0/GPIO1_C2__d | BUS_IOC_GPIO1C_IOMUX_SEL_L[11:8] = 4'ha |
| **IOMUX1** | | | |
| uart_rx | I | GMAC1_MCLKINOUT/II2S2_LRCK_M1/CAN1_TX_M0/UART3_RX_M1/PWM13_M0/GPIO3_B6_d | BUS_IOC_GPIO3B_IOMUX_SEL_H[11:8] = 4'ha |
| uart_tx | O | GMAC1_TXEN/I2S2_SCLK_M1/CAN1_RX_M0/UART3_TX_M1/PWM12_M0/GPIO3_B5_u | BUS_IOC_GPIO3B_IOMUX_SEL_H[7:4] = 4'ha |
| **IOMUX2** | | | |
| uart_rx | I | CIF_D6/BT1120_D6/I2S1_SDI1_M0/PCIE30X2_CLKREQN_M1/I2C5_SCL_M2/UART3_RX_M2/SPI2_CLK_M1/GPIO4_A6_d | BUS_IOC_GPIO4A_IOMUX_SEL_H[11:8] = 4'ha |
| uart_tx | O | CIF_D5/BT1120_D5/I2S1_SDI0_M0/PCIE30X1_0_PERSTN_M1/I2C3_SDA_M2/UART3_TX_M2/SPI2_MOSI_M1/GPIO4_A5_d | BUS_IOC_GPIO4A_IOMUX_SEL_H[7:4] = 4'ha |

Table 19-5 UART4 Interface Description

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| **IOMUX0** | | | |
| uart_rx | I | I2S0_SDI1/PDM0_SDI3_M0/I2C1_SDA_M4/UART4_RX_M0/PWM1_M1/SPI1 | BUS_IOC_GPIO1D_IOMUX_SEL_L[15:12] = |

Rockchip Confidential

| | | | |
|---|---|---|---|
| | | _CS0_M2/GPIO1_D3_d | 4'ha |
| uart_tx | O | I2S0_SDO3/I2S0_SDI2/PDM0_SDI2_M0/I2C1_SCL_M4/UART4_TX_M0/PWM0_M1/SPI1_CLK_M2/GPIO1_D2_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[11:8] = 4'ha |
| uart_cts_n | I | I2S0_SDO0/I2C4_SCL_M4/UART4_CTSN/GPIO1_C7_d | BUS_IOC_GPIO1C_IOMUX_SEL_H[15:12] = 4'ha |
| uart_rts_n | O | I2S0_LRCK/I2C2_SCL_M3/UART4_RTSN/GPIO1_C5_d | BUS_IOC_GPIO1C_IOMUX_SEL_H[7:4] = 4'ha |
| **IOMUX1** | | | |
| uart_rx | I | CIF_D12/PCIE20X1_2_WAKEN_M0/HDMI_TX0_SDA_M2/I2C5_SDA_M0/UART4_RX_M1/PWM8_M2/SPI3_CLK_M3/GPIO3_D0_u | BUS_IOC_GPIO3D_IOMUX_SEL_L[3:0] = 4'ha |
| uart_tx | O | CIF_D13/PCIE20X1_2_PERSTN_M0/HDMI_RX_CEC_M1/UART4_TX_M1/PWM9_M2/SPI0_MISO_M3/GPIO3_D1_d | BUS_IOC_GPIO3D_IOMUX_SEL_L[7:4] = 4'ha |
| **IOMUX2** | | | |
| uart_rx | I | PDM1_SDI3_M1/PCIE30X4_PERSTN_M3/UART4_RX_M2/SPI0_MOSI_M2/GPIO1_B2_d | BUS_IOC_GPIO1B_IOMUX_SEL_L[11:8] = 4'ha |
| uart_tx | O | PDM1_CLK1_M1/PCIE30X1_0_WAKEN_M2/SATA0_ACT_LED_M1/UART4_TX_M2/SPI0_CLK_M2/GPIO1_B3_d | BUS_IOC_GPIO1B_IOMUX_SEL_L[15:12] = 4'ha |

Table 19-6 UART5 Interface Description

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| **IOMUX0** | | | |
| uart_rx | I | SDMMC_CMD/PDM1_CLK1_M0/MCU_JTAG_TCK_M0/CAN0_TX_M1/UART5_RX_M0/PWM7_IR_M1/GPIO4_D4_u | BUS_IOC_GPIO4D_IOMUX_SEL_H[3:0] = 4'ha |
| uart_tx | O | SDMMC_CLK/PDM1_CLK0_M0/TEST_CLKOUT_M0/MCU_JTAG_TMS_M0/CAN0_RX_M1/UART5_TX_M0/GPIO4_D5_d | BUS_IOC_GPIO4D_IOMUX_SEL_H[7:4] = 4'ha |
| uart_cts_n | I | SDMMC_D2/PDM1_SDI1_M0/JTAG_TCK_M0/I2C8_SCL_M0/UART5_CTSN_M0/GPIO4_D2_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[11:8] = 4'ha |
| uart_rts_n | O | SDMMC_D3/PDM1_SDI0_M0/JTAG_TMS_M0/I2C8_SDA_M0/UART5_RTSN_M0/PWM10_M1/GPIO4_D3_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[15:12] = 4'ha |
| **IOMUX1** | | | |
| uart_rx | I | CIF_D9/FSPI_CS1N_M2/PCIE30X4_WAKEN_M2/HDMI_TX1_SDA_M1/CAN2_TX_M0/UART5_RX_M1/SPI3_CS1_M3/GPIO3_C5_u | BUS_IOC_GPIO3C_IOMUX_SEL_H[7:4] = 4'ha |
| uart_tx | O | CIF_D8/FSPI_CS0N_M2/PCIE30X4_CLKREQN_M2/HDMI_TX1_CEC_M2/CAN2_RX_M0/UART5_TX_M1/SPI3_CS0_M3/GPIO3_C4_u | BUS_IOC_GPIO3C_IOMUX_SEL_H[3:0] = 4'ha |
| uart_cts_n | I | EMMC_DATA_STROBE/I2C2_SDA_M2/UART5_CTSN_M1/GPIO2_A2_d | BUS_IOC_GPIO2A_IOMUX_SEL_L[11:8] = 4'ha |
| uart_rts_n | O | EMMC_RSTN/I2C2_SCL_M2/UART5_RTSN_M1/GPIO2_A3_d | BUS_IOC_GPIO2A_IOMUX_SEL_L[15:12] = |

Rockchip Confidential

| | | | |
|---|---|---|---|
| | | | 4'ha |
| **IOMUX2** | | | |
| uart_rx | I | EMMC_D4/I2C1_SCL_M3/UART5_RX_M2/GPIO2_D4_u | BUS_IOC_GPIO2D_IOMUX_SEL_H[3:0] = 4'ha |
| uart_tx | O | EMMC_D5/I2C1_SDA_M3/UART5_TX_M2/GPIO2_D5_u | BUS_IOC_GPIO2D_IOMUX_SEL_H[7:4] = 4'ha |

Table 19-7 UART6 Interface Description

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| **IOMUX0** | | | |
| uart_rx | I | GMAC0_RXD2/SDIO_D0_M0/FSPI_D0_M1/UART6_RX_M0/GPIO2_A6_u | BUS_IOC_GPIO2A_IOMUX_SEL_H[11:8] = 4'ha |
| uart_tx | O | GMAC0_RXD3/SDIO_D1_M0/FSPI_D1_M1/UART6_TX_M0/GPIO2_A7_u | BUS_IOC_GPIO2A_IOMUX_SEL_H[15:12] = 4'ha |
| uart_cts_n | I | GMAC0_TXD2/SDIO_D3_M0/FSPI_D3_M1/I2C8_SDA_M1/UART6_CTSN_M0/GPIO2_B1_u | BUS_IOC_GPIO2B_IOMUX_SEL_L[7:4] = 4'ha |
| uart_rts_n | O | GMAC0_RXCLK/SDIO_D2_M0/FSPI_D2_M1/I2C8_SCL_M1/UART6_RTSN_M0/GPIO2_B0_u | BUS_IOC_GPIO2B_IOMUX_SEL_L[3:0] = 4'ha |
| **IOMUX1** | | | |
| uart_rx | I | PCIE30X1_1_CLKREQN_M2/DP0_HPDIN_M2/I2C2_SDA_M4/UART6_RX_M1/SPI4_MISO_M2/GPIO1_A0_d | BUS_IOC_GPIO1A_IOMUX_SEL_L[3:0] = 4'ha |
| uart_tx | O | PCIE30X1_1_WAKEN_M2/DP1_HPDIN_M2/SATA1_ACT_LED_M1/I2C2_SCL_M4/UART6_TX_M1/SPI4_MOSI_M2/GPIO1_A1_d | BUS_IOC_GPIO1A_IOMUX_SEL_L[7:4] = 4'ha |
| uart_cts_n | I | HDMI_TX1_SDA_M2/I2C4_SCL_M3/UART6_CTSN_M1/PWM1_M2/SPI4_CS0_M2/GPIO1_A3_d | BUS_IOC_GPIO1A_IOMUX_SEL_L[15:12] = 4'ha |
| uart_rts_n | O | VOP_POST_EMPTY/I2C4_SDA_M3/UART6_RTSN_M1/PWM0_M2/SPI4_CLK_M2/GPIO1_A2_d | BUS_IOC_GPIO1A_IOMUX_SEL_L[11:8] = 4'ha |
| **IOMUX2** | | | |
| uart_rx | I | I2S0_SDO2/I2S0_SDI3/PDM0_SDI1_M0/I2C7_SDA_M0/UART6_RX_M2/SPI1_MOSI_M2/GPIO1_D1_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[7:4] = 4'ha |
| uart_tx | O | I2S0_SDO1/I2C7_SCL_M0/UART6_TX_M2/SPI1_MISO_M2/GPIO1_D0_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[3:0] = 4'ha |

Table 19-8 UART7 Interface Description

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| **IOMUX0** | | | |
| uart_rx | I | GMAC0_PTP_REFCLK/FSPI_CS0N_M1/HDMI_TX1_SDA_M0/I2C4_SDA_M1/UART7_RX_M0/GPIO2_B4_u | BUS_IOC_GPIO2B_IOMUX_SEL_H[3:0] = 4'ha |
| uart_tx | O | GMAC0_PPSTRING/FSPI_CS1N_M1/HDMI_TX1_SCL_M0/I2C4_SCL_M1/UART7_TX_M0/GPIO2_B5_u | BUS_IOC_GPIO2B_IOMUX_SEL_H[7:4] = 4'ha |
| uart_cts_n | I | GMAC0_TXER/I2C0_SDA_M1/UART7_ | BUS_IOC_GPIO4C_IOM |

Rockchip Confidential

| | | | |
|---|---|---|---|
| | | CTSN_M0/PWM7_IR_M3/SPI3_CLK_M0/GPIO4_C6_d | UX_SEL_H[11:8] = 4'ha |
| uart_rts_n | O | GMAC0_RXDV_CRS/UART7_RTSN_M0/PWM2_M2/SPI3_CS0_M0/GPIO4_C2_d | BUS_IOC_GPIO4C_IOMUX_SEL_L[11:8] = 4'ha |
| **IOMUX1** | | | |
| uart_rx | I | GMAC1_PPSCLK/PCIE30X2_BUTTON_RSTN/UART7_RX_M1/SPI1_CLK_M1/GPIO3_C1_d | BUS_IOC_GPIO3C_IOMUX_SEL_L[7:4] = 4'ha |
| uart_tx | O | GMAC1_PPSTRIG/I2C3_SDA_M1/UART7_TX_M1/SPI1_MISO_M1/GPIO3_C0_d | BUS_IOC_GPIO3C_IOMUX_SEL_L[3:0] = 4'ha |
| uart_cts_n | I | GMAC1_MDIO/MIPI_TE1/I2C8_SDA_M4/UART7_CTSN_M1/PWM15_IR_M0/SPI1_CS1_M1/GPIO3_C3_d | BUS_IOC_GPIO3C_IOMUX_SEL_L[15:12] = 4'ha |
| uart_rts_n | O | GMAC1_MDC/MIPI_TE0/I2C8_SCL_M4/UART7_RTSN_M1/PWM14_M0/SPI1_CS0_M1/GPIO3_C2_d | BUS_IOC_GPIO3C_IOMUX_SEL_L[11:8] = 4'ha |
| **IOMUX2** | | | |
| uart_rx | I | PDM1_CLK0_M1/PCIE30X1_0_PERSTN_M2/UART7_RX_M2/SPI0_CS0_M2/GPIO1_B4_u | BUS_IOC_GPIO1B_IOMUX_SEL_H[3:0] = 4'ha |
| uart_tx | O | PCIE30X1_0_CLKREQN_M2/UART7_TX_M2/SPI0_CS1_M2/GPIO1_B5_u | BUS_IOC_GPIO1B_IOMUX_SEL_H[7:4] = 4'ha |

Table 19-9 UART8 Interface Description

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| **IOMUX0** | | | |
| uart_rx | I | MIPI_CAMERA0_CLK_M0/SPDIF1_TX_M1/I2S1_SDO0_M0/PCIE30X1_0_BUTTON_RSTN/SATA2_ACT_LED_M0/I2C6_SCL_M3/UART8_RX_M0/SPI0_CS1_M1/GPIO4_B1_u | BUS_IOC_GPIO4B_IOMUX_SEL_L[7:4] = 4'ha |
| uart_tx | O | CIF_CLKIN/BT1120_CLKOUT/I2S1_SDI3_M0/PCIE30X2_PERSTN_M1/I2C6_SDA_M3/UART8_TX_M0/SPI2_CS1_M1/GPIO4_B0_d | BUS_IOC_GPIO4B_IOMUX_SEL_L[3:0] = 4'ha |
| uart_cts_n | I | CIF_VSYNC/BT1120_D9/I2S1_SDO2_M0/PCIE20X1_2_BUTTON_RSTN/I2C7_SDA_M3/UART8_CTSN_M0/PWM15_IR_M1/CAN1_TX_M1/GPIO4_B3_u | BUS_IOC_GPIO4B_IOMUX_SEL_L[15:12] = 4'ha |
| uart_rts_n | O | CIF_HREF/BT1120_D8/I2S1_SDO1_M0/PCIE30X1_1_BUTTON_RSTN/I2C7_SCL_M3/UART8_RTSN_M0/PWM14_M1/SPI0_CS0_M1/CAN1_RX_M1/GPIO4_B2_u | BUS_IOC_GPIO4B_IOMUX_SEL_L[11:8] = 4'ha |
| **IOMUX1** | | | |
| uart_rx | I | GMAC1_RXD3/SDIO_D3_M1/I2S3_SDO/AUDDSM_RN/FSPI_D3_M2/UART8_RX_M1/SPI4_CS0_M1/GPIO3_A3_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[15:12] = 4'ha |
| uart_tx | O | GMAC1_RXD2/SDIO_D2_M1/I2S3_LRCK/AUDDSM_LP/FSPI_D2_M2/UART8 | BUS_IOC_GPIO3A_IOMUX_SEL_L[11:8] = 4'ha |

Rockchip Confidential

| | | | |
|---|---|---|---|
| | | _TX_M1/SPI4_CLK_M1/GPIO3_A2_u | |
| uart_cts_n | I | GMAC1_RXCLK/SDIO_CLK_M1/MIPI_CAMERA0_CLK_M1/FSPI_CLK_M2/I2C4_SDA_M0/UART8_CTSN_M1/GPIO3_A5_d | BUS_IOC_GPIO3A_IOMUX_SEL_H[7:4] = 4'ha |
| uart_rts_n | O | GMAC1_TXCLK/SDIO_CMD_M1/I2S3_SDI/AUDDSM_RP/UART8_RTSN_M1/SPI4_CS1_M1/GPIO3_A4_d | BUS_IOC_GPIO3A_IOMUX_SEL_H[3:0] = 4'ha |

Table 19-10 UART9 Interface Description

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| **IOMUX0** | | | |
| uart_rx | I | GMAC0_PPSCLK/TEST_CLKOUT_M1/HDMI_TX1_CEC_M0/UART9_RX_M0/SPI1_CS1_M0/GPIO2_C4_d | BUS_IOC_GPIO2C_IOMUX_SEL_H[3:0] = 4'ha |
| uart_tx | O | GMAC0_RXD1/I2C6_SDA_M2/UART9_TX_M0/SPI1_MOSI_M0/GPIO2_C2_d | BUS_IOC_GPIO2C_IOMUX_SEL_L[11:8] = 4'ha |
| uart_cts_n | I | GMAC0_MDIO/I2C0_SCL_M1/UART9_CTSN_M0/PWM6_M2/SPI3_MOSI_M0/GPIO4_C5_d | BUS_IOC_GPIO4C_IOMUX_SEL_H[7:4] = 4'ha |
| uart_rts_n | O | GMAC0_MDC/I2C7_SDA_M1/UART9_RTSN_M0/PWM5_M2/SPI3_MISO_M0/GPIO4_C4_d | BUS_IOC_GPIO4C_IOMUX_SEL_H[3:0] = 4'ha |
| **IOMUX1** | | | |
| uart_rx | I | BT1120_D11/PCIE30X4_WAKEN_M1/HDMI_RX_CEC_M0/SATA1_ACT_LED_M0/UART9_RX_M1/PWM12_M1/SPI3_MISO_M1/GPIO4_B5_d | BUS_IOC_GPIO4B_IOMUX_SEL_H[7:4] = 4'ha |
| uart_tx | O | CIF_CLKOUT/BT1120_D10/I2S1_SDO3_M0/PCIE30X4_CLKREQN_M1/DP0_HPDIN_M0/SPDIF0_TX_M1/UART9_TX_M1/PWM11_IR_M1/GPIO4_B4_u | BUS_IOC_GPIO4B_IOMUX_SEL_H[3:0] = 4'ha |
| uart_cts_n | I | CIF_D1/BT1120_D1/I2S1_SCLK_M0/PCIE30X1_1_WAKEN_M1/UART9_CTSN_M1/SPI0_MOSI_M1/GPIO4_A1_d | BUS_IOC_GPIO4A_IOMUX_SEL_L[7:4] = 4'ha |
| uart_rts_n | O | CIF_D0/BT1120_D0/I2S1_MCLK_M0/PCIE30X1_1_CLKREQN_M1/UART9_RTSN_M1/SPI0_MISO_M1/GPIO4_A0_d | BUS_IOC_GPIO4A_IOMUX_SEL_L[3:0] = 4'ha |
| **IOMUX2** | | | |
| uart_rx | I | HDMI_TX0_HPD_M1/PCIE30X2_PERSTN_M2/HDMI_RX_HPDOUT_M1/MCU_JTAG_TCK_M1/UART9_RX_M2/SPI0_CS0_M3/GPIO3_D4_d | BUS_IOC_GPIO3D_IOMUX_SEL_H[3:0] = 4'ha |
| uart_tx | O | PCIE30X4_BUTTON_RSTN/DP1_HPDIN_M0/MCU_JTAG_TMS_M1/UART9_TX_M2/PWM11_IR_M3/SPI0_CS1_M3/GPIO3_D5_d | BUS_IOC_GPIO3D_IOMUX_SEL_H[7:4] = 4'ha |
| uart_cts_n | I | CIF_D15/PCIE30X2_WAKEN_M2/HDMI_RX_SDA_M1/I2C7_SDA_M2/UART9_CTSN_M2/PWM10_M2/SPI0_CLK_M3/GPIO3_D3_d | BUS_IOC_GPIO3D_IOMUX_SEL_L[15:12] = 4'ha |

Rockchip Confidential

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| uart_rts_n | O | CIF_D14/PCIE30X2_CLKREQN_M2/HDMI_RX_SCL_M1/I2C7_SCL_M2/UART9_RTSN_M2/SPI0_MOSI_M3/GPIO3_D2_d | BUS_IOC_GPIO3D_IOMUX_SEL_L[11:8] = 4'ha |

*Notes: **I**=input, **O**=output, **I/O**=input/output, bidirectional.*

## 19.6 Application Notes

### 19.6.1 None FIFO Mode Transfer Flow

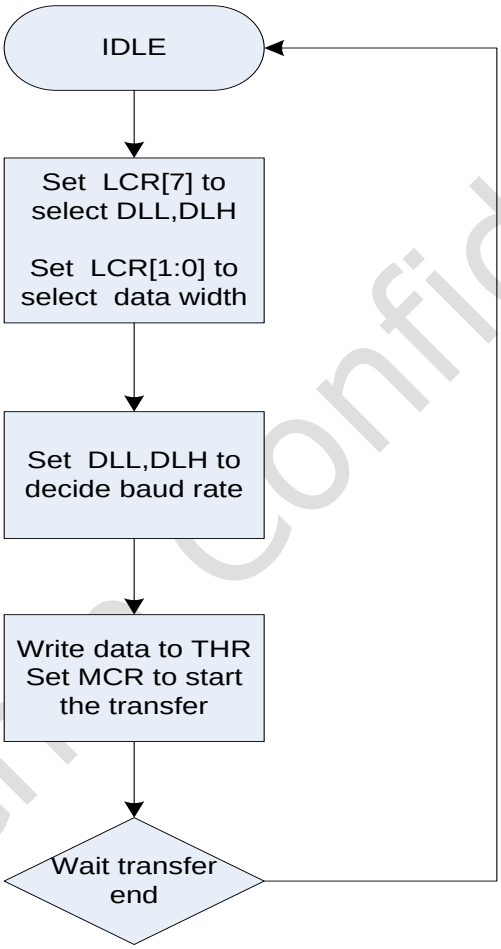



Fig. 19-7 UART none fifo mode

### 19.6.2 FIFO Mode Transfer Flow

Rockchip Confidencial

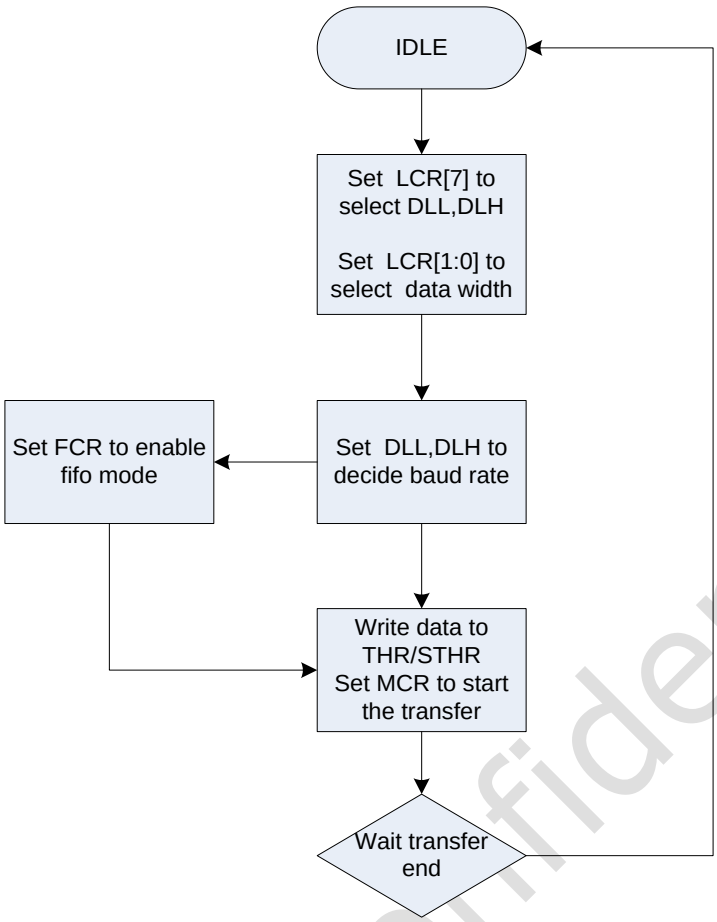



Fig. 19-8 UART fifo mode

The UART is an APB slave performing:
Serial-to-parallel conversion on data received from a peripheral device. Parallel-to-serial conversion on data transmitted to the peripheral device. The CPU reads and writes data and control/status information through the APB interface. The transmitting and receiving paths are buffered with internal FIFO memories enabling up to 64-bytes to be stored independently in both transmit and receive modes. A baud rate generator can generate a common transmit and receive internal clock input. The baud rates will depend on the internal clock frequency. The UART will also provide transmit, receive and exception interrupts to system. A DMA interface is implemented for improving the system performance.

## 19.6.3 Baud Rate Calculation

### UART clock generation

The following figures shows the UART clock generation. UARTs source clocks can be selected from different PLL outputs. UART clocks can be generated by 1 to 64 division of its source clock, or can be fractionally divided again, or be provided by XIN24M.

Rockchip Confidencial

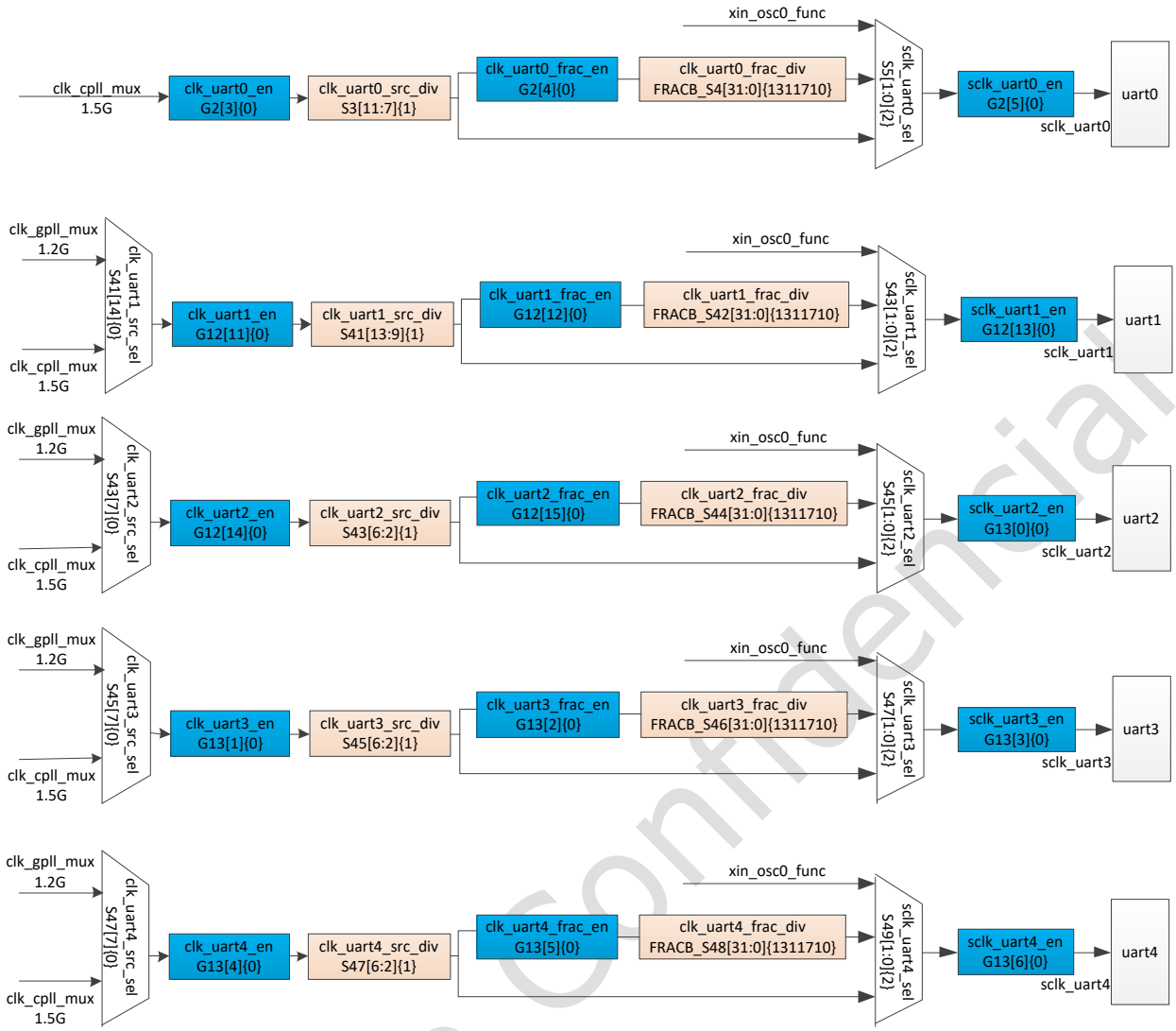



Fig. 19-9 UART0-UART4 clock generation

Rockchip Confidential

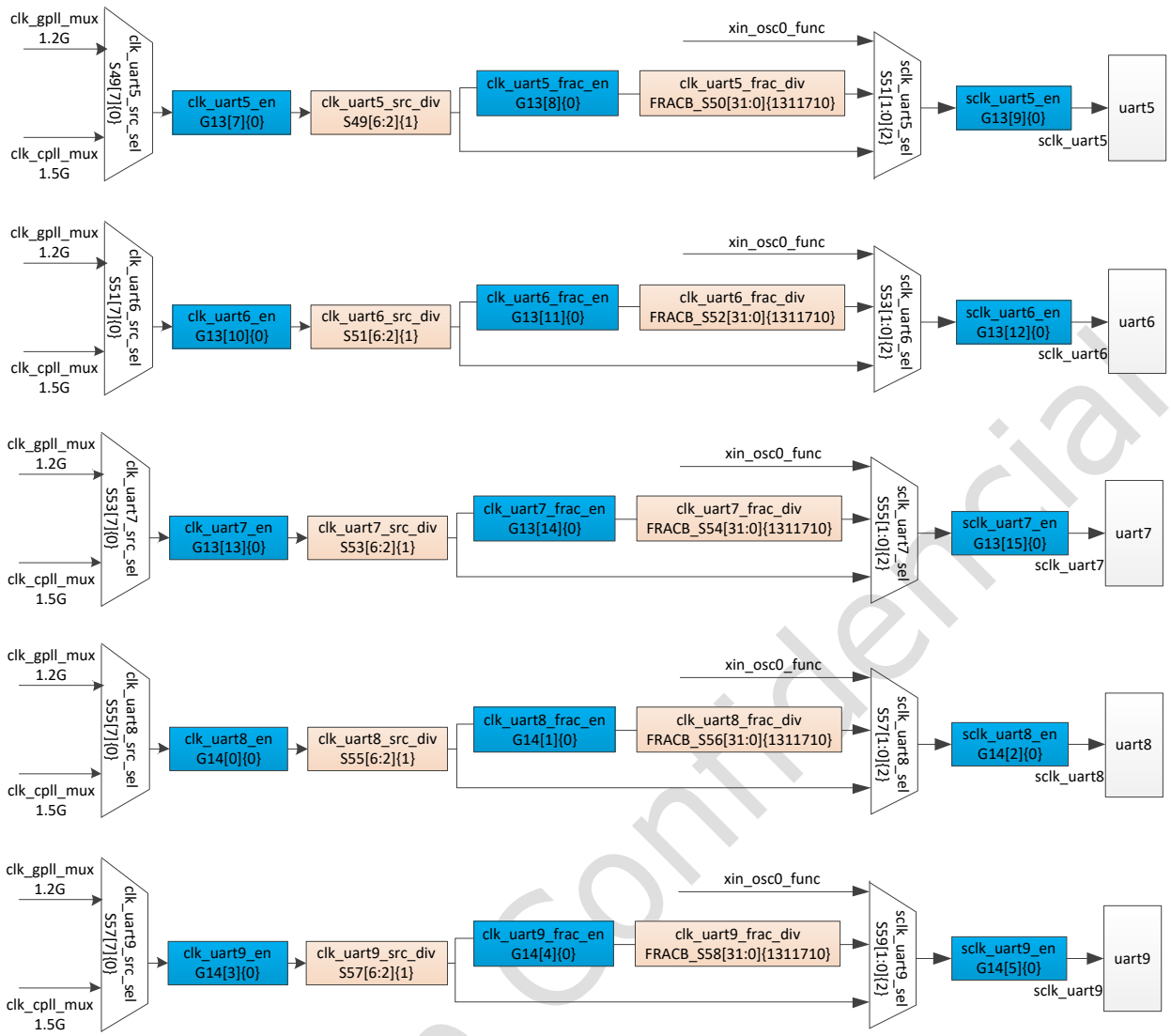



Fig. 19-10 UART5-UART9 clock generation

## UART baud rate configuration

The following table provides some reference configuration for different UART baud rates.

Table 19-11 UART baud rate configuration

| Baud Rate | Reference Configuration |
|---|---|
| 115.2 Kbps | Configure PLL to get 648MHz clock output; Divide 648MHz clock by 1152/50625 to get 14.7456MHz clock; Configure UART_DLL to 8. |
| 460.8 Kbps | Configure PLL to get 648MHz clock output; Divide 648MHz clock by 1152/50625 to get 14.7456MHz clock; Configure UART_DLL to 2. |
| 921.6 Kbps | Configure PLL to get 648MHz clock output; Divide 648MHz clock by 1152/50625 to get 14.7456MHz clock; Configure UART_DLL to 1. |
| 1.5 Mbps | Choose PLL to get 384MHz clock output; Divide 384MHz clock by 16 to get 24MHz clock; Configure UART_DLL to 1. |
| 3 Mbps | Choose PLL to get 384MHz clock output; Divide 384MHz clock by 8 to get 48MHz clock; Configure UART_DLL to 1. |
| 4 Mbps | Configure PLL to get 384MHz clock output; Divide 384MHz clock by 6 to get 64MHz clock; Configure UART_DLL to 1. |

Rockchip Confidential

# Chapter 20 GPIO

## 20.1 Overview

GPIO is a programmable General Purpose Programming I/O peripheral. This component is an APB slave device. GPIO controls the output data and direction of external I/O pads. It can also read back the data on external pads using memory-mapped registers.
GPIO supports the following features:

- 32 bits APB data bus width
- Up to 32 independently configurable signals
- Software control registers with write mask for each bit of each signal
- Configurable debounce logic with a slow clock to debounce interrupts
- Configurable interrupt mode
- Two virtual OS with independent control registers can be supported
- In two virtual OS model, each OS has independent interrupt
- Not in two virtual OS model, two interrupts with priority can be set

## 20.2 Block Diagram

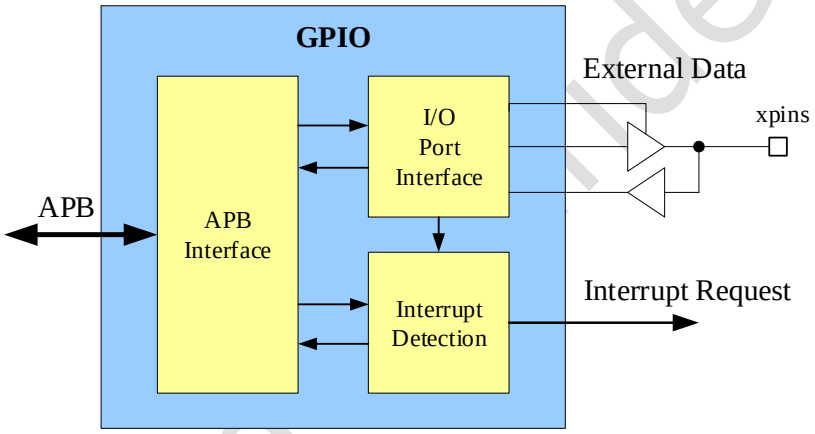



Fig. 20-1 GPIO Block Diagram

GPIO is comprised of:

- APB Interface

The APB Interface implements the APB slave operation. Its data bus width is 32 bits.

- I/O Port Interface

External data interface to or from I/O pads.

- Interrupt Detection
  Interrupt interface to or from interrupt controller.

## 20.3 Function Description

### 20.3.1 Data Control

Under software control, the data and direction control for the signal are sourced from the port data registers (GPIO_SWPORT_DR_L/GPIO_SWPORT_DR_H) and direction control registers (GPIO_SWPORT_DDR_L/GPIO_SWPORT_DRR_H).
The direction of the external I/O pad is controlled by the value of the port data direction registers. The data written to these memory-mapped registers gets mapped onto an output signal (gpio_port_ddr) of the GPIO peripheral. This output signal controls the direction of an external I/O pad. The default data direction is Input.
The data written to the port data registers drives the output buffer (gpio_port_dr) of the I/O pad.
External data are input on the external data signal (gpio_ext_port). Reading the external signal register (GPIO_EXT_PORT) shows the value of this signal, regardless of the direction. This register is read-only, meaning that it cannot be written from the APB software interface.

Rockchip Confidential

### 20.3.2 Interrupts

I/O port can be programmed to accept external signals as interrupt sources on any of the bits of the signal. The type of interrupt is programmable with one of the following settings:

- Active-high and level
- Active-low and level
- Rising edge
- Falling edge
- Both the rising edge and the falling edge

The interrupts can be masked by programming the GPIO_INT_MASK_L/GPIO_INT_MASK_H registers. The interrupt status can be read before masking (GPIO_INT_RAWSTATUS) and after masking (GPIO_INT_STATUS).

For edge-sensitive interrupts, the Interrupt Service Routine (ISR) can clear the interrupt by writing a 1 to the corresponding bit of the GPIO_PORT_EOI_L/GPIO_PORT_EOI_H registers. This write operation also clears the interrupt status and raw status registers. Writing to the interrupt clear registers has no effect on level-sensitive interrupts. If level-sensitive interrupts cause the processor to interrupt, then the ISR can poll the interrupt raw status register until the interrupt source disappears, or it can write to the interrupt mask register to mask the interrupt before exiting the ISR. If the ISR exits without masking or disabling the interrupt prior to exiting, then the level-sensitive interrupt repeatedly requests an interrupt until the interrupt is cleared at the source.

The interrupts are combined into an active-high interrupt output signal. In order to mask the combined interrupt, all individual interrupts have to be masked. The single combined interrupt does not have its own mask bit.

Whenever I/O port is configured for interrupts, the data direction must be set to Input. If the data direction is reprogrammed to Output, then any pending edge-sensitive interrupts are not lost. However, no new interrupts are generated, and level-sensitive interrupts are lost.

Interrupt signals are internally synchronized to a system clock pclk_intr, which is connected to the APB bus clock pclk. Therefore, the pclk needs to be running for interrupt detection.

### 20.3.3 Debounce Operation

The external signal can be debounced to remove any spurious glitches that are less than one period of the external debouncing clock.

When an input interrupt signal is debounced using a slow debounce clock (external input clock dbclk or internal divided clock dbclk_div), the signal must be active for a minimum of two cycles of the debounce clock to guarantee that it is registered. Any input pulse widths less than a debounce clock period are bounced. A pulse width between one and two debounce clock widths may or may not propagate, depending on its phase relationship to the debounce clock. If the input pulse spans two rising edges of the debounce clock, it is registered. If it spans only one rising edge, it is not registered.

The debounce function can be controlled by programming the debounce enable registers (GPIO_DEBOUNCE_L/GPIO_DEBOUNCE_H), debounce clock divide enable registers (GPIO_DBCLK_DIV_EN_L/GPIO_DBCLK_DIV_EN_H) and debounce clock divide control register (GPIO_DBCLK_DIV_CON).

### 20.3.4 Two OS Operation and Tow Interrupts

To select this model, virtual enable register should be set(GPIO_VIRTUAL_EN). Then all the configure can be allotted to two OS（for example OS_A and OS_B). OS_A will use the original address offset, OS_B will use the offset + 0x1000. The 32 bit I/O port should also be allotted to the OS by setting reg group registers(GPIO_REG_GROUP_L and GPIO_REG_GROUP_H). Once reg group is set, the I/O operation can only be used by the setting address offset. Each OS has its own interrupt for I/O port, this is depended on reg group.

If virtual enable register is disable, reg group can also be used to allotted I/O interrupt. These two independent interrupts may be used for priority interrupt setting.

## 20.4 Register Description

This section describes the control/status registers of the design. Software should read and

Rockchip Confidential

write these registers using 32-bits accesses. There are five GPIOs (GPIO0 in PD_PMU, GPIO1/GPIO2/GPIO3/GPIO4 in PD_BUS), and each of them has same register group. Therefore, five GPIOs' register groups have five different base addresses.

### 20.4.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| GPIO_SWPORT_DR_L | 0x0000 | W | 0x00000000 | Port Data Register (Low) |
| GPIO_SWPORT_DR_H | 0x0004 | W | 0x00000000 | Port Data Register (High) |
| GPIO_SWPORT_DDR_L | 0x0008 | W | 0x00000000 | Port Data Direction Register (Low) |
| GPIO_SWPORT_DDR_H | 0x000C | W | 0x00000000 | Port Data Direction Register (High) |
| GPIO_INT_EN_L | 0x0010 | W | 0x00000000 | Interrupt Enable Register (Low) |
| GPIO_INT_EN_H | 0x0014 | W | 0x00000000 | Interrupt Enable Register (High) |
| GPIO_INT_MASK_L | 0x0018 | W | 0x00000000 | Interrupt Mask Register (Low) |
| GPIO_INT_MASK_H | 0x001C | W | 0x00000000 | Interrupt Mask Register (High) |
| GPIO_INT_TYPE_L | 0x0020 | W | 0x00000000 | Interrupt Level Register (Low) |
| GPIO_INT_TYPE_H | 0x0024 | W | 0x00000000 | Interrupt Level Register (High) |
| GPIO_INT_POLARITY_L | 0x0028 | W | 0x00000000 | Interrupt Polarity Register (Low) |
| GPIO_INT_POLARITY_H | 0x002C | W | 0x00000000 | Interrupt Polarity Register (High) |
| GPIO_INT_BOTHEDGE_L | 0x0030 | W | 0x00000000 | Interrupt Both Edge Type Register (Low) |
| GPIO_INT_BOTHEDGE_H | 0x0034 | W | 0x00000000 | Interrupt Both Edge Type Register (High) |
| GPIO_DEBOUNCE_L | 0x0038 | W | 0x00000000 | Debounce Enable Register (Low) |
| GPIO_DEBOUNCE_H | 0x003C | W | 0x00000000 | Debounce Enable Register (High) |
| GPIO_DBCLK_DIV_EN_L | 0x0040 | W | 0x00000000 | DBCLK Divide Enable Register (Low) |
| GPIO_DBCLK_DIV_EN_H | 0x0044 | W | 0x00000000 | DBCLK Divide Enable Register (High) |
| GPIO_DBCLK_DIV_CON | 0x0048 | W | 0x00000001 | DBCLK Divide Control Register |
| GPIO_INT_STATUS | 0x0050 | W | 0x00000000 | Interrupt Status Register |
| GPIO_INT_RAWSTATUS | 0x0058 | W | 0x00000000 | Interrupt Raw Status Register |
| GPIO_PORT_EOI_L | 0x0060 | W | 0x00000000 | Interrupt Clear Register (Low) |
| GPIO_PORT_EOI_H | 0x0064 | W | 0x00000000 | Interrupt Clear Register (High) |
| GPIO_EXT_PORT | 0x0070 | W | 0x00000000 | External Port Data Register |
| GPIO_VER_ID | 0x0078 | W | 0x0101157C | Version ID Register |
| GPIO_GPIO_REG_GROUP_L | 0x0100 | W | 0x00000000 | GPIO Group Control |
| GPIO_GPIO_REG_GROUP_H | 0x0104 | W | 0x0000FFFF | GPIO Group Control |
| GPIO_GPIO_VIRTUAL_EN | 0x0108 | W | 0x00000000 | GPIO Virtual Enable |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access WORD (64 bits) access*

### 20.4.2 Detail Registers Description

**GPIO_SWPORT_DR_L**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0000 | swport_dr_low<br>Output data for the lower 16 bits of I/O Port, each bit is individual.<br>1'b0: Low<br>1'b1: High<br>Values written to this register are output on the I/O signals for the lower 16 bits of I/O Port if the corresponding data direction bits for I/O Port are set to Output mode. The value read back is equal to the last value written to this register. |

**GPIO_SWPORT_DR_H**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | swport_dr_high<br>Output data for the upper 16 bits of I/O Port, each bit is individual.<br>1'b0: Low<br>1'b1: High<br>Values written to this register are output on the I/O signals for the upper 16 bits of I/O Port if the corresponding data direction bits for I/O Port are set to Output mode. The value read back is equal to the last value written to this register. |

**GPIO_SWPORT_DDR_L**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | swport_ddr_low<br>Data direction for the lower 16 bits of I/O Port, each bit is individual.<br>1'b0: Input<br>1'b1: Output<br>Values written to this register independently control the direction of the corresponding data bit in the lower 16 bits of I/O Port. |

**GPIO_SWPORT_DDR_H**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0000 | swport_ddr_high<br>Data direction for the upper 16 bits of I/O Port, each bit is individual.<br>1'b0: Input<br>1'b1: Output<br>Values written to this register independently control the direction of the corresponding data bit in the upper 16 bits of I/O Port. |

**GPIO_INT_EN_L**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | int_en_low<br>Allows each bit of the lower 16 bits of I/O Port to be configured for interrupts.<br>1'b0: Interrupt is disabled<br>1'b1: Interrupt is enabled<br>Whenever a 1 is written to a bit of this register, it configures the corresponding bit on I/O Port to become an interrupt source; otherwise, I/O Port operates as a normal GPIO signal. Interrupts are disabled on the corresponding bits of I/O Port if the corresponding data direction register is set to Output. |

**GPIO_INT_EN_H**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | int_en_high<br>Allows each bit of the upper 16 bits of I/O Port to be configured for interrupts.<br>1'b0: Interrupt is disabled<br>1'b1: Interrupt is enabled<br>Whenever a 1 is written to a bit of this register, it configures the corresponding bit on I/O Port to become an interrupt source; otherwise, I/O Port operates as a normal GPIO signal. Interrupts are disabled on the corresponding bits of I/O Port if the corresponding data direction register is set to Output. |

**GPIO_INT_MASK_L**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0000 | int_mask_low<br>Controls whether an interrupt on the lower 16 bits of I/O Port can create an interrupt for the interrupt controller by not masking it.<br>1'b0: Interrupt is unmasked<br>1'b1: Interrupt is masked<br>Whenever a 1 is written to a bit in this register, it masks the interrupt generation capability for this signal; otherwise interrupts are allowed through. |

**GPIO_INT_MASK_H**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | int_mask_high<br>Controls whether an interrupt on the upper 16 bits of I/O Port can create an interrupt for the interrupt controller by not masking it.<br>1'b0: Interrupt is unmasked<br>1'b1: Interrupt is masked<br>Whenever a 1 is written to a bit in this register, it masks the interrupt generation capability for this signal; otherwise interrupts are allowed through. |

**GPIO_INT_TYPE_L**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | int_type_low<br>Controls the type of interrupt that can occur on the lower 16 bits of I/O Port.<br>1'b0: Level-sensitive<br>1'b1: Edge-sensitive<br>Whenever a 1 is written to a bit of this register, it configures the interrupt type to be edge-sensitive; otherwise, it is level-sensitive. |

**GPIO_INT_TYPE_H**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0000 | int_type_high<br>Controls the type of interrupt that can occur on the upper 16 bits of I/O Port.<br>1'b0: Level-sensitive<br>1'b1: Edge-sensitive<br>Whenever a 1 is written to a bit of this register, it configures the interrupt type to be edge-sensitive; otherwise, it is level-sensitive. |

**GPIO_INT_POLARITY_L**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | int_polarity_low<br>Controls the polarity of edge or level sensitivity that can occur on the lower 16 bits of I/O Port.<br>1'b0: Active-low<br>1'b1: Active-high<br>Whenever a 1 is written to a bit of this register, it configures the interrupt type to rising-edge or active-high sensitive; otherwise, it is falling-edge or active-low sensitive. |

**GPIO_INT_POLARITY_H**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | int_polarity_high<br>Controls the polarity of edge or level sensitivity that can occur on the upper 16 bits of I/O Port.<br>1'b0: Active-low<br>1'b1: Active-high<br>Whenever a 1 is written to a bit of this register, it configures the interrupt type to rising-edge or active-high sensitive; otherwise, it is falling-edge or active-low sensitive. |

**GPIO_INT_BOTHEDGE_L**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0000 | int_bothedge_low<br>Controls the edge type of interrupt that can occur on the lower 16 bits of I/O Port.<br>1'b0: Disable both-edge detection<br>1'b1: Enable both-edge detection<br>Whenever a particular bit is programmed to 1, it enables the generation of interrupts on both the rising edge and the falling edge of an external input signal corresponding to that bit on I/O Port. The values programmed in the registers int_type_low and int_polarity_low for this particular bit are not considered when the corresponding bit of this register is set to 1. Whenever a particular bit is programmed to 0, the interrupt type depends on the value of the corresponding bits in the int_type_low and int_polarity_low registers. |

**GPIO_INT_BOTHEDGE_H**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | int_bothedge_high<br>Controls the edge type of interrupt that can occur on the upper 16 bits of I/O Port.<br>1'b0: Disable both-edge detection<br>1'b1: Enable both-edge detection<br>Whenever a particular bit is programmed to 1, it enables the generation of interrupts on both the rising edge and the falling edge of an external input signal corresponding to that bit on I/O Port. The values programmed in the registers int_type_high and int_polarity_high for this particular bit are not considered when the corresponding bit of this register is set to 1. Whenever a particular bit is programmed to 0, the interrupt type depends on the value of the corresponding bits in the int_type_high and int_polarity_high registers. |

**GPIO_DEBOUNCE_L**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | debounce_low<br>Controls whether an external signal of the lower 16 bits of I/O Port that is the source of an interrupt needs to be debounced to remove any spurious glitches.<br>1'b0: Disable debounce<br>1'b1: Enable debounce<br>Writing a 1 to a bit in this register enables the debouncing circuitry. A signal must be valid for two periods of an external clock before it is internally processed. |

**GPIO_DEBOUNCE_H**

Rockchip Confidential

Address: Operational Base + offset (0x003C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | debounce_high<br>Controls whether an external signal of the lower 16 bits of I/O Port that is the source of an interrupt needs to be debounced to remove any spurious glitches.<br>1'b0: Disable debounce<br>1'b1: Enable debounce<br>Writing a 1 to a bit in this register enables the debouncing circuitry. A signal must be valid for two periods of an external clock before it is internally processed. |

**GPIO_DBCLK_DIV_EN_L**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | dbclk_div_en_low<br>Controls whether to use the internal divided clock when debounce function is enabled for an external signal of the lower 16 bits of I/O Port.<br>1'b0: Disable divider for debounce clock<br>1'b1: Enable divider for debounce clock<br>Whenever a 1 is written to a bit of this register, the clock divided from dbclk is used as debounce clock; otherwise, the original dbclk is used. The clock divide factor depends on the register dbclk_div_con. The values programmed in this register for this particular bit are not considered when the corresponding bit of the register debounce_low is set to 0. |

**GPIO_DBCLK_DIV_EN_H**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | dbclk_div_en_high<br>Controls whether to use the internal divided clock when debounce function is enabled for an external signal of the upper 16 bits of I/O Port.<br>1'b0: Disable divider for debounce clock<br>1'b1: Enable divider for debounce clock<br>Whenever a 1 is written to a bit of this register, the clock divided from dbclk is used as debounce clock; otherwise, the original dbclk is used. The clock divide factor depends on the register dbclk_div_con. The values programmed in this register for this particular bit are not considered when the corresponding bit of the register debounce_high is set to 0. |

Rockchip Confidencial

**GPIO_DBCLK_DIV_CON**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23:0 | RW | 0x000001 | dbclk_div_con<br>dbclk_div = dbclk / (dbclk_div_con + 1) |

**GPIO_INT_STATUS**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | int_status<br>Interrupt status of I/O Port. |

**GPIO_INT_RAWSTATUS**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | int_rawstatus<br>Interrupt raw status of I/O Port (premasking bits). |

**GPIO_PORT_EOI_L**

Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | R/WSC | 0x0000 | port_eoi_low<br>Controls the clearing of edge type interrupts from the lower 16 bits of I/O Port.<br>1'b0: Nothing<br>1'b1: Clear edge-sensitive interrupt<br>When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. Writing to this register has no effect on level-sensitive interrupts. All interrupts are cleared when I/O Port is not configured for interrupts. |

**GPIO_PORT_EOI_H**

Address: Operational Base + offset (0x0064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | R/WSC | 0x0000 | port_eoi_high<br>Controls the clearing of edge type interrupts from the upper 16 bits of I/O Port.<br>1'b0: Nothing<br>1'b1: Clear edge-sensitive interrupt<br>When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. Writing to this register has no effect on level-sensitive interrupts. All interrupts are cleared when I/O Port is not configured for interrupts. |

**GPIO_EXT_PORT**

Rockchip Confidencial

Address: Operational Base + offset (0x0070)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | ext_port<br>This register always reflects the value of the signals on the external I/O Port. |

**GPIO_VER_ID**

Address: Operational Base + offset (0x0078)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x0101157c | ver_id<br>Version ID. |

**GPIO_GPIO_REG_GROUP_L**

Address: Operational Base + offset (0x0100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0x0000 | gpio_reg_group_low<br>This register control the low 16 bit of GPIO and each bit corresponds each GPIO.<br>When virtual_en=1'b1:<br>1'b1: GPIO control by OS_A with offset 0x0000<br>1'b0: GPIO control by OS_B with offset 0x1000<br>When virtual_en=1'b0:<br>1'b1: GPIO interrupt connect to gpio_int_flag<br>1'b0: GPIO interrupt connect to gpio_int_flag_exp |

**GPIO_GPIO_REG_GROUP_H**

Address: Operational Base + offset (0x0104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:0 | RW | 0xffff | gpio_reg_group_high<br>This register control the high 16 bit of GPIO and each bit corresponds each GPIO.<br>When virtual_en=1'b1:<br>1'b1: GPIO control by OS_A with offset 0x0000<br>1'b0: GPIO control by OS_B with offset 0x1000<br>When virtual_en=1'b0:<br>1'b1: GPIO interrupt connect to gpio_int_flag<br>1'b0: GPIO interrupt connect to gpio_int_flag_exp |

**GPIO_GPIO_VIRTUAL_EN**

Address: Operational Base + offset (0x0108)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_mask<br>Write enable for lower 16 bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | gpio_virtual_en<br>1'b1: Enable virtual, two OS supported<br>1'b0: Disable virtual. |

## 20.5 Interface Description

Table 20-1 GPIO Interface Description

| Module Pin | Pad Name | IOMUX Setting |
|---|---|---|
| **GPIO0 Interface** | | |
| gpio0_port[0] | REFCLK_OUT/GPIO0_A0_d | PMU1_IOC_GPIO0A_IOMUX_SEL_L[3:0]=4'b0 |
| gpio0_port[1] | TSADC_SHUT_ORG/TSADC_SHUT/GPIO0_A1_z | PMU1_IOC_GPIO0A_IOMUX_SEL_L[7:4]=4'b0 |
| gpio0_port[2] | PMIC_SLEEP1/GPIO0_A2_d | PMU1_IOC_GPIO0A_IOMUX_SEL_L[11:8]=4'b0 |
| gpio0_port[3] | PMIC_SLEEP2/GPIO0_A3_d | PMU1_IOC_GPIO0A_IOMUX_SEL_L[15:12]=4'b0 |
| gpio0_port[4] | SDMMC_DET/GPIO0_A4_u | PMU1_IOC_GPIO0A_IOMUX_SEL_H[3:0]=4'b0 |
| gpio0_port[5] | SPI2_CLK_M2/SDMMC_PWREN/PMU_DEBUG/GPIO0_A5_d | PMU1_IOC_GPIO0A_IOMUX_SEL_H[7:4]=4'b0 |
| gpio0_port[6] | SPI2_MOSI_M2/I2C0_SDA_M0/GPIO0_A6_z | PMU1_IOC_GPIO0A_IOMUX_SEL_H[11:8]=4'b0 |
| gpio0_port[7] | PMIC_INT_L/GPIO0_A7_u | PMU1_IOC_GPIO0A_IOMUX_SEL_H[15:12]=4'b0 |
| gpio0_port[8] | SPI2_CS1_M2/I2C1_SCL_M1/UART0_RX_M1/GPIO0_B0_z | PMU1_IOC_GPIO0B_IOMUX_SEL_L[3:0]=4'b0 |
| gpio0_port[9] | SPI2_CS0_M2/I2C1_SDA_M1/PWM5_M0/UART0_TX_M1/GPIO0_B1_z | PMU1_IOC_GPIO0B_IOMUX_SEL_L[7:4]=4'b0 |
| gpio0_port[10] | CLK32K_IN/CLK32K_OUT0/GPIO0_B2_u | PMU1_IOC_GPIO0B_IOMUX_SEL_L[11:8]=4'b0 |
| gpio0_port[11] | SPI2_MISO_M2/I2C0_SCL_M0/GPIO0_B3_z | PMU1_IOC_GPIO0B_IOMUX_SEL_L[15:12]=4'b0 |
| gpio0_port[13] | I2S1_MCLK_M1/JTAG_TCK_M2/I2C1_SCL_M0/UART2_TX_M0/PCIE30X1_1_CLKREQN_M0/GPIO0_B5_d | PMU2_IOC_GPIO0B_IOMUX_SEL_H[7:4]=4'b0 |

Rockchip Confidential

| Module Pin | Pad Name | IOMUX Setting |
|---|---|---|
| gpio0_port[14] | I2S1_SCLK_M1/JTAG_TMS_M2/I2C1_SDA_M0/UART2_RX_M0/PCIE30X1_1_WAKEN_M0/GPIO0_B6_d | PMU2_IOC_GPIO0B_IOMUX_SEL_H[11:8]=4'b0 |
| gpio0_port[15] | I2S1_LRCK_M1/PWM0_M0/I2C2_SCL_M0/CAN0_TX_M0/SPI0_CS1_M0/PCIE30X1_1_PERSTN_M0/GPIO0_B7_d | PMU2_IOC_GPIO0B_IOMUX_SEL_H[15:12]=4'b0 |
| gpio0_port[16] | PDM0_CLK0_M1/PWM1_M0/I2C2_SDA_M0/CAN0_RX_M0/SPI0_MOSI_M0/PCIE30X1_0_CLKREQN_M0/GPIO0_C0_d | PMU2_IOC_GPIO0C_IOMUX_SEL_L[3:0]=4'b0 |
| gpio0_port[17] | PMIC_SLEEP3/GPIO0_C1_d | PMU2_IOC_GPIO0C_IOMUX_SEL_L[7:4]=4'b0 |
| gpio0_port[18] | PMIC_SLEEP4/GPIO0_C2_d | PMU2_IOC_GPIO0C_IOMUX_SEL_L[11:8]=4'b0 |
| gpio0_port[19] | PMIC_SLEEP5/GPIO0_C3_d | PMU2_IOC_GPIO0C_IOMUX_SEL_L[15:12]=4'b0 |
| gpio0_port[20] | PDM0_CLK1_M1/PWM2_M0/UART0_RX_M0/I2C4_SDA_M2/DP0_HPDIN_M1/PCIE30X1_0_WAKEN_M0/GPIO0_C4_d | PMU2_IOC_GPIO0C_IOMUX_SEL_H[3:0]=4'b0 |
| gpio0_port[21] | I2S1_SDI0_M1/GPU_AVS/UART0_TX_M0/I2C4_SCL_M2/DP1_HPDIN_M1/PWM4_M0/PCIE30X1_0_PERSTN_M0/GPIO0_C5_u | PMU2_IOC_GPIO0C_IOMUX_SEL_H[7:4]=4'b0 |
| gpio0_port[22] | I2S1_SDI1_M1/NPU_AVS/UART0_RTSN/PWM5_M1/SPI0_CLK_M0/PCIE30X4_CLKREQN_M0/SATA_CP_POD/GPIO0_C6_u | PMU2_IOC_GPIO0C_IOMUX_SEL_H[11:8]=4'b0 |
| gpio0_port[23] | I2S1_SDI2_M1/PDM0_SDI0_M1/I2C6_SDA_M0/UART1_RTSN_M2/PWM6_M0/SPI0_MISO_M0/PCIE30X4_WAKEN_M0/GPIO0_C7_d | PMU2_IOC_GPIO0C_IOMUX_SEL_H[15:12]=4'b0 |
| gpio0_port[24] | I2S1_SDI3_M1/PDM0_SDI1_M1/I2C6_SCL_M0/UART1_CTSN_M2/PWM7_IR_M0/SPI3_MISO_M2/PCIE30X4_PERSTN_M0/GPIO0_D0_d | PMU2_IOC_GPIO0D_IOMUX_SEL_L[3:0]=4'b0 |
| gpio0_port[25] | I2S1_SDO0_M1/CPU_BIG0_AVS/I2C0_SCL_M2/UART0_CTSN/UART1_TX_M2/HDMI_RX_SDA_M0/SPI0_CS0_M0/PCIE30X2_CLKREQN_M0/HDMI_TX0_CEC_M1/GPIO0_D1_u | PMU2_IOC_GPIO0D_IOMUX_SEL_L[7:4]=4'b0 |
| gpio0_port[26] | I2S1_SDO1_M1/I2C0_SDA_M2/UART1_RX_M2/HDMI_RX_SCL_M0/SPI3_MOSI_M2/PCIE30X2_WAKEN_M0/HDMI_TX1_CEC_M1/GPIO0_D2_u | PMU2_IOC_GPIO0D_IOMUX_SEL_L[11:8]=4'b0 |

Rockchip Confidential

| Module Pin | Pad Name | IOMUX Setting |
|---|---|---|
| gpio0_port[27] | LITCPU_AVS/SPI3_CLK_M2/GPIO0_D3_u | PMU2_IOC_GPIO0D_IOMUX_SEL_L[15:12]=4'b0 |
| gpio0_port[28] | I2S1_SDO2_M1/PDM0_SDI2_M1/PWM3_IR_M0/I2C1_SCL_M2/CAN2_RX_M1/HDMI_TX0_SDA_M1/SPI3_CS0_M2/PCIE30X2_PERSTN_M0/SATA_CPDET/GPIO0_D4_u | PMU2_IOC_GPIO0D_IOMUX_SEL_H[3:0]=4'b0 |
| gpio0_port[29] | I2S1_SDO3_M1/CPU_BIG1_AVS/I2C1_SDA_M2/CAN2_TX_M1/HDMI_TX0_SCL_M1/SPI3_CS1_M2/SATA_MP_SWITCH/GPIO0_D5_u | PMU2_IOC_GPIO0D_IOMUX_SEL_H[7:4]=4'b0 |
| gpio0_port[30] | PMIC_SLEEP6/PDM0_SDI3_M1/GPIO0_D6_d | PMU2_IOC_GPIO0D_IOMUX_SEL_H[11:8]=4'b0 |
| **GPIO1 Interface** | | |
| gpio1_port[0] | PCIE30X1_1_CLKREQN_M2/DP0_HPDIN_M2/I2C2_SDA_M4/UART6_RX_M1/SPI4_MISO_M2/GPIO1_A0_d | BUS_IOC_GPIO1A_IOMUX_SEL_L[3:0]=4'b0 |
| gpio1_port[1] | PCIE30X1_1_WAKEN_M2/DP1_HPDIN_M2/SATA1_ACT_LED_M1/I2C2_SCL_M4/UART6_TX_M1/SPI4_MOSI_M2/GPIO1_A1_d | BUS_IOC_GPIO1A_IOMUX_SEL_L[7:4]=4'b0 |
| gpio1_port[2] | VOP_POST_EMPTY/I2C4_SDA_M3/UART6_RTSN_M1/PWM0_M2/SPI4_CLK_M2/GPIO1_A2_d | BUS_IOC_GPIO1A_IOMUX_SEL_L[11:8]=4'b0 |
| gpio1_port[3] | HDMI_TX1_SDA_M2/I2C4_SCL_M3/UART6_CTSN_M1/PWM1_M2/SPI4_CS0_M2/GPIO1_A3_d | BUS_IOC_GPIO1A_IOMUX_SEL_L[15:12]=4'b0 |
| gpio1_port[4] | HDMI_TX1_SCL_M2/SPI2_MISO_M0/GPIO1_A4_d | BUS_IOC_GPIO1A_IOMUX_SEL_H[3:0]=4'b0 |
| gpio1_port[5] | HDMI_TX0_HPD_M0/SPI2_MOSI_M0/GPIO1_A5_d | BUS_IOC_GPIO1A_IOMUX_SEL_H[7:4]=4'b0 |
| gpio1_port[6] | HDMI_TX1_HPD_M0/SPI2_CLK_M0/GPIO1_A6_d | BUS_IOC_GPIO1A_IOMUX_SEL_H[11:8]=4'b0 |
| gpio1_port[7] | PDM1_SDI0_M1/PCIE30X1_1_PERSTN_M2/PWM3_IR_M3/SPI2_CS0_M0/GPIO1_A7_u | BUS_IOC_GPIO1A_IOMUX_SEL_H[15:12]=4'b0 |
| gpio1_port[8] | PDM1_SDI1_M1/PCIE30X4_CLKREQN_M3/SPI2_CS1_M0/GPIO1_B0_u | BUS_IOC_GPIO1B_IOMUX_SEL_L[3:0]=4'b0 |
| gpio1_port[9] | PDM1_SDI2_M1/PCIE30X4_WAKEN_M3/SPI0_MISO_M2/GPIO1_B1_d | BUS_IOC_GPIO1B_IOMUX_SEL_L[7:4]=4'b0 |

Rockchip Confidential

Copyright 2022 © Rockchip Electronics Co., Ltd. 

| Module Pin | Pad Name | IOMUX Setting |
|---|---|---|
| gpio1_port[10] | PDM1_SDI3_M1/PCIE30X4_PERSTN_M3/UART4_RX_M2/SPI0_MOSI_M2/GPIO1_B2_d | BUS_IOC_GPIO1B_IOMUX_SEL_L[11:8]=4'b0 |
| gpio1_port[11] | PDM1_CLK1_M1/PCIE30X1_0_WAKEN_M2/SATA0_ACT_LED_M1/UART4_TX_M2/SPI0_CLK_M2/GPIO1_B3_d | BUS_IOC_GPIO1B_IOMUX_SEL_L[15:12]=4'b0 |
| gpio1_port[12] | PDM1_CLK0_M1/PCIE30X1_0_PERSTN_M2/UART7_RX_M2/SPI0_CS0_M2/GPIO1_B4_u | BUS_IOC_GPIO1B_IOMUX_SEL_H[3:0]=4'b0 |
| gpio1_port[13] | PCIE30X1_0_CLKREQN_M2/UART7_TX_M2/SPI0_CS1_M2/GPIO1_B5_u | BUS_IOC_GPIO1B_IOMUX_SEL_H[7:4]=4'b0 |
| gpio1_port[14] | MIPI_CAMERA1_CLK_M0/SPDIF0_TX_M0/PCIE30X2_WAKEN_M3/HDMI_RX_HPDOUT_M2/I2C5_SCL_M3/UART1_TX_M1/GPIO1_B6_d | BUS_IOC_GPIO1B_IOMUX_SEL_H[11:8]=4'b0 |
| gpio1_port[15] | MIPI_CAMERA2_CLK_M0/SPDIF1_TX_M0/PCIE30X2_PERSTN_M3/HDMI_RX_CEC_M2/SATA2_ACT_LED_M1/I2C5_SDA_M3/UART1_RX_M1/PWM13_M2/GPIO1_B7_u | BUS_IOC_GPIO1B_IOMUX_SEL_H[15:12]=4'b0 |
| gpio1_port[16] | I2C3_SDA_M0/UART3_RX_M0/SPI4_MISO_M0/GPIO1_C0_z | BUS_IOC_GPIO1C_IOMUX_SEL_L[3:0]=4'b0 |
| gpio1_port[17] | I2C3_SCL_M0/UART3_TX_M0/SPI4_MOSI_M0/GPIO1_C1_z | BUS_IOC_GPIO1C_IOMUX_SEL_L[7:4]=4'b0 |
| gpio1_port[18] | I2S0_MCLK/I2C6_SDA_M1/UART3_RTSN/PWM3_IR_M2/SPI4_CLK_M0/GPIO1_C2__d | BUS_IOC_GPIO1C_IOMUX_SEL_L[11:8]=4'b0 |
| gpio1_port[19] | I2S0_SCLK/I2C6_SCL_M1/UART3_CTSN/PWM7_IR_M2/SPI4_CS0_M0/GPIO1_C3_d | BUS_IOC_GPIO1C_IOMUX_SEL_L[15:12]=4'b0 |
| gpio1_port[20] | PDM0_CLK1_M0/I2C2_SDA_M3/PWM11_IR_M2/SPI4_CS1_M0/GPIO1_C4_d | BUS_IOC_GPIO1C_IOMUX_SEL_H[3:0]=4'b0 |
| gpio1_port[21] | I2S0_LRCK/I2C2_SCL_M3/UART4_RTSN/GPIO1_C5_d | BUS_IOC_GPIO1C_IOMUX_SEL_H[7:4]=4'b0 |
| gpio1_port[22] | PDM0_CLK0_M0/I2C4_SDA_M4/PWM15_IR_M2/GPIO1_C6_d | BUS_IOC_GPIO1C_IOMUX_SEL_H[11:8]=4'b0 |
| gpio1_port[23] | I2S0_SDO0/I2C4_SCL_M4/UART4_CTSN/GPIO1_C7_d | BUS_IOC_GPIO1C_IOMUX_SEL_H[15:12]=4'b0 |
| gpio1_port[24] | I2S0_SDO1/I2C7_SCL_M0/UART6_TX_M2/SPI1_MISO_M2/GPIO1_D0_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[3:0]=4'b0 |

Rockchip Confidential

| Module Pin | Pad Name | IOMUX Setting |
|---|---|---|
| gpio1_port[25] | I2S0_SDO2/I2S0_SDI3/PDM0_SDI1_M0/I2C7_SDA_M0/UART6_RX_M2/SPI1_MOSI_M2/GPIO1_D1_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[7:4]=4'b0 |
| gpio1_port[26] | I2S0_SDO3/I2S0_SDI2/PDM0_SDI2_M0/I2C1_SCL_M4/UART4_TX_M0/PWM0_M1/SPI1_CLK_M2/GPIO1_D2_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[11:8]=4'b0 |
| gpio1_port[27] | I2S0_SDI1/PDM0_SDI3_M0/I2C1_SDA_M4/UART4_RX_M0/PWM1_M1/SPI1_CS0_M2/GPIO1_D3_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[15:12]=4'b0 |
| gpio1_port[28] | I2S0_SDI0/GPIO1_D4_d | BUS_IOC_GPIO1D_IOMUX_SEL_H[3:0]=4'b0 |
| gpio1_port[29] | PDM0_SDI0_M0/SPI1_CS1_M2/GPIO1_D5_d | BUS_IOC_GPIO1D_IOMUX_SEL_H[7:4]=4'b0 |
| gpio1_port[30] | MIPI_CAMERA3_CLK_M0/HDMI_RX_SCL_M2/I2C8_SCL_M2/UART1_RTSN_M1/PWM14_M2/GPIO1_D6_u | BUS_IOC_GPIO1D_IOMUX_SEL_H[11:8]=4'b0 |
| gpio1_port[31] | MIPI_CAMERA4_CLK_M0/PCIE30X2_CLKREQN_M3/HDMI_RX_SDA_M2/I2C8_SDA_M2/UART1_CTSN_M1/PWM15_IR_M3/GPIO1_D7_u | BUS_IOC_GPIO1C_IOMUX_SEL_H[15:12]=4'b0 |
| **GPIO2 Interface** | | |
| gpio2_port[0] | EMMC_CMD/FSPI_CLK_M0/GPIO2_A0_u | BUS_IOC_GPIO2A_IOMUX_SEL_L[3:0]=4'b0 |
| gpio2_port[1] | EMMC_CLKOUT/GPIO2_A1_d | BUS_IOC_GPIO2A_IOMUX_SEL_L[7:4]=4'b0 |
| gpio2_port[2] | EMMC_DATA_STROBE/I2C2_SDA_M2/UART5_CTSN_M1/GPIO2_A2_d | BUS_IOC_GPIO2A_IOMUX_SEL_L[11:8]=4'b0 |
| gpio2_port[3] | EMMC_RSTN/I2C2_SCL_M2/UART5_RTSN_M1/GPIO2_A3_d | BUS_IOC_GPIO2A_IOMUX_SEL_L[15:12]=4'b0 |
| gpio2_port[6] | GMAC0_RXD2/SDIO_D0_M0/FSPI_D0_M1/UART6_RX_M0/GPIO2_A6_u | BUS_IOC_GPIO2A_IOMUX_SEL_H[11:8]=4'b0 |
| gpio2_port[7] | GMAC0_RXD3/SDIO_D1_M0/FSPI_D1_M1/UART6_TX_M0/GPIO2_A7_u | BUS_IOC_GPIO2A_IOMUX_SEL_H[15:12]=4'b0 |
| gpio2_port[8] | GMAC0_RXCLK/SDIO_D2_M0/FSPI_D2_M1/I2C8_SCL_M1/UART6_RTSN_M0/GPIO2_B0_u | BUS_IOC_GPIO2B_IOMUX_SEL_L[3:0]=4'b0 |

Rockchip Confidential

| Module Pin | Pad Name | IOMUX Setting |
|---|---|---|
| gpio2_port[9] | GMAC0_TXD2/SDIO_D3_M0/FSPI_D3_M1/I2C8_SDA_M1/UART6_CTSN_M0/GPIO2_B1_u | BUS_IOC_GPIO2B_IOMUX_SEL_L[7:4]=4'b0 |
| gpio2_port[10] | GMAC0_TXD3/SDIO_CMD_M0/I2C3_SCL_M3/GPIO2_B2_u | BUS_IOC_GPIO2B_IOMUX_SEL_L[11:8]=4'b0 |
| gpio2_port[11] | GMAC0_TXCLK/SDIO_CLK_M0/FSPI_CLK_M1/I2C3_SDA_M3/GPIO2_B3_d | BUS_IOC_GPIO2B_IOMUX_SEL_L[15:12]=4'b0 |
| gpio2_port[12] | GMAC0_PTP_REFCLK/FSPI_CS0N_M1/HDMI_TX1_SDA_M0/I2C4_SDA_M1/UART7_RX_M0/GPIO2_B4_u | BUS_IOC_GPIO2B_IOMUX_SEL_H[3:0]=4'b0 |
| gpio2_port[13] | GMAC0_PPSTRING/FSPI_CS1N_M1/HDMI_TX1_SCL_M0/I2C4_SCL_M1/UART7_TX_M0/GPIO2_B5_u | BUS_IOC_GPIO2B_IOMUX_SEL_H[7:4]=4'b0 |
| gpio2_port[14] | GMAC0_TXD0/I2S2_MCLK_M0/I2C5_SCL_M4/UART1_RX_M0/GPIO2_B6_d | BUS_IOC_GPIO2B_IOMUX_SEL_H[11:8]=4'b0 |
| gpio2_port[15] | GMAC0_TXD1/I2S2_SCLK_M0/I2C5_SDA_M4/UART1_TX_M0/GPIO2_B7_d | BUS_IOC_GPIO2B_IOMUX_SEL_H[15:12]=4'b0 |
| gpio2_port[16] | GMAC0_RXCLK/SDIO_D2_M0/FSPI_D2_M1/I2C8_SCL_M1/UART6_RTSN_M0/GPIO2_B0_u | BUS_IOC_GPIO2C_IOMUX_SEL_L[3:0]=4'b0 |
| gpio2_port[17] | GMAC0_TXD2/SDIO_D3_M0/FSPI_D3_M1/I2C8_SDA_M1/UART6_CTSN_M0/GPIO2_B1_u | BUS_IOC_GPIO2C_IOMUX_SEL_L[7:4]=4'b0 |
| gpio2_port[18] | GMAC0_TXD3/SDIO_CMD_M0/I2C3_SCL_M3/GPIO2_B2_u | BUS_IOC_GPIO2C_IOMUX_SEL_L[11:8]=4'b0 |
| gpio2_port[19] | GMAC0_TXCLK/SDIO_CLK_M0/FSPI_CLK_M1/I2C3_SDA_M3/GPIO2_B3_d | BUS_IOC_GPIO2C_IOMUX_SEL_L[15:12]=4'b0 |
| gpio2_port[20] | GMAC0_PTP_REFCLK/FSPI_CS0N_M1/HDMI_TX1_SDA_M0/I2C4_SDA_M1/UART7_RX_M0/GPIO2_B4_u | BUS_IOC_GPIO2C_IOMUX_SEL_H[3:0]=4'b0 |
| gpio2_port[21] | GMAC0_PPSTRING/FSPI_CS1N_M1/HDMI_TX1_SCL_M0/I2C4_SCL_M1/UART7_TX_M0/GPIO2_B5_u | BUS_IOC_GPIO2C_IOMUX_SEL_H[7:4]=4'b0 |
| gpio2_port[22] | EMMC_D0/FSPI_D0_M0/GPIO2_D0_u | BUS_IOC_GPIO2D_IOMUX_SEL_L[3:0]=4'b0 |
| gpio2_port[25] | EMMC_D1/FSPI_D1_M0/GPIO2_D1_u | BUS_IOC_GPIO2D_IOMUX_SEL_L[7:4]=4'b0 |

Rockchip Confidencal

| Module Pin | Pad Name | IOMUX Setting |
|---|---|---|
| gpio2_port[26] | EMMC_D2/FSPI_D2_M0/GPIO2_D2_u | BUS_IOC_GPIO2D_IOMUX_SEL_L[11:8]=4'b0 |
| gpio2_port[27] | EMMC_D3/FSPI_D3_M0/GPIO2_D3_u | BUS_IOC_GPIO2D_IOMUX_SEL_L[15:12]=4'b0 |
| gpio2_port[28] | EMMC_D4/I2C1_SCL_M3/UART5_RX_M2/GPIO2_D4_u | BUS_IOC_GPIO2D_IOMUX_SEL_H[3:0]=4'b0 |
| gpio2_port[29] | EMMC_D5/I2C1_SDA_M3/UART5_TX_M2/GPIO2_D5_u | BUS_IOC_GPIO2D_IOMUX_SEL_H[7:4]=4'b0 |
| gpio2_port[30] | EMMC_D6/FSPI_CS0N_M0/GPIO2_D6_u | BUS_IOC_GPIO2D_IOMUX_SEL_H[11:8]=4'b0 |
| gpio2_port[31] | EMMC_D7/FSPI_CS1N_M0/GPIO2_D7_u | BUS_IOC_GPIO2D_IOMUX_SEL_H[15:12]=4'b0 |
| **GPIO3 Interface** | | |
| gpio3_port[0] | GMAC1_TXD2/SDIO_D0_M1/I2S3_MCLK/FSPI_D0_M2/I2C6_SDA_M4/PWM10_M0/SPI4_MISO_M1/GPIO3_A0_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[3:0]=4'b0 |
| gpio3_port[1] | GMAC1_TXD3/SDIO_D1_M1/I2S3_SCLK/AUDDSM_LN/FSPI_D1_M2/I2C6_SCL_M4/PWM11_IR_M0/SPI4_MOSI_M1/GPIO3_A1_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[7:4]=4'b0 |
| gpio3_port[2] | GMAC1_RXD2/SDIO_D2_M1/I2S3_LRCK/AUDDSM_LP/FSPI_D2_M2/UART8_TX_M1/SPI4_CLK_M1/GPIO3_A2_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[11:8]=4'b0 |
| gpio3_port[3] | GMAC1_RXD3/SDIO_D3_M1/I2S3_SDO/AUDDSM_RN/FSPI_D3_M2/UART8_RX_M1/SPI4_CS0_M1/GPIO3_A3_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[15:12]=4'b0 |
| gpio3_port[4] | GMAC1_TXCLK/SDIO_CMD_M1/I2S3_SDI/AUDDSM_RP/UART8_RTSN_M1/SPI4_CS1_M1/GPIO3_A4_d | BUS_IOC_GPIO3A_IOMUX_SEL_H[3:0]=4'b0 |
| gpio3_port[5] | GMAC1_RXCLK/SDIO_CLK_M1/MIPI_CAMERA0_CLK_M1/FSPI_CLK_M2/I2C4_SDA_M0/UART8_CTSN_M1/GPIO3_A5_d | BUS_IOC_GPIO3A_IOMUX_SEL_H[7:4]=4'b0 |
| gpio3_port[6] | ETH1_REFCLKO_25M/MIPI_CAMERA1_CLK_M1/I2C4_SCL_M0/GPIO3_A6_d | BUS_IOC_GPIO3A_IOMUX_SEL_H[11:8]=4'b0 |
| gpio3_port[7] | GMAC1_RXD0/MIPI_CAMERA2_CLK_M1/PWM8_M0/GPIO3_A7_u | BUS_IOC_GPIO3A_IOMUX_SEL_H[15:12]=4'b0 |

Rockchip Confidential

| Module Pin | Pad Name | IOMUX Setting |
|---|---|---|
| gpio3_port[8] | GMAC1_RXD1/MIPI_CAMERA3_CLK_M1/PWM9_M0/GPIO3_B0_u | BUS_IOC_GPIO3B_IOMUX_SEL_L[3:0]=4'b0 |
| gpio3_port[9] | GMAC1_RXDV_CRS/MIPI_CAMERA4_CLK_M1/UART2_TX_M2/PWM2_M1/GPIO3_B1_d | BUS_IOC_GPIO3B_IOMUX_SEL_L[7:4]=4'b0 |
| gpio3_port[10] | GMAC1_TXER/I2S2_SDI_M1/UART2_RX_M2/PWM3_IR_M1/GPIO3_B2_d | BUS_IOC_GPIO3B_IOMUX_SEL_L[11:8]=4'b0 |
| gpio3_port[11] | GMAC1_TXD0/I2S2_SDO_M1/UART2_RTSN/GPIO3_B3_u | BUS_IOC_GPIO3B_IOMUX_SEL_L[15:12]=4'b0 |
| gpio3_port[12] | GMAC1_TXD1/I2S2_MCLK_M1/UART2_CTSN/GPIO3_B4_u | BUS_IOC_GPIO3B_IOMUX_SEL_H[3:0]=4'b0 |
| gpio3_port[13] | GMAC1_TXEN/I2S2_SCLK_M1/CAN1_RX_M0/UART3_TX_M1/PWM12_M0/GPIO3_B5_u | BUS_IOC_GPIO3B_IOMUX_SEL_H[7:4]=4'b0 |
| gpio3_port[14] | GMAC1_MCLKINOUT/II2S2_LRCK_M1/CAN1_TX_M0/UART3_RX_M1/PWM13_M0/GPIO3_B6_d | BUS_IOC_GPIO3B_IOMUX_SEL_H[11:8]=4'b0 |
| gpio3_port[15] | GMAC1_PTP_REF_CLK/HDMI_TX1_HPD_M1/I2C3_SCL_M1/SPI1_MOSI_M1/GPIO3_B7_d | BUS_IOC_GPIO3B_IOMUX_SEL_H[15:12]=4'b0 |
| gpio3_port[16] | GMAC1_PPSTRIG/I2C3_SDA_M1/UART7_TX_M1/SPI1_MISO_M1/GPIO3_C0_d | BUS_IOC_GPIO3C_IOMUX_SEL_L[3:0]=4'b0 |
| gpio3_port[17] | GMAC1_PPSCLK/PCIE30X2_BUTTON_RSTN/UART7_RX_M1/SPI1_CLK_M1/GPIO3_C1_d | BUS_IOC_GPIO3C_IOMUX_SEL_L[7:4]=4'b0 |
| gpio3_port[18] | GMAC1_MDC/MIPI_TE0/I2C8_SCL_M4/UART7_RTSN_M1/PWM14_M0/SPI1_CS0_M1/GPIO3_C2_d | BUS_IOC_GPIO3C_IOMUX_SEL_L[11:8]=4'b0 |
| gpio3_port[19] | GMAC1_MDIO/MIPI_TE1/I2C8_SDA_M4/UART7_CTSN_M1/PWM15_IR_M0/SPI1_CS1_M1/GPIO3_C3_d | BUS_IOC_GPIO3C_IOMUX_SEL_L[15:12]=4'b0 |
| gpio3_port[20] | CIF_D8/FSPI_CS0N_M2/PCIE30X4_CLKREQN_M2/HDMI_TX1_CEC_M2/CAN2_RX_M0/UART5_TX_M1/SPI3_CS0_M3/GPIO3_C4_u | BUS_IOC_GPIO3C_IOMUX_SEL_H[3:0]=4'b0 |
| gpio3_port[21] | CIF_D9/FSPI_CS1N_M2/PCIE30X4_WAKEN_M2/HDMI_TX1_SDA_M1/CAN2_TX_M0/UART5_RX_M1/SPI3_CS1_M3/GPIO3_C5_u | BUS_IOC_GPIO3C_IOMUX_SEL_H[7:4]=4'b0 |
| gpio3_port[22] | CIF_D10/PCIE30X4_PERSTN_M2/HDMI_TX1_SCL_M1/SPI3_MISO_M3/GPIO3_C6_u | BUS_IOC_GPIO3C_IOMUX_SEL_H[11:8]=4'b0 |

Rockchip Confidential

| Module Pin | Pad Name | IOMUX Setting |
|---|---|---|
| gpio3_port[23] | CIF_D11/PCIE20X1_2_CLKREQN_M0/HDMI_TX0_SCL_M2/I2C5_SCL_M0/SPI3_MOSI_M3/GPIO3_C7_u | BUS_IOC_GPIO3C_IOMUX_SEL_H[15:12]=4'b0 |
| gpio3_port[24] | CIF_D12/PCIE20X1_2_WAKEN_M0/HDMI_TX0_SDA_M2/I2C5_SDA_M0/UART4_RX_M1/PWM8_M2/SPI3_CLK_M3/GPIO3_D0_u | BUS_IOC_GPIO3D_IOMUX_SEL_L[3:0]=4'b0 |
| gpio3_port[25] | CIF_D13/PCIE20X1_2_PERSTN_M0/HDMI_RX_CEC_M1/UART4_TX_M1/PWM9_M2/SPI0_MISO_M3/GPIO3_D1_d | BUS_IOC_GPIO3D_IOMUX_SEL_L[7:4]=4'b0 |
| gpio3_port[26] | CIF_D14/PCIE30X2_CLKREQN_M2/HDMI_RX_SCL_M1/I2C7_SCL_M2/UART9_RTSN_M2/SPI0_MOSI_M3/GPIO3_D2_d | BUS_IOC_GPIO3D_IOMUX_SEL_L[11:8]=4'b0 |
| gpio3_port[27] | CIF_D15/PCIE30X2_WAKEN_M2/HDMI_RX_SDA_M1/I2C7_SDA_M2/UART9_CTSN_M2/PWM10_M2/SPI0_CLK_M3/GPIO3_D3_d | BUS_IOC_GPIO3D_IOMUX_SEL_L[15:12]=4'b0 |
| gpio3_port[28] | HDMI_TX0_HPD_M1/PCIE30X2_PERSTN_M2/HDMI_RX_HPDOUT_M1/MCU_JTAG_TCK_M1/UART9_RX_M2/SPI0_CS0_M3/GPIO3_D4_d | BUS_IOC_GPIO3D_IOMUX_SEL_H[3:0]=4'b0 |
| gpio3_port[29] | PCIE30X4_BUTTON_RSTN/DP1_HPDIN_M0/MCU_JTAG_TMS_M1/UART9_TX_M2/PWM11_IR_M3/SPI0_CS1_M3/GPIO3_D5_d | BUS_IOC_GPIO3D_IOMUX_SEL_H[7:4]=4'b0 |
| **GPIO4 Interface** | | |
| gpio4_port[0] | CIF_D0/BT1120_D0/I2S1_MCLK_M0/PCIE30X1_1_CLKREQN_M1/UART9_RTSN_M1/SPI0_MISO_M1/GPIO4_A0_d | BUS_IOC_GPIO4A_IOMUX_SEL_L[3:0]=4'b0 |
| gpio4_port[1] | CIF_D1/BT1120_D1/I2S1_SCLK_M0/PCIE30X1_1_WAKEN_M1/UART9_CTSN_M1/SPI0_MOSI_M1/GPIO4_A1_d | BUS_IOC_GPIO4A_IOMUX_SEL_L[7:4]=4'b0 |
| gpio4_port[2] | CIF_D2/BT1120_D2/I2S1_LRCK_M0/PCIE30X1_1_PERSTN_M1/SPI0_CLK_M1/GPIO4_A2_d | BUS_IOC_GPIO4A_IOMUX_SEL_L[11:8]=4'b0 |
| gpio4_port[3] | CIF_D3/BT1120_D3/PCIE30X1_0_CLKREQN_M1/UART0_TX_M2/GPIO4_A3_d | BUS_IOC_GPIO4A_IOMUX_SEL_L[15:12]=4'b0 |
| gpio4_port[4] | CIF_D4/BT1120_D4/PCIE30X1_0_WAKEN_M1/I2C3_SCL_M2/UART0_RX_M2/SPI2_MISO_M1/GPIO4_A4_d | BUS_IOC_GPIO4A_IOMUX_SEL_H[3:0]=4'b0 |

Rockchip Confidential

| Module Pin | Pad Name | IOMUX Setting |
|---|---|---|
| gpio4_port[5] | CIF_D5/BT1120_D5/I2S1_SDI0_M0/PCIE30X1_0_PERSTN_M1/I2C3_SDA_M2/UART3_TX_M2/SPI2_MOSI_M1/GPIO4_A5_d | BUS_IOC_GPIO4A_IOMUX_SEL_H[7:4]=4'b0 |
| gpio4_port[6] | CIF_D6/BT1120_D6/I2S1_SDI1_M0/PCIE30X2_CLKREQN_M1/I2C5_SCL_M2/UART3_RX_M2/SPI2_CLK_M1/GPIO4_A6_d | BUS_IOC_GPIO4A_IOMUX_SEL_H[11:8]=4'b0 |
| gpio4_port[7] | CIF_D7/BT1120_D7/I2S1_SDI2_M0/PCIE30X2_WAKEN_M1/I2C5_SDA_M2/SPI2_CS0_M1/GPIO4_A7_d | BUS_IOC_GPIO4A_IOMUX_SEL_H[15:12]=4'b0 |
| gpio4_port[8] | CIF_CLKIN/BT1120_CLKOUT/I2S1_SDI3_M0/PCIE30X2_PERSTN_M1/I2C6_SDA_M3/UART8_TX_M0/SPI2_CS1_M1/GPIO4_B0_d | BUS_IOC_GPIO4B_IOMUX_SEL_L[3:0]=4'b0 |
| gpio4_port[9] | MIPI_CAMERA0_CLK_M0/SPDIF1_TX_M1/I2S1_SDO0_M0/PCIE30X1_0_BUTTON_RSTN/SATA2_ACT_LED_M0/I2C6_SCL_M3/UART8_RX_M0/SPI0_CS1_M1/GPIO4_B1_u | BUS_IOC_GPIO4B_IOMUX_SEL_L[7:4]=4'b0 |
| gpio4_port[10] | CIF_HREF/BT1120_D8/I2S1_SDO1_M0/PCIE30X1_1_BUTTON_RSTN/I2C7_SCL_M3/UART8_RTSN_M0/PWM14_M1/SPI0_CS0_M1/CAN1_RX_M1/GPIO4_B2_u | BUS_IOC_GPIO4B_IOMUX_SEL_L[11:8]=4'b0 |
| gpio4_port[11] | CIF_VSYNC/BT1120_D9/I2S1_SDO2_M0/PCIE20X1_2_BUTTON_RSTN/I2C7_SDA_M3/UART8_CTSN_M0/PWM15_IR_M1/CAN1_TX_M1/GPIO4_B3_u | BUS_IOC_GPIO4B_IOMUX_SEL_L[15:12]=4'b0 |
| gpio4_port[12] | CIF_CLKOUT/BT1120_D10/I2S1_SDO3_M0/PCIE30X4_CLKREQN_M1/DP0_HPDIN_M0/SPDIF0_TX_M1/UART9_TX_M1/PWM11_IR_M1/GPIO4_B4_u | BUS_IOC_GPIO4B_IOMUX_SEL_H[3:0]=4'b0 |
| gpio4_port[13] | BT1120_D11/PCIE30X4_WAKEN_M1/HDMI_RX_CEC_M0/SATA1_ACT_LED_M0/UART9_RX_M1/PWM12_M1/SPI3_MISO_M1/GPIO4_B5_d | BUS_IOC_GPIO4B_IOMUX_SEL_H[7:4]=4'b0 |
| gpio4_port[14] | BT1120_D12/PCIE30X4_PERSTN_M1/HDMI_RX_HPDOUT_M0/SATA0_ACT_LED_M0/I2C5_SCL_M1/PWM13_M1/SPI3_MOSI_M1/GPIO4_B6_d | BUS_IOC_GPIO4B_IOMUX_SEL_H[11:8]=4'b0 |
| gpio4_port[15] | BT1120_D13/PCIE20X1_2_CLKREQN_M1/HDMI_TX0_SCL_M0/I2C5_SDA_M1/SPI3_CLK_M1/GPIO4_B7_u | BUS_IOC_GPIO4B_IOMUX_SEL_H[15:12]=4'b0 |

Rockchip Confidential

| Module Pin | Pad Name | IOMUX Setting |
|---|---|---|
| gpio4_port[16] | BT1120_D14/PCIE20X1_2_WAKEN_M1/HDMI_TX0_SDA_M0/I2C8_SCL_M3/SPI3_CS0_M1/GPIO4_C0_u | BUS_IOC_GPIO4C_IOMUX_SEL_L[3:0]=4'b0 |
| gpio4_port[17] | BT1120_D15/SPDIF1_TX_M2/PCIE20X1_2_PERSTN_M1/HDMI_TX0_CEC_M0/I2C8_SDA_M3/PWM6_M1/SPI3_CS1_M1/GPIO4_C1_d | BUS_IOC_GPIO4C_IOMUX_SEL_L[7:4]=4'b0 |
| gpio4_port[18] | GMAC0_RXDV_CRS/UART7_RTSN_M0/PWM2_M2/SPI3_CS0_M0/GPIO4_C2_d | BUS_IOC_GPIO4C_IOMUX_SEL_L[11:8]=4'b0 |
| gpio4_port[19] | GMAC0_MCLKINOUT/I2S2_SDO_M0/I2C7_SCL_M1/PWM4_M1/SPI3_CS1_M0/GPIO4_C3_d | BUS_IOC_GPIO4C_IOMUX_SEL_L[15:12]=4'b0 |
| gpio4_port[20] | GMAC0_MDC/I2C7_SDA_M1/UART9_RTSN_M0/PWM5_M2/SPI3_MISO_M0/GPIO4_C4_d | BUS_IOC_GPIO4C_IOMUX_SEL_H[3:0]=4'b0 |
| gpio4_port[21] | GMAC0_MDIO/I2C0_SCL_M1/UART9_CTSN_M0/PWM6_M2/SPI3_MOSI_M0/GPIO4_C5_d | BUS_IOC_GPIO4C_IOMUX_SEL_H[7:4]=4'b0 |
| gpio4_port[22] | GMAC0_TXER/I2C0_SDA_M1/UART7_CTSN_M0/PWM7_IR_M3/SPI3_CLK_M0/GPIO4_C6_d | BUS_IOC_GPIO4C_IOMUX_SEL_H[11:8]=4'b0 |
| gpio4_port[24] | SDMMC_D0/PDM1_SDI3_M0/JTAG_TCK_M1/I2C3_SCL_M4/UART2_TX_M1/PWM8_M1/GPIO4_D0_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[3:0]=4'b0 |
| gpio4_port[25] | SDMMC_D1/PDM1_SDI2_M0/JTAG_TMS_M1/I2C3_SDA_M4/UART2_RX_M1/PWM9_M1/GPIO4_D1_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[7:4]=4'b0 |
| gpio4_port[26] | SDMMC_D2/PDM1_SDI1_M0/JTAG_TCK_M0/I2C8_SCL_M0/UART5_CTSN_M0/GPIO4_D2_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[11:8]=4'b0 |
| gpio4_port[27] | SDMMC_D3/PDM1_SDI0_M0/JTAG_TMS_M0/I2C8_SDA_M0/UART5_RTSN_M0/PWM10_M1/GPIO4_D3_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[15:12]=4'b0 |
| gpio4_port[28] | SDMMC_CMD/PDM1_CLK1_M0/MCU_JTAG_TCK_M0/CAN0_TX_M1/UART5_RX_M0/PWM7_IR_M1/GPIO4_D4_u | BUS_IOC_GPIO4D_IOMUX_SEL_H[3:0]=4'b0 |
| gpio4_port[29] | SDMMC_CLK/PDM1_CLK0_M0/TEST_CLKOUT_M0/MCU_JTAG_TMS_M0/CAN0_RX_M1/UART5_TX_M0/GPIO4_D5_d | BUS_IOC_GPIO4D_IOMUX_SEL_H[7:4]=4'b0 |

*Notes: Unused Module Pin is tied to zero!*

Rockchip Confidential

## 20.6 Application Notes

- Reading from an unused location or unused bits in a particular register always returns zeros. There is no error mechanism in the APB.
- Programming the GPIO registers for interrupt detection should be completed prior to enabling the interrupts in order to prevent spurious glitches on the interrupt output signal to the interrupt controller.

Rockchip Confidencial

Copyright 2022 © Rockchip Electronics Co., Ltd. 

# Chapter 21 I2C Interface

## 21.1 Overview

The Inter-Integrated Circuit (I2C) is a two wired (SCL and SDA), bi-directional serial bus that provides an efficient and simple method of information exchange between devices. This I2C bus controller supports master mode acting as a bridge between AMBA protocol and generic I2C bus system.

I2C Controller supports the following features:

- Support 9 independent I2C: I2C0~8, with 42 pairs IOs.
- Item Compatible with I2C-bus
- AMBA APB slave interface
- Supports master mode of I2C bus
- Software programmable clock frequency and transfer rate up to 400Kbit/sec
- Supports 7 bits and 10 bits addressing modes
- Interrupt or polling driven multiple bytes data transfer
- Clock stretching and wait state generation
- Filter out glitch on SCL and SDA

## 21.2 Block Diagram

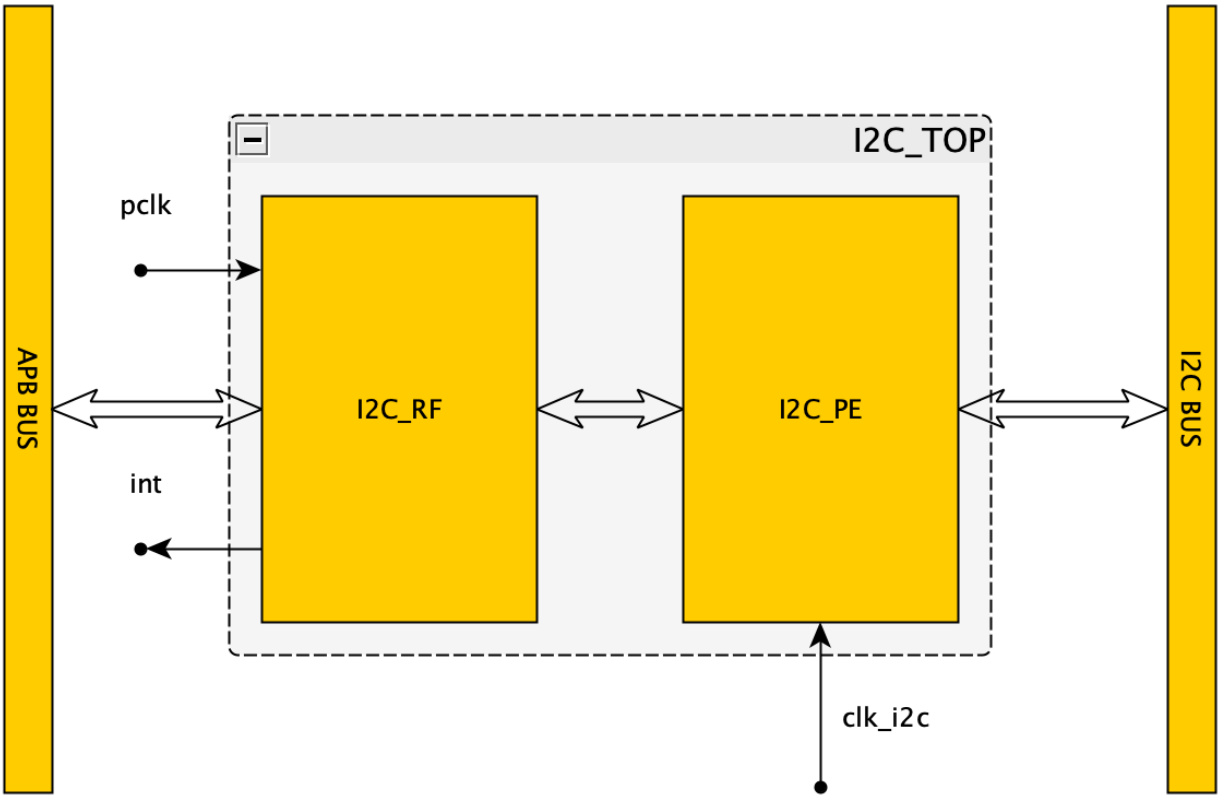



Fig. 21-1 I2C architecture

### 21.2.1 I2C_RF

I2C_RF module is used to control the I2C controller operation by the host with APB interface. It implements the register set and the interrupt functionality. The I2C_RF component operates synchronously with the pclk.

### 21.2.2 I2C_PE

I2C_PE module implements the I2C master operation for transmit data to and receive data from other I2C devices. The I2C master controller operates synchronously with the clk_i2c.

Copyright 2022 © Rockchip Electronics Co., Ltd.

### 21.2.3 I2C_TOP

I2C_TOP module is the top module of the I2C controller.

## 21.3 Function Description

This chapter provides a description about the functions and behavior under various conditions.
The I2C controller supports only Master function. It supports the 7-bits/10-bits addressing mode and support general call address. The maximum clock frequency and transfer rate can be up to 400Kbit/sec.
The operations of I2C controller is divided to 2 parts and described separately: initialization and master mode programming.

### 21.3.1 Initialization

The I2C controller is based on AMBA APB bus architecture and usually is part of a SOC. So before I2C operates, some system setting and configuration must be conformed, which includes:

- I2C interrupt connection type: CPU interrupt scheme should be considered. If the I2C interrupt is connected to extra Interrupt Controller module, we need decide the INTC vector.
- I2C Clock Rate: The I2C controller uses the APB clock to configure controller and uses clk_i2c as the working clock. The correct register setting is subject to the system requirement.

### 21.3.2 Master Mode Programming

- SCL Clock
  When the I2C controller is programmed in Master mode, the SCL frequency is determined by I2C_CLKDIV register. The SCL frequency is calculated by the following formula:
  SCL Divisor = 8*(CLKDIVL + 1 + CLKDIVH + 1); clk_i2c = 100MHz~200MHz.
  SCL = clk_i2c/ SCLK Divisor.

- Data Receiver Register Access
  When the I2C controller received MRXCNT bytes data, CPU can get the data through register RXDATA0 ~ RXDATA7. The controller can receive up to 32 bytes' data in one transaction.
  When MRXCNT register is written, the I2C controller will start to drive SCL to receive data.

- Transmit Transmitter Register
  Data to transmit are written to TXDATA0~7 by CPU. The controller can transmit up to 32 bytes' data in one transaction. The lower byte will be transmitted first.
  When MTXCNT register is written, the I2C controller will start to transmit data.

- Start Command
  Write 1 to I2C_CON[3], the controller will send I2C start command.

- Stop Command
  Write 1 to I2C_CON[4], the controller will send I2C stop command.

- I2C Operation mode
  There are four i2c operation modes.
  - When I2C_CON[2:1] is 2'b00, the controller transmit all valid data in TXDATA0~TXDATA7 byte by byte. The controller will transmit lower byte first.
  - When I2C_CON[2:1] is 2'b01, the controller will transmit device address in MRXADDR first (Write/Read bit = 0) and then transmit device register address in MRXRADDR. After that, the controller will assert restart signal and resend MRXADDR

Rockchip Confidential

(Write/Read bit = 1). At last, the controller enter receive mode.
- When I2C_CON[2:1] is 2'b10, the controller is in receive mode, it will trigger clock to read MRXCNT byte data.
- When I2C_CON[2:1] is 2'b11, the controller will transmit device address in MRXADDR first (Write/Read bit = 1) and then transmit device register address in MRXRADDR. After that, the controller will assert restart signal and resend MRXADDR (Write/Read bit = 1). At last, the controller enter receive mode.

- Read/Write Command
  - When I2C_OPMODE(I2C_CON[2:1]) is 2'b01 or 2'b11, the Read/Write command bit is decided by controller itself.
  - In RX only mode (I2C_CON[2:1] is 2'b10), the Read/Write command bit is decided by MRXADDR[0].
  - In TX only mode (I2C_CON[[2:1] is 2'b00), the Read/Write command bit is decided by TXDATA[0].

- Master Interrupt Condition
  There are 7 interrupt bits in I2C_ISR register related to master mode.
  - Byte transmitted finish interrupt (Bit 0): The bit is asserted when Master completed transmitting a byte.
  - Byte received finish interrupt (Bit 1): The bit is asserted when Master completed receiving a byte.
  - MTXCNT bytes data transmitted finish interrupt (Bit 2): The bit is asserted when Master completed transmitting MTXCNT bytes.
  - MRXCNT bytes data received finish interrupt (Bit 3): The bit is asserted when Master completed receiving MRXCNT bytes.
  - Start interrupt (Bit 4): The bit is asserted when Master finished asserting start command to I2C bus.
  - Stop interrupt (Bit 5): The bit is asserted when Master finished asserting stop command to I2C bus.
  - NAK received interrupt (Bit 6): The bit is asserted when Master received a NAK handshake.

- Last byte acknowledge control
  - If I2C_CON[5] is 1, the I2C controller will transmit NAK handshake to slave when the last byte received in RX only mode.
  - If I2C_CON[5] is 0, the I2C controller will transmit ACK handshake to slave when the last byte received in RX only mode.

- How to handle NAK handshake received
  - If I2C_CON[6] is 1, the I2C controller will stop all transactions when NAK handshake received. And the software should take responsibility to handle the problem.
  - If I2C_CON[6] is 0, the I2C controller will ignore all NAK handshake received.

- I2C controller data transfer waveform
  - Bit transferring
    - Data Validity
      The SDA line must be stable during the high period of SCL, and the data on SDA line can only be changed when SCL is in low state.

Rockchip Confidential

Copyright 2022 © Rockchip Electronics Co., Ltd. 

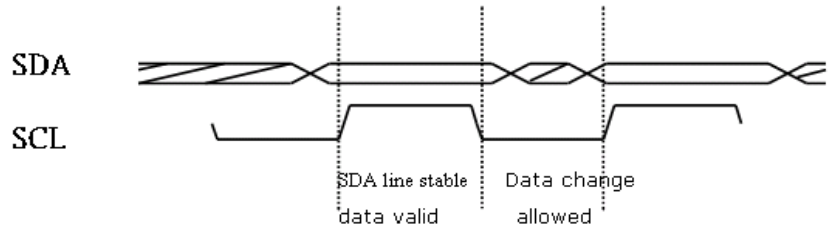



Fig. 21-2 I2C DATA Validity

- START and STOP conditions
  START condition occurs when SDA goes low while SCL is in high period. STOP condition is generated when SDA line goes high while SCL is in high state.

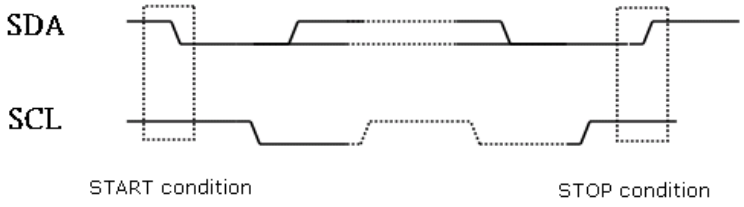



Fig. 21-3 I2C Start and stop conditions

- Data transfer
  - Acknowledge
    After a byte of data transferring (clocks labeled as 1~8), in 9th clock the receiver must assert an ACK signal on SDA line, if the receiver pulls SDA line to low, it means "ACK", on the contrary, it's "NOT ACK".

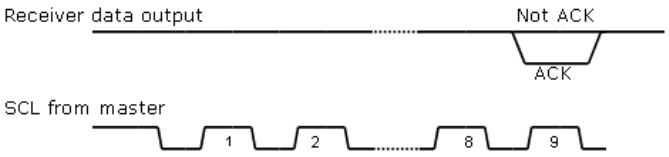



Fig. 21-4 I2C Acknowledge

  - Byte transfer
    The master own I2C bus might initiate multi byte to transfer to a slave. The transfer starts from a "START" command and ends in a "STOP" command. After every byte transfer, the receiver must reply an ACK to transmitter.

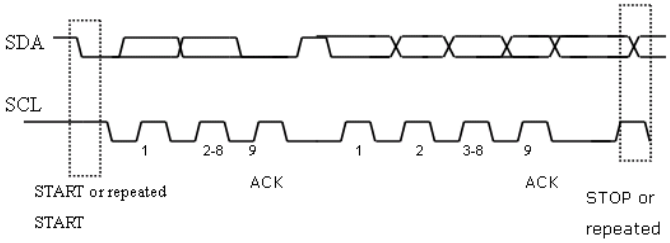



Fig. 21-5 I2C byte transfer

# 21.4 Register Description

## 21.4.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKI2C_CON | 0x0000 | W | 0x00050000 | Control register |

Rockchip Confidential

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKI2C_CLKDIV | 0x0004 | W | 0x00000001 | Clock divider register I2C CLK = PCLK / (16*CLKDIV) |
| RKI2C_MRXADDR | 0x0008 | W | 0x00000000 | The slave address accessed for master rx mode |
| RKI2C_MRXRADDR | 0x000C | W | 0x00000000 | The slave register address accessed for master rx mode |
| RKI2C_MTXCNT | 0x0010 | W | 0x00000000 | Master transmit count, specify the total bytes to be transmit (0~32) |
| RKI2C_MRXCNT | 0x0014 | W | 0x00000000 | Master rx count, specify the total bytes to be recieved(0~32) |
| RKI2C_IEN | 0x0018 | W | 0x00000000 | Interrupt enable register |
| RKI2C_IPD | 0x001C | W | 0x00000000 | Interrupt pending register |
| RKI2C_FCNT | 0x0020 | W | 0x00000000 | Finished count: the count of data which has been transmitted or received for debug purpose |
| RKI2C_SCL_OE_DB | 0x0024 | W | 0x00000020 | Slave hold debounce configure register |
| RKI2C_TXDATA0 | 0x0100 | W | 0x00000000 | I2C tx data register 0 |
| RKI2C_TXDATA1 | 0x0104 | W | 0x00000000 | I2C tx data register 1 |
| RKI2C_TXDATA2 | 0x0108 | W | 0x00000000 | I2C tx data register 2 |
| RKI2C_TXDATA3 | 0x010C | W | 0x00000000 | I2C tx data register 3 |
| RKI2C_TXDATA4 | 0x0110 | W | 0x00000000 | I2C tx data register 4 |
| RKI2C_TXDATA5 | 0x0114 | W | 0x00000000 | I2C tx data register 5 |
| RKI2C_TXDATA6 | 0x0118 | W | 0x00000000 | I2C tx data register 6 |
| RKI2C_TXDATA7 | 0x011C | W | 0x00000000 | I2C tx data register 7 |
| RKI2C_RXDATA0 | 0x0200 | W | 0x00000000 | I2C rx data register 0 |
| RKI2C_RXDATA1 | 0x0204 | W | 0x00000000 | I2C rx data register 1 |
| RKI2C_RXDATA2 | 0x0208 | W | 0x00000000 | I2C rx data register 2 |
| RKI2C_RXDATA3 | 0x020C | W | 0x00000000 | I2C rx data register 3 |
| RKI2C_RXDATA4 | 0x0210 | W | 0x00000000 | I2C rx data register 4 |
| RKI2C_RXDATA5 | 0x0214 | W | 0x00000000 | I2C rx data register 5 |
| RKI2C_RXDATA6 | 0x0218 | W | 0x00000000 | I2C rx data register 6 |
| RKI2C_RXDATA7 | 0x021C | W | 0x00000000 | I2C rx data register 7 |
| RKI2C_ST | 0x0220 | W | 0x00000000 | Status debug register |
| RKI2C_DBGCTRL | 0x0224 | W | 0x00000000 | Debug config register |
| RKI2C_CON1 | 0x0228 | W | 0x00000000 | Control register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 21.4.2 Detail Registers Description

**RKI2C_CON**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0005 | version<br>Rki2c version information. |
| 15:14 | RW | 0x0 | stop_setup<br>Stop setup config.<br>TSU;sto = (stop_setup + 1) * T(SCL_HIGH) + Tclk_i2c. |
| 13:12 | RW | 0x0 | start_setup<br>Start setup config.<br>TSU;sta = (start_setup + 1) * T(SCL_HIGH) + Tclk_i2c.<br>THD;sta = (start_setup + 2) * T(SCL_HIGH) - Tclk_i2c. |

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:8 | RW | 0x0 | data_upd_st<br>SDA update point config.<br>Used to config sda change state when scl is low, used to adjust setup/hold time.<br>4'bn: Thold = (n + 1) * Tclk_i2c.<br>Note: 0 <= n <= 5 |
| 7 | RO | 0x0 | reserved |
| 6 | RW | 0x0 | act2nak<br>Operation when NAK handshake is received.<br>1'b0: Ignored.<br>1'b1: Stop transaction. |
| 5 | RW | 0x0 | ack<br>Last byte acknowledge control in master receive mode.<br>1'b0: ACK<br>1'b1: NAK |
| 4 | RW | 0x0 | stop<br>Stop enable, when this bit is written to 1, I2C will generate stop signal. |
| 3 | RW | 0x0 | start<br>Start enable, when this bit is written to 1, I2C will generate start signal. |
| 2:1 | RW | 0x0 | i2c_mode<br>I2c mode select.<br>2'b00: Transmit only.<br>2'b01: Transmit address (device + register address) --> Restart --> Transmit address -> Receive only.<br>2'b10: Receive only.<br>2'b11: Transmit address (device + register address, write/read bit is 1) --> Restart --> Transmit address (device address) --> Receive data. |
| 0 | RW | 0x0 | i2c_en<br>I2c module enable.<br>1'b0: Disable<br>1'b1: Enable |

**RKI2C_CLKDIV**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | CLKDIVH<br>SCL high level clock count.<br>T(SCL_HIGH) = Tclk_i2c * (CLKDIVH + 1) * 8. |
| 15:0 | RW | 0x0001 | CLKDIVL<br>SCL low level clock count.<br>T(SCL_LOW) = Tclk_i2c * (CLKDIVL + 1) * 8. |

**RKI2C_MRXADDR**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:27 | RO | 0x00 | reserved |
| 26 | RW | 0x0 | addhvld<br>Address high byte valid.<br>1'b0: Invalid<br>1'b1: Valid |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 25 | RW | 0x0 | addmvld<br>Address middle byte valid.<br>1'b0: Invalid<br>1'b1: Valid |
| 24 | RW | 0x0 | addlvld<br>Address low byte valid.<br>1'b0: Invalid<br>1'b1: Valid |
| 23:0 | RW | 0x000000 | saddr<br>Master address register.<br>The lowest bit indicate write or read.<br>24 bits address register. |

**RKI2C_MRXRADDR**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:27 | RO | 0x00 | reserved |
| 26 | RW | 0x0 | sraddhvld<br>Address high byte valid.<br>1'b0: Invalid<br>1'b1: Valid |
| 25 | RW | 0x0 | sraddmvld<br>Address middle byte valid.<br>1'b0: Invalid<br>1'b1: Valid |
| 24 | RW | 0x0 | sraddlvld<br>Address low byte valid.<br>1'b0: Invalid<br>1'b1: Valid |
| 23:0 | RW | 0x000000 | sraddr<br>Slave register address accessed.<br>24 bits register address |

**RKI2C_MTXCNT**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5:0 | RW | 0x00 | mtxcnt<br>Master transmit count.<br>6 bits counter |

**RKI2C_MRXCNT**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5:0 | RW | 0x00 | mrxcnt<br>Master rx count.<br>6 bits counter |

**RKI2C_IEN**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x0 | slavehdsclen<br>Slave hold scl interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | nakrcvien<br>NAK handshake received interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | stopien<br>Stop operation finished interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | startien<br>Start operation finished interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | mbrfien<br>MRXCNT data received finished interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | mbtfien<br>MTXCNT data transfer finished interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | brfien<br>Byte rx finished interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | btfien<br>Byte tx finished interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |

**RKI2C_IPD**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RW | 0x0 | slavehdsclipd<br>Slave hold scl interrupt pending bit.<br>1'b0: No interrupt available.<br>1'b1: Slave hold scl interrupt appear, write 1 to clear. |
| 6 | W1C | 0x0 | nakrcvipd<br>NAK handshake received interrupt pending bit.<br>1'b0: No interrupt available.<br>1'b1: NAK handshake received interrupt appear, write 1 to clear. |
| 5 | W1C | 0x0 | stopipd<br>Stop operation finished interrupt pending bit.<br>1'b0: No interrupt available.<br>1'b1: Stop operation finished interrupt appear, write 1 to clear. |
| 4 | W1C | 0x0 | startipd<br>Start operation finished interrupt pending bit.<br>1'b0: No interrupt available.<br>1'b1: Start operation finished interrupt appear, write 1 to clear. |

Rockchip Confidencial

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | W1C | 0x0 | mbrfipd<br>MRXCNT data received finished interrupt pending bit.<br>1'b0: No interrupt available.<br>1'b1: MRXCNT data received finished interrupt appear, write 1 to clear. |
| 2 | W1C | 0x0 | mbtfipd<br>MTXCNT data transfer finished interrupt pending bit.<br>1'b0: No interrupt available.<br>1'b1: MTXCNT data transfer finished interrupt appear, write 1 to clear. |
| 1 | W1C | 0x0 | brfipd<br>Byte rx finished interrupt pending bit.<br>1'b0: No interrupt available.<br>1'b1: Byte rx finished interrupt appear, write 1 to clear. |
| 0 | W1C | 0x0 | btfipd<br>Byte tx finished interrupt pending bit.<br>1'b0: No interrupt available.<br>1'b1: Byte tx finished interrupt appear, write 1 to clear. |

**RKI2C_FCNT**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5:0 | RO | 0x00 | fcnt<br>The count of data which has been transmitted or received for debug purpose. |

**RKI2C_SCL_OE_DB**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x20 | scl_oe_db<br>Slave hold scl debounce.<br>Cycles for debounce (unit: Tclk_i2c). |

**RKI2C_TXDATA0**

Address: Operational Base + offset (0x0100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | txdata0<br>Data0 to be transmitted.<br>32 bits data |

**RKI2C_TXDATA1**

Address: Operational Base + offset (0x0104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | txdata1<br>Data1 to be transmitted.<br>32 bits data |

**RKI2C_TXDATA2**

Address: Operational Base + offset (0x0108)

Rockchip Confidential

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | txdata2<br>Data2 to be transmitted.<br>32 bits data |

**RKI2C_TXDATA3**

Address: Operational Base + offset (0x010C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | txdata3<br>Data3 to be transmitted.<br>32 bits data |

**RKI2C_TXDATA4**

Address: Operational Base + offset (0x0110)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | txdata4<br>Data4 to be transmitted.<br>32 bits data |

**RKI2C_TXDATA5**

Address: Operational Base + offset (0x0114)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | txdata5<br>Data5 to be transmitted.<br>32 bits data |

**RKI2C_TXDATA6**

Address: Operational Base + offset (0x0118)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | txdata6<br>Data6 to be transmitted.<br>32 bits data |

**RKI2C_TXDATA7**

Address: Operational Base + offset (0x011C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | txdata7<br>Data7 to be transmitted.<br>32 bits data |

**RKI2C_RXDATA0**

Address: Operational Base + offset (0x0200)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | rxdata0<br>Data0 received.<br>32 bits data |

**RKI2C_RXDATA1**

Address: Operational Base + offset (0x0204)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | rxdata1<br>Data1 received.<br>32 bits data |

**RKI2C_RXDATA2**

Rockchip Confidencial

Address: Operational Base + offset (0x0208)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | rxdata2<br>Data2 received.<br>32 bits data |

**RKI2C_RXDATA3**

Address: Operational Base + offset (0x020C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | rxdata3<br>Data3 received.<br>32 bits data |

**RKI2C_RXDATA4**

Address: Operational Base + offset (0x0210)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | rxdata4<br>Data4 received.<br>32 bits data |

**RKI2C_RXDATA5**

Address: Operational Base + offset (0x0214)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | rxdata5<br>Data5 received.<br>32 bits data |

**RKI2C_RXDATA6**

Address: Operational Base + offset (0x0218)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | rxdata6<br>Data6 received.<br>32 bits data |

**RKI2C_RXDATA7**

Address: Operational Base + offset (0x021C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | rxdata7<br>Data7 received.<br>32 bits data |

**RKI2C_ST**

Address: Operational Base + offset (0x0220)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RO | 0x0 | scl_st<br>SCL status.<br>1'b0: SCL status low.<br>1'b0: SCL status high. |
| 0 | RO | 0x0 | sda_st<br>SDA status.<br>1'b0: SDA status low.<br>1'b0: SDA status high. |

**RKI2C_DBGCTRL**

Rockchip Confidencial

Address: Operational Base + offset (0x0224)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:15 | RO | 0x00000 | reserved |
| 14 | RW | 0x0 | h0_check_scl<br>1'b0: Check if scl been pull down by slave at the whole SCL_HIGH.<br>1'b1: Check if scl been pull down by slave only at the h0 of SCL_HIGH(SCL_HIGH including h0~h7). |
| 13 | RW | 0x0 | nak_release_scl<br>1'b0: Hold scl as low when recieved nack.<br>1'b1: Release scl as high when recieved nack. |
| 12 | RW | 0x0 | flt_en<br>SCL edage glitch filter enable.<br>1'b0: Disable<br>1'b1: Enable |
| 11:8 | RW | 0x0 | slv_hold_scl_th<br>Slave hold scl threshold = slv_hold_scl_db * Tclk_i2c. |
| 7:4 | RW | 0x0 | flt_r<br>Filter scl rising edge glitches of width less than flt_r * Tclk_i2c. |
| 3:0 | RW | 0x0 | flt_f<br>Filter scl falling edge glitches of width less than flt_f * Tclk_i2c. |

**RKI2C_CON1**

Address: Operational Base + offset (0x0228)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2 | RW | 0x0 | auto_stop_nak<br>Auto stop when i2c master recieved nak from slave.<br>Work when CON1[0]=1'b1.<br>1'b0: Do not auto stop when recieved nak.<br>1'b1: Auto stop when recieved nak. |
| 1 | RW | 0x0 | auto_stop_tx_end<br>Auto stop when i2c master tx end.<br>Work when CON1[0]=1'b1.<br>1'b0: Do not auto stop when tx end.<br>1'b1: Auto stop when tx end. |
| 0 | RW | 0x0 | auto_stop<br>Auto stop when i2c master recieved nak from slave or tx end.<br>1'b0: Do not auto stop when recieved nak or tx end.<br>1'b1: Auto stop when recieved nak or tx end. |

Rockchip Confidential

## 21.5

## 21.6 Interface Description

Table 21-1 I2C Interface Description

| Module pin | Direction | Pin name | IOMUX |
|---|---|---|---|
| I2C0_SCL_M0 | I/O | SPI2_MISO_M2/I2C0_SCL_M0/GPIO0_B3_z | PMU1_IOC_GPIO0B_IOMUX_SEL_L[15:12]=0x2 |
| I2C0_SDA_M0 | I/O | SPI2_MOSI_M2/I2C0_SDA_M0/GPIO0_A6_z | PMU1_IOC_GPIO0A_IOMUX_SEL_H[11:8]=0x2 |
| I2C0_SCL_M1 | I/O | GMAC0_MDIO/I2C0_SCL_M1/UART9_CTSN_M0/PWM6_M2/SPI3_MOSI_M0/GPIO4_C5_d | BUS_IOC_GPIO4C_IOMUX_SEL_H[7:4]=0x9 |
| I2C0_SDA_M1 | I/O | GMAC0_TXER/I2C0_SDA_M1/UART7_CTSN_M0/PWM7_IR_M3/SPI3_CLK_M0/GPIO4_C6_d | BUS_IOC_GPIO4C_IOMUX_SEL_H[11:8]=0x9 |
| I2C0_SCL_M2 | I/O | I2S1_SDO0_M1/CPU_BIG0_AVS/I2C0_SCL_M2/UART0_CTSN/UART1_TX_M2/HDMI_RX_SDA_M0/SPI0_CS0_M0/PCIE30X2_CLKREQN_M0/HDMI_TX0_CEC_M1/GPIO0_D1_u | PMU1_IOC_GPIO0D_IOMUX_SEL_L[7:4]=0x3 |
| I2C0_SDA_M2 | I/O | I2S1_SDO1_M1/I2C0_SDA_M2/UART1_RX_M2/HDMI_RX_SCL_M0/SPI3_MOSI_M2/PCIE30X2_WAKEN_M0/HDMI_TX1_CEC_M1/GPIO0_D2_u | PMU1_IOC_GPIO0D_IOMUX_SEL_L[11:8]=0x3 |
| I2C1_SCL_M0 | I/O | I2S1_MCLK_M1/JTAG_TCK_M2/I2C1_SCL_M0/UART2_TX_M0/PCIE30X1_1_CLKREQN_M0/GPIO0_B5_d | BUS_IOC_GPIO0B_IOMUX_SEL_H[7:4]=0x9<br>PMU2_IOC_GPIO0B_IOMUX_SEL_H[7:4]=0x8 |
| I2C1_SDA_M0 | I/O | I2S1_SCLK_M1/JTAG_TMS_M2/I2C1_SDA_M0/UART2_RX_M0/PCIE30X1_1_WAKEN_M0/GPIO0_B6_d | BUS_IOC_GPIO0B_IOMUX_SEL_H[11:8]=0x9<br>PMU2_IOC_GPIO0B_IOMUX_SEL_H[11:8]=0x8 |
| I2C1_SCL_M1 | I/O | SPI2_CS1_M2/I2C1_SCL_M1/UART0_RX_M1/GPIO0_B0_z | PMU1_IOC_GPIO0B_IOMUX_SEL_L[3:0]=0x2 |
| I2C1_SDA_M1 | I/O | SPI2_CS0_M2/I2C1_SDA_M1/PWM5_M0/UART0_TX_M1/GPIO0_B1_z | PMU1_IOC_GPIO0B_IOMUX_SEL_L[7:4]=0x2 |
| I2C1_SCL_M2 | I/O | I2S1_SDO2_M1/PDM0_SDI2_M1/PWM3_IR_M0/I2C1_SCL_M2/CAN2_RX_M1/HDMI_TX0_SDA_M1/SPI3_CS0_M2/PCIE30X2_PERSTN_M0/SATA_CPDET/GPIO0_D4_u | BUS_IOC_GPIO0D_IOMUX_SEL_H[3:0]=0x9<br>PMU2_IOC_GPIO0D_IOMUX_SEL_H[3:0]=0x8 |
| I2C1_SDA_M2 | I/O | I2S1_SDO3_M1/CPU_BIG1_AVS/I2C1_SDA_M2/CAN2_TX_M1/HDMI_TX0_SCL_M1/SPI3_CS1_M2/SATA_MP_SWITCH/GPIO0_D5_u | BUS_IOC_GPIO0D_IOMUX_SEL_H[7:4]=0x9<br>PMU2_IOC_GPIO0D_IOMUX_SEL_H[7:4]=0x8 |
| I2C1_SCL_M3 | I/O | EMMC_D4/I2C1_SCL_M3/UART5_RX_M2/GPIO2_D4_u | BUS_IOC_GPIO2D_IOMUX_SEL_H[3:0]=0x9 |

Rockchip Confidential

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Module pin | Direction | Pin name | IOMUX |
|---|---|---|---|
| I2C1_SDA_M3 | I/O | EMMC_D5/I2C1_SDA_M3/UART5_TX_M2/GPIO2_D5_u | BUS_IOC_GPIO2D_IOMUX_SEL_H[7:4]=0x9 |
| I2C1_SCL_M4 | I/O | I2S0_SDO3/I2S0_SDI2/PDM0_SDI2_M0/I2C1_SCL_M4/UART4_TX_M0/PWM0_M1/SPI1_CLK_M2/GPIO1_D2_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[11:8]=0x9 |
| I2C1_SDA_M4 | I/O | I2S0_SDI1/PDM0_SDI3_M0/I2C1_SDA_M4/UART4_RX_M0/PWM1_M1/SPI1_CS0_M2/GPIO1_D3_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[15:12]=0x9 |
| I2C2_SCL_M0 | I/O | I2S1_LRCK_M1/PWM0_M0/I2C2_SCL_M0/CAN0_TX_M0/SPI0_CS1_M0/PCIE30X1_1_PERSTN_M0/GPIO0_B7_d | BUS_IOC_GPIO0B_IOMUX_SEL_H[15:12]=0x9<br>PMU2_IOC_GPIO0B_IOMUX_SEL_H[15:12]=0x8 |
| I2C2_SDA_M0 | I/O | PDM0_CLK0_M1/PWM1_M0/I2C2_SDA_M0/CAN0_RX_M0/SPI0_MOSI_M0/PCIE30X1_0_CLKREQN_M0/GPIO0_C0_d | BUS_IOC_GPIO0C_IOMUX_SEL_L[3:0]=0x9<br>PMU2_IOC_GPIO0C_IOMUX_SEL_L[3:0]=0x8 |
| I2C2_SCL_M1 | I/O | GMAC0_RXD0/I2C2_SCL_M1/UART1_CTSN_M0/SPI1_MISO_M0/GPIO2_C1_d | BUS_IOC_GPIO2C_IOMUX_SEL_L[7:4]=0x9 |
| I2C2_SDA_M1 | I/O | GMAC0_TXEN/I2S2_LRCK_M0/I2C2_SDA_M1/UART1_RTSN_M0/SPI1_CLK_M0/GPIO2_C0_d | BUS_IOC_GPIO2C_IOMUX_SEL_L[3:0]=0x9 |
| I2C2_SCL_M2 | I/O | EMMC_RSTN/I2C2_SCL_M2/UART5_RTSN_M1/GPIO2_A3_d | BUS_IOC_GPIO2A_IOMUX_SEL_L[15:12]=0x9 |
| I2C2_SDA_M2 | I/O | EMMC_DATA_STROBE/I2C2_SDA_M2/UART5_CTSN_M1/GPIO2_A2_d | BUS_IOC_GPIO2A_IOMUX_SEL_L[11:8]=0x9 |
| I2C2_SCL_M3 | I/O | I2S0_LRCK/I2C2_SCL_M3/UART4_RTSN/GPIO1_C5_d | BUS_IOC_GPIO1C_IOMUX_SEL_H[7:4]=0x9 |
| I2C2_SDA_M3 | I/O | PDM0_CLK1_M0/I2C2_SDA_M3/PWM11_IR_M2/SPI4_CS1_M0/GPIO1_C4_d | BUS_IOC_GPIO1C_IOMUX_SEL_H[3:0]=0x9 |
| I2C2_SCL_M4 | I/O | PCIE30X1_1_WAKEN_M2/DP1_HPDIN_M2/SATA1_ACT_LED_M1/I2C2_SCL_M4/UART6_TX_M1/SPI4_MOSI_M2/GPIO1_A1_d | BUS_IOC_GPIO1A_IOMUX_SEL_L[7:4]=0x9 |
| I2C2_SDA_M4 | I/O | PCIE30X1_1_CLKREQN_M2/DP0_HPDIN_M2/I2C2_SDA_M4/UART6_RX_M1/SPI4_MISO_M2/GPIO1_A0_d | BUS_IOC_GPIO1A_IOMUX_SEL_L[3:0]=0x9 |
| I2C3_SCL_M0 | I/O | I2C3_SCL_M0/UART3_TX_M0/SPI4_MOSI_M0/GPIO1_C1_z | BUS_IOC_GPIO1C_IOMUX_SEL_L[7:4]=0x9 |
| I2C3_SDA_M0 | I/O | I2C3_SDA_M0/UART3_RX_M0/SPI4_MISO_M0/GPIO1_C0_z | BUS_IOC_GPIO1C_IOMUX_SEL_L[3:0]=0x9 |
| I2C3_SCL_M1 | I/O | GMAC1_PTP_REF_CLK/HDMI_TX1_HPD_M1/I2C3_SCL_M1/SPI1_MOSI_M1/GPIO3_B7_d | BUS_IOC_GPIO3B_IOMUX_SEL_H[15:12]=0x9 |
| I2C3_SDA_M1 | I/O | GMAC1_PPSTRIG/I2C3_SDA_M1/UART7_TX_M1/SPI1_MISO_M1/GPIO3_C0_d | BUS_IOC_GPIO3C_IOMUX_SEL_L[3:0]=0x9 |
| I2C3_SCL_M2 | I/O | CIF_D4/BT1120_D4/PCIE30X1_0_WAKEN_M1/I2C3_SCL_M2/UART0_RX_M2/SPI2_MISO_M1/GPIO4_A4_d | BUS_IOC_GPIO4A_IOMUX_SEL_H[3:0]=0x9 |

Rockchip Confidential

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Module pin | Direction | Pin name | IOMUX |
|---|---|---|---|
| I2C3_SDA_M2 | I/O | CIF_D5/BT1120_D5/I2S1_SDI0_M0/PCIE30X1_0_PERSTN_M1/I2C3_SDA_M2/UART3_TX_M2/SPI2_MOSI_M1/GPIO4_A5_d | BUS_IOC_GPIO4A_IOMUX_SEL_H[7:4]=0x9 |
| I2C3_SCL_M3 | I/O | GMAC0_TXD3/SDIO_CMD_M0/I2C3_SCL_M3/GPIO2_B2_u | BUS_IOC_GPIO2B_IOMUX_SEL_L[11:8]=0x9 |
| I2C3_SDA_M3 | I/O | GMAC0_TXCLK/SDIO_CLK_M0/FSPI_CLK_M1/I2C3_SDA_M3/GPIO2_B3_d | BUS_IOC_GPIO2B_IOMUX_SEL_L[15:12]=0x9 |
| I2C3_SCL_M4 | I/O | SDMMC_D0/PDM1_SDI3_M0/JTAG_TCK_M1/I2C3_SCL_M4/UART2_TX_M1/PWM8_M1/GPIO4_D0_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[3:0]=0x9 |
| I2C3_SDA_M4 | I/O | SDMMC_D1/PDM1_SDI2_M0/JTAG_TMS_M1/I2C3_SDA_M4/UART2_RX_M1/PWM9_M1/GPIO4_D1_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[7:4]=0x9 |
| I2C4_SCL_M0 | I/O | ETH1_REFCLKO_25M/MIPI_CAMERA1_CLK_M1/I2C4_SCL_M0/GPIO3_A6_d | BUS_IOC_GPIO3A_IOMUX_SEL_H[11:8]=0x9 |
| I2C4_SDA_M0 | I/O | GMAC1_RXCLK/SDIO_CLK_M1/MIPI_CAMERA0_CLK_M1/FSPI_CLK_M2/I2C4_SDA_M0/UART8_CTSN_M1/GPIO3_A5_d | BUS_IOC_GPIO3A_IOMUX_SEL_H[7:4]=0x9 |
| I2C4_SCL_M1 | I/O | GMAC0_PPSTRING/FSPI_CS1N_M1/HDMI_TX1_SCL_M0/I2C4_SCL_M1/UART7_TX_M0/GPIO2_B5_u | BUS_IOC_GPIO2B_IOMUX_SEL_H[7:4]=0x9 |
| I2C4_SDA_M1 | I/O | GMAC0_PTP_REFCLK/FSPI_CS0N_M1/HDMI_TX1_SDA_M0/I2C4_SDA_M1/UART7_RX_M0/GPIO2_B4_u | BUS_IOC_GPIO2B_IOMUX_SEL_H[3:0]=0x9 |
| I2C4_SCL_M2 | I/O | I2S1_SDI0_M1/GPU_AVS/UART0_TX_M0/I2C4_SCL_M2/DP1_HPDIN_M1/PWM4_M0/PCIE30X1_0_PERSTN_M0/GPIO0_C5_u | BUS_IOC_GPIO0C_IOMUX_SEL_H[7:4]=0x9<br>PMU2_IOC_GPIO0C_IOMUX_SEL_H[7:4]=0x8 |
| I2C4_SDA_M2 | I/O | PDM0_CLK1_M1/PWM2_M0/UART0_RX_M0/I2C4_SDA_M2/DP0_HPDIN_M1/PCIE30X1_0_WAKEN_M0/GPIO0_C4_d | BUS_IOC_GPIO0C_IOMUX_SEL_H[3:0]=0x9<br>PMU2_IOC_GPIO0C_IOMUX_SEL_H[3:0]=0x8 |
| I2C4_SCL_M3 | I/O | HDMI_TX1_SDA_M2/I2C4_SCL_M3/UART6_CTSN_M1/PWM1_M2/SPI4_CS0_M2/GPIO1_A3_d | BUS_IOC_GPIO1A_IOMUX_SEL_L[15:12]=0x9 |
| I2C4_SDA_M3 | I/O | VOP_POST_EMPTY/I2C4_SDA_M3/UART6_RTSN_M1/PWM0_M2/SPI4_CLK_M2/GPIO1_A2_d | BUS_IOC_GPIO1A_IOMUX_SEL_L[11:8]=0x9 |
| I2C4_SCL_M4 | I/O | I2S0_SDO0/I2C4_SCL_M4/UART4_CTSN/GPIO1_C7_d | BUS_IOC_GPIO1C_IOMUX_SEL_H[15:12]=0x9 |
| I2C4_SDA_M4 | I/O | PDM0_CLK0_M0/I2C4_SDA_M4/PWM15_IR_M2/GPIO1_C6_d | BUS_IOC_GPIO1C_IOMUX_SEL_H[11:8]=0x9 |
| I2C5_SCL_M0 | I/O | CIF_D11/PCIE20X1_2_CLKREQN_M0/HDMI_TX0_SCL_M2/I2C5_SCL_M0/SPI3_MOSI_M3/GPIO3_C7_u | BUS_IOC_GPIO3C_IOMUX_SEL_H[15:12]=0x9 |
| I2C5_SDA_M0 | I/O | CIF_D12/PCIE20X1_2_WAKEN_M0/HDMI_TX0_SDA_M2/I2C5_SDA_M0/UART4_RX_M1/PWM8_M2/SPI3_CLK_M3/GPIO3_D0_u | BUS_IOC_GPIO3D_IOMUX_SEL_L[3:0]=0x9 |
| I2C5_SCL_M1 | I/O | BT1120_D12/PCIE30X4_PERSTN_M1/HDMI_RX_HPDOUT_M0/SATA0_ACT_LED_M0/I2C5_SCL_M1/PWM13_M1/SPI3_MOSI_M1/GPIO4_B6_d | BUS_IOC_GPIO4B_IOMUX_SEL_H[11:8]=0x9 |

Rockchip Confidential

| Module pin | Direction | Pin name | IOMUX |
|---|---|---|---|
| I2C5_SDA_M1 | I/O | BT1120_D13/PCIE20X1_2_CLKREQN_M1/HDMI_TX0_SCL_M0/I2C5_SDA_M1/SPI3_CLK_M1/GPIO4_B7_u | BUS_IOC_GPIO4B_IOMUX_SEL_H[15:12]=0x9 |
| I2C5_SCL_M2 | I/O | CIF_D6/BT1120_D6/I2S1_SDI1_M0/PCIE30X2_CLKREQN_M1/I2C5_SCL_M2/UART3_RX_M2/SPI2_CLK_M1/GPIO4_A6_d | BUS_IOC_GPIO4A_IOMUX_SEL_H[11:8]=0x9 |
| I2C5_SDA_M2 | I/O | CIF_D7/BT1120_D7/I2S1_SDI2_M0/PCIE30X2_WAKEN_M1/I2C5_SDA_M2/SPI2_CS0_M1/GPIO4_A7_d | BUS_IOC_GPIO4A_IOMUX_SEL_H[15:12]=0x9 |
| I2C5_SCL_M3 | I/O | MIPI_CAMERA1_CLK_M0/SPDIF0_TX_M0/PCIE30X2_WAKEN_M3/HDMI_RX_HPDOUT_M2/I2C5_SCL_M3/UART1_TX_M1/GPIO1_B6_d | BUS_IOC_GPIO1B_IOMUX_SEL_H[11:8]=0x9 |
| I2C5_SDA_M3 | I/O | MIPI_CAMERA2_CLK_M0/SPDIF1_TX_M0/PCIE30X2_PERSTN_M3/HDMI_RX_CEC_M2/SATA2_ACT_LED_M1/I2C5_SDA_M3/UART1_RX_M1/PWM13_M2/GPIO1_B7_u | BUS_IOC_GPIO1B_IOMUX_SEL_H[15:12]=0x9 |
| I2C5_SCL_M4 | I/O | GMAC0_TXD0/I2S2_MCLK_M0/I2C5_SCL_M4/UART1_RX_M0/GPIO2_B6_d | BUS_IOC_GPIO2B_IOMUX_SEL_H[11:8]=0x9 |
| I2C5_SDA_M4 | I/O | GMAC0_TXD1/I2S2_SCLK_M0/I2C5_SDA_M4/UART1_TX_M0/GPIO2_B7_d | BUS_IOC_GPIO2B_IOMUX_SEL_H[15:12]=0x9 |
| I2C6_SCL_M0 | I/O | I2S1_SDI3_M1/PDM0_SDI1_M1/I2C6_SCL_M0/UART1_CTSN_M2/PWM7_IR_M0/SPI3_MISO_M2/PCIE30X4_PERSTN_M0/GPIO0_D0_d | BUS_IOC_GPIO0D_IOMUX_SEL_L[3:0]=0x9 |
| I2C6_SDA_M0 | I/O | I2S1_SDI2_M1/PDM0_SDI0_M1/I2C6_SDA_M0/UART1_RTSN_M2/PWM6_M0/SPI0_MISO_M0/PCIE30X4_WAKEN_M0/GPIO0_C7_d | BUS_IOC_GPIO0C_IOMUX_SEL_H[15:12]=0x9 |
| I2C6_SCL_M1 | I/O | I2S0_SCLK/I2C6_SCL_M1/UART3_CTSN/PWM7_IR_M2/SPI4_CS0_M0/GPIO1_C3_d | BUS_IOC_GPIO1C_IOMUX_SEL_L[15:12]=0x9 |
| I2C6_SDA_M1 | I/O | I2S0_MCLK/I2C6_SDA_M1/UART3_RTSN/PWM3_IR_M2/SPI4_CLK_M0/GPIO1_C2__d | BUS_IOC_GPIO1C_IOMUX_SEL_L[11:8]=0x9 |
| I2C6_SCL_M2 | I/O | ETH0_REFCLKO_25M/I2S2_SDI_M0/I2C6_SCL_M2/SPI1_CS0_M0/GPIO2_C3_d | BUS_IOC_GPIO2C_IOMUX_SEL_L[15:12]=0x9 |
| I2C6_SDA_M2 | I/O | GMAC0_RXD1/I2C6_SDA_M2/UART9_TX_M0/SPI1_MOSI_M0/GPIO2_C2_d | BUS_IOC_GPIO2C_IOMUX_SEL_L[11:8]=0x9 |
| I2C6_SCL_M3 | I/O | MIPI_CAMERA0_CLK_M0/SPDIF1_TX_M1/I2S1_SDO0_M0/PCIE30X1_0_BUTTON_RSTN/SATA2_ACT_LED_M0/I2C6_SCL_M3/UART8_RX_M0/SPI0_CS1_M1/GPIO4_B1_u | BUS_IOC_GPIO4B_IOMUX_SEL_L[7:4]=0x9 |
| I2C6_SDA_M3 | I/O | CIF_CLKIN/BT1120_CLKOUT/I2S1_SDI3_M0/PCIE30X2_PERSTN_M1/I2C6_SDA_M3/UART8_TX_M0/SPI2_CS1_M1/GPIO4_B0_d | BUS_IOC_GPIO4B_IOMUX_SEL_L[3:0]=0x9 |
| I2C6_SCL_M4 | I/O | GMAC1_TXD3/SDIO_D1_M1/I2S3_SCLK/AUDDSM_LN/FSPI_D1_M2/I2C6_SCL_M4/PWM11_IR_M0/SPI4_MOSI_M1/GPIO3_A1_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[7:4]=0x9 |
| I2C6_SDA_M4 | I/O | GMAC1_TXD2/SDIO_D0_M1/I2S3_MCLK/FSPI_D0_M2/I2C6_SDA_M4/PWM10_M0/SPI4_MISO_M1/GPIO3_A0_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[3:0]=0x9 |
| I2C7_SCL_M0 | I/O | I2S0_SDO1/I2C7_SCL_M0/UART6_TX_M2/SPI1_MISO_M2/GPIO1_D0_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[3:0]=0x9 |
| I2C7_SDA_M0 | I/O | I2S0_SDO2/I2S0_SDI3/PDM0_SDI1_M0/I2C7_SDA_M0/UART6_RX_M2/SPI1_MOSI_M2/GPIO1_D1_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[7:4]=0x9 |
| I2C7_SCL_M1 | I/O | GMAC0_MCLKINOUT/I2S2_SDO_M0/I2C7_SCL_M1/PWM4_M1/SPI3_CS1_M0/GPIO4_C3_d | BUS_IOC_GPIO4C_IOMUX_SEL_L[15:12]=0x9 |

Rockchip Confidential

| Module pin | Direction | Pin name | IOMUX |
|---|---|---|---|
| I2C7_SDA_M1 | I/O | GMAC0_MDC/I2C7_SDA_M1/UART9_RTSN_M0/PWM5_M2/SPI3_MISO_M0/GPIO4_C4_d | BUS_IOC_GPIO4C_IOMUX_SEL_H[3:0]=0x9 |
| I2C7_SCL_M2 | I/O | CIF_D14/PCIE30X2_CLKREQN_M2/HDMI_RX_SCL_M1/I2C7_SCL_M2/UART9_RTSN_M2/SPI0_MOSI_M3/GPIO3_D2_d | BUS_IOC_GPIO3D_IOMUX_SEL_L[11:8]=0x9 |
| I2C7_SDA_M2 | I/O | CIF_D15/PCIE30X2_WAKEN_M2/HDMI_RX_SDA_M1/I2C7_SDA_M2/UART9_CTSN_M2/PWM10_M2/SPI0_CLK_M3/GPIO3_D3_d | BUS_IOC_GPIO3D_IOMUX_SEL_L[15:12]=0x9 |
| I2C7_SCL_M3 | I/O | CIF_HREF/BT1120_D8/I2S1_SDO1_M0/PCIE30X1_1_BUTTON_RSTN/I2C7_SCL_M3/UART8_RTSN_M0/PWM14_M1/SPI0_CS0_M1/CAN1_RX_M1/GPIO4_B2_u | BUS_IOC_GPIO4B_IOMUX_SEL_L[11:8]=0x9 |
| I2C7_SDA_M3 | I/O | CIF_VSYNC/BT1120_D9/I2S1_SDO2_M0/PCIE20X1_2_BUTTON_RSTN/I2C7_SDA_M3/UART8_CTSN_M0/PWM15_IR_M1/CAN1_TX_M1/GPIO4_B3_u | BUS_IOC_GPIO4B_IOMUX_SEL_L[15:12]=0x9 |
| I2C8_SCL_M0 | I/O | SDMMC_D2/PDM1_SDI1_M0/JTAG_TCK_M0/I2C8_SCL_M0/UART5_CTSN_M0/GPIO4_D2_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[11:8]=0x9 |
| I2C8_SDA_M0 | I/O | SDMMC_D3/PDM1_SDI0_M0/JTAG_TMS_M0/I2C8_SDA_M0/UART5_RTSN_M0/PWM10_M1/GPIO4_D3_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[15:12]=0x9 |
| I2C8_SCL_M1 | I/O | GMAC0_RXCLK/SDIO_D2_M0/FSPI_D2_M1/I2C8_SCL_M1/UART6_RTSN_M0/GPIO2_B0_u | BUS_IOC_GPIO2B_IOMUX_SEL_L[3:0]=0x9 |
| I2C8_SDA_M1 | I/O | GMAC0_TXD2/SDIO_D3_M0/FSPI_D3_M1/I2C8_SDA_M1/UART6_CTSN_M0/GPIO2_B1_u | BUS_IOC_GPIO2B_IOMUX_SEL_L[7:4]=0x9 |
| I2C8_SCL_M2 | I/O | MIPI_CAMERA3_CLK_M0/HDMI_RX_SCL_M2/I2C8_SCL_M2/UART1_RTSN_M1/PWM14_M2/GPIO1_D6_u | BUS_IOC_GPIO1D_IOMUX_SEL_H[11:8]=0x9 |
| I2C8_SDA_M2 | I/O | MIPI_CAMERA4_CLK_M0/PCIE30X2_CLKREQN_M3/HDMI_RX_SDA_M2/I2C8_SDA_M2/UART1_CTSN_M1/PWM15_IR_M3/GPIO1_D7_u | BUS_IOC_GPIO1D_IOMUX_SEL_H[15:12]=0x9 |
| I2C8_SCL_M3 | I/O | BT1120_D14/PCIE20X1_2_WAKEN_M1/HDMI_TX0_SDA_M0/I2C8_SCL_M3/SPI3_CS0_M1/GPIO4_C0_u | BUS_IOC_GPIO4C_IOMUX_SEL_L[3:0]=0x9 |
| I2C8_SDA_M3 | I/O | BT1120_D15/SPDIF1_TX_M2/PCIE20X1_2_PERSTN_M1/HDMI_TX0_CEC_M0/I2C8_SDA_M3/PWM6_M1/SPI3_CS1_M1/GPIO4_C1_d | BUS_IOC_GPIO4C_IOMUX_SEL_L[7:4]=0x9 |
| I2C8_SCL_M4 | I/O | GMAC1_MDC/MIPI_TE0/I2C8_SCL_M4/UART7_RTSN_M1/PWM14_M0/SPI1_CS0_M1/GPIO3_C2_d | BUS_IOC_GPIO3C_IOMUX_SEL_L[11:8]=0x9 |
| I2C8_SDA_M4 | I/O | GMAC1_MDIO/MIPI_TE1/I2C8_SDA_M4/UART7_CTSN_M1/PWM15_IR_M0/SPI1_CS1_M1/GPIO3_C3_d | BUS_IOC_GPIO3C_IOMUX_SEL_L[15:12]=0x9 |

Rockchip Confidential

Copyright 2022 © Rockchip Electronics Co., Ltd.

## 21.7 Application Notes

The I2C controller core operation flow chart below is to describe how the software configures and performs an I2C transaction through this I2C controller core. Descriptions are divided into 3 sections, transmit only mode, receive only mode, and mix mode. Users are strongly advised to follow:

- Transmit only mode (I2C_CON[1:0]=2'b00)

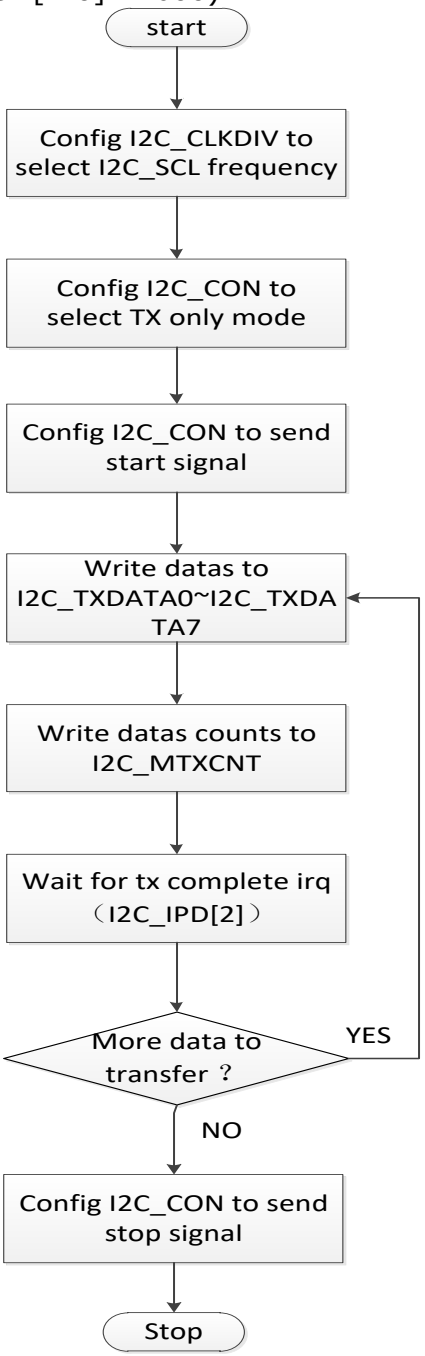



Fig. 21-6 I2C Flow chat for transmit only mode

Copyright 2022 © Rockchip Electronics Co., Ltd.

- Receive only mode (I2C_CON[1:0]=2'b10)

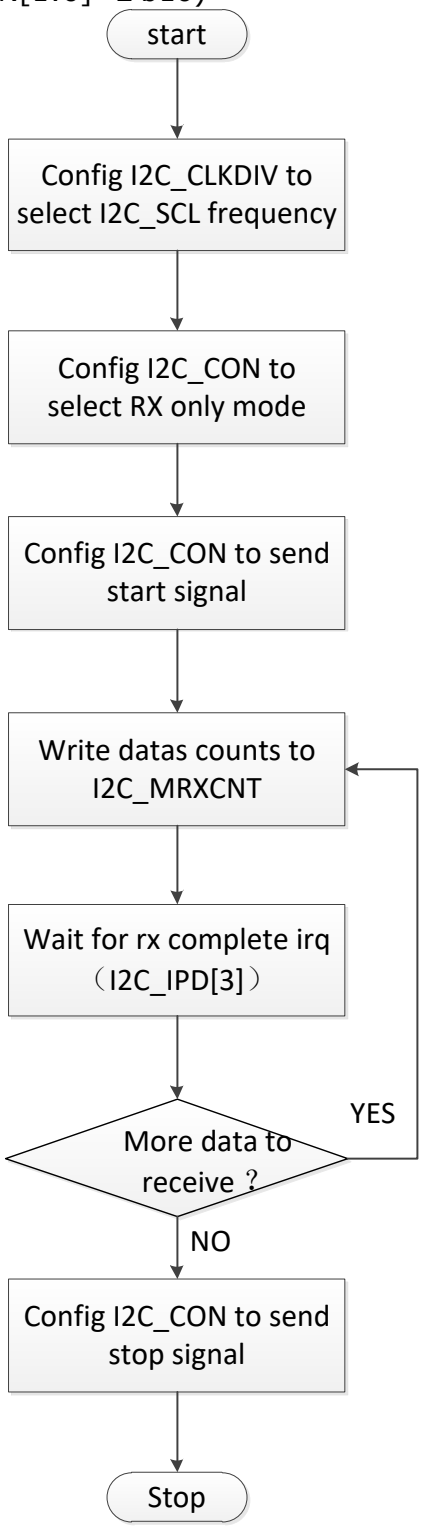



Fig. 21-7 I2C Flow chat for receive only mode

Copyright 2022 © Rockchip Electronics Co., Ltd.

- Mix mode (I2C_CON[1:0]=2'b01 or I2C_CON[1:0]=2'b11)

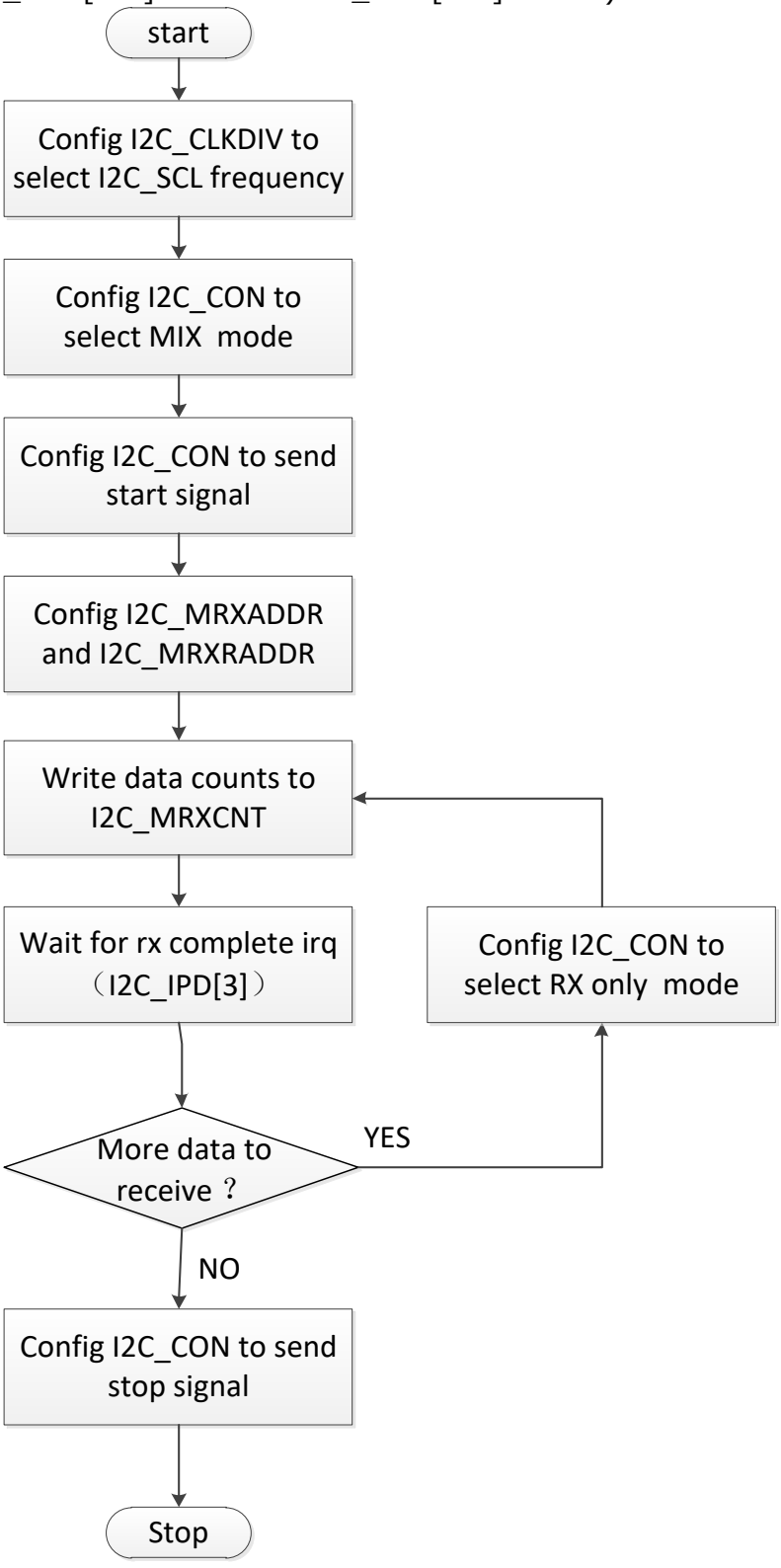



Fig. 21-8 I2C Flow chat for mix mode

Copyright 2022 © Rockchip Electronics Co., Ltd.

# Chapter 22 I2S

## 22.1 Overview

The I2S/PCM/TDM controller is designed for interfacing between the AHB bus and the I2S bus.
The I2S bus (Inter-IC sound bus) is a serial link for digital audio data transfer between devices in the system and is invented by Philips Semiconductor. Now it is widely used by many semiconductor manufacturers.
I2S bus is widely used in the devices such as ADC, DAC, DSP, CPU, etc. With the I2S interface, we can connect audio devices and the embedded SoC platform together and provide an audio interface solution for the system.

### 22.1.1 Features

There are nine I2S/PCM/TDM controllers and two I2S/PCM controllers embed in the system. I2S/PCM/TDM controllers support I2S format, PCM format and TDM format. While I2S/PCM controllers only support I2S format and PCM format. The nine I2S/PCM/TDM controllers are I2S0, I2S1, I2S4, I2S5, I2S6, I2S7, I2S8, I2S9 and I2S10. Remaining two I2S/PCM controllers are 2-channel I2S2 and I2S3.
Unless stated separately, all of the following features apply to I2S0~I2S10.

- Support eight internal 32-bit wide and 32-location deep FIFOs, four for transmitting and the others for receiving audio data for I2S0 and I2S1
- Support two internal 32-bit wide and 32-location deep FIFOs, one for transmitting and the other for receiving audio data for each I2S2 and I2S3
- Support four internal 32-bit wide and 32-location deep transmitting FIFOs for I2S4, I2S5, I2S6 and I2S8
- Support four internal 32-bit wide and 32-location deep receiving FIFOs for I2S7, I2S9 and I2S10
- Support AHB bus interface
- Support 16~32 bits audio data transfer
- Support master and slave mode for I2S0, I2S1, I2S2 and I2S3
- Support only master TX mode for I2S4, I2S5, I2S6 and I2S8
- Support only slave RX mode for I2S7, I2S9 and I2S10
- Support DMA handshaking interface and configurable DMA water level
- Support transmit FIFO empty, underflow, receive FIFO full, overflow interrupt and all interrupts can be masked
- Support configurable water level of transmit FIFO empty and receive FIFO full interrupt
- Support combined interrupt output
- Support 2-channel audio transmitting and receiving in PCM mode for I2S0, I2S1, I2S2 and I2S3
- Support 2-channel audio transmitting in PCM mode for I2S4, I2S5, I2S6 and I2S8
- Support 2-channel audio receiving in PCM mode for I2S7, I2S9 and I2S10
- Support 8-channel audio transmitting and receiving in I2S mode for I2S0 and I2S1
- Support 2-channel audio transmitting and receiving in I2S mode for I2S2 and I2S3
- Support 8-channel audio transmitting in I2S mode for I2S4, I2S5, I2S6 and I2S8
- Support 8-channel audio receiving in I2S mode for I2S7, I2S9 and I2S10
- Support up to 16-channel audio transmitting and receiving in TDM mode for I2S/PCM/TDM controllers
- Support up to 192kHz sample rate for I2S0, I2S1, I2S2, I2S3, I2S4 and I2S8
- Support up to 768kHz sample rate for I2S5, I2S6, I2S7, I2S9 and I2S10
- Support I2S normal, left and right justified mode serial audio data transfer
- Support PCM early, late1, late2, late3 mode serial audio data transfer
- Support TDM normal, 1/2 cycle left shift , 1 cycle left shift, 2 cycle left shift, right shift mode serial audio data transfer for I2S/PCM/TDM controllers
- Support MSB or LSB first serial audio data transfer
- Support 16 to 31 bit audio data left or right justified in 32-bit wide FIFO

Copyright 2022 © Rockchip Electronics Co., Ltd.

- Support two 16-bit audio data store together in one 32-bit wide location
- Support configurable SCLK and LRCK polarity
- Support a range of 16 to 32 programmable slot bit width in TDM mode for I2S/PCM/TDM controllers
- Support a range of 32 to 512 programmable frame width in TDM mode for I2S/PCM/TDM controllers
- Support a range of 32 to 256 programmable frame width in I2S/PCM mode for I2S/PCM/TDM controllers and I2S/PCM controllers except I2S4 and I2S8
- Support a range of 32 to 512 programmable frame width in I2S/PCM mode for I2S4 and I2S8

## 22.2 Block Diagram

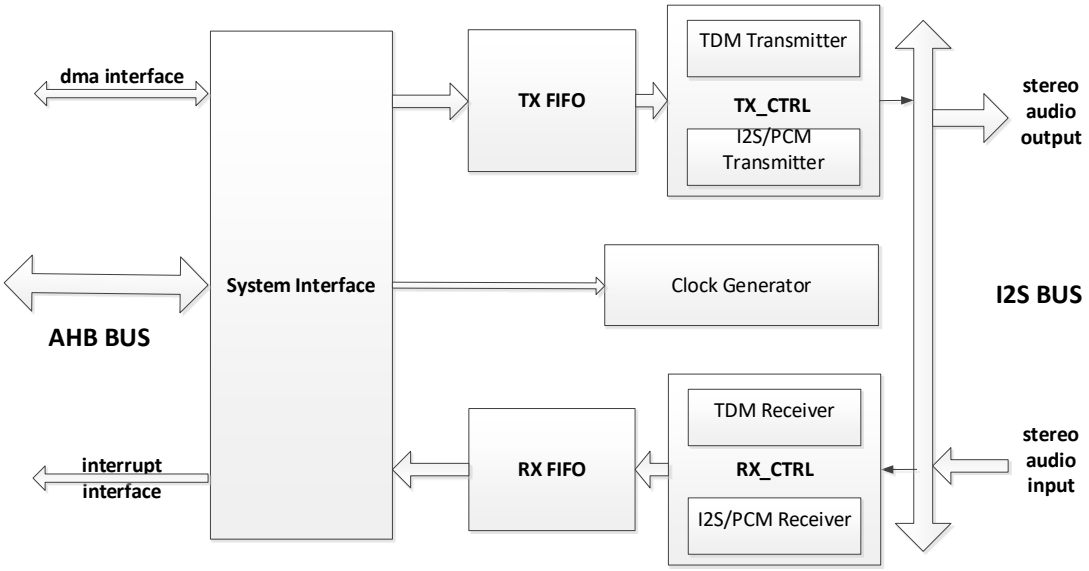



Fig. 22-1 I2S/PCM/TDM Controller (8-channel) Block Diagram

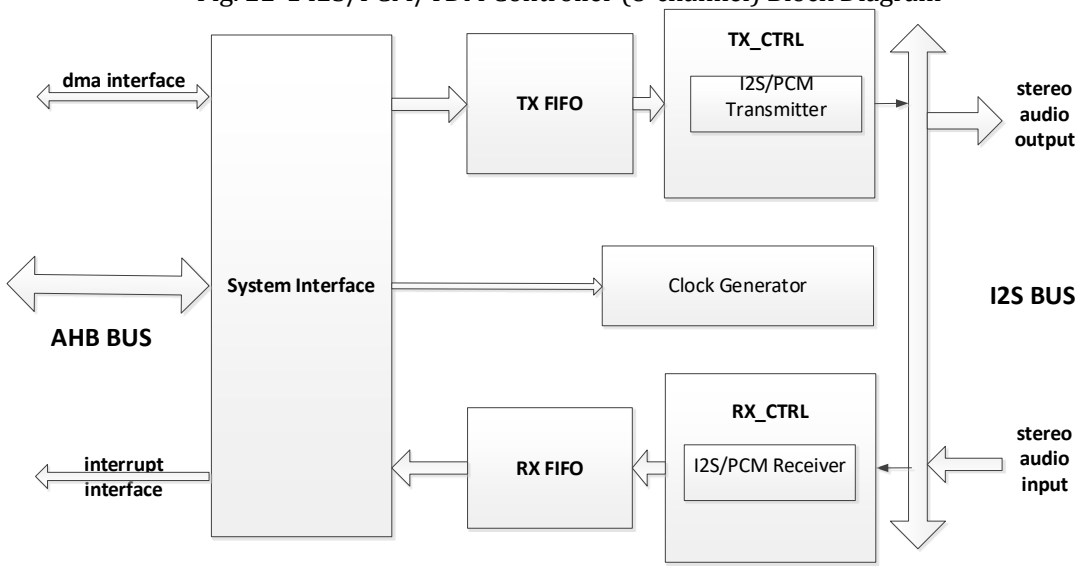



Fig. 22-2 I2S/PCM Controller (2-channel) Block Diagram

**System Interface**

The system interface implements the AHB slave operation. It contains not only control registers of transmitters and receiver inside but also interrupt and DMA handshaking interface.

**Clock Generator**

The Clock Generator implements clock generation function. By the divider of the module, the clock generator generates SCLK and LRCK to transmitter and receiver.

**TX_CTRL**

For I2S/PCM/TDM Controller, TX_CTRL includes TDM transmitter and I2S/PCM transmitter. While for I2S/PCM Controller, TX_CTRL only includes I2S/PCM transmitter. The Transmitters

implement transmission operation. The transmitters can act as either a master or a slave, with I2S, PCM or TDM mode surround serial audio interface.

**RX_CTRL**

For I2S/PCM/TDM Controller, RX_CTRL includes TDM receiver and I2S/PCM receiver. While for I2S/PCM Controller, RX_CTRL only includes I2S/PCM receiver. The Receiver implements receive operation. The receiver can act as either a master or a slave, with I2S, PCM or TDM mode stereo serial audio interface.

**TX FIFO**

The transmit FIFO is the buffer to store transmitted audio data. The size of one FIFO is 32bits x 32.

**RX FIFO**

The receive FIFO is the buffer to store received audio data. The size of one FIFO is 32bits x 32.

## 22.3 Function description

In the I2S/PCM/TDM or I2S/PCM controller, there are four types: transmitter-master & receiver-master; transmitter-master & receiver-slave; transmitter-slave & receiver-master; transmitter-slave & receiver-slave.

In broadcasting application, the I2S/PCM/TDM or I2S/PCM controller is used as a transmitter and external or internal audio CODEC is used as a receiver. In recording application, the I2S/PCM/TDM or I2S/PCM controller is used as a receiver and external or internal audio CODEC is used as a transmitter. Either the I2S/PCM/TDM or I2S/PCM controller or the audio CODEC can act as a master or a slave, but if one is master, the other must be slave.

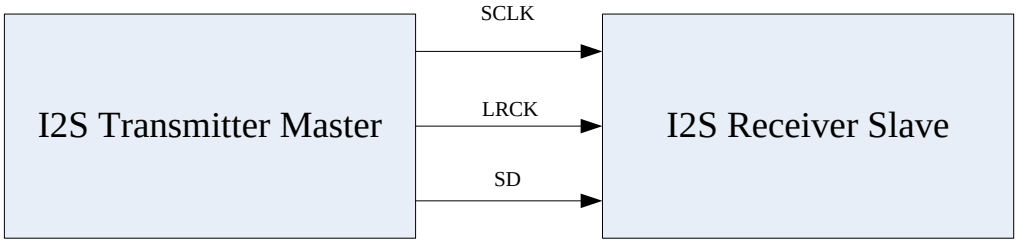



Fig. 22-3 I2S Transmitter-Master & Receiver-Slave Condition

When the transmitter acts as a master, it sends all signals to the receiver (the slave), and CPU controls when to send clock and data to the receiver. When acts as a slave, SD signal still goes from transmitter to receiver, but SCLK and LRCK signals are from the receiver (the master) to the transmitter. Based on three interface specifications, transmitting data should be ready before transmitter receives SCLK and LRCK signals. CPU should know when the receiver to initialize a transaction and when the transmitter to send data.

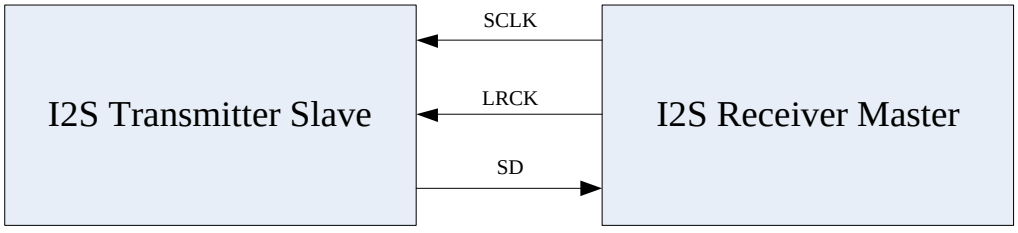



Fig. 22-4 I2S Transmitter-Slave & Receiver-Master Condition

When the receiver acts as a master, it sends SCLK and LRCK signals to the transmitter (the slave) and receives serial data. So CPU must tell the transmitter when to start a transaction for it to prepare transmitting data then start a transfer and send clock and channel-select signals. When the receiver acts as a slave, CPU should only do initial setting and wait for all signals and then start reading data.

Before transmitting or receiving data, CPU need do initial setting to the I2S register. These includes CPU settings, I2S interface registers settings, and maybe the embedded SoC platform settings. These registers must be set before starting data transfer.

Copyright 2022 © Rockchip Electronics Co., Ltd.

### 22.3.1 I2S Normal Mode

This is the waveform of I2S normal mode. For LRCK (i2s_lrck) signal, it goes low to indicate left channel and high to right channel. For SD (i2s_sdo, i2s_sdi) signal, it starts sending the first bit (MSB or LSB) one SCLK clock cycle after LRCK changes. The range of SD signal width is from 16 to 32bits.

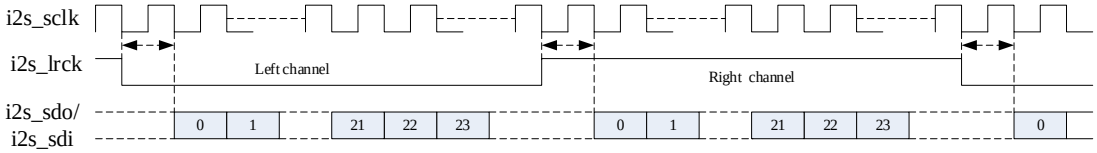



Fig. 22-5 I2S Normal Mode Timing Format

### 22.3.2 I2S Left Justified Mode

This is the waveform of I2S left justified mode. For LRCK (i2s_lrck) signal, it goes high to indicate left channel and low to right channel. For SD (i2s_sdo, i2s_sdi) signal, it starts sending the first bit (MSB or LSB) at the same time when LRCK changes. The range of SD signal width is from 16 to 32bits.

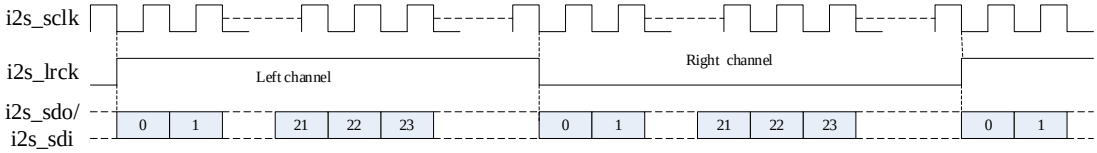



Fig. 22-6 I2S Left Justified Mode Timing Format

### 22.3.3 I2S Right Justified Mode

This is the waveform of I2S right justified mode. For LRCK (i2s_lrck) signal, it goes high to indicate left channel and low to right channel. For SD (i2s_sdo, i2s_sdi) signal, it transfers MSB or LSB first; but what is different from I2S normal or left justified mode, the last bit of the transferred data is aligned to the transition edge of the LRCK signal while one bit is transferred at one SCLK cycle. The range of SD signal width is from 16 to 32bits.

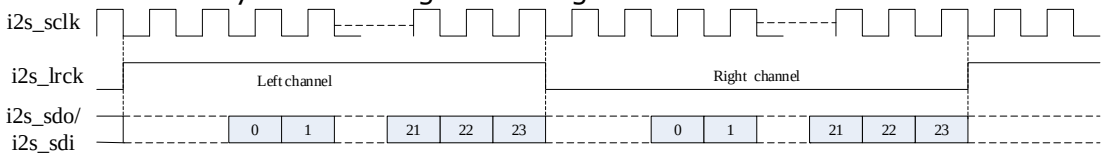



Fig. 22-7 I2S Right Justified Mode Timing Format

### 22.3.4 PCM Early Mode

This is the waveform of PCM early mode. For LRCK (i2s_lrck) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo, i2s_sdi) signal, it sends the first bit (MSB or LSB) at the same time when LRCK goes high. The range of SD signal width is from 16 to 32bits.

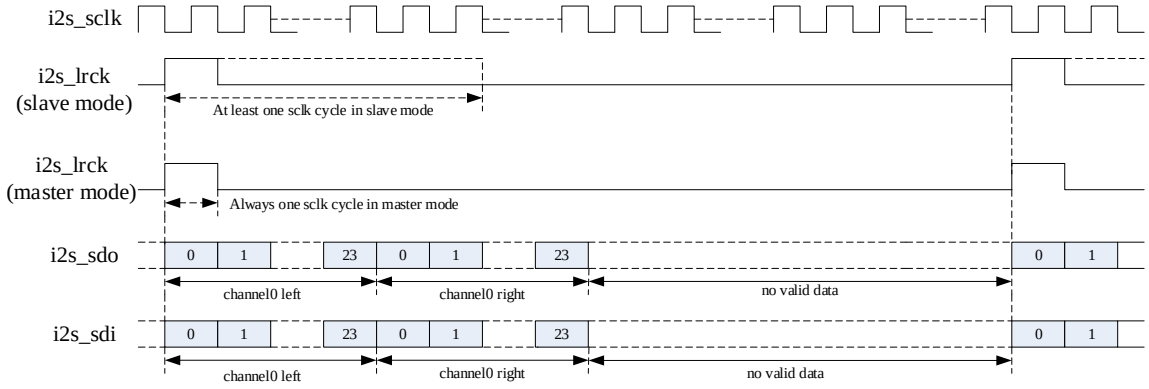



Fig. 22-8 PCM Early Mode Timing Format

### 22.3.5 PCM Late1 Mode

This is the waveform of PCM early mode. For LRCK (i2s_lrck) signal, it goes high to indicate

the start of a group of audio channels. For SD (i2s_sdo, i2s_sdi) signal, it sends the first bit (MSB or LSB) one SCLK clock cycle after LRCK goes high. The range of SD signal width is from 16 to 32bits.

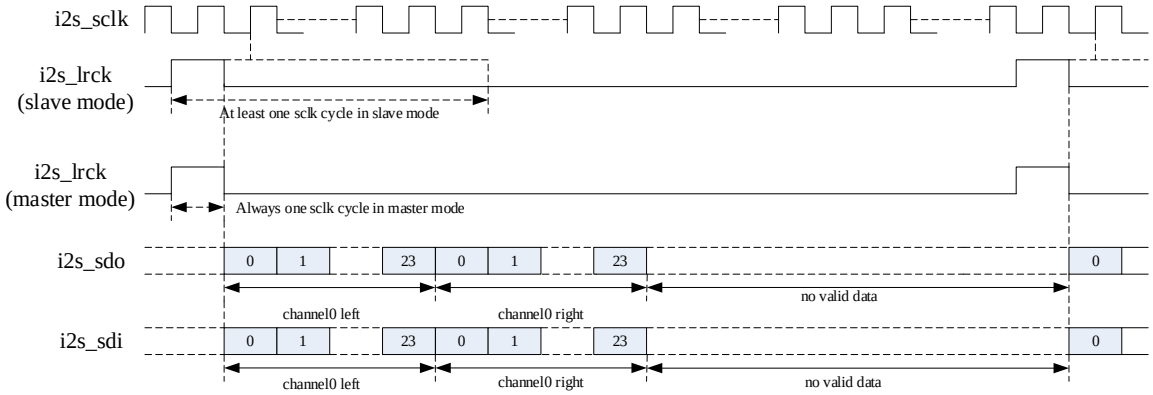



Fig. 22-9 PCM Late1 Mode Timing Format

## 22.3.6 PCM Late2 Mode

This is the waveform of PCM early mode. For LRCK (i2s_lrck) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo, i2s_sdi) signal, it sends the first bit(MSB or LSB) two SCLK clock cycles after LRCK goes high. The range of SD signal width is from 16 to 32bits.

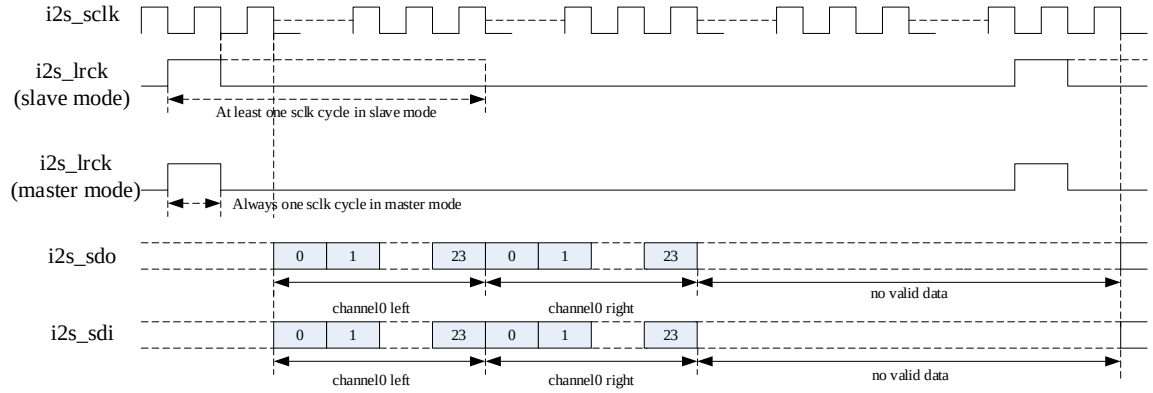



Fig. 22-10 PCM Late2 Mode Timing Format

## 22.3.7 PCM Late3 Mode

This is the waveform of PCM early mode. For LRCK (i2s_lrck) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo, i2s_sdi) signal, it sends the first bit (MSB or LSB) three SCLK clock cycles after LRCK goes high. The range of SD signal width is from 16 to 32bits.

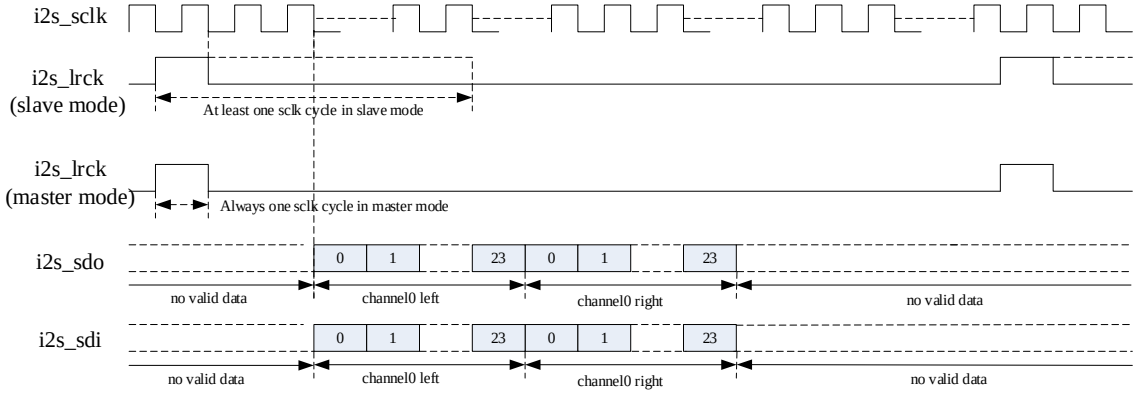



Fig. 22-11 PCM Late3 Mode Timing Format

## 22.3.8 TDM Normal Mode (PCM Format)

This is the waveform of TDM normal mode. For LRCK (i2s_lrck) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo, i2s_sdi) signal, it sends the first bit (MSB or LSB) on the second falling edge of SCLK after LRCK goes high. The range of SD signal width is from 16 to 32bits.

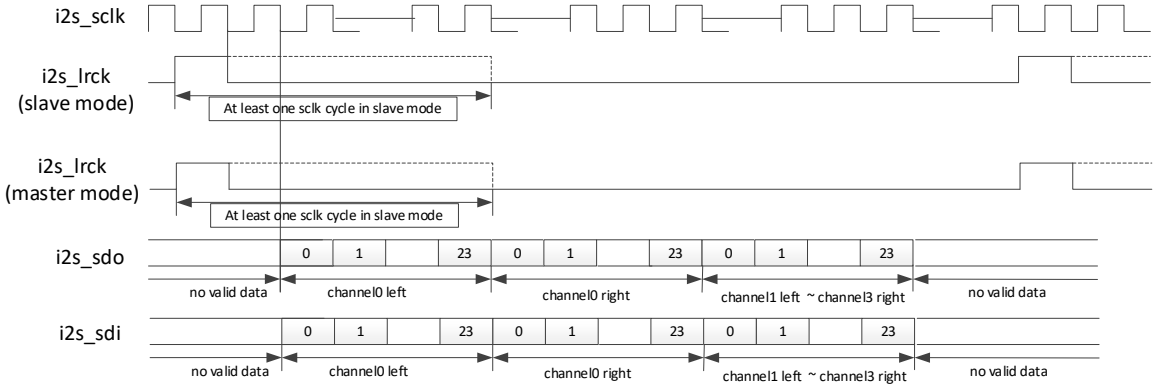



Fig. 22-12 TDM Normal Mode Timing Format (PCM Format)

## 22.3.9 TDM Left Shift Mode0 (PCM Format)

This is the waveform of PCM early mode. For LRCK (i2s_lrck) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo, i2s_sdi) signal, it sends the first bit (MSB or LSB) on the second rising edge of SCLK after LRCK goes high. The range of SD signal width is from 16 to 32bits.

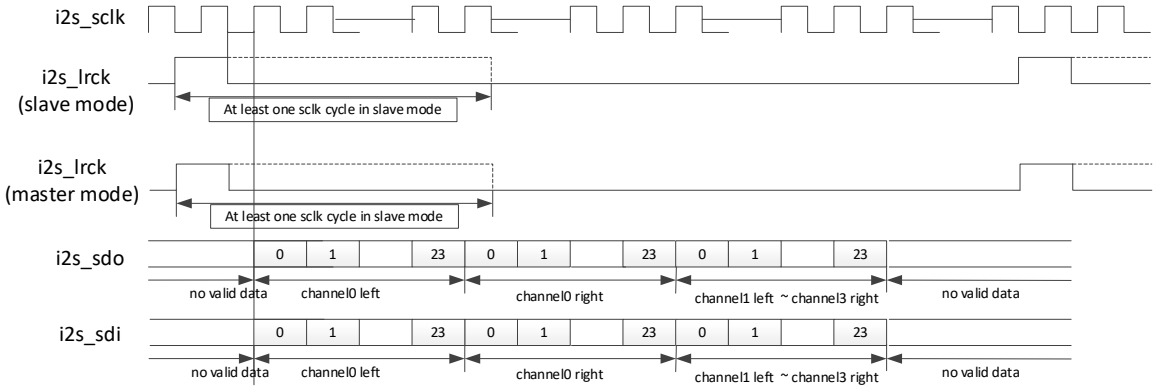



Fig. 22-13 TDM Left Shift Mode 0 Timing Format (PCM Format)

## 22.3.10 TDM Left Shift Mode1 (PCM Format)

This is the waveform of PCM early mode. For LRCK (i2s_lrck) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo, i2s_sdi) signal, it sends the first bit (MSB or LSB) on the first falling edge of SCLK after LRCK goes high. The range of SD signal width is from 16 to 32bits.

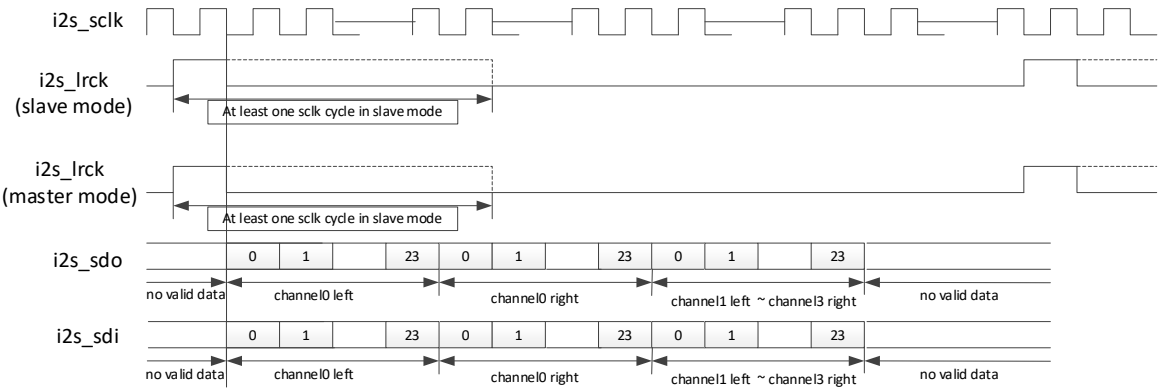



Fig. 22-14 TDM Left Shift Mode 1 Timing Format (PCM Format)

Copyright 2022 © Rockchip Electronics Co., Ltd. 

## 22.3.11 TDM Left Shift Mode2 (PCM Format)

This is the waveform of PCM early mode. For LRCK (i2s_lrck) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo, i2s_sdi) signal, it sends the first bit (MSB or LSB) on the first rising edge of SCLK after LRCK goes high. The range of SD signal width is from 16 to 32bits.

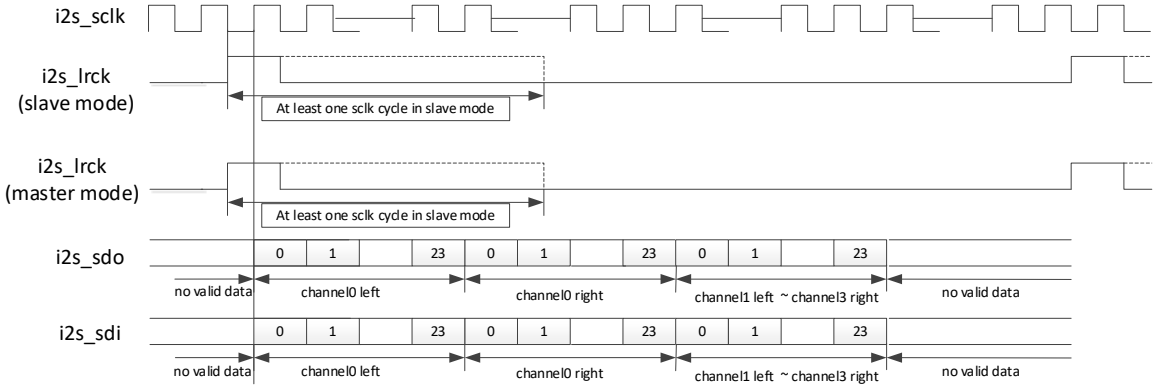



Fig. 22-15 TDM Left Shift Mode 2 Timing Format (PCM Format)

## 22.3.12 TDM Left Shift Mode3 (PCM Format)

This is the waveform of PCM early mode. For LRCK (i2s1_lrck) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo, i2s_sdi) signal, it sends the first bit (MSB or LSB) at the same time when LRCK goes high. The range of SD signal width is from 16 to 32bits.

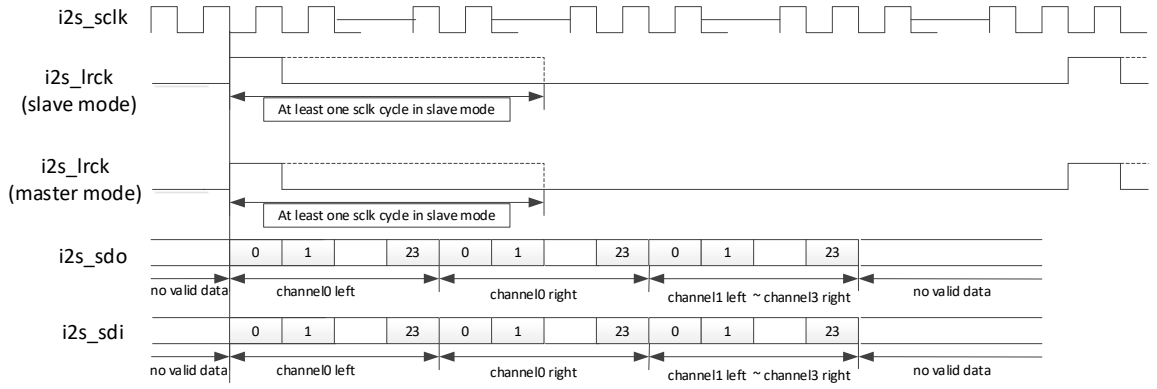
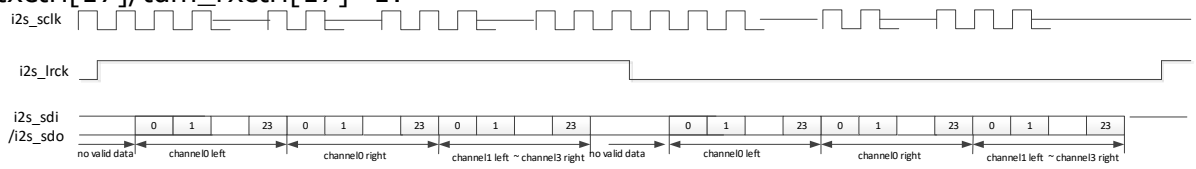



Fig. 22-16 TDM Left Shift Mode 3 Timing Format (PCM Format)

## 22.3.13 TDM Normal Mode (I2S Format)

This is the waveform of I2S normal mode. For SD (i2s_sdo, i2s_sdi) signal, it starts sending the first bit (MSB or LSB)on the first falling edge of SCLK after LRCK changes. The range of SD signal width is from 16 to 32bits.

tdm_txctrl[17]/tdm_rxctrl[17]=1:




tdm_txctrl[17]/tdm_rxctrl[17]=0:

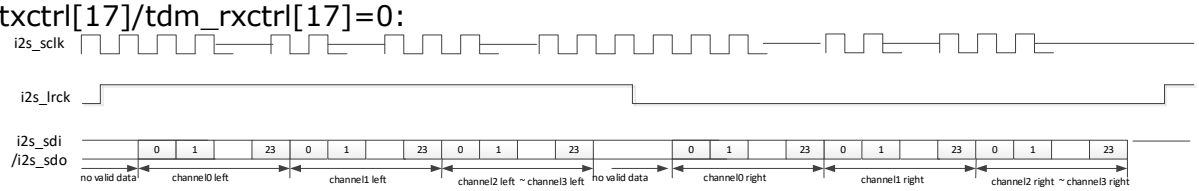



Fig. 22-17 TDM Normal Mode Timing Format (I2S Format)

Copyright 2022 © Rockchip Electronics Co., Ltd. 

### 22.3.14 TDM Left Justified Mode (I2S Format)

This is the waveform of I2S left justified mode. For SD (i2s_sdo, i2s_sdi) signal, it starts sending the first bit (MSB or LSB) at the same time when LRCK changes. The range of SD signal width is from 16 to 32bits.

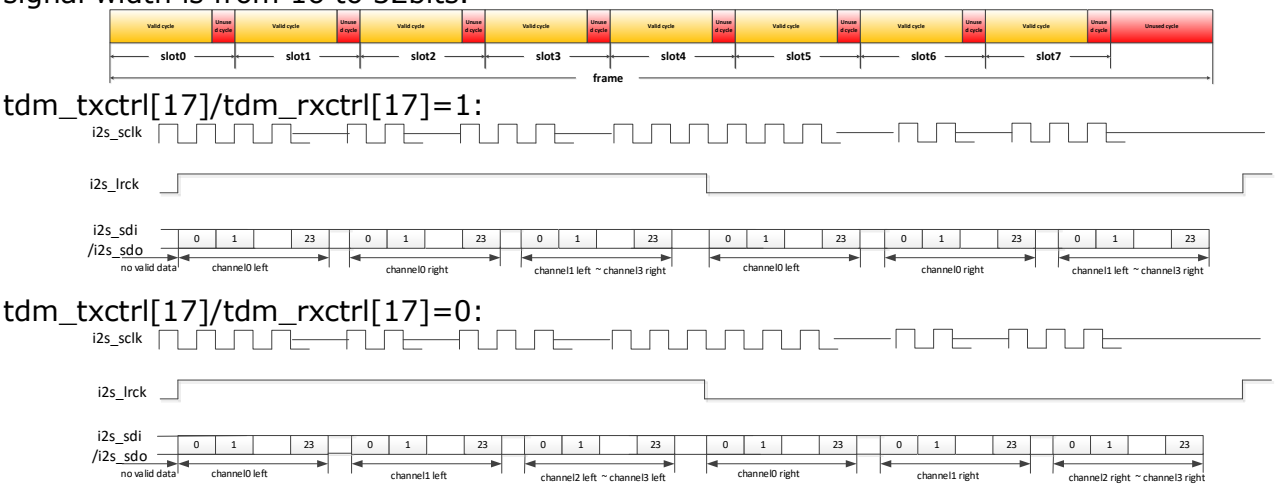



Fig. 22-18 TDM Left Justified Mode Timing Format (I2S Format)

### 22.3.15 TDM Right Justified Mode (I2S Format)

This is the waveform of I2S right justified mode. For SD (i2s_sdo, i2s_sdi) signal, it transfers MSB or LSB first; but what is different from I2S normal or left justified mode. The range of SD signal width is from 16 to 32bits.

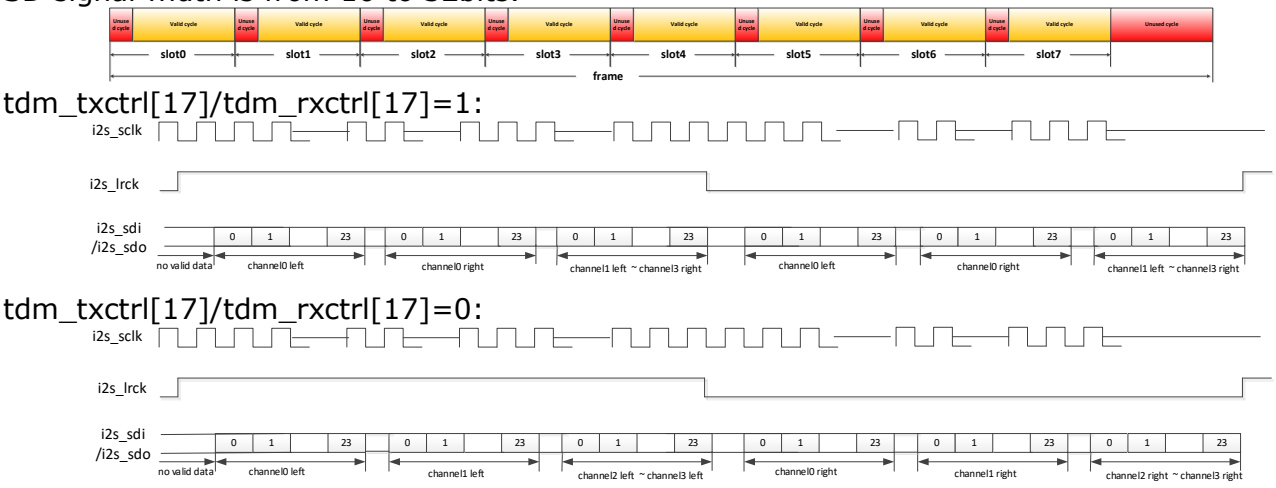



Fig. 22-19 TDM Right Justified Mode Timing Format (I2S Format)

## 22.4 Register description

### 22.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

### 22.4.2 Registers Summary for I2S/PCM controllers

Following register summary can be applied to I2S0, I2S1, I2S5, I2S6, I2S7, I2S9 and I2S10.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| I2S_2CH_TXCR | 0x0000 | W | 0x0000000F | Transmit Operation Control Register |

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| I2S_2CH_RXCR | 0x0004 | W | 0x0000000F | Receive Operation Control Register |
| I2S_2CH_CKR | 0x0008 | W | 0x00071F1F | Clock Generation Register |
| I2S_2CH_TXFIFOLR | 0x000C | W | 0x00000000 | TX FIFO Level Register |
| I2S_2CH_DMACR | 0x0010 | W | 0x001F0000 | DMA Control Register |
| I2S_2CH_INTCR | 0x0014 | W | 0x01F00000 | Interrupt Control Register |
| I2S_2CH_INTSR | 0x0018 | W | 0x00000000 | Interrupt Status Register |
| I2S_2CH_XFER | 0x001C | W | 0x00000000 | Transfer Start Register |
| I2S_2CH_CLR | 0x0020 | W | 0x00000000 | SCLK Domain Logic Clear Register |
| I2S_2CH_TXDR | 0x0024 | W | 0x00000000 | Transmit FIFO Data Register |
| I2S_2CH_RXDR | 0x0028 | W | 0x00000000 | Receive FIFO Data Register |
| I2S_2CH_RXFIFOLR | 0x002C | W | 0x00000000 | RX FIFO Level Register |
| I2S_2CH_VERSION | 0x0030 | W | 0x20150001 | Version Register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 22.4.3 Detail Registers Description

**I2S_2CH_TXCR**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x000 | reserved |
| 22:17 | RW | 0x00 | RCNT<br>Right justified counter<br>Can be written only when XFER[0] bit is 0.<br>Only valid in I2S right justified format and slave TX mode is selected.<br>Start to transmit data RCNT sclk cycles after left channel valid. |
| 16:15 | RW | 0x0 | CSR<br>Channel select<br>2'b00: 2 channel<br>2'b01~2'b11: Reserved |
| 14 | RW | 0x0 | HWT<br>Halfword word transform<br>Can be written only when XFER[0] bit is 0.<br>Only valid when VDW select 16bit data.<br>1'b0: 32 bit data valid from AHB/APB bus. Low 16 bit for left channel and high 16 bit for right channel.<br>1'b1: Low 16bit data valid from AHB/APB bus, high 16 bit data invalid. |
| 13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | SJM<br>Store justified mode<br>Can be written only when XFER[0] bit is 0.<br>16bit~31bit DATA stored in 32 bits width FIFO.<br>If VDW select 16bit data, this bit is valid only when HWT select 0.Because if HWT is 1'b1, every FIFO unit contain two 16bit data and 32 bit space is full, it is impossible to choose justified mode.<br>1'b0: Right justified<br>1'b1: Left justified |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11 | RW | 0x0 | FBM<br>First bit mode<br>Can be written only when XFER[0] bit is 0.<br>1'b0: MSB<br>1'b1: LSB |
| 10:9 | RW | 0x0 | IBM<br>I2S bus mode<br>Can be written only when XFER[0] bit is 0.<br>2'b00: I2S normal<br>2'b01: I2S left justified<br>2'b10: I2S right justified<br>2'b11: Reserved |
| 8:7 | RW | 0x0 | PBM<br>PCM bus mode<br>Can be written only when XFER[0] bit is 0.<br>2'b00: PCM no delay mode<br>2'b01: PCM delay 1 mode<br>2'b10: PCM delay 2 mode<br>2'b11: PCM delay 3 mode |
| 6 | RO | 0x0 | reserved |
| 5 | RW | 0x0 | TFS<br>Transfer format select<br>Can be written only when XFER[0] bit is 0.<br>1'b0: I2S format<br>1'b1: PCM format |
| 4:0 | RW | 0x0f | VDW<br>Valid data width<br>Can be written only when XFER[0] bit is 0.<br>5'b00000~5'b01110: Reserved<br>5'b01111: 16bit<br>5'b10000: 17bit<br>5'b10001: 18bit<br>5'b10010: 19bit<br>.....<br>5'b11100: 29bit<br>5'b11101: 30bit<br>5'b11110: 31bit<br>5'b11111: 32bit |

**I2S_2CH_RXCR**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:15 | RO | 0x00000 | reserved |
| 14 | RW | 0x0 | HWT<br>Halfword word transform<br>Can be written only when XFER[1] bit is 0.<br>Only valid when VDW select 16bit data.<br>1'b0: 32 bit data valid to AHB/APB bus. Low 16 bit for left channel and high 16 bit for right channel.<br>1'b1: Low 16bit data valid to AHB/APB bus, high 16 bit data invalid. |
| 13 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | SJM<br>Store justified mode<br>Can be written only when XFER[1] bit is 0.<br>16bit~31bit DATA stored in 32 bits width FIFO.<br>If VDW select 16bit data, this bit is valid only when HWT select 0.Because if HWT is 1'b1, every FIFO unit contain two 16bit data and 32 bit space is full, it is impossible to choose justified mode.<br>1'b0: Right justified<br>1'b1: Left justified |
| 11 | RW | 0x0 | FBM<br>First bit mode<br>Can be written only when XFER[1] bit is 0.<br>1'b0: MSB<br>1'b1: LSB |
| 10:9 | RW | 0x0 | IBM<br>I2S bus mode<br>Can be written only when XFER[1] bit is 0.<br>2'b00: I2S normal<br>2'b01: I2S left justified<br>2'b10: I2S right justified<br>2'b11: Reserved |
| 8:7 | RW | 0x0 | PBM<br>PCM bus mode<br>Can be written only when XFER[1] bit is 0.<br>2'b00: PCM no delay mode<br>2'b01: PCM delay 1 mode<br>2'b10: PCM delay 2 mode<br>2'b11: PCM delay 3 mode |
| 6 | RO | 0x0 | reserved |
| 5 | RW | 0x0 | TFS<br>Transfer format select<br>Can be written only when XFER[1] bit is 0.<br>1'b0: I2S format<br>1'b1: PCM format |
| 4:0 | RW | 0x0f | VDW<br>Valid data width<br>Can be written only when XFER[1] bit is 0.<br>5'b00000~5'b01110: Reserved<br>5'b01111: 16bit<br>5'b10000: 17bit<br>5'b10001: 18bit<br>5'b10010: 19bit<br>.....<br>5'b11100: 29bit<br>5'b11101: 30bit<br>5'b11110: 31bit<br>5'b11111: 32bit |

**I2S_2CH_CKR**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 29:28 | RW | 0x0 | TRCM<br>LRCK Control<br>2'b00: Generates LRCK for TX only.<br>2'b01: Generates LRCK for TX/RX or RX.<br>2'b10/2'b11: Reseverd<br>If only TX works, please set TRCM to 2'b00. If TX and RX work at the same time or only RX works, please set TRCM to 2'b01.<br>Note: When set to 2'b01, if user wants to use both transmitting and receiving in master mode, user should configure as following.<br>a. The value of TSD and RSD should be same.<br>b. User should start TX transfer and RX transfer at the same time. |
| 27 | RW | 0x0 | MSS<br>Master/slave mode select<br>Can be written only when XFER[1] or XFER[0] bit is 0.<br>1'b0: Master mode (sclk output)<br>1'b1: Slave mode (sclk input) |
| 26 | RW | 0x0 | CKP<br>Sclk polarity<br>Can be written only when XFER[1] or XFER[0] bit is 0.<br>1'b0: Sample data at posedge sclk and drive data at negedge sclk.<br>1'b1: Sample data at negedge sclk and drive data at posedge sclk. |
| 25 | RO | 0x0 | reserved |
| 24 | RW | 0x0 | LRCKP<br>Lrck polarity<br>Can be written only when XFER[1] or XFER[0] bit is 0.<br>1'b0: Normal polarity<br>(I2S normal: Low for left channel, high for right channel<br>I2S left/right just: High for left channel, low for right channel<br>PCM start signal: High valid)<br>1'b1: Opposite polarity<br>(I2S normal: High for left channel, low for right channel<br>I2S left/right just: Low for left channel, high for right channel<br>PCM start signal: Low valid) |
| 23:16 | RW | 0x07 | MDIV<br>Mclk divider<br>Can be written only when XFER[1] or XFER[0] bit is 0.<br>mclk divider = (mclk/sclk)-1.<br>For example, if mclk divider is 5, then the frequency of sclk is mclk/6 |
| 15:8 | RW | 0x1f | RSD<br>Receive Sclk Divider<br>Can be written only when XFER[1] or XFER[0] bit is 0.<br>8'h00~8'h1e: Reserved<br>8'h1f~8'hff: Frequency of sclk = ((RSD>>1)+1)*2*frequency of lrck for I2S format. Frequency of sclk = (RSD+1)*frequency of lrck for PCM format. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:0 | RW | 0x1f | TSD<br>Transmit sclk divider<br>Can be written only when XFER[1] or XFER[0] bit is 0.<br>8'h00~8'h1e: Reserved<br>8'h1f~8'hff: Frequency of sclk = ((TSD>>1)+1)*2*frequency of lrck for I2S format. Frequency of sclk = (TSD+1)*frequency of lrck for PCM format. |

**I2S_2CH_TXFIFOLR**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5:0 | RO | 0x00 | TFL<br>Transmit FIFO level<br>Contains the number of valid data entries in the transmit FIFO. |

**I2S_2CH_DMACR**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x00 | reserved |
| 24 | RW | 0x0 | RDE<br>Receive DMA enable<br>1'b0: Receive DMA disabled<br>1'b1: Receive DMA enabled |
| 23:21 | RO | 0x0 | reserved |
| 20:16 | RW | 0x1f | RDL<br>Receive data level<br>This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1. That is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1. |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | TDE<br>Transmit DMA enable<br>1'b0: Transmit DMA disabled<br>1'b1: Transmit DMA enabled |
| 7:5 | RO | 0x0 | reserved |
| 4:0 | RW | 0x00 | TDL<br>Transmit data level<br>This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the TXFIFO is equal to or below this field value. |

**I2S_2CH_INTCR**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x00 | reserved |
| 24:20 | RW | 0x1f | RFT<br>Receive FIFO threshold<br>When the number of receive FIFO entries is more than or equal to this threshold plus 1, the receive FIFO full interrupt is triggered. |
| 19 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 18 | WO | 0x0 | RXOIC<br>RX overrun interrupt clear<br>Write 1'b1 to clear RX overrun interrupt. |
| 17 | RW | 0x0 | RXOIE<br>RX overrun interrupt enable<br>1'b0: Disable<br>1'b1: Enable |
| 16 | RW | 0x0 | RXFIE<br>RX full interrupt enable<br>1'b0: Disable<br>1'b1: Enable |
| 15:9 | RO | 0x00 | reserved |
| 8:4 | RW | 0x00 | TFT<br>Transmit FIFO threshold<br>When the number of transmit FIFO entries is less than or equal to this threshold, the transmit FIFO empty interrupt is triggered. |
| 3 | RO | 0x0 | reserved |
| 2 | WO | 0x0 | TXUIC<br>TX underrun interrupt clear<br>Write 1'b1 to clear TX underrun interrupt. |
| 1 | RW | 0x0 | TXUIE<br>TX underrun interrupt enable<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | TXEIE<br>TX empty interrupt enable<br>1'b0: Disable<br>1'b1: Enable |

**I2S_2CH_INTSR**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17 | RO | 0x0 | RXOI<br>RX overrun interrupt<br>1'b0: Inactive<br>1'b1: Active |
| 16 | RO | 0x0 | RXFI<br>RX full interrupt<br>1'b0: Inactive<br>1'b1: Active |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RO | 0x0 | TXUI<br>TX underrun interrupt<br>1'b0: Inactive<br>1'b1: Active |
| 0 | RO | 0x0 | TXEI<br>TX empty interrupt<br>1'b0: Inactive<br>1'b1: Active |

**I2S_2CH_XFER**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | RXS<br>RX transfer start bit<br>1'b0: Stop RX transfer<br>1'b1: Start RX transfer |
| 0 | RW | 0x0 | TXS<br>TX transfer start bit<br>1'b0: Stop TX transfer.<br>1'b1: Start TX transfer. |

**I2S_2CH_CLR**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | RXC<br>RX logic clear<br>This is a self-cleared bit. Write 1'b1 to clear all receive logic. |
| 0 | RW | 0x0 | TXC<br>TX logic clear<br>This is a self-cleared bit. Write 1'b1 to clear all transmit logic. |

**I2S_2CH_TXDR**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | WO | 0x00000000 | TDR<br>Transmit FIFO data register<br>When it is written to, data are moved into the transmit FIFO. |

**I2S_2CH_RXDR**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RDR<br>Receive FIFO data register<br>When the register is read, data in the receive FIFO is accessed. |

**I2S_2CH_RXFIFOLR**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5:0 | RO | 0x00 | RFL<br>Receive FIFO level<br>Contains the number of valid data entries in the receive FIFO. |

**I2S_2CH_VERSION**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x20150001 | VER<br>Version of I2S_2CH |

## 22.4.4 Registers Summary for I2S/PCM/TDM controllers Part 1

Following register summary can be applied to I2S0, I2S1, I2S5, I2S6, I2S7, I2S9 and I2S10. Note that for I2S5 and I2S6, only TX is used, RX related registers should be ignored. For I2S7, I2S9 and I2S10, only RX is used, TX related registers should be ignored.

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| I2S_TDM_8CH_TXCR | 0x0000 | W | 0x7200000F | Transmit Operation Control Register |
| I2S_TDM_8CH_RXCR | 0x0004 | W | 0x01C8000F | Receive Operation Control Register |
| I2S_TDM_8CH_CKR | 0x0008 | W | 0x00071F1F | Clock Generation Register |
| I2S_TDM_8CH_TXFIFOLR | 0x000C | W | 0x00000000 | TX FIFO Level Register |
| I2S_TDM_8CH_DMACR | 0x0010 | W | 0x001F0000 | DMA Control Register |
| I2S_TDM_8CH_INTCR | 0x0014 | W | 0x01F00000 | Interrupt Control Register |
| I2S_TDM_8CH_INTSR | 0x0018 | W | 0x00000000 | Interrupt Status Register |
| I2S_TDM_8CH_XFER | 0x001C | W | 0x00000000 | Transfer Start Register |
| I2S_TDM_8CH_CLR | 0x0020 | W | 0x00000000 | Sclk Domain Logic Clear Register |
| I2S_TDM_8CH_TXDR | 0x0024 | W | 0x00000000 | Transmit FIFO Data Register |
| I2S_TDM_8CH_RXDR | 0x0028 | W | 0x00000000 | Receive FIFO Data Register |
| I2S_TDM_8CH_RXFIFOLR | 0x002C | W | 0x00000000 | RX FIFO Level Register |
| I2S_TDM_8CH_TDM_TXCTRL | 0x0030 | W | 0x00003EFF | TDM Mode Transmit Operation Control Register |
| I2S_TDM_8CH_TDM_RXCTRL | 0x0034 | W | 0x00003EFF | TDM Mode Receive Operation Control Register |
| I2S_TDM_8CH_CLKDIV | 0x0038 | W | 0x00000707 | Clock Divider Register |
| I2S_TDM_8CH_VERSION | 0x003C | W | 0x20150001 | Version Register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 22.4.5 Detail Registers Description

### I2S_TDM_8CH_TXCR

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |
| 30:29 | RW | 0x3 | TX_PATH_SEL3<br>TX path select 3<br>2'b00: Sdo3 output data from path0<br>2'b01: Sdo3 output data from path1<br>2'b10: Sdo3 output data from path2<br>2'b11: Sdo3 output data from path3<br>Note: When TDM mode, only path0 enable. |
| 28:27 | RW | 0x2 | TX_PATH_SEL2<br>TX path select 2<br>2'b00: Sdo2 output data from path0<br>2'b01: Sdo2 output data from path1<br>2'b10: Sdo2 output data from path2<br>2'b11: Sdo2 output data from path3<br>Note: When TDM mode, only path0 enable. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 26:25 | RW | 0x1 | TX_PATH_SEL1<br>TX path select 1<br>2'b00: Sdo1 output data from path0<br>2'b01: Sdo1 output data from path1<br>2'b10: Sdo1 output data from path2<br>2'b11: Sdo1 output data from path3<br>Note: When TDM mode, only path0 enable. |
| 24:23 | RW | 0x0 | TX_PATH_SEL0<br>TX path select 0<br>2'b00: Sdo0 output data from path0<br>2'b01: Sdo0 output data from path1<br>2'b10: Sdo0 output data from path2<br>2'b11: Sdo0 output data from path3<br>Note: When TDM mode, only path0 enable. |
| 22:17 | RW | 0x00 | RCNT<br>Can be written only when XFER[0] bit is 0.<br>Only valid in I2S right justified format and slave TX mode is selected.<br>Start to transmit data RCNT sclk cycles after left channel valid.<br>Note: Only function when TX TFS[1]=0. |
| 16:15 | RW | 0x0 | TCSR<br>Transmit channel select<br>2'b00: Two channel<br>2'b01: Four channel<br>2'b10: Six channel<br>2'b11: Eight channel |
| 14 | RW | 0x0 | HWT<br>Halfword word transform<br>Can be written only when XFER[0] bit is 0.<br>Only valid when VDW select 16bit data.<br>1'b0: 32 bit data valid from AHB/APB bus. Low 16 bit for left channel and high 16 bit for right channel.<br>1'b1: Low 16bit data valid from AHB/APB bus, high 16 bit data invalid. |
| 13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | SJM<br>Store justified mode<br>Can be written only when XFER[0] bit is 0.<br>16bit~31bit DATA stored in 32 bits width FIFO.<br>If VDW select 16bit data, this bit is valid only when HWT select 1'b0. Because if HWT is 1'b1, every FIFO unit contains two 16bit data and 32 bit space is full, it is impossible to choose justified mode.<br>1'b0: Right justified<br>1'b1: Left justified |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11 | RW | 0x0 | FBM<br>First bit mode<br>Can be written only when XFER[0] bit is 0.<br>1'b0: MSB<br>1'b1: LSB |
| 10:9 | RW | 0x0 | IBM<br>I2S bus mode<br>Can be written only when XFER[0] bit is 0.<br>2'b00: I2S normal<br>2'b01: I2S left justified<br>2'b10: I2S right justified<br>2'b11: Reserved |
| 8:7 | RW | 0x0 | PBM<br>Can be written only when XFER[0] bit is 0.<br>2'b00: PCM no delay mode<br>2'b01: PCM delay 1 mode<br>2'b10: PCM delay 2 mode<br>2'b11: PCM delay 3 mode<br>Note: Function when TX TFS[1:0] is 2'b01. |
| 6:5 | RW | 0x0 | TFS<br>Can be written only when XFER[0] bit is 0.<br>2'b00: I2S format<br>2'b01: PCM format<br>2'b10: TDM format 0 (PCM mode)<br>2'b11: TDM format 1 (I2S mode) |
| 4:0 | RW | 0x0f | VDW<br>Valid data width<br>Can be written only when XFER[0] bit is 0.<br>5'b00000~5'b01110: Reserved<br>5'b01111: 16bit<br>5'b10000: 17bit<br>5'b10001: 18bit<br>5'b10010: 19bit<br>.....<br>5'b11100: 29bit<br>5'b11101: 30bit<br>5'b11110: 31bit<br>5'b11111: 32bit |

**I2S_TDM_8CH_RXCR**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x00 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 24:23 | RW | 0x3 | RX_PATH_SEL3<br>RX path select 3<br>2'b00: Path3 data from sdi0<br>2'b01: Path3 data from sdi1<br>2'b10: Path3 data from sdi2<br>2'b11: Path3 data from sdi3<br>Note: Inoperative at TDM mode. |
| 22:21 | RW | 0x2 | RX_PATH_SEL2<br>RX path select 2<br>2'b00: Path2 data from sdi0<br>2'b01: Path2 data from sdi1<br>2'b10: Path2 data from sdi2<br>2'b11: Path2 data from sdi3<br>Note: Inoperative at TDM mode. |
| 20:19 | RW | 0x1 | RX_PATH_SEL1<br>RX path select 1<br>2'b00: Path1 data from sdi0<br>2'b01: Path1 data from sdi1<br>2'b10: Path1 data from sdi2<br>2'b11: Path1 data from sdi3<br>Note: Inoperative at TDM mode. |
| 18:17 | RW | 0x0 | RX_PATH_SEL0<br>RX path select 0<br>2'b00: Path0 data from sdi0<br>2'b01: Path0 data from sdi1<br>2'b10: Path0 data from sdi2<br>2'b11: Path0 data from sdi3 |
| 16:15 | RW | 0x0 | RCSR<br>Receive channel select<br>2'b00: Two channel<br>2'b01: Four channel<br>2'b10: Six channel<br>2'b11: Eight channel |
| 14 | RW | 0x0 | HWT<br>Halfword word transform<br>Can be written only when XFER[1] bit is 0.<br>Only valid when VDW select 16bit data.<br>1'b0: 32 bit data valid to AHB/APB bus. Low 16 bit for left channel and high 16 bit for right channel.<br>1'b1: Low 16bit data valid to AHB/APB bus, high 16 bit data invalid. |
| 13 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | SJM<br>Store justified mode<br>Can be written only when XFER[1] bit is 0.<br>16bit~31bit DATA stored in 32 bits width FIFO.<br>If VDW select 16bit data, this bit is valid only when HWT select 1'b0. Because if HWT is 1'b1, every FIFO unit contains two 16bit data and 32 bit space is full, it is impossible to choose justified mode.<br>1'b0: Right justified<br>1'b1: Left justified |
| 11 | RW | 0x0 | FBM<br>First bit mode<br>Can be written only when XFER[1] bit is 0.<br>1'b0: MSB<br>1'b1: LSB |
| 10:9 | RW | 0x0 | IBM<br>I2S bus mode<br>Can be written only when XFER[1] bit is 0.<br>2'b00: I2S normal<br>2'b01: I2S left justified<br>2'b10: I2S right justified<br>2'b11: Reserved |
| 8:7 | RW | 0x0 | PBM<br>PCM bus mode<br>Can be written only when XFER[1] bit is 0.<br>2'b00: PCM no delay mode<br>2'b01: PCM delay 1 mode<br>2'b10: PCM delay 2 mode<br>2'b11: PCM delay 3 mode |
| 6:5 | RW | 0x0 | TFS<br>Transfer format select<br>Can be written only when XFER[1] bit is 0.<br>2'b00: I2S format<br>2'b01: PCM format<br>2'b10: TDM format 0 (PCM mode)<br>2'b11: TDM format 1 (I2S mode) |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4:0 | RW | 0x0f | VDW<br>Valid data width<br>Can be written only when XFER[1] bit is 0.<br>5'b00000~5'b01110: Reserved<br>5'b01111: 16bit<br>5'b10000: 17bit<br>5'b10001: 18bit<br>5'b10010: 19bit<br>.....<br>5'b11100: 29bit<br>5'b11101: 30bit<br>5'b11110: 31bit<br>5'b11111: 32bit |

**I2S_TDM_8CH_CKR**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:28 | RW | 0x0 | LRCK_CTRL<br>LRCK Control<br>2'b01: Generates LRCK for TX or RX.<br>Others: Reseverd<br>Please set it to 2'b01 in all situations.<br>Note: When set to 2'b01, if user wants to use both transmitting and receiving in master mode, user should configure as following.<br>a. The value of TSD and RSD should be same.<br>b. User should start TX transfer and RX transfer at the same time. |
| 27 | RW | 0x0 | MSS<br>Master/slave mode select<br>Can be written only when XFER[1] or XFER[0] bit is 0.<br>1'b0: Master mode (sclk output)<br>1'b1: Slave mode (sclk input) |
| 26 | RW | 0x0 | CKP<br>Sclk polarity<br>Can be written only when XFER[1] or XFER[0] bit is 0.<br>1'b0: Sample data at posedge sclk and drive data at negedge sclk.<br>1'b1: Sample data at negedge sclk and drive data at posedge sclk. |
| 25 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 24 | RW | 0x0 | LRCKP<br>Lrck polarity<br>Can be written only when XFER[1] or XFER[0] bit is 0.<br>1'b0: Normal polarity<br>(I2S normal: Low for left channel, high for right channel<br>I2S left/right just: High for left channel, low for right channel<br>PCM start signal: High valid)<br>1'b1: Opposite polarity<br>(I2S normal: High for left channel, low for right channel<br>I2S left/right just: Low for left channel, high for right channel<br>PCM start signal: Low valid) |
| 23:16 | RO | 0x07 | reserved |
| 15:8 | RW | 0x1f | RSD<br>Receive Sclk Divider<br>Can be written only when XFER[1] or XFER[0] bit is 0.<br>8'h00~8'h1e: Reserved<br>8'h1f~8'hff:<br>Frequency of sclk = ((RSD>>1)+1)*2*frequency of lrck when RX TFS[1:0] is 2'b00.<br>Frequency of sclk = (RSD+1)*frequency of lrck when RX TFS[1:0] is 2'b01.<br>Frequency of sclk = (TDM_RX_FRAME_WIDTH+1)*frequency of lrck when RX TFS[1:0] is 2'b10.<br>Frequency of sclk = (TDM_RX_FRAME_WIDTH+1)*2*frequency of lrck when RX TFS[1:0] is 2'b11 and RX_TDM_FSYNC_WIDTH_SEL0 is 1'b1.<br>Frequency of sclk = ((TDM_RX_FRAME_WIDTH>>1)+1)*2*frequency of lrck when RX TFS[1:0] is 2'b11 and RX_TDM_FSYNC_WIDTH_SEL0 is 1'b0. |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:0 | RW | 0x1f | TSD<br>Transmit sclk divider<br>Can be written only when XFER[1] or XFER[0] bit is 0.<br>8'h00~8'h1e: Reserved<br>8'h1f~8'hff:<br>Frequency of sclk = ((TSD>>1)+1)*2*frequency of lrck when TX TFS[1:0] is 2'b00.<br>Frequency of sclk = (TSD+1)*frequency of lrck when TX TFS[1:0] is 2'b01.<br>Frequency of sclk = (TDM_TX_FRAME_WIDTH+1)*frequency of lrck when TX TFS[1:0] is 2'b10.<br>Frequency of sclk = (TDM_TX_FRAME_WIDTH+1)*2*frequency of lrck when TX TFS[1:0] is 2'b11 and TX_TDM_FSYNC_WIDTH_SEL0 is 1'b1.<br>Frequency of sclk = ((TDM_TX_FRAME_WIDTH>>1)+1)*2*frequency of lrck when TX TFS[1:0] is 2'b11 and TX_TDM_FSYNC_WIDTH_SEL0 is 1'b0. |

**I2S_TDM_8CH_TXFIFOLR**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23:18 | RO | 0x00 | TFL3<br>Transmit FIFO3 level<br>Contains the number of valid data entries in the transmit FIFO3. |
| 17:12 | RO | 0x00 | TFL2<br>Transmit FIFO2 level<br>Contains the number of valid data entries in the transmit FIFO2. |
| 11:6 | RO | 0x00 | TFL1<br>Transmit FIFO1 level<br>Contains the number of valid data entries in the transmit FIFO1. |
| 5:0 | RO | 0x00 | TFL0<br>Transmit FIFO0 level<br>Contains the number of valid data entries in the transmit FIFO0. |

**I2S_TDM_8CH_DMACR**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x00 | reserved |
| 24 | RW | 0x0 | RDE<br>Receive DMA enable<br>1'b0: Receive DMA disabled<br>1'b1: Receive DMA enabled |
| 23:21 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 20:16 | RW | 0x1f | RDL<br>Receive Data Level<br>This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1. That is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1. |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | TDE<br>Transmit DMA enable<br>1'b0: Transmit DMA disabled<br>1'b1: Transmit DMA enabled |
| 7:5 | RO | 0x0 | reserved |
| 4:0 | RW | 0x00 | TDL<br>Transmit data level<br>This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level. That is, the dma_tx_req signal is generated when the number of valid data entries in the TX FIFO(TX FIFO0 if CSR=2'b00;TX FIFO1 if CSR>=2'b01,TX FIFO2 if CSR>=2'b10,TX FIFO3 if CSR=2'b11)is equal to or below this field value. |

**I2S_TDM_8CH_INTCR**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x00 | reserved |
| 24:20 | RW | 0x1f | RFT<br>Receive FIFO threshold<br>When the number of receive FIFO entries is more than or equal to this threshold plus 1, the receive FIFO full interrupt is triggered. |
| 19 | RO | 0x0 | reserved |
| 18 | WO | 0x0 | RXOIC<br>RX overrun interrupt clear<br>Write 1'b1 to clear RX overrun interrupt. |
| 17 | RW | 0x0 | RXOIE<br>RX overrun interrupt enable<br>1'b0: Disable<br>1'b1: Enable |
| 16 | RW | 0x0 | RXFIE<br>RX full interrupt enable<br>1'b0: Disable<br>1'b1: Enable |
| 15:9 | RO | 0x00 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8:4 | RW | 0x00 | TFT<br>Transmit FIFO threshold<br>When the number of transmit FIFO entries is less than or equal to this threshold, the transmit FIFO empty interrupt is triggered. |
| 3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | TXUIC<br>TX underrun interrupt clear<br>Write 1'b1 to clear TX underrun interrupt. |
| 1 | RW | 0x0 | TXUIE<br>TX underrun interrupt enable<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | TXEIE<br>TX empty interrupt enable<br>1'b0: Disable<br>1'b1: Enable |

**I2S_TDM_8CH_INTSR**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17 | RO | 0x0 | RXOI<br>RX overrun interrupt<br>1'b0: Inactive<br>1'b1: Active |
| 16 | RO | 0x0 | RXFI<br>RX full interrupt<br>1'b0: Inactive<br>1'b1: Active |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RO | 0x0 | TXUI<br>TX underrun interrupt<br>1'b0: Inactive<br>1'b1: Active |
| 0 | RO | 0x0 | TXEI<br>TX empty interrupt<br>1'b0: Inactive<br>1'b1: Active |

**I2S_TDM_8CH_XFER**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | RXS<br>RX start bit<br>1'b0: Stop RX transfer.<br>1'b1: Start RX transfer. |
| 0 | RW | 0x0 | TXS<br>TX transfer start bit<br>1'b0: Stop TX transfer.<br>1'b1: Start TX transfer. |

**I2S_TDM_8CH_CLR**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | RXC<br>RX logic clear<br>This is a self-cleared bit. Write 1'b1 to clear all receive logic. |
| 0 | RW | 0x0 | TXC<br>TX logic clear<br>This is a self-cleared bit. Write 1'b1 to clear all transmit logic. |

**I2S_TDM_8CH_TXDR**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | WO | 0x00000000 | TXDR<br>Transmit FIFO data register<br>When it is written, data are moved into the transmit FIFO. |

**I2S_TDM_8CH_RXDR**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXDR<br>Receive FIFO data register<br>When the register is read, data in the receive FIFO is accessed. |

**I2S_TDM_8CH_RXFIFOLR**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23:18 | RO | 0x00 | RFL3<br>Receive FIFO3 level<br>Contains the number of valid data entries in the receive FIFO3. |
| 17:12 | RO | 0x00 | RFL2<br>Receive FIFO2 level<br>Contains the number of valid data entries in the receive FIFO2. |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:6 | RO | 0x00 | RFL1<br>Receive FIFO1 level<br>Contains the number of valid data entries in the receive FIFO1. |
| 5:0 | RO | 0x00 | RFL0<br>Receive FIFO0 level<br>Contains the number of valid data entries in the receive FIFO0. |

**I2S_TDM_8CH_TDM_TXCTRL**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x000 | reserved |
| 20:18 | RW | 0x0 | TX_TDM_FSYNC_WIDTH_SEL1<br>TDM transfer fsync width sel1<br>Can be written only when XFER[0] is 0.<br>3'b000: Single period of the sclk<br>3'b001: 2 period of the sclk<br>n: n+1 period of the sclk<br>3'b110: 7 period of the sclk<br>3'b111: The width is equivalent to a channel block.<br>Note: Function when TX TFS[1:0] is 2 or 3. |
| 17 | RW | 0x0 | TX_TDM_FSYNC_WIDTH_SEL0<br>TDM transfer fsync width sel0<br>Can be written only when XFER[0] is 0.<br>1'b0: 1/2 frame width. It should be set to an even number.<br>1'b1: Frame width. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 16:14 | RW | 0x0 | TDM_TX_SHIFT_CTRL<br>TDM transfer shift ctrl<br>Can be written only when XFER[0] is 0.<br>3'b000:<br>PCM format 0: Normal mode, drive data on the second negedge of sclk after rising edge of LRCK.<br>I2S format 0: Normal mode<br>3'b001:<br>PCM format 1: 1/2 cycle shift left, drive data on second posedge of sclk after rising edge of LRCK.<br>I2S format 1: Left justified mode<br>3'b010:<br>PCM format 2: 1 cycle shift left, drive data on first negedge of sclk after rising edge of LRCK.<br>I2S format 2: Right justified mode<br>3'b011:<br>PCM format 3: 3/2 cycle shift left, drive data on first posedge of sclk after rising edge of LRCK.<br>I2S format: Not supported<br>3'b100:<br>PCM format 4: 2 cycle shift left, drive data aligned to the posedge of LRCK.<br>I2S format: Not supported<br>3'b101~3'b111: Not supported<br>Note: Function when TX TFS[1:0] is 2 or 3. |
| 13:9 | RW | 0x1f | TDM_TX_SLOT_BIT_WIDTH<br>TDM transfer slot bits<br>Can be written only when XFER[0] is 0.<br>5'h00~5'h0e: Reserved<br>5'h0f: 16bit<br>5'h10: 17bit<br>5'h11: 18bit<br>5'h12: 19bit<br>.....<br>5'h1f: 32bit<br>Note: Function when TX TFS[1:0] is 2 or 3. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8:0 | RW | 0x0ff | TDM_TX_FRAME_WIDTH<br>TDM transfer frame width<br>Can be written only when XFER[0] is 0.<br>9'h000~9'h01e: Reserved<br>9'h01f: 32bit<br>9'h020: 33bit<br>9'h021: 34bit<br>9'h022: 35bit<br>.....<br>9'h1ff: 512bit<br>Note: Functional when TX TFS[1:0] is 2 or 3. |

**I2S_TDM_8CH_TDM_RXCTRL**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x000 | reserved |
| 20:18 | RW | 0x0 | RX_TDM_FSYNC_WIDTH_SEL1<br>TDM receive fsync width sel1<br>Can be written only when XFER[1] is 0.<br>3'b000: Single period of the sclk<br>3'b001: 2 period of the sclk<br>n: n+1 period of the sclk<br>3'b110: 7 period of the sclk<br>3'b111: The width is equivalent to a channel block<br>Note: Function when RX TFS[1:0] is 2 or 3. |
| 17 | RW | 0x0 | RX_TDM_FSYNC_WIDTH_SEL0<br>TDM receive fsync width sel0<br>Can be written only when XFER[1] is 0.<br>1'b0: 1/2 frame width. It should be set to an even number.<br>1'b1: Frame width |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 16:14 | RW | 0x0 | TDM_RX_SHIFT_CTRL<br>TDM receive shift ctrl<br>Can be written only when XFER[1] is 0.<br>3'b000:<br>PCM format 0: Normal mode, sample data on the third posedge of sclk after rising edge of LRCK.<br>I2S format 0: Normal mode<br>3'b001:<br>PCM format 1: 1/2 cycle shift left, sample data on second negedge of sclk after rising edge of LRCK.<br>I2S format 1: left justified mode<br>3'b010:<br>PCM format 2: 1 cycle shift left, sample data on second posedge of sclk after rising edge of LRCK.<br>I2S format 2: Right justified mode<br>3'b011:<br>PCM format 3: 3/2 cycle shift left, sample data on first negedge of sclk after rising edge of LRCK.<br>I2S format: Not supported<br>3'b100:<br>PCM format 4: 2 cycle shift left, sample data on the first posedge of sclk after rising edge of LRCK.<br>I2S format: Not supported<br>3'b101~3'b111: Not supported<br>Note: Function when RX TFS[1:0] is 2 or 3. |
| 13:9 | RW | 0x1f | TDM_RX_SLOT_BIT_WIDTH<br>TDM receive slot bits<br>Can be written only when XFER[1] is 0.<br>5'h00~5'h0e: Reserved<br>5'h0f: 16bit<br>5'h10: 17bit<br>5'h11: 18bit<br>5'h12: 19bit<br>.....<br>5'h1f: 32bit<br>Note: Function when RX TFS[1:0] is 2 or 3. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8:0 | RW | 0x0ff | TDM_RX_FRAME_WIDTH<br>TDM receive frame width<br>Can be written only when XFER[1] is 0.<br>9'h000~9'h01e: Reserved<br>9'h01f: 32bit<br>9'h020: 33bit<br>9'h021: 34bit<br>9'h022: 35bit<br>.....<br>9'h1ff: 512bit<br>Note: Functional when RX TFS[1:0] is 2 or 3. |

**I2S_TDM_8CH_CLKDIV**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0007 | reserved |
| 7:0 | RW | 0x07 | MDIV<br>Mclk divider<br>Can be written only when XFER[0] bit is 0.<br>mclk divider = (mclk/sclk)-1.<br>For example, if mclk divider is 5, then the frequency of sclk is mclk/6. |

**I2S_TDM_8CH_VERSION**

Address: Operational Base + offset (0x003C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x20150001 | VER<br>Version of I2S_TDM_8CH |

## 22.4.6 Registers Summary for I2S/PCM/TDM controllers Part 2

For I2S4 and I2S8, only master TX mode is used, RX related registers should be ignored. Registers of I2S4 and I2S8 are same as I2S0, I2S1, I2S5, I2S6, I2S7, I2S9 and I2S10 except that I2S_TDM_8CH_CKR is different.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| I2S_TDM_8CH_CKR | 0x0000 | W | 0x00003e1f | Clock Generation Register |

## 22.4.7 Detail Registers Description

**I2S_TDM_8CH_CKR**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 29:28 | RW | 0x0 | LRCK_CTRL<br>LRCK Control<br>2'b00: Generates LRCK for TX.<br>Others: Reseverd<br>Please set it to 2’b00 in all situations. |
| 27 | RW | 0x0 | MSS<br>Master/slave mode select<br>Can be written only when XFER[1] or XFER[0] bit is 0.<br>1'b0: Master mode (sclk output)<br>1'b1: Slave mode (sclk input) |
| 26 | RW | 0x0 | CKP<br>Sclk polarity<br>Can be written only when XFER[1] or XFER[0] bit is 0.<br>1'b0: Sample data at posedge sclk and drive data at negedge sclk.<br>1'b1: Sample data at negedge sclk and drive data at posedge sclk. |
| 25 | RO | 0x0 | reserved |
| 24 | RW | 0x0 | LRCKP<br>Lrck polarity<br>Can be written only when XFER[1] or XFER[0] bit is 0.<br>1'b0: Normal polarity<br>(I2S normal: Low for left channel, high for right channel<br>I2S left/right just: High for left channel, low for right channel<br>PCM start signal: High valid)<br>1'b1: Opposite polarity<br>(I2S normal: High for left channel, low for right channel<br>I2S left/right just: Low for left channel, high for right channel<br>PCM start signal: Low valid) |
| 23:18 | RO | 0x00 | reserved |
| 17:9 | RO | 0x1f | reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8:0 | RW | 0x1f | TSD<br>Transmit sclk divider<br>Can be written only when XFER[1] or XFER[0] bit is 0.<br>8'h00~8'h1e: Reserved<br>8'h1f~8'hff:<br>Frequency of sclk = ((TSD>>1)+1)*2*frequency of lrck when TX TFS[1:0] is 2'b00.<br>Frequency of sclk = (TSD+1)*frequency of lrck when TX TFS[1:0] is 2'b01.<br>Frequency of sclk = (TDM_TX_FRAME_WIDTH+1)*frequency of lrck when TX TFS[1:0] is 2'b10.<br>Frequency of sclk = (TDM_TX_FRAME_WIDTH+1)*2*frequency of lrck when TX TFS[1:0] is 2'b11 and TX_TDM_FSYNC_WIDTH_SEL0 is 1'b1.<br>Frequency of sclk = ((TDM_TX_FRAME_WIDTH>>1)+1)*2*frequency of lrck when TX TFS[1:0] is 2'b11 and TX_TDM_FSYNC_WIDTH_SEL0 is 1'b0. |

# 22.5 Interface Description

## 22.5.1 I2S0 Interface Description

The following table shows the I2S0 interface description.

Table 22-1 I2S0 Interface Description

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| i2s0_mclk | I/O | I2S0_MCLK/I2C6_SDA_M1/UART3_RTSN/PWM3_IR_M2/SPI4_CLK_M0/GPIO1_C2_d | BUS_IOC_GPIO1C_IOMUX_SEL_L[11:8]=4'h1 |
| i2s0_sclk | I/O | I2S0_SCLK/I2C6_SCL_M1/UART3_CTSN/PWM7_IR_M2/SPI4_CS0_M0/GPIO1_C3_d | BUS_IOC_GPIO1C_IOMUX_SEL_L[15:12]=4'h1 |
| i2s0_lrck | I/O | I2S0_LRCK/I2C2_SCL_M3/UART4_RTSN/GPIO1_C5_d | BUS_IOC_GPIO1C_IOMUX_SEL_H[7:4]=4'h1 |
| i2s0_sdo0 | O | I2S0_SDO0/I2C4_SCL_M4/UART4_CTSN/GPIO1_C7_d | US_IOC_GPIO1C_IOMUX_SEL_H[15:12]=4'h1 |
| i2s0_sdo1 | O | I2S0_SDO1/I2C7_SCL_M0/UART6_TX_M2/SPI1_MISO_M2/GPIO1_D0_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[3:0]=4'h1 |
| i2s0_sdo2 | O | I2S0_SDO2/I2S0_SDI3/PDM0_SDI1_M0/PCIE30PHY_DTB1/I2C7_SDA_M0/UART6_RX_M2/SPI1_MOSI_M2/GPIO1_D1_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[7:4]=4'h1 |
| i2s0_sdo3 | O | I2S0_SDO3/I2S0_SDI2/PDM0_SDI2_M0/I2C1_SCL_M4/UART4_TX_M0/PWM0_M1/SPI1_CLK_M2/GPIO1_D2_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[11:8]=4'h1 |
| i2s0_sdi3 | I | I2S0_SDO2/I2S0_SDI3/PDM0_SDI1_M0/PCIE30PHY_DTB1/I2C7_SDA_M0/UART6_RX_M2/SPI1_MOSI_M2/GPIO1_D1_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[7:4]=4'h2 |
| i2s0_sdi2 | I | I2S0_SDO3/I2S0_SDI2/PDM0_SDI2_M0/I2C1_SCL_M4/UART4_TX_M0/PWM0_M1/SPI1_CLK_M2/GPIO1_D2_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[11:8]=4'h2 |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| i2s0_sdi1 | I | I2S0_SDI1/PDM0_SDI3_M0/I2C1_SDA_M4/UART4_RX_M0/PWM1_M1/SPI1_CS0_M2/GPIO1_D3_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[15:12]=4'h2 |
| i2s0_sdi0 | I | I2S0_SDI0/GPIO1_D4_d | BUS_IOC_GPIO1D_IOMUX_SEL_H[3:0]=4'h2 |

## 22.5.2 I2S1 Interface Description

The following table shows the I2S1 group 0 interface description.

Table 22-2 I2S1 Group 0 Interface Description

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| i2s1_mclk | I/O | CIF_D0/BT1120_D0/I2S1_MCLK_M0/PCIE30X1_1_CLKREQN_M1/DDRPHY_CH0_DTB0/UART9_RTSN_M1/SPI0_MISO_M1/GPIO4_A0_d | BUS_IOC_GPIO4A_IOMUX_SEL_L[3:0]=4'h3 && PMU1_IOC_GPIO0B_IOMUX_SEL_H[7:4]==4'h0 |
| i2s1_sclk | I/O | CIF_D1/BT1120_D1/I2S1_SCLK_M0/PCIE30X1_1_WAKEN_M1/DDRPHY_CH0_DTB_1/UART9_CTSN_M1/SPI0_MOSI_M1/GPIO4_A1_d | BUS_IOC_GPIO4A_IOMUX_SEL_L[7:4]=4'h3 && PMU1_IOC_GPIO0B_IOMUX_SEL_H[11:8]==4'h0 |
| i2s1_lrck | I/O | CIF_D2/BT1120_D2/I2S1_LRCK_M0/PCIE30X1_1_PERSTN_M1/DDRPHY_CH0_DTB2/SPI0_CLK_M1/GPIO4_A2_d | BUS_IOC_GPIO4A_IOMUX_SEL_L[11:8]=4'h3 && PMU1_IOC_GPIO0B_IOMUX_SEL_H[15:12]==4'h0 |
| i2s1_sdo0 | O | MIPI_CAMERA0_CLK_M0/SPDIF1_TX_M1/I2S1_SDO0_M0/PCIE30X1_0_BUTTON_RSTN/SATA2_ACT_LED_M0/DDRPHY_CH2_DTB1/I2C6_SCL_M3/UART8_RX_M0/SPI0_CS1_M1/GPIO4_B1_u | BUS_IOC_GPIO4B_IOMUX_SEL_L[7:4]=4'h3 |
| i2s1_sdo1 | O | CIF_HREF/BT1120_D8/I2S1_SDO1_M0/PCIE30X1_1_BUTTON_RSTN/DDRPHY_CH2_DTB2/I2C7_SCL_M3/UART8_RTSN_M0/PWM14_M1/SPI0_CS0_M1/CAN1_RX_M1/GPIO4_B2_u | BUS_IOC_GPIO4B_IOMUX_SEL_L[11:8]=4'h3 |
| i2s1_sdo2 | O | CIF_VSYNC/BT1120_D9/I2S1_SDO2_M0/PCIE20X1_2_BUTTON_RSTN/DDRPHY_CH2_DTB3/I2C7_SDA_M3/UART8_CTSN_M0/PWM15_IR_M1/CAN1_TX_M1/GPIO4_B3_u | BUS_IOC_GPIO4B_IOMUX_SEL_L[15:12]=4'h3 |
| i2s1_sdo3 | O | CIF_CLKOUT/BT1120_D10/I2S1_SDO3_M0/PCIE30X4_CLKREQN_M1/DP0_HPDIN_M0/SPDIF0_TX_M1/DDRPHY_CH3_DTB0/UART9_TX_M1/PWM11_IR_M1/GPIO4_B4_u | BUS_IOC_GPIO4B_IOMUX_SEL_H[3:0]=4'h3 |
| i2s1_sdi0 | I | CIF_D5/BT1120_D5/I2S1_SDI0_M0/PCIE30X1_0_PERSTN_M1/DDRPHY_CH1_DTB_1/I2C3_SDA_M2/UART3_TX_M2/SPI2_MOSI_M1/GPIO4_A5_d | BUS_IOC_GPIO4A_IOMUX_SEL_H[7:4]=4'h3 && PMU1_IOC_GPIO0C_IOMUX_SEL_H[7:4]==4'h0 |
| i2s1_sdi1 | I | CIF_D6/BT1120_D6/I2S1_SDI1_M0/PCIE30X2_CLKREQN_M1/DDRPHY_CH1_DTB2/ | BUS_IOC_GPIO4A_IOMUX_SEL_H[11:8]=4'h3 && PMU1_IOC_GPIO0C_IOMUX_SEL_H[11:8]==4'h0 |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| | | I2C5_SCL_M2/UART3_RX_M2/SPI2_CLK_M1/GPIO4_A6_d | |
| i2s1_sdi2 | I | CIF_D7/BT1120_D7/I2S1_SDI2_M0/PCIE30X2_WAKEN_M1/DDRPHY_CH1_DTB3/I2C5_SDA_M2/SPI2_CS0_M1/GPIO4_A7_d | BUS_IOC_GPIO4A_IOMUX_SEL_H[15:12]=4'h3 && PMU1_IOC_GPIO0C_IOMUX_SEL_H[15:12]==4'h0 |
| i2s1_sdi3 | I | CIF_CLKIN/BT1120_CLKOUT/I2S1_SDI3_M0/PCIE30X2_PERSTN_M1/DDRPHY_CH2_DTB0/I2C6_SDA_M3/UART8_TX_M0/SPI2_CS1_M1/GPIO4_B0_d | BUS_IOC_GPIO4B_IOMUX_SEL_L[3:0]=4'h3 && PMU1_IOC_GPIO0D_IOMUX_SEL_L[3:0]==4'h0 |

The following table shows the I2S1 group 1 interface description.

Table 22-3 I2S1 Group 1 Interface Description

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| i2s1_mclk | I/O | I2S1_MCLK_M1/JTAG_TCK_M2/I2C1_SCL_M0/UART2_TX_M0/PCIE30X1_1_CLKREQN_M0/GPIO0_B5_d | PMU1_IOC_GPIO0B_IOMUX_SEL_H[7:4]=4'h1 |
| i2s1_sclk | I/O | I2S1_SCLK_M1/JTAG_TMS_M2/I2C1_SDA_M0/UART2_RX_M0/PCIE30X1_1_WAKEN_M0/GPIO0_B6_d | PMU1_IOC_GPIO0B_IOMUX_SEL_H[11:8]=4'h1 |
| i2s1_lrck | I/O | I2S1_LRCK_M1/PWM0_M0/I2C2_SCL_M0/CAN0_TX_M0/SPI0_CS1_M0/PCIE30X1_1_PERSTN_M0/GPIO0_B7_d | PMU1_IOC_GPIO0B_IOMUX_SEL_H[15:12]==4'h1 |
| i2s1_sdo0 | O | I2S1_SDO0_M1/CPU_BIG0_AVS/I2C0_SCL_M2/UART0_CTSN/UART1_TX_M2/HDMI_RX_SDA_M0/SPI0_CS0_M0/PCIE30X2_CLKREQN_M0/HDMI_TX0_CEC_M1/GPIO0_D1_u | PMU1_IOC_GPIO0D_IOMUX_SEL_L[7:4]=4'h1 |
| i2s1_sdo1 | O | I2S1_SDO1_M1/I2C0_SDA_M2/UART1_RX_M2/HDMI_RX_SCL_M0/SPI3_MOSI_M2/PCIE30X2_WAKEN_M0/HDMI_TX1_CEC_M1/GPIO0_D2_u | PMU1_IOC_GPIO0D_IOMUX_SEL_L[11:8]=4'h1 |
| i2s1_sdo2 | O | I2S1_SDO2_M1/PDM0_SDI2_M1/PWM3_IR_M0/I2C1_SCL_M2/CAN2_RX_M1/HDMI_TX0_SDA_M1/SPI3_CS0_M2/PCIE30X2_PERSTN_M0/SATA_CPDET/GPIO0_D4_u | PMU1_IOC_GPIO0D_IOMUX_SEL_H[3:0]=4'h1 |
| i2s1_sdo3 | O | I2S1_SDO3_M1/CPU_BIG1_AVS/I2C1_SDA_M2/CAN2_TX_M1/HDMI_TX0_SCL_M1/SPI3_CS1_M2/SATA_MP_SWITCH/GPIO0_D5_u | PMU1_IOC_GPIO0D_IOMUX_SEL_H[7:4]=4'h1 |
| i2s1_sdi0 | I | I2S1_SDI0_M1/GPU_AVS/UART0_TX_M0/I2C4_SCL_M2/DP1_HPDIN_M1/PWM4_M0/PCIE30X1_0_PERSTN_M0/GPIO0_C5_u | PMU1_IOC_GPIO0C_IOMUX_SEL_H[7:4]==4'h1 |
| i2s1_sdi1 | I | I2S1_SDI1_M1/NPU_AVS/UART0_RTSN/PWM5_M1/SPI0_CLK_M0/PCIE30X4_CLKREQN_M0/SATA_CP_POD/GPIO0_C6_u | PMU1_IOC_GPIO0C_IOMUX_SEL_H[11:8]==4'h1 |
| i2s1_sdi2 | I | I2S1_SDI2_M1/PDM0_SDI0_M1/I2C6_SDA_M0/UART1_RTSN_M2/PWM6_M0/SPI0_ | PMU1_IOC_GPIO0C_IOMUX_SEL_H[15:12]==4'h1 |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| | | MISO_M0/PCIE30X4_WAKEN_M0/GPIO0_C7_d | |
| i2s1_sdi3 | I | I2S1_SDI3_M1/PDM0_SDI1_M1/I2C6_SCL_M0/UART1_CTSN_M2/PWM7_IR_M0/SPI3_MISO_M2/PCIE30X4_PERSTN_M0/GPIO0_D0_d | PMU1_IOC_GPIO0D_IOMUX_SEL_L[3:0]==4'h1 |

## 22.5.3 I2S2 Interface Description

The following table shows the I2S2 group 0 interface description.

Table 22-4 I2S2 Group 0 Interface Description

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| i2s2_mclk | I/O | GMAC0_TXD0/I2S2_MCLK_M0/I2C5_SCL_M4/UART1_RX_M0/GPIO2_B6_d | BUS_IOC_GPIO2B_IOMUX_SEL_H[11:8]=4'h2 && BUS_IOC_GPIO3B_IOMUX_SEL_H[3:0]=4'h0 |
| i2s2_sclk | I/O | GMAC0_TXD1/I2S2_SCLK_M0/I2C5_SDA_M4/UART1_TX_M0/GPIO2_B7_d | BUS_IOC_GPIO2B_IOMUX_SEL_H[15:12]=4'h2 && BUS_IOC_GPIO3B_IOMUX_SEL_H[7:4]=4'h0 |
| i2s2_lrck | I/O | GMAC0_TXEN/I2S2_LRCK_M0/I2C2_SDA_M1/UART1_RTSN_M0/SPI1_CLK_M0/GPIO2_C0_d | BUS_IOC_GPIO2C_IOMUX_SEL_L[3:0]=4'h2 && BUS_IOC_GPIO3B_IOMUX_SEL_H[11:8]=4'h0 |
| i2s2_sdo0 | O | GMAC0_MCLKINOUT/I2S2_SDO_M0/I2C7_SCL_M1/PWM4_M1/SPI3_CS1_M0/GPIO4_C3_d | BUS_IOC_GPIO4C_IOMUX_SEL_L[15:12]=4'h2 |
| i2s2_sdi0 | I | ETH0_REFCLKO_25M/I2S2_SDI_M0/I2C6_SCL_M2/SPI1_CS0_M0/GPIO2_C3_d | BUS_IOC_GPIO2C_IOMUX_SEL_L[15:12]=4'h2 && BUS_IOC_GPIO3B_IOMUX_SEL_L[11:8]=4'h0 |

The following table shows the I2S2 group 1 interface description.

Table 22-5 I2S2 Group 1 Interface Description

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| i2s2_mclk | I/O | GMAC1_TXD1/I2S2_MCLK_M1/UART2_CTSN/GPIO3_B4_u | BUS_IOC_GPIO3B_IOMUX_SEL_H[3:0]=4'h3 |
| i2s2_sclk | I/O | GMAC1_TXEN/I2S2_SCLK_M1/CAN1_RX_M0/UART3_TX_M1/PWM12_M0/GPIO3_B5_u | BUS_IOC_GPIO3B_IOMUX_SEL_H[7:4]=4'h3 |
| i2s2_lrck | I/O | GMAC1_MCLKINOUT/I2S2_LRCK_M1/CAN1_TX_M0/UART3_RX_M1/PWM13_M0/GPIO3_B6_d | BUS_IOC_GPIO3B_IOMUX_SEL_H[11:8]=4'h3 |
| i2s2_sdo0 | O | GMAC1_TXD0/I2S2_SDO_M1/UART2_RTSN/GPIO3_B3_u | BUS_IOC_GPIO3B_IOMUX_SEL_L[15:12]=4'h3 |
| i2s2_sdi0 | I | GMAC1_TXER/I2S2_SDI_M1/UART2_RX_M2/PWM3_IR_M1/GPIO3_B2_d | BUS_IOC_GPIO3B_IOMUX_SEL_L[11:8]=4'h3 |

There are 2 IOMUX groups connected to I2S2. BUS_IOC_GPIO3B_IOMUX_SEL_H[3:0], BUS_IOC_GPIO3B_IOMUX_SEL_H[7:4], BUS_IOC_GPIO3B_IOMUX_SEL_L[3:0], BUS_IOC_GPIO3B_IOMUX_SEL_H[11:8], BUS_IOC_GPIO3B_IOMUX_SEL_L[7:4] and BUS_IOC_GPIO3B_IOMUX_SEL_L[11:8] are used to select whether I2S2 group 0 interface or group 1 interface is used.

## 22.5.4 I2S3 Interface Description

The following table shows the I2S3 interface description.

Copyright 2022 © Rockchip Electronics Co., Ltd.

Table 22-6 I2S3 Interface Description

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| i2s3_mclk | I/O | GMAC1_TXD2/SDIO_D0_M1/I2S3_MCLK/FSPI_D0_M2/I2C6_SDA_M4/PWM10_M0/SPI4_MISO_M1/GPIO3_A0_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[3:0]=4'h3 |
| i2s3_sclk | I/O | GMAC1_TXD3/SDIO_D1_M1/I2S3_SCLK/AUDDSM_LN/FSPI_D1_M2/I2C6_SCL_M4/PWM11_IR_M0/SPI4_MOSI_M1/GPIO3_A1_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[7:4]=4'h3 && SYS_GRF_SOC_CON6[8]=1'b1 |
| i2s3_lrck | I/O | GMAC1_RXD2/SDIO_D2_M1/I2S3_LRCK/AUDDSM_LP/FSPI_D2_M2/UART8_TX_M1/SPI4_CLK_M1/GPIO3_A2_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[11:8]=4'h3 && SYS_GRF_SOC_CON6[9]=1'b1 |
| i2s3_sdo0 | O | GMAC1_RXD3/SDIO_D3_M1/I2S3_SDO/AUDDSM_RN/FSPI_D3_M2/UART8_RX_M1/SPI4_CS0_M1/GPIO3_A3_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[15:12]=4'h3 |
| i2s3_sdi0 | I | GMAC1_TXCLK/SDIO_CMD_M1/I2S3_SDI/AUDDSM_RP/UART8_RTSN_M1/SPI4_CS1_M1/GPIO3_A4_d | BUS_IOC_GPIO3A_IOMUX_SEL_H[3:0]=4'h3 |

The TX interface of I2S3 can be also connected to the RX interface of Digital Audio Codec by programming SYS_GRF_SOC_CON6[11]. If SYS_GRF_SOC_CON6[11] is 1'b1, I2S3 is connected to Digital Audio Codec.

### 22.5.5 I2S4 and I2S8 Interface Description

I2S4 and I2S8 are connected to DPTX0 and DPTX1 respectively. I2S4 and I2S8 should be always operate in master TX mode, other modes are not support. Following table shows connection between I2S4/8 and DPTX0/1.

Table 22-7 I2S4/8 and DPTX0/1 Interface Description

| Module Pin (I2S4/8) | Direction | Module Pin (DPTX0/1) |
|---|---|---|
| i2sx_sclk(x=4,8) | O | i2sclk |
| i2sx_lrck(x=4,8) | O | i2slrclk_i |
| i2sx_sdo[3:0] (x=4,8) | O | i2sdata_i[3:0] |

### 22.5.6 I2S5 and I2S6 Interface Description

The TX interface of I2S5 can be connected to EDP TX Controller0 and HDMI TX Controller0 at the same time by programming VO1_GRF_VO1_CON0[3] to 1'b1 and VO1_GRF_VO1_CON3[13] to 1'b1 respectively. Note that I2S5 should always operate in master TX mode, other modes are not support.

The TX interface of I2S6 can be connected to EDP TX Controller1 and HDMI TX Controller1 at the same time by programming VO1_GRF_VO1_CON1[3] to 1'b1 and VO1_GRF_VO1_CON6[13] to 1'b1 respectively. Note that I2S6 should always operate in master TX mode, other modes are not support.

Following table shows connection between I2S5/6 and EDP TX Controller0/1.

Table 22-8 I2S5/6 and EDP TX Controller0/1 Interface Description

| Module Pin (I2S5/6) | Direction | Module Pin (EDP TX Controller0/1) |
|---|---|---|
| i2sx_sclk(x=5,6) | O | I_I2S_SCK_IN |
| i2sx_lrck(x=5,6) | O | I_I2S_WS_IN |
| i2sx_sdo0 (x=5,6) | O | I_I2S_SD0_IN |
| i2sx_sdo1 (x=5,6) | O | I_I2S_SD1_IN |
| i2sx_sdo2 (x=5,6) | O | I_I2S_SD2_IN |
| i2sx_sdo3 (x=5,6) | O | I_I2S_SD3_IN |

Copyright 2022 © Rockchip Electronics Co., Ltd.

Table 22-9 I2S5/6 and HDMI TX Controller0/1 Interface Description

| Module Pin (I2S5/6) | Direction | Module Pin (HDMI TX Controller0/1) |
|---|---|---|
| i2sx_sclk(x=5,6) | O | ii2s_sck |
| i2sx_lrck(x=5,6) | O | ii2s_ws |
| i2sx_sdo[3:0] (x=5,6) | O | ii2s_sdin[3:0] |

### 22.5.7 I2S7 Interface Description

The RX interface of I2S7 is connected to HDMIRX. I2S7 should always operate in RX slave mode, other modes are not support. Following table shows connection between I2S7 and HDMIRX.

Table 22-10 I2S7 and HDMIRX Interface Description

| Module Pin | Direction | Module Pin |
|---|---|---|
| i2s7_sclk | I | osao_i2s_sck |
| i2s7_lrck | I | osao_i2s_ws |
| i2s7_sdi[3:0] | I | osao_i2s_data[3:0] |

### 22.5.8 I2S9 and I2S10 Interface Description

The RX interface of I2S9 and I2S10 are connected to HDMI TX Controller0 and HDMI TX Controller1 respectively. I2S9 and I2S10 should always operate in RX slave mode, other modes are not support. Following table shows connection between I2S9/10 and HDMI TX Controller0/1.

Table 22-11 I2S9/10 and HDMI TX Controller0/1 Interface Description

| Module Pin (I2S9/10) | Direction | Module Pin (HDMI TX Controller0/1) |
|---|---|---|
| i2sx_sclk(x=9,10) | I | oearcrx_dmac_sao_i2s_sck |
| i2sx_lrck(x=9,10) | I | oearcrx_dmac_sao_i2s_ws |
| i2sx_sdi[3:0](x=9,10) | I | oearcrx_dmac_sao_i2s_data[3:0] |

## 22.6 Application Notes

### 22.6.1 Software Application Notes

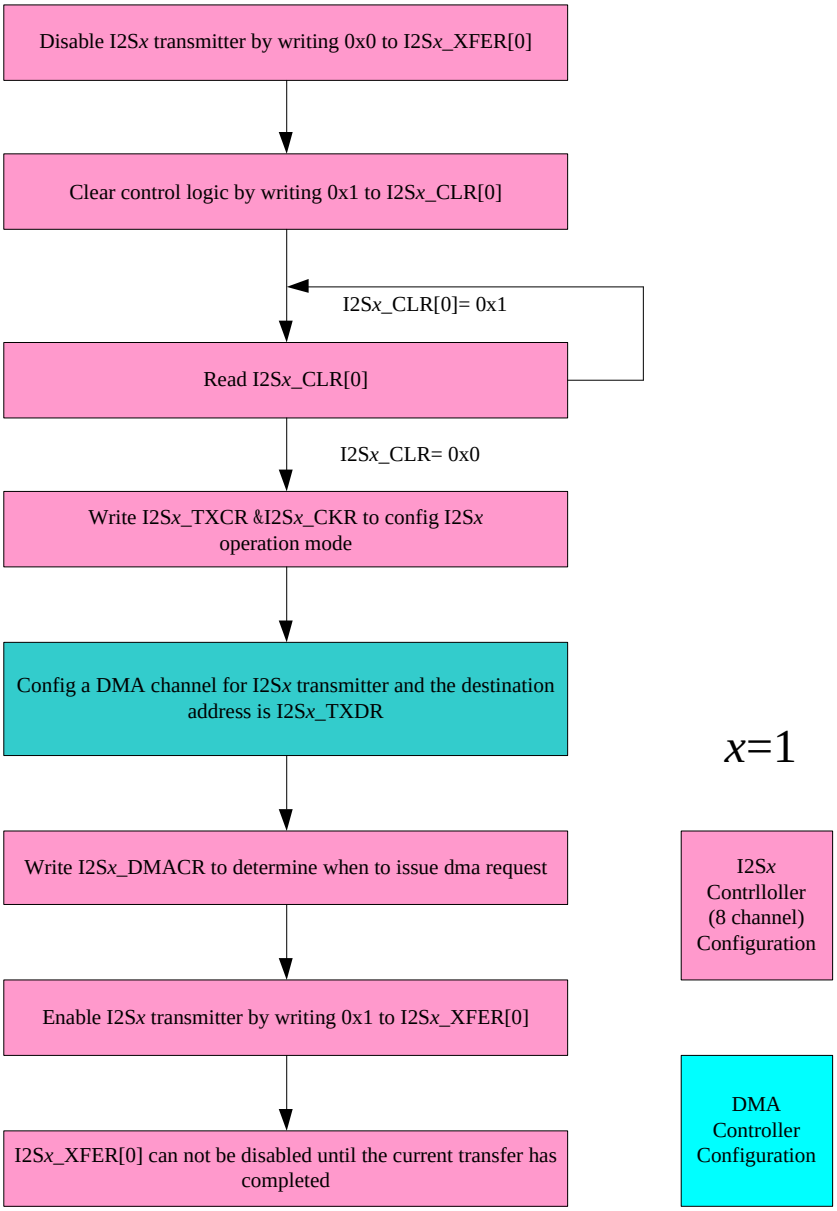



Fig. 22-20 I2S/PCM/TDM Controller Transmit Operation Flow Chart

*Note: User should clear TX/RX logical by CLR[0]/CLR[1] and wait clear operation done before configure the other registers.*

For I2S0, I2S1, I2S4, I2S5, I2S6, I2S7, I2S8, I2S9 and I2S10, these are I2S/PCM/TDM controllers. I2S/PCM/TDM controllers can support up to 16 channels when operate in TDM mode. Following configurations must be observed when in 16-channel TDM mode before starting sending or receiving audio data.

1. Set I2S_TDM_8CH_TXCR.TFS to 2'b11 or I2S_TDM_8CH_RXCR.TFS to 2'b11.
2. Set I2S_TDM_8CH_TDM_TXCTRL.TX_TDM_FSYNC_WIDTH_SEL0 to 1'b1 or I2S_TDM_8CH_TDM_RXCTRL.RX_TDM_FSYNC_WIDTH_SEL0 to 1'b1.
3. Set other registers properly.

Copyright 2022 © Rockchip Electronics Co., Ltd.

# Chapter 23 SPDIF Transmitter

## 23.1 Overview

The SPDIF transmitter is a self-clocking, serial, unidirectional interface for the interconnection of digital audio equipment for consumer and professional applications, using linear PCM coded audio samples.
It provides the basic structure of the interface. Separate documents define items specific to particular applications.
When used in a professional application, the interface is primarily intended to carry monophonic or stereophonic programmes, at a 48 kHz sampling frequency and with a resolution of up to 24bits per sample; it may alternatively be used to carry signals sampled at 32 kHz or 44.1 kHz.
When used in a consumer application, the interface is primarily intended to carry stereophonic programmes, with a resolution of up to 20 bits per sample, an extension to 24 bits per sample being possible.
When used for other purposes, the interface is primarily intended to carry audio data coded other than as linear PCM coded audio samples. Provision is also made to allow the interface to carry data related to computer software or signals coded using non-linear PCM. The format specification for these applications is not part of this standard.
In all cases, the clock references and auxiliary information are transmitted along with the programme.
There are 6 SPDIF transmitters in total. They are SPDIF0, SPDIF1, SPDIF2, SPDIF3, SPDIF4 and SPDIF5.
MCLK is the operation clock of SPDIF transmitter. The maximum frequency of MCLK are different for the 6 SPDIF transmitters. Following table shows the maximum frequency of MCLK for SPDIF0, SPDIF1, SPDIF2, SPDIF3, SPDIF4 and SPDIF5.

Table 23-1 Maximum Frequency of MCLK for the 6 SPDIF Transmitters

| SPDIF transmitter | Maximum frequency of MCLK |
|---|---|
| SPDIF0, SPDIF1 | 49.152MHz |
| SPDIF2, SPDIF5 | 393.216MHz |
| SPDIF3, SPDIF4 | 196.608MHz |

Each SPDIF transmitter supports following features.

- Support one internal 32-bit wide and 32-location deep sample data buffer
- Support two 16-bit audio data store together in one 32-bit wide location
- Support AHB bus interface
- Support biphase format stereo audio data output
- Support DMA handshake interface and configurable DMA water level
- Support sample data buffer empty and block terminate interrupt
- Support combine interrupt output
- Support 16 to 31 bit audio data left or right justified in 32-bit wide sample data buffer
- Support 48, 44.1, 32kHz sample rate
- Support 16, 20, 24 bits audio data transfer

Copyright 2022 © Rockchip Electronics Co., Ltd.

## 23.2 Block Diagram

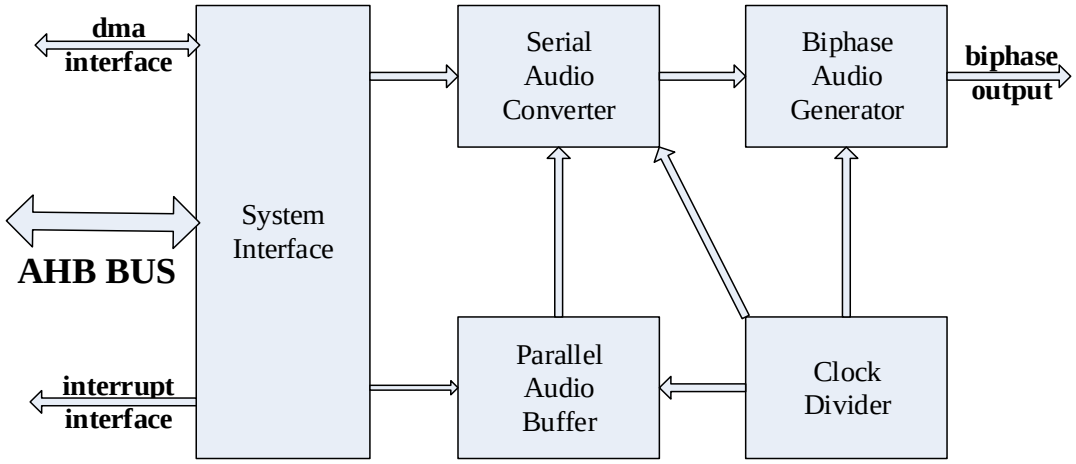



Fig. 23-1 SPDIF transmitter Block Diagram

The SPDIF transmitter is composed of following module.

**System Interface**

The system interface implements the AHB slave operation. It contains not only control registers of transmitters and receiver inside but also interrupt and DMA handshaking interface.

**Clock Divider**

The clock divider implements clock generation function. It divides the source clock MCLK to generate the working clock used for the digital audio data transformation and transmission.

**Parallel Audio Buffer**

The parallel audio buffer stores the audio data to be transmitted. The size of the FIFO is 32bits x 32.

**Serial Audio Converter**

The serial audio converter converts the parallel audio data from the parallel audio buffer to the serial audio data.

**Biphase Audio Generator**

The biphase audio generator reads serial audio data from the serial audio converter and generates biphase audio data based on IEC-60958 standard.

## 23.3 Function description

### 23.3.1 Frame Format

A frame is uniquely composed of two sub-frames. For linear coded audio applications, the rate of transmission of frames corresponds exactly to the source sampling frequency.
In the 2-channel operation mode, the samples taken from both channels are transmitted by time multiplexing in consecutive sub-frames. The first sub-frame(left channel in stereophonic operation and primary channel in monophonic operation) normally use preamble M. However, the preamble is changed to preamble B once every 192 frame to identify the start of the block structure used to organize the channel status information. The second sub-frame (right in stereophonic operation and secondary channel in monophonic operation) always use preamble W.

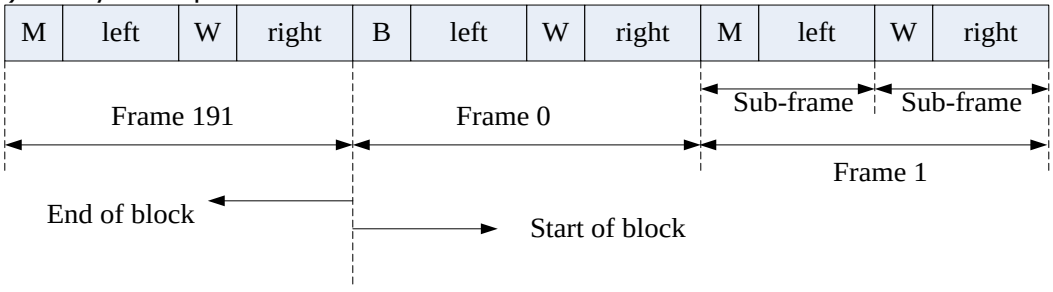



Fig. 23-2 SPDIF Frame Format

In the single channel operation mode in a professional application, the frame format is the

Copyright 2022 © Rockchip Electronics Co., Ltd.

same as in the 2-channel mode. Data is carried only in the first sub-frame and may be duplicated in the second sub-frame. If the second sub-frame is not carrying duplicate data, then time slot 28 (validity flag) shall be set to logical '1' (not valid).

### 23.3.2 Sub-frame Format

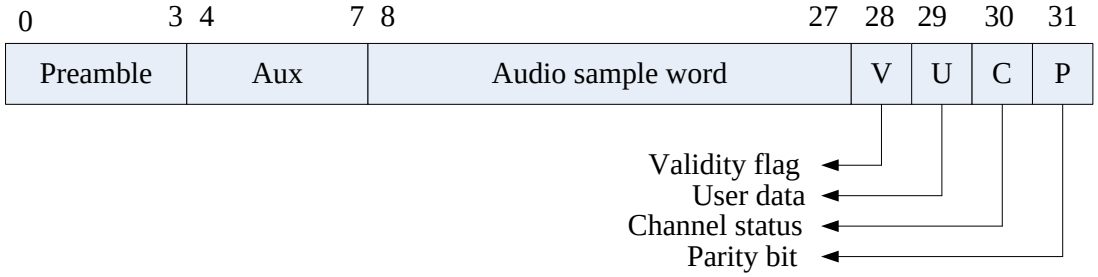



Fig. 23-3 SPDIF Sub-frame Format

Each sub-frame is divided into 32 time slots, numbered from 0 to 31. Time slot 0 to 3 carries one of the three permitted preambles. Time slot 4 to 27 carry the audio sample word in linear 2's complement representation. The MSB is carried by time slot 27. When a 24-bit coding range is used, the LSB is in time slot 4. When a 20-bit coding range is used, time slot 8 to 27 carry the audio sample word with the LSB in time slot 8.Time slot 4 to 7 may be used for other application. Under these circumstances, the bits in the time slot 4 to 7 are designated auxiliary sample bits.

If the source provides fewer bits than the interface allows (either 24 or 20), the unused LSBs are set to a logical '0'. For a non-linear PCM audio application or a data application the main data field may carry any other information. Time slot 28 carries the validity flag associated with the main data field. Time slot 29 carries 1 bit of the user data associated with the audio channel transmitted in the same sub-frame. Time slot 30 carries one bit of the channel status words associated with the main data field channel transmitted in the same sub-frame. Time slot 31 carries a parity bit such that time slots 4 to 31 inclusive carries an even number of ones and an even number of zeros.

### 23.3.3 Channel Coding

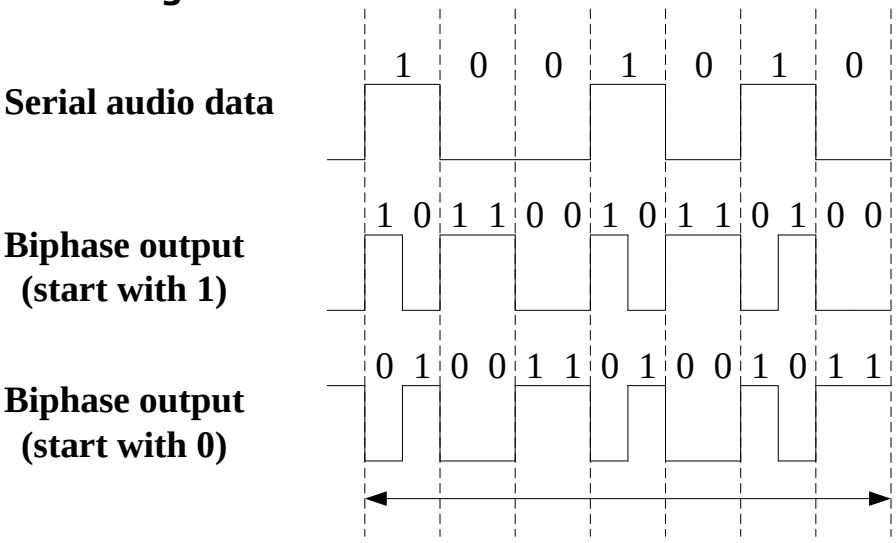



Fig. 23-4 SPDIF Channel Coding

To minimize the direct current component on the transmission line, to facilitate clock recovery from the data stream and to make the interface insensitive to the polarity of connections, time slots 4 to 31 are encoded in biphase-mark.

Each bit to be transmitted is represented by a symbol comprising two consecutive binary states. The first state of a symbol is always different from the second state of the previous symbol. The second state of the symbol is identical to the first if the bit to be transmitted is logical '0'.However, it is different from the first if the bit is logical '1'.

### 23.3.4 Preamble

Preambles are specific patterns providing synchronization and identification of the sub-frames and blocks.

Copyright 2022 © Rockchip Electronics Co., Ltd.

To achieve synchronization within one sampling period and to make this process completely reliable, these patterns violate the biphase-mark code rules, thereby avoiding the possibility of data imitating the preambles.
A set of three preambles is used. These preambles are transmitted in the time allocated to four time slots (time slots 0 to 3) and are represented by eight successive states. The first state of the preamble is always different from the second state of the previous symbol.

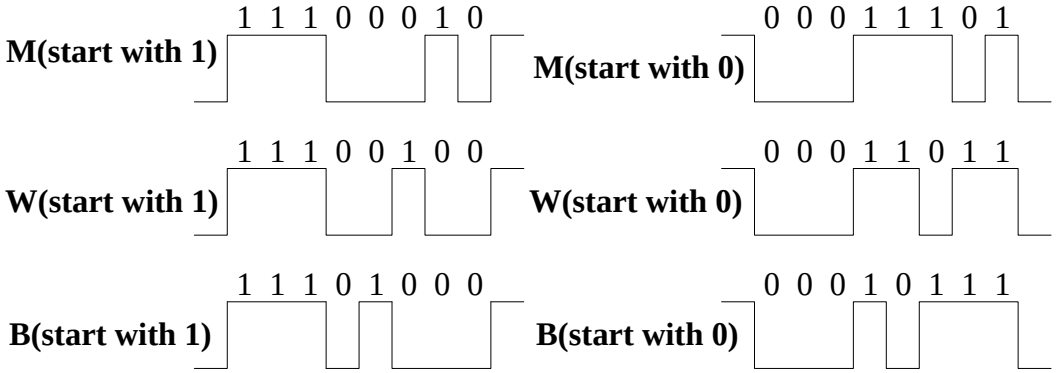



Fig. 23-5 SPDIF Preamble

Like biphase code, these preambles are dc free and provide clock recovery. They differ in at least two states from any valid biphase sequence.

# 23.4 Register Description

## 23.4.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| SPDIF_CFGR | 0x0000 | W | 0x00000000 | Transfer Configuration Register |
| SPDIF_SDBLR | 0x0004 | W | 0x00000000 | Sample Date Buffer Level Register |
| SPDIF_DMACR | 0x0008 | W | 0x00000000 | DMA Control Register |
| SPDIF_INTCR | 0x000C | W | 0x00000000 | Interrupt Control Register |
| SPDIF_INTSR | 0x0010 | W | 0x00000000 | Interrupt Status Register |
| SPDIF_XFER | 0x0018 | W | 0x00000000 | Transfer Start Register |
| SPDIF_SMPDR | 0x0020 | W | 0x00000000 | Sample Data Register |
| SPDIF_VLDFRn | 0x0060 | W | 0x00000000 | Validity Flag Register n(n=0~11) |
| SPDIF_USRDRn | 0x0090 | W | 0x00000000 | User Data Register n(n=0~11) |
| SPDIF_CHNSRn | 0x00C0 | W | 0x00000000 | Channel Status Register n(n=0~11) |
| SPDIF_BURTSINFO | 0x0100 | W | 0x00000000 | Channel Burst Info Register |
| SPDIF_REPETTION | 0x0104 | W | 0x00000000 | Channel Repetition Register |
| SPDIF_BURTSINFO_SHD | 0x0108 | W | 0x00000000 | Shadow Channel Burst Info Register |
| SPDIF_REPETTION_SHD | 0x010C | W | 0x00000000 | Shadow Channel Repetition Register |
| SPDIF_USRDR_SHDn | 0x0190 | W | 0x00000000 | Shadow User Data Register n(n=0~11) |
| SPDIF_VERSION | 0x01C0 | W | 0x20160100 | Version Register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 23.4.2 Detail Registers Description

### SPDIF_CFGR

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:16 | RW | 0x00 | MCD<br>Mclk divider<br>Mclk is the operation clock. This parameter can be calculated by (frequency of mclk)/(Fs*128). Fs=sample frequency |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | PCMTYPE<br>1'b0: Linear PCM<br>1'b1: Non-linear PCM |
| 7 | WO | 0x0 | CLR<br>Write 1'b1 to clear MCLK domain logic. Read return zero. |
| 6 | RW | 0x0 | CSE<br>Channel status enable.<br>1'b0: Disable.<br>1'b1: Enable.<br>The bit should be set to 1'b1 when the channel conveys non-linear PCM. |
| 5 | RW | 0x0 | UDE<br>User data enable.<br>1'b0: Disable. User data bit field is 1'b0.<br>1'b1: Enable. User data bit field is defined by SPDIF_VLDFRn. |
| 4 | RW | 0x0 | VFE<br>Validity data enable.<br>1'b0: Disable. Validity data bit field is 1'b0.<br>1'b1: Enable. For linear PCM mode, validity data bit field is defined by SPDIF_VLDFRn. For non-linear PCM mode, validity data bit field is 1'b1. |
| 3 | RW | 0x0 | ADJ<br>1'b0: Right justified<br>1'b1: Left justified<br>If right justified, audio data bit23~0(VDW=2'b10)/bit19~0(VDW=2'b01)/bit15~0(VDW=2'b00) will be the valid bit to be transmitted.<br>If left justified, audio data bit31~8(VDW=2'b10)/bit31~12(VDW=2'b01)/bit31~16(VDW=2'b00) will be the valid bit to be transmitted. |
| 2 | RW | 0x0 | HWT<br>1'b0: Disable<br>1'b1: Enable<br>It is valid only when the valid data width is 16bit. |
| 1:0 | RW | 0x0 | VDW<br>2'b00: 16bit<br>2'b01: 20bit<br>2'b10: 24bit<br>2'b11: Reserved<br>The valid data width is 16bit only for non-linear PCM. |

**SPDIF_SDBLR**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5:0 | RW | 0x00 | SDBLR<br>Contains the number of valid data entries in the sample data buffer. |

**SPDIF_DMACR**

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5 | RW | 0x0 | TDE<br>1'b0: Transmit DMA disabled.<br>1'b1: Transmit DMA enabled. |
| 4:0 | RW | 0x00 | TDL<br>This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level. That is, the dma_tx_req signal is generated when the number of valid data entries in the Sample Date Buffer is equal to or below this field value. |

**SPDIF_INTCR**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17 | W1C | 0x0 | UDTIC<br>Write 1'b1 to clear the user data interrupt. |
| 16 | W1C | 0x0 | BTTIC<br>Write 1'b1 to clear the block transfer finish interrupt. |
| 15:10 | RO | 0x00 | reserved |
| 9:5 | RW | 0x00 | SDBT<br>Sample date buffer threshold for empty interrupt. |
| 4 | RW | 0x0 | SDBEIE<br>Sample data buffer empty interrupt enable.<br>1'b0: Disable<br>1'b1: Enable<br>Sample data buffer empty interrupt will generate if interrupt is enabled and the number of entries is lower than threshold of empty interrupt. |
| 3 | RW | 0x0 | BTTIE<br>Block transfer finish interrupt enable.<br>1'b0: Disable<br>1'b1: Enable<br>When enabled, an interrupt will assert when the block transfer is finished if the channel conveys linear PCM or when the repetition period is reached if the channel conveys non-linear PCM. |
| 2 | RW | 0x0 | UDTIE<br>User data interrupt enable.<br>1'b0: Disable<br>1'b1: Enable<br>If enabled, an interrupt will assert when the content of the user data register is fed into the corresponding shadow register. |
| 1:0 | RO | 0x0 | reserved |

**SPDIF_INTSR**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4 | RO | 0x0 | SDBEIS<br>Sample data buffer empty interrupt status.<br>1'b0: Inactive<br>1'b1: Active |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RO | 0x0 | BTTIS<br>Block transfer finish interrupt status.<br>1'b0: Inactive<br>1'b1: Active |
| 2 | RO | 0x0 | UDTIS<br>User data interrupt status.<br>1'b0: Inactive<br>1'b1: Active |
| 1:0 | RO | 0x0 | reserved |

**SPDIF_XFER**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | XFER<br>Transfer start. |

**SPDIF_SMPDR**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | WO | 0x00000000 | SMPDR<br>Sample data written to this register will be pushed into internal transfer buffer. |

**SPDIF_VLDFRn**

Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | VLDFR_SUB_1<br>Validity flag for subframe 1 |
| 15:0 | RW | 0x0000 | VLDFR_SUB_0<br>Validity flag for subframe 0 |

**SPDIF_USRDRn**

Address: Operational Base + offset (0x0090)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | USR_SUB_1<br>User data bit for subframe 1 |
| 15:0 | RW | 0x0000 | USR_SUB_0<br>User data bit for subframe 0 |

**SPDIF_CHNSRn**

Address: Operational Base + offset (0x00C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | CHNSR_SUB_1<br>Channel status bit for subframe 1 |
| 15:0 | RW | 0x0000 | CHNSR_SUB_0<br>Channel status bit for subframe 0 |

**SPDIF_BURTSINFO**

Address: Operational Base + offset (0x0100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | PD<br>Preamble Pd for non-linear PCM, indicating the length of burst payload in unit of bytes or bits. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:13 | RW | 0x0 | BSNUM<br>This field indicates the bitstream number. Usually the bitstream number is 0. |
| 12:8 | RW | 0x00 | DATAINFO<br>This field gives the data-type-dependent info. |
| 7 | RW | 0x0 | ERRFLAG<br>1'b0: Indicates a valid burst-payload.<br>1'b1: Indicates that the burst-payload may contain errors. |
| 6:0 | RW | 0x00 | DATATYPE<br>7'b0000000: Null data<br>7'b0000001: AC-3 data<br>7'b0000011: Pause data<br>7'b0000100: MPEG-1 layer 1 data<br>7'b0000101: MPEG-1 layer 2 or 3 data or MPEG-2 without extension<br>7'b0000110: MPEG-2 data with extension<br>7'b0000111: MPEG-2 AAC<br>7'b0001000: MPEG-2, layer-1 low sampling frequency<br>7'b0001001: MPEG-2, layer-2 low sampling frequency<br>7'b0001010: MPEG-2, layer-3 low sampling frequency<br>7'b0001011: DTS type I<br>7'b0001100: DTS type II<br>7'b0001101: DTS type III<br>7'b0001110: ATRAC<br>7'b0001111: ATRAC 2/3<br>7'b0010000: ATRAC-X<br>7'b0010001: DTS type IV<br>7'b0010010: WMA professional type I<br>7'b0110010: WMA professional type II<br>7'b1010010: WMA professional type III<br>7'b1110010: WMA professional type IV<br>7'b0010011: MPEG-2 AAC low sampling frequency<br>7'b0110011: MPEG-2 AAC low sampling frequency<br>7'b1010011: MPEG-2 AAC low sampling frequency<br>7'b1110011: MPEG-2 AAC low sampling frequency<br>7'b0010100: MPEG-4 AAC<br>7'b0110100: MPEG-4 AAC<br>7'b1010100: MPEG-4 AAC<br>7'b1110100: MPEG-4 AAC<br>7'b0010101: Enhanced AC-3<br>7'b0010110: MAT<br>Others: Reserved |

**SPDIF_REPETTION**

Address: Operational Base + offset (0x0104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | REPETTION<br>This defines the repetition period when the channel conveys non-linear PCM. |

**SPDIF_BURTSINFO_SHD**

Address: Operational Base + offset (0x0108)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | PD<br>Preamble Pd for non-linear PCM, indicating the length of burst payload in unit of bytes or bits. |
| 15:13 | RO | 0x0 | BSNUM<br>This field indicates the bitstream number. Usually the bitstream number is 0. |
| 12:8 | RO | 0x00 | DATAINFO<br>This field gives the data-type-dependent info. |
| 7 | RO | 0x0 | ERRFLAG<br>1'b0: Indicates a valid burst-payload.<br>1'b1: Indicates that the burst-payload may contain errors. |
| 6:0 | RO | 0x00 | DATATYPE<br>7'b0000000: Null data<br>7'b0000001: AC-3 data<br>7'b0000011: Pause data<br>7'b0000100: MPEG-1 layer 1 data<br>7'b0000101: MPEG-1 layer 2 or 3 data or MPEG-2 without extension<br>7'b0000110: MPEG-2 data with extension<br>7'b0000111: MPEG-2 AAC<br>7'b0001000: MPEG-2, layer-1 low sampling frequency<br>7'b0001001: MPEG-2, layer-2 low sampling frequency<br>7'b0001010: MPEG-2, layer-3 low sampling frequency<br>7'b0001011: DTS type I<br>7'b0001100: DTS type II<br>7'b0001101: DTS type III<br>7'b0001110: ATRAC<br>7'b0001111: ATRAC 2/3<br>7'b0010000: ATRAC-X<br>7'b0010001: DTS type IV<br>7'b0010010: WMA professional type I<br>7'b0110010: WMA professional type II<br>7'b1010010: WMA professional type III<br>7'b1110010: WMA professional type IV<br>7'b0010011: MPEG-2 AAC low sampling frequency<br>7'b0110011: MPEG-2 AAC low sampling frequency<br>7'b1010011: MPEG-2 AAC low sampling frequency<br>7'b1110011: MPEG-2 AAC low sampling frequency<br>7'b0010100: MPEG-4 AAC<br>7'b0110100: MPEG-4 AAC<br>7'b1010100: MPEG-4 AAC<br>7'b1110100: MPEG-4 AAC<br>7'b0010101: Enhanced AC-3<br>7'b0010110: MAT<br>Others: Reserved |

**SPDIF_REPETTION_SHD**

Address: Operational Base + offset (0x010C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RO | 0x0000 | REPETTION<br>This register provides the repetition of the bitstream when channel conveys non-linear PCM. It defines the length between Pa of the two consecutive data-burst. For the same audio format, the definition is different. Please convert the actual repetition in order to comply with the design. |

**SPDIF_USRDR_SHDn**

Address: Operational Base + offset (0x0190)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | USR_SUB_1<br>User data bit for subframe 1 |
| 15:0 | RO | 0x0000 | USR_SUB_0<br>User data bit for subframe 0 |

**SPDIF_VERSION**

Address: Operational Base + offset (0x01C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x20160100 | VER<br>Version of SPDIF |

## 23.5 Interface Description

SPDIF0 and SPDIF1 are used to communicate with audio equipment outside this chip. Following table shows the interface of SPDIF0 and SPDIF1.

Table 23-2 SPDIF0 Interface Description

| Module Pin | Dir | PIN Name | IOMUX Setting |
|---|---|---|---|
| spdif0_sdo | O | MIPI_CAMERA1_CLK_M0/SPDIF0_TX_M0/PCIE30X2_WAKEN_M3/HDMI_RX_HPDOUT_M2/I2C5_SCL_M3/UART1_TX_M1/GPIO1_B6_d | BUS_IOC_GPIO1B_IOMUX_SEL_H[11:8]=4'h3 |
| ~spdif0_sdo/ spdif0_sdo | O | CIF_CLKOUT/BT1120_D10/I2S1_SDO3_M0/PCIE30X4_CLKREQN_M1/DP0_HPDIN_M0/SPDIF0_TX_M1/UART9_TX_M1/PWM11_IR_M1/GPIO4_B4_u | BUS_IOC_GPIO4B_IOMUX_SEL_H[3:0]=4'h6 |

*Notes: I=input, O=output, I/O=input/output, bidirectional, ~spdif0_sdo means inverse of spdif0_sdo*

*SYS_GRF_SOC_CON1[15] controls whether ~spdif0_sdo or spdif0_sdo is connected to SPDIF0_TX_M1/UART9_TX_M1/PWM11_IR_M1/GPIO4_B4_u.*

Table 23-3 SPDIF1 Interface Description

| Module Pin | Dir | PIN Name | IOMUX Setting |
|---|---|---|---|
| spdif1_sdo | O | MIPI_CAMERA2_CLK_M0/SPDIF1_TX_M0/PCIE30X2_PERSTN_M3/HDMI_RX_CEC_M2/SATA2_ACT_LED_M1/I2C5_SDA_M3/UART1_RX_M1/PWM13_M2/GPIO1_B7_u | BUS_IOC_GPIO1B_IOMUX_SEL_H[15:12]=4'h3 |
| spdif1_sdo | O | MIPI_CAMERA0_CLK_M0/SPDIF1_TX_M1/I2S1_SDO0_M0/PCIE30X1_0_BUTTON_RSTN/SATA2_ACT_LED_M0/I2C6_SCL_M3/UART8_RX_M0/SPI0_CS1_M1/GPIO4_B1_u | BUS_IOC_GPIO4B_IOMUX_SEL_L[7:4]=4'h2 |
| spdif1_sdo | O | BT1120_D15/SPDIF1_TX_M2/PCIE20X1_2_PERSTN_M1/HDMI_TX0_CEC_M0/I2C8_SDA_M3/PWM6_M1/SPI3_CS1_M1/GPIO4_C1_d | BUS_IOC_GPIO4C_IOMUX_SEL_L[7:4]=4'h3 |

*Notes: I=input, O=output, I/O=input/output, bidirectional*

*The output of SPDIF3 are internally connected to EDP TX Controller0 and HDMI TX Controller0 respectively. The SPDIF audio interface of EDP TX Controller0 and HDMI TX Controller0 can work at the same time. If GRF_VO1_CON0[4] is set 1'b1, then the output of SPDIF3 are connected to*

Copyright 2022 © Rockchip Electronics Co., Ltd. 

*EDP TX Controller0. If GRF_VO1_CON3[14] is set 1'b1, then the output of SPDIF3 are connected to HDMI TX Controller0.*
*The output of SPDIF4 are internally connected to EDP TX Controller1 and HDMI TX Controller1 respectively. The SPDIF audio interface of EDP TX Controller1 and HDMI TX Controller1 can work at the same time. If GRF_VO1_CON1[4] is set 1'b1, then the output of SPDIF4 are connected to EDP TX Controller1. If GRF_VO1_CON6[14] is set 1'b1, then the output of SPDIF3 are connected to HDMI TX Controller1.*
*The output of SPDIF2 are internally connected to DPTX0. DPTX0 SPDIF audio interface operation clock and MCLK of SPDIF2 are from the same source. MCLK of SPDIF2 should be divided by 4 by programming SPDIF_CFGR.MCD to 3 to meet the requirement that DPTX0 SPDIF audio interface operates at 4 times frequency over sample the output of SPDIF2. SPDIF5 is similar with SPDIF2 except that SPDIF5 is connected to DPTX1.*

## 23.6 Application Notes

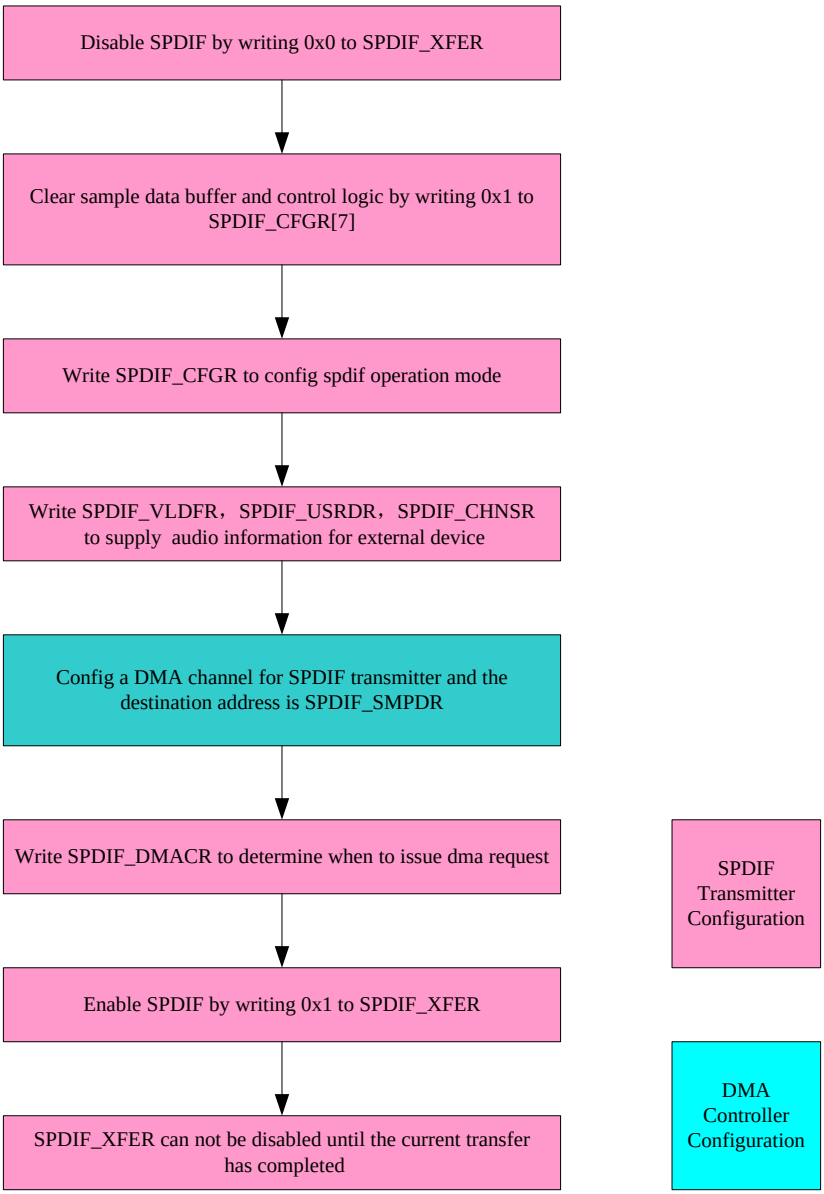



Fig. 23-6 SPDIF transmitter operation flow chart

The above figure shows the operation flow of SPDIF operation. Note that the configuration register can be written only when the transfer is stopped.

Copyright 2022 © Rockchip Electronics Co., Ltd.

# Chapter 24 SPDIF Receiver

## 24.1 Overview

The SPDIF receiver is a self-clocking, serial, unidirectional interface for the interconnection of digital audio equipment for consumer and professional applications, using linear PCM coded audio samples.
It provides the basic structure of the interface. Separate documents define items specific to particular applications.
When used in a professional application, the interface is primarily intended to receive monophonic or stereophonic programmes, at a 48 kHz sampling frequency and with a resolution of up to 24bits per sample; it may alternatively be used to receive signals sampled at 32 kHz or 44.1 kHz.
When used in a consumer application, the interface is primarily intended to receive stereophonic programmes, with a resolution of up to 24 bits per sample.
When used for other purposes, the interface is primarily intended to receive audio data coded other than as linear PCM coded audio samples. Provision is also made to allow the interface to receive data related to computer software or signals coded using non-linear PCM. The format specification for these applications is not part of this standard.
There are 3 SPDIF receivers(SPDIF_RX) in total. That are SPDIF_RX0, SPDIF_RX1 and SPDIF_RX2. Each of them supports following features.

- Support AHB Bus Interface
- Support one internal 30-bit wide and 32-location deep FIFO for receiving audio data
- Support combined interrupt output
- Support DMA handshaking interface and configurable DMA water level
- Support liner PCM(IEC60958) and non-liner PCM(IEC61937)
- Support 16~24 bits audio sample length for liner PCM application
- Support 16 bits audio sample length for non-liner PCM application
- Support up to 384kHz sample rate with the corresponding reference clock equal to 384KHz*64*2*10, that is 491.52MHz
- Support the frequency of reference clock is at least 10 times the frequency of the biphase encoding clock, but not more than 256 times
- Support recovering clock and audio data from input bitstream

## 24.2 Block Diagram

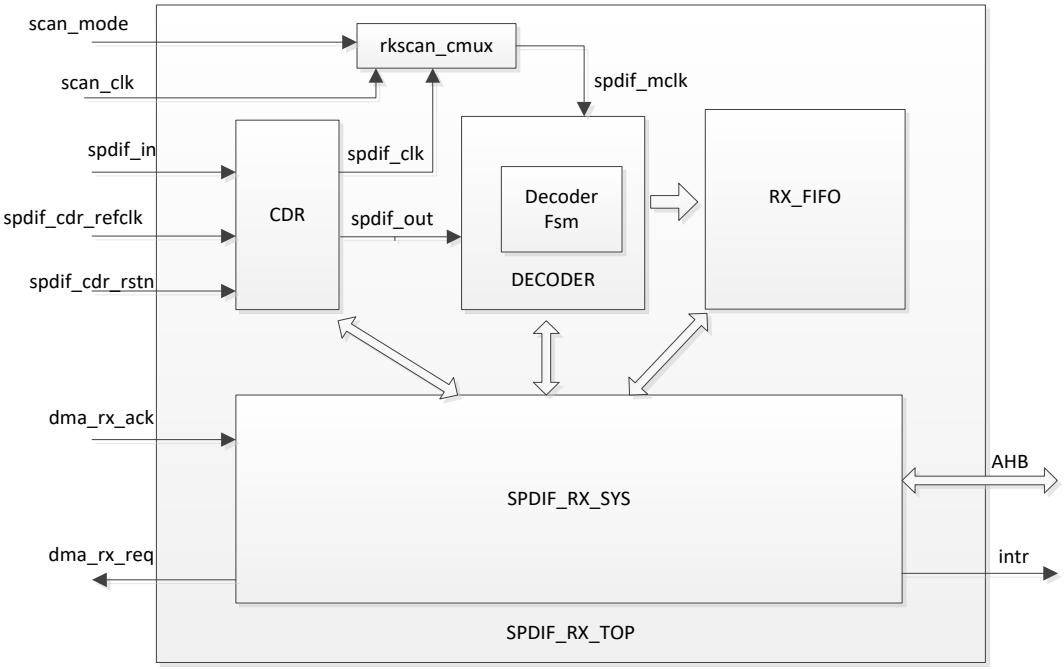



Fig. 24-1 SPDIF receiver Block Diagram

The SPDIF receiver is composed of following modules.

Copyright 2022 © Rockchip Electronics Co., Ltd.

**SPDIF_RX_SYS**
The module implements the AHB slave operation. It contains not only control registers of SPDIF receiver inside but also interrupt and DMA handshaking interface.
**CDR**
The CDR is short for clock and data recovery. Clock and data can be recovered from the input bitstream by using a high frequency reference clock.
**DECODER**
The clock recovered from the CDR is used as the working clock to decode the input bitstream such as extracting audio data, the corresponding preamble code, V/U/C/P flags and other audio information.
**RX_FIFO**
The RX FIFO stores the audio data extracted from input bitstream. The size of the FIFO is 30bitsx32.

# 24.3 Function description

## 24.3.1 Frame Format

SPDIF receiver follows the same protocol(IEC60958/IEC61937) as SPDIF transmitter. A frame is uniquely composed of two sub-frames. For linear coded audio applications, the rate of receiving of frames corresponds exactly to the source sampling frequency.
In the 2-channel operation mode, the samples received from both channels are arranged by time multiplexing in consecutive sub-frames. The first subframe(left channel in stereophonic operation and primary channel in monophonic operation) normally use preamble M. However, the preamble is changed to preamble B once every 192 frame to identify the start of the block structure used to organize the channel status information. The second sub-frame (right in stereophonic operation and secondary channel in monophonic operation) always use preamble W.

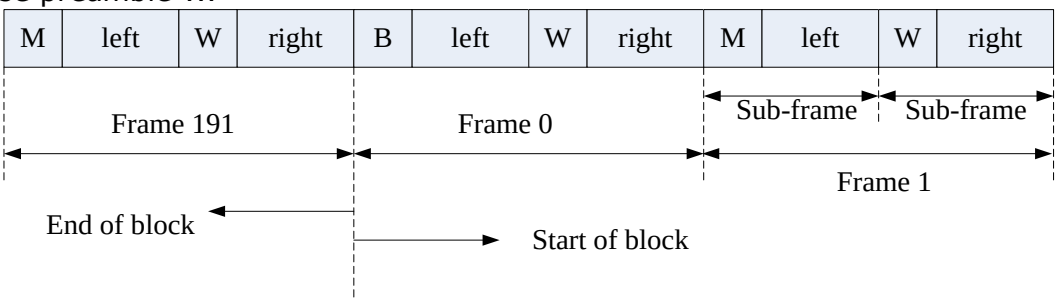



Fig. 24-2 SPDIF Frame Format

In the single channel operation mode in a professional application, the frame format is the same as in the 2-channel mode. Data is carried only in the first sub-frame and may be duplicated in the second sub-frame. If the second sub-frame is not carrying duplicate data, then time slot 28 (validity flag) shall be set to logical '1' (not valid).

## 24.3.2 Sub-frame Format

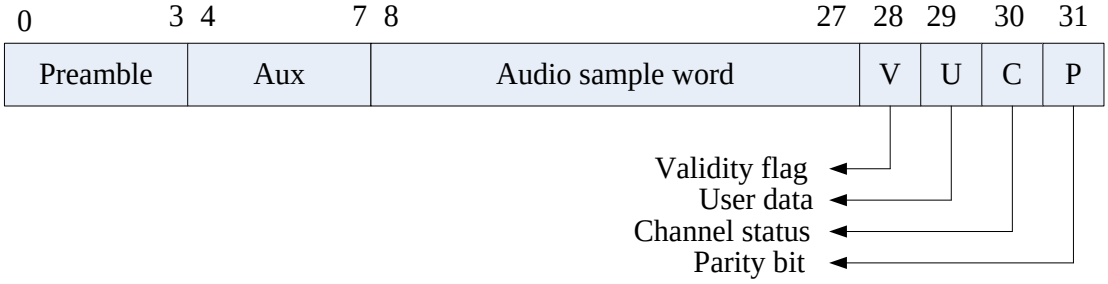



Fig. 24-3 SPDIF Sub-frame Format

Each sub-frame is divided into 32 time slots, numbered from 0 to 31. Time slot 0 to 3 carries one of the three permitted preambles. Time slot 4 to 27 carry the audio sample word in linear 2's complement representation. The MSB is carried by time slot 27. When a 24-bit coding range is used, the LSB is in time slot 4. When a 20-bit coding range is used, time slot 8 to 27 carry the audio sample word with the LSB in time slot 8. Time slot 4 to 7 may be

Copyright 2022 © Rockchip Electronics Co., Ltd. 

used for other application. Under these circumstances, the bits in the time slot 4 to 7 are designated auxiliary sample bits.
If the source provides fewer bits than the interface allows (either 24 or 20), the unused LSBs are set to a logical '0'. For a non-linear PCM audio application or a data application the main data field may carry any other information. Time slot 28 carries the validity flag associated with the main data field. Time slot 29 carries 1 bit of the user data associated with the audio channel transmitted in the same sub-frame. Time slot 30 carries one bit of the channel status words associated with the main data field channel transmitted in the same sub-frame. Time slot 31 carries a parity bit such that time slots 4 to 31 inclusive carries an even number of ones and an even number of zeros.

### 24.3.3 Channel Coding

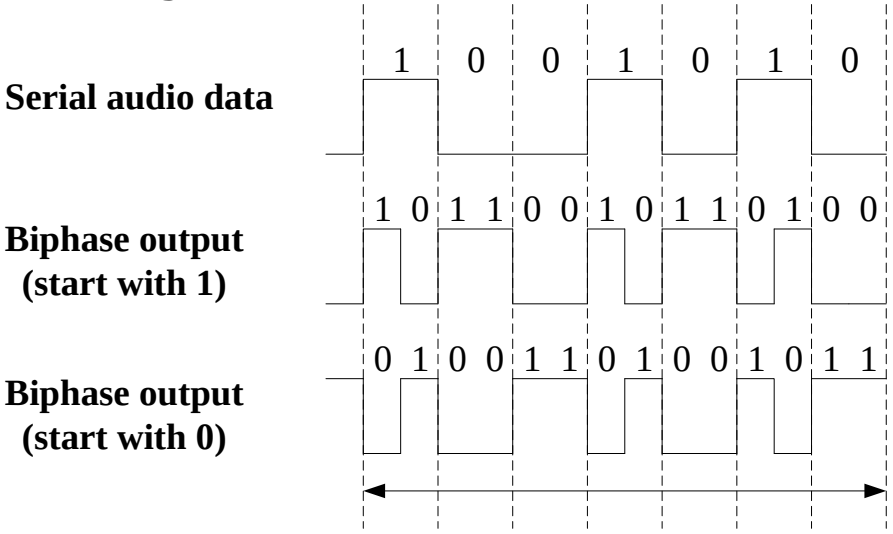



Fig. 24-4 SPDIF Channel Coding

To minimize the direct current component on the transmission/receiving line, to facilitate clock recovery from the data stream and to make the interface insensitive to the polarity of connections, time slots 4 to 31 are encoded in biphase-mark.
Each bit to be transmitted is represented by a symbol comprising two consecutive binary states. The first state of a symbol is always different from the second state of the previous symbol. The second state of the symbol is identical to the first if the bit to be transmitted is logical '0'.However, it is different from the first if the bit is logical '1'.

### 24.3.4 Preamble

Preambles are specific patterns providing synchronization and identification of the sub-frames and blocks.
To achieve synchronization within one sampling period and to make this process completely reliable, these patterns violate the biphase-mark code rules, thereby avoiding the possibility of data imitating the preambles.
A set of three preambles is used. These preambles are transmitted in the time allocated to four time slots (time slots 0 to 3) and are represented by eight successive states. The first state of the preamble is always different from the second state of the previous symbol.

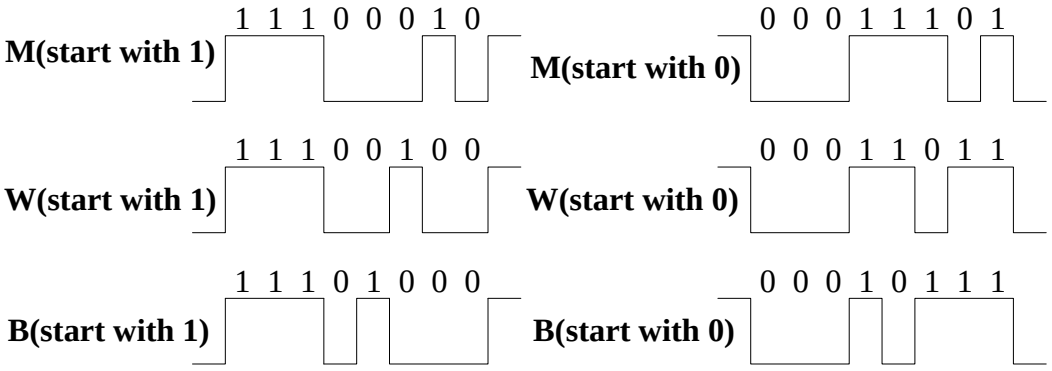



Fig. 24-5 SPDIF Preamble

Like biphase code, these preambles are dc free and provide clock recovery. They differ in at

least two states from any valid biphase sequence.

# 24.4 Register Description

## 24.4.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| SPDIF_RX_VERSION | 0x0000 | W | 0x00000100 | Version Register |
| SPDIF_RX_CFGR | 0x0004 | W | 0x00000000 | Transfer Configuration Register |
| SPDIF_RX_CLR | 0x0008 | W | 0x00000000 | Clear Register |
| SPDIF_RX_CDR | 0x000C | W | 0x000000A1 | Clock And Data Recovery Register |
| SPDIF_RX_CDRST | 0x0010 | W | 0x03FF00FF | Clock And Data Recovery Status Register |
| SPDIF_RX_DMACR | 0x0014 | W | 0x00000000 | DMA Control Register |
| SPDIF_RX_FIFOCTRL | 0x0018 | W | 0x00000000 | FIFO Control Register |
| SPDIF_RX_INTEN | 0x001C | W | 0x00000000 | Interrupt Enable Register |
| SPDIF_RX_INTMASK | 0x0020 | W | 0x00000000 | Interrupt Mask Register |
| SPDIF_RX_INTSR | 0x0024 | W | 0x00000000 | Interrupt Status Register |
| SPDIF_RX_INTCLR | 0x0028 | W | 0x00000000 | Interrupt Clear Register |
| SPDIF_RX_SMPDR | 0x002C | W | 0x00000000 | Sample Data Register |
| SPDIF_RX_USRDRn | 0x0030 | W | 0x00000000 | User Data Register n(n=0~11) |
| SPDIF_RX_CHNSRn | 0x0060 | W | 0x00000000 | Channel Status Register n(n=0~11) |
| SPDIF_RX_BURTSINFO | 0x0100 | W | 0x00000000 | Channel Burst Info Register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 24.4.2 Detail Registers Description

### SPDIF_RX_VERSION

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000100 | VER<br>Version of SPDIF_RX |

### SPDIF_RX_CFGR

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | TWAD<br>1'b0: Only audio data transmitted to FIFO.<br>1'b1: Block start, channel number and VUCP transmitted with audio data to FIFO. |
| 0 | RW | 0x0 | EN<br>1'b0: Disable SPDIF_RX<br>1'b1: Enable SPDIF_RX |

### SPDIF_RX_CLR

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | RXSC<br>This is a software self-cleared bit. Write 1'b1 to clear all receive logic. |

**SPDIF_RX_CDR**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x00 | reserved |
| 24 | RW | 0x0 | JITTRSH<br>CDR jitter threshold. It is valid only when BYPASS is 1'b0. |
| 23:16 | RW | 0x00 | MIDRGE<br>CDR jitter middle range. It is valid only when BYPASS is 1'b0. |
| 15:11 | RO | 0x00 | reserved |
| 10:9 | RO | 0x0 | CS<br>CDR state<br>2'b00: Idle state. CDR is idle and waits for rising edge of SPDIF_RX input bitstream.<br>2'b01: Detect state<br>2'b10: Measurement state<br>2'b11: Synchronization state |
| 8:7 | RO | 0x1 | JITST<br>CDR jitter status<br>2'b01: Low<br>2'b10: High<br>2'b11: Normal<br>It is valid only when BYPASS is 1'b0. |
| 6 | RO | 0x0 | FULL<br>CDR FIFO full status.<br>1'b0: Not full<br>1'b1: Full |
| 5 | RO | 0x1 | EMPTY<br>CDR FIFO empty status.<br>1'b0: Not empty<br>1'b1: Empty |
| 4:2 | RW | 0x0 | AVGWIN<br>Average the non-jitter recovered clk from bitstream at a period of AVGWIN time. |
| 1 | RW | 0x0 | AVGSEL<br>Select if the min or average number of cycles from the calculation of SPDIF_RX input bitstream pulse width.<br>1'b0: Minimum number of cycles<br>1'b1: Average number of cycles, that is (max+min)/4. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x1 | BYPASS<br>Write 1'b1 to enable CDR non-jitter bypass mode. It's recommended that this bit set to 1'b1. Please ensure that this bit is set to 1'b1 before starting receiving data. |

**SPDIF_RX_CDRST**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x03ff | NOSTRTHR<br>The threshold counter determines the latency between input bitstream idle and exit synchronous status. Make sure that this value is large than 16'h03ff. |
| 15:8 | RO | 0x00 | MAXCNT<br>The value indicates the number of reference clock cycles to oversample the maximum pulse width of bitstream. |
| 7:0 | RO | 0xff | MINCNT<br>The value indicates the number of reference clock cycles to oversample the minimum pulse width of bitstream. |

**SPDIF_RX_DMACR**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5 | RW | 0x0 | RDE<br>1'b0: Receive DMA disabled.<br>1'b1: Receive DMA enabled. |
| 4:0 | RW | 0x00 | RDL<br>This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1. That is, dma_rx_req is generated when the number of valid data entries in the sample date buffer is equal to or above this field value + 1. |

**SPDIF_RX_FIFOCTRL**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RO | 0x00000 | reserved |
| 13:8 | RO | 0x00 | RFL<br>Contains the number of valid data entries in the receive FIFO. |
| 7:5 | RO | 0x0 | reserved |
| 4:0 | RW | 0x00 | RFT<br>When the number of receive FIFO entries is more than or equal to this threshold plus 1, the receive FIFO full interrupt is triggered. |

**SPDIF_RX_INTEN**

Address: Operational Base + offset (0x001C)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:11 | RO | 0x000000 | reserved |
| 10 | RW | 0x0 | UBCIE<br>1'b0: Disable<br>1'b1: Enable<br>If enabled, an interrupt will generate if current user bit is different from previous one. |
| 9 | RW | 0x0 | ESYNCIE<br>1'b0: Disable<br>1'b1: Enable<br>If enabled, an interrupt will generate when entering synchronous state. |
| 8 | RW | 0x0 | BTEIE<br>1'b0: Disable<br>1'b1: Enable<br>When enabled, an interrupt will generate when the block receive is finished if the channel conveys linear PCM or when the repetition period is reached if the channel conveys non-linear PCM. |
| 7 | RW | 0x0 | NSYNCIE<br>1'b0: Disable<br>1'b1: Enable<br>If enabled, an interrupt will generate if CDR change from synchronization state to idle state. |
| 6 | RW | 0x0 | BMDEIE<br>1'b0: Disable<br>1'b1: Enable<br>If enabled, an interrupt will generate if a bi-phase mark decoding error has occurred. |
| 5 | RW | 0x0 | RXOIE<br>1'b0: Disable<br>1'b1: Enable<br>If enabled, an interrupt will generate if CDR FIFO is overrun. |
| 4 | RW | 0x0 | RXFIE<br>1'b0: Disable<br>1'b1: Enable<br>If enabled, an interrupt will generate if CDR FIFO is full. |
| 3 | RW | 0x0 | NPSPIE<br>1'b0: Disable<br>1'b1: Enable<br>If enabled, an interrupt will generate if non-liner PCM sync word is received. |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | NVLDIE<br>1'b0: Disable<br>1'b1: Enable<br>If enabled, an interrupt will generate if validity bit received from bitstream is 1'b1. |
| 1 | RW | 0x0 | CSCIE<br>1'b0: Disable<br>1'b1: Enable<br>If enabled, an interrupt will generate if current channel status bit is different from previous one. |
| 0 | RW | 0x0 | PEIE<br>1'b0: Disable<br>1'b1: Enable<br>If enabled, an interrupt will generate if a parity error has occurred. |

**SPDIF_RX_INTMASK**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:11 | RO | 0x000000 | reserved |
| 10 | RW | 0x0 | UBCIMSK<br>1'b0: Unmask<br>1'b1: Mask |
| 9 | RW | 0x0 | ESYNCIMSK<br>1'b0: Unmask<br>1'b1: Mask |
| 8 | RW | 0x0 | BTEIMSK<br>1'b0: Unmask<br>1'b1: Mask |
| 7 | RW | 0x0 | NSYNCIMSK<br>1'b0: Unmask<br>1'b1: Mask |
| 6 | RW | 0x0 | BMDEIMSK<br>1'b0: Don't mask<br>1'b1: Mask |
| 5 | RW | 0x0 | RXOIMSK<br>1'b0: Unmask<br>1'b1: Mask |
| 4 | RW | 0x0 | RXFIMSK<br>1'b0: Unmask<br>1'b1: Mask |
| 3 | RW | 0x0 | NPSPIMSK<br>1'b0: Unmask<br>1'b1: Mask |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | NVLDIMSK<br>1'b0: Don't mask<br>1'b1: Mask |
| 1 | RW | 0x0 | CSCIMSK<br>1'b0: Unmask<br>1'b1: Mask |
| 0 | RW | 0x0 | PEIMSK<br>1'b0: Unmask<br>1'b1: Mask |

**SPDIF_RX_INTSR**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:11 | RO | 0x000000 | reserved |
| 10 | RO | 0x0 | UBCISR<br>1'b0: Inactive<br>1'b1: Active |
| 9 | RO | 0x0 | ESYNCISR<br>1'b0: Inactive<br>1'b1: Active |
| 8 | RO | 0x0 | BTEISR<br>1'b0: Inactive<br>1'b1: Active |
| 7 | RO | 0x0 | NSYNCISR<br>1'b0: Inactive<br>1'b1: Active |
| 6 | RO | 0x0 | BMDEISR<br>1'b0: Inactive<br>1'b1: Active |
| 5 | RO | 0x0 | RXOIS<br>1'b0: Inactive<br>1'b1: Active |
| 4 | RO | 0x0 | RXFIS<br>1'b0: Inactive<br>1'b1: Active |
| 3 | RO | 0x0 | NPSPIS<br>1'b0: Inactive<br>1'b1: Active |
| 2 | RO | 0x0 | NVLDIS<br>1'b0: Inactive<br>1'b1: Active |
| 1 | RO | 0x0 | CSCIS<br>1'b0: Inactive<br>1'b1: Active |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RO | 0x0 | PEIS<br>1'b0: Inactive<br>1'b1: Active |

**SPDIF_RX_INTCLR**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:11 | RO | 0x000000 | reserved |
| 10 | RW | 0x0 | UBCICLR<br>Write 1'b1 to clear user bit change interrupt. |
| 9 | RW | 0x0 | ESYNCICLR<br>Write 1'b1 to clear entering synchronous state interrupt. |
| 8 | RW | 0x0 | BTEICLR<br>Write 1'b1 to clear block transfer/repetition period end interrupt. |
| 7 | RW | 0x0 | NSYNCICLR<br>Write 1'b1 to clear CDR not synchronization interrupt. |
| 6 | RW | 0x0 | BMDEICLR<br>Write 1'b1 to clear bi-phase mark decoding interrupt. |
| 5 | RW | 0x0 | RXOICLR<br>Write 1'b1 to clear receive overrun interrupt. |
| 4 | RW | 0x0 | RXFICLR<br>Write 1'b1 to clear receive full interrupt. |
| 3 | RW | 0x0 | NPSPICLR<br>Write 1'b1 to clear non-liner PCM sync word received interrupt. |
| 2 | RW | 0x0 | NVLDICLR<br>Write 1'b1 to clear validity bit received interrupt. |
| 1 | RW | 0x0 | CSCICLR<br>Write 1'b1 to clear channel status change interrupt. |
| 0 | RW | 0x0 | PEICLR<br>Write 1'b1 to clear parity error interrupt. |

**SPDIF_RX_SMPDR**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | SMPDR<br>Sample Data Register |

**SPDIF_RX_USRDRn**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | USR_SUB_1<br>User data bit for subframe 1 |
| 15:0 | RO | 0x0000 | USR_SUB_0<br>User data bit for subframe 0 |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**SPDIF_RX_CHNSRn**

Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | CHNSR_SUB_1<br>Channel status bit for subframe 1 |
| 15:0 | RO | 0x0000 | CHNSR_SUB_0<br>Channel status bit for subframe 0 |

**SPDIF_RX_BURTSINFO**

Address: Operational Base + offset (0x0100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | PD<br>Preamble Pd for non-linear PCM, indicating the length of burst payload in unit of bytes or bits. |
| 15:13 | RW | 0x0 | BSNUM<br>This field indicates the bitstream number. Usually the bitstream number is 0. |
| 12:8 | RO | 0x00 | DATAINFO<br>This field gives the data-type-dependent info. |
| 7 | RO | 0x0 | ERRFLAG<br>1'b0: Indicates a valid burst-payload.<br>1'b1: Indicates that the burst-payload may contain errors. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6:0 | RO | 0x00 | DATATYPE<br>7'b0000000: Null data<br>7'b0000001: AC-3 data<br>7'b0000011: Pause data<br>7'b0000100: MPEG-1 layer 1 data<br>7'b0000101: MPEG-1 layer 2 or 3 data or MPEG-2 without extension<br>7'b0000110: MPEG-2 data with extension<br>7'b0000111: MPEG-2 AAC<br>7'b0001000: MPEG-2, layer-1 low sampling frequency<br>7'b0001001: MPEG-2, layer-2 low sampling frequency<br>7'b0001010: MPEG-2, layer-3 low sampling frequency<br>7'b0001011: DTS type I<br>7'b0001100: DTS type II<br>7'b0001101: DTS type III<br>7'b0001110: ATRAC<br>7'b0001111: ATRAC 2/3<br>7'b0010000: ATRAC-X<br>7'b0010001: DTS type IV<br>7'b0010010: WMA professional type I<br>7'b0110010: WMA professional type II<br>7'b1010010: WMA professional type III<br>7'b1110010: WMA professional type IV<br>7'b0010011: MPEG-2 AAC low sampling frequency<br>7'b0110011: MPEG-2 AAC low sampling frequency<br>7'b1010011: MPEG-2 AAC low sampling frequency<br>7'b1110011: MPEG-2 AAC low sampling frequency<br>7'b0010100: MPEG-4 AAC<br>7'b0110100: MPEG-4 AAC<br>7'b1010100: MPEG-4 AAC<br>7'b1110100: MPEG-4 AAC<br>7'b0010101: Enhanced AC-3<br>7'b0010110: MAT<br>Others: Reserved |

## 24.5 Interface Description

SPDIF_RX0/SPDIF_RX1 are connected to HDMI TX Controller0/HDMI TX Controller1 respectively, while SPDIF_RX2 is connected to HDMIRX.

Copyright 2022 © Rockchip Electronics Co., Ltd.

## 24.6 Application Notes

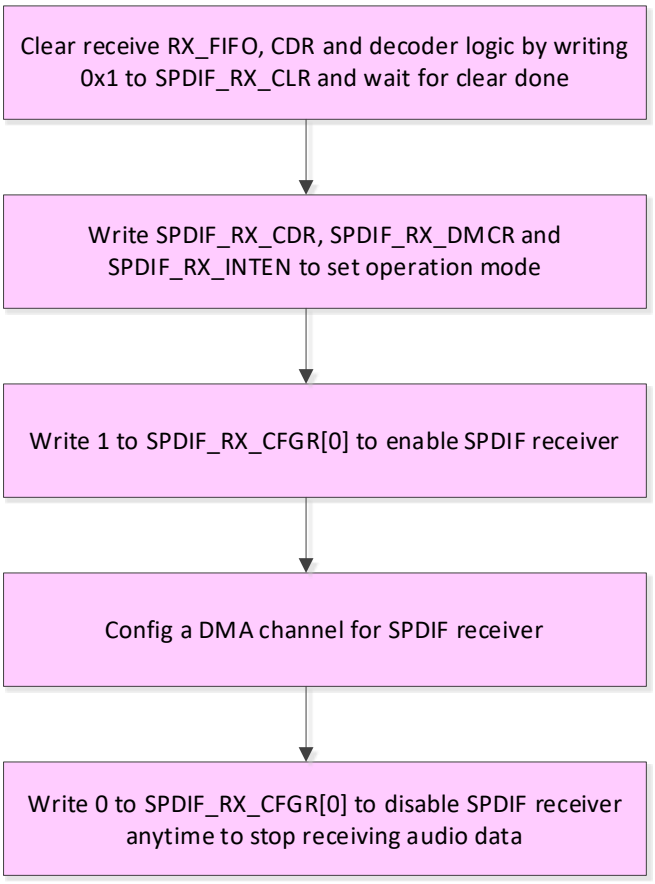



Fig. 24-6 SPDIF receiver operation flow chart

The above figure shows the operation flow of SPDIF receiver operation.

Copyright 2022 © Rockchip Electronics Co., Ltd.

# Chapter 25 Gigabit Media Access Controller (GMAC)

## 25.1 Overview

The Ethernet Quality-of-Service controller(EQOS is commonly referred to as GMAC in this document) provides a complete Ethernet interface from processor to a Reduced Media Independent Interface (RMII) and Reduced Gigabit Media Independent Interface (RGMII) compliant Ethernet PHY. The GMAC includes a DMA controller. The DMA controller efficiently moves packet data from microprocessor's RAM, formats the data for an IEEE 802.3-2002 compliant packet and transmits the data to an Ethernet Physical Interface (PHY). It also efficiently moves packet data from RXFIFO to microprocessor's RAM.
The following features may or may not be present in the actual product. Please contact Rockchip for the actual feature configurations and the third-party licensing requirements.

### 25.1.1 MAC Features

#### 25.1.1.1 MAC Tx and Rx Common Features

- Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces
- Supports 10/100-Mbps data transfer rates with the RMII interfaces
- Half-duplex operation:
  - CSMA/CD Protocol support
  - Flow control using back-pressure support (based on implementation-specific white papers and UNH Ethernet Clause 4 MAC Test Suite - Annex D)
  - Packet bursting and packet extension in 1000 Mbps half-duplex operation
- Standard IEEE 802.3az-2010 for Energy Efficient Ethernet in Reduced Gigabit Media Independent Interface (RGMII) PHYs
- 64-bit data transfer interface on the application side
- Full-duplex flow control operations (IEEE 802.3x Pause packets and Priority flow control)
- network statistics with RMON or MIB Counters (RFC2819/RFC2665)
- Support Ethernet packet timestamping as described in IEEE 1588-2002 and IEEE 1588-2008 (64-bit timestamps given in the Tx or Rx status of PTP packet). Both one-step and two-step timestamping is supported in TX direction
- Flexibility to control the Pulse-Per-Second (PPS) output signal (ptp_pps_o)
- Media clock generation and recovery
- MDIO (Clause 22 and Clause 45) master interface for PHY device configuration and management

#### 25.1.1.2 MAC Tx Features

- Preamble and start of packet data (SFD) insertion
- Separate 32-bit status for each packet transmitted from the application
- Automatic CRC and pad generation controllable on a per-packet basis
- Programmable packet length to support Standard or Jumbo Ethernet packets with up to 16 KB of size
- Programmable Inter Packet Gap (40–96 bit times in steps of 8)
- IEEE 802.3x Flow Control automatic transmission of zero-quanta Pause packet when flow control input transitions from assertion to de-assertion (in full-duplex mode)
- Source Address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted packets with per-packet or static-global control
- Insertion, replacement, or deletion of up to two VLAN tags
- Frame Preemption for MAC Tx

#### 25.1.1.3 MAC Rx Features

- Automatic Pad and CRC Stripping options
- Option to disable Automatic CRC checking
- Preamble and SFD deletion
- Separate 112-bit or 128-bit status
- Programmable watchdog timeout limit
- Flexible address filtering modes:
  - Up to 31 additional 48-bit perfect (DA) address filters with masks for each byte

Copyright 2022 © Rockchip Electronics Co., Ltd.

  - Up to 96 additional 48-bit perfect (DA) address filters that can be selected in blocks of 32 and 64 registers
  - Up to 31 48-bit SA address comparison check with masks for each byte
  - 32 bit, 64 bit, 128 bit, or 256 bit Hash filter (optional) for multicast and unicast (DA) addresses
  - Option to pass all multi-cast addressed packets
  - Promiscuous mode to pass all packets without any filtering for network monitoring
  - Pass all incoming packets (as per filter) with a status report
- Additional packet filtering:
  - VLAN tag-based: Perfect match and Hash-based (optional) filtering. Filtering based on either outer or inner VLAN tag is possible
  - Layer 3 and Layer 4-based: TCP or UDP over IPv4 or IPv6
  - Extended VLAN tag based filtering 4, 8, 16, or 32 filter selection
- IEEE 802.1Q VLAN tag detection and option to delete the VLAN tags in received packets
- Optional module to detect remote wake-up packets and AMD magic packets
- Optional forwarding of received Pause packets to the application (in full-duplex mode)
- Frame Preemption for MAC Rx

## 25.1.2 MTL Features

### 25.1.2.1 MTL Tx and Rx Common Features

- 32-bit, 64-bit, or 128-bit Transaction Layer block (bridges the application and the MAC)
- Data transfers executed using simple FIFO protocol
- Synchronization for all clocks in the design (Transmit, Receive, and Application clocks)
- Optimization for packet-oriented transfers with packets delimiters
- Option to have dual-port RAM based asynchronous FIFO controllers or Single-port RAM based synchronous FIFO controllers
- RAM memory instantiation outside the top-level module to facilitate memory testing or instantiation
- Programmable burst length, up to half the size of the MTL Rx queue or Tx queue size, to support burst data transfer in the EQOS-MTL configuration
- Programmable threshold capability for each queue (default of 64 bytes)
- Optional Debug and slave mode operation on Queue 0 (default queue)

### 25.1.2.2 MTL Tx Features

- TX FIFO sizes on transmission is 16 KB
- Store-and-Forward mechanism or threshold mode (cut-through) for transmission to the MAC
- Programmable queue size in configurations with multiple queues. Each queue size can be programmed in terms of 256 bytes
- Automatic retransmission of collision packets in half-duplex mode
- Discard packets on late collision, excessive collisions, excessive deferral, and under-run conditions with appropriate status
- Disabling of Data Memory RAM chip-select when inactive to reduce power consumption
- Optional module to calculate and insert IPv4 header checksum and TCP, UDP, or ICMP checksum
- Programmable interrupt options for different operational conditions
- Statistics by generating pulses for packets dropped (because of underflow) in the Tx FIFO
- Optional packet-level control for
  - VLAN tag insertion or replacement
  - Ethernet source address insertion
  - Layer3/Layer4 Checksum insertion control
  - One-step timestamp
  - Timestamp control
  - CRC and pad control
- Following scheduling algorithms in configurations with multiple queues:
  - Weighted Round Robin (WRR)
  - (When Data Center Bridging is enabled) Deficit Weighted Round Robin (DWRR)

Copyright 2022 © Rockchip Electronics Co., Ltd.

  - (When Data Center Bridging is enabled) Weighted Fair Queuing (WFQ)
  - Strict Priority (SP)
  - (When Audio-Video Bridging is enabled) Credit-based Shaper (CBS)
  - (When TSN is enabled), Enhancement to Scheduled Traffic (EST)
  - (When TSN is enabled), Time Based Scheduling (TBS)
- Option to support dropping of Tx Status to improve the Transmit throughput

#### 25.1.2.3 MTL Rx Features

- Rx queue sizes in the Receive path is 32 KB
- Insertion of Rx Status vectors into the Rx queue after the EOP transfer (in Threshold mode) and before SOP (in Store-and-Forward mode) in EQOS-MTL configuration
- Programmable Rx queue threshold (default fixed at 64 bytes) in Threshold (or cut-through) mode
- Option to filter all error packets on reception and not forward them to the application in the store-and-forward mode
- Option to forward the undersized good packets
- Statistics by generating pulses for packets dropped (because of overflow) in the Rx FIFO
- Automatic generation of Pause packet control or backpressure signal to the MAC based on the Rx Queue fill level
- Arbitration among queues when multiple queues are present. The following arbitration schemes are supported:
  - Weighted Round Robin (WRR)
  - Weighted Strict priority (WSP)
  - Strict Priority (SP)
- Option to replicate received multicast packets for transfer by multiple Rx DMA channels
- Option to have a programmable lookup table based flexible Parser for filtering and steering the Rx packets

### 25.1.3 DMA Block Features

- 64-bit data transfers
- Separate DMA channel in the Transmit path for each queue in MTL
- Single or multiple DMA channels for any number of queues in MTL Receive path
- Fully synchronous design operating on a single application clock (except for CSR module, when a separate CSR clock is configured)
- Optimization for packet-oriented DMA transfers with packet delimiters
- Byte-aligned addressing for data buffer support
- Dual-buffer (ring) descriptor support
- Descriptor architecture to allow large blocks of data transfer with minimum CPU intervention (each descriptor can transfer up to 32 KB of data)
- Comprehensive status reporting for normal operation and transfers with errors
- Individual programmable burst length for Tx DMA and Rx DMA engines for optimal host bus utilization
- Programmable interrupt options for different operational conditions
- Per-packet Transmit or Receive Complete Interrupt control
- Round-robin or fixed-priority arbitration between the Receive and Transmit engines
- Start and Stop modes
- Separate ports for host CSR access and host data interface
- support for TCP Segmentation Offload (TSO) and UDP Segmentation Offload (USO)
- Selectable number of Tx DMA channels with TSO/USO feature enabled
- Routing of received packets to the DMA channels based on the DA or VLAN Priority in multi-channel DMA configurations
- Option to split the packet header (Layer 3 and Layer 4) and payload in a different buffers
- Time-sensitive conditional packet fetching from system memory by comparing the Slot Time or IEEE 1588 time information provided in the descriptor (useful for AV applications)
- Programmable control for Transmit Descriptor posted writes to improve the throughput
- Sideband signals to control starting and stopping of DMA channels

Copyright 2022 © Rockchip Electronics Co., Ltd. 

## 25.2 Block Diagram

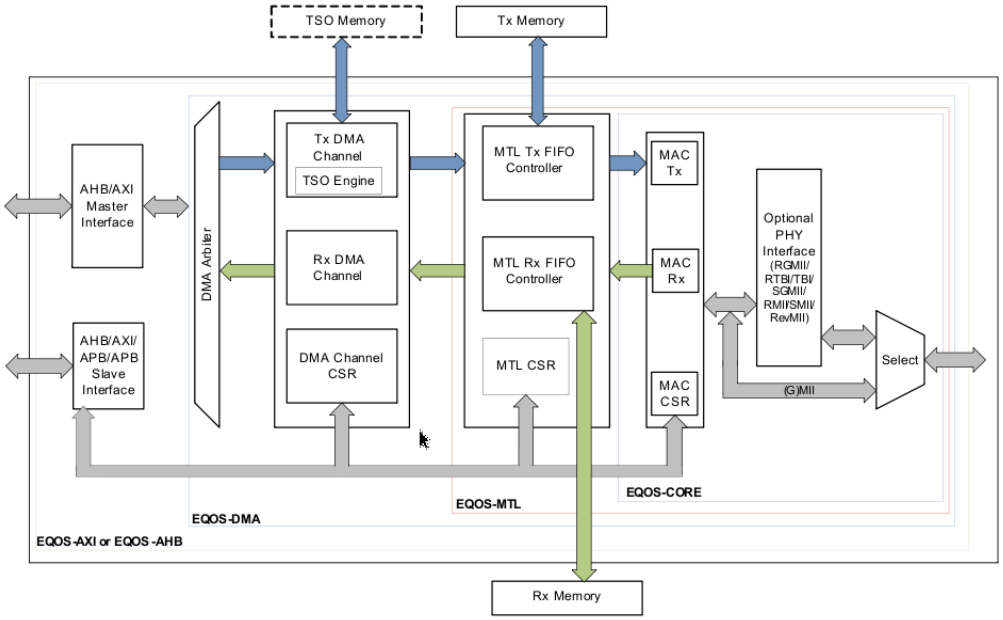



Fig. 25-1 GMAC Block Diagram

The GMAC is broken up into multiple separate functional units. These blocks are interconnected in the MAC module. The block diagram shows the general flow of data and control signals between these blocks.

The GMAC transfers data to system memory through the AXI master interface. The host CPU uses the APB Slave interface to access the GMAC subsystem's control and status registers (CSRs).

The GMAC supports the PHY interfaces of reduced GMII (RGMII) and reduced MII (RMII).

The Transmit FIFO (Tx FIFO) buffers data read from system memory by the DMA before transmission by the GMAC Core. Similarly, the Receive FIFO (Rx FIFO) stores the Ethernet frames received from the line until they are transferred to system memory by the DMA. These are asynchronous FIFOs, as they also transfer the data between the application clock and the GMAC line clocks.

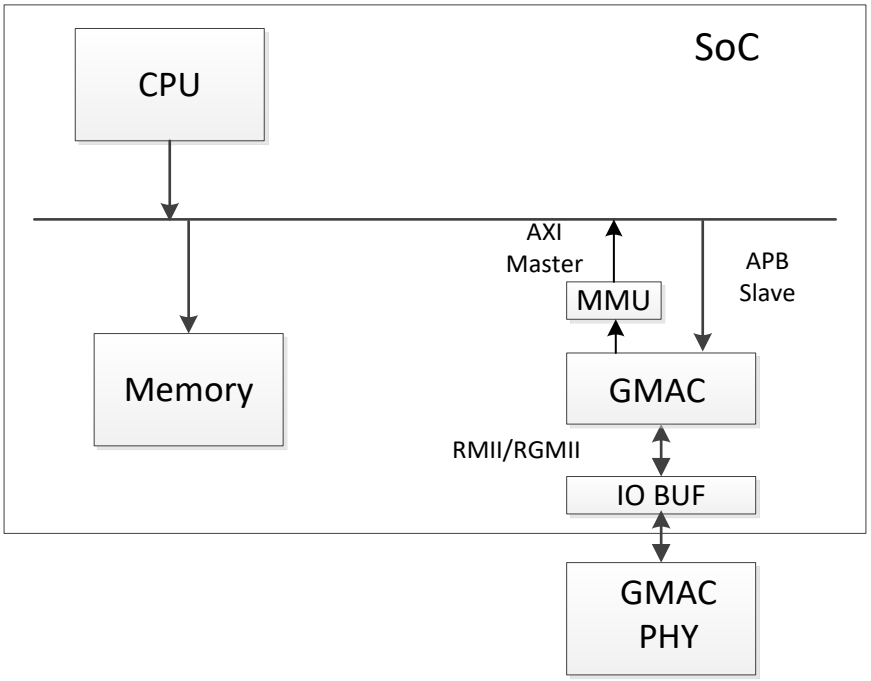



Fig. 25-2 GMAC in SOC

GMAC Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces and Supports 10/100-Mbps data transfer rates with the RMII interfaces.

Copyright 2022 © Rockchip Electronics Co., Ltd.

# 25.3 Function Description

## 25.3.1 Frame Structure

Data frames transmitted shall have the frame format shown in Fig.1-3.

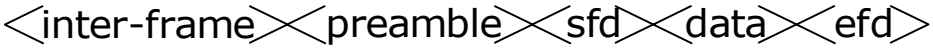



Fig. 25-3 Frame Format

The preamble <preamble> begins a frame transmission. The bit value of the preamble field consists of 7 octets with the following bit values:
10101010 10101010 10101010 10101010 10101010 10101010 10101010
The SFD (start frame delimiter) <sfd> indicates the start of a frame and follows the preamble. The bit value is 10101011.The data in a well formed frame shall consist of N octet's data.

### 25.3.1.1 RMII Interface timing diagram

The Reduced Media Independent Interface (RMII) specification reduces the pin count between Ethernet PHYs and Switch ASICs (only in 10/100 mode). According to the IEEE 802.3u standard, an MII contains 16 pins for data and control. In devices incorporating multiple MAC or PHY interfaces (such as switches), the number of pins adds significant cost with increase in port count. The RMII specification addresses this problem by reducing the pin count to 7 for each port - a 62.5% decrease in pin count.
The RMII module is instantiated between the GMAC and the PHY. This helps translation of the MAC's MII into the RMII. The RMII block has the following characteristics:
Supports 10-Mbps and 100-Mbps operating rates. It does not support 1000-Mbps operation.
Two clock references are sourced externally or CRU, providing independent, 2-bit wide transmit and receive paths.

### 25.3.1.2 Transmit Bit Ordering

Each nibble from the MII must be transmitted on the RMII a di-bit at a time with the order of di-bit transmission shown in Fig.1-4. The lower order bits (D1 and D0) are transmitted first followed by higher order bits (D2 and D3).

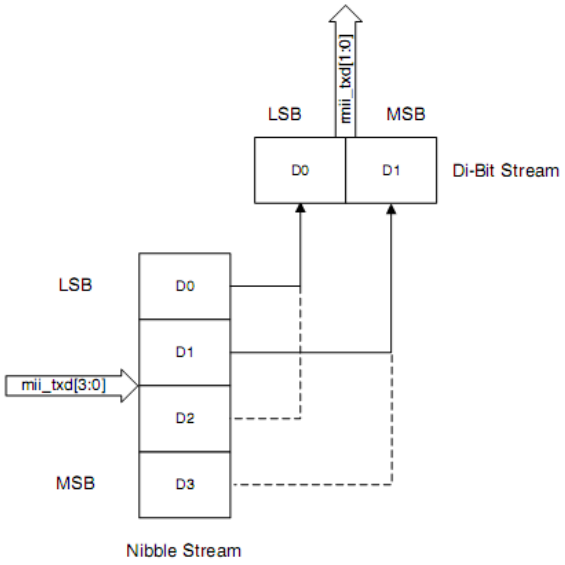



Fig. 25-4 RMII Transmission Bit Ordering

### 25.3.1.3 RMII Transmit Timing Diagrams

Fig.1-5 through 1-8 show MII-to-RMII transaction timing. The clk_rmii_i (REF_CLK) frequency is 50MHz in RMII interface. In 10Mb/s mode, as the REF_CLK frequency is 10 times as the data rate, the value on rmii_txd_o[1:0] (TXD[1:0]) shall be valid such that TXD[1:0] may be sampled every 10th cycle, regard-less of the starting cycle within the group and yield the correct frame data.

Copyright 2022 © Rockchip Electronics Co., Ltd.

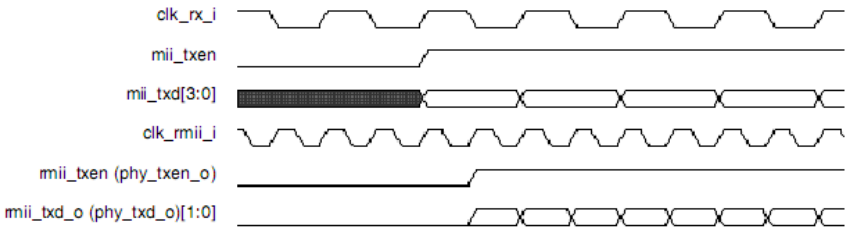



Fig. 25-5 Start of MII and RMII Transmission in 100-Mbps Mode

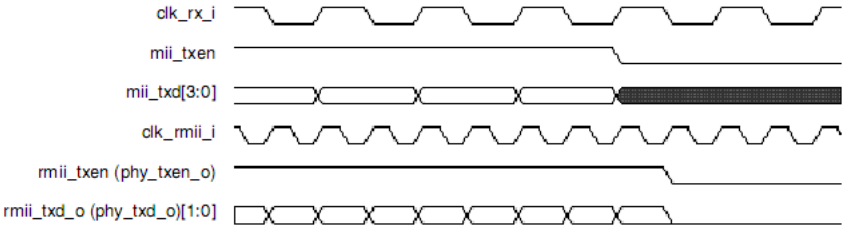



Fig. 25-6 End of MII and RMII Transmission in 100-Mbps Mode

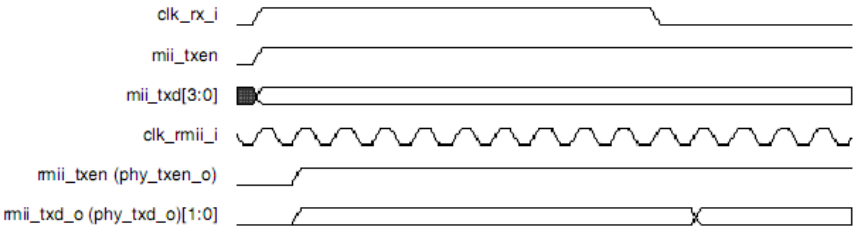



Fig. 25-7 Start of MII and RMII Transmission in 10-Mbps Mode

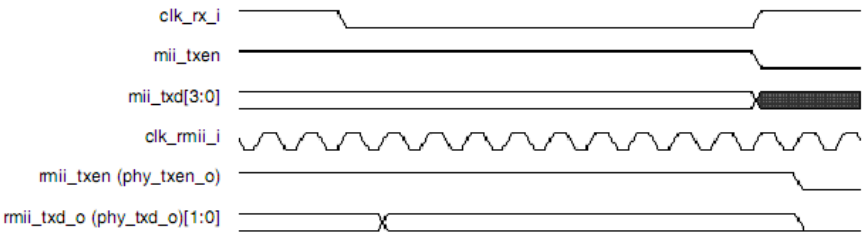



Fig. 25-8 End of MII and RMII Transmission in 10-Mbps Mode

#### 25.3.1.4 Receive Bit Ordering

Each nibble is transmitted to the MII from the di-bit received from the RMII in the nibble transmission order shown in Fig.1-9. The lower order bits (D0 and D1) are received first, followed by the higher order bits (D2 and D3).

Copyright 2022 © Rockchip Electronics Co., Ltd.

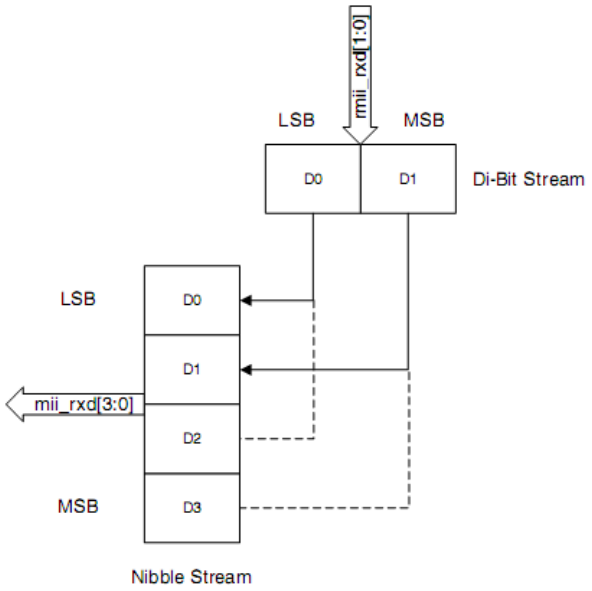



Fig. 25-9 RMII Receive Bit Ordering

#### 25.3.1.5 RGMII Interface

The Reduced Gigabit Media Independent Interface (RGMII) specification reduces the pin count of the interconnection between the GMAC 10/100/1000 controller and the PHY for GMII and MII interfaces. To achieve this, the data path and control signals are reduced and multiplexed together with both the edges of the transmission and receive clocks. For gigabit operation the clocks operate at 125 MHz; for 10/100 operation, the clock rates are 2.5 MHz/25 MHz.

In the GMAC 10/100/1000 controller, the RGMII module is instantiated between the GMAC core's GMII and the PHY to translate the control and data signals between the GMII and RGMII protocols.

The RGMII block has the following characteristics:

- Supports 10-Mbps, 100-Mbps, and 1000-Mbps operation rates
- For the RGMII block, no extra clock is required because both the edges of the incoming clocks are used
- The RGMII block extracts the in-band (link speed, duplex mode and link status) status signals from the PHY and provides them to the GMAC core logic for link detection

### 25.3.2 Station Management Agent

The application can access the PHY registers through the Station Management Agent (SMA) module. SMA is a two-wire Station Management interface (MIM).

For MIM accesses, the maximum operating frequency of the MDC (gmii_mdc_o) is 2.5 MHz, as specified in the IEEE 802.3. In the GMAC core, the gmii_mdc_o clock is derived from the application clock or clk_csr_i, using a divider-counter. The divide factor depends on the clock range setting (CR field) in the MAC_MDIO_Address register Select the clock divide factor as mentioned in the description of CR field of MAC_MDIO_Address register, to meet IEEE specifications. However, if your system supports higher clock frequencies on the MIM interface, there is a provision to select a different divider.

The MDIO frame structure is as follows:

Table 25-1 MDIO Clause 45 Frame Structure

| Field | Description |
|---|---|
| IDLE | The mdio line is in tri-state; there is no clock on gmii_mdc_o signal. |
| PREAMBLE | 32 continuous bits of value 1 |
| START | Start of packet is 2'b00 |
| OPCODE | ■ 2'b00<br>■ 2'b01<br>■ 2'b10 |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Field | Description |
|---|---|
| | ■ 2'b11 |
| PHY ADDR | 5-bit address select for one of 32 PHYs |
| DEV ADDR | 5-bit address select for one of 32 devices |
| TA | Turnaround<br>■ 2'bZ0: Read and post-read increment address<br>■ 2'b10: Write and address MDIO accesses<br>Where Z is the tri-state level |
| DATA/ADDRESS | 16-bit value: For an address cycle (OPCODE = 2'b00), this frame contains the address of the register to be accessed on the next cycle. For the data cycle of a write frame, this field contains the data to be written to the register. For read or post-read increment address frames, this field contains the contents of the register read from the PHY.<br>■ In address and data write cycles, the GMAC drives the MDIO line during the transfer of these 16 bits.<br>■ In read and post-read increment address cycles, the PHY drives the MDIO line during the transfer of these 16 bits. |

The frame structure for Clause 22 frames is also supported. The C45E bit in the MAC_MDIO_Address register can be programmed to enable Clause 22 or Clause 45 mode of operation. Table.1-2 shows the Clause 22 frame format.

Table 25-2 MDIO Clause 22 Frame Structure

| Field | Description |
|---|---|
| IDLE | The mdio line is in tri-state; there is no clock on gmii_mdc_o signal. |
| PREAMBLE | 32 continuous bits of value 1 |
| START | Start of packet is 2'b01 |
| OPCODE | ■ 2'b01 : Write<br>■ 2'b10 : Read |
| PHY ADDR | 5-bit address select for one of 32 PHYs |
| DEV ADDR | 5-bit address to select the register within each MMD |
| TA | Turnaround<br>■ 2'bZ0: Read and post-read increment address<br>■ 2'b10: Write and address MDIO accesses<br>Where Z is the tri-state level |
| DATA/ADDRESS | Any 16-bit value:<br>■ In a write operation, the GMAC drives MDIO<br>■ In read operation, the PHY drives MDIO |

In addition to normal read and write operations, the SMA also supports post-read increment address while operating in Clause 45 mode.

### 25.3.3 Power Management and Energy Efficient Ethernet

The GMAC supports the following techniques to save power.

- Magic Packet
- Remote Wakeup
- Energy Efficient Ethernet

The Magic Packet and Remove Wakeup techniques are used to save power in the host

system when it is idle (Sleep mode) and has to be woken up only at the reception of specific packets from the Ethernet network. In the Sleep mode, the power to the host logic along with majority of the GMAC (except the MAC receiver logic), can be shut down. On receiving the specific packets from the network, the MAC provides the trigger to restore the power to the host system and come back to normal state.
The Energy Efficient Ethernet (EEE) mode is compliant with the IEEE 802.3az-2010 standard. It is primarily targeted to save power in the Ethernet port when there is no traffic on the line. In this mode, the host indicates to the far-end that it does not have any packets to transmit for near future and puts the transmitter port (MAC Controller, PCS and PHY layers) into low-power mode. Similarly, the Receiver port can also be put into low-power mode when the far-end host indicates that it does not have any traffic to transfer. This allows significant saving of power in the Ethernet port (mainly in the PHY) with intermittent and bursty traffic profile. The triggering of entry and exit out of the EEE mode is controlled by the MAC and is supported within the GMAC.
Simultaneous operation of the EEE mode along with any or both the other power saving modes is also supported in GMAC.

### 25.3.4 IEEE 1588 Timestamp Support

The IEEE 1588 defines a Precision Time Protocol (PTP) which enables precise synchronization of time in measurement and control systems. This protocol enables heterogeneous systems that include clocks of varying inherent precision, resolution, and stability to synchronize. The protocol supports system-wide synchronization accuracy in the sub-microsecond range with minimal network and local clock computing resources.
The GMAC supports the IEEE 1588-2002 (version 1) and IEEE 1588-2008 (version 2). The IEEE 1588-2002 supports PTP transported over UDP/IP and IEEE 1588-2008 supports PTP transported over Ethernet. The GMAC provides programmable support for both standards. The controller supports the following features:

- Provides an option to take snapshot of all packets or only PTP type packets
- Provides an option to take snapshot of only event messages
- Provides an option to take the snapshot based on the clock type: ordinary, boundary, end-to-end transparent, and peer-to-peer transparent
- Provides an option to select the node to be a master or slave for ordinary and boundary clock
- Identifies the PTP message type, version, and PTP payload in packets sent directly over Ethernet and sends the status
- Provides an option to measure sub-second time in digital or binary format

### 25.3.5 TCP/IP Segmentation Offload (TSO) Engine

The TCP Segmentation Offload (TSO) engine is useful in offloading the TCP segmentation functions to the hardware.
It also supports UDP Segmentation Offload (USO) in which the UDP payload is segmented in the hardware. There are no sequencing/ordering controls available or updated in the segments, so it can be used in point to point applications in which out of order packets are not expected by the receiver. The description and flow of TSO mentioned in this section is same as USO, any deviation is provided as notes.
In the TCP segmentation offload (TSO) feature, the DMA splits a large TCP packet into multiple small packets and passes these packets to the MTL Tx Queue.

### 25.3.6 MAC Management Counters

The GMAC supports storing the statistics about the received and transmitted packets in registers that are accessible through the application.
The counters in the MAC Management Counters (MMC) module can be viewed as an extension of the register address space of the CSR module. The MMC module maintains a set of registers for gathering statistics on the received and transmitted packets. The register set includes a control register for controlling the behavior of the registers, two status registers containing interrupts generated (receive and transmit), and Interrupt Enable registers (receive and transmit). These registers are accessible from the Application through

Copyright 2022 © Rockchip Electronics Co., Ltd. 

the MAC Control Interface (MCI). Each register is 32-bits wide. The write data is qualified with the corresponding mci_be_i signals. Therefore, non-32-bit accesses are allowed as long as the address is word-aligned. The MMCs are accessed using transactions, in the same way the CSR address space is accessed.
The MMC counters are free running. There is no separate enable for the counters to start. If a particular MMC counter is present in the RTL, it starts counting when corresponding packet is received or transmitted. The Receive MMC counters are updated for packets that are passed by the Address Filter (AFM) block. The statistics of packets, dropped by the AFM module, are not updated unless they are runt packets of less than 6 bytes (DA bytes are not received fully). To get statistics of all packets, set Bit 0 in the “MAC_Packet_Filter” register.
The MMC module gathers statistics on encapsulated IPv4, IPv6, TCP, UDP, or ICMP payloads in received Ethernet packets.

# 25.4 Register Description

## 25.4.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| GMAC_MAC_Configuration | 0x0000 | W | 0x00000000 | The MAC Configuration Register establishes the operating mode of the MAC |
| GMAC_MAC_Ext_Configuration | 0x0004 | W | 0x00000000 | The MAC Extended Configuration Register establishes the operating mode of the MAC |
| GMAC_MAC_Packet_Filter | 0x0008 | W | 0x00000000 | The MAC Packet Filter register contains the filter controls for receiving packets |
| GMAC_MAC_Watchdog_Timeout | 0x000c | W | 0x00000000 | The Watchdog Timeout register controls the watchdog timeout for received packets |
| GMAC_MAC_Hash_Table_Reg0 | 0x0010 | W | 0x00000000 | The Hash Table Register 0 contains the first 32 bits of the hash table |
| GMAC_MAC_Hash_Table_Reg1 | 0x0014 | W | 0x00000000 | The Hash Table Register 1 contains the second 32 bits of the hash table |
| GMAC_MAC_Hash_Table_Reg2 | 0x0018 | W | 0x00000000 | The Hash Table Register 2 contains the third 32 bits of the hash table |
| GMAC_MAC_VLAN_Tag_Ctrl | 0x0050 | W | 0x00000000 | This register is the redefined format of the MAC VLAN Tag Register. It is used for indirect addressing. It contains the address offset, command type and Busy Bit for CSR access of the Per VLAN Tag registers |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| GMAC_MAC_VLAN_Tag_Data | 0x0054 | W | 0x00000000 | This register holds the read/write data for Indirect Access of the Per VLAN Tag registers.During the read access, this field contains valid read data only after the OB bit is reset. During the write access, this field should be valid prior to setting the OB bit in the MAC_VLAN_Tag_Ctrl Register |
| GMAC_MAC_VLAN_Hash_Table | 0x0058 | W | 0x00000000 | When VTHM bit of the MAC_VLAN_Tag register is set, the 16-bit VLAN Hash Table register is used for group address filtering based on the VLAN tag |
| GMAC_MAC_VLAN_Incl | 0x0060 | W | 0x00000000 | The VLAN Tag Inclusion or Replacement register contains the VLAN tag for insertion or replacement in the Transmit packets. It also contains the VLAN tag insertion controls |
| GMAC_MAC_Inner_VLAN_Incl | 0x0064 | W | 0x00000000 | The Inner VLAN Tag Inclusion or Replacement register contains the inner VLAN tag to be inserted or replaced in the Transmit packet. It also contains the inner VLAN tag insertion controls |
| GMAC_MAC_Q0_Tx_Flow_Ctrl | 0x0070 | W | 0x00000000 | The Flow Control register controls the generation and reception of the Control (Pause Command) packets by the Flow control module of the MAC |
| GMAC_MAC_Rx_Flow_Ctrl | 0x0090 | W | 0x00000000 | The Receive Flow Control register controls the pausing of MAC Transmit based on the received Pause packet |
| GMAC_MAC_RxQ_Ctrl4 | 0x0094 | W | 0x00000000 | The Receive Queue Control 4 register controls the routing of unicast and multicast packets that fail the Destination or Source address filter to the Rx queues |
| GMAC_MAC_RxQ_Ctrl0 | 0x00a0 | W | 0x00000000 | The Receive Queue Control 0 register controls the queue management in the MAC Receiver |
| GMAC_MAC_RxQ_Ctrl1 | 0x00a4 | W | 0x00000000 | The Receive Queue Control 1 register controls the routing of multicast, broadcast, AV, DCB, and untagged packets to the Rx queues |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| GMAC_MAC_RxQ_Ctrl2 | 0x00a8 | W | 0x00000000 | This register controls the routing of tagged packets based on the USP (user Priority) field of the received packets to the RxQueues 0 to 3 |
| GMAC_MAC_Interrupt_Status | 0x00b0 | W | 0x00000000 | The Interrupt Status register contains the status of interrupts |
| GMAC_MAC_Interrupt_Enable | 0x00b4 | W | 0x00000000 | The Interrupt Enable register contains the masks for generating the interrupts |
| GMAC_MAC_Rx_Tx_Status | 0x00b8 | W | 0x00000000 | The Receive Transmit Status register contains the Receive and Transmit Error status |
| GMAC_MAC_PMT_Control_Status | 0x00c0 | W | 0x00000000 | The PMT Control and Status Register |
| GMAC_MAC_RWK_Packet_Filter | 0x00c4 | W | 0x00000000 | The Remote Wakeup Filter registers are implemented as 8, 16, or 32 indirect access registers (wkuppktfilter_reg#i) based on whether 4, 8, or 16 Remote Wakeup Filters are selected in the configuration and accessed by application through MAC_RWK_Packet_Filter register |
| GMAC_RWK_Filter0_Byte_Mask | 0x00c4 | W | 0x00000000 | RWK Filter0 Byte Mask |
| GMAC_RWK_Filter1_Byte_Mask | 0x00c4 | W | 0x00000000 | RWK Filter1 Byte Mask |
| GMAC_RWK_Filter2_Byte_Mask | 0x00c4 | W | 0x00000000 | RWK Filter2 Byte Mask |
| GMAC_RWK_Filter3_Byte_Mask | 0x00c4 | W | 0x00000000 | RWK Filter3 Byte Mask |
| GMAC_RWK_Filter01_CRC | 0x00c4 | W | 0x00000000 | RWK Filter 0/1 CRC-16 |
| GMAC_RWK_Filter23_CRC | 0x00c4 | W | 0x00000000 | RWK Filter 2/3 CRC-16 |
| GMAC_RWK_Filter_Offset | 0x00c4 | W | 0x00000000 | RWK Filter Offset |
| GMAC_RWK_Filter_Command | 0x00c4 | W | 0x00000000 | RWK Filter Command |
| GMAC_MAC_LPI_Control_Status | 0x00d0 | W | 0x00000000 | The LPI Control and Status Register controls the LPI functions and provides the LPI interrupt status. The status bits are cleared when this register is read |
| GMAC_MAC_LPI_Timers_Control | 0x00d4 | W | 0x03e80000 | The LPI Timers Control register controls the timeout values in the LPI states. |
| GMAC_MAC_LPI_Entry_Timer | 0x00d8 | W | 0x00000000 | This register controls the Tx LPI entry timer |
| GMAC_MAC_1US_Tic_Counter | 0x00dc | W | 0x0000003f | This register controls the generation of the Reference time (1 microsecond tic) |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| GMAC_MAC_PHYIF_Control_Status | 0x00f8 | W | 0x00000000 | PHY Interface Control and Status Register |
| GMAC_MAC_Version | 0x0110 | W | 0x00003051 | The version register identifies the version of the GMAC |
| GMAC_MAC_Debug | 0x0114 | W | 0x00000000 | The Debug register provides the debug status of various MAC blocks |
| GMAC_MAC_HW_Feature0 | 0x011c | W | 0x181173f3 | This register indicates the presence of first set of the optional features or functions |
| GMAC_MAC_HW_Feature1 | 0x0120 | W | 0x111e01e8 | This register indicates the presence of second set of the optional features or functions |
| GMAC_MAC_HW_Feature2 | 0x0124 | W | 0x11041041 | This register indicates the presence of third set of the optional features or functions |
| GMAC_MAC_HW_Feature3 | 0x0128 | W | 0x0c370031 | This register indicates the presence of fourth set the optional features or functions |
| GMAC_MAC_MDIO_Address | 0x0200 | W | 0x00000000 | The MDIO Address register controls the management cycles to external PHY through a management interface |
| GMAC_MAC_MDIO_Data | 0x0204 | W | 0x00000000 | The MDIO Data register stores the Write data to be written to the PHY register located at the address specified in MAC_MDIO_Address |
| GMAC_MAC_ARP_Address | 0x0210 | W | 0x00000000 | The ARP Address register contains the IPv4 Destination Address of the MAC |
| GMAC_MAC_CSR_SW_Ctrl | 0x0230 | W | 0x00000000 | This register contains SW programmable controls for changing the CSR access response and status bits clearing |
| GMAC_MAC_FPE_CTRL_STS | 0x0234 | W | 0x00000000 | This register controls the operation of Frame Preemption |
| GMAC_MAC_Ext_Cfg1 | 0x0238 | W | 0x00000000 | This register contains Split mode control field and offset field for Split Header feature |
| GMAC_MAC_Presn_Time_ns | 0x0240 | W | 0x00000000 | This register contains the 32-bit binary rollover equivalent time of the PTP System Time in ns |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| GMAC_MAC_Presn_Time_Updt | 0x0244 | W | 0x00000000 | This field holds the 32-bit value of MAC 1722 Presentation Time in ns, that should be added to the Current Presentation Time Counter value. Init happens when TSINIT is set, and update happens when the TSUPDT bit is set (TSINIT and TSINIT defined in MAC_Timestamp_ Control register |
| GMAC_MAC_Address0_High | 0x0300 | W | 0x0000ffff | The MAC Address0 High register holds the upper 16 bits of the first 6-byte MAC address of the station |
| GMAC_MAC_Address0_Low | 0x0304 | W | 0xffffffff | The MAC Address0 Low register holds the lower 32 bits of the 6-byte first MAC address of the station |
| GMAC_MMC_Control | 0x0700 | W | 0x00000000 | This register establishes the operating mode of MMC |
| GMAC_MMC_Rx_Interrupt | 0x0704 | W | 0x00000000 | Maintains the interrupts generated from all Receive statistics counters |
| GMAC_MMC_Tx_Interrupt | 0x0708 | W | 0x00000000 | Maintains the interrupts generated from all Transmit statistics counters |
| GMAC_MMC_Rx_Interrupt_Mask | 0x070c | W | 0x00000000 | This register maintains the masks for interrupts generated from all Receive statistics counters |
| GMAC_MMC_Tx_Interrupt_Mask | 0x0710 | W | 0x00000000 | This register maintains the masks for interrupts generated from all Transmit statistics counters |
| GMAC_Tx_Octet_Count_Good_Bad | 0x0714 | W | 0x00000000 | This register provides the number of bytes transmitted by the GMAC, exclusive of preamble and retried bytes, in good and bad packets |
| GMAC_Tx_Packet_Count_Good_Bad | 0x0718 | W | 0x00000000 | This register provides the number of good and bad packets, exclusive of retried packets |
| GMAC_Tx_Underflow_Error_Packets | 0x0748 | W | 0x00000000 | This register provides the number of packets aborted because of packets underflow error |
| GMAC_Tx_Carrier_Error_Packets | 0x0760 | W | 0x00000000 | This register provides the number of packets aborted because of carrier sense error (no carrier or loss of carrier) |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| GMAC_Tx_Octet_Count_Good | 0x0764 | W | 0x00000000 | This register provides the number of bytes exclusive of preamble, only in good packets |
| GMAC_Tx_Packet_Count_Good | 0x0768 | W | 0x00000000 | This register provides the number of good packets transmitted by GMAC |
| GMAC_Tx_Pause_Packets | 0x0770 | W | 0x00000000 | This register provides the number of good Pause packets transmitted by GMAC |
| GMAC_Rx_Packets_Count_Good_Bad | 0x0780 | W | 0x00000000 | This register provides the number of good and bad packets received by GMAC |
| GMAC_Rx_Octet_Count_Good_Bad | 0x0784 | W | 0x00000000 | This register provides the number of bytes received by GMAC, exclusive of preamble, in good and bad packets |
| GMAC_Rx_Octet_Count_Good | 0x0788 | W | 0x00000000 | This register provides the number of bytes received by GMAC, exclusive of preamble, only in good packets |
| GMAC_Rx_Multicast_Packets_Good | 0x0790 | W | 0x00000000 | This register provides the number of good multicast packets received by GMAC |
| GMAC_Rx_CRC_Error_Packets | 0x0794 | W | 0x00000000 | This register provides the number of packets received by GMAC with CRC error |
| GMAC_Rx_Oversize_Packets_Good | 0x07a8 | W | 0x00000000 | This register provides the number of packets received by GMAC without errors, with length greater than the maxsize (1,518 bytes or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in the S2KP bit of the MAC_Configuration register) |
| GMAC_Rx_Length_Error_Packets | 0x07c8 | W | 0x00000000 | This register provides the number of packets received by GMAC with length error (Length Type field not equal to packet size), for all packets with valid length field |
| GMAC_Rx_Pause_Packets | 0x07d0 | W | 0x00000000 | This register provides the number of good and valid Pause packets received by GMAC |
| GMAC_Rx_FIFO_Overflow_Packets | 0x07d4 | W | 0x00000000 | This register provides the number of missed received packets because of FIFO overflow |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| GMAC_Rx_Watchdog_Error_Packets | 0x07dc | W | 0x00000000 | This register provides the number of packets received by GMAC with error because of watchdog timeout error (packets with a data load larger than 2,048 bytes (when JE and WD bits are reset in MAC_Configuration register), 10,240 bytes (when JE bit is set and WD bit is reset in MAC_Configuration register), 16,384 bytes (when WD bit is set in MAC_Configuration register) or the value programmed in the MAC_Watchdog_Timeout register) |
| GMAC_MMC_IPC_Rx_Interrupt_Mask | 0x0800 | W | 0x00000000 | This register maintains the mask for the interrupt generated from the receive IPC statistic counters |
| GMAC_MMC_IPC_Rx_Interrupt | 0x0808 | W | 0x00000000 | This register maintains the interrupt that the receive IPC statistic counters generate |
| GMAC_RxIPv4_Good_Packets | 0x0810 | W | 0x00000000 | This register provides the number of good IPv4 datagrams received by GMAC with the TCP, UDP, or ICMP payload |
| GMAC_RxIPv4_Header_Error_Packets | 0x0814 | W | 0x00000000 | This register provides the number of IPv4 datagrams received by GMAC with header (checksum, length, or version mismatch) errors |
| GMAC_RxIPv6_Good_Packets | 0x0824 | W | 0x00000000 | This register provides the number of good IPv6 datagrams received by GMAC |
| GMAC_RxIPv6_Header_Error_Packets | 0x0828 | W | 0x00000000 | This register provides the number of IPv6 datagrams received by GMAC with header (length or version mismatch) errors |
| GMAC_RxUDP_Error_Packets | 0x0834 | W | 0x00000000 | This register provides the number of good IP datagrams received by GMAC whose UDP payload has a checksum error |
| GMAC_RxTCP_Error_Packets | 0x083c | W | 0x00000000 | This register provides the number of good IP datagrams received by GMAC whose TCP payload has a checksum error |
| GMAC_RxICMP_Error_Packets | 0x0844 | W | 0x00000000 | This register provides the number of good IP datagrams received by GMAC whose ICMP payload has a checksum error |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| GMAC_RxIPv4_Header_Error_Octets | 0x0854 | W | 0x00000000 | This register provides the number of bytes received by GMAC in IPv4 datagrams with header errors (checksum, length, version mismatch) |
| GMAC_RxIPv6_Header_Error_Octets | 0x0868 | W | 0x00000000 | This register provides the number of bytes received by GMAC in IPv6 datagrams with header errors (length, version mismatch) |
| GMAC_RxUDP_Error_Octets | 0x0874 | W | 0x00000000 | This register provides the number of bytes received by GMAC in a UDP segment that had checksum errors |
| GMAC_RxTCP_Error_Octets | 0x087c | W | 0x00000000 | This register provides the number of bytes received by GMAC in a TCP segment that had checksum errors |
| GMAC_RxICMP_Error_Octets | 0x0884 | W | 0x00000000 | This register provides the number of bytes received by GMAC in a good ICMP segment |
| GMAC_MMC_FPE_Tx_Interrupt | 0x08a0 | W | 0x00000000 | This register maintains the interrupts generated from all FPE related Transmit statistics counters |
| GMAC_MMC_FPE_Tx_Interrupt_Mask | 0x08a4 | W | 0x00000000 | This register maintains the masks for interrupts generated from all FPE related Transmit statistics counters |
| GMAC_MMC_Tx_FPE_Fragment_Cntr | 0x08a8 | W | 0x00000000 | This register provides the number of additional mPackets transmitted due to preemption |
| GMAC_MMC_Tx_Hold_Req_Cntr | 0x08ac | W | 0x00000000 | This register provides the count of number of times a hold request is given to MAC |
| GMAC_MMC_FPE_Rx_Interrupt | 0x08c0 | W | 0x00000000 | This register maintains the interrupts generated from all FPE related Receive statistics counters |
| GMAC_MMC_FPE_Rx_Interrupt_Mask | 0x08c4 | W | 0x00000000 | This register maintains the masks for interrupts generated from all FPE related Receive statistics counters |
| GMAC_MMC_Rx_Packet_Asm_Err_Cntr | 0x08c8 | W | 0x00000000 | This register provides the number of MAC frames with reassembly errors on the Receiver, due to mismatch in the Fragment Count value |
| GMAC_MMC_Rx_Packet_SMD_Err_Cntr | 0x08cc | W | 0x00000000 | This register provides the number of received MAC frames rejected due to unknown SMD value and MAC frame fragments rejected due to arriving with an SMD-C when there was no |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| GMAC_MMC_Rx_Packet_Assembly_OK_Cntr | 0x08d0 | W | 0x00000000 | This register provides the number of MAC frames that were successfully reassembled and delivered to MAC |
| GMAC_MMC_Rx_FPE_Fragment_Cntr | 0x08d4 | W | 0x00000000 | This register provides the number of additional mPackets transmitted due to preemption |
| GMAC_MAC_L3_L4_Control0 | 0x0900 | W | 0x00000000 | The Layer 3 and Layer 4 Control register controls the operations of filter 0 of Layer 3 and Layer 4 |
| GMAC_MAC_Layer4_Address0 | 0x0904 | W | 0x00000000 | The MAC_Layer4_Address0, MAC_L3_L4_Control0, MAC_Layer3_Addr0_Reg0, MAC_Layer3_Addr1_Reg0, MAC_Layer3_Addr2_Reg0 and MAC_Layer3_Ad dr3_Reg0 registers are reserved (RO with default value) if Enable Layer 3 and Layer 4 Packet Filter option is not selected while configuring the core |
| GMAC_MAC_Layer3_Addr0_Reg0 | 0x0910 | W | 0x00000000 | For IPv4 packets, the Layer 3 Address 0 Register 0 register contains the 32-bit IP Source Address field. For IPv6 packets, it contains Bits[31:0] of the 128-bit IP Source Address or Destination Address field |
| GMAC_MAC_Layer3_Addr1_Reg0 | 0x0914 | W | 0x00000000 | For IPv4 packets, the Layer 3 Address 1 Register 0 register contains the 32-bit IP Destination Address field. For IPv6 packets, it contains Bits[63:32] of the 128-bit IP Source Address or Destination Address field |
| GMAC_MAC_Layer3_Addr2_Reg0 | 0x0918 | W | 0x00000000 | The Layer 3 Address 2 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[95:64] of 128-bit IP Source Address or Destination Address field |
| GMAC_MAC_Layer3_Addr3_Reg0 | 0x091c | W | 0x00000000 | The Layer 3 Address 3 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[127:96] of 128-bit IP Source Address or Destination Address field |
| GMAC_MAC_Timestamp_Control | 0x0b00 | W | 0x00000000 | This register controls the operation of the System Time generator and processing of PTP packets for timestamping in the Receiver |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| GMAC_MAC_Sub_Second_Increment | 0x0b04 | W | 0x00000000 | Specifies the value to be added to the internal system time register every cycle of clk_ptp_ref_i clock |
| GMAC_MAC_System_Time_Secs | 0x0b08 | W | 0x00000000 | The System Time Nanoseconds register, along with System Time Seconds register, indicates the current value of the system time maintained by the MAC |
| GMAC_MAC_System_Time_NS | 0x0b0c | W | 0x00000000 | The System Time Nanoseconds register, along with System Time Seconds register, indicates the current value of the system time maintained by the MAC |
| GMAC_MAC_Sys_Time_Secs_Update | 0x0b10 | W | 0x00000000 | The System Time Seconds Update register, along with the System Time Nanoseconds Update register, initializes or updates the system time maintained by the MAC |
| GMAC_MAC_Sys_Time_NS_Update | 0x0b14 | W | 0x00000000 | MAC System Time Nanoseconds Update register |
| GMAC_MAC_Timestamp_Addend | 0x0b18 | W | 0x00000000 | Timestamp Addend register. This register value is used only when the system time is configured for Fine Update mode (TSCFUPDT bit in the MAC_Timestamp_Control register) |
| GMAC_MAC_Timestamp_Status | 0x0b20 | W | 0x00000000 | Timestamp Status register. All bits except Bits[27:25] gets cleared when the application reads this register |
| GMAC_MAC_Tx_TS_Status_NS | 0x0b30 | W | 0x00000000 | This register contains the nanosecond part of timestamp captured for Transmit packets when Tx status is disabled |
| GMAC_MAC_Tx_TS_Status_Secs | 0x0b34 | W | 0x00000000 | The register contains the higher 32 bits of the timestamp (in seconds) captured when a PTP packet is transmitted |
| GMAC_MAC_Auxiliary_Control | 0x0b40 | W | 0x00000000 | The Auxiliary Timestamp Control register controls the Auxiliary Timestamp snapshot |
| GMAC_MAC_Auxiliary_TS_NS | 0x0b48 | W | 0x00000000 | The Auxiliary Timestamp Nanoseconds register, along with MAC_Auxiliary_Timestamp_Seconds, gives the 64-bit timestamp stored as auxiliary snapshot |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| GMAC_MAC_Auxiliary_TS_Secs | 0x0b4c | W | 0x00000000 | The Auxiliary Timestamp - Seconds register contains the lower 32 bits of the Seconds field of the auxiliary timestamp register |
| GMAC_MAC_TS_Ingress_Corr_NS | 0x0b58 | W | 0x00000000 | This register contains the correction value in nanoseconds to be used with the captured timestamp value in the ingress path |
| GMAC_MAC_TS_Egress_Corr_NS | 0x0b5c | W | 0x00000000 | This register contains the correction value in nanoseconds to be used with the captured timestamp value in the egress path |
| GMAC_MAC_TS_Ingress_Latency | 0x0b68 | W | 0x00000000 | This register holds the Ingress MAC latency |
| GMAC_MAC_TS_Egress_Latency | 0x0b6c | W | 0x00000000 | This register holds the Egress MAC latency |
| GMAC_MAC_PPS_Control | 0x0b70 | W | 0x00000000 | PPS Control register |
| GMAC_MAC_PPS0_Target_Time_Seconds | 0x0b80 | W | 0x00000000 | The PPS Target Time Seconds register, along with PPS Target Time Nanoseconds register, is used to schedule an interrupt event [Bit 1 of MAC_Timestamp_Status] when the system time exceeds the value programmed in these registers |
| GMAC_MAC_PPS0_Target_Time_Ns | 0x0b84 | W | 0x00000000 | PPS0 Target Time Nanoseconds register |
| GMAC_MAC_PPS0_Interval | 0x0b88 | W | 0x00000000 | The PPS0 Interval register contains the number of units of sub-second increment value between the rising edges of PPS0 signal output (ptp_pps_o[0]) |
| GMAC_MAC_PPS0_Width | 0x0b8c | W | 0x00000000 | The PPS0 Width register contains the number of units of sub-second increment value |
| GMAC_MTL_Operation_Mode | 0x0c00 | W | 0x00000000 | The Operation Mode register establishes the Transmit and Receive operating modes and commands |
| GMAC_MTL_DBG_CTL | 0x0c08 | W | 0x00000000 | The FIFO Debug Access Control and Status register controls the operation mode of FIFO debug access |
| GMAC_MTL_DBG_STS | 0x0c0c | W | 0x01900000 | The FIFO Debug Status register contains the status of FIFO debug access |
| GMAC_MTL_FIFO_Debug_Data | 0x0c10 | W | 0x00000000 | The FIFO Debug Data register contains the data to be written to or read from the FIFOs |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| GMAC_MTL_Interrupt_Status | 0x0c20 | W | 0x00000000 | The software driver (application) reads this register during interrupt service routine or polling to determine the interrupt status of MTL queues and the MAC |
| GMAC_MTL_RxQ_DMA_Map0 | 0x0c30 | W | 0x00000000 | The Receive Queue and DMA Channel Mapping 0 register is reserved in EQOS-CORE and EQOS-MTL configurations |
| GMAC_MTL_TBS_CTRL | 0x0c40 | W | 0x00000000 | This register controls the operation of Time Based Scheduling |
| GMAC_MTL_EST_Control | 0x0c50 | W | 0x00000000 | This register controls the operation of Enhancements to Scheduled Transmission (IEEE802.1Qbv) |
| GMAC_MTL_EST_Status | 0x0c58 | W | 0x00000000 | This register provides Status related to Enhancements to Scheduled Transmission |
| GMAC_MTL_EST_Sch_Error | 0x0c60 | W | 0x00000000 | This register provides the One Hot encoded Queue Numbers that are having the Scheduling related error (timeout) |
| GMAC_MTL_EST_Frm_Size_Error | 0x0c64 | W | 0x00000000 | This register provides the One Hot encoded Queue Numbers that are having the Frame |
| GMAC_MTL_EST_Frm_Size_Capture | 0x0c68 | W | 0x00000000 | This register captures the Frame Size and Queue Number of the first occurrence of the Frame Size related error. Up on clearing it captures the data of immediate next occurrence of a similar error |
| GMAC_MTL_EST_Intr_Enable | 0x0c70 | W | 0x00000000 | This register implements the Interrupt Enable bits for the various events that generate an interrupt. Bit positions have a 1 to 1 correlation with the status bit positions in MTL_ETS_Status |
| GMAC_MTL_EST_GCL_Control | 0x0c80 | W | 0x00000000 | This register provides the control information for reading/writing to the Gate Control lists |
| GMAC_MTL_EST_GCL_Data | 0x0c84 | W | 0x00000000 | This register holds the read data or write data in case of reads and writes respectively |
| GMAC_MTL_FPE_CTRL_STS | 0x0c90 | W | 0x00000000 | This register controls the operation of, and provides status for Frame Preemption (IEEE802.1Qbu/802.3br) |
| GMAC_MTL_FPE_Advance | 0x0c94 | W | 0x00000000 | This register holds the Hold and Release Advance time |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| GMAC_MTL_TxQ0_Operation_Mode | 0x0d00 | W | 0x00060000 | The Queue 0 Transmit Operation Mode register establishes the Transmit queue operating modes and commands |
| GMAC_MTL_TxQ0_Underflow | 0x0d04 | W | 0x00000000 | The Queue 0 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush |
| GMAC_MTL_TxQ0_Debug | 0x0d08 | W | 0x00000000 | The Queue 0 Transmit Debug register gives the debug status of various blocks related to the Transmit queue |
| GMAC_MTL_TxQ0_ETS_Status | 0x0d14 | W | 0x00000000 | The Queue 0 ETS Status register provides the average traffic transmitted in Queue 0 |
| GMAC_MTL_TxQ0_Quantum_Weight | 0x0d18 | W | 0x00000000 | The Queue 0 Quantum or Weights register contains the quantum value for Deficit Weighted Round Robin (DWRR), weights for the Weighted Round Robin (WRR), and Weighted Fair Queuing (WFQ) for Queue 0 |
| GMAC_MTL_Q0_Interrupt_Ctrl_Status | 0x0d2c | W | 0x00000000 | This register contains the interrupt enable and status bits for the queue 0 interrupts |
| GMAC_MTL_RxQ0_Operation_Mode | 0x0d30 | W | 0x00000000 | The Queue 0 Receive Operation Mode register establishes the Receive queue operating modes and command |
| GMAC_MTL_RxQ0_Miss_Pkt_Ovf_Cnt | 0x0d34 | W | 0x00000000 | The Queue 0 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow |
| GMAC_MTL_RxQ0_Debug | 0x0d38 | W | 0x00000000 | The Queue 0 Receive Debug register gives the debug status of various blocks related to the Receive queue |
| GMAC_MTL_RxQ0_Control | 0x0d3c | W | 0x00000000 | The Queue Receive Control register controls the receive arbitration and passing of received packets to the application |
| GMAC_DMA_Mode | 0x1000 | W | 0x00000000 | The Bus Mode register establishes the bus operating modes for the DMA |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| GMAC_DMA_SysBus_Mode | 0x1004 | W | 0x00010000 | The System Bus mode register controls the behavior of the AHB or AXI master |
| GMAC_DMA_Interrupt_Status | 0x1008 | W | 0x00000000 | The application reads this Interrupt Status register during interrupt service routine or polling to determine the interrupt status of DMA channels, MTL queues, and the MAC |
| GMAC_DMA_Debug_Status0 | 0x100c | W | 0x00000000 | The Debug Status 0 register gives the Receive and Transmit process status for DMA Channel 0-Channel 2 for debugging purpose |
| GMAC_AXI_LPI_Entry_Interval | 0x1040 | W | 0x00000000 | This register is used to control the AXI LPI entry interval |
| GMAC_DMA_TBS_CTRL | 0x1050 | W | 0x00000000 | This register is used to control the TBS attributes |
| GMAC_DMA_CH0_Control | 0x1100 | W | 0x00000000 | The register specifies the MSS value for segmentation, length to skip between two descriptors, and 8xPBL mode |
| GMAC_DMA_CH0_Tx_Control | 0x1104 | W | 0x00000000 | The register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights |
| GMAC_DMA_CH0_Rx_Control | 0x1108 | W | 0x00000000 | The DMA Channel0 Receive Control register controls the Rx features such as PBL, buffer size, and extended status |
| GMAC_DMA_CH0_TxDesc_List_Address | 0x1114 | W | 0x00000000 | The Channel0 Tx Descriptor List Address register points the DMA to the start of Transmit |
| GMAC_DMA_CH0_RxDesc_List_Address | 0x111c | W | 0x00000000 | The Channel0 Rx Descriptor List Address register points the DMA to the start of Receive descriptor list |
| GMAC_DMA_CH0_TxDesc_Tail_Pointer | 0x1120 | W | 0x00000000 | The Channel0 Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor |
| GMAC_DMA_CH0_RxDesc_Tail_Pointer | 0x1128 | W | 0x00000000 | The Channel0 Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor |
| GMAC_DMA_CH0_TxDesc_Ring_Length | 0x112c | W | 0x00000000 | The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| GMAC_DMA_CH0_RxDesc_Ring_Length | 0x1130 | W | 0x00000000 | The Channel0 Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring |
| GMAC_DMA_CH0_Interrupt_Enable | 0x1134 | W | 0x00000000 | The Channel0 Interrupt Enable register enables the interrupts reported by the Status register |
| GMAC_DMA_CH0_Rx_Interrupt_WD_Timer | 0x1138 | W | 0x00000000 | The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA |
| GMAC_DMA_CH0_Slot_Func_Ctrl_Status | 0x113c | W | 0x000007c0 | The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path |
| GMAC_DMA_CH0_Current_App_TxDesc | 0x1144 | W | 0x00000000 | The Channel0 Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA |
| GMAC_DMA_CH0_Current_App_RxDesc | 0x114c | W | 0x00000000 | The Channel0 Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA |
| GMAC_DMA_CH0_Current_App_TxBuffer | 0x1154 | W | 0x00000000 | The Channel0 Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA |
| GMAC_DMA_CH0_Current_App_RxBuffer | 0x115c | W | 0x00000000 | The Channel0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA |
| GMAC_DMA_CH0_Status | 0x1160 | W | 0x00000000 | The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA |
| GMAC_DMA_CH0_Miss_Frame_Cnt | 0x1164 | W | 0x00000000 | This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH0_Rx_Control register |
| GMAC_DMA_CH0_RX_ERI_Cnt | 0x1168 | W | 0x00000000 | The DMA_CH0_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| GMAC_MAC_Address1_High | 0x0308 | W | 0x0000ffff | The MAC Address1 High register holds the upper 16 bits of the first 6-byte MAC address of the station |
| GMAC_MAC_Address1_Low | 0x030c | W | 0xffffffff | The MAC Address0 Low register holds the lower 32 bits of the 6-byte first MAC address of the station |
| GMAC_MAC_Address2_High | 0x0310 | W | 0x0000ffff | The MAC Address2 High register holds the upper 16 bits of the first 6-byte MAC address of the station |
| GMAC_MAC_Address2_Low | 0x0314 | W | 0xffffffff | The MAC Address0 Low register holds the lower 32 bits of the 6-byte first MAC address of the station |
| GMAC_MAC_Address3_High | 0x0318 | W | 0x0000ffff | The MAC Address3 High register holds the upper 16 bits of the first 6-byte MAC address of the station |
| GMAC_MAC_Address3_Low | 0x031c | W | 0xffffffff | The MAC Address0 Low register holds the lower 32 bits of the 6-byte first MAC address of the station |
| GMAC_MAC_L3_L4_Control1 | 0x0930 | W | 0x00000000 | The Layer 3 and Layer 4 Control register controls the operations of filter 0 of Layer 3 and Layer 4 |
| GMAC_MAC_Layer4_Address1 | 0x0934 | W | 0x00000000 | The MAC_Layer4_Address1, MAC_L3_L4_Control1, MAC_Layer3_Addr0_Reg1, MAC_Layer3_Addr1_Reg1, MAC_Layer3_Addr2_Reg1 and MAC_Layer3_Addr3_Reg1 registers are reserved (RO with default value) if Enable Layer 3 and Layer 4 Packet Filter option is not selected while configuring the core |
| GMAC_MAC_Layer3_Addr0_Reg1 | 0x0940 | W | 0x00000000 | For IPv4 packets, the Layer 3 Address 0 Register 1 register contains the 32-bit IP Source Address field. For IPv6 packets, it contains Bits[31:0] of the 128-bit IP Source Address or Destination Address field |
| GMAC_MAC_Layer3_Addr1_Reg1 | 0x0944 | W | 0x00000000 | For IPv4 packets, the Layer 3 Address 1 Register 1 register contains the 32-bit IP Destination Address field. For IPv6 packets, it contains Bits[63:32] of the 128-bit IP Source Address or Destination Address field |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| GMAC_MAC_Layer3_Addr2_Reg1 | 0x0948 | W | 0x00000000 | The Layer 3 Address 2 Register 1 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[95:64] of 128-bit IP Source Address or Destination Address field |
| GMAC_MAC_Layer3_Addr3_Reg1 | 0x094c | W | 0x00000000 | The Layer 3 Address 3 Register 1 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[127:96] of 128-bit IP Source Address or Destination Address field |
| GMAC_MTL_TxQ1_Operation_Mode | 0x0d40 | W | 0x00060000 | The Queue 1 Transmit Operation Mode register establishes the Transmit queue operating modes and commands |
| GMAC_MTL_TxQ1_Underflow | 0x0d44 | W | 0x00000000 | The Queue 1 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush |
| GMAC_MTL_TxQ1_Debug | 0x0d48 | W | 0x00000000 | The Queue 1 Transmit Debug register gives the debug status of various blocks related to the Transmit queue |
| GMAC_MTL_TxQ1_ETS_Control | 0x0d50 | W | 0x00000000 | The Queue ETS Control register controls the enhanced transmission selection operation |
| GMAC_MTL_TxQ1_ETS_Status | 0x0d54 | W | 0x00000000 | The Queue 1 ETS Status register provides the average traffic transmitted in Queue 1 |
| GMAC_MTL_TxQ1_Quantum_Weight | 0x0d58 | W | 0x00000000 | The Queue 1 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 1 |
| GMAC_MTL_TxQ1_SendSlopeCredit | 0x0d5c | W | 0x00000000 | The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue |
| GMAC_MTL_TxQ1_HiCredit | 0x0d60 | W | 0x00000000 | The hiCredit register contains the hiCredit value required for the credit-based shaper |
| GMAC_MTL_TxQ1_LoCredit | 0x0d64 | W | 0x00000000 | The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue |
| GMAC_MTL_Q1_Interrupt_Ctrl_Status | 0x0d6c | W | 0x00000000 | This register contains the interrupt enable and status bits for the queue 1 interrupts |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| GMAC_MTL_RxQ1_Operation_Mode | 0x0d70 | W | 0x00000000 | The Queue 1 Receive Operation Mode register establishes the Receive queue operating modes and command |
| GMAC_MTL_RxQ1_Miss_Pkt_Ovf_Cnt | 0x0d74 | W | 0x00000000 | The Queue 1 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow |
| GMAC_MTL_RxQ1_Debug | 0x0d78 | W | 0x00000000 | The Queue 1 Receive Debug register gives the debug status of various blocks related to the Receive queue |
| GMAC_MTL_RxQ1_Control | 0x0d7c | W | 0x00000000 | The Queue Receive Control register controls the receive arbitration and passing of received packets to the application |
| GMAC_DMA_CH1_Control | 0x1180 | W | 0x00000000 | The register specifies the MSS value for segmentation, length to skip between two descriptors, and 8xPBL mode |
| GMAC_DMA_CH1_Tx_Control | 0x1184 | W | 0x00000000 | The register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights |
| GMAC_DMA_CH1_Rx_Control | 0x1188 | W | 0x00000000 | The DMA Channel1 Receive Control register controls the Rx features such as PBL, buffer size, and extended status |
| GMAC_DMA_CH1_TxDesc_List_Address | 0x1194 | W | 0x00000000 | The Channel1 Tx Descriptor List Address register points the DMA to the start of Transmit |
| GMAC_DMA_CH1_RxDesc_List_Address | 0x119c | W | 0x00000000 | The Channel1 Rx Descriptor List Address register points the DMA to the start of Receive descriptor list |
| GMAC_DMA_CH1_TxDesc_Tail_Pointer | 0x11a0 | W | 0x00000000 | The Channel1 Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor |
| GMAC_DMA_CH1_RxDesc_Tail_Pointer | 0x11a8 | W | 0x00000000 | The Channel1 Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor |
| GMAC_DMA_CH1_TxDesc_Ring_Length | 0x11ac | W | 0x00000000 | The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| GMAC_DMA_CH1_RxDesc_Ring_Length | 0x11b0 | W | 0x00000000 | The Channel1 Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring |
| GMAC_DMA_CH1_Interrupt_Enable | 0x11b4 | W | 0x00000000 | The Channel1 Interrupt Enable register enables the interrupts reported by the Status register |
| GMAC_DMA_CH1_Rx_Interrupt_WD_Timer | 0x11b8 | W | 0x00000000 | The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA |
| GMAC_DMA_CH1_Slot_Func_Ctrl_Status | 0x11bc | W | 0x000007c0 | The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path |
| GMAC_DMA_CH1_Current_App_TxDesc | 0x11c4 | W | 0x00000000 | The Channel1 Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA |
| GMAC_DMA_CH1_Current_App_RxDesc | 0x11cc | W | 0x00000000 | The Channel1 Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA |
| GMAC_DMA_CH1_Current_App_TxBuffer | 0x11d4 | W | 0x00000000 | The Channel1 Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA |
| GMAC_DMA_CH1_Current_App_RxBuffer | 0x11dc | W | 0x00000000 | The Channel1 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA |
| GMAC_DMA_CH1_Status | 0x11e0 | W | 0x00000000 | The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA |
| GMAC_DMA_CH1_Miss_Frame_Cnt | 0x11e4 | W | 0x00000000 | This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH1_Rx_Control register |
| GMAC_DMA_CH1_RX_ERI_Cnt | 0x11e8 | W | 0x00000000 | The DMA_CH1_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

## 25.4.2 Detail Registers Description

**GMAC_MAC_Configuration**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | ARPEN<br>ARP Offload Enable<br>When this bit is set, the MAC can recognize an incoming ARP request packet and schedules the ARP packet for transmission. It forwards the ARP packet to the application and also indicate the events in the RxStatus. When this bit is reset, the MAC receiver does not recognize any ARP packet and indicates them as Type frame in the RxStatus.<br>This bit is available only when the Enable IPv4 ARP Offload is selected.<br>Values:<br>1'b0: ARP Offload is disabled<br>1'b1: ARP Offload is enabled |
| 30:28 | RW | 0x0 | SARC<br>Source Address Insertion or Replacement Control<br>This field controls the source address insertion or replacement for all transmitted packets. Bit 30 specifies which MAC Address register (0 or 1) is used for source address insertion or replacement based on the values of Bits[29:28]:<br>2'b0x:<br>The mti_sa_ctrl_i and ati_sa_ctrl_i input signals control the SA field generation.<br>2'b10:<br>1.If Bit 30 is set to 0, the MAC inserts the content of the MAC Address 0 registers in the SA field of all transmitted packets.<br>2.If Bit 30 is set to 1 and the Enable MAC Address Register 1 option is selected while configuring the core, the MAC inserts the content of the MAC Address 1 registers in the SA field of all transmitted packets.<br>2'b11:<br>1.If Bit 30 is set to 0, the MAC replaces the content of the MAC Address 0 registers in the SA field of all transmitted packets.<br>2.If Bit 30 is set to 1 and the MAC Address Register 1 is enabled, the MAC replaces the content of the MAC Address 1 registers in the SA field of all transmitted packets.<br>Note: Changes to this field take effect only on the start of a packet. If you write to this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value.<br>0x0 (SA_CTRL_IN): mti_sa_ctrl_i and ati_sa_ctrl_i input signals control the SA field generation<br>0x2 (MAC0_INS_SA): Contents of MAC Addr-0 inserted in SA field<br>0x3 (MAC0_REP_SA): Contents of MAC Addr-0 replaces SA field<br>0x6 (MAC1_INS_SA): Contents of MAC Addr-1 inserted in SA field<br>0x7 (MAC1_REP_SA): Contents of MAC Addr-1 replaces SA field |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 27 | RW | 0x0 | IPC<br>Checksum Offload<br>When set, this bit enables the IPv4 header checksum checking and IPv4 or IPv6 TCP, UDP, or ICMP payload checksum checking. When this bit is reset, the COE function in the receiver is disabled.The Layer 3 and Layer 4 Packet Filter and Enable Split Header features automatically selects the IPC Full Checksum Offload Engine on the Receive side. When any of these features are enabled, you must set the IPC bit.<br>Values:<br>1'b0: IP header/payload checksum checking is disabled<br>1'b1: IP header/payload checksum checking is enabled |
| 26:24 | RW | 0x0 | IPG<br>Inter-Packet Gap<br>These bits control the minimum IPG between packets during transmission. This range of minimum IPG is valid in full-duplex mode.In the half-duplex mode, the minimum IPG can be configured only for 64-bit times (IPG = 100). Lower values are not considered. When a JAM pattern is being transmitted because of backpressure activation, the MAC does not consider the minimum IPG.The above function (IPG less than 96 bit times) is valid only when EIPGEN bit in MAC_Ext_Configuration register is reset. When EIPGEN is set, then the minimum IPG (greater than 96 bit times) is controlled as per the description given in EIPG field in MAC_Ext_Configuration register.<br>Values:<br>3'b000: 96 bit times IPG<br>3'b001: 88 bit times IPG<br>3'b010: 80 bit times IPG<br>3'b011: 72 bit times IPG<br>3'b100: 64 bit times IPG<br>3'b101: 56 bit times IPG<br>3'b110: 48 bit times IPG<br>3'b111: 40 bit times IPG |
| 23 | RW | 0x0 | GPSLCE<br>Giant Packet Size Limit Control Enable<br>When this bit is set, the MAC considers the value in GPSL field in MAC_Ext_Configuration register to declare a received packet as Giant packet. This field must be programmed to more than 1,518 bytes. Otherwise, the MAC considers 1,518 bytes as giant packet limit. When this bit is reset, the MAC considers a received packet as Giant packet when its size is greater than 1,518 bytes (1522 bytes for tagged packet).The watchdog timeout limit, Jumbo Packet Enable and 2K Packet Enable have higher precedence over this bit, that is the MAC considers a received packet as Giant packet when its size is greater than 9,018 bytes (9,022 bytes for tagged packet) with Jumbo Packet Enabled and greater than 2,000 bytes with 2K Packet Enabled. The watchdog timeout, if enabled, terminates the received packet when watchdog limit is reached. Therefore, the programmed giant packet limit should be less than the watchdog limit to get the giant packet status.<br>Values:<br>1'b0: Giant Packet Size Limit Control is disabled<br>1'b1: Giant Packet Size Limit Control is enabled |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 22 | RW | 0x0 | S2KP<br>IEEE 802.3as Support for 2K Packets<br>When this bit is set, the MAC considers all packets with up to 2,000 bytes length as normal packets. When the JE bit is not set, the MAC considers all received packets of size more than 2K bytes as Giant packets.When this bit is reset and the JE bit is not set, the MAC considers all received packets of size more than 1,518 bytes (1,522 bytes for tagged) as giant packets.<br>Note: When the JE bit is set, setting this bit has no effect on the giant packet status.<br>Values:<br>1'b0: Support upto 2K packet is disabled<br>1'b1: Support upto 2K packet is Enabled |
| 21 | RW | 0x0 | CST<br>CRC stripping for Type packets<br>When this bit is set, the last four bytes (FCS) of all packets of Ether type (type field greater than 1,536) are stripped and dropped before forwarding the packet to the application.<br>Note: For information about how the settings of the ACS bit and this bit impact the packet length, see the Table, Packet Length based on the CST and ACS Bits.<br>Values:<br>1'b0: CRC stripping for Type packets is disabled<br>1'b1: CRC stripping for Type packets is enabled |
| 20 | RW | 0x0 | ACS<br>Automatic Pad or CRC Stripping<br>When this bit is set, the MAC strips the Pad or FCS field on the incoming packets only if the value of the length field is less than 1,536 bytes. All received packets with length field greater than or equal to 1,536 bytes are passed to the application without stripping the Pad or FCS field.When this bit is reset, the MAC passes all incoming packets to the application, without any modification.<br>Note: For information about how the settings of CST bit and this bit impact the packet length, see the Table, Packet Length based on the CST and ACS Bit.<br>Values:<br>1'b0: Automatic Pad or CRC Stripping is disabled<br>1'b1: Automatic Pad or CRC Stripping is enabled |
| 19 | RW | 0x0 | WD<br>Watchdog Disable<br>When this bit is set, the MAC disables the watchdog timer on the receiver. The MAC can receive packets of up to 16,383 bytes.When this bit is reset, the MAC does not allow more than 2,048 bytes (10,240 if JE is set high) of the packet being received. The MAC cuts off any bytes received after 2,048 bytes.<br>Values:<br>1'b0: Watchdog is enabled<br>1'b1: Watchdog is disabled |
| 18 | RW | 0x0 | BE<br>Packet Burst Enable<br>When this bit is set, the MAC allows packet bursting during transmission in the GMII half-duplex mode.<br>Values:<br>1'b0: Packet Burst is disabled<br>1'b1: Packet Burst is enabled |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17 | RW | 0x0 | JD<br>Jabber Disable<br>When this bit is set, the MAC disables the jabber timer on the transmitter. The MAC can transfer packets of up to 16,383 bytes. When this bit is reset, if the application sends more than 2,048 bytes of data (10,240 if JE is set high) during transmission, the MAC does not send rest of the bytes in that packet.<br>Values:<br>1'b0: Jabber is enabled<br>1'b1: Jabber is disabled |
| 16 | RW | 0x0 | JE<br>Jumbo Packet Enable<br>When this bit is set, the MAC allows jumbo packets of 9,018 bytes (9,022 bytes for VLAN tagged packets) without reporting a giant packet error in the Rx packet status.<br>Values:<br>1'b0: Jumbo packet is disabled<br>1'b1: Jumbo packet is enabled |
| 15 | RW | 0x0 | PS<br>Port Select<br>This bit selects the Ethernet line speed. This bit, along with Bit 14, selects the exact line speed. In the 10/100 Mbps-only (always 1) or 1000 Mbps-only (always 0) configurations, this bit is read-only (RO) with appropriate value. In default 10/100/1000 Mbps configurations, this bit is read-write (R/W). The mac_speed_o[1] signal reflects the value of this bit.<br>Values:<br>1'b0: For 1000 or 2500 Mbps operations<br>1'b1: For 10 or 100 Mbps operations |
| 14 | RW | 0x0 | FES<br>Speed<br>This bit selects the speed mode. The mac_speed_o[0] signal reflects the value of this bit.<br>Values:<br>1'b0: 10 Mbps when PS bit is 1 and 1 Gbps when PS bit is 0<br>1'b1: 100 Mbps when PS bit is 1 and 2.5 Gbps when PS bit is 0 |
| 13 | RW | 0x0 | DM<br>Duplex Mode<br>When this bit is set, the MAC operates in the full-duplex mode in which it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in the full-duplex-only configurations.<br>Values:<br>1'b0: Half-duplex mode<br>1'b1: Full-duplex mode |
| 12 | RW | 0x0 | LM<br>Loopback Mode<br>When this bit is set, the MAC operates in the loopback mode at GMII or MII. The (G)MII Rx clock input (clk_rx_i) is required for the loopback to work properly. This is because the Tx clock is not internally looped back.<br>Values:<br>1'b0: Loopback is disabled<br>1'b1: Loopback is enabled |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11 | RW | 0x0 | ECRSFD<br>Enable Carrier Sense Before Transmission in Full-Duplex Mode<br>When this bit is set, the MAC transmitter checks the CRS signal before packet transmission in the full-duplex mode. The MAC starts the transmission only when the CRS signal is low.When this bit is reset, the MAC transmitter ignores the status of the CRS signal.<br>Values:<br>1'b0: ECRSFD is disabled<br>1'b1: ECRSFD is enabled |
| 10 | RW | 0x0 | DO<br>Disable Receive Own<br>When this bit is set, the MAC disables the reception of packets when the gmii_txen_o is asserted in the half-duplex mode. When this bit is reset, the MAC receives all packets given by the PHY.This bit is not applicable in the full-duplex mode.<br>Values:<br>1'b0: Enable Receive Own<br>1'b1: Disable Receive Own |
| 9 | RW | 0x0 | DCRS<br>Disable Carrier Sense During Transmission<br>When this bit is set, the MAC transmitter ignores the (G)MII CRS signal during packet transmission in the half-duplex mode. As a result, no errors are generated because of Loss of Carrier or No Carrier during transmission.<br>When this bit is reset, the MAC transmitter generates errors because of Carrier Sense. The MAC can even abort the transmission.<br>Values:<br>1'b0: Enable Carrier Sense During Transmission<br>1'b1: Disable Carrier Sense During Transmission |
| 8 | RW | 0x0 | DR<br>Disable Retry<br>When this bit is set, the MAC attempts only one transmission. When a collision occurs on the GMII or MII interface, the MAC ignores the current packet transmission and reports a Packet Abort with excessive collision error in the Tx packet status.When this bit is reset, the MAC retries based on the settings of the BL field. This bit is applicable only in the half-duplex mode.<br>Values:<br>1'b0: Enable Retry<br>1'b1: Disable Retry |
| 7 | RO | 0x0 | reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6:5 | RW | 0x0 | BL<br>Back-Off Limit<br>The back-off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000/2500 Mbps; 512 bit times for 10/100 Mbps) for which the MAC waits before rescheduling a transmission attempt during retries after a collision. n = retransmission attempt.<br>The random integer r takes the value in the range 0 <= r < 2^k<br>This bit is applicable only in the half-duplex mode.<br>Values:<br>2'b00: k = min(n,10)<br>2'b01: k = min(n,8)<br>2'b10: k = min(n,4)<br>2'b11: k = min(n,1) |
| 4 | RW | 0x0 | DC<br>Deferral Check<br>When this bit is set, the deferral check function is enabled in the MAC. The MAC issues a Packet Abort status, along with the excessive deferral error bit set in the Tx packet status, when the Tx state machine is deferred for more than 24,288 bit times in 10 or 100 Mbps mode. If the MAC is configured for 1000/2500 Mbps operation, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but it is prevented<br>because of an active carrier sense signal (CRS) on GMII or MII. The defer time is not cumulative. For example, if the transmitter defers for 10,000 bit times because the CRS signal is active and the CRS signal becomes inactive, the transmitter transmits and collision happens. Because of collision, the transmitter needs to back off and then defer again after back off completion. In such a scenario, the deferral timer is reset to 0, and it is restarted. When this bit is reset, the deferral check function is disabled and the MAC defers until the CRS signal goes inactive. This bit is applicable only in the half-duplex mode.<br>Values:<br>1'b0: Deferral check function is disabled<br>1'b1: Deferral check function is enabled |
| 3:2 | RW | 0x0 | PRELEN<br>Preamble Length for Transmit packets<br>These bits control the number of preamble bytes that are added to the beginning of every Tx packet. The preamble reduction occurs only when the MAC is operating in the full-duplex mode.<br>Values:<br>2'b00: 7 bytes of preamble<br>2'b01: 5 bytes of preamble<br>2'b10: 3 bytes of preamble<br>2'b11: Reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | TE<br>Transmitter Enable<br>When this bit is set, the Tx state machine of the MAC is enabled for transmission on the GMII or MII interface. When this bit is reset, the MAC Tx state machine is disabled after it completes the transmission of the current packet. The Tx state machine does not transmit any more packets.<br>Values:<br>1'b0: Transmitter is disabled<br>1'b1: Transmitter is enabled |
| 0 | RW | 0x0 | RE<br>Receiver Enable<br>When this bit is set, the Rx state machine of the MAC is enabled for receiving packets from the GMII or MII interface. When this bit is reset, the MAC Rx state machine is disabled after it completes the reception of the current packet. The Rx state machine does not receive any more packets from the GMII or MII interface.<br>Values:<br>1'b0: Receiver is disabled<br>1'b1: Receiver is enabled |

**GMAC_MAC_Ext_Configuration**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:25 | RW | 0x00 | EIPG<br>Extended Inter-Packet Gap<br>The value in this field is applicable when the EIPGEN bit is set. This field (as Most Significant bits), along with IPG field in MAC_Configuration register, gives the minimum IPG greater than 96 bit times in steps of 8 bit times: EIPG, IPG<br>8'h00 - 104 bit times<br>8'h01 - 112 bit times<br>8'h02 - 120 bit times<br>----------<br>8'hFF - 2144 bit times |
| 24 | RW | 0x0 | EIPGEN<br>Extended Inter-Packet Gap Enable<br>When this bit is set, the MAC interprets EIPG field and IPG field in MAC_Configuration register together as minimum IPG greater than 96 bit times in steps of 8 bit times. When this bit is reset, the MAC ignores EIPG field and interprets IPG field in MAC_Configuration register as minimum IPG less than or equal to 96 bit times in steps of 8 bit times.<br>Note: The extended Inter-Packet Gap feature must be enabled when operating in Full-Duplex mode only. There may be undesirable effects on back-pressure function and frame transmission if it is enabled in Half-Duplex mode.<br>Values:<br>1'b0: Extended Inter-Packet Gap is disabled<br>1'b1: Extended Inter-Packet Gap is enabled |
| 23 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 22:20 | RW | 0x0 | HDSMS<br>Maximum Size for Splitting the Header Data<br>These bits indicate the maximum header size allowed for splitting the header data in the received packet.<br>Values:<br>0x0 (64BYTES): Maximum Size for Splitting the Header Data is 64 bytes<br>0x1 (128BYTES): Maximum Size for Splitting the Header Data is 128 bytes<br>0x2 (256BYTES): Maximum Size for Splitting the Header Data is 256 bytes<br>0x3 (512BYTES): Maximum Size for Splitting the Header Data is 512 bytes<br>0x4 (1024BYTES): Maximum Size for Splitting the Header Data is 1024 bytes<br>0x5 (Reserved): Reserved |
| 19 | RO | 0x0 | reserved |
| 18 | RW | 0x0 | USP<br>Unicast Slow Protocol Packet Detect<br>When this bit is set, the MAC detects the Slow Protocol packets with unicast address of the station specified in the MAC_Address0_High and MAC_Address0_Low registers. The MAC also detects the Slow Protocol packets with the Slow Protocols multicast address (01-80-C2-00-00-02). When this bit is reset, the MAC detects only Slow Protocol packets with the Slow Protocol multicast address specified in the IEEE 802.3-2015, Section 5.<br>Values:<br>1'b0: Unicast Slow Protocol Packet Detection is disabled<br>1'b1: Unicast Slow Protocol Packet Detection is enabled |
| 17 | RW | 0x0 | SPEN<br>Slow Protocol Detection Enable<br>When this bit is set, MAC processes the Slow Protocol packets (Ether Type 0x8809) and provides the Rx status. The MAC discards the Slow Protocol packets with invalid sub-types. When this bit is reset, the MAC forwards all error-free Slow Protocol packets to the application. The MAC considers such packets as normal Type packets.<br>Values:<br>1'b0: Slow Protocol Detection is disabled<br>1'b1: Slow Protocol Detection is enabled |
| 16 | RW | 0x0 | DCRCC<br>Disable CRC Checking for Received Packets<br>When this bit is set, the MAC receiver does not check the CRC field in the received packets. When this bit is reset, the MAC receiver always checks the CRC field in the received packets.<br>Values:<br>1'b0: CRC Checking is enabled<br>1'b1: CRC Checking is disabled |
| 15:14 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:0 | RW | 0x0000 | GPSL<br>Giant Packet Size Limit<br>If the received packet size is greater than the value programmed in this field in units of bytes, the MAC declares the received packet as Giant packet. The value programmed in this field must be greater than or equal to 1,518 bytes. Any other programmed value is considered as 1,518 bytes. For VLAN tagged packets, the MAC adds 4 bytes to the programmed value. When the Enable Double VLAN Processing option is selected, the MAC adds 8 bytes to the programmed value for double VLAN tagged packets. The value in this field is applicable when the GPSLCE bit is set in MAC_Configuration register. |

**GMAC_MAC_Packet_Filter**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | RA<br>Receive All<br>When this bit is set, the MAC Receiver module passes all received packets to the application, irrespective of whether they pass the address filter or not. The result of the SA or DA filtering is updated (pass or fail) in the corresponding bit in the Rx Status Word.<br>When this bit is reset, the Receiver module passes only those packets to the application that pass the SA or DA address filter.<br>0x0 (DISABLE): Receive All is disabled<br>0x1 (ENABLE): Receive All is enabled |
| 30:22 | RO | 0x000 | reserved |
| 21 | RW | 0x0 | DNTU<br>Drop Non-TCP/UDP over IP Packets<br>When this bit is set, the MAC drops the non-TCP or UDP over IP packets. The MAC forward only those packets that are processed by the Layer 4 filter. When this bit is reset, the MAC forwards all non-TCP or UDP over IP packets.<br>0x0 (FWD): Forward Non-TCP/UDP over IP Packets<br>0x1 (DROP): Drop Non-TCP/UDP over IP Packets |
| 20 | RW | 0x0 | IPFE<br>Layer 3 and Layer 4 Filter Enable<br>When this bit is set, the MAC drops packets that do not match the enabled Layer 3 and Layer 4 filters. If Layer 3 or Layer 4 filters are not enabled for matching, this bit does not have any effect.<br>When this bit is reset, the MAC forwards all packets irrespective of the match status of the Layer 3 and Layer 4 fields.<br>0x0 (DISABLE): Layer 3 and Layer 4 Filters are disabled<br>0x1 (ENABLE): Layer 3 and Layer 4 Filters are enabled |
| 19:17 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 16 | RW | 0x0 | VTFE<br>VLAN Tag Filter Enable<br>When this bit is set, the MAC drops the VLAN tagged packets that do not match the VLAN Tag. When this bit is reset, the MAC forwards all packets irrespective of the match status of the VLAN Tag.<br>Values:<br>1'b0: VLAN Tag Filter is disabled<br>1'b1: VLAN Tag Filter is enabled |
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | HPF<br>Hash or Perfect Filter<br>When this bit is set, the address filter passes a packet if it matches either the perfect filtering or hash filtering as set by the HMC or HUC bit. When this bit is reset and the HUC or HMC bit is set, the packet is passed only if it matches the Hash filter.<br>Values:<br>1'b0: Hash or Perfect Filter is disabled<br>2'b1: Hash or Perfect Filter is enabled |
| 9 | RW | 0x0 | SAF<br>Source Address Filter Enable<br>When this bit is set, the MAC compares the SA field of the received packets with the values programmed in the enabled SA registers. If the comparison fails, the MAC drops the packet.<br>When this bit is reset, the MAC forwards the received packet to the application with updated SAF bit of the Rx Status depending on the SA address comparison.<br>Note: According to the IEEE specification, Bit 47 of the SA is reserved. However, in GMAC, the MAC compares all 48 bits. The software driver should take this into consideration while programming the MAC address registers for SA.<br>0x0 (DISABLE): SA Filtering is disabled<br>0x1 (ENABLE): SA Filtering is enabled |
| 8 | RW | 0x0 | SAIF<br>SA Inverse Filtering<br>When this bit is set, the Address Check block operates in the inverse filtering mode for SA address comparison. If the SA of a packet matches the values programmed in the SA registers, it is marked as failing the SA Address filter.<br>When this bit is reset, if the SA of a packet does not match the values programmed in the SA registers, it is marked as failing the SA Address filter.<br>0x0 (DISABLE): SA Inverse Filtering is disabled<br>0x1 (ENABLE): SA Inverse Filtering is enabled |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:6 | RW | 0x0 | PCF<br>Pass Control Packets<br>These bits control the forwarding of all control packets (including unicast and multicast Pause packets).<br>Values:<br>2'b00: MAC filters all control packets from reaching the application<br>2'b01: MAC forwards all control packets except Pause packets to the application even if they fail the Address filter<br>2'b10: MAC forwards all control packets to the application even if they fail the Address filter<br>2'b11: MAC forwards the control packets that pass the Address filter |
| 5 | RW | 0x0 | DBF<br>Disable Broadcast Packets<br>When this bit is set, the AFM module blocks all incoming broadcast packets. In addition, it overrides all other filter settings. When this bit is reset, the AFM module passes all received broadcast packets.<br>Values:<br>1'b0: Enable Broadcast Packets<br>1'b1: Disable Broadcast Packets |
| 4 | RW | 0x0 | PM<br>Pass All Multicast<br>When this bit is set, it indicates that all received packets with a multicast destination address (first bit in the destination address field is '1') are passed. When this bit is reset, filtering of multicast packet depends on HMC bit.<br>Values:<br>1'b0: Pass All Multicast is disabled<br>1'b1: Pass All Multicast is enabled |
| 3 | RW | 0x0 | DAIF<br>DA Inverse Filtering<br>When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast packets. When this bit is reset, normal filtering of packets is performed.<br>Values:<br>1'b0: DA Inverse Filtering is disabled<br>1'b1: DA Inverse Filtering is enabled |
| 2 | RW | 0x0 | HMC<br>Hash Multicast<br>When this bit is set, the MAC performs the destination address filtering of received multicast packets according to the hash table. When this bit is reset, the MAC performs the perfect destination address filtering for multicast packets, that is, it compares the DA field with the values programmed in DA registers.<br>Values:<br>1'b0: Hash Multicast is disabled<br>1'b1: Hash Multicast is enabled |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | HUC<br>Hash Unicast<br>When this bit is set, the MAC performs the destination address filtering of unicast packets according to the hash table. When this bit is reset, the MAC performs a perfect destination address filtering for unicast packets, that is, it compares the DA field with the values programmed in DA registers.<br>Values:<br>1'b0: Hash Unicast is disabled<br>1'b1: Hash Unicast is enabled |
| 0 | RW | 0x0 | PR<br>Promiscuous Mode<br>When this bit is set, the Address Filtering module passes all incoming packets irrespective of the destination or source address. The SA or DA Filter Fails status bits of the Rx Status Word are always cleared when PR is set.<br>Values:<br>1'b0: Promiscuous Mode is disabled<br>1'b1: Promiscuous Mode is enabled |

**GMAC_MAC_Watchdog_Timeout**

Address: Operational Base + offset (0x000c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:9 | RO | 0x000000 | reserved |
| 8 | RW | 0x0 | PWE<br>Programmable Watchdog Enable<br>Programmable Watchdog Enable<br>When this bit is set and the WD bit of the MAC_Configuration register is reset, the WTO field is used as watchdog timeout for a received packet. When this bit is cleared, the watchdog timeout for a received packet is controlled by setting of WD and JE bits in MAC_Configuration register.<br>Values:<br>1'b0: Programmable Watchdog is disabled<br>1'b1: Programmable Watchdog is enabled |
| 7:4 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RW | 0x0 | WTO<br>Watchdog Timeout<br>When the PWE bit is set and the WD bit of the MAC_Configuration register is reset, this field is used as watchdog timeout for a received packet. If the length of a received packet exceeds the value of this field, such packet is terminated and declared as an error packet.<br>Note: When the PWE bit is set, the value in this field should be more than 1,522 (0x05F2). Otherwise, the IEEE 802.3-specified valid tagged packets are declared as error packets and then dropped.<br>Values:<br>4'b0000: 2 KB<br>4'b0001: 3 KB<br>4'b0010: 4 KB<br>4'b0011: 5 KB<br>4'b0100: 6 KB<br>4'b0101: 7 KB<br>4'b0110: 8 KB<br>4'b0111: 9 KB<br>4'b1000: 10 KB<br>4'b1001: 11 KB<br>4'b1010: 12 KB<br>4'b1011: 13 KB<br>4'b1100: 14 KB<br>4'b1101: 15 KB<br>4'b1110: 16383 Bytes<br>4'b1111: Reserved |

**GMAC_MAC_Hash_Table_Reg0**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | HT31T0<br>MAC Hash Table First 32 Bits<br>This field contains the first 32 Bits [31:0] of the Hash table. The Hash table is used for group address filtering. For hash filtering, the content of the destination address in the incoming packet is passed through the CRC logic and the upper six (seven in 128-bit Hash or eight in 256-bit Hash) bits of the CRC register are used to index the content of the Hash table. The most significant bits determines the register to be used (Hash Table Register X), and the least significant five bits determine the bit within the register. For example, a hash value of 6'b100000 (in 64-bit Hash) selects Bit 0 of the Hash Table Register 1, a value of 7b'1110000 (in 128-bit Hash) selects Bit 16 of the Hash Table Register 3 and a value of 8b'10111111 (in 256-bit Hash) selects Bit 31 of the Hash Table Register 5.<br>The hash value of the destination address is calculated in the following way:<br>1. Calculate the 32-bit CRC for the DA (See IEEE 802.3, Section 3.2.8 for the steps to calculate CRC32).<br>2. Perform bitwise reversal for the value obtained in Step 1.<br>3. Take the upper 6 (or 7 or 8) bits from the value obtained in Step 2. If the corresponding bit value of the register is 1'b1, the packet is accepted. Otherwise, it is rejected. If the PM bit is set in MAC_Packet_Filter, all multicast packets are accepted regardless of the multicast hash values.<br>If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the Hash Table Register X registers are written.If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain. |

**GMAC_MAC_Hash_Table_Reg1**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | HT63T32<br>MAC Hash Table Second 32 Bits<br>This field contains the second 32 Bits [63:32] of the Hash table. |

**GMAC_MAC_Hash_Table_Reg2**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | HT95T64<br>MAC Hash Table Third 32 Bits<br>This field contains the third 32 Bits [95:64] of the Hash table. |

**GMAC_MAC_VLAN_Tag_Ctrl**

Address: Operational Base + offset (0x0050)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | EIVLRXS<br>Enable Inner VLAN Tag in Rx Status<br>When this bit is set, the MAC provides the inner VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the inner VLAN Tag in Rx status.<br>0x0 (DISABLE): Inner VLAN Tag in Rx status is disabled<br>0x1 (ENABLE): Inner VLAN Tag in Rx status is enabled |
| 30 | RO | 0x0 | reserved |
| 29:28 | RW | 0x0 | EIVLS<br>Enable Inner VLAN Tag Stripping on Receive<br>This field indicates the stripping operation on inner VLAN Tag in received packet.<br>0x0 (DONOT): Do not strip<br>0x1 (IFPASS): Strip if VLAN filter passes<br>0x2 (IFFAIL): Strip if VLAN filter fails<br>0x3 (ALWAYS): Always strip |
| 27 | RW | 0x0 | ERIVLT<br>Enable Inner VLAN Tag<br>0x0 (DISABLE): Inner VLAN tag is disabled<br>0x1 (ENABLE): Inner VLAN tag is enabled |
| 26 | RW | 0x0 | EDVLP<br>Enable Double VLAN Processing<br>When this bit is set, the MAC enables processing of up to two VLAN Tags on Tx and Rx (if present). When this bit is reset, the MAC enables processing of up to one VLAN Tag on Tx and Rx (if present).<br>0x0 (DISABLE): Double VLAN Processing is disabled<br>0x1 (ENABLE): Double VLAN Processing is enabled |
| 25 | RW | 0x0 | VTHM<br>VLAN Tag Hash Table Match Enable<br>When this bit is set, the most significant four bits of CRC of VLAN Tag (ones-complement of most significant four bits of CRC of VLAN Tag when ETV bit is reset) are used to index the content of the MAC_VLAN_Hash_Table register. A value of 1 in the VLAN Hash Table register, corresponding to the index, indicates that the packet matched the VLAN hash table.<br>When the ETV bit is set, the CRC of the 12-bit VLAN Identifier (VID) is used for comparison. When the ETV bit is reset, the ones-complement of the CRC of the 16-bit VLAN tag is used for comparison.<br>When this bit is reset, the VLAN Hash Match operation is not performed.<br>0x0 (DISABLE): VLAN Tag Hash Table Match is disabled<br>0x1 (ENABLE): VLAN Tag Hash Table Match is enabled |
| 24 | RW | 0x0 | EVLRXS<br>Enable VLAN Tag in Rx status<br>When this bit is set, MAC provides the outer VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the outer VLAN Tag in Rx status.<br>Values:<br>1'b0: VLAN Tag in Rx status is disabled<br>1'b1: VLAN Tag in Rx status is enabled |
| 23 | RO | 0x0 | reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 22:21 | RW | 0x0 | EVLS<br>Enable VLAN Tag Stripping on Receive<br>This field indicates the stripping operation on the outer VLAN Tag in received packet.<br>Values:<br>2'b00: Do not strip<br>2'b01: Strip if VLAN filter passes<br>2'b10: Strip if VLAN filter fails<br>2'b11: Always strip |
| 20:19 | RO | 0x0 | reserved |
| 18 | RW | 0x0 | ESVL<br>Enable S-VLAN<br>When this bit is set, the MAC transmitter and receiver consider the S-VLAN packets (Type = 0x88A8) as valid VLAN tagged packets.<br>Values:<br>1'b0: S-VLAN is disabled<br>1'b1: S-VLAN is enabled |
| 17 | RW | 0x0 | VTIM<br>VLAN Tag Inverse Match Enable<br>When this bit is set, this bit enables the VLAN Tag inverse matching. The packets without matching VLAN Tag are marked as matched. When reset, this bit enables the VLAN Tag perfect matching. The packets with matched VLAN Tag are marked as matched.<br>Values:<br>1'b0: VLAN Tag Inverse Match is disabled<br>1'b1: VLAN Tag Inverse Match is enabled |
| 16:7 | RO | 0x000 | reserved |
| 6:2 | RW | 0x00 | OFS<br>Offset<br>This field holds the address offset of the MAC VLAN Tag Filter Register which the application is trying to access.The width of the field depends on the number of MAC VLAN Tag Registers enabled. |
| 1 | RW | 0x0 | CT<br>Command Type<br>This bit indicates if the current register access is a read or a write.<br>When set, it indicate a read operation. When reset, it indicates a write operation.<br>0x0 (WRITE): Write operation<br>0x1 (READ): Read operation |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | OB<br>Operation Busy<br>This bit is set along with a read or write command for initiating the indirect access to per VLAN Tag Filter register. This bit is reset when the read or write command to per VLAN Tag Filter indirect access register is complete. The next indirect register access can be initiated only after this bit is reset.<br>During a write operation, the bit is reset only after the data has been written into the Per VLAN Tag register. During a read operation, the data should be read from the MAC_VLAN_Tag_Data register only after this bit is reset.<br>0x0 (DISABLE): Operation Busy is disabled<br>0x1 (ENABLE): Operation Busy is enabled |

**GMAC_MAC_VLAN_Tag_Data**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |
| 25 | RW | 0x0 | DMACHN<br>DMA Channel Number<br>The DMA Channel number to which the VLAN Tagged Frame is to be routed if it passes this VLAN Tag Filter is programmed in this field.<br>If the Routing based on VLAN Tag Filter is not necessary, this field need not be programmed. |
| 24 | RW | 0x0 | DMACHEN<br>DMA Channel Number Enable<br>This bit is the Enable for the DMA Channel Number value programmed in the field DMACH.<br>When this bit is reset, the Routing does not occur based on VLAN Filter result. The frame is routed based on DA Based DMA Channel Routing.<br>0x0 (DISABLE): DMA Channel Number is disabled<br>0x1 (ENABLE): DMA Channel Number is enabled |
| 23:21 | RO | 0x0 | reserved |
| 20 | RW | 0x0 | ERIVLT<br>Enable Inner VLAN Tag Comparison<br>This bit is valid only when VLAN Tag Enable of the Filter is set.<br>When this bit and the EDVLP field are set, the MAC receiver enables operation on the inner VLAN Tag (if present).<br>When this bit is reset, the MAC receiver enables operation on the outer VLAN Tag (if present).<br>0x0 (DISABLE): Inner VLAN tag comparison is disabled<br>0x1 (ENABLE): Inner VLAN tag comparison is enabled |
| 19 | RW | 0x0 | ERSVLM<br>Enable S-VLAN Match for received Frames<br>This bit is valid only when VLAN Tag Enable of the Filter is set.<br>When this bit is set, the MAC receiver enables filtering or matching for S-VLAN (Type = 0x88A8) packets.<br>When this bit is reset, the MAC receiver enables filtering or matching for C-VLAN (Type = 0x8100) packets.<br>0x0 (DISABLE): Receive S-VLAN Match is disabled<br>0x1 (ENABLE): Receive S-VLAN Match is enabled |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 18 | RW | 0x0 | DOVLTC<br>Disable VLAN Type Comparison<br>This bit is valid only when VLAN Tag Enable of the Filter is set.When this bit is set, the MAC does not check whether the VLAN Tag specified by the Enable Inner VLAN Tag Comparison bit is of type S-VLAN or C-VLAN.<br>When this bit is reset, the MAC filters or matches the VLAN Tag specified by the Enable Inner VLAN Tag Comparison bit only when VLAN Tag type is similar to the one specified by the Enable S-VLAN Match for received Frames bit.<br>0x0 (ENABLE): VLAN type comparison is enabled<br>0x1 (DISABLE): VLAN type comparison is disabled |
| 17 | RW | 0x0 | ETV<br>12bits or 16bits VLAN comparison<br>This bit is valid only when VEN of the Filter is set.When this bit is set, a 12-bit VLAN identifier is used for comparing and filtering instead of the complete 16-bit VLAN tag. Bits [11:0] of VLAN tag are compared with the corresponding field in the received VLAN-tagged packet.<br>0x0 (16BIT): 16 bit VLAN comparison<br>0x1 (12BIT): 12 bit VLAN comparison |
| 16 | RW | 0x0 | VEN<br>VLAN Tag Enable<br>This bit is used to enable or disable the VLAN Tag.When this bit is set, the MAC compares the VLAN Tag of received packet with the VLAN Tag ID.<br>When this bit is reset, no comparison is performed irrespective of the programming of the other fields.<br>0x0 (DISABLE): VLAN Tag is disabled<br>0x1 (ENABLE): VLAN Tag is enabled |
| 15:0 | RW | 0x0000 | VID<br>VLAN Tag ID<br>This field holds the VLAN Tag value which is used by the MAC for perfect comparison. It is valid when VLAN Tag Enable is set. |

**GMAC_MAC_VLAN_Hash_Table**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0000 | VLHT<br>VLAN Hash Table<br>This field contains the 16-bit VLAN Hash Table.<br>For hash filtering, the content of the 16-bit VLAN tag or 12-bit VLAN ID (based on the ETV bit of MAC_VLAN_Tag Register) in the incoming packet is passed through the CRC logic. When ETV bit of MAC_VLAN_Tag register is set, the upper four bits of the calculated CRC are used to index the contents of the VLAN Hash table. When ETV bit of MAC_VLAN_Tag register is reset, the ones-complement of upper four bits of the calculated CRC are used to index the contents of the VLAN Hash table. For example, when ETV bit is set a hash value of 4b'1000 selects Bit 8 of the VLAN Hash table, whereas when ETV bit is reset a hash value of 4b'1000 selects Bit 7 of the VLAN Hash table.<br>The hash value of the destination address is calculated in the following way:<br>1.Calculate the 32-bit CRC for the VLAN tag or ID (For steps to calculate CRC32, see Section 3.2.8 of IEEE 802.3).<br>2.Perform bitwise reversal for the value obtained in step 1.<br>3.Take the upper four bits from the value obtained in step 2.<br>If the VLAN hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[15:8] (in little-endian mode) or Bits[7:0] (in big-endian mode) of this register are written.<br>1.If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain. |

**GMAC_MAC_VLAN_Incl**

Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | BUSY<br>Busy<br>This bit indicates the status of the read/write operation of indirect access to the queue/channel specific VLAN inclusion register.<br>For write operation write to a register is complete when this bit is reset. For read operation the read data is valid when the bit is reset.<br>The application must make sure that this bit is reset before attempting subsequent access to this register.<br>Values:<br>0x0 (INACTIVE): Busy status not detected<br>0x1 (ACTIVE): Busy status detected |
| 30 | RW | 0x0 | RDWR<br>Read write control<br>This bit controls the read or write operation for indirectly accessing the queue/channel specific VLAN Inclusion register.<br>When set indicates write operation and when reset indicates read operation.<br>This does not have any effect when CBTI is reset.<br>Values:<br>0x0 (READ): Read operation of indirect access<br>0x1 (WRITE): Write operation of indirect access |
| 29:25 | RO | 0x00 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 24 | RW | 0x0 | ADDR<br>Address<br>This field selects one of the queue/channel specific VLAN Inclusion register for read/write access. This does not have any effect when CBTI is reset. |
| 23:22 | RO | 0x0 | reserved |
| 21 | RW | 0x0 | CBTI<br>Channel based tag insertion<br>When this bit is set, outer VLAN tag is inserted for every packets transmitted by the MAC. The tag value is taken from the queue/channel specific VLAN tag register. The VLTI, VLP, VLC, and VLT fields of this register are ignored when this bit is set. When this bit is set, a write operation to byte 3 of this register initiates the read/write access to the indirect register. When reset, outer VLAN operation is based on the setting of VLTI, VLP, VLC and VLT fields of this register. |
| 20 | RW | 0x0 | VLTI<br>VLAN Tag Input<br>When this bit is set, it indicates that the VLAN tag to be inserted or replaced in Tx packet should be taken from the following:<br>1.The mti_vlan_tag_i signal in EQOS-CORE configurations<br>2.The control word in EQOS-MTL configurations<br>3.The Tx descriptor in EQOS-AHB, EQOS-AXI, or EQOS-DMA configurations<br>Values:<br>0x0 (DISABLE): VLAN Tag Input is disabled<br>0x1 (ENABLE): VLAN Tag Input is enabled |
| 19 | RW | 0x0 | CSVL<br>C-VLAN or S-VLAN<br>When this bit is set, S-VLAN type (0x88A8) is inserted or replaced in the 13th and 14th bytes of transmitted packets. When this bit is reset, C-VLAN type (0x8100) is inserted or replaced in the 13th and 14th bytes of transmitted packets.<br>Values:<br>0x0 (C-VLAN): C-VLAN type (0x8100) is inserted or replaced<br>0x1 (S-VLAN): S-VLAN type (0x88A8) is inserted or replaced |
| 18 | RW | 0x0 | VLP<br>VLAN Priority Control<br>When this bit is set, the control bits[17:16] are used for VLAN deletion, insertion, or replacement. When this bit is reset, the mti_vlan_ctrl_i control input is used and bits[17:16] are ignored.<br>Values:<br>0x0 (DISABLE): VLAN Priority Control is disabled<br>0x1 (ENABLE): VLAN Priority Control is enabled |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17:16 | RW | 0x0 | VLC<br>VLAN Tag Control in Transmit Packets<br>2'b00: No VLAN tag deletion, insertion, or replacement<br>2'b01: VLAN tag deletion<br>The MAC removes the VLAN type (bytes 13 and 14) and VLAN tag (bytes 15 and 16) of all transmitted packets with VLAN tags.<br>2'b10: VLAN tag insertion<br>The MAC inserts VLT in bytes 15 and 16 of the packet after inserting the Type value (0x8100 or 0x88a8) in bytes 13 and 14. This operation is performed on all transmitted packets, irrespective of whether they already have a VLAN tag.<br>2'b11: VLAN tag replacement<br>The MAC replaces VLT in bytes 15 and 16 of all VLAN-type transmitted packets (Bytes 13 and 14 are 0x8100 or 0x88a8).<br>Note: Changes to this field take effect only on the start of a packet. If you write this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value.<br>Values:<br>0x0 (NONE): No VLAN tag deletion, insertion, or replacement<br>0x1 (DELETE): VLAN tag deletion<br>0x2 (INSERT): VLAN tag insertion<br>0x3 (REPLACE): VLAN tag replacement |
| 15:0 | RW | 0x0000 | VLT<br>VLAN Tag for Transmit Packets<br>This field contains the value of the VLAN tag to be inserted or replaced. The value must only be changed when the transmit lines are inactive or during the initialization phase.Bits[15:13] are the User Priority field, Bit 12 is the CFI/DEI field, and Bits[11:0] are the VID field in the VLAN tag.<br>The following list describes the bits of this field:<br>1.Bits[15:13]: User Priority<br>2.Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI)<br>3.Bits[11:0]: VLAN Identifier (VID) field of VLAN tag |

**GMAC_MAC_Inner_VLAN_Incl**

Address: Operational Base + offset (0x0064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x000 | reserved |
| 20 | RW | 0x0 | VLTI<br>VLAN Tag Input<br>When this bit is set, it indicates that the VLAN tag to be inserted or replaced in Tx packet should be taken from the following:<br>1.The mti_vlan_tag_i signal in EQOS-CORE configurations<br>2.The control word in EQOS-MTL configurations<br>3.The Tx descriptor in EQOS-AHB, EQOS-AXI, or EQOS-DMA configurations<br><br>0x0 (DISABLE): VLAN Tag Input is disabled<br>0x1 (ENABLE): VLAN Tag Input is enabled |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19 | RW | 0x0 | CSVL<br>C-VLAN or S-VLAN<br>When this bit is set, S-VLAN type (0x88A8) is inserted or replaced in the 13th and 14th bytes of transmitted packets. When this bit is reset, C-VLAN type (0x8100) is inserted or replaced in the 13th and 14th bytes of transmitted packets.<br>Values:<br>0x0 (C-VLAN): C-VLAN type (0x8100) is inserted<br>0x1 (S-VLAN): S-VLAN type (0x88A8) is inserted |
| 18 | RW | 0x0 | VLP<br>VLAN Priority Control<br>When this bit is set, the VLC field is used for VLAN deletion, insertion, or replacement. When this bit is reset, the mti_vlan_ctrl_i control input is used and the VLC field is ignored.<br>Values:<br>0x0 (DISABLE): VLAN Priority Control is disabled<br>0x1 (ENABLE): VLAN Priority Control is enabled |
| 17:16 | RW | 0x0 | VLC<br>VLAN Tag Control in Transmit Packets<br>2'b00: No VLAN tag deletion, insertion, or replacement<br>2'b01: VLAN tag deletion<br>The MAC removes the VLAN type (bytes 17 and 18) and VLAN tag (bytes 19 and 20) of all transmitted packets with VLAN tags.<br>2'b10: VLAN tag insertion<br>The MAC inserts VLT in bytes 19 and 20 of the packet after inserting the Type value (0x8100 or 0x88a8) in bytes 17 and 18. This operation is performed on all transmitted packets, irrespective of whether they already have a VLAN tag.<br>2'b11: VLAN tag replacement<br>The MAC replaces VLT in bytes 19 and 20 of all VLAN-type transmitted packets (Bytes 17 and 18 are 0x8100 or 0x88a8).<br>Note: Changes to this field take effect only on the start of a packet. If you write this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value.<br>Values:<br>0x0 (NONE): No VLAN tag deletion, insertion, or replacement<br>0x1 (DELETE): VLAN tag deletion<br>0x2 (INSERT): VLAN tag insertion<br>0x3 (REPLACE): VLAN tag replacement |
| 15:0 | RW | 0x0000 | VLT<br>VLAN Tag for Transmit Packets<br>This field contains the value of the VLAN tag to be inserted or replaced. The value must only be changed when the transmit lines are inactive or during the initialization phase. Bits[15:13] are the User Priority field, Bit 12 is the CFI/DEI field, and Bits[11:0] are the VID field in the VLAN tag.<br>The following list describes the bits of this field:<br>1.Bits[15:13]: User Priority<br>2.Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI)<br>3.Bits[11:0]: VLAN Identifier (VID) field of VLAN tag |

**GMAC_MAC_Q0_Tx_Flow_Ctrl**

Address: Operational Base + offset (0x0070)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | PT<br>Pause Time<br>This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain. |
| 15:8 | RO | 0x00 | reserved |
| 7 | RW | 0x0 | DZPQ<br>Disable Zero-Quanta Pause<br>When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i).<br>When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled.<br>Values:<br>1'b0: Zero-Quanta Pause packet generation is enabled<br>1'b1: Zero-Quanta Pause packet generation is disabled |
| 6:4 | RW | 0x0 | PLT<br>Pause Low Threshold<br>This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted.<br>The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times.<br>Values:<br>3'b000: Pause Time minus 4 Slot Times (PT -4 slot times)<br>3'b001: Pause Time minus 28 Slot Times (PT -28 slot times)<br>3'b010: Pause Time minus 36 Slot Times (PT -36 slot times)<br>3'b011: Pause Time minus 144 Slot Times (PT -144 slot times)<br>3'b100: Pause Time minus 256 Slot Times (PT -256 slot times)<br>3'b101: Pause Time minus 512 Slot Times (PT -512 slot times)<br>3'b110: Reserved |
| 3:2 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | TFE<br>Transmit Flow Control Enable<br>Full-Duplex Mode:<br>In the full-duplex mode, when this bit is set, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets.<br>Half-Duplex Mode:<br>In the half-duplex mode, when this bit is set, the MAC enables the backpressure operation. When this bit is reset, the backpressure feature is disabled.<br>Values:<br>1'b0: Transmit Flow Control is disabled<br>1'b1: Transmit Flow Control is enabled |
| 0 | RW | 0x0 | FCB_BPA<br>Flow Control Busy or Backpressure Activate<br>This bit initiates a Pause packet in the full-duplex mode and activates the backpressure function in the half-duplex mode if the TFE bit is set.<br>Full-Duplex Mode:<br>In the full-duplex mode, this bit should be read as 1'b0 before writing to this register. To initiate a Pause packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When Pause packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared.<br>Half-Duplex Mode:<br>When this bit is set (and TFE bit is set) in the half-duplex mode, the MAC asserts the backpressure. During backpressure, when the MAC receives a new packet, the transmitter starts sending a JAM pattern resulting in a collision. This control register bit is logically ORed with the mti_flowctrl_i input signal for the backpressure function. When the MAC is configured for the full-duplex mode, the BPA is automatically disabled. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.<br>Values:<br>1'b0: Flow Control Busy or Backpressure Activate is disabled<br>1'b1: Flow Control Busy or Backpressure Activate is enabled |

**GMAC_MAC_Rx_Flow_Ctrl**

Address: Operational Base + offset (0x0090)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | UP<br>Unicast Pause Packet Detect<br>A pause packet is processed when it has the unique multicast address specified in the IEEE 802.3. When this bit is set, the MAC can also detect Pause packets with unicast address of the station. This unicast address should be as specified in MAC_Address0_High and MAC_Address0_Low. When this bit is reset, the MAC only detects Pause packets with unique multicast address.<br>Note: The MAC does not process a Pause packet if the multicast address is different from the unique multicast address. This is also applicable to the received PFC packet when the Priority Flow Control (PFC) is enabled. The unique multicast address (0x01_80_C2_00_00_01) is as specified in IEEE 802.1 Qbb-2011.<br>Values:<br>1'b0: Unicast Pause Packet Detect disabled<br>1'b1: Unicast Pause Packet Detect enabled |
| 0 | RW | 0x0 | RFE<br>Receive Flow Control Enable<br>When this bit is set and the MAC is operating in full-duplex mode, the MAC decodes the received Pause packet and disables its transmitter for a specified (Pause) time. When this bit is reset or the MAC is operating in half-duplex mode, the decode function of the Pause packet is disabled. When PFC is enabled, flow control is enabled for PFC packets. The MAC decodes the received PFC packet and disables the Transmit queue, with matching priorities, for a duration of received Pause time.<br>Values:<br>1'b0: Receive Flow Control is disabled<br>1'b1: Receive Flow Control is enabled |

**GMAC_MAC_RxQ_Ctrl4**

Address: Operational Base + offset (0x0094)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17 | RW | 0x0 | VFFQ<br>VLAN Tag Filter Fail Packets Queue<br>This field holds the Rx queue number to which the tagged packets failing the Destination or Source Address filter (and UFFQE/MFFQE not enabled) or failing the VLAN tag filter must be routed to. This field is valid only when the VFFQE bit is set. |
| 16 | RW | 0x0 | VFFQE<br>VLAN Tag Filter Fail Packets Queuing Enable<br>When this bit is set, the tagged packets which fail the Destination or Source address filter or fail the VLAN tag filter, are routed to the Rx Queue Number programmed in the VFFQ. When this bit is reset, the tagged packets which fail the Destination or Source address filter or fail the VLAN tag filter are routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set.<br>0x0 (DISABLE): VLAN tag Filter Fail Packets Queuing is disabled<br>0x1 (ENABLE): VLAN tag Filter Fail Packets Queuing is enabled |
| 15:10 | RO | 0x00 | reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RW | 0x0 | MFFQ<br>Multicast Address Filter Fail Packets Queue<br>This field holds the Rx queue number to which the Multicast packets failing the Destination or Source Address filter are routed to. This field is valid only when the MFFQE bit is set. |
| 8 | RW | 0x0 | MFFQE<br>Multicast Address Filter Fail Packets Queuing Enable<br>When this bit is set, the Multicast packets which fail the Destination or Source address filter is routed to the Rx Queue Number programmed in the MFFQ. When this bit is reset, the Multicast packets which fail the Destination or Source address filter is routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set.<br>0x0 (DISABLE): Multicast Address Filter Fail Packets Queuing is disabled<br>0x1 (ENABLE): Multicast Address Filter Fail Packets Queuing is enabled |
| 7:2 | RO | 0x00 | reserved |
| 1 | RW | 0x0 | UFFQ<br>Unicast Address Filter Fail Packets Queue<br>This field holds the Rx queue number to which the Unicast packets failing the Destination or Source Address filter are routed to. This field is valid only when the UFFQE bit is set. |
| 0 | RW | 0x0 | UFFQE<br>Unicast Address Filter Fail Packets Queuing Enable<br>When this bit is set, the Unicast packets which fail the Destination or Source address filter is routed to the Rx Queue Number programmed in the UFFQ. When this bit is reset, the Unicast packets which fail the Destination or Source address filter is routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set.<br>Values:<br>0x0 (DISABLE): Unicast Address Filter Fail Packets Queuing is disabled<br>0x1 (ENABLE): Unicast Address Filter Fail Packets Queuing is enabled |

**GMAC_MAC_RxQ_Ctrl0**

Address: Operational Base + offset (0x00a0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3:2 | RW | 0x0 | RXQ1EN<br>Receive Queue 1 Enable<br>This field is similar to the RXQ0EN field.<br>Values:<br>0x0 (DISABLE): Queue not enabled<br>0x1 (EN_AV): Queue enabled for AV<br>0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic<br>0x3 (Reserved): Reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1:0 | RW | 0x0 | RXQ0EN<br>Receive Queue 0 Enable<br>This field indicates whether Rx Queue 0 is enabled for AV or DCB.<br>Values:<br>0x0 (DISABLE): Queue not enabled<br>0x1 (EN_AV): Queue enabled for AV<br>0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic<br>0x3 (Reserved): Reserved<br>Note: In multiple Rx queues configuration, all the queues are disabled by default. Enable the Rx queue by programming the corresponding field in this register. |

**GMAC_MAC_RxQ_Ctrl1**

Address: Operational Base + offset (0x00a4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:27 | RO | 0x00 | reserved |
| 26:24 | RW | 0x0 | FPRQ<br>Frame Preemption Residue Queue<br>This field holds the Rx queue number to which the residual preemption frames must be forwarded. Preemption frames that are tagged and pass the SA/DA/VLAN filtering are routed based on PSRQ and all other frames are treated as residual frames and is routed to the queue number mentioned in this field. The Queue-0 is used as a default queue for express frames, so this field cannot be programmed to a value 0. |
| 23:22 | RW | 0x0 | TPQC<br>Tagged PTP over Ethernet Packets Queuing Control<br>This field controls the routing of the VLAN Tagged PTPoE packets.<br>If GMAC_AV_ENABLE is selected in the configuration, the following programmable options are allowed.<br>2'b00: VLAN Tagged PTPoE packets are routed as generic VLAN Tagged packet (based on PSRQ for only non-AV enabled Rx Queues).<br>2'b01: VLAN Tagged PTPoE packets are routed to Rx Queue specified by PTPQ field (That Rx Queue can be enabled for AV or non-AV traffic).<br>2'b10: VLAN Tagged PTPoE packets are routed to only AV enabled Rx Queues based on PSRQ.<br>2'b11: Reserved<br>If GMAC_AV_ENABLE is not selected in the configuration, the following programmable options are allowed.<br>1'b0: VLAN Tagged PTPoE packets are routed as generic VLAN Tagged packet (based on PSRQ for DCB/Generic enabled Rx Queues).<br>1'b1: VLAN Tagged PTPoE packets are routed to Rx Queues specified by PTPQ field. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 21 | RW | 0x0 | TACPQE<br>Tagged AV Control Packets Queuing Enable<br>When set, the MAC routes the received Tagged AV Control packets to the Rx queue specified by AVCPQ field. When reset, the MAC routes the received Tagged AV Control packets based on the tag priority matching the PSRQ fields in MAC_RxQ_Ctrl2 and MAC_RxQ_Ctrl3 registers.<br>Values:<br>0x0 (DISABLE): Tagged AV Control Packets Queuing is disabled<br>0x1 (ENABLE): Tagged AV Control Packets Queuing is enabled |
| 20 | RW | 0x0 | MCBCQEN<br>Multicast and Broadcast Queue Enable<br>This bit specifies that Multicast or Broadcast packets routing to the Rx Queue is enabled and the Multicast or Broadcast packets must be routed to Rx Queue specified in MCBCQ field.<br>Values:<br>0x0 (DISABLE): Multicast and Broadcast Queue is disabled<br>0x1 (ENABLE): Multicast and Broadcast Queue is enabled |
| 19 | RO | 0x0 | reserved |
| 18:16 | RW | 0x0 | MCBCQ<br>Multicast and Broadcast Queue<br>This field specifies the Rx Queue onto which Multicast or Broadcast Packets are routed. Any Rx Queue enabled for Generic/DCB/AV traffic can be used to route the Multicast or Broadcast Packets.<br>Values:<br>0x0 (QUEUE0): Receive Queue 0<br>0x1 (QUEUE1): Receive Queue 1<br>0x2 (QUEUE2): Receive Queue 2<br>0x3 (QUEUE3): Receive Queue 3<br>0x4 (QUEUE4): Receive Queue 4<br>0x5 (QUEUE5): Receive Queue 5<br>0x6 (QUEUE6): Receive Queue 6<br>0x7 (QUEUE7): Receive Queue 7 |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x0 | UPQ<br>Untagged Packet Queue<br>This field indicates the Rx Queue to which Untagged Packets are to be routed. Any Rx Queue enabled for Generic/DCB/AV traffic can be used to route the Untagged Packets.<br>Values:<br>0x0 (QUEUE0): Receive Queue 0<br>0x1 (QUEUE1): Receive Queue 1<br>0x2 (QUEUE2): Receive Queue 2<br>0x3 (QUEUE3): Receive Queue 3<br>0x4 (QUEUE4): Receive Queue 4<br>0x5 (QUEUE5): Receive Queue 5<br>0x6 (QUEUE6): Receive Queue 6<br>0x7 (QUEUE7): Receive Queue 7 |
| 11:7 | RO | 0x00 | reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6:4 | RW | 0x0 | PTPQ<br>PTP Packets Queue<br>This field specifies the Rx queue on which the PTP packets sent over the Ethernet payload (not over IPv4 or IPv6) are routed. When the AV8021ASMEN bit of MAC_Timestamp_Control register is set, only untagged PTP over Ethernet packets are routed on an Rx Queue. If the bit is not set, then based on programming of TPQC field, both tagged and untagged PTPoE packets can be routed to this Rx Queue.<br>Values:<br>0x0 (QUEUE0): Receive Queue 0<br>0x1 (QUEUE1): Receive Queue 1<br>0x2 (QUEUE2): Receive Queue 2<br>0x3 (QUEUE3): Receive Queue 3<br>0x4 (QUEUE4): Receive Queue 4<br>0x5 (QUEUE5): Receive Queue 5<br>0x6 (QUEUE6): Receive Queue 6<br>0x7 (QUEUE7): Receive Queue 7 |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x0 | AVCPQ<br>AV Untagged Control Packets Queue<br>This field specifies the Receive queue on which the received AV tagged and untagged control packets are routed. The AV tagged (when TACPQE bit is set) and untagged control packets are routed to Receive queue specified by this field.<br>Values:<br>0x0 (QUEUE0): Receive Queue 0<br>0x1 (QUEUE1): Receive Queue 1<br>0x2 (QUEUE2): Receive Queue 2<br>0x3 (QUEUE3): Receive Queue 3<br>0x4 (QUEUE4): Receive Queue 4<br>0x5 (QUEUE5): Receive Queue 5<br>0x6 (QUEUE6): Receive Queue 6<br>0x7 (QUEUE7): Receive Queue 7 |

**GMAC_MAC_RxQ_Ctrl2**

Address: Operational Base + offset (0x00a8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:8 | RW | 0x00 | PSRQ1<br>Priorities Selected in the Receive Queue 1<br>This field decides the priorities assigned to Rx Queue 1. All packets with priorities that match the values set in this field are routed to Rx Queue 1. For example, if PSRQ1[4] is set, packets with USP field equal to 4 are routed to Rx Queue 1. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. When the DCB feature is selected, this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 1 crosses the flow control threshold settings. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:0 | RW | 0x00 | PSRQ0<br>Priorities Selected in the Receive Queue 0<br>This field decides the priorities assigned to Rx Queue 0. All packets with priorities that match the values set in this field are routed to Rx Queue 0. For example, if PSRQ0[5] is set, packets with USP field equal to 5 are routed to Rx Queue 0. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. When the DCB feature is selected, this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 0 crosses the flow control threshold settings. |

**GMAC_MAC_Interrupt_Status**

Address: Operational Base + offset (0x00b0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x000 | reserved |
| 20 | RO | 0x0 | MFRIS<br>MMC FPE Receive Interrupt Status<br>This bit is set high when an interrupt is generated in the MMC FPE Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option along with FPE support.<br>Values:<br>0x0 (INACTIVE): MMC FPE Receive Interrupt status not active<br>0x1 (ACTIVE): MMC FPE Receive Interrupt status active |
| 19 | RO | 0x0 | MFTIS<br>MMC FPE Transmit Interrupt Status<br>This bit is set high when an interrupt is generated in the MMC FPE Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option along with FPE support.<br>Values:<br>0x0 (INACTIVE): MMC FPE Transmit Interrupt status not active<br>0x1 (ACTIVE): MMC FPE Transmit Interrupt status active |
| 18 | RO | 0x0 | MDIOIS<br>MDIO Interrupt Status<br>This bit indicates an interrupt event after the completion of MDIO operation. To reset this bit, the application has to read this bit/Write 1 to this bit when RCWE bit of MAC_CSR_SW_Ctrl register is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.<br>Values:<br>1'b0: MDIO Interrupt status not active<br>1'b1: MDIO Interrupt status active |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17 | RO | 0x0 | FPEIS<br>Frame Preemption Interrupt Status<br>This bit indicates an interrupt event during the operation of Frame Preemption (Bits[19:16] of MAC_FPE_CTRL_STS register is set). To reset this bit, the application must clear the event in MAC_FPE_CTRL_STS that has caused the Interrupt.<br>Values:<br>0x0 (INACTIVE): Frame Preemption Interrupt status not active<br>0x1 (ACTIVE): Frame Preemption Interrupt status active |
| 16:15 | RO | 0x0 | reserved |
| 14 | RO | 0x0 | RXSTSIS<br>Receive Status Interrupt<br>This bit indicates the status of received packets. This bit is set when the RWT bit is set in the MAC_Rx_Tx_Status register. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register.<br>Values:<br>1'b0: Receive Interrupt status not active<br>1'b1: Receive Interrupt status active |
| 13 | RO | 0x0 | TXSTSIS<br>Transmit Status Interrupt<br>This bit indicates the status of transmitted packets. This bit is set when any of the following bits is set in the MAC_Rx_Tx_Status register:<br>1. Excessive Collision (EXCOL)<br>2. Late Collision (LCOL)<br>3. Excessive Deferral (EXDEF)<br>4. Loss of Carrier (LCARR)<br>5. No Carrier (NCARR)<br>6. Jabber Timeout (TJT)<br>This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register.<br>Values:<br>1'b0: Transmit Interrupt status not active<br>1'b1: Transmit Interrupt status active |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RO | 0x0 | TSIS<br>Timestamp Interrupt Status<br>If the Timestamp feature is enabled, this bit is set when any of the following conditions is true:<br>1. The system time value is equal to or exceeds the value specified in the Target Time High and Low registers.<br>2. There is an overflow in the Seconds register.<br>3. The Target Time Error occurred, that is, programmed target time already elapsed.<br>If the Auxiliary Snapshot feature is enabled, this bit is set when the auxiliary snapshot trigger is asserted. In configurations other than EQOS_CORE, when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers. When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Timestamp_Status register.<br>Values:<br>1'b0: Timestamp Interrupt status not active<br>1'b1: Timestamp Interrupt status active |
| 11 | RO | 0x0 | MMCRXIPIS<br>MMC Receive Checksum Offload Interrupt Status<br>This bit is set high when an interrupt is generated in the MMC Receive Checksum Offload Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) and Enable Receive TCP/IP Checksum Check options.<br>Values:<br>1'b0: MMC Receive Checksum Offload Interrupt status not active<br>1'b1: MMC Receive Checksum Offload Interrupt status active |
| 10 | RO | 0x0 | MMCTXIS<br>MMC Transmit Interrupt Status<br>This bit is set high when an interrupt is generated in the MMC Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option.<br>Values:<br>1'b0: MMC Transmit Interrupt status not active<br>1'b1: MMC Transmit Interrupt status active |
| 9 | RO | 0x0 | MMCRXIS<br>MMC Receive Interrupt Status<br>This bit is set high when an interrupt is generated in the MMC Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option.<br>Values:<br>1'b0: MMC Receive Interrupt status not active<br>1'b1: MMC Receive Interrupt status active |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RO | 0x0 | MMCIS<br>MMC Interrupt Status<br>This bit is set high when Bit 11, Bit 10, or Bit 9 is set high. This bit is cleared only when all these bits are low. This bit is valid only when you select the Enable MAC Management Counters (MMC) option.<br>Values:<br>1'b0: MMC Interrupt status not active<br>1'b1: MMC Interrupt status active |
| 7:6 | RO | 0x0 | reserved |
| 5 | RO | 0x0 | LPIIS<br>LPI Interrupt Status<br>When the Energy Efficient Ethernet feature is enabled, this bit is set for any LPI state entry or exit in the MAC Transmitter or Receiver. This bit is cleared when the corresponding interrupt source bit of MAC_LPI_Control_Status register is read (or corresponding interrupt source bit of MAC_LPI_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set).<br>Values:<br>1'b0: LPI Interrupt status not active<br>1'b1: LPI Interrupt status active |
| 4 | RO | 0x0 | PMTIS<br>PMT Interrupt Status<br>This bit is set when a Magic packet or Wake-on-LAN packet is received in the power-down mode (RWKPRCVD and MGKPRCVD bits in MAC_PMT_Control_Status register). This bit is cleared when corresponding interrupt source bit are cleared because of a Read operation to the MAC_PMT_Control_Status register (or corresponding interrupt source bit of MAC_PMT_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set).<br>This bit is valid only when you select the Enable Power Management option.<br>Values:<br>1'b0: PMT Interrupt status not active<br>1'b1: PMT Interrupt status active |
| 3 | RO | 0x0 | PHYIS<br>PHY Interrupt<br>This bit is set when rising edge is detected on the phy_intr_i input. This bit is cleared when this register is read (or this bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set).<br>Values:<br>1'b0: PHY Interrupt not detected<br>1'b1: PHY Interrupt detected |
| 2:1 | RO | 0x0 | reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RO | 0x0 | RGSMIIIS<br>RGMII or SMII Interrupt Status<br>This bit is set because of any change in value of the Link Status of RGMII or SMII interface (LNKSTS bit in MAC_PHYIF_Control_Status register). This bit is cleared when the MAC_PHYIF_Control_Status register is read (or LNKSTS bit of MAC_PHYIF_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the optional RGMII or SMII PHY interface.<br>Values:<br>1'b0: RGMII or SMII Interrupt Status is not active<br>1'b1: RGMII or SMII Interrupt Status is active |

**GMAC_MAC_Interrupt_Enable**

Address: Operational Base + offset (0x00b4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:19 | RO | 0x0000 | reserved |
| 18 | RW | 0x0 | MDIOIE<br>MDIO Interrupt Enable<br>When this bit is set, it enables the assertion of the interrupt when MDIOIS field is set in the MAC_Interrupt_Status register.<br>Values:<br>1'b0: MDIO Interrupt is disabled<br>1'b1: MDIO Interrupt is enabled |
| 17 | RW | 0x0 | FPEIE<br>Frame Preemption Interrupt Enable<br>When this bit is set, it enables the assertion of the interrupt when FPEIS field is set in the MAC_Interrupt_Status register.<br>Values:<br>0x0 (DISABLE): Frame Preemption Interrupt is disabled<br>0x1 (ENABLE): Frame Preemption Interrupt is enabled |
| 16:15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | RXSTSIE<br>Receive Status Interrupt Enable<br>When this bit is set, it enables the assertion of the interrupt signal because of the setting of RXSTSIS bit in the MAC_Interrupt_Status register.<br>Values:<br>1'b0: Receive Status Interrupt is disabled<br>1'b1: Receive Status Interrupt is enabled |
| 13 | RW | 0x0 | TXSTSIE<br>Transmit Status Interrupt Enable<br>When this bit is set, it enables the assertion of the interrupt signal because of the setting of TXSTSIS bit in the MAC_Interrupt_Status register.<br>Values:<br>1'b0: Timestamp Status Interrupt is disabled<br>1'b1: Timestamp Status Interrupt is enabled |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | TSIE<br>Timestamp Interrupt Enable<br>When this bit is set, it enables the assertion of the interrupt signal because of the setting of TSIS bit in MAC_Interrupt_Status register.<br>Values:<br>1'b0: Timestamp Interrupt is disabled<br>1'b1: Timestamp Interrupt is enabled |
| 11:6 | RO | 0x00 | reserved |
| 5 | RW | 0x0 | LPIIE<br>LPI Interrupt Enable<br>When this bit is set, it enables the assertion of the interrupt signal because of the setting of LPIIS bit in MAC_Interrupt_Status register.<br>Values:<br>1'b0: LPI Interrupt is disabled<br>1'b1: LPI Interrupt is enabled |
| 4 | RW | 0x0 | PMTIE<br>PMT Interrupt Enable<br>When this bit is set, it enables the assertion of the interrupt signal because of the setting of PMTIS bit in MAC_Interrupt_Status register.<br>Values:<br>1'b0: PMT Interrupt is disabled<br>1'b1: PMT Interrupt is enabled |
| 3 | RW | 0x0 | PHYIE<br>PHY Interrupt Enable<br>When this bit is set, it enables the assertion of the interrupt signal because of the setting of PHYIS bit in MAC_Interrupt_Status register.<br>Values:<br>1'b0: PHY Interrupt is disabled<br>1'b1: PHY Interrupt is enabled |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | RGSMIIIE<br>RGMII or SMII Interrupt Enable<br>When this bit is set, it enables the assertion of the interrupt signal because of the setting of RGSMIIIS bit in MAC_Interrupt_Status register.<br>Values:<br>1'b0: RGMII or SMII Interrupt is disabled<br>1'b1: RGMII or SMII Interrupt is enabled |

**GMAC_MAC_Rx_Tx_Status**

Address: Operational Base + offset (0x00b8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:9 | RO | 0x000000 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RO | 0x0 | RWT<br>Receive Watchdog Timeout<br>This bit is set when a packet with length greater than 2,048 bytes is received (10, 240 bytes when Jumbo Packet mode is enabled) and the WD bit is reset in the MAC_Configuration register. This bit is set when a packet with length greater than 16,383 bytes is received and the WD bit is set in the MAC_Configuration register.<br>Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.<br>Values:<br>1'b0: No receive watchdog timeout<br>1'b1: Receive watchdog timed out |
| 7:6 | RO | 0x0 | reserved |
| 5 | RO | 0x0 | EXCOL<br>Excessive Collisions<br>When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the transmission aborted after 16 successive collisions while attempting to transmit the current packet. If the DR bit is set in the MAC_Configuration register, this bit is set after the first collision and the packet transmission is aborted.<br>Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.<br>Values:<br>1'b0: No collision<br>1'b1: Excessive collision is sensed |
| 4 | RO | 0x0 | LCOL<br>Late Collision<br>When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the packet transmission aborted because a collision occurred after the collision window (64 bytes including Preamble in MII mode; 512 bytes including Preamble and Carrier Extension in GMII mode). This bit is not valid if the Underflow error occurs.<br>Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.<br>Values:<br>1'b0: No collision<br>1'b1: Late collision is sensed |
| 3 | RO | 0x0 | EXDEF<br>Excessive Deferral<br>When the DTXSTS bit is set in the MTL_Operation_Mode register and the DC bit is set in the MAC_Configuration register, this bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 in 1000/2500 Mbps mode or when Jumbo packet is enabled).<br>Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.<br>Values:<br>1'b0: No Excessive deferral<br>1'b1: Excessive deferral |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RO | 0x0 | LCARR<br>Loss of Carrier<br>When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the loss of carrier occurred during packet transmission, that is, the phy_crs_i signal was inactive for one or more transmission clock periods during packet transmission. This bit is valid only for packets transmitted without collision.<br>Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.<br>Values:<br>1'b0: Carrier is present<br>1'b1: Loss of carrier |
| 1 | RO | 0x0 | NCARR<br>No Carrier<br>When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the carrier signal from the PHY is not present at the end of preamble transmission.<br>Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.<br>Values:<br>1'b0: Carrier is present<br>1'b1: No carrier |
| 0 | RO | 0x0 | TJT<br>Transmit Jabber Timeout<br>This bit indicates that the Transmit Jabber Timer expired which happens when the packet size exceeds 2,048 bytes (10,240 bytes when the Jumbo packet is enabled) and JD bit is reset in the MAC_Configuration register. This bit is set when the packet size exceeds 16,383 bytes and the JD bit is set in the MAC_Configuration register.<br>Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.<br>Values:<br>1'b0: No Transmit Jabber Timeout<br>1'b1: Transmit Jabber Timeout occurr |

**GMAC_MAC_PMT_Control_Status**

Address: Operational Base + offset (0x00c0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | RWKFILTRST<br>Remote Wake-Up Packet Filter Register Pointer Reset<br>When this bit is set, the remote wake-up packet filter register pointer is reset to 3'b000. It is automatically cleared after 1 clock cycle.<br>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.<br>Values:<br>1'b0: Remote Wake-Up Packet Filter Register Pointer is not Reset<br>1'b1: Remote Wake-Up Packet Filter Register Pointer is Reset |
| 30:29 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 28:24 | RO | 0x00 | RWKPTR<br>Remote Wake-up FIFO Pointer<br>This field gives the current value (0 to 7, 15, or 31 when 4, 8, or 16 Remote Wake-up Packet Filters are selected) of the Remote Wake-up Packet Filter register pointer. When the value of this pointer is equal to maximum for the selected number of Remote Wake-up Packet Filters, the contents of the Remote Wake-up Packet Filter Register are transferred to the clk_rx_i domain when a Write occurs to that register. |
| 23:11 | RO | 0x0000 | reserved |
| 10 | RW | 0x0 | RWKPFE<br>Remote Wake-up Packet Forwarding Enable<br>When this bit is set along with RWKPKTEN, the MAC receiver drops all received frames until it receives the expected Wake-up frame. All frames after that event including the received wake-up frame are forwarded to application. This bit is then self-cleared on receiving the wake-up packet. The application can also clear this bit before the expected wake-up frame is received. In such cases, the MAC reverts to the default behavior where packets received are forwarded to the application. This bit must only be set when RWKPKTEN is set high and PWRDWN is set low. The setting of this bit has no effect when PWRDWN is set high.<br>Note: If Magic Packet Enable and Wake-Up Frame Enable are both set along with setting of this bit and Magic Packet is received prior to wake-up frame, this bit is self-cleared on receiving Magic Packet, the received Magic packet is dropped, and all frames after received Magic Packet are forwarded to application.<br>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.<br>Values:<br>1'b0: Remote Wake-up Packet Forwarding is disabled<br>1'b1: Remote Wake-up Packet Forwarding is enabled |
| 9 | RW | 0x0 | GLBLUCAST<br>Global Unicast<br>When this bit set, any unicast packet filtered by the MAC (DAF) address recognition is detected as a remote wake-up packet.<br>Values:<br>1'b0: Global unicast is disabled<br>1'b1: Global unicast is enabled |
| 8:7 | RO | 0x0 | reserved |
| 6 | RO | 0x0 | RWKPRCVD<br>Remote Wake-Up Packet Received<br>When this bit is set, it indicates that the power management event is generated because of the reception of a remote wake-up packet. This bit is cleared when this register is read.<br>Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.<br>Values:<br>1'b0: Remote wake-up packet is received<br>1'b1: Remote wake-up packet is received |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RO | 0x0 | MGKPRCVD<br>Magic Packet Received<br>When this bit is set, it indicates that the power management event is generated because of the reception of a magic packet. This bit is cleared when this register is read.<br>Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.<br>Values:<br>1'b0: No Magic packet is received<br>1'b1: Magic packet is received |
| 4:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | RWKPKTEN<br>Remote Wake-Up Packet Enable<br>When this bit is set, a power management event is generated when the MAC receives a remote wake-up packet.<br>Values:<br>1'b0: Remote wake-up packet is disabled<br>1'b1: Remote wake-up packet is enabled |
| 1 | RW | 0x0 | MGKPKTEN<br>Magic Packet Enable<br>When this bit is set, a power management event is generated when the MAC receives a magic packet.<br>Values:<br>1'b0: Magic Packet is disabled<br>1'b1: Magic Packet is enabled |
| 0 | RW | 0x0 | PWRDWN<br>Power Down<br>When this bit is set, the MAC receiver drops all received packets until it receives the expected magic packet or remote wake-up packet. This bit is then self-cleared and the power-down mode is disabled. The software can clear this bit before the expected magic packet or remote wake-up packet is received. The packets received by the MAC after this bit is cleared are forwarded to the application. This bit must only be set when the Magic Packet Enable, Global Unicast, or Remote Wake-Up Packet Enable bit is set high.<br>Note: You can gate-off the CSR clock during the power-down mode. However, when the CSR clock is gated-off, you cannot perform any read or write operations on this register. Therefore, the Software cannot clear this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.<br>Values:<br>1'b0: Power down is disabled<br>1'b1: Power down is enabled |

**GMAC_MAC_RWK_Packet_Filter**

Address: Operational Base + offset (0x00c4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | WKUPFRMFTR(cont.)<br>(4) If filters chained by And_Previous bit setting have complementary programming, then a frame may never pass the AND chained filter. For example, if Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set), Filter 1 Address_Type bit is set (bit 3 in Filter 1 command is set) indicating multicast detection and Filter 2 Address_Type bit is reset (bit 3 in Filter 2 command is reset) indicating unicast detection or vice versa, a remote wakeup frame does not pass the AND chained filter as a remote wakeup frame cannot be of both unicast and multicast address type.<br>4. Bit 0 is the enable for filter i. If Bit 0 is not set, filter i is disabled.<br>Filter i Byte Mask: The filter i byte mask register defines the bytes of the packet that are examined by filter i (0, 1, 2, 3, .., 15) to determine whether or not a packet is a wake-up packet.<br>1. The MSB (31st bit) must be zero.<br>2. Bit j[30:0] is the byte mask.<br>3. If Bit j (byte number) of the byte mask is set, the CRC block processes the Filter i Offset + j of the incoming packet; otherwise Filter i Offset + j is ignored.<br>Filter i Offset: The filter i offset register defines the offset (within the packet) from which the filter i examines the packets.<br>1. This 8-bit pattern-offset is the offset for the filter i first byte to be examined.<br>2. The minimum allowed offset is 12, which refers to the 13th byte of the packet.<br>3. The offset value 0 refers to the first byte of the packet.<br>Filter i CRC-16: The filter i CRC-16 register contains the CRC-16 value calculated from the pattern and the byte mask programmed in the Remote Wakeup filter register.<br>1. The 16-bit CRC calculation uses the following polynomial: G(x) = x^16 + x^15 + x^2 + 1<br>2. Each mask, used in the hash function calculation, is compared with a 16-bit value associated with that mask. Each filter has the following:<br>(1)32-bit Mask: Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1, the corresponding byte is taken into the CRC16 calculation.<br>(2) 8-bit Offset Pointer: Specifies the byte to start the CRC-16 computation. The pointer and the mask are used together to locate the bytes to be used in the CRC-16 calculations. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | WKUPFRMFTR<br>RWK Packet Filter<br>This field contains the various controls of RWK Packet filter.<br>When the Remote Wakeup Filters are to be programmed, the entire set of wkuppktfilter_reg registers must be written. The wkuppktfilter_reg register is programmed by sequentially writing the eight, sixteen or thirty-two register values in MAC_RWK_Packet_Filter register for wkuppktfilter_reg0, wkuppktfilter_reg1, ..., wkuppktfilter_reg31 respectively. The wkuppktfilter_reg register is read in a similar way.<br>The MAC updates the wkuppktfilter_reg register current pointer value in RWKPTR field of MAC_PMT_Control_Status register.<br>The Remote Wakeup Filters are arranged in blocks of 4 filters each and each such block have eight 32-bit wide registers, viz. wkuppktfilter_reg0-7, wkuppktfilter_reg8-15, wkuppktfilter_reg16-23 and wkuppktfilter_reg24-31. The fields of Remote Wakeup Filter are described as follows:<br>Filter i Command: The 4-bit filter i command controls the filter i operation.<br>1. Bit 3 specifies the address type, defining the destination address type of the pattern. When the bit is set, the pattern applies to only multicast packets; when the bit is reset, the pattern applies only to unicast packet.<br>2. Bit 2 (Inverse Mode), when set, reverses the logic of the CRC16 hash function signal, to reject a packet with matching CRC-16 value. Bit 2, along with Bit 1, allows a MAC to reject a subset of remote wake-up packets by creating filter logic such as "Pattern 1 AND NOT Pattern 2".<br>3. Bit 1 (And_Previous) implements the Boolean logic. When set, the result of the current entry is logically ANDed with the result of the previous filter. This AND logic allows a filter pattern longer than 32 bytes by splitting the mask among two, three, or four filters. This depends on the number of filters that have the And_Previous bit set. The details are provided below:<br>(1) The And_Previous bit setting is applicable within a set of 4 filters.<br>(2) Setting of And_Previous bit of filter that is not enabled has no effect, that is setting And_Previous bit of lowest number filter in the set of 4 filters has no effect. For example, setting of And_Previous bit of Filter 0 has no effect.<br>(3) If And_Previous bit is set for filter to form AND chained filter, the AND chain breaks at the point any filter is not enabled. For example: If Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set) but Filter 1 is not enabled (bit 0 in Filter 1 command is reset), then only Filter 2 result is considered. If Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set), Filter 3 And_Previous bit is set (bit 1 in Filter 3 command is set), but Filter 1 is not enabled (bit 0 in Filter 1 command is reset), then only Filter 2 result ANDed with Filter 3 result is considered. If Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set), Filter 3 And_Previous bit is set (bit 1 in Filter 3 command is set), but Filter 2 is not enabled (bit 0 in Filter 2 command is reset), then since setting of Filter 2 And_Previous bit has no effect only Filter 1 result ORed with Filter 3 result is considered. |

**GMAC_RWK_Filter0_Byte_Mask**

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

Address: Operational Base + offset (0x00c4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Filter0_Byte_Mask<br>Filter0 32-bit Mask<br>Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1', the corresponding byte is taken into the CRC16 calculation. |

**GMAC_RWK_Filter1_Byte_Mask**

Address: Operational Base + offset (0x00c4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Filter1_Byte_Mask<br>Filter1 32-bit Mask<br>Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1', the corresponding byte is taken into the CRC16 calculation. |

**GMAC_RWK_Filter2_Byte_Mask**

Address: Operational Base + offset (0x00c4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Filter2_Byte_Mask<br>Filter2 32-bit Mask<br>Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1', the corresponding byte is taken into the CRC16 calculation. |

**GMAC_RWK_Filter3_Byte_Mask**

Address: Operational Base + offset (0x00c4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | Filter3_Byte_Mask<br>Filter3 32-bit Mask<br>Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1', the corresponding byte is taken into the CRC16 calculation. |

**GMAC_RWK_Filter01_CRC**

Address: Operational Base + offset (0x00c4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | Filter1_CRC<br>Filter1 CRC-16<br>This filter CRC-16 contains the CRC_16 value of the pattern.<br>The 16-bit CRC calculation uses the following polynomial:<br>G(x) = x^16 + x^15 + x^2 + 1 |
| 15:0 | RW | 0x0000 | Filter0_CRC<br>Filter0 CRC-16<br>This filter CRC-16 contains the CRC_16 value of the pattern.<br>The 16-bit CRC calculation uses the following polynomial:<br>G(x) = x^16 + x^15 + x^2 + 1 |

**GMAC_RWK_Filter23_CRC**

Address: Operational Base + offset (0x00c4)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | Filter3_CRC<br>Filter3 CRC-16<br>This filter CRC-16 contains the CRC_16 value of the pattern.<br>The 16-bit CRC calculation uses the following polynomial:<br>G(x) = x^16 + x^15 + x^2 + 1 |
| 15:0 | RW | 0x0000 | Filter2_CRC<br>Filter2 CRC-16<br>This filter CRC-16 contains the CRC_16 value of the pattern.<br>The 16-bit CRC calculation uses the following polynomial:<br>G(x) = x^16 + x^15+ x^2 + 1 |

**GMAC_RWK_Filter_Offset**

Address: Operational Base + offset (0x00c4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | Filter3_Offset<br>Filter3 Offset<br>This filter offset defines the offset (within the packet) from which the filter examines the packets.<br>1. This 8-bit pattern-offset is the offset for the filter first byte to be examined.<br>2. The minimum allowed offset is 12, which refers to the 13th byte of the packet.<br>3. The offset value 0 refers to the first byte of the packet. |
| 23:16 | RW | 0x00 | Filter2_Offset<br>Filter2 Offset<br>This filter offset defines the offset (within the packet) from which the filter examines the packets.<br>1. This 8-bit pattern-offset is the offset for the filter first byte to be examined.<br>2. The minimum allowed offset is 12, which refers to the 13th byte of the packet.<br>3. The offset value 0 refers to the first byte of the packet. |
| 15:8 | RW | 0x00 | Filter1_Offset<br>Filter1 Offset<br>This filter offset defines the offset (within the packet) from which the filter examines the packets.<br>1. This 8-bit pattern-offset is the offset for the filter first byte to be examined.<br>2. The minimum allowed offset is 12, which refers to the 13th byte of the packet.<br>3. The offset value 0 refers to the first byte of the packet. |
| 7:0 | RW | 0x00 | Filter0_Offset<br>Filter0 Offset<br>This filter offset defines the offset (within the packet) from which the filter examines the packets.<br>1. This 8-bit pattern-offset is the offset for the filter first byte to be examined.<br>2. The minimum allowed offset is 12, which refers to the 13th byte of the packet.<br>3. The offset value 0 refers to the first byte of the packet. |

**GMAC_RWK_Filter_Command**

Address: Operational Base + offset (0x00c4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 27:24 | RW | 0x0 | Filter3_Command<br>Filter3 Command<br>The 4-bit filter command controls the filter operation.<br>1. Bit 3 specifies the address type, defining the destination address type of the pattern. When the bit is set, the pattern applies to only multicast packets; when the bit is reset, the pattern applies only to unicast packet.<br>2. Bit 2 (Inverse Mode), when set, reverses the logic of the CRC16 hash function signal, to reject a packet with matching CRC_16 value.<br>3. Bit 2, along with Bit 1, allows a MAC to reject a subset of remote wake-up packets by creating filter logic such as "Pattern 1 AND NOT Pattern 2".<br>4. Bit 1 (And_Previous) implements the Boolean logic. When set, the result of the current entry is logically ANDed with the result of the previous filter. This AND logic allows a filter pattern longer than 32 bytes by splitting the mask among two, three, or four filters. This depends on the number of filters that have the And_Previous bit set.<br>5. Bit 0 is the enable for filter. If Bit 0 is not set, filter is disabled. |
| 23:20 | RO | 0x0 | reserved |
| 19:16 | RW | 0x0 | Filter2_Command<br>Filter2 Command<br>The 4-bit filter command controls the filter operation.<br>1. Bit 3 specifies the address type, defining the destination address type of the pattern. When the bit is set, the pattern applies to only multicast packets; when the bit is reset, the pattern applies only to unicast packet.<br>2. Bit 2 (Inverse Mode), when set, reverses the logic of the CRC16 hash function signal, to reject a packet with matching CRC_16 value.<br>3. Bit 2, along with Bit 1, allows a MAC to reject a subset of remote wake-up packets by creating filter logic such as "Pattern 1 AND NOT Pattern 2".<br>4. Bit 1 (And_Previous) implements the Boolean logic. When set, the result of the current entry is logically ANDed with the result of the previous filter. This AND logic allows a filter pattern longer than 32 bytes by splitting the mask among two, three, or four filters. This depends on the number of filters that have the And_Previous bit set.<br>5. Bit 0 is the enable for filter. If Bit 0 is not set, filter is disabled. |
| 15:12 | RO | 0x0 | reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:8 | RW | 0x0 | Filter1_Command<br>Filter1 Command<br>The 4-bit filter command controls the filter operation.<br>1. Bit 3 specifies the address type, defining the destination address type of the pattern. When the bit is set, the pattern applies to only multicast packets; when the bit is reset, the pattern applies only to unicast packet.<br>2. Bit 2 (Inverse Mode), when set, reverses the logic of the CRC16 hash function signal, to reject a packet with matching CRC_16 value.<br>3. Bit 2, along with Bit 1, allows a MAC to reject a subset of remote wake-up packets by creating filter logic such as "Pattern 1 AND NOT Pattern 2".<br>4. Bit 1 (And_Previous) implements the Boolean logic. When set, the result of the current entry is logically ANDed with the result of the previous filter. This AND logic allows a filter pattern longer than 32 bytes by splitting the mask among two, three, or four filters. This depends on the number of filters that have the And_Previous bit set.<br>5. Bit 0 is the enable for filter. If Bit 0 is not set, filter is disabled. |
| 7:4 | RO | 0x0 | reserved |
| 3:0 | RW | 0x0 | Filter0_Command<br>Filter0 Command<br>The 4-bit filter command controls the filter operation.<br>1. Bit 3 specifies the address type, defining the destination address type of the pattern. When the bit is set, the pattern applies to only multicast packets; when the bit is reset, the pattern applies only to unicast packet.<br>2. Bit 2 (Inverse Mode), when set, reverses the logic of the CRC16 hash function signal, to reject a packet with matching CRC_16 value.<br>3. Bit 2, along with Bit 1, allows a MAC to reject a subset of remote wake-up packets by creating filter logic such as "Pattern 1 AND NOT Pattern 2".<br>4. Bit 1 (And_Previous) implements the Boolean logic. When set, the result of the current entry is logically ANDed with the result of the previous filter. This AND logic allows a filter pattern longer than 32 bytes by splitting the mask among two, three, or four filters. This depends on the number of filters that have the And_Previous bit set.<br>5. Bit 0 is the enable for filter. If Bit 0 is not set, filter is disabled. |

**GMAC_MAC_LPI_Control_Status**

Address: Operational Base + offset (0x00d0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 21 | RW | 0x0 | LPITCSE<br>LPI Tx Clock Stop Enable<br>When this bit is set, the MAC asserts sbd_tx_clk_gating_ctrl_o signal high after it enters Tx LPI mode to indicate that the Tx clock to MAC can be stopped.<br>When this bit is reset, the MAC does not assert sbd_tx_clk_gating_ctrl_o signal high after it enters Tx LPI mode.<br>If RGMII Interface is selected, the Tx clock is required for transmitting the LPI pattern. The Tx Clock cannot be gated and so the LPITCSE bit cannot be programmed.<br>Values:<br>1'b0: LPI Tx Clock Stop is disabled<br>1'b1: LPI Tx Clock Stop is enabled |
| 20 | RW | 0x0 | LPIATE<br>LPI Timer Enable<br>This bit controls the automatic entry of the MAC Transmitter into and exit out of the LPI state. When LPIATE, LPITXA and LPIEN bits are set, the MAC Transmitter enters LPI state only when the complete MAC TX data path is IDLE for a period indicated by the MAC_LPI_Entry_Timer register. After entering LPI state, if the data path becomes non-IDLE (due to a new packet being accepted for transmission), the Transmitter exits LPI state but does not clear LPIEN bit. This enables the re-entry into LPI state when it is IDLE again. When LPIATE is 0, the LPI Auto timer is disabled and MAC Transmitter enters LPI state based on the settings of LPITXA and LPIEN bit descriptions.<br>Values:<br>1'b0: LPI Timer is disabled<br>1'b1: LPI Timer is enabled |
| 19 | RW | 0x0 | LPITXA<br>LPI Tx Automate<br>This bit controls the behavior of the MAC when it is entering or coming out of the LPI mode on the Transmit side. This bit is not functional in the EQOS-CORE configurations in which the Tx clock gating is done during the LPI mode.<br>If the LPITXA and LPIEN bits are set to 1, the MAC enters the LPI mode only after all outstanding packets (in the core) and pending packets (in the application interface) have been transmitted. The MAC comes out of the LPI mode when the application sends any packet for transmission or the application issues a Tx FIFO Flush command. In addition, the MAC automatically clears the LPIEN bit when it exits the LPI state. If Tx FIFO Flush is set in the FTQ bit of MTL_TxQ0_Operation_Mode register, when the MAC is in the LPI mode, it exits the LPI mode.<br>When this bit is 0, the LPIEN bit directly controls behavior of the MAC when it is entering or coming out of the LPI mode.<br>Values:<br>1'b0: LPI Tx Automate is disabled<br>1'b1: LPI Tx Automate is enabled |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 18 | RW | 0x0 | PLSEN<br>PHY Link Status Enable<br>This bit enables the link status received on the RGMII, SGMII, or SMII Receive paths to be used for activating the LPI LS TIMER. When this bit is set, the MAC uses the link-status bits of the MAC_PHYIF_Control_Status register and the PLS bit for the LPI LS Timer trigger. When this bit is reset, the MAC ignores the link-status bits of the MAC_PHYIF_Control_Status register and takes only the PLS bit.<br>Values:<br>1'b0: PHY Link Status is disabled<br>1'b1: PHY Link Status is enabled |
| 17 | RW | 0x0 | PLS<br>PHY Link Status<br>This bit indicates the link status of the PHY. The MAC Transmitter asserts the LPI pattern only when the link status is up (OKAY) at least for the time indicated by the LPI LS TIMER.<br>When this bit is set, the link is considered to be okay (UP) and when this bit is reset, the link is considered to be down.<br>Values:<br>1'b0: link is down<br>1'b1: link is okay (UP) |
| 16 | RW | 0x0 | LPIEN<br>LPI Enable<br>When this bit is set, it instructs the MAC Transmitter to enter the LPI state. When this bit is reset, it instructs the MAC to exit the LPI state and resume normal transmission.<br>This bit is cleared when the LPITXA bit is set and the MAC exits the LPI state because of the arrival of a new packet for transmission.<br>Values:<br>1'b0: LPI state is disabled<br>1'b1: LPI state is enabled |
| 15:10 | RO | 0x00 | reserved |
| 9 | RO | 0x0 | RLPIST<br>Receive LPI State<br>When this bit is set, it indicates that the MAC is receiving the LPI pattern on the GMII or MII interface.<br>Values:<br>1'b0: Receive LPI state not detected<br>1'b1: Receive LPI state detected |
| 8 | RO | 0x0 | TLPIST<br>Transmit LPI State<br>When this bit is set, it indicates that the MAC is transmitting the LPI pattern on the GMII or MII interface.<br>Values:<br>1'b0: Transmit LPI state not detected<br>1'b1: Transmit LPI state detected |
| 7:4 | RO | 0x0 | reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | RLPIEX<br>Receive LPI Exit<br>When this bit is set, it indicates that the MAC Receiver has stopped receiving the LPI pattern on the GMII or MII interface, exited the LPI state, and resumed the normal reception. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set).<br>Note: This bit may not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock.<br>Values:<br>1'b0: Receive LPI exit not detected<br>1'b1: Receive LPI exit detected |
| 2 | RO | 0x0 | RLPIEN<br>Receive LPI Entry<br>When this bit is set, it indicates that the MAC Receiver has received an LPI pattern and entered the LPI state. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set).<br>Note: This bit may not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock.<br>Values:<br>1'b0: Receive LPI entry not detected<br>1'b1: Receive LPI entry detected |
| 1 | RO | 0x0 | TLPIEX<br>Transmit LPI Exit<br>When this bit is set, it indicates that the MAC transmitter exited the LPI state after the application cleared the LPIEN bit and the LPI TW Timer has expired. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set).<br>Values:<br>1'b0: Transmit LPI exit not detected<br>1'b1: Transmit LPI exit detected |
| 0 | RO | 0x0 | TLPIEN<br>Transmit LPI Entry<br>When this bit is set, it indicates that the MAC Transmitter has entered the LPI state because of the setting of the LPIEN bit. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set).<br>Values:<br>1'b0: Transmit LPI entry not detected<br>1'b1: Transmit LPI entry detected |

**GMAC_MAC_LPI_Timers_Control**

Address: Operational Base + offset (0x00d4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 25:16 | RW | 0x3e8 | LST<br>LPI LS Timer<br>This field specifies the minimum time (in milliseconds) for which the link status from the PHY should be up (OKAY) before the LPI pattern can be transmitted to the PHY. The MAC does not transmit the LPI pattern even when the LPIEN bit is set unless the LPI LS Timer reaches the programmed terminal count. The default value of the LPI LS Timer is 1000 (1 sec) as defined in the IEEE standard. |
| 15:0 | RW | 0x0000 | TWT<br>LPI TW Timer<br>This field specifies the minimum time (in microseconds) for which the MAC waits after it stops transmitting the LPI pattern to the PHY and before it resumes the normal transmission. The TLPIEX status bit is set after the expiry of this timer. |

**GMAC_MAC_LPI_Entry_Timer**

Address: Operational Base + offset (0x00d8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:3 | RW | 0x00000 | LPIET<br>LPI Entry Timer<br>This field specifies the time in microseconds the MAC waits to enter LPI mode, after it has transmitted all the frames. This field is valid and used only when LPITE and LPITXA are set to 1. Bits [2:0] are read-only so that the granularity of this timer is in steps of 8 micro-seconds. |

**GMAC_MAC_1US_Tic_Counter**

Address: Operational Base + offset (0x00dc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x03f | TIC_1US_CNTR<br>1US TIC Counter<br>The application must program this counter so that the number of clock cycles of CSR clock is 1us. (Subtract 1 from the value before programming). For example if the CSR clock is 100MHz then this field needs to be programmed to value 100 - 1 = 99 (which is 0x63). This is required to generate the 1US events that are used to update some of the EEE related counters. |

**GMAC_MAC_PHYIF_Control_Status**

Address: Operational Base + offset (0x00f8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19 | RO | 0x0 | LNKSTS<br>Link Status<br>This bit indicates whether the link is up (1'b1) or down (1'b0).<br>Values:<br>1'b0: Link down<br>1'b1: Link up |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 18:17 | RO | 0x0 | LNKSPEED<br>Link Speed<br>This bit indicates the current speed of the link. Bit 2 is reserved when the MAC is configured for the SMII PHY interface.<br>Values:<br>2'b00: 2.5 MHz<br>2'b01: 25 MHz<br>2'b10: 125 MHz<br>2'b11: Reserved |
| 16 | RO | 0x0 | LNKMOD<br>Link Mode<br>This bit indicates the current mode of operation of the link.<br>Values:<br>1'b0: Half-duplex mode<br>1'b1: Full-duplex mode |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x0 | LUD<br>Link Up or Down<br>This bit indicates whether the link is up or down during transmission of configuration in the RGMII, SGMII, or SMII interface.<br>Values:<br>1'b0: Link down<br>1'b1: Link up |
| 0 | RW | 0x0 | TC<br>Transmit Configuration in RGMII, SGMII, or SMII<br>When set, this bit enables the transmission of duplex mode, link speed, and link up or down information to the PHY in the RGMII, SMII, or SGMII port. When this bit is reset, no such information is driven to the PHY. The details of this feature are provided in the following sections:<br>1. "Reduced Gigabit Media Independent Interface"<br>2. "Serial Media Independent Interface"<br>3. "Serial Gigabit Media Independent Interface"<br>Values:<br>1'b0: Disable Transmit Configuration in RGMII, SGMII, or SMII<br>1'b1: Enable Transmit Configuration in RGMII, SGMII, or SMII |

**GMAC_MAC_Version**

Address: Operational Base + offset (0x0110)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:8 | RW | 0x30 | USERVER<br>User-defined Version |
| 7:0 | RW | 0x51 | RKVER<br>Rockchip-defined Version |

**GMAC_MAC_Debug**

Address: Operational Base + offset (0x0114)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:19 | RO | 0x0000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 18:17 | RO | 0x0 | TFCSTS<br>MAC Transmit Packet Controller Status<br>This field indicates the state of the MAC Transmit Packet Controller module.<br>Values:<br>2'b00: Idle state<br>2'b01: Waiting for one of the following: Status of the previous packet OR IPG or back off period to be over<br>2'b10: Generating and transmitting a Pause control packet (in full-duplex mode)<br>2'b11: Transferring input packet for transmission |
| 16 | RO | 0x0 | TPESTS<br>MAC GMII or MII Transmit Protocol Engine Status<br>When this bit is set, it indicates that the MAC GMII or MII transmit protocol engine is actively transmitting data, and it is not in the Idle state.<br>Values:<br>1'b0: MAC GMII or MII Transmit Protocol Engine Status not detected<br>1'b1: MAC GMII or MII Transmit Protocol Engine Status detected |
| 15:3 | RO | 0x0000 | reserved |
| 2:1 | RO | 0x0 | RFCFCSTS<br>MAC Receive Packet Controller FIFO Status<br>When this bit is set, this field indicates the active state of the small FIFO Read and Write controllers of the MAC Receive Packet Controller module. |
| 0 | RO | 0x0 | RPESTS<br>MAC GMII or MII Receive Protocol Engine Status<br>When this bit is set, it indicates that the MAC GMII or MII receive protocol engine is actively receiving data, and it is not in the Idle state.<br>Values:<br>1'b0: MAC GMII or MII Receive Protocol Engine Status not detected<br>1'b1: MAC GMII or MII Receive Protocol Engine Status detected |

**GMAC_MAC_HW_Feature0**

Address: Operational Base + offset (0x011c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x1 | ACTPHYSEL<br>Active PHY Selected<br>When you have multiple PHY interfaces in your configuration, this field indicates the sampled value of phy_intf_sel_i during reset de-assertion.<br>Values:<br>4'b0000: GMII or MII<br>4'b0001: RGMII<br>4'b0010: SGMII<br>4'b0011: TBI<br>4'b0100: RMII<br>4'b0101: RTBI<br>4'b0110: SMII<br>4'b0111: RevMII |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 27 | RO | 0x1 | SAVLANINS<br>Source Address or VLAN Insertion Enable<br>This bit is set to 1 when the Enable SA and VLAN Insertion on Tx option is selected.<br>Values:<br>1'b0: Source Address or VLAN Insertion Enable option is not selected<br>1'b1: Source Address or VLAN Insertion Enable option is selected |
| 26:25 | RO | 0x0 | TSSTSSEL<br>Timestamp System Time Source<br>This bit indicates the source of the Timestamp system time:<br>This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected.<br>Values:<br>2'b00: Internal<br>2'b01: External<br>2'b10: Both<br>2'b11: Reserved |
| 24 | RO | 0x0 | MACADR64SEL<br>MAC Addresses 64-127 Selected<br>This bit is set to 1 when the Enable Additional 64 MAC Address Registers (64-127) option is selected.<br>Values:<br>1'b0: MAC Addresses 64-127 Select option is not selected<br>1'b1: MAC Addresses 64-127 Select option is selected |
| 23 | RO | 0x0 | MACADR32SEL<br>MAC Addresses 32-63 Selected<br>This bit is set to 1 when the Enable Additional 32 MAC Address Registers (32-63) option is selected.<br>Values:<br>1'b0: MAC Addresses 32-63 Select option is not selected<br>1'b1: MAC Addresses 32-63 Select option is selected |
| 22:18 | RO | 0x04 | ADDMACADRSEL<br>MAC Addresses 1-31 Selected<br>This bit is set to 1 when the non-zero value is selected for Enable Additional 1-31 MAC Address Registers option. |
| 17 | RO | 0x0 | reserved |
| 16 | RO | 0x1 | RXCOESEL<br>Receive Checksum Offload Enabled<br>This bit is set to 1 when the Enable Receive TCP/IP Checksum Check option is selected.<br>Values:<br>1'b0: Receive Checksum Offload Enable option is not selected<br>1'b1: Receive Checksum Offload Enable option is selected |
| 15 | RO | 0x0 | reserved |
| 14 | RO | 0x1 | TXCOESEL<br>Transmit Checksum Offload Enabled<br>This bit is set to 1 when the Enable Transmit TCP/IP Checksum Insertion option is selected.<br>Values:<br>1'b0: Transmit Checksum Offload Enable option is not selected<br>1'b1: Transmit Checksum Offload Enable option is selected |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RO | 0x1 | EEESEL<br>Energy Efficient Ethernet Enabled<br>This bit is set to 1 when the Enable Energy Efficient Ethernet (EEE) option is selected.<br>Values:<br>1'b0: Energy Efficient Ethernet Enable option is not selected<br>1'b1: Energy Efficient Ethernet Enable option is selected |
| 12 | RO | 0x1 | TSSEL<br>IEEE 1588-2008 Timestamp Enabled<br>This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected.<br>Values:<br>1'b0: IEEE 1588-2008 Timestamp Enable option is not selected.<br>1'b1: IEEE 1588-2008 Timestamp Enable option is selected. |
| 11:10 | RO | 0x0 | reserved |
| 9 | RO | 0x1 | ARPOFFSEL<br>ARP Offload Enabled<br>This bit is set to 1 when the Enable IPv4 ARP Offload option is selected.<br>Values:<br>1'b0: ARP Offload Enable option is not selected<br>1'b1: ARP Offload Enable option is selected |
| 8 | RO | 0x1 | MMCSEL<br>RMON Module Enable<br>This bit is set to 1 when the Enable MAC Management Counters (MMC) option is selected.<br>Values:<br>1'b0: RMON Module Enable option is not selected<br>1'b1: RMON Module Enable option is selected |
| 7 | RO | 0x1 | MGKSEL<br>PMT Magic Packet Enable<br>This bit is set to 1 when the Enable Magic Packet Detection option is selected.<br>Values:<br>1'b0: PMT Magic Packet Enable option is not selected<br>1'b1: PMT Magic Packet Enable option is selected |
| 6 | RO | 0x1 | RWKSEL<br>PMT Remote Wake-up Packet Enable<br>This bit is set to 1 when the Enable Remote Wake-Up Packet Detection option is selected.<br>Values:<br>1'b0: PMT Remote Wake-up Packet Enable option is not selected<br>1'b1: PMT Remote Wake-up Packet Enable option is selected |
| 5 | RO | 0x1 | SMASEL<br>SMA (MDIO) Interface<br>This bit is set to 1 when the Enable Station Management (MDIO Interface) option is selected.<br>Values:<br>1'b0: SMA (MDIO) Interface not selected<br>1'b1: SMA (MDIO) Interface selected |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RO | 0x1 | VLHASH<br>VLAN Hash Filter Selected<br>This bit is set to 1 when the Enable VLAN Hash Table Based Filtering option is selected.<br>Values:<br>1'b0: VLAN Hash Filter not selected<br>1'b1: VLAN Hash Filter selected |
| 3 | RO | 0x0 | PCSSEL<br>PCS Registers (TBI, SGMII, or RTBI PHY interface)<br>This bit is set to 1 when the TBI, SGMII, or RTBI PHY interface option is selected.<br>Values:<br>1'b0: No PCS Registers (TBI, SGMII, or RTBI PHY interface)<br>1'b1: PCS Registers (TBI, SGMII, or RTBI PHY interface) |
| 2 | RO | 0x0 | HDSEL<br>Half-duplex Support<br>This bit is set to 1 when the half-duplex mode is selected.<br>Values:<br>1'b0: No Half-duplex support<br>1'b1: Half-duplex support |
| 1 | RO | 0x1 | GMIISEL<br>1000 Mbps Support<br>This bit is set to 1 when 1000 Mbps is selected as the Mode of Operation.<br>Values:<br>1'b0: No 1000 Mbps support<br>1'b1: 1000 Mbps support |
| 0 | RO | 0x1 | MIISEL<br>10 or 100 Mbps Support<br>This bit is set to 1 when 10/100 Mbps is selected as the Mode of Operation.<br>Values:<br>1'b0: No 10 or 100 Mbps support<br>1'b1: 10 or 100 Mbps support |

**GMAC_MAC_HW_Feature1**

Address: Operational Base + offset (0x0120)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |
| 30:27 | RO | 0x2 | L3L4FNUM<br>Total number of L3 or L4 Filters<br>This field indicates the total number of L3 or L4 filters:<br>Values:<br>4'b0000: No L3 or L4 Filter<br>4'b0001: 1 L3 or L4 Filter<br>4'b0010: 2 L3 or L4 Filters<br>4'b0011: 3 L3 or L4 Filters<br>4'b0100: 4 L3 or L4 Filters<br>4'b0101: 5 L3 or L4 Filters<br>4'b0110: 6 L3 or L4 Filters<br>4'b0111: 7 L3 or L4 Filters<br>4'b1000: 8 L3 or L4 Filters |
| 26 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 25:24 | RO | 0x1 | HASHTBLSZ<br>Hash Table Size<br>This field indicates the size of the hash table:<br>Values:<br>2'b00: No hash table<br>2'b01: 64<br>2'b10: 128<br>2'b11: 256 |
| 23 | RO | 0x0 | POUOST<br>One Step for PTP over UDP/IP Feature Enable<br>This bit is set to 1 when the Enable One step timestamp for PTP over UDP/IP feature is selected.<br>Values:<br>1'b0: One Step for PTP over UDP/IP Feature is not selected<br>1'b1: One Step for PTP over UDP/IP Feature is selected |
| 22 | RO | 0x0 | reserved |
| 21 | RO | 0x0 | RAVSEL<br>Rx Side Only AV Feature Enable<br>This bit is set to 1 when the Enable Audio Video Bridging option on Rx Side Only is selected.<br>Values:<br>1'b0: Rx Side Only AV Feature is not selected<br>1'b1: Rx Side Only AV Feature is selected |
| 20 | RO | 0x1 | AVSEL<br>AV Feature Enable<br>This bit is set to 1 when the Enable Audio Video Bridging option is selected.<br>Values:<br>1'b0: AV Feature is not selected<br>1'b1: AV Feature is selected |
| 19 | RO | 0x1 | DBGMEMA<br>DMA Debug Registers Enable<br>This bit is set to 1 when the Debug Mode Enable option is selected.<br>Values:<br>1'b0: DMA Debug Registers option is not selected<br>1'b1: DMA Debug Registers option is selected |
| 18 | RO | 0x1 | TSOEN<br>TCP Segmentation Offload Enable<br>This bit is set to 1 when the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected.<br>Values:<br>1'b0: TCP Segmentation Offload Feature is not selected<br>1'b1: TCP Segmentation Offload Feature is selected |
| 17 | RO | 0x1 | SPHEN<br>Split Header Feature Enable<br>This bit is set to 1 when the Enable Split Header Structure option is selected.<br>Values:<br>1'b0: Split Header Feature is not selected<br>1'b1: Split Header Feature is selected |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 16 | RO | 0x0 | DCBEN<br>DCB Feature Enable<br>This bit is set to 1 when the Enable Data Center Bridging option is selected.<br>Values:<br>1'b0: DCB Feature is not selected<br>1'b1: DCB Feature is selected |
| 15:14 | RO | 0x0 | ADDR64<br>Address Width<br>This field indicates the configured address width:<br>Values:<br>2'b00: 32<br>2'b01: 40<br>2'b10: 48<br>2'b11: Reserved |
| 13 | RO | 0x0 | ADVTHWORD<br>IEEE 1588 High Word Register Enable<br>This bit is set to 1 when the Add IEEE 1588 Higher Word Register option is selected.<br>Values:<br>1'b0: IEEE 1588 High Word Register option is not selected<br>1'b1: IEEE 1588 High Word Register option is selected |
| 12 | RO | 0x0 | PTOEN<br>PTP Offload Enable<br>This bit is set to 1 when the Enable PTP Timestamp Offload Feature is selected.<br>Values:<br>1'b0: PTP Offload feature is not selected<br>1'b1: PTP Offload feature is selected |
| 11 | RO | 0x0 | OSTEN<br>One-Step Timestamping Enable<br>This bit is set to 1 when the Enable One-Step Timestamp Feature is selected.<br>Values:<br>1'b0: One-Step Timestamping feature is not selected<br>1'b1: One-Step Timestamping feature is selected |
| 10:6 | RO | 0x07 | TXFIFOSIZE<br>MTL Transmit FIFO Size<br>This field contains the configured value of MTL Tx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(TXFIFO_SIZE) -7:<br>Values:<br>5'b00000: 128 bytes<br>5'b00001: 256 bytes<br>5'b00010: 512 bytes<br>5'b00011: 1024 bytes<br>5'b00100: 2048 bytes<br>5'b00101: 4096 bytes<br>5'b00110: 8192 bytes<br>5'b00111: 16384 bytes<br>5'b01000: 32 KB<br>5'b01001: 64 KB<br>5'b01010: 128 KB<br>5'b01011: Reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RO | 0x1 | SPRAM<br>Single Port RAM Enable<br>This bit is set to 1 when the Use single port RAM Feature is selected.<br>Values:<br>1'b0: Single Port RAM feature is not selected<br>1'b1: Single Port RAM feature is selected |
| 4:0 | RO | 0x08 | RXFIFOSIZE<br>MTL Receive FIFO Size<br>This field contains the configured value of MTL Rx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(RXFIFO_SIZE) -7:<br>Values:<br>5'b00000: 128 bytes<br>5'b00001: 256 bytes<br>5'b00010: 512 bytes<br>5'b00011: 1024 bytes<br>5'b00100: 2048 bytes<br>5'b00101: 4096 bytes<br>5'b00110: 8192 bytes<br>5'b00111: 16384 bytes<br>5'b01000: 32 KB<br>5'b01001: 64 KB<br>5'b01010: 128 KB<br>5'b01011: 256 KB<br>5'b01100: Reserved |

**GMAC_MAC_HW_Feature2**

Address: Operational Base + offset (0x0124)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |
| 30:28 | RO | 0x1 | AUXSNAPNUM<br>Number of Auxiliary Snapshot Inputs<br>This field indicates the number of auxiliary snapshot inputs:<br>Values:<br>3'b000: No auxiliary input<br>3'b001: 1 auxiliary input<br>3'b010: 2 auxiliary input<br>3'b011: 3 auxiliary input<br>3'b100: 4 auxiliary input<br>3'b101: Reserved |
| 27 | RO | 0x0 | reserved |
| 26:24 | RO | 0x1 | PPSOUTNUM<br>Number of PPS Outputs<br>This field indicates the number of PPS outputs:<br>Values:<br>3'b000: No PPS output<br>3'b001: 1 PPS output<br>3'b010: 2 PPS output<br>3'b011: 3 PPS output<br>3'b100: 4 PPS output<br>3'b101: Reserved |
| 23:22 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 21:18 | RO | 0x1 | TXCHCNT<br>Number of DMA Transmit Channels<br>This field indicates the number of DMA Transmit channels:<br>Values:<br>4'b0000: 1 MTL Tx Channel<br>4'b0001: 2 MTL Tx Channels<br>4'b0010: 3 MTL Tx Channels<br>4'b0011: 4 MTL Tx Channels<br>4'b0100: 5 MTL Tx Channels<br>4'b0101: 6 MTL Tx Channels<br>4'b0110: 7 MTL Tx Channels<br>4'b0111: 8 MTL Tx Channels |
| 17:16 | RO | 0x0 | reserved |
| 15:12 | RO | 0x1 | RXCHCNT<br>Number of DMA Receive Channels<br>This field indicates the number of DMA Receive channels:<br>Values:<br>4'b0000: 1 MTL Rx Channel<br>4'b0001: 2 MTL Rx Channels<br>4'b0010: 3 MTL Rx Channels<br>4'b0011: 4 MTL Rx Channels<br>4'b0100: 5 MTL Rx Channels<br>4'b0101: 6 MTL Rx Channels<br>4'b0110: 7 MTL Rx Channels<br>4'b0111: 8 MTL Rx Channels |
| 11:10 | RO | 0x0 | reserved |
| 9:6 | RO | 0x1 | TXQCNT<br>Number of MTL Transmit Queues<br>This field indicates the number of MTL Transmit queues:<br>Values:<br>4'b0000: 1 MTL Tx Queue<br>4'b0001: 2 MTL Tx Queues<br>4'b0010: 3 MTL Tx Queues<br>4'b0011: 4 MTL Tx Queues<br>4'b0100: 5 MTL Tx Queues<br>4'b0101: 6 MTL Tx Queues<br>4'b0110: 7 MTL Tx Queues<br>4'b0111: 8 MTL Tx Queues |
| 5:4 | RO | 0x0 | reserved |
| 3:0 | RO | 0x1 | RXQCNT<br>Number of MTL Receive Queues<br>This field indicates the number of MTL Receive queues:<br>Values:<br>4'b0000: 1 MTL Rx Queue<br>4'b0001: 2 MTL Rx Queues<br>4'b0010: 3 MTL Rx Queues<br>4'b0011: 4 MTL Rx Queues<br>4'b0100: 5 MTL Rx Queues<br>4'b0101: 6 MTL Rx Queues<br>4'b0110: 7 MTL Rx Queues<br>4'b0111: 8 MTL Rx Queues |

**GMAC_MAC_HW_Feature3**

Address: Operational Base + offset (0x0128)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:28 | RO | 0x0 | ASP<br>Automotive Safety Package<br>Following are the encoding for the different Safety features.<br>Values:<br>2'b00: No Safety features selected<br>2'b01: Only "ECC protection for external memory" feature is selected<br>2'b10: All the Automotive Safety features are selected without the "Parity Port Enable for external interface" feature<br>2'b11: All the Automotive Safety features are selected with the "Parity Port Enable for external interface" feature |
| 27 | RO | 0x1 | TBSSEL<br>Time Based Scheduling Enable<br>This bit is set to 1 when the Time Based Scheduling feature is selected.<br>Values:<br>1'b0: Time Based Scheduling Enable feature is not selected<br>1'b1: Time Based Scheduling Enable feature is selected |
| 26 | RO | 0x1 | FPESEL<br>Frame Preemption Enable<br>This bit is set to 1 when the Enable Frame preemption feature is selected.<br>Values:<br>1'b0: Frame Preemption Enable feature is not selected<br>1'b1: Frame Preemption Enable feature is selected |
| 25:22 | RO | 0x0 | reserved |
| 21:20 | RO | 0x3 | ESTWID<br>Width of the Time Interval field in the Gate Control List<br>This field indicates the width of the Configured Time Interval Field.<br>Values:<br>2'b00: Width not configured<br>2'b01: 16<br>2'b10: 20<br>2'b11: 24 |
| 19:17 | RW | 0x3 | ESTDEP<br>Depth of the Gate Control List<br>This field indicates the depth of Gate Control list expressed as Log2(GMAC_EST_DEP)-5.<br>Values:<br>3'b000: No Depth configured<br>3'b001: 64<br>3'b010: 128<br>3'b011: 256<br>3'b100: 512<br>3'b101: 1024<br>3'b110: Reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 16 | RO | 0x1 | ESTSEL<br>Enhancements to Scheduling Traffic Enable<br>This bit is set to 1 when the Enable Enhancements to Scheduling Traffic feature is selected.<br>Values:<br>1'b0: Enable Enhancements to Scheduling Traffic feature is not selected<br>1'b1: Enable Enhancements to Scheduling Traffic feature is selected |
| 15 | RO | 0x0 | reserved |
| 14:13 | RO | 0x0 | FRPES<br>Flexible Receive Parser Table Entries size<br>This field indicates the Max Number of Parser Entries supported by Flexible Receive Parser.<br>Values:<br>2'b00: 64 Entries<br>2'b01: 128 Entries<br>2'b10: 256 Entries<br>2'b11: Reserved |
| 12:11 | RO | 0x0 | FRPBS<br>Flexible Receive Parser Buffer size<br>This field indicates the supported Max Number of bytes of the packet data to be Parsed by Flexible Receive Parser.<br>Values:<br>2'b00: 64 Bytes<br>2'b01: 128 Bytes<br>2'b10: 256 Bytes<br>2'b11: Reserved |
| 10 | RO | 0x0 | FRPSEL<br>Flexible Receive Parser Selected<br>This bit is set to 1 when the Enable Flexible Programmable Receive Parser option is selected.<br>Values:<br>1'b0: Flexible Receive Parser feature is not selected<br>1'b1: Flexible Receive Parser feature is selected |
| 9 | RO | 0x0 | PDUPSEL<br>Broadcast/Multicast Packet Duplication<br>This bit is set to 1 when the Broadcast/Multicast Packet Duplication feature is selected.<br>Values:<br>1'b0: Broadcast/Multicast Packet Duplication feature is not selected<br>1'b1: Broadcast/Multicast Packet Duplication feature is selected |
| 8:6 | RO | 0x0 | reserved |
| 5 | RO | 0x1 | DVLAN<br>Double VLAN Tag Processing Selected<br>This bit is set to 1 when the Enable Double VLAN Processing Feature is selected.<br>Values:<br>1'b0: Double VLAN option is not selected<br>1'b1: Double VLAN option is selected |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RO | 0x1 | CBTISEL<br>Queue/Channel based VLAN tag insertion on Tx Enable<br>This bit is set to 1 when the Enable Queue/Channel based VLAN tag insertion on Tx Feature is selected.<br>Values:<br>1'b0: Enable Queue/Channel based VLAN tag insertion on Tx feature is not selected<br>1'b1: Enable Queue/Channel based VLAN tag insertion on Tx feature is selected |
| 3 | RO | 0x0 | reserved |
| 2:0 | RO | 0x1 | NRVF<br>Number of Extended VLAN Tag Filters Enabled<br>This field indicates the Number of Extended VLAN Tag Filters selected:<br>Values:<br>3'b000: No Extended Rx VLAN Filters<br>3'b001: 4 Extended Rx VLAN Filters<br>3'b010: 8 Extended Rx VLAN Filters<br>3'b011: 16 Extended Rx VLAN Filters<br>3'b100: 24 Extended Rx VLAN Filters<br>3'b101: 32 Extended Rx VLAN Filters<br>3'b110: Reserved |

**GMAC_MAC_MDIO_Address**

Address: Operational Base + offset (0x0200)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27 | RW | 0x0 | PSE<br>Preamble Suppression Enable<br>When this bit is set, the SMA suppresses the 32-bit preamble and transmits MDIO frames with only 1 preamble bit. When this bit is 0, the MDIO frame always has 32 bits of preamble as defined in the IEEE specifications.<br>Values:<br>1'b0: Preamble Suppression disabled<br>1'b1: Preamble Suppression enabled |
| 26 | RW | 0x0 | BTB<br>Back to Back transactions<br>When this bit is set and the NTC has value greater than 0, then the MAC informs the completion of a read or write command at the end of frame transfer (before the trailing clocks are transmitted). The software can thus initiate the next command which is executed immediately irrespective of the number trailing clocks generated for the previous frame. When this bit is reset, then the read/write command completion (GB is cleared) only after the trailing clocks are generated. In this mode, it is ensured that the NTC is always generated after each frame. This bit must not be set when NTC=0.<br>Values:<br>1'b0: Back to Back transactions disabled<br>1'b1: Back to Back transactions enabled |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 25:21 | RW | 0x00 | PA<br>Physical Layer Address<br>This field indicates which Clause 22 PHY devices (out of 32 devices) the MAC is accessing. For RevMII, this field gives the PHY Address of the RevMII module. This field indicates which Clause 45 capable PHYs (out of 32 PHYs) the MAC is accessing. |
| 20:16 | RW | 0x00 | RDA<br>Register/Device Address<br>These bits select the PHY register in selected Clause 22 PHY device. For RevMII, these bits select the CSR register in the RevMII Registers set. These bits select the Device (MMD) in selected Clause 45 capable PHY. |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x0 | NTC<br>Number of Trailing Clocks<br>This field controls the number of trailing clock cycles generated on gmii_mdc_o (MDC) after the end of transmission of MDIO frame. The valid values can be from 0 to 7. Programming the value to 3'h3 indicates that there are additional three clock cycles on the MDC line after the end of MDIO frame transfer. |
| 11:8 | RW | 0x0 | CR<br>CSR Clock Range<br>The CSR Clock Range selection determines the frequency of the MDC clock according to the CSR clock frequency used in your design:<br>4'b0000: CSR clock = 60-100 MHz; MDC clock = CSR clock/42<br>4'b0001: CSR clock = 100-150 MHz; MDC clock = CSR clock/62<br>4'b0010: CSR clock = 20-35 MHz; MDC clock = CSR clock/16<br>4'b0011: CSR clock = 35-60 MHz; MDC clock = CSR clock/26<br>4'b0100: CSR clock = 150-250 MHz; MDC clock = CSR clock/102<br>4'b0101: CSR clock = 250-300 MHz; MDC clock = CSR clock/124<br>4'b0110: CSR clock = 300-500 MHz; MDC clock = CSR clock/204<br>4'b0111: CSR clock = 500-800 MHz; MDC clock = CSR clock/324<br>The suggested range of CSR clock frequency applicable for each value (when Bit 11 = 0) ensures that the MDC clock is approximately between 1.0 MHz to 2.5 MHz frequency range. When Bit 11 is set, you can achieve a higher frequency of the MDC clock than the frequency limit of 2.5 MHz (specified in the IEEE 802.3) and program a clock divider of lower value. For example, when CSR clock is of 100 MHz frequency and you program these bits as 1010, the resultant MDC clock is of 12.5 MHz which is above the range specified in IEEE 802.3. Program the following values only if the interfacing chips support faster MDC clocks:<br>4'b1000: CSR clock/4<br>4'b1001: CSR clock/6<br>4'b1010: CSR clock/8<br>4'b1011: CSR clock/10<br>4'b1100: CSR clock/12<br>4'b1101: CSR clock/14<br>4'b1110: CSR clock/16<br>4'b1111: CSR clock/18<br>These bits are not used for accessing RevMII. These bits are read-only if the RevMII interface is selected as single PHY interface. |
| 7:5 | RO | 0x0 | reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | SKAP<br>Skip Address Packet<br>When this bit is set, the SMA does not send the address packets before read, write, or post-read increment address packets. This bit is valid only when C45E is set.<br>Values:<br>1'b0: Skip Address Packet is disabled<br>1'b1: Skip Address Packet is enabled |
| 3 | RW | 0x0 | GOC_1<br>GMII Operation Command 1<br>This bit is higher bit of the operation command to the PHY or RevMII, GOC_1 and GOC_O is encoded as follows:<br>2'b00: Reserved<br>2'b01: Write<br>2'b10: Post Read Increment Address for Clause 45 PHY<br>2'b11: Read<br>When Clause 22 PHY or RevMII is enabled, only Write and Read commands are valid.<br>Values:<br>1'b0: GMII Operation Command 1 is disabled<br>1'b1: GMII Operation Command 1 is enabled |
| 2 | RW | 0x0 | GOC_0<br>GMII Operation Command 0<br>This is the lower bit of the operation command to the PHY or RevMII. When in SMA mode (MDIO master) this bit along with GOC_1 determines the operation to be performed to the PHY. When only RevMII is selected in configuration this bit is read-only and tied to 1.<br>Values:<br>1'b0: GMII Operation Command 0 is disabled<br>1'b1: GMII Operation Command 0 is enabled |
| 1 | RW | 0x0 | C45E<br>Clause 45 PHY Enable<br>When this bit is set, Clause 45 capable PHY is connected to MDIO. When this bit is reset, Clause 22 capable PHY is connected to MDIO.<br>Values:<br>1'b0: Clause 45 PHY is disabled<br>1'b1: Clause 45 PHY is enabled |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | GB<br>GMII Busy<br>The application sets this bit to instruct the SMA to initiate a Read or Write access to the MDIO slave. The MAC clears this bit after the MDIO frame transfer is completed. Hence the software must not write or change any of the fields in MAC_MDIO_Address and MAC_MDIO_Data registers as long as this bit is set.<br>For write transfers, the application must first write 16-bit data in the GDl field (and also RA field when C45E is set) in MAC_MDIO_Data register before setting this bit. When C45E is set, it should also write into the RA field of MAC_MDIO_Data register before initiating a read transfer. When a read transfer is completed (GB=0), the data read from the PHY register is valid in the GD field of the MAC_MDIO_Data register.<br>Note: Even if the addressed PHY is not present, there is no change in the functionality of this bit. Access restriction applies.<br>Setting 1 sets. Self-cleared. Setting 0 has no effect.<br>Values:<br>1'b0: GMII Busy is disabled<br>1'b1: GMII Busy is enabled |

**GMAC_MAC_MDIO_Data**

Address: Operational Base + offset (0x0204)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16 | RW | 0x0 | RA<br>Register Address<br>This field is valid only when C45E is set. It contains the Register Address in the PHY to which the MDIO frame is intended for. |
| 15:0 | RW | 0x0000 | GD<br>GMII Data<br>This field contains the 16-bit data value read from the PHY or RevMII after a Management Read operation or the 16-bit data value to be written to the PHY or RevMII before a Management Write operation. |

**GMAC_MAC_ARP_Address**

Address: Operational Base + offset (0x0210)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ARPPA<br>ARP Protocol Address<br>This field contains the IPv4 Destination Address of the MAC. This address is used for perfect match with the Protocol Address of Target field in the received ARP packet.<br>This field is available only when the Enable IPv4 ARP Offload option is selected. |

**GMAC_MAC_CSR_SW_Ctrl**

Address: Operational Base + offset (0x0230)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | RCWE<br>Register Clear on Write 1 Enable<br>When this bit is set, the access mode of some register fields changes to Clear on Write 1, the application needs to set that respective bit to 1 to clear it. When this bit is reset, the access mode of these register fields remain as Clear on Read.<br>Values:<br>1'b0: Register Clear on Write 1 is disabled<br>1'b1: Register Clear on Write 1 is enabled |

**GMAC_MAC_FPE_CTRL_STS**

Address: Operational Base + offset (0x0234)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19 | RW | 0x0 | TRSP<br>Transmitted Respond Frame<br>Set when a Respond mPacket is transmitted (triggered by setting SRSP field). An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.<br>Values:<br>0x0 (INACTIVE): Not transmitted Respond Frame<br>0x1 (ACTIVE): transmitted Respond Frame |
| 18 | RW | 0x0 | TVER<br>Transmitted Verify Frame<br>Set when a Verify mPacket is transmitted (triggered by setting SVER field). An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.<br>Values:<br>0x0 (INACTIVE): Not transmitted Verify Frame<br>0x1 (ACTIVE): transmitted Verify Frame |
| 17 | RW | 0x0 | RRSP<br>Received Respond Frame<br>Set when a Respond mPacket is received. An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set.<br>Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.<br>Values:<br>0x0 (INACTIVE): Not received Respond Frame<br>0x1 (ACTIVE): Received Respond Frame |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 16 | RW | 0x0 | RVER<br>Received Verify Frame<br>Set when a Verify mPacket is received. An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set.<br>Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.<br>Values:<br>0x0 (INACTIVE): Not received Verify Frame<br>0x1 (ACTIVE): Received Verify Frame |
| 15:4 | RO | 0x000 | reserved |
| 3 | RW | 0x0 | S1_SET_0<br>Reserved, Must be set to "0". This field is reserved for Internal use, and must always be set to "0" unless instructed by Rockchip. Setting to "1" might cause unexpected behavior in the IP. |
| 2 | RW | 0x0 | SRSP<br>Send Respond mPacket<br>When set indicates hardware to send a Respond mPacket. Reset by hardware after sending the Respond mPacket. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.<br>Values:<br>0x0 (DISABLE): Send Respond mPacket is disabled<br>0x1 (ENABLE): Send Respond mPacket is enabled |
| 1 | RW | 0x0 | SVER<br>Send Verify mPacket<br>When set indicates hardware to send a verify mPacket. Reset by hardware after sending the Verify mPacket.<br>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.<br>Values:<br>0x0 (DISABLE): Send Verify mPacket is disabled<br>0x1 (ENABLE): Send Verify mPacket is enabled |
| 0 | RW | 0x0 | EFPE<br>Enable Tx Frame Preemption<br>When set Frame Preemption Tx functionality is enabled.<br>Values:<br>0x0 (DISABLE): Tx Frame Preemption is disabled<br>0x1 (ENABLE): Tx Frame Preemption is enabled |

**GMAC_MAC_Ext_Cfg1**

Address: Operational Base + offset (0x0238)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9:8 | RW | 0x0 | SPLM<br>Split Mode<br>These bits indicate the mode of splitting the incoming Rx packets.<br>Values:<br>0x0 (L3L4): Split at L3/L4 header<br>0x1 (L2OFST): Split at L2 header with an offset. Always Split at SPLOFST bytes from the beginning of Length/Type field of the Frame<br>0x2 (COMBN): Combination mode: Split similar to SPLM=00 for IP packets that are untagged or tagged and VLAN stripped<br>0x3 (Reserved): Reserved |
| 7 | RO | 0x0 | reserved |
| 6:0 | RW | 0x00 | SPLOFST<br>Split Offset<br>These bits indicate the value of offset from the beginning of Length/Type field at which header split should take place when the appropriate SPLM is selected. The reset value of this field is 2 bytes indicating a split at L2 header. Value is in terms of bytes. |

**GMAC_MAC_Presn_Time_ns**

Address: Operational Base + offset (0x0240)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x000 | reserved |
| 20:0 | RO | 0x000000 | MPTN<br>MAC 1722 Presentation Time in ns<br>These bits indicate the value of the 32-bit binary rollover equivalent time of the PTP System Time in ns. |

**GMAC_MAC_Presn_Time_Updt**

Address: Operational Base + offset (0x0244)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | MPTU<br>MAC 1722 Presentation Time Update<br>This field holds the init value or the update value for the presentation time. When used for update, this field holds the 32-bit value in ns, that should be added to the Current Presentation Time Counter value. Init happens when TSINIT is set, and update happens when the TSUPDT bit is set (TSINIT and TSINIT defined in MAC_Timestamp_ Control register).<br>When ADDSUB field of MAC_System_Time_Nanoseconds_Update is set, this value is directly used for subtraction. |

**GMAC_MAC_Address0_High**

Address: Operational Base + offset (0x0300)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | AE<br>Address Enable<br>This bit is always set to 1.<br>Values:<br>1'b0: This bit must be always set to 1<br>1'b1: This bit is always set to 1 |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 30 | RW | 0x0 | SA<br>Source Address<br>When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet.<br>Values:<br>0x0 (DA): Compare with Destination Address<br>0x1 (SA): Compare with Source Address |
| 29:24 | RW | 0x00 | MBC<br>Mask Byte Control<br>These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows:<br>Bit 29: MAC_Address0_High[15:8]<br>Bit 28: MAC_Address0_High[7:0]<br>Bit 27: MAC_Address0_Low[31:24]<br>...<br>Bit 24: MAC_Address0_Low[7:0]<br>You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address. |
| 23:17 | RO | 0x00 | reserved |
| 16 | RW | 0x0 | DCS<br>DMA Channel Select<br>If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address0 content is routed.<br>If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address0 content is routed. |
| 15:0 | RW | 0xffff | ADDRHI<br>MAC Address0[47:32]<br>This field contains the upper 16 bits [47:32] of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets. |

**GMAC_MAC_Address0_Low**

Address: Operational Base + offset (0x0304)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0xffffffff | ADDRLO<br>MAC Address0[31:0]<br>This field contains the lower 32 bits of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets. |

**GMAC_MMC_Control**

Address: Operational Base + offset (0x0700)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:9 | RO | 0x000000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | UCDBC<br>Update MMC Counters for Dropped Broadcast Packets<br>Note: The CNTRST bit has a higher priority than the CNTPRST bit. Therefore, when the software tries to set both bits in the same write cycle, all counters are cleared and the CNTPRST bit is not set.<br>When set, the MAC updates all related MMC Counters for Broadcast packets that are dropped because of the setting of the DBF bit of MAC_Packet_Filter register.<br>When reset, the MMC Counters are not updated for dropped Broadcast packets.<br>Values:<br>1'b0: Update MMC Counters for Dropped Broadcast Packets is disabled<br>1'b1: Update MMC Counters for Dropped Broadcast Packets is enabled |
| 7:6 | RO | 0x0 | reserved |
| 5 | RW | 0x0 | CNTPRSTLVL<br>Full-Half Preset<br>When this bit is low and the CNTPRST bit is set, all MMC counters get preset to almost-half value. All octet counters get preset to 0x7FFF_F800 (Half 2KBytes) and all packet-counters gets preset to 0x7FFF_FFF0 (Half 16). When this bit is high and the CNTPRST bit is set, all MMC counters get preset to almost-full value. All octet counters get preset to 0xFFFF_F800 (Full 2KBytes) and all packet-counters gets preset to 0xFFFF_FFF0 (Full 16). For 16-bit counters, the almost-half preset values are 0x7800 and 0x7FF0 for the respective octet and packet counters. Similarly, the almost-full preset values for the 16-bit counters are 0xF800 and 0xFFF0.<br>Values:<br>1'b0: Full-Half Preset is disabled<br>1'b1: Full-Half Preset is enabled |
| 4 | RW | 0x0 | CNTPRST<br>Counters Preset<br>When this bit is set, all counters are initialized or preset to almost full or almost half according to the CNTPRSTLVL bit. This bit is cleared automatically after 1 clock cycle. This bit, along with the CNTPRSTLVL bit, is useful for debugging and testing the assertion of interrupts because of MMC counter becoming half-full or full. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets.<br>Values:<br>1'b0: Counters Preset is disabled<br>1'b1: Counters Preset is enabled |
| 3 | RW | 0x0 | CNTFREEZ<br>MMC Counter Freeze<br>When this bit is set, it freezes all MMC counters to their current value. Until this bit is reset to 0, no MMC counter is updated because of any transmitted or received packet. If any MMC counter is read with the Reset on Read bit set, then that counter is also cleared in this mode.<br>Values:<br>1'b0: MMC Counter Freeze is disabled<br>1'b1: MMC Counter Freeze is enabled |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | RSTONRD<br>Reset on Read<br>When this bit is set, the MMC counters are reset to zero after Read (self-clearing after reset). The counters are cleared when the least significant byte lane (Bits[7:0]) is read.<br>Values:<br>1'b0: Reset on Read is disabled<br>1'b1: Reset on Read is enabled |
| 1 | RW | 0x0 | CNTSTOPRO<br>Counter Stop Rollover<br>When this bit is set, the counter does not roll over to zero after reaching the maximum value.<br>Values:<br>1'b0: Counter Stop Rollover is disabled<br>1'b1: Counter Stop Rollover is enabled |
| 0 | RW | 0x0 | CNTRST<br>Counters Reset<br>When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle.<br>Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets.<br>Values:<br>1'b0: Counters are not reset<br>1'b1: All counters are reset |

**GMAC_MMC_Rx_Interrupt**

Address: Operational Base + offset (0x0704)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23 | RO | 0x0 | RXWDOGPIS<br>MMC Receive Watchdog Error Packet Counter Interrupt Status<br>This bit is set when the rxwatchdog error counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>0x0 (INACTIVE): MMC Receive Watchdog Error Packet Counter Interrupt Status not detected<br>0x1 (ACTIVE): MMC Receive Watchdog Error Packet Counter Interrupt Status detected |
| 22 | RO | 0x0 | reserved |
| 21 | RO | 0x0 | RXFOVPIS<br>MMC Receive FIFO Overflow Packet Counter Interrupt Status<br>This bit is set when the rxfifooverflow counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Receive FIFO Overflow Packet Counter Interrupt Status not detected<br>1'b1: MMC Receive FIFO Overflow Packet Counter Interrupt Status detected |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 20 | RO | 0x0 | RXPAUSPIS<br>MMC Receive Pause Packet Counter Interrupt Status<br>This bit is set when the rxpausepackets counter reaches half of the maximum value or the maximum value.Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>0x0 (INACTIVE): MMC Receive Pause Packet Counter Interrupt Status not detected<br>0x1 (ACTIVE): MMC Receive Pause Packet Counter Interrupt Status detected |
| 19 | RO | 0x0 | reserved |
| 18 | RO | 0x0 | RXLENERPIS<br>MMC Receive Length Error Packet Counter Interrupt Status<br>This bit is set when the rxlengtherror counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Receive Length Error Packet Counter Interrupt Status not detected<br>1'b1: MMC Receive Length Error Packet Counter Interrupt Status detected |
| 17:11 | RO | 0x00 | reserved |
| 10 | RO | 0x0 | RXOSIZEGPIS<br>MMC Receive Oversize Good Packet Counter Interrupt Status<br>This bit is set when the rxoversize_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>0x0 (INACTIVE): MMC Receive Oversize Good Packet Counter Interrupt Status not detected<br>0x1 (ACTIVE): MMC Receive Oversize Good Packet Counter Interrupt Status detected |
| 9:6 | RO | 0x0 | reserved |
| 5 | RO | 0x0 | RXCRCERPIS<br>MMC Receive CRC Error Packet Counter Interrupt Status<br>This bit is set when the rxcrcerror counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Receive CRC Error Packet Counter Interrupt Status not detected<br>1'b1: MMC Receive CRC Error Packet Counter Interrupt Status detected |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RO | 0x0 | RXMCGPIS<br>MMC Receive Multicast Good Packet Counter Interrupt Status<br>This bit is set when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Receive Multicast Good Packet Counter Interrupt Status not detected<br>1'b1: MMC Receive Multicast Good Packet Counter Interrupt Status detected |
| 3 | RO | 0x0 | reserved |
| 2 | RO | 0x0 | RXGOCTIS<br>MMC Receive Good Octet Counter Interrupt Status<br>This bit is set when the rxoctetcount_g counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Receive Good Octet Counter Interrupt Status not detected<br>1'b1: MMC Receive Good Octet Counter Interrupt Status detected |
| 1 | RO | 0x0 | RXGBOCTIS<br>MMC Receive Good Bad Octet Counter Interrupt Status<br>This bit is set when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Receive Good Bad Octet Counter Interrupt Status not detected<br>1'b1: MMC Receive Good Bad Octet Counter Interrupt Status detected |
| 0 | RO | 0x0 | RXGBPKTIS<br>MMC Receive Good Bad Packet Counter Interrupt Status<br>This bit is set when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Receive Good Bad Packet Counter Interrupt Status not detected<br>1'b1: MMC Receive Good Bad Packet Counter Interrupt Status detected |

**GMAC_MMC_Tx_Interrupt**

Address: Operational Base + offset (0x0708)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23 | RO | 0x0 | TXPAUSPIS<br>MMC Transmit Pause Packet Counter Interrupt Status<br>This bit is set when the txpausepacketserror counter reaches half of the maximum value or the maximum value.Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>0x0 (INACTIVE): MMC Transmit Pause Packet Counter Interrupt Status not detected<br>0x1 (ACTIVE): MMC Transmit Pause Packet Counter Interrupt Status detected |
| 22 | RO | 0x0 | reserved |
| 21 | RO | 0x0 | TXGPKTIS<br>MMC Transmit Good Packet Counter Interrupt Status<br>This bit is set when the txpacketcount_g counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Transmit Good Packet Counter Interrupt Status not detected<br>1'b1: MMC Transmit Good Packet Counter Interrupt Status detected |
| 20 | RO | 0x0 | TXGOCTIS<br>MMC Transmit Good Octet Counter Interrupt Status<br>This bit is set when the txoctetcount_g counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Transmit Good Octet Counter Interrupt Status not detected<br>1'b1: MMC Transmit Good Octet Counter Interrupt Status detected |
| 19 | RO | 0x0 | TXCARERPIS<br>MMC Transmit Carrier Error Packet Counter Interrupt Status<br>This bit is set when the txcarriererror counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Transmit Carrier Error Packet Counter Interrupt Status not detected<br>1'b1: MMC Transmit Carrier Error Packet Counter Interrupt Status detected |
| 18:14 | RO | 0x00 | reserved |
| 13 | RO | 0x0 | TXUFLOWERPIS<br>MMC Transmit Underflow Error Packet Counter Interrupt Status<br>This bit is set when the txunderflowerror counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Transmit Underflow Error Packet Counter Interrupt Status not detected<br>1'b1: MMC Transmit Underflow Error Packet Counter Interrupt Status detected |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12:2 | RO | 0x000 | reserved |
| 1 | RO | 0x0 | TXGBPKTIS<br>MMC Transmit Good Bad Packet Counter Interrupt Status<br>This bit is set when the txpacketcount_gb counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Transmit Good Bad Packet Counter Interrupt Status not detected<br>1'b1: MMC Transmit Good Bad Packet Counter Interrupt Status detected |
| 0 | RO | 0x0 | TXGBOCTIS<br>MMC Transmit Good Bad Octet Counter Interrupt Status<br>This bit is set when the txoctetcount_gb counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Transmit Good Bad Octet Counter Interrupt Status not detected<br>1'b1: MMC Transmit Good Bad Octet Counter Interrupt Status detected |

**GMAC_MMC_Rx_Interrupt_Mask**

Address: Operational Base + offset (0x070c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23 | RW | 0x0 | RXWDOGPIM<br>MMC Receive Watchdog Error Packet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxwatchdog counter reaches half of the maximum value or the maximum value.<br>Values:<br>0x0 (DISABLE): MMC Receive Watchdog Error Packet Counter Interrupt Mask is disabled<br>0x1 (ENABLE): MMC Receive Watchdog Error Packet Counter Interrupt Mask is enabled |
| 22 | RO | 0x0 | reserved |
| 21 | RW | 0x0 | RXFOVPIM<br>MMC Receive FIFO Overflow Packet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxfifooverflow counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Receive FIFO Overflow Packet Counter Interrupt Mask is disabled<br>1'b1: MMC Receive FIFO Overflow Packet Counter Interrupt Mask is enabled |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 20 | RW | 0x0 | RXPAUSPIM<br>MMC Receive Pause Packet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxpausepackets counter reaches half of the maximum value or the maximum value.<br>Values:<br>0x0 (DISABLE): MMC Receive Pause Packet Counter Interrupt Mask is disabled<br>0x1 (ENABLE): MMC Receive Pause Packet Counter Interrupt Mask is enabled |
| 19 | RO | 0x0 | reserved |
| 18 | RW | 0x0 | RXLENERPIM<br>MMC Receive Length Error Packet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxlengtherror counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Receive Length Error Packet Counter Interrupt Mask is disabled<br>1'b1: MMC Receive Length Error Packet Counter Interrupt Mask is enabled |
| 17:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | RXOSIZEGPIM<br>MMC Receive Oversize Good Packet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxoversize_g counter reaches half of the maximum value or the maximum value.<br>Values:<br>0x0 (DISABLE): MMC Receive Oversize Good Packet Counter Interrupt Mask is disabled<br>0x1 (ENABLE): MMC Receive Oversize Good Packet Counter Interrupt Mask is enabled |
| 9:6 | RO | 0x0 | reserved |
| 5 | RW | 0x0 | RXCRCERPIM<br>MMC Receive CRC Error Packet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxcrcerror counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Receive CRC Error Packet Counter Interrupt Mask is disabled<br>1'b1: MMC Receive CRC Error Packet Counter Interrupt Mask is enabled |
| 4 | RW | 0x0 | RXMCGPIM<br>MMC Receive Multicast Good Packet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Receive Multicast Good Packet Counter Interrupt Mask is disabled<br>1'b1: MMC Receive Multicast Good Packet Counter Interrupt Mask is enabled |
| 3 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | RXGOCTIM<br>MMC Receive Good Octet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxoctetcount_g counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Receive Good Octet Counter Interrupt Mask is disabled<br>1'b1: MMC Receive Good Octet Counter Interrupt Mask is enabled |
| 1 | RW | 0x0 | RXGBOCTIM<br>MMC Receive Good Bad Octet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Receive Good Bad Octet Counter Interrupt Mask is disabled<br>1'b1: MMC Receive Good Bad Octet Counter Interrupt Mask is enabled |
| 0 | RW | 0x0 | RXGBPKTIM<br>MMC Receive Good Bad Packet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Receive Good Bad Packet Counter Interrupt Mask is disabled<br>1'b1: MMC Receive Good Bad Packet Counter Interrupt Mask is enabled |

**GMAC_MMC_Tx_Interrupt_Mask**

Address: Operational Base + offset (0x0710)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23 | RW | 0x0 | TXPAUSPIM<br>MMC Transmit Pause Packet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the txpausepackets counter reaches half of the maximum value or the maximum value.<br>Values:<br>0x0 (DISABLE): MMC Transmit Pause Packet Counter Interrupt Mask is disabled<br>0x1 (ENABLE): MMC Transmit Pause Packet Counter Interrupt Mask is enabled |
| 22 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 21 | RW | 0x0 | TXGPKTIM<br>MMC Transmit Good Packet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the txpacketcount_g counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Transmit Good Packet Counter Interrupt Mask is disabled<br>1'b1: MMC Transmit Good Packet Counter Interrupt Mask is enabled |
| 20 | RW | 0x0 | TXGOCTIM<br>MMC Transmit Good Octet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the txoctetcount_g counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Transmit Good Octet Counter Interrupt Mask is disabled<br>1'b1: MMC Transmit Good Octet Counter Interrupt Mask is enabled |
| 19 | RW | 0x0 | TXCARERPIM<br>MMC Transmit Carrier Error Packet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the txcarriererror counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Transmit Carrier Error Packet Counter Interrupt Mask is disabled<br>1'b1: MMC Transmit Carrier Error Packet Counter Interrupt Mask is enabled |
| 18:14 | RO | 0x00 | reserved |
| 13 | RW | 0x0 | TXUFLOWERPIM<br>MMC Transmit Underflow Error Packet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the txunderflowerror counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Transmit Underflow Error Packet Counter Interrupt Mask is disabled<br>1'b1: MMC Transmit Underflow Error Packet Counter Interrupt Mask is enabled |
| 12:2 | RO | 0x000 | reserved |
| 1 | RW | 0x0 | TXGBPKTIM<br>MMC Transmit Good Bad Packet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the txpacketcount_gb counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Transmit Good Bad Packet Counter Interrupt Mask is disabled<br>1'b1: MMC Transmit Good Bad Packet Counter Interrupt Mask is enabled |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | TXGBOCTIM<br>MMC Transmit Good Bad Octet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the txoctetcount_gb counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Transmit Good Bad Octet Counter Interrupt Mask is disabled<br>1'b1: MMC Transmit Good Bad Octet Counter Interrupt Mask is enabled |

**GMAC_Tx_Octet_Count_Good_Bad**

Address: Operational Base + offset (0x0714)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | TXOCTGB<br>Tx Octet Count Good Bad<br>This field indicates the number of bytes transmitted, exclusive of preamble and retried bytes, in good and bad packets. |

**GMAC_Tx_Packet_Count_Good_Bad**

Address: Operational Base + offset (0x0718)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | TXPKTGB<br>Tx Packet Count Good Bad<br>This field indicates the number of good and bad packets transmitted, exclusive of retried packets. |

**GMAC_Tx_Underflow_Error_Packets**

Address: Operational Base + offset (0x0748)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | TXUNDRFLW<br>Tx Underflow Error Packets<br>This field indicates the number of packets aborted because of packets underflow error. |

**GMAC_Tx_Carrier_Error_Packets**

Address: Operational Base + offset (0x0760)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | TXCARR<br>Tx Carrier Error Packets<br>This field indicates the number of packets aborted because of carrier sense error (no carrier or loss of carrier). |

**GMAC_Tx_Octet_Count_Good**

Address: Operational Base + offset (0x0764)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | TXOCTG<br>Tx Octet Count Good<br>This field indicates the number of bytes transmitted, exclusive of preamble, only in good packets. |

**GMAC_Tx_Packet_Count_Good**

Address: Operational Base + offset (0x0768)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | TXPKTG<br>Tx Packet Count Good<br>This field indicates the number of good packets transmitted. |

**GMAC_Tx_Pause_Packets**

Address: Operational Base + offset (0x0770)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | TXPAUSE<br>Tx Pause Packets<br>This field indicates the number of good Pause packets transmitted. |

**GMAC_Rx_Packets_Count_Good_Bad**

Address: Operational Base + offset (0x0780)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXPKTGB<br>Rx Packets Count Good Bad<br>This field indicates the number of good and bad packets received. |

**GMAC_Rx_Octet_Count_Good_Bad**

Address: Operational Base + offset (0x0784)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXOCTGB<br>Rx Octet Count Good Bad<br>This field indicates the number of bytes received, exclusive of preamble, in good and bad packets. |

**GMAC_Rx_Octet_Count_Good**

Address: Operational Base + offset (0x0788)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXOCTG<br>Rx Octet Count Good<br>This field indicates the number of bytes received, exclusive of preamble, only in good packets. |

**GMAC_Rx_Multicast_Packets_Good**

Address: Operational Base + offset (0x0790)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXMCASTG<br>Rx Multicast Packets Good<br>This field indicates the number of good multicast packets received. |

**GMAC_Rx_CRC_Error_Packets**

Address: Operational Base + offset (0x0794)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXCRCERR<br>Rx CRC Error Packets<br>This field indicates the number of packets received with CRC error. |

**GMAC_Rx_Oversize_Packets_Good**

Address: Operational Base + offset (0x07a8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXOVERSZG<br>Rx Oversize Packets Good<br>This field indicates the number of packets received without errors, with length greater than the maxsize (1,518 bytes or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in the S2KP bit of the MAC_Configuration register). |

**GMAC_Rx_Length_Error_Packets**

Address: Operational Base + offset (0x07c8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXLENERR<br>Rx Length Error Packets<br>This field indicates the number of packets received with length error (Length Type field not equal to packet size), for all packets with valid length field. |

**GMAC_Rx_Pause_Packets**

Address: Operational Base + offset (0x07d0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXPAUSEPKT<br>Rx Pause Packets<br>This field indicates the number of good and valid Pause packets received. |

**GMAC_Rx_FIFO_Overflow_Packets**

Address: Operational Base + offset (0x07d4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXFIFOOVFL<br>Rx FIFO Overflow Packets<br>This field indicates the number of missed received packets because of FIFO overflow. |

**GMAC_Rx_Watchdog_Error_Packets**

Address: Operational Base + offset (0x07dc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXWDGERR<br>Rx Watchdog Error Packets<br>This field indicates the number of packets received with error because of watchdog timeout error (packets with a data load larger than 2,048 bytes (when JE and WD bits are reset in MAC_Configuration register), 10,240 bytes (when JE bit is set and WD bit is reset in MAC_Configuration register), 16,384 bytes (when WD bit is set in MAC_Configuration register) or the value programmed in the MAC_Watchdog_Timeout register). |

**GMAC_MMC_IPC_Rx_Interrupt_Mask**

Address: Operational Base + offset (0x0800)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 29 | RW | 0x0 | RXICMPEROIM<br>MMC Receive ICMP Error Octet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Receive ICMP Error Octet Counter Interrupt Mask is disabled<br>1'b1: MMC Receive ICMP Error Octet Counter Interrupt Mask is enabled |
| 28 | RO | 0x0 | reserved |
| 27 | RW | 0x0 | RXTCPEROIM<br>MMC Receive TCP Error Octet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Receive TCP Error Octet Counter Interrupt Mask is disabled<br>1'b1: MMC Receive TCP Error Octet Counter Interrupt Mask is enabled |
| 26 | RO | 0x0 | reserved |
| 25 | RW | 0x0 | RXUDPEROIM<br>MMC Receive UDP Error Octet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxudp_err_octets counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Receive UDP Error Octet Counter Interrupt Mask is disabled<br>1'b1: MMC Receive UDP Error Octet Counter Interrupt Mask is enabled |
| 24:23 | RO | 0x0 | reserved |
| 22 | RW | 0x0 | RXIPV6HEROIM<br>MMC Receive IPV6 Header Error Octet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxipv6_nopay_octets counter reaches half of the maximum value or the maximum value.<br>Value:<br>1'b0: MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is disabled<br>1'b1: MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is enabled |
| 21:18 | RO | 0x0 | reserved |
| 17 | RW | 0x0 | RXIPV4HEROIM<br>MMC Receive IPV4 Header Error Octet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is disabled<br>1'b1: MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is enabled |
| 16:14 | RO | 0x0 | reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | RXICMPERPIM<br>MMC Receive ICMP Error Packet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Receive ICMP Error Packet Counter Interrupt Mask is disabled<br>1'b1: MMC Receive ICMP Error Packet Counter Interrupt Mask is enabled |
| 12 | RO | 0x0 | reserved |
| 11 | RW | 0x0 | RXTCPERPIM<br>MMC Receive TCP Error Packet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Receive TCP Error Packet Counter Interrupt Mask is disabled<br>1'b1: MMC Receive TCP Error Packet Counter Interrupt Mask is enabled |
| 10 | RO | 0x0 | reserved |
| 9 | RW | 0x0 | RXUDPERPIM<br>MMC Receive UDP Error Packet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Receive UDP Error Packet Counter Interrupt Mask is disabled<br>1'b1: MMC Receive UDP Error Packet Counter Interrupt Mask is enabled |
| 8:7 | RO | 0x0 | reserved |
| 6 | RW | 0x0 | RXIPV6HERPIM<br>MMC Receive IPV6 Header Error Packet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is disabled<br>1'b1: MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is enabled |
| 5 | RW | 0x0 | RXIPV6GPIM<br>MMC Receive IPV6 Good Packet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Receive IPV6 Good Packet Counter Interrupt Mask is disabled<br>1'b1: MMC Receive IPV6 Good Packet Counter Interrupt Mask is enabled |
| 4:2 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | RXIPV4HERPIM<br>MMC Receive IPV4 Header Error Packet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is disabled<br>1'b1: MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is enabled |
| 0 | RW | 0x0 | RXIPV4GPIM<br>MMC Receive IPV4 Good Packet Counter Interrupt Mask<br>Setting this bit masks the interrupt when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value.<br>Values:<br>1'b0: MMC Receive IPV4 Good Packet Counter Interrupt Mask is disable<br>1'b1: MMC Receive IPV4 Good Packet Counter Interrupt Mask is enabled |

**GMAC_MMC_IPC_Rx_Interrupt**

Address: Operational Base + offset (0x0808)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29 | RO | 0x0 | RXICMPEROIS<br>MMC Receive ICMP Error Octet Counter Interrupt Status<br>This bit is set when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Receive ICMP Error Octet Counter Interrupt Status not detected<br>1'b1: MMC Receive ICMP Error Octet Counter Interrupt Status detected |
| 28 | RO | 0x0 | reserved |
| 27 | RO | 0x0 | RXTCPEROIS<br>MMC Receive TCP Error Octet Counter Interrupt Status<br>This bit is set when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Receive TCP Error Octet Counter Interrupt Status not detected<br>1'b1: MMC Receive TCP Error Octet Counter Interrupt Status detected |
| 26 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 25 | RO | 0x0 | RXUDPEROIS<br>MMC Receive UDP Error Octet Counter Interrupt Status<br>This bit is set when the rxudp_err_octets counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Receive UDP Error Octet Counter Interrupt Status not detected<br>1'b1: MMC Receive UDP Error Octet Counter Interrupt Status detected |
| 24:23 | RO | 0x0 | reserved |
| 22 | RO | 0x0 | RXIPV6HEROIS<br>MMC Receive IPV6 Header Error Octet Counter Interrupt Status<br>This bit is set when the rxipv6_hdrerr_octets counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Receive IPV6 Header Error Octet Counter Interrupt Status not detected<br>1'b1: MMC Receive IPV6 Header Error Octet Counter Interrupt Status detected |
| 21:18 | RO | 0x0 | reserved |
| 17 | RO | 0x0 | RXIPV4HEROIS<br>MMC Receive IPV4 Header Error Octet Counter Interrupt Status<br>This bit is set when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Receive IPV4 Header Error Octet Counter Interrupt Status not detected<br>1'b1: MMC Receive IPV4 Header Error Octet Counter Interrupt Status detected |
| 16:14 | RO | 0x0 | reserved |
| 13 | RO | 0x0 | RXICMPERPIS<br>MMC Receive ICMP Error Packet Counter Interrupt Status<br>This bit is set when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Receive ICMP Error Packet Counter Interrupt Status not detected<br>1'b1: MMC Receive ICMP Error Packet Counter Interrupt Status detected |
| 12 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11 | RO | 0x0 | RXTCPERPIS<br>MMC Receive TCP Error Packet Counter Interrupt Status<br>This bit is set when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Receive TCP Error Packet Counter Interrupt Status not detected<br>1'b1: MMC Receive TCP Error Packet Counter Interrupt Status detected |
| 10 | RO | 0x0 | reserved |
| 9 | RO | 0x0 | RXUDPERPIS<br>MMC Receive UDP Error Packet Counter Interrupt Status<br>This bit is set when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Receive UDP Error Packet Counter Interrupt Status not detected<br>1'b1: MMC Receive UDP Error Packet Counter Interrupt Status detected |
| 8:7 | RO | 0x0 | reserved |
| 6 | RO | 0x0 | RXIPV6HERPIS<br>MMC Receive IPV6 Header Error Packet Counter Interrupt Status<br>This bit is set when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Receive IPV6 Header Error Packet Counter Interrupt Status not detected<br>1'b1: MMC Receive IPV6 Header Error Packet Counter Interrupt Status detected |
| 5 | RO | 0x0 | RXIPV6GPIS<br>MMC Receive IPV6 Good Packet Counter Interrupt Status<br>This bit is set when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Receive IPV6 Good Packet Counter Interrupt Status not detected<br>1'b1: MMC Receive IPV6 Good Packet Counter Interrupt Status detected |
| 4:2 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RO | 0x0 | RXIPV4HERPIS<br>MMC Receive IPV4 Header Error Packet Counter Interrupt Status<br>This bit is set when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Receive IPV4 Header Error Packet Counter Interrupt Status not detected<br>1'b1: MMC Receive IPV4 Header Error Packet Counter Interrupt Status detected |
| 0 | RO | 0x0 | RXIPV4GPIS<br>MMC Receive IPV4 Good Packet Counter Interrupt Status<br>This bit is set when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: MMC Receive IPV4 Good Packet Counter Interrupt Status not detected<br>1'b1: MMC Receive IPV4 Good Packet Counter Interrupt Status detected |

**GMAC_RxIPv4_Good_Packets**

Address: Operational Base + offset (0x0810)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXIPV4GDPKT<br>RxIPv4 Good Packets<br>This field indicates the number of good IPv4 datagrams received with the TCP, UDP, or ICMP payload. |

**GMAC_RxIPv4_Header_Error_Packets**

Address: Operational Base + offset (0x0814)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXIPV4HDRERRPKT<br>RxIPv4 Header Error Packets<br>This field indicates the number of IPv4 datagrams received with header (checksum, length, or version mismatch) errors. |

**GMAC_RxIPv6_Good_Packets**

Address: Operational Base + offset (0x0824)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXIPV6GDPKT<br>RxIPv6 Good Packets<br>This field indicates the number of good IPv6 datagrams received with the TCP, UDP, or ICMP payload. |

**GMAC_RxIPv6_Header_Error_Packets**

Address: Operational Base + offset (0x0828)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXIPV6HDRERRPKT<br>RxIPv6 Header Error Packets<br>This field indicates the number of IPv6 datagrams received with header (length or version mismatch) errors. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**GMAC_RxUDP_Error_Packets**

Address: Operational Base + offset (0x0834)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXUDPERRPKT<br>RxUDP Error Packets<br>This field indicates the number of good IP datagrams received whose UDP payload has a checksum error. |

**GMAC_RxTCP_Error_Packets**

Address: Operational Base + offset (0x083c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXTCPERRPKT<br>RxTCP Error Packets<br>This field indicates the number of good IP datagrams received whose TCP payload has a checksum error. |

**GMAC_RxICMP_Error_Packets**

Address: Operational Base + offset (0x0844)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXICMPERRPKT<br>RxICMP Error Packets<br>This field indicates the number of good IP datagrams received whose ICMP payload has a checksum error. |

**GMAC_RxIPv4_Header_Error_Octets**

Address: Operational Base + offset (0x0854)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXIPV4HDRERROCT<br>RxIPv4 Header Error Octets<br>This field indicates the number of bytes received in IPv4 datagrams with header errors (checksum, length, version mismatch). The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter. |

**GMAC_RxIPv6_Header_Error_Octets**

Address: Operational Base + offset (0x0868)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXIPV6HDRERROCT<br>RxIPv6 Header Error Octets<br>This field indicates the number of bytes received in IPv6 datagrams with header errors (length, version mismatch). The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter. |

**GMAC_RxUDP_Error_Octets**

Address: Operational Base + offset (0x0874)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXUDPERROCT<br>RxUDP Error Octets<br>This field indicates the number of bytes received in a UDP segment that had checksum errors. This counter does not count IP header bytes. |

**GMAC_RxTCP_Error_Octets**

Address: Operational Base + offset (0x087c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXTCPERROCT<br>RxTCP Error Octets<br>This field indicates the number of bytes received in a TCP segment that had checksum errors. This counter does not count IP header bytes. |

**GMAC_RxICMP_Error_Octets**

Address: Operational Base + offset (0x0884)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | RXICMPERROCT<br>RxICMP Error Octets<br>This field indicates the number of bytes received in a ICMP segment that had checksum errors. This counter does not count IP header bytes. |

**GMAC_MMC_FPE_Tx_Interrupt**

Address: Operational Base + offset (0x08a0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RO | 0x0 | HRCIS<br>MMC Tx Hold Request Counter Interrupt Status<br>This bit is set when the Tx_Hold_Req_Cntr counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration.<br>Values:<br>0x0 (INACTIVE): MMC Tx Hold Request Counter Interrupt Status not detected<br>0x1 (ACTIVE): MMC Tx Hold Request Counter Interrupt Status detected |
| 0 | RO | 0x0 | FCIS<br>MMC Tx FPE Fragment Counter Interrupt status<br>This bit is set when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.<br>Values:<br>0x0 (INACTIVE): MMC Tx FPE Fragment Counter Interrupt status not detected<br>0x1 (ACTIVE): MMC Tx FPE Fragment Counter Interrupt status detected |

**GMAC_MMC_FPE_Tx_Interrupt_Mask**

Address: Operational Base + offset (0x08a4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | HRCIM<br>MMC Transmit Hold Request Counter Interrupt Mask<br>Setting this bit masks the interrupt when the Tx_Hold_Req_Cntr counter reaches half of the maximum value or the maximum value.<br>Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration.<br>Values:<br>0x0 (DISABLE): MMC Transmit Hold Request Counter Interrupt Mask is disabled<br>0x1 (ENABLE): MMC Transmit Hold Request Counter Interrupt Mask is enabled |
| 0 | RW | 0x0 | FCIM<br>MMC Transmit Fragment Counter Interrupt Mask<br>Setting this bit masks the interrupt when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value.<br>Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.<br>Values:<br>0x0 (DISABLE): MMC Transmit Fragment Counter Interrupt Mask is disabled<br>0x1 (ENABLE): MMC Transmit Fragment Counter Interrupt Mask is enabled |

**GMAC_MMC_Tx_FPE_Fragment_Cntr**

Address: Operational Base + offset (0x08a8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | TXFFC<br>Tx FPE Fragment counter<br>This field indicates the number of additional mPackets that has been transmitted due to preemption exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. |

**GMAC_MMC_Tx_Hold_Req_Cntr**

Address: Operational Base + offset (0x08ac)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | TXHRC<br>Tx Hold Request Counter<br>This field indicates count of number of a hold request is given to MAC.<br>Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration. |

**GMAC_MMC_FPE_Rx_Interrupt**

Address: Operational Base + offset (0x08c0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RO | 0x0 | FCIS<br>MMC Rx FPE Fragment Counter Interrupt Status<br>This bit is set when the Rx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.<br>Values:<br>0x0 (INACTIVE): MMC Rx FPE Fragment Counter Interrupt Status not detected<br>0x1 (ACTIVE): MMC Rx FPE Fragment Counter Interrupt Status detected |
| 2 | RO | 0x0 | PAOCIS<br>MMC Rx Packet Assembly OK Counter Interrupt Status<br>This bit is set when the Rx_Packet_Assemble_Ok_Cntr counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.<br>Values:<br>0x0 (INACTIVE): MMC Rx Packet Assembly OK Counter Interrupt Status not detected<br>0x1 (ACTIVE): MMC Rx Packet Assembly OK Counter Interrupt Status detected |
| 1 | RO | 0x0 | PSECIS<br>MMC Rx Packet SMD Error Counter Interrupt Status<br>This bit is set when the Rx_Packet_SMD_Err_Cntr counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.<br>Values:<br>0x0 (INACTIVE): MMC Rx Packet SMD Error Counter Interrupt Status not detected<br>0x1 (ACTIVE): MMC Rx Packet SMD Error Counter Interrupt Status detected |
| 0 | RO | 0x0 | PAECIS<br>MMC Rx Packet Assembly Error Counter Interrupt Status<br>This bit is set when the Rx_Packet_Assemble_Err_Cntr counter reaches half of the maximum value or the maximum value.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.<br>Values:<br>0x0 (INACTIVE): MMC Rx Packet Assembly Error Counter Interrupt Status not detected<br>0x1 (ACTIVE): MMC Rx Packet Assembly Error Counter Interrupt Status detected |

**GMAC_MMC_FPE_Rx_Interrupt_Mask**

Address: Operational Base + offset (0x08c4)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3 | RW | 0x0 | FCIM<br>MMC Rx FPE Fragment Counter Interrupt Mask<br>Setting this bit masks the interrupt when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value.<br>Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.<br>Values:<br>0x0 (DISABLE): MMC Rx FPE Fragment Counter Interrupt Mask is disabled<br>0x1 (ENABLE): MMC Rx FPE Fragment Counter Interrupt Mask is enabled |
| 2 | RW | 0x0 | PAOCIM<br>MMC Rx Packet Assembly OK Counter Interrupt Mask<br>Setting this bit masks the interrupt when the Rx_Packet_Assemble_Ok_Cntr counter reaches half of the maximum value or the maximum value.<br>Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.<br>Values:<br>0x0 (DISABLE): MMC Rx Packet Assembly OK Counter Interrupt Mask is disabled<br>0x1 (ENABLE): MMC Rx Packet Assembly OK Counter Interrupt Mask is enabled |
| 1 | RW | 0x0 | PSECIM<br>MMC Rx Packet SMD Error Counter Interrupt Mask<br>Setting this bit masks the interrupt when the Rx_Packet_SMD_Err_Cntr counter reaches half of the maximum value or the maximum value.<br>Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.<br>Values:<br>0x0 (DISABLE): MMC Rx Packet SMD Error Counter Interrupt Mask is disabled<br>0x1 (ENABLE): MMC Rx Packet SMD Error Counter Interrupt Mask is enabled |
| 0 | RW | 0x0 | PAECIM<br>MMC Rx Packet Assembly Error Counter Interrupt Mask<br>Setting this bit masks the interrupt when the Rx_Packet_Assemble_Err_Cntr counter reaches half of the maximum value or the maximum value.<br>Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.<br>Values:<br>0x0 (DISABLE): MMC Rx Packet Assembly Error Counter Interrupt Mask is disabled<br>0x1 (ENABLE): MMC Rx Packet Assembly Error Counter Interrupt Mask is enabled |

**GMAC_MMC_Rx_Packet_Asm_Err_Cntr**

Address: Operational Base + offset (0x08c8)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | PAEC<br>Rx Packet Assembly Error Counter<br>This field indicates the number of MAC frames with reassembly errors on the Receiver, due to mismatch in the Fragment Count value.<br>Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. |

**GMAC_MMC_Rx_Packet_SMD_Err_Cntr**

Address: Operational Base + offset (0x08cc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | PSEC<br>Rx Packet SMD Error Counter<br>This field indicates the number of MAC frames rejected due to unknown SMD value and MAC frame fragments rejected due to arriving with an SMD-C when there was no preceding preempted frame.<br>Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration. |

**GMAC_MMC_Rx_Packet_Assembly_OK_Cntr**

Address: Operational Base + offset (0x08d0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | PAOC<br>Rx Packet Assembly OK Counter<br>This field indicates the number of MAC frames that were successfully reassembled and delivered to MAC.<br>Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration. |

**GMAC_MMC_Rx_FPE_Fragment_Cntr**

Address: Operational Base + offset (0x08d4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | FFC<br>Rx FPE Fragment Counter<br>This field indicates the number of additional mPackets received due to preemption exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration. |

**GMAC_MAC_L3_L4_Control0**

Address: Operational Base + offset (0x0900)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28 | RW | 0x0 | DMCHEN0<br>DMA Channel Select Enable<br>When set, this bit enables the selection of the DMA channel number for the packet that is passed by this L3_L4 filter. The DMA channel is indicated by the DMCHN bits. When this bit is reset, the DMA channel is not decided by this filter.<br>Values:<br>0x0 (DISABLE): DMA Channel Select is disabled<br>0x1 (ENABLE): DMA Channel Select is enabled |
| 27:25 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 24 | RW | 0x0 | DMCHN0<br>DMA Channel Number<br>When DMCHEN is set high, this field selects the DMA Channel number to which the packet passed by this filter is routed. The width of this field depends on the number of the DMA channels present in your configuration. |
| 23:22 | RO | 0x0 | reserved |
| 21 | RW | 0x0 | L4DPIM0<br>Layer 4 Destination Port Inverse Match Enable<br>When this bit is set, the Layer 4 Destination Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Destination Port number field is enabled for perfect matching.<br>This bit is valid and applicable only when the L4DPM0 bit is set high.<br>Values:<br>0x0 (DISABLE): Layer 4 Destination Port Inverse Match is disabled<br>0x1 (ENABLE): Layer 4 Destination Port Inverse Match is enabled |
| 20 | RW | 0x0 | L4DPM0<br>Layer 4 Destination Port Match Enable<br>When this bit is set, the Layer 4 Destination Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Destination Port number field for matching.<br>Values:<br>0x0 (DISABLE): Layer 4 Destination Port Match is disabled<br>0x1 (ENABLE): Layer 4 Destination Port Match is enabled |
| 19 | RW | 0x0 | L4SPIM0<br>Layer 4 Source Port Inverse Match Enable<br>When this bit is set, the Layer 4 Source Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Source Port number field is enabled for perfect matching.<br>This bit is valid and applicable only when the L4SPM0 bit is set high.<br>Values:<br>0x0 (DISABLE): Layer 4 Source Port Inverse Match is disabled<br>0x1 (ENABLE): Layer 4 Source Port Inverse Match is enabled |
| 18 | RW | 0x0 | L4SPM0<br>Layer 4 Source Port Match Enable<br>When this bit is set, the Layer 4 Source Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Source Port number field for matching.<br>Values:<br>0x0 (DISABLE): Layer 4 Source Port Match is disabled<br>0x1 (ENABLE): Layer 4 Source Port Match is enabled |
| 17 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 16 | RW | 0x0 | L4PEN0<br>Layer 4 Protocol Enable<br>When this bit is set, the Source and Destination Port number fields of UDP packets are used for matching. When this bit is reset, the Source and Destination Port number fields of TCP packets are used for matching.<br>The Layer 4 matching is done only when the L4SPM0 or L4DPM0 bit is set.<br>Values:<br>0x0 (DISABLE): Layer 4 Protocol is disabled<br>0x1 (ENABLE): Layer 4 Protocol is enabled |
| 15:11 | RW | 0x00 | L3HDBM0<br>Layer 3 IP DA Higher Bits Match<br>IPv4 Packets:<br>This field contains the number of higher bits of IP Destination Address that are matched in the IPv4 packets. The following list describes the values of this field:<br>0: No bits are masked.<br>1: LSb[0] is masked<br>2: Two LSbs [1:0] are masked<br>..<br>31: All bits except MSb are masked.<br>IPv6 Packets:<br>Bits[12:11] of this field correspond to Bits[6:5] of L3HSBM0 which indicate the number of lower bits of IP Source or Destination Address that are masked in the IPv6 packets. The following list describes the concatenated values of the L3HDBM0[1:0] and L3HSBM0 bits:<br>0: No bits are masked.<br>1: LSb[0] is masked.<br>2: Two LSbs [1:0] are masked<br>..<br>127: All bits except MSb are masked.<br>This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set. |
| 10:6 | RW | 0x00 | L3HSBM0<br>Layer 3 IP SA Higher Bits Match<br>IPv4 Packets:<br>This field contains the number of lower bits of IP Source Address that are masked for matching in the IPv4 packets. The following list describes the values of this field:<br>0: No bits are masked.<br>1: LSb[0] is masked<br>2: Two LSbs [1:0] are masked<br>..<br>31: All bits except MSb are masked.<br>IPv6 Packets:<br>This field contains Bits[4:0] of L3HSBM0. These bits indicate the number of higher bits of IP Source or Destination Address matched in the IPv6 packets. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set high. |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | L3DAIM0<br>Layer 3 IP DA Inverse Match Enable<br>When this bit is set, the Layer 3 IP Destination Address field is enabled for inverse matching. When this bit is reset, the Layer 3 IP Destination Address field is enabled for perfect matching.<br>This bit is valid and applicable only when the L3DAM0 bit is set high.<br>Values:<br>0x0 (DISABLE): Layer 3 IP DA Inverse Match is disabled<br>0x1 (ENABLE): Layer 3 IP DA Inverse Match is enabled |
| 4 | RW | 0x0 | L3DAM0<br>Layer 3 IP DA Match Enable<br>When this bit is set, the Layer 3 IP Destination Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Destination Address field for matching.<br>Note: When the L3PEN0 bit is set, you should set either this bit or the L3SAM0 bit because either IPv6 DA or SA can be checked for filtering.<br>Values:<br>0x0 (DISABLE): Layer 3 IP DA Match is disabled<br>0x1 (ENABLE): Layer 3 IP DA Match is enabled |
| 3 | RW | 0x0 | L3SAIM0<br>Layer 3 IP SA Inverse Match Enable<br>When this bit is set, the Layer 3 IP Source Address field is enabled for inverse matching. When this bit reset, the Layer 3 IP Source Address field is enabled for perfect matching.<br>This bit is valid and applicable only when the L3SAM0 bit is set.<br>Values:<br>0x0 (DISABLE): Layer 3 IP SA Inverse Match is disabled<br>0x1 (ENABLE): Layer 3 IP SA Inverse Match is enabled |
| 2 | RW | 0x0 | L3SAM0<br>Layer 3 IP SA Match Enable<br>When this bit is set, the Layer 3 IP Source Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Source Address field for matching.<br>Note: When the L3PEN0 bit is set, you should set either this bit or the L3DAM0 bit because either IPv6 SA or DA can be checked for filtering.<br>Values:<br>0x0 (DISABLE): Layer 3 IP SA Match is disabled<br>0x1 (ENABLE): Layer 3 IP SA Match is enabled |
| 1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | L3PEN0<br>Layer 3 Protocol Enable<br>When this bit is set, the Layer 3 IP Source or Destination Address matching is enabled for IPv6 packets. When this bit is reset, the Layer 3 IP Source or Destination Address matching is enabled for IPv4 packets.<br>The Layer 3 matching is done only when the L3SAM0 or L3DAM0 bit is set.<br>Values:<br>0x0 (DISABLE): Layer 3 Protocol is disabled<br>0x1 (ENABLE): Layer 3 Protocol is enabled |

**GMAC_MAC_Layer4_Address0**

Address: Operational Base + offset (0x0904)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | L4DP0<br>Layer 4 Destination Port Number Field<br>When the L4PEN0 bit is reset and the L4DPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Destination Port Number field in the IPv4 or IPv6 packets.<br>When the L4PEN0 and L4DPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Destination Port Number field in the IPv4 or IPv6 packets. |
| 15:0 | RW | 0x0000 | L4SP0<br>Layer 4 Source Port Number Field<br>When the L4PEN0 bit is reset and the L4SPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Source Port Number field in the IPv4 or IPv6 packets.<br>When the L4PEN0 and L4SPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Source Port Number field in the IPv4 or IPv6 packets. |

**GMAC_MAC_Layer3_Addr0_Reg0**

Address: Operational Base + offset (0x0910)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | L3A00<br>Layer 3 Address 0 Field<br>When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Source Address field in the IPv6 packets.<br>When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Destination Address field in the IPv6 packets.<br>When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Source Address field in the IPv4 packets. |

**GMAC_MAC_Layer3_Addr1_Reg0**

Address: Operational Base + offset (0x0914)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | L3A10<br>Layer 3 Address 1 Field<br>When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Source Address field in the IPv6 packets.<br>When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Destination Address field in the IPv6 packets.<br>When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Destination Address field in the IPv4 packets. |

**GMAC_MAC_Layer3_Addr2_Reg0**

Address: Operational Base + offset (0x0918)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | L3A20<br>Layer 3 Address 2 Field<br>When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Source Address field in the IPv6 packets.<br>When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Destination Address field in the IPv6 packets.<br>When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used. |

**GMAC_MAC_Layer3_Addr3_Reg0**

Address: Operational Base + offset (0x091c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | L3A30<br>Layer 3 Address 3 Field<br>When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Source Address field in the IPv6 packets.<br>When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Destination Address field in the IPv6 packets.<br>When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used. |

**GMAC_MAC_Timestamp_Control**

Address: Operational Base + offset (0x0b00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 28 | RW | 0x0 | AV8021ASMEN<br>AV 802.1AS Mode Enable<br>When this bit is set, the MAC processes only untagged PTP over Ethernet packets for providing PTP status and capturing timestamp snapshots, that is, IEEE 802.1AS mode of operation. When PTP offload feature is enabled, for the purpose of PTP offload, the transport specific field in the PTP header is generated and checked based on the value of this bit.<br>Values:<br>1'b0: AV 802.1AS Mode is disabled<br>1'b1: AV 802.1AS Mode is enabled |
| 27:25 | RO | 0x0 | reserved |
| 24 | RW | 0x0 | TXTSSTSM<br>Transmit Timestamp Status Mode<br>When this bit is set, the MAC overwrites the earlier transmit timestamp status even if it is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register. When this bit is reset, the MAC ignores the timestamp status of current packet if the timestamp status of previous packet is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register.<br>Values:<br>1'b0: Transmit Timestamp Status Mode is disabled<br>1'b1: Transmit Timestamp Status Mode is enabled |
| 23:19 | RO | 0x00 | reserved |
| 18 | RW | 0x0 | TSENMACADDR<br>Enable MAC Address for PTP Packet Filtering<br>When this bit is set, the DA MAC address (that matches any MAC Address register) is used to filter the PTP packets when PTP is directly sent over Ethernet.<br>When this bit is set, received PTP packets with DA containing a special multicast or unicast address that matches the one programmed in MAC address registers are considered for processing as indicated below, when PTP is directly sent over Ethernet.<br>For normal time stamping operation, MAC address registers 0 to 31 is considered for unicast destination address matching.<br>For PTP offload, only MAC address register 0 is considered for unicast destination address matching.<br>Values:<br>1'b0: MAC Address for PTP Packet Filtering is disabled<br>1'b1: MAC Address for PTP Packet Filtering is enabled |
| 17:16 | RW | 0x0 | SNAPTYPSEL<br>Select PTP packets for Taking Snapshots<br>These bits, along with Bits 15 and 14, decide the set of PTP packet types for which snapshot needs to be taken. The encoding is given in Timestamp Snapshot Dependency on Register Bits Table. |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x0 | TSMSTRENA<br>Enable Snapshot for Messages Relevant to Master<br>When this bit is set, the snapshot is taken only for the messages that are relevant to the master node. Otherwise, the snapshot is taken for the messages relevant to the slave node.<br>Values:<br>1'b0: Snapshot for Messages Relevant to Master is disabled<br>1'b1: Snapshot for Messages Relevant to Master is enabled |
| 14 | RW | 0x0 | TSEVNTENA<br>Enable Timestamp Snapshot for Event Messages<br>When this bit is set, the timestamp snapshot is taken only for event messages (SYNC, Delay_Req, Pdelay_Req, or Pdelay_Resp). When this bit is reset, the snapshot is taken for all messages except Announce, Management, and Signaling. For more information about the timestamp snapshots, see Timestamp Snapshot Dependency on Register Bits Table.<br>Values:<br>1'b0: Timestamp Snapshot for Event Messages is disabled<br>1'b1: Timestamp Snapshot for Event Messages is enabled |
| 13 | RW | 0x0 | TSIPV4ENA<br>Enable Processing of PTP Packets Sent over IPv4-UDP<br>When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv4-UDP packets. When this bit is reset, the MAC ignores the PTP transported over IPv4-UDP packets. This bit is set by default.<br>Values:<br>1'b0: Processing of PTP Packets Sent over IPv4-UDP is disabled<br>1'b1: Processing of PTP Packets Sent over IPv4-UDP is enabled |
| 12 | RW | 0x0 | TSIPV6ENA<br>Enable Processing of PTP Packets Sent over IPv6-UDP<br>When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv6-UDP packets. When this bit is clear, the MAC ignores the PTP transported over IPv6-UDP packets.<br>Values:<br>1'b0: Processing of PTP Packets Sent over IPv6-UDP is disabled<br>1'b1: Processing of PTP Packets Sent over IPv6-UDP is enabled |
| 11 | RW | 0x0 | TSIPENA<br>Enable Processing of PTP over Ethernet Packets<br>When this bit is set, the MAC receiver processes the PTP packets encapsulated directly in the Ethernet packets. When this bit is reset, the MAC ignores the PTP over Ethernet packets.<br>Values:<br>1'b0: Processing of PTP over Ethernet Packets is disabled<br>1'b1: Processing of PTP over Ethernet Packets is enabled |
| 10 | RW | 0x0 | TSVER2ENA<br>Enable PTP Packet Processing for Version 2 Format<br>When this bit is set, the IEEE 1588 version 2 format is used to process the PTP packets. When this bit is reset, the IEEE 1588 version 1 format is used to process the PTP packets. The IEEE 1588 formats are described in 'PTP Processing and Control'.<br>Values:<br>1'b0: PTP Packet Processing for Version 2 Format is disabled<br>1'b1: PTP Packet Processing for Version 2 Format is enabled |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RW | 0x0 | TSCTRLSSR<br>Timestamp Digital or Binary Rollover Control<br>When this bit is set, the Timestamp Low register rolls over after 0x3B9A_C9FF value (that is, 1 nanosecond accuracy) and increments the timestamp (High) seconds. When this bit is reset, the rollover value of sub-second register is 0x7FFF_FFFF. The sub-second increment must be programmed correctly depending on the PTP reference clock frequency and the value of this bit.<br>Values:<br>1'b0: Timestamp Digital or Binary Rollover Control is disabled<br>1'b1: Timestamp Digital or Binary Rollover Control is enabled |
| 8 | RW | 0x0 | TSENALL<br>Enable Timestamp for All Packets<br>When this bit is set, the timestamp snapshot is enabled for all packets received by the MAC.<br>Values:<br>1'b0: Timestamp for All Packets disabled<br>1'b1: Timestamp for All Packets enabled |
| 7 | RO | 0x0 | reserved |
| 6 | RW | 0x0 | PTGE<br>Presentation Time Generation Enable<br>When this bit is set the Presentation Time generation will be enabled.<br>Values:<br>0x0 (DISABLE): Presentation Time Generation is disabled<br>0x1 (ENABLE): Presentation Time Generation is enabled |
| 5 | RW | 0x0 | TSADDREG<br>Update Addend Register<br>When this bit is set, the content of the Timestamp Addend register is updated in the PTP block for fine correction. This bit is cleared when the update is complete. This bit should be zero before it is set.<br>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.<br>Values:<br>1'b0: Addend Register is not updated<br>1'b1: Addend Register is updated |
| 4 | RO | 0x0 | reserved |
| 3 | RW | 0x0 | TSUPDT<br>Update Timestamp<br>When this bit is set, the system time is updated (added or subtracted) with the value specified in MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before updating it. This bit is reset when the update is complete in hardware. The Timestamp Higher Word register (if enabled during core configuration) is not updated.When Media Clock Generation and Recovery is configured (GMAC_FLEXI_PPS_OUT_EN) and enabled MAC_Presn_Time_Updt should also be updated before setting this field.<br>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.<br>Values:<br>1'b0: Timestamp is not updated<br>1'b1: Timestamp is updated |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | TSINIT<br>Initalize Timestamp<br>When this bit is set, the system time is initialized (overwritten) with the value specified in the MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before it is updated. This bit is reset when the initialization is complete. The Timestamp Higher Word register (if enabled during core configuration) can only be initialized.When Media Clock Generation and Recovery is configured (GMAC_FLEXI_PPS_OUT_EN) and enabled MAC_Presn_Time_Updt should also be updated before setting this field.<br>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.<br>Values:<br>1'b0: Timestamp is not initialized<br>1'b1: Timestamp is initialized |
| 1 | RW | 0x0 | TSCFUPDT<br>Fine or Coarse Timestamp Update<br>When this bit is set, the Fine method is used to update system timestamp. When this bit is reset, Coarse method is used to update the system timestamp.<br>Values:<br>1'b0: Coarse method is used to update system timestamp<br>1'b1: Fine method is used to update system timestamp |
| 0 | RW | 0x0 | TSENA<br>Enable Timestamp<br>When this bit is set, the timestamp is added for Transmit and Receive packets. When disabled, timestamp is not added for transmit and receive packets and the Timestamp Generator is also suspended. You need to initialize the Timestamp (system time) after enabling this mode.On the Receive side, the MAC processes the 1588 packets only if this bit is set.<br>Values:<br>1'b0: Timestamp is disabled<br>1'b1: Timestamp is enabled |

**GMAC_MAC_Sub_Second_Increment**

Address: Operational Base + offset (0x0b04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23:16 | RW | 0x00 | SSINC<br>Sub-second Increment Value<br>The value programmed in this field is accumulated every clock cycle (of clk_ptp_i) with the contents of the sub-second register. For example, when the PTP clock is 50 MHz (period is 20 ns), you should program 20 (0x14) when the System Time Nanoseconds register has an accuracy of 1 ns [Bit 9 (TSCTRLSSR) is set in MAC_Timestamp_Control]. When TSCTRLSSR is clear, the Nanoseconds register has a resolution of ~0.465 ns. In this case, you should program a value of 43 (0x2B) which is derived by 20 ns/0.465. |

**GMAC_MAC_System_Time_Secs**

Address: Operational Base + offset (0x0b08)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | TSS<br>Timestamp Second<br>The value in this field indicates the current value in seconds of the System Time maintained by the MAC. |

**GMAC_MAC_System_Time_NS**

Address: Operational Base + offset (0x0b0c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |
| 30:0 | RW | 0x00000000 | TSSS<br>Timestamp Sub Seconds<br>The value in this field has the sub-second representation of time, with an accuracy of 0.46 ns. When Bit 9 is set in MAC_Timestamp_Control, each bit represents 1 ns. The maximum value is 0x3B9A_C9FF after which it rolls-over to zero. |

**GMAC_MAC_Sys_Time_Secs_Update**

Address: Operational Base + offset (0x0b10)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | TSS<br>Timestamp Seconds<br>The value in this field is the seconds part of the update. When ADDSUB is reset, this field must be programmed with the seconds part of the update value.<br>When ADDSUB is set, this field must be programmed with the complement of the seconds part of the update value. For example, if 2.000000001 seconds need to be subtracted from the system time, the TSS field in the MAC_Timestamp_Seconds_Update register must be 0xFFFF_FFFE (that is, 2^32 - 2). |

**GMAC_MAC_Sys_Time_NS_Update**

Address: Operational Base + offset (0x0b14)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | ADDSUB<br>Add or Subtract Time<br>When this bit is set, the time value is subtracted with the contents of the update register. When this bit is reset, the time value is added with the contents of the update register.<br>Values:<br>1'b0: Add time<br>1'b1: Subtract time |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 30:0 | RW | 0x00000000 | TSSS<br>Timestamp Sub Seconds<br>The value in this field is the sub-seconds part of the update. When ADDSUB is reset, this field must be programmed with the sub-seconds part of the update value, with an accuracy based on the TSCTRLSSR bit of the MAC_Timestamp_Control register.When ADDSUB is set, this field must be programmed with the complement of the sub-seconds part of the update value as described below.<br>When TSCTRLSSR bit in MAC_Timestamp_Control is set, the programmed value must be 10^9 - <sub-second value>. When TSCTRLSSR bit in MAC_Timestamp_Control is reset, the programmed value must be 2^31 - <sub-second_value>. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, each bit represents an accuracy of 0.46 ns. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, each bit represents 1 ns and the programmed value should not exceed 0x3B9A_C9FF.<br>For example, if 2.000000001 seconds need to be subtracted from the system time, then the TSSS field in the MAC_Timestamp_Nanoseconds_Update register must be 0x7FFF_FFFF (that is, 2^31 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is reset and 0x3B9A_C9FF (that is, 10^9 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is set. |

**GMAC_MAC_Timestamp_Addend**

Address: Operational Base + offset (0x0b18)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | TSAR<br>Timestamp Addend Register<br>This field indicates the 32-bit time value to be added to the Accumulator register to achieve time synchronization. |

**GMAC_MAC_Timestamp_Status**

Address: Operational Base + offset (0x0b20)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:25 | RO | 0x00 | ATSNS<br>Number of Auxiliary Timestamp Snapshots<br>This field indicates the number of Snapshots available in the FIFO. A value equal to the selected depth of FIFO (4, 8, or 16) indicates that the Auxiliary Snapshot FIFO is full. These bits are cleared (to 00000) when the Auxiliary snapshot FIFO clear bit is set. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 24 | RO | 0x0 | ATSSTM<br>Auxiliary Timestamp Snapshot Trigger Missed<br>This bit is set when the Auxiliary timestamp snapshot FIFO is full and external trigger was set. This indicates that the latest snapshot is not stored in the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected.<br>Values:<br>1'b0: Auxiliary Timestamp Snapshot Trigger Missed status not detected<br>1'b1: Auxiliary Timestamp Snapshot Trigger Missed status detected |
| 23:16 | RO | 0x00 | reserved |
| 15 | RO | 0x0 | TXTSSIS<br>Tx Timestamp Status Interrupt Status<br>In non-EQOS_CORE configurations when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers. When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets. This bit is cleared when the MAC_Tx_Timestamp_Status_Seconds register is read (or write to MAC_Tx_Timestamp_Status_Seconds register when RCWE bit of MAC_CSR_SW_Ctrl register is set).<br>Values:<br>1'b0: Tx Timestamp Status Interrupt status not detected<br>1'b1: Tx Timestamp Status Interrupt status detected |
| 14:4 | RO | 0x000 | reserved |
| 3 | RO | 0x0 | TSTRGTERR0<br>Timestamp Target Time Error<br>This bit is set when the latest target time programmed in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers elapses. This bit is cleared when the application reads this bit.<br>Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.<br>Values:<br>1'b0: Timestamp Target Time Error status not detected<br>1'b1: Timestamp Target Time Error status detected |
| 2 | RO | 0x0 | AUXTSTRIG<br>Auxiliary Timestamp Trigger Snapshot<br>This bit is set high when the auxiliary snapshot is written to the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected.<br>Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.<br>Values:<br>1'b0: Auxiliary Timestamp Trigger Snapshot status not detected<br>1'b1: Auxiliary Timestamp Trigger Snapshot status detected |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RO | 0x0 | TSTARGT0<br>Timestamp Target Time Reached<br>When set, this bit indicates that the value of system time is greater than or equal to the value specified in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers.<br>Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.<br>Values:<br>1'b0: Timestamp Target Time Reached status not detected<br>1'b1: Timestamp Target Time Reached status detected |
| 0 | RO | 0x0 | TSSOVF<br>Timestamp Seconds Overflow<br>When this bit is set, it indicates that the seconds value of the timestamp (when supporting version 2 format) has overflowed beyond 32'hFFFF_FFFF.<br>Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.<br>Values:<br>1'b0: Timestamp Seconds Overflow status not detected<br>1'b1: Timestamp Seconds Overflow status detected |

**GMAC_MAC_Tx_TS_Status_NS**

Address: Operational Base + offset (0x0b30)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | TXTSSMIS<br>Transmit Timestamp Status Missed<br>When this bit is set, it indicates one of the following:<br>1. The timestamp of the current packet is ignored if TXTSSTSM bit of the MAC_Timestamp_Control register is reset.<br>2. The timestamp of the previous packet is overwritten with timestamp of the current packet if TXTSSTSM bit of the MAC_Timestamp_Control register is set.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: Transmit Timestamp Status Missed status not detected<br>1'b1: Transmit Timestamp Status Missed status detected |
| 30:0 | RO | 0x00000000 | TXTSSLO<br>Transmit Timestamp Status Low<br>This field contains the 31 bits of the Nanoseconds field of the Transmit packet's captured timestamp. |

**GMAC_MAC_Tx_TS_Status_Secs**

Address: Operational Base + offset (0x0b34)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | TXTSSHI<br>Transmit Timestamp Status High<br>This field contains the lower 32 bits of the Seconds field of Transmit packet's captured timestamp. |

**GMAC_MAC_Auxiliary_Control**

Address: Operational Base + offset (0x0b40)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4 | RW | 0x0 | ATSEN0<br>Auxiliary Snapshot 0 Enable<br>This bit controls the capturing of Auxiliary Snapshot Trigger 0. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i[0] input is enabled. When this bit is reset, the events on this input are ignored.<br>Values:<br>0x0 (DISABLE): Auxiliary Snapshot 0 is disabled<br>0x1 (ENABLE): Auxiliary Snapshot 0 is enabled |
| 3:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | ATSFC<br>Auxiliary Snapshot FIFO Clear<br>When set, this bit resets the pointers of the Auxiliary Snapshot FIFO. This bit is cleared when the pointers are reset and the FIFO is empty. When this bit is high, the auxiliary snapshots are stored in the FIFO.<br>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.<br>Values:<br>1'b0: Auxiliary Snapshot FIFO Clear is disabled<br>1'b1: Auxiliary Snapshot FIFO Clear is enabled |

**GMAC_MAC_Auxiliary_TS_NS**

Address: Operational Base + offset (0x0b48)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |
| 30:0 | RO | 0x00000000 | AUXTSLO<br>Auxiliary Timestamp<br>Contains the lower 31 bits (nanoseconds field) of the auxiliary timestamp. |

**GMAC_MAC_Auxiliary_TS_Secs**

Address: Operational Base + offset (0x0b4c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | AUXTSHI<br>Auxiliary Timestamp<br>Contains the lower 32 bits of the Seconds field of the auxiliary timestamp. |

**GMAC_MAC_TS_Ingress_Corr_NS**

Address: Operational Base + offset (0x0b58)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | TSIC<br>Timestamp Ingress Correction<br>This field contains the ingress path correction value as defined by the Ingress Correction expression. |

**GMAC_MAC_TS_Egress_Corr_NS**

Address: Operational Base + offset (0x0b5c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | TSEC<br>Timestamp Egress Correction<br>This field contains the nanoseconds part of the egress path correction value as defined by the Egress Correction expression. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**GMAC_MAC_TS_Ingress_Latency**

Address: Operational Base + offset (0x0b68)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23:16 | RO | 0x00 | ITLNS<br>Ingress Timestamp Latency, in sub-nanoseconds<br>This register holds the average latency in sub-nanoseconds between the input ports (phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken. |
| 15:8 | RO | 0x00 | ITLSNS<br>Ingress Timestamp Latency, in nanoseconds<br>This register holds the average latency in nanoseconds between the input ports (phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken. |

**GMAC_MAC_TS_Egress_Latency**

Address: Operational Base + offset (0x0b6c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23:16 | RO | 0x00 | ETLNS<br>Egress Timestamp Latency, in nanoseconds<br>This register holds the average latency in nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC. |
| 15:8 | RO | 0x00 | ETLSNS<br>Egress Timestamp Latency, in sub-nanoseconds<br>This register holds the average latency in sub-nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC. |

**GMAC_MAC_PPS_Control**

Address: Operational Base + offset (0x0b70)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RW | 0x0 | MCGREN0<br>MCGR Mode Enable for PPS0 Output<br>This field enables the 0th PPS instance to operate in PPS or MCGR mode. When set it operates in MCGR mode and on reset it operates in PPS mode.<br>Values:<br>0x0 (PPS): 0th PPS instance is enabled to operate in PPS mode<br>0x1 (MCGR): 0th PPS instance is enabled to operate in MCGR mode |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6:5 | RW | 0x0 | TRGTMODSEL0<br>Target Time Register Mode for PPS0 Output<br>This field indicates the Target Time registers (MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds) mode for PPS0 output signal:<br>Values:<br>0x0 (ONLY_INT): Target Time registers are programmed only for generating the interrupt event. The Flexible PPS function must not be enabled in this mode, otherwise spurious transitions may be observed on the corresponding ptp_pps_o output port<br>0x1 (Reserved): Reserved<br>0x2 (INT_ST): Target Time registers are programmed for generating the interrupt event and starting or stopping the PPS0 output signal generation<br>0x3 (ONLY_ST): Target Time registers are programmed only for starting or stopping the PPS0 output signal generation. No interrupt is asserted |
| 4 | RW | 0x0 | PPSEN0<br>Flexible PPS Output Mode Enable<br>When this bit is set, Bits[3:0] function as PPSCMD. When this bit is reset, Bits[3:0] function as PPSCTRL (Fixed PPS mode).<br>Values:<br>0x0 (DISABLE): Flexible PPS Output Mode is disabled<br>0x1 (ENABLE): Flexible PPS Output Mode is enabled |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RW | 0x0 | PPSCTRL_PPSCMD(cont.)<br>Flexible PPS Output (ptp_pps_o[0]) Control<br>Programming these bits with a non-zero value instructs the MAC to initiate an event. When the command is transferred or synchronized to the PTP clock domain, these bits get cleared automatically. The software should ensure that these bits are programmed only when they are 'all-zero'. The following list describes the values of PPSCMD0:<br>4'b0000: No Command<br>4'b0001: START Single Pulse<br>This command generates single pulse rising at the start point defined in MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds register and of a duration defined in the PPS0 Width Register.<br>4'b0010: START Pulse Train<br>This command generates the train of pulses rising at the start point defined in the Target Time Registers and of a duration defined in the PPS0 Width Register and repeated at interval defined in the PPS Interval Register. By default, the PPS pulse train is free-running unless stopped by the 'Stop Pulse train at time' or 'Stop Pulse Train immediately' commands.<br>4'b0011: Cancel START<br>This command cancels the START Single Pulse and START Pulse Train commands if the system time has not crossed the programmed start time.<br>4'b0100: STOP Pulse train at time<br>This command stops the train of pulses initiated by the START Pulse Train command (PPSCMD = 0010) after the time programmed in the Target Time registers elapses.<br>4'b0101: STOP Pulse Train immediately<br>This command immediately stops the train of pulses initiated by the START Pulse Train command (PPSCMD = 0010).<br>4'b0110: Cancel STOP Pulse train<br>This command cancels the STOP pulse train at time command if the programmed stop time has not elapsed. The PPS pulse train becomes free-running on the successful execution of this command.<br>4'b0111-4'b1111: Reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RW | 0x0 | PPSCTRL_PPSCMD<br>PPS Output Frequency Control<br>This field controls the frequency of the PPS0 output (ptp_pps_o[0]) signal. The default value of PPSCTRL is 0000, and the PPS output is 1 pulse (of width clk_ptp_i) every second. For other values of PPSCTRL, the PPS output becomes a generated clock of following frequencies:<br>4'b0001: The binary rollover is 2 Hz, and the digital rollover is 1 Hz.<br>4'b0010: The binary rollover is 4 Hz, and the digital rollover is 2 Hz.<br>4'b0011: The binary rollover is 8 Hz, and the digital rollover is 4 Hz.<br>4'b0100: The binary rollover is 16 Hz, and the digital rollover is 8 Hz.<br>...<br>4'b1111: The binary rollover is 32.768 KHz and the digital rollover is 16.384 KHz.<br>Note:<br>In the binary rollover mode, the PPS output (ptp_pps_o) has a duty cycle of 50 percent with these frequencies. In the digital rollover mode, the PPS output frequency is an average number. The actual clock is of different frequency that gets synchronized every second. For example:<br>1. When PPSCTRL = 0001, the PPS (1 Hz) has a low period of 537 ms and a high period of 463 ms.<br>2. When PPSCTRL = 0010, the PPS (2 Hz) is a sequence of One clock of 50 percent duty cycle and 537 ms period Second clock of 463 ms period (268 ms low and 195 ms high).<br>3. When PPSCTRL = 0011, the PPS (4 Hz) is a sequence of Three clocks of 50 percent duty cycle and 268 ms period Fourth clock of 195 ms period (134 ms low and 61 ms high).<br>This behavior is because of the non-linear toggling of bits in the digital rollover mode in the MAC_System_Time_Nanoseconds register. |

**GMAC_MAC_PPS0_Target_Time_Seconds**

Address: Operational Base + offset (0x0b80)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | TSTRH0<br>PPS Target Time Seconds Register<br>This field stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on Target Time mode selected for the corresponding PPS output in the MAC_PPS_Control register.<br>If GMAC_FLEXI_PPS_OUT_EN is enabled in the configuration and PTGE field of MAC_Timestamp_Control Register is set with Presentation time control set in recovery mode, then these bits indicate the TPT being programmed by the application and in generation mode it indicates the CPT generated at the sampled trigger. |

**GMAC_MAC_PPS0_Target_Time_Ns**

Address: Operational Base + offset (0x0b84)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | TRGTBUSY0<br>PPS Target Time Register Busy<br>The MAC sets this bit when the PPSCMD0 field in the MAC_PPS_Control register is programmed to 010 or 011. Programming the PPSCMD0 field to 010 or 011 instructs the MAC to synchronize the Target Time Registers to the PTP clock domain.The MAC clears this bit after synchronizing the Target Time Registers to the PTP clock domain The application must not update the Target Time Registers when this bit is read as 1. Otherwise, the synchronization of the previous programmed timegets corrupted.<br>Values:<br>0x0 (INACTIVE): PPS Target Time Register Busy status is not detected<br>0x1 (ACTIVE): PPS Target Time Register Busy is detected |
| 30:0 | RW | 0x00000000 | TTSL0<br>Target Time Low for PPS Register<br>This register stores the time in (signed) nanoseconds. When the value of the timestamp matches the value in both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on the TRGTMODSEL0 field (Bits [6:5]) in MAC_PPS_Control.<br>When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, this value should be (time in ns / 0.465). The actual start or stop time of the PPS signal output may have an error margin up to one unit of sub-second increment value.<br>When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, this value should not exceed 0x3B9A_C9FF. The actual start or stop time of the<br>PPS signal output may have an error margin up to one unit of sub-second increment value.<br>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. |

**GMAC_MAC_PPS0_Interval**

Address: Operational Base + offset (0x0b88)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | PPSINT0<br>PPS Output Signal Interval<br>These bits store the interval between the rising edges of PPS0 signal output. The interval is stored in terms of number of units of sub-second increment value.<br>You need to program one value less than the required interval. For example, if the PTP reference clock is 50 MHz (period of 20 ns), and desired interval between the rising edges of PPS0 signal output is 100 ns (that is, 5 units of sub-second increment value), you should program value 4 (5-1) in this register. |

**GMAC_MAC_PPS0_Width**

Address: Operational Base + offset (0x0b8c)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | PPSWIDTH0<br>PPS Output Signal Width<br>These bits store the width between the rising edge and corresponding falling edge of PPS0 signal output. The width is stored in terms of number of units of sub-second increment value.<br>You need to program one value less than the required interval. For example, if PTP reference clock is 50 MHz (period of 20 ns), and width between the rising and corresponding falling edges of PPS0 signal output is 80 ns (that is, four units of sub-second increment value), you should program value 3 (4-1) in this register.<br>Note: The value programmed in this register must be lesser than the value programmed in MAC_PPS0_Interval. |

**GMAC_MTL_Operation_Mode**

Address: Operational Base + offset (0x0c00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9 | RW | 0x0 | CNTCLR<br>Counters Reset<br>When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle.<br>If this bit is set along with CNT_PRESET bit, CNT_PRESET has precedence.<br>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.<br>Values:<br>0x0 (DISABLE): Counters are not reset<br>0x1 (ENABLE): All counters are reset |
| 8 | RW | 0x0 | CNTPRST<br>Counters Preset<br>When this bit is set,<br>1.MTL_TxQ[0-7]_Underflow register is initialized/preset to 12'h7F0.<br>2.Missed Packet and Overflow Packet counters in MTL_RxQ[0-7]_Missed_Packet_Overflow_Cnt register is initialized/preset to 12'h7F0.<br>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.<br>Values:<br>0x0 (DISABLE): Counters Preset is disabled<br>0x1 (ENABLE): Counters Preset is enabled |
| 7 | RO | 0x0 | reserved |
| 6:5 | RW | 0x0 | SCHALG<br>Tx Scheduling Algorithm<br>This field indicates the algorithm for Tx scheduling:Values:<br>0x0 (WRR): WRR algorithm<br>0x1 (WFQ): WFQ algorithm when DCB feature is selected. Otherwise, Reserved<br>0x2 (DWRR): DWRR algorithm when DCB feature is selected. Otherwise, Reserved<br>0x3 (SP): Strict priority algorithm |
| 4:3 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | RAA<br>Receive Arbitration Algorithm<br>This field is used to select the arbitration algorithm for the Rx side.<br>0: Strict priority (SP)<br>Queue 0 has the lowest priority and the last queue has the highest priority.<br>1: Weighted Strict Priority (WSP)<br>Values:<br>0x0 (SP): Strict priority (SP)<br>0x1 (WSP): Weighted Strict Priority (WSP) |
| 1 | RW | 0x0 | DTXSTS<br>Drop Transmit Status<br>When this bit is set, the Tx packet status received from the MAC is dropped in the MTL. When this bit is reset, the Tx packet status received from the MAC is forwarded to the application.<br>Values:<br>0x0 (DISABLE): Drop Transmit Status is disabled<br>0x1 (ENABLE): Drop Transmit Status is enabled |

**GMAC_MTL_DBG_CTL**

Address: Operational Base + offset (0x0c08)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15 | RW | 0x0 | STSIE<br>Transmit Status Available Interrupt Status Enable<br>When this bit is set, an interrupt is generated when Transmit status is available in slave mode.<br>Values:<br>1'b0: Transmit Packet Available Interrupt Status is disabled<br>1'b1: Transmit Packet Available Interrupt Status is enabled |
| 14 | RW | 0x0 | PKTIE<br>Receive Packet Available Interrupt Status Enable<br>When this bit is set, an interrupt is generated when EOP of received packet is written to the Rx FIFO.<br>Values:<br>1'b0: Receive Packet Available Interrupt Status is disabled<br>1'b1: Receive Packet Available Interrupt Status is enabled |
| 13:12 | RW | 0x0 | FIFOSEL<br>FIFO Selected for Access<br>This field indicates the FIFO selected for debug access:<br>Values:<br>2'b00: Tx FIFO<br>2'b01: Tx Status FIFO (only read access when SLVMOD is set)<br>2'b10: TSO FIFO (cannot be accessed when SLVMOD is set)<br>2'b11: Rx FIFO |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11 | RW | 0x0 | FIFOWREN<br>FIFO Write Enable<br>When this bit is set, it enables the Write operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0.<br>Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets.<br>Values:<br>1'b0: FIFO Write is disabled<br>1'b1: FIFO Write is enabled |
| 10 | RW | 0x0 | FIFORDEN<br>FIFO Read Enable<br>When this bit is set, it enables the Read operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0.<br>Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets.<br>Values:<br>1'b0: FIFO Read is disabled<br>1'b1: FIFO Read is enabled |
| 9 | RW | 0x0 | RSTSEL<br>Reset Pointers of Selected FIFO<br>When this bit is set, the pointers of the currently-selected FIFO are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0.<br>Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets.<br>Values:<br>1'b0: Reset Pointers of Selected FIFO is disabled<br>1'b1: Reset Pointers of Selected FIFO is enabled |
| 8 | RW | 0x0 | RSTALL<br>Reset All Pointers<br>When this bit is set, the pointers of all FIFOs are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0.<br>Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets.<br>Values:<br>1'b0: Reset All Pointers is disabled<br>1'b1: Reset All Pointers is enabled |
| 7 | RO | 0x0 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6:5 | RW | 0x0 | PKTSTATE<br>Encoded Packet State<br>This field is used to write the control information to the Tx FIFO or Rx FIFO.<br>Tx FIFO:<br>2'b00: Packet Data<br>2'b01: Control Word<br>2'b10: SOP Data<br>2'b11: EOP Data<br>Rx FIFO:<br>2'b00: Packet Data<br>2'b01: Normal Status<br>2'b10: Last Status<br>2'b11: EOP<br>Values:<br>2'b00: Packet Data<br>2'b01: Control Word/Normal Status<br>2'b10: SOP Data/Last Status<br>2'b11: EOP Data/EOP |
| 4 | RO | 0x0 | reserved |
| 3:2 | RW | 0x0 | BYTEEN<br>Byte Enables<br>This field indicates the number of data bytes valid in the data register during Write operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected.<br>Values:<br>2'b00: Byte 0 valid<br>2'b01: Byte 0 and Byte 1 are valid<br>2'b10: Byte 0, Byte 1, and Byte 2 are valid<br>2'b11: All four bytes are valid |
| 1 | RW | 0x0 | DBGMOD<br>Debug Mode Access to FIFO<br>When this bit is set, it indicates that the current access to the FIFO is read, write, and debug access. In this mode, the following access types are allowed:<br>1. Read and Write access to Tx FIFO, TSO FIFO, and Rx FIFO<br>2. Read access is allowed to Tx Status FIFO.<br>When this bit is reset, it indicates that the current access to the FIFO is slave access bypassing the DMA. In this mode, the following access are allowed:<br>1. Write access to the Tx FIFO<br>2. Read access to the Rx FIFO and Tx Status FIFO<br>Values:<br>1'b0: Debug Mode Access to FIFO is disabled<br>1'b1: Debug Mode Access to FIFO is enabled |
| 0 | RW | 0x0 | FDBGEN<br>FIFO Debug Access Enable<br>When this bit is set, it indicates that the debug mode access to the FIFO is enabled. When this bit is reset, it indicates that the FIFO can be accessed only through a master interface.<br>Values:<br>1'b0: FIFO Debug Access is disabled<br>1'b1: FIFO Debug Access is enabled |

**GMAC_MTL_DBG_STS**

Address: Operational Base + offset (0x0c0c)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15 | RO | 0x320 | LOCR<br>Remaining Locations in the FIFO<br>Slave Access Mode:<br>This field indicates the space available in selected FIFO.<br>Debug Access Mode:<br>This field contains the Write or Read pointer value of the selected FIFO during Write or Read operation, respectively.<br>Reset: In single Tx Queue configurations, (GMAC_TXFIFO_SIZE/(GMAC_DATAWIDTH/8)), Otherwise 0000H. |
| 14:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | STSI<br>Transmit Status Available Interrupt Status<br>When set, this bit indicates that the Slave mode Tx packet is transmitted, and the status is available in Tx Status FIFO. This bit is reset when 1 is written to this bit.<br>Values:<br>1'b0: Transmit Status Available Interrupt Status not detected<br>1'b1: Transmit Status Available Interrupt Status detected |
| 8 | RW | 0x0 | PKTI<br>Receive Packet Available Interrupt Status<br>When set, this bit indicates that MAC layer has written the EOP of received packet to the Rx FIFO. This bit is reset when 1 is written to this bit.<br>Values:<br>1'b0: Receive Packet Available Interrupt Status not detected<br>1'b1: Receive Packet Available Interrupt Status detected |
| 7:5 | RO | 0x0 | reserved |
| 4:3 | RO | 0x0 | BYTEEN<br>Byte Enables<br>This field indicates the number of data bytes valid in the data register during Read operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected.<br>Values:<br>2'b00: Byte 0 valid<br>2'b01: Byte 0 and Byte 1 are valid<br>2'b10: Byte 0, Byte 1, and Byte 2 are valid<br>2'b11: All four bytes are valid |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2:1 | RO | 0x0 | PKTSTATE<br>Encoded Packet State<br>This field is used to get the control or status information of the selected FIFO.<br>Tx FIFO:<br>2'b00: Packet Data<br>2'b01: Control Word<br>2'b10: SOP Data<br>2'b11: EOP Data<br>Rx FIFO:<br>2'b00: Packet Data<br>2'b01: Normal Status<br>2'b10: Last Status<br>2'b11: EOP<br>This field is applicable only for Tx FIFO and Rx FIFO during Read operation.<br>Values:<br>2'b00: Packet Data<br>2'b01: Control Word/Normal Status<br>2'b10: SOP Data/Last Status<br>2'b11: EOP Data/EOP |
| 0 | RO | 0x0 | FIFOBUSY<br>FIFO Busy<br>When set, this bit indicates that a FIFO operation is in progress in the MAC and content of the following fields is not valid:<br>1. All other fields of this register<br>2. All fields of the MTL_FIFO_Debug_Data register<br>Values:<br>1'b0: FIFO Busy not detected<br>1'b1: FIFO Busy detected |

**GMAC_MTL_FIFO_Debug_Data**

Address: Operational Base + offset (0x0c10)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | FDBGDATA<br>FIFO Debug Data<br>During debug or slave access write operation, this field contains the data to be written to the Tx FIFO, Rx FIFO, or TSO FIFO.<br>During debug or slave access read operation, this field contains the data read from the Tx FIFO, Rx FIFO, TSO FIFO, or Tx Status FIFO. |

**GMAC_MTL_Interrupt_Status**

Address: Operational Base + offset (0x0c20)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:19 | RO | 0x0000 | reserved |
| 18 | RO | 0x0 | ESTIS<br>EST (TAS- 802.1Qbv) Interrupt Status<br>This bit indicates an interrupt event during the operation of 802.1Qbv. To reset this bit, the application must clear the error/event that has caused the Interrupt.<br>Values:<br>0x0 (INACTIVE): EST (TAS- 802.1Qbv) Interrupt status not detected<br>0x1 (ACTIVE): EST (TAS- 802.1Qbv) Interrupt status detected |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17 | RO | 0x0 | DBGIS<br>Debug Interrupt status<br>This bit indicates an interrupt event during the slave access. To reset this bit, the application must read the FIFO Debug Access Status register to get the exact cause of the interrupt and clear its source.<br>Values:<br>1'b0: Debug Interrupt status not detected<br>1'b1: Debug Interrupt status detected |
| 16:2 | RO | 0x0000 | reserved |
| 1 | RO | 0x0 | Q1IS<br>Queue 1 Interrupt status<br>This bit indicates that there is an interrupt from Queue 1. To reset this bit, the application must read the MTL_Q1_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source.<br>Values:<br>0x0 (INACTIVE): Queue 1 Interrupt status not detected<br>0x1 (ACTIVE): Queue 1 Interrupt status detected |
| 0 | RO | 0x0 | Q0IS<br>Queue 0 Interrupt status<br>This bit indicates that there is an interrupt from Queue 0. To reset this bit, the application must read Queue 0 Interrupt Control and Status register to get the exact cause of the interrupt and clear its source.<br>Values:<br>1'b0: Queue 0 Interrupt status not detected<br>1'b1: Queue 0 Interrupt status detected |

**GMAC_MTL_RxQ_DMA_Map0**

Address: Operational Base + offset (0x0c30)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |
| 12 | RW | 0x0 | Q1DDMACH<br>Queue 1 Enabled for DA-based DMA Channel Selection<br>When set, this bit indicates that the packets received in Queue 1 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address.<br>When reset, this bit indicates that the packets received in Queue 1 are routed to the DMA Channel programmed in the Q1MDMACH field (Bits[10:8]).<br>Values:<br>0x0 (DISABLE): Queue 1 disabled for DA-based DMA Channel Selection<br>0x1 (ENABLE): Queue 1 enabled for DA-based DMA Channel Selection |
| 11:9 | RO | 0x0 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | Q1MDMACH<br>Queue 1 Mapped to DMA Channel<br>This field controls the routing of the received packet in Queue 1 to the DMA channel:<br>000: DMA Channel 0<br>001: DMA Channel 1<br>010: DMA Channel 2<br>011: DMA Channel 3<br>100: DMA Channel 4<br>101: DMA Channel 5<br>110: DMA Channel 6<br>111: DMA Channel 7<br>This field is valid when the Q1DDMACH field is reset.<br>The width of this field depends on the number of RX DMA channels and not all the values may be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved. |
| 7:5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | Q0DDMACH<br>Queue 0 Enabled for DA-based DMA Channel Selection<br>When set, this bit indicates that the packets received in Queue 0 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address.<br>When reset, this bit indicates that the packets received in Queue 0 are routed to the DMA Channel programmed in the Q0MDMACH field.<br>Values:<br>0x0 (DISABLE): Queue 0 disabled for DA-based DMA Channel Selection<br>0x1 (ENABLE): Queue 0 enabled for DA-based DMA Channel Selection |
| 3:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | Q0MDMACH<br>Queue 0 Mapped to DMA Channel<br>This field controls the routing of the packet received in Queue 0 to the DMA channel:<br>000: DMA Channel 0<br>001: DMA Channel 1<br>010: DMA Channel 2<br>011: DMA Channel 3<br>100: DMA Channel 4<br>101: DMA Channel 5<br>110: DMA Channel 6<br>111: DMA Channel 7<br>This field is valid when the Q0DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values may be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved. |

**GMAC_MTL_TBS_CTRL**

Address: Operational Base + offset (0x0c40)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RW | 0x000000 | LEOS<br>Launch Expiry Offset<br>The value in units of 256 nanoseconds that has to be added to the Launch time to compute the Launch Expiry time. Value valid only when LEOV is set.<br>Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value. |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x0 | LEGOS<br>Launch Expiry GSN Offset<br>The number GSN slots that has to be added to the Launch GSN to compute the Launch Expiry time. Value valid only when LEOV is set. |
| 3:2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | LEOV<br>Launch Expiry Offset Valid<br>When set indicates the LEOS field is valid. When not set, indicates the Launch Expiry Offset is not valid and the MTL must not check for Launch expiry time.<br>Values:<br>0x0 (INVALID): LEOS field is invalid<br>0x1 (VALID): LEOS field is valid |
| 0 | RW | 0x0 | ESTM<br>EST offset Mode<br>When this bit is set, the Launch Time value used in Time Based Scheduling is interpreted as an EST offset value and is added to the Base Time Register (BTR) of the current list.<br>When reset, the Launch Time value is used as an absolute value that should be compared with the System time [39:8].<br>Values:<br>0x0 (DISABLE): EST offset Mode is disabled<br>0x1 (ENABLE): EST offset Mode is enabled |

**GMAC_MTL_EST_Control**

Address: Operational Base + offset (0x0c50)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | PTOV<br>PTP Time Offset Value<br>The value of PTP Clock period multiplied by 6 in nanoseconds. This value is needed to avoid transmission overruns at the beginning of the installation of a new GCL. |
| 23 | RO | 0x0 | reserved |
| 22:11 | RW | 0x000 | CTOV<br>Current Time Offset Value<br>Provides a 12 bit time offset value in nano second that is added to the current time to compensate for all the implementation pipeline delays such as the CDC sync delay, buffering delays, data path delays etc. This offset helps to ensure that the impact of gate controls is visible on the line exactly at the pre-determined schedule (or as close to the schedule as possible). |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10:8 | RW | 0x0 | TILS<br>Time Interval Left Shift Amount<br>This field provides the left shift amount for the programmed Time Interval values used in the Gate Control Lists.<br>000: No left shift needed (equal to x1ns)<br>001: Left shift TI by 1 bit (equal to x2ns)<br>010: Left shift TI by 2 bits (equal to x4ns)<br>...<br>100: Left shift TI by 7 bits (equal to x128ns)<br>Based on the configuration one or more bits of this field should be treated as Reserved/Read-Only. |
| 7:6 | RW | 0x0 | LCSE<br>Loop Count to report Scheduling Error<br>Programmable number of GCL list iterations before reporting an HLBS error defined in EST_Status register.<br>Values:<br>0x0 (4_ITERNS): 4 iterations<br>0x1 (8_ITERNS): 8 iterations<br>0x2 (16_ITERNS): 16 iterations<br>0x3 (32_ITERNS): 32 iterations |
| 5 | RW | 0x0 | DFBS<br>Drop Frames causing Scheduling Error<br>When set frames reported to cause HOL Blocking due to not getting scheduled (HLBS field of EST_Status register) after 4,8,16,32 (based on LCSE field of this register) GCL iterations are dropped.<br>Values:<br>0x0 (DONT_DROP): Do not Drop Frames causing Scheduling Error<br>0x1 (DROP): Drop Frames causing Scheduling Error |
| 4 | RW | 0x0 | DDBF<br>Do not Drop frames during Frame Size Error<br>When set, frames are not be dropped during Head-of-Line blocking due to Frame Size Error (HLBF field of EST_Status register).<br>Values:<br>0x0 (DROP): Drop frames during Frame Size Error<br>0x1 (DONT_DROP): Do not Drop frames during Frame Size Error |
| 3:2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | SSWL<br>Switch to S/W owned list<br>When set indicates that the software has programmed that list that it currently owns (SWOL) and the hardware should switch to the new list based on the new BTR. Hardware clears this bit when the switch to the SWOL happens to indicate the completion of the switch or when an BTR error (BTRE in Status register) is set. When BTRE is set this bit is cleared but SWOL is not updated as the switch was not successful.<br>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.<br>Values:<br>0x0 (DISABLE): Switch to S/W owned list is disabled<br>0x1 (ENABLE): Switch to S/W owned list is enabled |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | EEST<br>Enable EST<br>When reset, the gate control list processing is halted and all gates are assumed to be in Open state. Should be set for the hardware to start processing the gate control lists. During the toggle from 0 to 1, the gate control list processing starts only after the SSWL bit it set.<br>When GMAC_ASP_ECC is selected during the configuration, if any uncorrectable error is detected in the EST memory the hardware will reset this bit and disable the EST function.<br>Values:<br>0x0 (DISABLE): EST is disabled<br>0x1 (ENABLE): EST is enabled |

**GMAC_MTL_EST_Status**

Address: Operational Base + offset (0x0c58)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:16 | RO | 0x0 | CGSN<br>Current GCL Slot Number<br>Indicates the slot number of the GCL list. Slot number is a modulo 16 count of the GCL List loops executed so far. Even if a new GCL list is installed, the count is incremental. |
| 15:12 | RO | 0x0 | reserved |
| 11:8 | RO | 0x0 | BTRL<br>BTR Error Loop Count<br>Provides the minimum count (N) for which the equation Current Time =< New BTR + (N * New Cycle Time) becomes true. N = "1111" indicates the iterations exceeded the value of 8 and the hardware was not able to update New BTR to be equal to or greater than Current Time. Software intervention is needed to update the New BTR. Value cleared when BTRE field of this register is cleared. |
| 7 | RO | 0x0 | SWOL<br>S/W owned list<br>When '0' indicates Gate control list number "0" is owned by software and when "1" indicates the Gate Control list "1" is owned by the software. Any reads/writes by the software (using indirect access via GCL_Control) is directed to the list indicated by this value by default. The inverse of this value is treated as HWOL.<br>R/W operations performed by hardware are directed to the list pointed by HWOL by default.<br>Values:<br>0x0 (INACTIVE): Gate control list number "0" is owned by software<br>0x1 (ACTIVE): Gate control list number "1" is owned by software |
| 6:5 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | CGCE<br>Constant Gate Control Error<br>This error occurs when the list length (LLR) is 1 and the programmed Time Interval (TI) value after the optional Left Shifting is less than or equal to the Cycle Time (CTR). The above programming implies Gates are either always Closed or always Open based on the Gate Control values; the same effect can be achieved by other simpler (non TSN) programming mechanisms. Since the implementation does not support such a programming an error is reported.<br>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.<br>Values:<br>0x0 (INACTIVE): Constant Gate Control Error not detected<br>0x1 (ACTIVE): Constant Gate Control Error detected |
| 3 | RO | 0x0 | HLBS<br>Head-Of-Line Blocking due to Scheduling<br>Set when the frame is not able to win arbitration and get scheduled even after 4 iterations of the GCL. Indicates to software a potential programming error. The one hot encoded values of the Queue Numbers that are not able to make progress are indicated in the MTL_EST_Sch_Error register. Bit cleared when MTL_EST_Sch_Error register is all zeros.<br>Values:<br>0x0 (INACTIVE): Head-Of-Line Blocking due to Scheduling not detected<br>0x1 (ACTIVE): Head-Of-Line Blocking due to Scheduling detected |
| 2 | RO | 0x0 | HLBF<br>Head-Of-Line Blocking due to Frame Size<br>Set when HOL Blocking is noticed on one or more Queues as a result of none of the Time Intervals of gate open in the GCL being greater than or equal to the duration needed for frame size (or frame fragment size when preemption is enabled) transmission. The one hot encoded Queue numbers that are experiencing HLBF are indicated in the MTL_EST_Frm_Size_Error register. Additionally, the first Queue number that experienced HLBF along with the frame size is captured in MTL_EST_Frm_Size_Capture register. Bit cleared when MTL_EST_Frame_Size_ Error register is all zeros.<br>Values:<br>0x0 (INACTIVE): Head-Of-Line Blocking due to Frame Size not detected<br>0x1 (ACTIVE): Head-Of-Line Blocking due to Frame Size detected |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | BTRE<br>BTR Error<br>When "1" indicates a programming error in the BTR of SWOL where the programmed value is less than current time. If the BTRL = "1111", SWOL is not updated and Software should reprogram the BTR to a value greater than current time and then set SSWL to reinitiate the switch to SWOL. Else if the value of BTRL < "1111", SWOL is updated and this field indicates the number of iterations (of + CycleTime) taken by hardware to update the BTR to a value greater than Current Time.<br>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.<br>Values:<br>0x0 (INACTIVE): BTR Error not detected<br>0x1 (ACTIVE): BTR Error detected |
| 0 | RW | 0x0 | SWLC<br>Switch to S/W owned list Complete<br>When "1" indicates the hardware has successfully switched to the SWOL, and the SWOL bit has been updated to that effect. Cleared when the SSWL of EST_Control register transitions from 0 to 1, or on a software write.<br>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.<br>Values:<br>0x0 (INACTIVE): Switch to S/W owned list Complete not detected<br>0x1 (ACTIVE): Switch to S/W owned list Complete detected |

**GMAC_MTL_EST_Sch_Error**

Address: Operational Base + offset (0x0c60)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1:0 | RW | 0x0 | SEQN<br>Schedule Error Queue Number<br>The One Hot Encoded Queue Numbers that have experienced error/timeout described in HLBS field of status register.<br>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. |

**GMAC_MTL_EST_Frm_Size_Error**

Address: Operational Base + offset (0x0c64)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1:0 | RW | 0x0 | FEQN<br>Frame Size Error Queue Number<br>The One Hot Encoded Queue Numbers that have experienced error described in HLBF field of status register.<br>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. |

**GMAC_MTL_EST_Frm_Size_Capture**

Address: Operational Base + offset (0x0c68)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 16 | RO | 0x0 | HBFQ<br>Queue Number of HLBF<br>Captures the binary value of the of the first Queue (number) experiencing HLBF error (see HLBF field of status register). Value once written is not altered by any subsequent queue errors of similar nature. Once cleared the queue number of the next occurring HLBF error is captured. Width is based on the number of Tx Queues configured; remaining bits are Read-Only. Cleared when MTL_EST_Frm_Size_Error register is all zeros. |
| 15 | RO | 0x0 | reserved |
| 14:0 | RO | 0x0000 | HBFS<br>Frame Size of HLBF<br>Captures the Frame Size of the dropped frame related to queue number indicated in HBFQ field of this register. Contents of this register should be considered invalid, if this field is zero. Cleared when MTL_EST_Frm_Size_Error register is all zeros. |

**GMAC_MTL_EST_Intr_Enable**

Address: Operational Base + offset (0x0c70)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4 | RW | 0x0 | CGCE<br>Interrupt Enable for CGCE<br>When set, generates interrupt when the Constant Gate Control Error occurs and is indicated in the status. When reset this event does not generate an interrupt<br>Values:<br>0x0 (DISABLE): Interrupt for CGCE is disabled<br>0x1 (ENABLE): Interrupt for CGCE is enabled |
| 3 | RW | 0x0 | IEHS<br>Interrupt Enable for HLBS<br>When set, generates interrupt when the Head-of-Line Blocking due to Scheduling issue and is indicated in the status. When reset this event does not generate an interrupt.<br>Values:<br>0x0 (DISABLE): Interrupt for HLBS is disabled<br>0x1 (ENABLE): Interrupt for HLBS is enabled |
| 2 | RW | 0x0 | IEHF<br>Interrupt Enable for HLBF<br>When set, generates interrupt when the Head-of-Line Blocking due to Frame Size error occurs and is indicated in the status. When reset this event does not generate an interrupt.<br>Values:<br>0x0 (DISABLE): Interrupt for HLBF is disabled<br>0x1 (ENABLE): Interrupt for HLBF is enabled |
| 1 | RW | 0x0 | IEBE<br>Interrupt Enable for BTR Error<br>When set, generates interrupt when the BTR Error occurs and is indicated in the status. When reset this event does not generate an interrupt.<br>Values:<br>0x0 (DISABLE): Interrupt for BTR Error is disabled<br>0x1 (ENABLE): Interrupt for BTR Error is enabled |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | IECC<br>Interrupt Enable for Switch List<br>When set, generates interrupt when the configuration change is successful and the hardware has switched to the new list.<br>When reset this event does not generate an interrupt.<br>Values:<br>0x0 (DISABLE): Interrupt for Switch List is disabled<br>0x1 (ENABLE): Interrupt for Switch List is enabled |

**GMAC_MTL_EST_GCL_Control**

Address: Operational Base + offset (0x0c80)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23:22 | RW | 0x0 | ESTEIEC<br>ECC Inject Error Control for EST Memory<br>When EIEE bit of this register is set, following are the errors inserted based on the value encoded in this field.<br>This filed will be valid only if GMAC_ASP_ECC feature is selected during the configuration, else it will be reserved.<br>Values:<br>0x0 (1BIT): Insert 1 bit error<br>0x1 (2BIT): Insert 2 bit errors<br>0x2 (3BIT): Insert 3 bit errors<br>0x3 (1BIT_ADDR): Insert 1 bit error in address field |
| 21 | RO | 0x0 | ESTEIEE<br>EST ECC Inject Error Enable<br>When set along with EEST bit of MTL_EST_Control register, enables the ECC error injection feature.<br>When reset, disables the ECC error injection feature.<br>Values:<br>0x0 (DISABLE): EST ECC Inject Error is disabled<br>0x1 (ENABLE): EST ECC Inject Error is enabled |
| 20 | RW | 0x0 | ERR0<br>When set indicates the last write operation was aborted as software writes to GCL and GCL registers is prohibited when SSWL bit of MTL_EST_Control Register is set.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br>Values:<br>0x0 (DISABLE): ERR0 is disabled<br>0x1 (ENABLE): ERR1 is enabled |
| 19:16 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:8 | RW | 0x00 | ADDR<br>Gate Control List Address: (GCLA when GCRR is "0").<br>Provides the address (row number) of the Gate Control List at which the R/W operation has to be performed. By default the Gate Control List pointed by SWOL of MTL_EST_Status is selected for R/W, however if the DBGM bit of this register is set, a debug mode access is given to R/W from DBGB. The width of this field is dependent on GMAC_EST_DEP; unused bits should be treated as read only. Gate Control list Related Registers Address: (GCRA when GCRR is "1"). By default the GCL related register set pointed by SWOL of MTL_EST_Status is selected for R/W, however if the DBGM bit of this register is set, a debug mode access is given to R/W from DBGB. Lower 3 bits are only used in this mode, higher order bits are treated as dont cares.<br>000: BTR Low (31:0)<br>001: BTR High (63:31)<br>010: CTR Low (31:0)<br>011: CTR High (39:32)<br>100: TER (31:0)<br>101: LLR (n:0) (where n is (logGMAC_EST_DEP / log2))<br>Others: Reserved |
| 7:6 | RO | 0x0 | reserved |
| 5 | RW | 0x0 | DBGB<br>Debug Mode Bank Select<br>When set to "0" indicates R/W in debug mode should be directed to Bank 0 (GCL0 and corresponding Time related registers).<br>When set to "1" indicates R/W in debug mode should be directed to Bank 1 (GCL1 and corresponding Time related registers). This value is used when DBGM is set and overrides by value of SWOL which is normally used.<br>Values:<br>0x0 (BANK0): R/W in debug mode should be directed to Bank 0<br>0x1 (BANK1): R/W in debug mode should be directed to Bank 1 |
| 4 | RW | 0x0 | DBGM<br>Debug Mode<br>When set to "1" indicates R/W in debug mode where the memory bank (for GCL and Time related registers) is explicitly provided by DBGB value, when set to "0" SWOL bit is used to determine which bank to use.<br>Values:<br>0x0 (DISABLE): Debug Mode is disabled<br>0x1 (ENABLE): Debug Mode is enabled |
| 3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | GCRR<br>Gate Control Related Registers<br>When set to "1" indicates the R/W access is for the GCL related registers (BTR, CTR, TER, LLR) whose address is provided by GCRA. When "0" indicates R/W should be directed to GCL from the address provided by GCLA.<br>Values:<br>0x0 (DISABLE): Gate Control Related Registers are disabled<br>0x1 (ENABLE): Gate Control Related Registers are enabled |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | R1W0<br>Read '1', Write '0':<br>When set to '1': Read Operation<br>When set to '0': Write Operation.<br>Values:<br>0x0 (WRITE): Write Operation<br>0x1 (READ): Read Operation |
| 0 | RW | 0x0 | SRWO<br>Start Read/Write Op<br>When set indicates a Read/Write Op has started and is in progress.<br>When reset by hardware indicates the R/W Op has completed or an error has occurred (when bit 20 is set)<br>Reads: Data can be read from MTL_EST_GCL_Data register after this bit is reset<br>Writes: MTL_EST_GCL_Data should be programmed with write data before setting SRWO.<br>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.<br>Values:<br>0x0 (DISABLE): Start Read/Write Op disabled<br>0x1 (ENABLE): Start Read/Write Op enabled |

**GMAC_MTL_EST_GCL_Data**

Address: Operational Base + offset (0x0c84)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | GCD<br>Gate Control Data<br>The data corresponding to the address selected in the GCL_Control register. Used for both Read and Write operations. |

**GMAC_MTL_FPE_CTRL_STS**

Address: Operational Base + offset (0x0c90)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28 | RO | 0x0 | HRS<br>Hold/Release Status<br>1: Indicates a Set-and-Hold-MAC operation was last executed and the pMAC is in Hold State.<br>0: Indicates a Set-and-Release-MAC operation was last executed and the pMAC is in Release State.<br>Values:<br>0x0 (SET_REL): Indicates a Set-and-Release-MAC operation was last executed and the pMAC is in Release State<br>0x1 (SET_HOLD): Indicates a Set-and-Hold-MAC operation was last executed and the pMAC is in Hold State |
| 27:10 | RO | 0x00000 | reserved |
| 9:8 | RW | 0x0 | PEC<br>Preemption Classification<br>When set indicates the corresponding Queue must be classified as preemptable, when '0' Queue is classified as express. When both EST (Qbv) and Preemption are enabled, Queue-0 is always assumed to be preemptable. When EST (Qbv) is enabled Queues categorized as preemptable here are always assumed to be in "Open" state in the Gate Control List. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:2 | RO | 0x00 | reserved |
| 1:0 | RW | 0x0 | AFSZ<br>Additional Fragment Size<br>used to indicate, in units of 64 bytes, the minimum number of bytes over 64 bytes required in non-final fragments of preempted frames. The minimum non-final fragment size is (AFSZ +1) * 64 byte. |

**GMAC_MTL_FPE_Advance**

Address: Operational Base + offset (0x0c94)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | RADV<br>Release Advance<br>The maximum time in nanoseconds that can elapse between issuing a RELEASE to the MAC and the MAC being ready to resume transmission of preemptable frames, in the absence of there being any express frames available for transmission. |
| 15:0 | RW | 0x0000 | HADV<br>Hold Advance<br>The maximum time in nanoseconds that can elapse between issuing a HOLD to the MAC and the MAC ceasing to transmit any preemptable frame that is in the process of transmission or any preemptable frames that are queued for transmission. |

**GMAC_MTL_TxQ0_Operation_Mode**

Address: Operational Base + offset (0x0d00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:16 | RW | 0x06 | TQS<br>Transmit Queue Size<br>This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes.<br>When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value.<br>The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits |
| 15:7 | RO | 0x000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6:4 | RW | 0x0 | TTC<br>Transmit Threshold Control<br>These bits control the threshold level of the MTL Tx Queue. The transmission starts when the packet size within the MTL Tx Queue is larger than the threshold. In addition, full packets with length less than the threshold are also transmitted. These bits are used only when the TSF bit is reset.<br>Values:<br>3'b000: 32 bytes<br>3'b001: 64 bytes<br>3'b010: 96 bytes<br>3'b011: 128 bytes<br>3'b100: 192 bytes<br>3'b101: 256 bytes<br>3'b110: 384 bytes<br>3'b111: 512 bytes |
| 3:2 | RW | 0x0 | TXQEN<br>Transmit Queue Enable<br>This field is used to enable/disable the transmit queue 0.<br>2'b00: Not enabled<br>2'b01: Reserved<br>2'b10: Enabled<br>2'b11: Reserved<br>This field is Read Only in Single Queue configurations and Read Write in Multiple Queue configurations.<br>Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field.<br>Values:<br>0x0 (DISABLE): Not enabled<br>0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV)<br>0x2 (ENABLE): Enabled<br>0x3 (Reserved2): Reserved |
| 1 | RW | 0x0 | TSF<br>Transmit Store and Forward<br>When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped.<br>Values:<br>1'b0: Transmit Store and Forward is disabled<br>1'b1: Transmit Store and Forward is enabled |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | FTQ<br>Flush Transmit Queue<br>When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission.<br>Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active.<br>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.<br>Values:<br>1'b0: Flush Transmit Queue is disabled<br>1'b1: Flush Transmit Queue is enabled |

**GMAC_MTL_TxQ0_Underflow**

Address: Operational Base + offset (0x0d04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11 | RO | 0x0 | UFCNTOVF<br>Overflow Bit for Underflow Packet Counter<br>This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: Overflow not detected for Underflow Packet Counter<br>1'b1: Overflow detected for Underflow Packet Counter |
| 10:0 | RO | 0x000 | UFFRMCNT<br>Underflow Packet Counter<br>This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event. |

**GMAC_MTL_TxQ0_Debug**

Address: Operational Base + offset (0x0d08)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x000 | reserved |
| 22:20 | RO | 0x0 | STXSTSF<br>Number of Status Words in Tx Status FIFO of Queue<br>This field indicates the current number of status in the Tx Status FIFO of this queue.When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19 | RO | 0x0 | reserved |
| 18:16 | RO | 0x0 | PTXQ<br>Number of Packets in the Transmit Queue<br>This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue. |
| 15:6 | RO | 0x000 | reserved |
| 5 | RO | 0x0 | TXSTSFSTS<br>MTL Tx Status FIFO Full Status<br>When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission.<br>Values:<br>1'b0: MTL Tx Status FIFO Full status is not detected<br>1'b1: MTL Tx Status FIFO Full status is detected |
| 4 | RO | 0x0 | TXQSTS<br>MTL Tx Queue Not Empty Status<br>When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission.<br>Values:<br>1'b0: MTL Tx Queue Not Empty status is not detected<br>1'b1: MTL Tx Queue Not Empty status is detected |
| 3 | RO | 0x0 | TWCSTS<br>MTL Tx Queue Write Controller Status<br>When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue.<br>Values:<br>1'b0: MTL Tx Queue Write Controller status is not detected<br>1'b1: MTL Tx Queue Write Controller status is detected |
| 2:1 | RO | 0x0 | TRCSTS<br>MTL Tx Queue Read Controller Status<br>This field indicates the state of the Tx Queue Read Controller:<br>Values:<br>2'b00: Idle state<br>2'b01: Read state (transferring data to the MAC transmitter)<br>2'b10: Waiting for pending Tx Status from the MAC transmitter<br>2'b11: Flushing the Tx queue because of the Packet Abort request from the MAC |
| 0 | RO | 0x0 | TXQPAUSED<br>Transmit Queue in Pause<br>When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following:<br>1. Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled<br>2. Reception of 802.3x Pause packet when PFC is disabled<br>Values:<br>1'b0: Transmit Queue in Pause status is not detected<br>1'b1: Transmit Queue in Pause status is detected |

**GMAC_MTL_TxQ0_ETS_Status**

Address: Operational Base + offset (0x0d14)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RO | 0x0 | ABS<br>Average Bits per Slot<br>This field contains the average transmitted bits per slot. When the DCB operation is enabled for Queue 0, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680. |

**GMAC_MTL_TxQ0_Quantum_Weight**

Address: Operational Base + offset (0x0d18)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x000 | reserved |
| 20:0 | RW | 0x000000 | ISCQW<br>Quantum or Weights<br>When the DCB operation is enabled with DWRR algorithm for Queue 0 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes.<br>When DCB operation is enabled with WFQ algorithm for Queue 0 traffic, this field contains the weight for this queue.<br>The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. The higher the programmed weights lesser the bandwidth allocated for the particular Transmit Queue. This is because the weights are used to compute the packet finish time (weights*packet_size). Lesser the finish time, higher the probability of the packet getting scheduled first and using more bandwidth.<br>When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 0 traffic, this field contains the weight for this queue. The maximum value is 0x64.Bits [20:7] must be written to zero. |

**GMAC_MTL_Q0_Interrupt_Ctrl_Status**

Address: Operational Base + offset (0x0d2c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x00 | reserved |
| 24 | RW | 0x0 | RXOIE<br>Receive Queue Overflow Interrupt Enable<br>When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled.<br>Values:<br>1'b0: Receive Queue Overflow Interrupt is disabled<br>1'b1: Receive Queue Overflow Interrupt is enabled |
| 23:17 | RO | 0x00 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 16 | RW | 0x0 | RXOVFIS<br>Receive Queue Overflow Interrupt Status<br>This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit.<br>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.<br>Values:<br>1'b0: Receive Queue Overflow Interrupt Status not detected<br>1'b1: Receive Queue Overflow Interrupt Status detected |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | ABPSIE<br>Average Bits Per Slot Interrupt Enable<br>When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated.<br>When this bit is cleared, the interrupt is not asserted for such an event.<br>Values:<br>0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled<br>0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled |
| 8 | RW | 0x0 | TXUIE<br>Transmit Queue Underflow Interrupt Enable<br>When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled.<br>Values:<br>1'b0: Transmit Queue Underflow Interrupt Status is disabled<br>1'b1: Transmit Queue Underflow Interrupt Status is enabled |
| 7:2 | RO | 0x00 | reserved |
| 1 | RW | 0x0 | ABPSIS<br>Average Bits Per Slot Interrupt Status<br>When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br>Values:<br>0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected<br>0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected |
| 0 | RW | 0x0 | TXUNFIS<br>Transmit Queue Underflow Interrupt Status<br>This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit.<br>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.<br>Values:<br>1'b0: Transmit Queue Underflow Interrupt Status not detected<br>1'b1: Transmit Queue Underflow Interrupt Status detected |

**GMAC_MTL_RxQ0_Operation_Mode**

Address: Operational Base + offset (0x0d30)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:27 | RO | 0x00 | reserved |
| 26:20 | RW | 0x00 | RQS<br>Receive Queue Size<br>This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes.<br>When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value.<br>The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits |
| 19:14 | RW | 0x00 | RFD<br>Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes)<br>These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation:<br>0: Full minus 1 KB, that is, FULL 1 KB<br>1: Full minus 1.5 KB, that is, FULL 1.5 KB<br>2: Full minus 2 KB, that is, FULL 2 KB<br>3: Full minus 2.5 KB, that is, FULL 2.5 KB<br>...<br>62: Full minus 32 KB, that is, FULL 32 KB<br>63: Full minus 32.5 KB, that is, FULL 32.5 KB<br>The de-assertion is effective only after flow control is asserted.<br>Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only. |
| 13:8 | RW | 0x00 | RFA<br>Threshold for Activating Flow Control (in half-duplex and full-duplex)<br>These bits control the threshold (fill-level of Rx queue) at which the flow control is activated:For more information on encoding for this field, see RFD. |
| 7 | RW | 0x0 | EHFC<br>Enable Hardware Flow Control<br>When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled.<br>Values:<br>1'b0: Hardware Flow Control is disabled<br>1'b1: Hardware Flow Control is enabled |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | DIS_TCP_EF<br>Disable Dropping of TCP/IP Checksum Error Packets<br>When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset.<br>Values:<br>1'b0: Dropping of TCP/IP Checksum Error Packets is enabled<br>1'b1: Dropping of TCP/IP Checksum Error Packets is disabled |
| 5 | RW | 0x0 | RSF<br>Receive Queue Store and Forward<br>When this bit is set, the GMAC reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register.<br>Values:<br>1'b0: Receive Queue Store and Forward is disabled<br>1'b1: Receive Queue Store and Forward is enabled |
| 4 | RW | 0x0 | FEP<br>Forward Error Packets<br>When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped.<br>When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet may be forwarded to the application or DMA.<br>Values:<br>1'b0: Forward Error Packets is disabled<br>1'b1: Forward Error Packets is enabled |
| 3 | RW | 0x0 | FUP<br>Forward Undersized Good Packets<br>When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01.<br>Values:<br>1'b0: Forward Undersized Good Packets is disabled<br>1'b1: Forward Undersized Good Packets is enabled |
| 2 | RO | 0x0 | reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1:0 | RW | 0x0 | RTC<br>Receive Queue Threshold Control<br>These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. |

**GMAC_MTL_RxQ0_Miss_Pkt_Ovf_Cnt**

Address: Operational Base + offset (0x0d34)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27 | RO | 0x0 | MISCNTOVF<br>Missed Packet Counter Overflow Bit<br>When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: Missed Packet Counter overflow not detected<br>1'b1: Missed Packet Counter overflow detected |
| 26:16 | RO | 0x000 | MISPKTCNT<br>Missed Packet Counter<br>This field indicates the number of packets missed by the GMAC because the application asserted ari_pkt_flush_i[] for this queue. This counter is incremented each time the application issues ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. In EQOS-DMA, EQOS-AXI, and EQOS-AHB configurations, This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event. |
| 15:12 | RO | 0x0 | reserved |
| 11 | RO | 0x0 | OVFCNTOVF<br>Overflow Counter Overflow Bit<br>When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: Overflow Counter overflow not detected<br>1'b1: Overflow Counter overflow detected |
| 10:0 | RO | 0x000 | OVFPKTCNT<br>Overflow Packet Counter<br>This field indicates the number of packets discarded by the GMAC because of Receive queue overflow. This counter is incremented each time the GMAC discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**GMAC_MTL_RxQ0_Debug**

Address: Operational Base + offset (0x0d38)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:16 | RO | 0x0 | PRXQ<br>Number of Packets in Receive Queue<br>This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/Min_Packet_Size. |
| 15:6 | RO | 0x000 | reserved |
| 5:4 | RO | 0x0 | RXQSTS<br>MTL Rx Queue Fill-Level Status<br>This field gives the status of the fill-level of the Rx Queue:<br>Values:<br>2'b00: Rx Queue empty<br>2'b01: Rx Queue fill-level below flow-control deactivate threshold<br>2'b10: Rx Queue fill-level above flow-control activate threshold<br>2'b11: Rx Queue full |
| 3 | RO | 0x0 | reserved |
| 2:1 | RO | 0x0 | RRCSTS<br>MTL Rx Queue Read Controller State<br>This field gives the state of the Rx queue Read controller:<br>Values:<br>2'b00: Idle state<br>2'b01: Reading packet data<br>2'b10: Reading packet status (or timestamp)<br>2'b11: Flushing the packet data and status |
| 0 | RO | 0x0 | RWCSTS<br>MTL Rx Queue Write Controller Active Status<br>When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue.<br>Values:<br>1'b0: MTL Rx Queue Write Controller Active Status not detected<br>1'b1: MTL Rx Queue Write Controller Active Status detected |

**GMAC_MTL_RxQ0_Control**

Address: Operational Base + offset (0x0d3c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | RXQ_FRM_ARBIT<br>Receive Queue Packet Arbitration<br>When this bit is set, the GMAC drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue.<br>When this bit is reset, the GMAC drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue:<br>1.PBL amount of data (indicated by ari_qN_pbl_i[])<br>2.Complete data of a packet<br>The status and the timestamp are not a part of the PBL data. Therefore, the GMAC drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode).<br>Values:<br>0x0 (DISABLE): Receive Queue Packet Arbitration is disabled<br>0x1 (ENABLE): Receive Queue Packet Arbitration is enabled |
| 2:0 | RW | 0x0 | RXQ_WEGT<br>Receive Queue Weight<br>This field indicates the weight assigned to the Rx Queue 0. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. |

**GMAC_DMA_Mode**

Address: Operational Base + offset (0x1000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17:16 | RW | 0x0 | INTM<br>Interrupt Mode<br>This field defines the interrupt mode of GMAC. The behavior of the following outputs changes depending on the following settings:<br>1. sbd_perch_tx_intr_o[] (Transmit Per Channel Interrupt)<br>2. sbd_perch_rx_intr_o[] (Receive Per Channel Interrupt)<br>3. sbd_intr_o (Common Interrupt)<br>It also changes the behavior of the RI/TI bits in the DMA_CH0_Status.<br>2'b00: sbd_perch_* are pulse signals for each TX/RX packet transfer completion events (irrespective of whether corresponding interrupts are enabled) for which IOC bits are enabled in descriptor. sbd_intr_o is also asserted when corresponding interrupts are enabled and cleared only when software clears the corresponding RI/TI status bits.<br>2'b01: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events.<br>2'b10: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. However, the signal is asserted again if the same event occurred again before it was cleared. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events.<br>2'b11: Reserved<br>Values:<br>2'b00: See above description<br>2'b01: See above description<br>2'b10: See above description<br>2'b11: Reserved |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | DSPW<br>Descriptor Posted Write<br>When this bit is set to 0, the descriptor writes are always non-posted.<br>When this bit is set to 1, the descriptor writes are non-posted only when IOC (Interrupt on completion) is set in last descriptor, otherwise the descriptor writes are always posted.<br>Values:<br>1'b0: Descriptor Posted Write is disabled<br>1'b1: Descriptor Posted Write is enabled |
| 7:1 | RO | 0x00 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | SWR<br>Software Reset<br>When this bit is set, the MAC and the DMA controller reset the logic and all internal registers of the DMA, MTL, and MAC. This bit is automatically cleared after the reset operation is complete in all GMAC clock domains. Before reprogramming any GMAC register, a value of zero should be read in this bit. This bit must be read at least 4 CSR clock cycles after it is written to 1.<br>Note: The reset operation is complete only when all resets in all active clock domains are de-asserted. Therefore, it is essential that all PHY inputs clocks (applicable for the selected PHY interface) are present for software reset completion. The time to complete the software reset operation depends on the frequency of the slowest active clock.<br>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.<br>Values:<br>1'b0: Software Reset is disabled<br>1'b1: Software Reset is enabled |

**GMAC_DMA_SysBus_Mode**

Address: Operational Base + offset (0x1004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | EN_LPI<br>Enable Low Power Interface (LPI)<br>When set to 1, this bit enables the LPI mode supported by the EQOS-AXI configuration and accepts the LPI request from the AXI System Clock controller.<br>When set to 0, this bit disables the LPI mode and always denies the LPI request from the AXI System Clock controller.<br>Values:<br>1'b0: Low Power Interface (LPI) is disabled<br>1'b1: Low Power Interface (LPI) is enabled |
| 30 | RW | 0x0 | LPI_XIT_PKT<br>Unlock on Magic Packet or Remote Wake-Up Packet<br>When set to 1, this bit enables the AXI master to come out of the LPI mode only when the magic packet or remote wake-up packet is received. When set to 0, this bit enables the AXI master to come out of the LPI mode when any packet is received.<br>Values:<br>1'b0: Unlock on Magic Packet or Remote Wake-Up Packet is disabled<br>1'b1: Unlock on Magic Packet or Remote Wake-Up Packet is enabled |
| 29:26 | RO | 0x0 | reserved |
| 25:24 | RW | 0x0 | WR_OSR_LMT<br>AXI Maximum Write Outstanding Request Limit<br>This value limits the maximum outstanding request on the AXI write interface. Maximum outstanding requests = WR_OSR_LMT + 1<br>Note:<br>1. Bit 26 is reserved if GMAC_AXI_MAX-_WR_REQ = 4<br>2. Bit 27 is reserved if GMAC_AXI_MAX-_WR_REQ!= 16 |
| 23:19 | RO | 0x00 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 18:16 | RW | 0x1 | RD_OSR_LMT<br>AXI Maximum Read Outstanding Request Limit<br>This value limits the maximum outstanding request on the AXI read interface. Maximum outstanding requests = RD_OSR_LMT + 1<br>Note:<br>1. Bit 18 is reserved if parameter GMAC_AXI_-MAX_RD_REQ = 4<br>2. Bit 19 is reserved if parameter GMAC_AXI_-MAX_RD_REQ!= 16 |
| 15:13 | RO | 0x0 | reserved |
| 12 | RW | 0x0 | AAL<br>Address-Aligned Beats<br>When this bit is set to 1, the EQOS-AXI or EQOS-AHB master performs address-aligned burst transfers on Read and Write channels.<br>Values:<br>1'b0: Address-Aligned Beats is disabled<br>1'b1: Address-Aligned Beats is enabled |
| 11 | RO | 0x0 | reserved |
| 10 | RW | 0x0 | AALE<br>Automatic AXI LPI enable<br>When set to 1, enables the AXI master to enter into LPI state when there is no activity in the GMAC for number of system clock cycles programmed in the LPIEI field of AXI_LPI_Entry_Interval register.<br>Values:<br>1'b0: Automatic AXI LPI is disabled<br>1'b1: Automatic AXI LPI is enabled |
| 9:4 | RO | 0x00 | reserved |
| 3 | RW | 0x0 | BLEN16<br>AXI Burst Length 16<br>When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 16 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect.<br>Values:<br>1'b0: No effect<br>1'b1: AXI Burst Length 16 |
| 2 | RW | 0x0 | BLEN8<br>AXI Burst Length 8<br>When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 8 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect.<br>Values:<br>1'b0: No effect<br>1'b1: AXI Burst Length 8 |
| 1 | RW | 0x0 | BLEN4<br>AXI Burst Length 4<br>When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 4 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect.<br>Values:<br>1'b0: No effect<br>1'b1: AXI Burst Length 4 |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | FB<br>Fixed Burst Length<br>When this bit is set to 1, the EQOS-AXI master initiates burst transfers of specified lengths as given below.<br>1. Burst transfers of fixed burst lengths as indicated by the BLEN256, BLEN128, BLEN64, BLEN32, BLEN16, BLEN8, or BLEN4 field<br>2. Burst transfers of length 1<br>When this bit is set to 0, the EQOS-AXI master initiates burst transfers that are equal to or less than the maximum allowed burst length programmed in Bits[7:1].<br>Values:<br>1'b0: Fixed Burst Length is disabled<br>1'b1: Fixed Burst Length is enabled |

**GMAC_DMA_Interrupt_Status**

Address: Operational Base + offset (0x1008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17 | RO | 0x0 | MACIS<br>MAC Interrupt Status<br>This bit indicates an interrupt event in the MAC. To reset this bit to 1'b0, the software must read the corresponding register in the MAC to get the exact cause of the interrupt and clear its source.<br>Values:<br>1'b0: MAC Interrupt Status not detected<br>1'b1: MAC Interrupt Status detected |
| 16 | RO | 0x0 | MTLIS<br>MTL Interrupt Status<br>This bit indicates an interrupt event in the MTL. To reset this bit to 1'b0, the software must read the corresponding register in the MTL to get the exact cause of the interrupt and clear its source.<br>Values:<br>1'b0: MTL Interrupt Status not detected<br>1'b1: MTL Interrupt Status detected |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RO | 0x0 | DC0IS<br>DMA Channel 0 Interrupt Status<br>This bit indicates an interrupt event in DMA Channel 0. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 0 to get the exact cause of the interrupt and clear its source.<br>Values:<br>1'b0: DMA Channel 0 Interrupt Status not detected<br>1'b1: DMA Channel 0 Interrupt Status detected |

**GMAC_DMA_Debug_Status0**

Address: Operational Base + offset (0x100c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:20 | RO | 0x0 | TPS1<br>DMA Channel 1 Transmit Process State<br>This field indicates the Tx DMA FSM state for Channel 1. The MSB of this field always returns 0. This field does not generate an interrupt.<br>Values:<br>0x0 (STOP): Stopped (Reset or Stop Transmit Command issued)<br>0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor)<br>0x2 (RUN_WS): Running (Waiting for status)<br>0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO))<br>0x4 (TSTMP_WS): Timestamp write state<br>0x5 (Reserved): Reserved for future use<br>0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow)<br>0x7 (RUN_CTD): Running (Closing Tx Descriptor) |
| 19:16 | RO | 0x0 | RPS1<br>DMA Channel 1 Receive Process State<br>This field indicates the Rx DMA FSM state for Channel 1. The MSB of this field always returns 0. This field does not generate an interrupt.<br>Values:<br>0x0 (STOP): Stopped (Reset or Stop Receive Command issued)<br>0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor)<br>0x2 (Reserved): Reserved for future use<br>0x3 (RUN_WRP): Running (Waiting for Rx packet)<br>0x4 (SUSPND): Suspended (Rx Descriptor Unavailable)<br>0x5 (RUN_CRD): Running (Closing the Rx Descriptor)<br>0x6 (TSTMP): Timestamp write state<br>0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory) |
| 15:12 | RO | 0x0 | TPS0<br>DMA Channel 0 Transmit Process State<br>This field indicates the Tx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt.<br>Values:<br>4'b0000: Stopped (Reset or Stop Transmit Command issued)<br>4'b0001: Running (Fetching Tx Transfer Descriptor)<br>4'b0010: Running (Waiting for status)<br>4'b0011: Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO))<br>4'b0100: Timestamp write state<br>4'b0101: Reserved for future use<br>4'b0110: Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow)<br>4'b0111: Running (Closing Tx Descriptor) |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:8 | RO | 0x0 | RPS0<br>DMA Channel 0 Receive Process State<br>This field indicates the Rx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt.<br>Values:<br>4'b0000: Stopped (Reset or Stop Receive Command issued)<br>4'b0001: Running (Fetching Rx Transfer Descriptor)<br>4'b0010: Reserved for future use<br>4'b0011: Running (Waiting for Rx packet)<br>4'b0100: Suspended (Rx Descriptor Unavailable)<br>4'b0101: Running (Closing the Rx Descriptor)<br>4'b0110: Timestamp write state<br>4'b0111: Running (Transferring the received packet data from the Rx buffer to the system memory) |
| 7:2 | RO | 0x00 | reserved |
| 1 | RO | 0x0 | AXRHSTS<br>AXI Master Read Channel Status<br>When high, this bit indicates that the read channel of the AXI master is active, and it is transferring the data.<br>Values:<br>1'b0: AXI Master Read Channel Status not detected<br>1'b1: AXI Master Read Channel Status detected |
| 0 | RO | 0x0 | AXWHSTS<br>AXI Master Write Channel or AHB Master Status<br>EQOS-AXI Configuration:<br>When high, this bit indicates that the write channel of the AXI master is active, and it is transferring data.<br>EQOS-AHB Configuration:<br>When high, this bit indicates that the AHB master FSMs are in the non-idle state.<br>Values:<br>1'b0: AXI Master Write Channel or AHB Master Status not detected<br>1'b1: AXI Master Write Channel or AHB Master Status detected |

**GMAC_AXI_LPI_Entry_Interval**

Address: Operational Base + offset (0x1040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3:0 | RW | 0x0 | LPIEI<br>LPI Entry Interval<br>Contains the number of system clock cycles, multiplied by 64, to wait for an activity in the GMAC to enter into the AXI low power state. 0 indicates 64 clock cycles. |

**GMAC_DMA_TBS_CTRL**

Address: Operational Base + offset (0x1050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RW | 0x000000 | FTOS<br>Fetch Time Offset<br>The value in units of 256 nanoseconds, that has to be deducted from the Launch time to compute the Fetch Time. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x0 | FGOS<br>Fetch GSN Offset<br>The number GSN slots that must be deducted from the Launch GSN to compute the Fetch GSN. Value valid only when FTOV is set. |
| 3:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | FTOV<br>Fetch Time Offset Valid<br>When set indicates the FTOS field is valid. When not set, indicates the Fetch Offset is not valid and the DMA engine can fetch the frames from host memory without any time restrictions.<br>Values:<br>0x0 (INVALID): Fetch Time Offset is invalid<br>0x1 (VALID): Fetch Time Offset is valid |

**GMAC_DMA_CH0_Control**

Address: Operational Base + offset (0x1100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x000 | reserved |
| 20:18 | RW | 0x0 | DSL<br>Descriptor Skip Length<br>This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor.<br>When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous. |
| 17 | RO | 0x0 | reserved |
| 16 | RW | 0x0 | PBLx8<br>8xPBL mode<br>When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH0_Tx_Control and Bits[21:16] in DMA_CH0_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value.<br>0x0 (DISABLE): 8xPBL mode is disabled<br>0x1 (ENABLE): 8xPBL mode is enabled |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | MSS<br>Maximum Segment Size<br>This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH0_Tx_Control register is set.<br>The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more. |

**GMAC_DMA_CH0_Tx_Control**

Address: Operational Base + offset (0x1104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 21:16 | RW | 0x00 | TxPBL<br>Transmit Programmable Burst Length<br>These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior.<br>To transfer more than 32 beats, perform the following steps:<br>1. Set the 8xPBL mode in DMA_CH0_Control register.<br>2. Set the TxPBL.<br>Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ[n]_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32. |
| 15 | RW | 0x0 | IPBL<br>Ignore PBL Requirement<br>When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL may use handshaking to slow the DMA.<br>Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it may block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer.<br>0x0 (DISABLE): Ignore PBL Requirement is disabled<br>0x1 (ENABLE): Ignore PBL Requirement is enabled |
| 14:13 | RW | 0x0 | TSE_MODE<br>TSE Mode<br>00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation.<br>01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets.<br>10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets.<br>11: Reserved<br><br>0x0 (TSO_USO): TSO/USO<br>0x1 (UFOWC): UFO with Checksum<br>0x2 (UFOWOC): UFO without Checksum<br>0x3 (Reserved): Reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | TSE<br>TCP Segmentation Enabled<br>When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4.<br>0x0 (DISABLE): TCP Segmentation is disabled<br>0x1 (ENABLE): TCP Segmentation is enabled |
| 11:5 | RO | 0x00 | reserved |
| 4 | RW | 0x0 | OSF<br>Operate on Second Packet<br>When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained.<br>0x0 (DISABLE): Operate on Second Packet disabled<br>0x1 (ENABLE): Operate on Second Packet enabled |
| 3:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | ST<br>Start or Stop Transmission Command<br>When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted.<br>The DMA tries to acquire descriptor from either of the following positions:<br>1.The current position in the list<br>This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register.<br>2.The position at which the transmission was previously stopped<br><br>If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable.<br>When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state.<br>0x0 (STOP): Stop Transmission Command<br>0x1 (START): Start Transmission Command |

**GMAC_DMA_CH0_Rx_Control**

Address: Operational Base + offset (0x1108)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | RPF<br>Rx Packet Flush<br>When this bit is set to 1, then GMAC automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue.<br>When this bit is set to 0, the GMAC not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This may in turn cause head-of-line blocking in the corresponding RxQueue.<br>0x0 (DISABLE): Rx Packet Flush is disabled<br>0x1 (ENABLE): Rx Packet Flush is enabled |
| 30:22 | RO | 0x000 | reserved |
| 21:16 | RW | 0x00 | RxPBL<br>Receive Programmable Burst Length<br>These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior.<br>To transfer more than 32 beats, perform the following steps:<br>1. Set the 8xPBL mode in the DMA_CH0_Control register.<br>2. Set the RxPBL.<br>Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ[n]_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32. |
| 15 | RO | 0x0 | reserved |
| 14:4 | RW | 0x000 | RBSZ_13_y<br>Receive Buffer size High<br>RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_3_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled.<br><br>Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_3_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width). |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:1 | RO | 0x0 | RBSZ_3_0<br>Receive Buffer size Low<br>RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_3_0. The RBSZ_3_0 is the lower field whose width is based on data bus width of the configuration.<br>This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO). |
| 0 | RW | 0x0 | SR<br>Start or Stop Receive<br>When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets.The DMA tries to acquire descriptor from either of the following positions:<br>1.The current position in the list<br>This is the address set by the DMA_CH0_RxDesc_List_Address register.<br>2.The position at which the Rx process was previously stopped<br>If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable.<br>When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state.<br>0x0 (STOP): Stop Receive<br>0x1 (START): Start Receive |

**GMAC_DMA_CH0_TxDesc_List_Address**

Address: Operational Base + offset (0x1114)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RW | 0x00000000 | TDESLA<br>Start of Transmit List<br>This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO).<br>The width of this field depends on the configuration:<br>31:2 for 32-bit configuration<br>31:3 for 64-bit configuration<br>31:4 for 128-bit configuration |

**GMAC_DMA_CH0_RxDesc_List_Address**

Address: Operational Base + offset (0x111c)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RW | 0x00000000 | RDESLA<br>Start of Receive List<br>This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO).<br>The width of this field depends on the configuration:<br>31:2 for 32-bit configuration<br>31:3 for 64-bit configuration<br>31:4 for 128-bit configuration |

**GMAC_DMA_CH0_TxDesc_Tail_Pointer**

Address: Operational Base + offset (0x1120)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RW | 0x00000000 | TDTP<br>Transmit Descriptor Tail Pointer<br>This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers.<br>The width of this field depends on the configuration:<br>31:2 for 32-bit configuration<br>31:3 for 64-bit configuration<br>31:4 for 128-bit configuration |

**GMAC_DMA_CH0_RxDesc_Tail_Pointer**

Address: Operational Base + offset (0x1128)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RW | 0x00000000 | RDRT<br>Receive Descriptor Tail Pointer<br>This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers.<br>The width of this field depends on the configuration:<br>31:2 for 32-bit configuration<br>31:3 for 64-bit configuration<br>31:4 for 128-bit configuration |

**GMAC_DMA_CH0_TxDesc_Ring_Length**

Address: Operational Base + offset (0x112c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9:0 | RW | 0x000 | TDRL<br>Transmit Descriptor Ring Length<br>This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. we recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**GMAC_DMA_CH0_RxDesc_Ring_Length**

Address: Operational Base + offset (0x1130)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9:0 | RW | 0x000 | RDRL<br>Receive Descriptor Ring Length<br>This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9. |

**GMAC_DMA_CH0_Interrupt_Enable**

Address: Operational Base + offset (0x1134)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15 | RW | 0x0 | NIE<br>Normal Interrupt Summary Enable<br>When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register:<br>Bit 0: Transmit Interrupt<br>Bit 2: Transmit Buffer Unavailable<br>Bit 6: Receive Interrupt<br>Bit 11: Early Receive Interrupt<br>When this bit is reset, the normal interrupt summary is disabled.<br>0x0 (DISABLE): Normal Interrupt Summary is disabled<br>0x1 (ENABLE): Normal Interrupt Summary is enabled |
| 14 | RW | 0x0 | AIE<br>Abnormal Interrupt Summary Enable<br>When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register:<br>Bit 1: Transmit Process Stopped<br>Bit 7: Rx Buffer Unavailable<br>Bit 8: Receive Process Stopped<br>Bit 9: Receive Watchdog Timeout<br>Bit 10: Early Transmit Interrupt<br>Bit 12: Fatal Bus Error<br>Bit 13: Context Descriptor Error<br>When this bit is reset, the abnormal interrupt summary is disabled.<br>0x0 (DISABLE): Abnormal Interrupt Summary is disabled<br>0x1 (ENABLE): Abnormal Interrupt Summary is enabled |
| 13 | RW | 0x0 | CDEE<br>Context Descriptor Error Enable<br>When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled.<br>0x0 (DISABLE): Context Descriptor Error is disabled<br>0x1 (ENABLE): Context Descriptor Error is enabled |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | FBEE<br>Fatal Bus Error Enable<br>When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled.<br>0x0 (DISABLE): Fatal Bus Error is disabled<br>0x1 (ENABLE): Fatal Bus Error is enabled |
| 11 | RW | 0x0 | ERIE<br>Early Receive Interrupt Enable<br>When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled.<br>0x0 (DISABLE): Early Receive Interrupt is disabled<br>0x1 (ENABLE): Early Receive Interrupt is enabled |
| 10 | RW | 0x0 | ETIE<br>Early Transmit Interrupt Enable<br>When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled.<br>0x0 (DISABLE): Early Transmit Interrupt is disabled<br>0x1 (ENABLE): Early Transmit Interrupt is enabled |
| 9 | RW | 0x0 | RWTE<br>Receive Watchdog Timeout Enable<br>When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled.<br>0x0 (DISABLE): Receive Watchdog Timeout is disabled<br>0x1 (ENABLE): Receive Watchdog Timeout is enabled |
| 8 | RW | 0x0 | RSE<br>Receive Stopped Enable<br>When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. |
| 7 | RW | 0x0 | RBUE<br>Receive Buffer Unavailable Enable<br>When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled.<br>0x0 (DISABLE): Receive Buffer Unavailable is disabled<br>0x1 (ENABLE): Receive Buffer Unavailable is enabled |
| 6 | RW | 0x0 | RIE<br>Receive Interrupt Enable<br>When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled.<br>0x0 (DISABLE): Receive Interrupt is disabled<br>0x1 (ENABLE): Receive Interrupt is enabled |
| 5:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | TBUE<br>Transmit Buffer Unavailable Enable<br>When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled.<br>0x0 (DISABLE): Transmit Buffer Unavailable is disabled<br>0x1 (ENABLE): Transmit Buffer Unavailable is enabled |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | TXSE<br>Transmit Stopped Enable<br>When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled.<br>0x0 (DISABLE): Transmit Stopped is disabled<br>0x1 (ENABLE): Transmit Stopped is enabled |
| 0 | RW | 0x0 | TIE<br>Transmit Interrupt Enable<br>When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled.<br>0x0 (DISABLE): Transmit Interrupt is disabled<br>0x1 (ENABLE): Transmit Interrupt is enabled |

**GMAC_DMA_CH0_Rx_Interrupt_WD_Timer**

Address: Operational Base + offset (0x1138)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17:16 | RW | 0x0 | RWTU<br>Receive Interrupt Watchdog Timer Count Units<br>This fields indicates the number of system clock cycles corresponding to one unit in RWT field.<br>2'b00: 256<br>2'b01: 512<br>2'b10: 1024<br>2'b11: 2048<br>For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles. |
| 15:8 | RO | 0x00 | reserved |
| 7:0 | RW | 0x00 | RWT<br>Receive Interrupt Watchdog Timer Count<br>This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set.<br>The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30].<br>When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet. |

**GMAC_DMA_CH0_Slot_Func_Ctrl_Status**

Address: Operational Base + offset (0x113c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:16 | RO | 0x0 | RSN<br>Reference Slot Number<br>This field gives the current value of the reference slot number in the DMA. It is used for slot comparison. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:4 | RW | 0x07c | SIV<br>Slot Interval Value<br>This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us. |
| 3:2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | ASC<br>Advance Slot Check<br>When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is<br>1.equal to the reference slot number given in the RSN field<br>2.ahead of the reference slot number by up to two slots<br>This bit is applicable only when the ESC bit is set.<br>Values:<br>0x0 (DISABLE): Advance Slot Check is disabled<br>0x1 (ENABLE): Advance Slot Check is |
| 0 | RW | 0x0 | ESC<br>Enable Slot Comparison<br>When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is<br>1.equal to the reference slot number<br>2.ahead of the reference slot number by one slot<br>When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed.<br>Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets.<br>Values:<br>0x0 (DISABLE): Slot Comparison is disabled<br>0x1 (ENABLE): Slot Comparison is enabled |

**GMAC_DMA_CH0_Current_App_TxDesc**

Address: Operational Base + offset (0x1144)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | CURTDESAPTR<br>Application Transmit Descriptor Address Pointer<br>The DMA updates this pointer during Tx operation. This pointer is cleared on reset. |

**GMAC_DMA_CH0_Current_App_RxDesc**

Address: Operational Base + offset (0x114c)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | CURRDESAPTR<br>Application Receive Descriptor Address Pointer<br>The DMA updates this pointer during Rx operation. This pointer is cleared on reset. |

**GMAC_DMA_CH0_Current_App_TxBuffer**

Address: Operational Base + offset (0x1154)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | CURTBUFAPTR<br>Application Transmit Buffer Address Pointer<br>The DMA updates this pointer during Tx operation. This pointer is cleared on reset. |

**GMAC_DMA_CH0_Current_App_RxBuffer**

Address: Operational Base + offset (0x115c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | CURRBUFAPTR<br>Application Receive Buffer Address Pointer<br>The DMA updates this pointer during Rx operation. This pointer is cleared on reset. |

**GMAC_DMA_CH0_Status**

Address: Operational Base + offset (0x1160)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:19 | RO | 0x0 | REB<br>Rx DMA Error Bits<br>This field indicates the type of error that caused a Bus Error.<br>For example, error response on the AHB or AXI interface.<br>1.Bit 21<br>1'b1: Error during data transfer by Rx DMA<br>1'b0: No Error during data transfer by Rx DMA<br>2.Bit 20<br>1'b1: Error during descriptor access<br>1'b0: Error during data buffer access<br>3.Bit 19<br>1'b1: Error during read transfer<br>1'b0: Error during write transfer<br>This field is valid only when the FBE bit is set. This field does not generate an interrupt. |
| 18:16 | RO | 0x0 | TEB<br>Tx DMA Error Bits<br>This field indicates the type of error that caused a Bus Error.<br>For example, error response on the AHB or AXI interface.<br>1.Bit 18<br>1'b1: Error during data transfer by Tx DMA<br>1'b0: No Error during data transfer by Tx DMA<br>2.Bit 17<br>1'b1: Error during descriptor access<br>1'b0: Error during data buffer access<br>3.Bit 16<br>1'b1: Error during read transfer<br>1'b0: Error during write transfer<br>This field is valid only when the FBE bit is set. This field does not generate an interrupt. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x0 | NIS<br>Normal Interrupt Summary<br>Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register:<br>Bit 0: Transmit Interrupt<br>Bit 2: Transmit Buffer Unavailable<br>Bit 6: Receive Interrupt<br>Bit 11: Early Receive Interrupt<br>Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit.<br>This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Normal Interrupt Summary status not detected<br>0x1 (ACTIVE): Normal Interrupt Summary status detected |
| 14 | RW | 0x0 | AIS<br>Abnormal Interrupt Summary<br>Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register:<br>Bit 1: Transmit Process Stopped<br>Bit 7: Receive Buffer Unavailable<br>Bit 8: Receive Process Stopped<br>Bit 10: Early Transmit Interrupt<br>Bit 12: Fatal Bus Error<br>Bit 13: Context Descriptor Error<br>Only unmasked bits affect the Abnormal Interrupt Summary bit.<br>This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br>0x0 (INACTIVE): Abnormal Interrupt Summary status not detected<br>0x1 (ACTIVE): Abnormal Interrupt Summary status |
| 13 | RW | 0x0 | CDE<br>Context Descriptor Error<br>This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow ( intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Context Descriptor Error status not detected<br>0x1 (ACTIVE): Context Descriptor Error status detected |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | FBE<br>Fatal Bus Error<br>This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Fatal Bus Error status not detected<br>0x1 (ACTIVE): Fatal Bus Error status detected |
| 11 | RW | 0x0 | ERI<br>Early Receive Interrupt<br>This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer.The setting of RI bit automatically clears this bit.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Early Receive Interrupt status not detected<br>0x1 (ACTIVE): Early Receive Interrupt status detected |
| 10 | RW | 0x0 | ETI<br>Early Transmit Interrupt<br>This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL.<br>When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Early Transmit Interrupt status not detected<br>0x1 (ACTIVE): Early Transmit Interrupt status detected |
| 9 | RW | 0x0 | RWT<br>Receive Watchdog Timeout<br>This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received.<br><br>0x0 (INACTIVE): Receive Watchdog Timeout status not detected<br>0x1 (ACTIVE): Receive Watchdog Timeout status detected |
| 8 | RW | 0x0 | RPS<br>Receive Process Stopped<br>This bit is asserted when the Rx process enters the Stopped state.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Receive Process Stopped status not detected<br>0x1 (ACTIVE): Receive Process Stopped status detected |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x0 | RBU<br>Receive Buffer Unavailable<br>This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor.<br>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Receive Buffer Unavailable status not detected<br>0x1 (ACTIVE): Receive Buffer Unavailable status detected |
| 6 | RW | 0x0 | RI<br>Receive Interrupt<br>This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor.<br>The reception remains in the Running state.<br>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Receive Interrupt status not detected<br>0x1 (ACTIVE): Receive Interrupt status detected |
| 5:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | TBU<br>Transmit Buffer Unavailable<br>This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it.<br>Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions.<br>To resume processing the Transmit descriptors, the application should do the following:<br>1. Change the ownership of the descriptor by setting Bit 31 of TDES3.<br>2. Issue a Transmit Poll Demand command.<br>For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Transmit Buffer Unavailable status not detected<br>0x1 (ACTIVE): Transmit Buffer Unavailable status |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | TPS<br>Transmit Process Stopped<br>This bit is set when the transmission is stopped.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Transmit Process Stopped status not detected<br>0x1 (ACTIVE): Transmit Process Stopped status detected |
| 0 | RW | 0x0 | TI<br>Transmit Interrupt<br>This bit indicates that the packet transmission is complete.<br>When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Transmit Interrupt status not detected<br>0x1 (ACTIVE): Transmit Interrupt status detected |

**GMAC_DMA_CH0_Miss_Frame_Cnt**

Address: Operational Base + offset (0x1164)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15 | RO | 0x0 | MFC0<br>Overflow status of the MFC Counter<br>When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br><br>0x0 (INACTIVE): Miss Frame Counter overflow not occurred<br>0x1 (ACTIVE): Miss Frame Counter overflow occurred |
| 14:11 | RO | 0x0 | reserved |
| 10:0 | RO | 0x000 | MFC<br>Dropped Packet Counters<br>This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH$i_Rx_Control register.<br>The counter gets cleared when this register is read.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event. |

**GMAC_DMA_CH0_RX_ERI_Cnt**

Address: Operational Base + offset (0x1168)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RO | 0x0 | ECNT<br>ERI Counter<br>When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter will get reset at the start of new packet. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**GMAC_MAC_Address1_High**

Address: Operational Base + offset (0x0308)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | AE<br>Address Enable<br>This bit is always set to 1.<br>Values:<br>1'b0: This bit must be always set to 1<br>1'b1: This bit is always set to 1 |
| 30 | RW | 0x0 | SA<br>Source Address<br>When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet.<br>Values:<br>0x0 (DA): Compare with Destination Address<br>0x1 (SA): Compare with Source Address |
| 29:24 | RW | 0x00 | MBC<br>Mask Byte Control<br>These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows:<br>Bit 29: MAC_Address1_High[15:8]<br>Bit 28: MAC_Address1_High[7:0]<br>Bit 27: MAC_Address1_Low[31:24]<br>...<br>Bit 24: MAC_Address1_Low[7:0]<br>You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address. |
| 23:17 | RO | 0x00 | reserved |
| 16 | RW | 0x0 | DCS<br>DMA Channel Select<br>If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address1 content is routed.<br>If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address1 content is routed. |
| 15:0 | RW | 0xffff | ADDRHI<br>MAC Address1[47:32]<br>This field contains the upper 16 bits [47:32] of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets. |

**GMAC_MAC_Address1_Low**

Address: Operational Base + offset (0x030c)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0xffffffff | ADDRLO<br>MAC Address1[31:0]<br>This field contains the lower 32 bits of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets. |

**GMAC_MAC_Address2_High**

Address: Operational Base + offset (0x0310)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | AE<br>Address Enable<br>This bit is always set to 1.<br>Values:<br>1'b0: This bit must be always set to 1<br>1'b1: This bit is always set to 1 |
| 30 | RW | 0x0 | SA<br>Source Address<br>When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet.<br>Values:<br>0x0 (DA): Compare with Destination Address<br>0x1 (SA): Compare with Source Address |
| 29:24 | RW | 0x00 | MBC<br>Mask Byte Control<br>These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows:<br>Bit 29: MAC_Address2_High[15:8]<br>Bit 28: MAC_Address2_High[7:0]<br>Bit 27: MAC_Address2_Low[31:24]<br>...<br>Bit 24: MAC_Address2_Low[7:0]<br>You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address. |
| 23:17 | RO | 0x00 | reserved |
| 16 | RW | 0x0 | DCS<br>DMA Channel Select<br>If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address1 content is routed.<br>If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address1 content is routed. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0xffff | ADDRHI<br>MAC Address2[47:32]<br>This field contains the upper 16 bits [47:32] of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets. |

**GMAC_MAC_Address2_Low**

Address: Operational Base + offset (0x0314)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0xffffffff | ADDRLO<br>MAC Address2[31:0]<br>This field contains the lower 32 bits of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets. |

**GMAC_MAC_Address3_High**

Address: Operational Base + offset (0x0318)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | AE<br>Address Enable<br>This bit is always set to 1.<br>Values:<br>1'b0: This bit must be always set to 1<br>1'b1: This bit is always set to 1 |
| 30 | RW | 0x0 | SA<br>Source Address<br>When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet.<br>Values:<br>0x0 (DA): Compare with Destination Address<br>0x1 (SA): Compare with Source Address |
| 29:24 | RW | 0x00 | MBC<br>Mask Byte Control<br>These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows:<br>Bit 29: MAC_Address3_High[15:8]<br>Bit 28: MAC_Address3_High[7:0]<br>Bit 27: MAC_Address3_Low[31:24]<br>...<br>Bit 24: MAC_Address3_Low[7:0]<br>You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address. |
| 23:17 | RO | 0x00 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 16 | RW | 0x0 | DCS<br>DMA Channel Select<br>If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address1 content is routed.<br>If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address1 content is routed. |
| 15:0 | RW | 0xffff | ADDRHI<br>MAC Address3[47:32]<br>This field contains the upper 16 bits [47:32] of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets. |

**GMAC_MAC_Address3_Low**

Address: Operational Base + offset (0x031c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0xffffffff | ADDRLO<br>MAC Address3[31:0]<br>This field contains the lower 32 bits of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets. |

**GMAC_MAC_L3_L4_Control1**

Address: Operational Base + offset (0x0930)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28 | RW | 0x0 | DMCHEN0<br>DMA Channel Select Enable<br>When set, this bit enables the selection of the DMA channel number for the packet that is passed by this L3_L4 filter. The DMA channel is indicated by the DMCHN bits. When this bit is reset, the DMA channel is not decided by this filter.<br>Values:<br>0x0 (DISABLE): DMA Channel Select is disabled<br>0x1 (ENABLE): DMA Channel Select is enabled |
| 27:25 | RO | 0x0 | reserved |
| 24 | RW | 0x0 | DMCHN0<br>DMA Channel Number<br>When DMCHEN is set high, this field selects the DMA Channel number to which the packet passed by this filter is routed. The width of this field depends on the number of the DMA channels present in your configuration. |
| 23:22 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 21 | RW | 0x0 | L4DPIM0<br>Layer 4 Destination Port Inverse Match Enable<br>When this bit is set, the Layer 4 Destination Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Destination Port number field is enabled for perfect matching.<br>This bit is valid and applicable only when the L4DPM0 bit is set high.<br>Values:<br>0x0 (DISABLE): Layer 4 Destination Port Inverse Match is disabled<br>0x1 (ENABLE): Layer 4 Destination Port Inverse Match is enabled |
| 20 | RW | 0x0 | L4DPM0<br>Layer 4 Destination Port Match Enable<br>When this bit is set, the Layer 4 Destination Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Destination Port number field for matching.<br>Values:<br>0x0 (DISABLE): Layer 4 Destination Port Match is disabled<br>0x1 (ENABLE): Layer 4 Destination Port Match is enabled |
| 19 | RW | 0x0 | L4SPIM0<br>Layer 4 Source Port Inverse Match Enable<br>When this bit is set, the Layer 4 Source Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Source Port number field is enabled for perfect matching.<br>This bit is valid and applicable only when the L4SPM0 bit is set high.<br>Values:<br>0x0 (DISABLE): Layer 4 Source Port Inverse Match is disabled<br>0x1 (ENABLE): Layer 4 Source Port Inverse Match is enabled |
| 18 | RW | 0x0 | L4SPM0<br>Layer 4 Source Port Match Enable<br>When this bit is set, the Layer 4 Source Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Source Port number field for matching.<br>Values:<br>0x0 (DISABLE): Layer 4 Source Port Match is disabled<br>0x1 (ENABLE): Layer 4 Source Port Match is enabled |
| 17 | RO | 0x0 | reserved |
| 16 | RW | 0x0 | L4PEN0<br>Layer 4 Protocol Enable<br>When this bit is set, the Source and Destination Port number fields of UDP packets are used for matching. When this bit is reset, the Source and Destination Port number fields of TCP packets are used for matching.<br>The Layer 4 matching is done only when the L4SPM0 or L4DPM0 bit is set.<br>Values:<br>0x0 (DISABLE): Layer 4 Protocol is disabled<br>0x1 (ENABLE): Layer 4 Protocol is enabled |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:11 | RW | 0x00 | L3HDBM0<br>Layer 3 IP DA Higher Bits Match<br>IPv4 Packets:<br>This field contains the number of higher bits of IP Destination Address that are matched in the IPv4 packets. The following list describes the values of this field:<br>0: No bits are masked.<br>1: LSb[0] is masked<br>2: Two LSbs [1:0] are masked<br>..<br>31: All bits except MSb are masked.<br>IPv6 Packets:<br>Bits[12:11] of this field correspond to Bits[6:5] of L3HSBM0 which indicate the number of lower bits of IP Source or Destination Address that are masked in the IPv6 packets. The following list describes the concatenated values of the L3HDBM0[1:0] and L3HSBM0 bits:<br>0: No bits are masked.<br>1: LSb[0] is masked.<br>2: Two LSbs [1:0] are masked<br>..<br>127: All bits except MSb are masked.<br>This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set. |
| 10:6 | RW | 0x00 | L3HSBM0<br>Layer 3 IP SA Higher Bits Match<br>IPv4 Packets:<br>This field contains the number of lower bits of IP Source Address that are masked for matching in the IPv4 packets. The following list describes the values of this field:<br>0: No bits are masked.<br>1: LSb[0] is masked<br>2: Two LSbs [1:0] are masked<br>..<br>31: All bits except MSb are masked.<br>IPv6 Packets:<br>This field contains Bits[4:0] of L3HSBM0. These bits indicate the number of higher bits of IP Source or Destination Address matched in the IPv6 packets. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set high. |
| 5 | RW | 0x0 | L3DAIM0<br>Layer 3 IP DA Inverse Match Enable<br>When this bit is set, the Layer 3 IP Destination Address field is enabled for inverse matching. When this bit is reset, the Layer 3 IP Destination Address field is enabled for perfect matching. This bit is valid and applicable only when the L3DAM0 bit is set high.<br>Values:<br>0x0 (DISABLE): Layer 3 IP DA Inverse Match is disabled<br>0x1 (ENABLE): Layer 3 IP DA Inverse Match is enabled |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | L3DAM0<br>Layer 3 IP DA Match Enable<br>When this bit is set, the Layer 3 IP Destination Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Destination Address field for matching.<br>Note: When the L3PEN0 bit is set, you should set either this bit or the L3SAM0 bit because either IPv6 DA or SA can be checked for filtering.<br>Values:<br>0x0 (DISABLE): Layer 3 IP DA Match is disabled<br>0x1 (ENABLE): Layer 3 IP DA Match is enabled |
| 3 | RW | 0x0 | L3SAIM0<br>Layer 3 IP SA Inverse Match Enable<br>When this bit is set, the Layer 3 IP Source Address field is enabled for inverse matching. When this bit reset, the Layer 3 IP Source Address field is enabled for perfect matching.<br>This bit is valid and applicable only when the L3SAM0 bit is set.<br>Values:<br>0x0 (DISABLE): Layer 3 IP SA Inverse Match is disabled<br>0x1 (ENABLE): Layer 3 IP SA Inverse Match is enabled |
| 2 | RW | 0x0 | L3SAM0<br>Layer 3 IP SA Match Enable<br>When this bit is set, the Layer 3 IP Source Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Source Address field for matching.<br>Note: When the L3PEN0 bit is set, you should set either this bit or the L3DAM0 bit because either IPv6 SA or DA can be checked for filtering.<br>Values:<br>0x0 (DISABLE): Layer 3 IP SA Match is disabled<br>0x1 (ENABLE): Layer 3 IP SA Match is enabled |
| 1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | L3PEN0<br>Layer 3 Protocol Enable<br>When this bit is set, the Layer 3 IP Source or Destination Address matching is enabled for IPv6 packets. When this bit is reset, the Layer 3 IP Source or Destination Address matching is enabled for IPv4 packets.<br>The Layer 3 matching is done only when the L3SAM0 or L3DAM0 bit is set.<br>Values:<br>0x0 (DISABLE): Layer 3 Protocol is disabled<br>0x1 (ENABLE): Layer 3 Protocol is enabled |

**GMAC_MAC_Layer4_Address1**

Address: Operational Base + offset (0x0934)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | L4DP0<br>Layer 4 Destination Port Number Field<br>When the L4PEN0 bit is reset and the L4DPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Destination Port Number field in the IPv4 or IPv6 packets.<br>When the L4PEN0 and L4DPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Destination Port Number field in the IPv4 or IPv6 packets. |
| 15:0 | RW | 0x0000 | L4SP0<br>Layer 4 Source Port Number Field<br>When the L4PEN0 bit is reset and the L4SPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Source Port Number field in the IPv4 or IPv6 packets.<br>When the L4PEN0 and L4SPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Source Port Number field in the IPv4 or IPv6 packets. |

**GMAC_MAC_Layer3_Addr0_Reg1**

Address: Operational Base + offset (0x0940)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | L3A00<br>Layer 3 Address 0 Field<br>When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Source Address field in the IPv6 packets.<br>When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Destination Address field in the IPv6 packets.<br>When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Source Address field in the IPv4 packets. |

**GMAC_MAC_Layer3_Addr1_Reg1**

Address: Operational Base + offset (0x0944)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | L3A10<br>Layer 3 Address 1 Field<br>When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Source Address field in the IPv6 packets.<br>When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Destination Address field in the IPv6 packets.<br>When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Destination Address field in the IPv4 packets. |

**GMAC_MAC_Layer3_Addr2_Reg1**

Address: Operational Base + offset (0x0948)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | L3A20<br>Layer 3 Address 2 Field<br>When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Source Address field in the IPv6 packets.<br>When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Destination Address field in the IPv6 packets.<br>When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used. |

**GMAC_MAC_Layer3_Addr3_Reg1**

Address: Operational Base + offset (0x094c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | L3A30<br>Layer 3 Address 3 Field<br>When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Source Address field in the IPv6 packets.<br>When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Destination Address field in the IPv6 packets.<br>When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used. |

**GMAC_MTL_TxQ1_Operation_Mode**

Address: Operational Base + offset (0x0d40)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 21:16 | RW | 0x06 | TQS<br>Transmit Queue Size<br>This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes.<br>When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value.<br>The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits |
| 15:7 | RO | 0x000 | reserved |
| 6:4 | RW | 0x0 | TTC<br>Transmit Threshold Control<br>These bits control the threshold level of the MTL Tx Queue. The transmission starts when the packet size within the MTL Tx Queue is larger than the threshold. In addition, full packets with length less than the threshold are also transmitted. These bits are used only when the TSF bit is reset.<br>Values:<br>3'b000: 32 bytes<br>3'b001: 64 bytes<br>3'b010: 96 bytes<br>3'b011: 128 bytes<br>3'b100: 192 bytes<br>3'b101: 256 bytes<br>3'b110: 384 bytes<br>3'b111: 512 bytes |
| 3:2 | RW | 0x0 | TXQEN<br>Transmit Queue Enable<br>This field is used to enable/disable the transmit queue 0.<br>2'b00: Not enabled<br>2'b01: Reserved<br>2'b10: Enabled<br>2'b11: Reserved<br>This field is Read Only in Single Queue configurations and Read Write in Multiple Queue configurations.<br>Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field.<br>Values:<br>0x0 (DISABLE): Not enabled<br>0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV)<br>0x2 (ENABLE): Enabled<br>0x3 (Reserved2): Reserved |
| 1 | RW | 0x0 | TSF<br>Transmit Store and Forward<br>When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped.<br>Values:<br>1'b0: Transmit Store and Forward is disabled<br>1'b1: Transmit Store and Forward is enabled |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | FTQ<br>Flush Transmit Queue<br>When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission.<br>Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active.<br>Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.<br>Values:<br>1'b0: Flush Transmit Queue is disabled<br>1'b1: Flush Transmit Queue is enabled |

**GMAC_MTL_TxQ1_Underflow**

Address: Operational Base + offset (0x0d44)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11 | RO | 0x0 | UFCNTOVF<br>Overflow Bit for Underflow Packet Counter<br>This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: Overflow not detected for Underflow Packet Counter<br>1'b1: Overflow detected for Underflow Packet Counter |
| 10:0 | RO | 0x000 | UFFRMCNT<br>Underflow Packet Counter<br>This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event. |

**GMAC_MTL_TxQ1_Debug**

Address: Operational Base + offset (0x0d48)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x000 | reserved |
| 22:20 | RO | 0x0 | STXSTSF<br>Number of Status Words in Tx Status FIFO of Queue<br>This field indicates the current number of status in the Tx Status FIFO of this queue.When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19 | RO | 0x0 | reserved |
| 18:16 | RO | 0x0 | PTXQ<br>Number of Packets in the Transmit Queue<br>This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue. |
| 15:6 | RO | 0x000 | reserved |
| 5 | RO | 0x0 | TXSTSFSTS<br>MTL Tx Status FIFO Full Status<br>When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission.<br>Values:<br>1'b0: MTL Tx Status FIFO Full status is not detected<br>1'b1: MTL Tx Status FIFO Full status is detected |
| 4 | RO | 0x0 | TXQSTS<br>MTL Tx Queue Not Empty Status<br>When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission.<br>Values:<br>1'b0: MTL Tx Queue Not Empty status is not detected<br>1'b1: MTL Tx Queue Not Empty status is detected |
| 3 | RO | 0x0 | TWCSTS<br>MTL Tx Queue Write Controller Status<br>When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue.<br>Values:<br>1'b0: MTL Tx Queue Write Controller status is not detected<br>1'b1: MTL Tx Queue Write Controller status is detected |
| 2:1 | RO | 0x0 | TRCSTS<br>MTL Tx Queue Read Controller Status<br>This field indicates the state of the Tx Queue Read Controller:<br>Values:<br>2'b00: Idle state<br>2'b01: Read state (transferring data to the MAC transmitter)<br>2'b10: Waiting for pending Tx Status from the MAC transmitter<br>2'b11: Flushing the Tx queue because of the Packet Abort request from the MAC |
| 0 | RO | 0x0 | TXQPAUSED<br>Transmit Queue in Pause<br>When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following:<br>1. Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled<br>2. Reception of 802.3x Pause packet when PFC is disabled<br>Values:<br>1'b0: Transmit Queue in Pause status is not detected<br>1'b1: Transmit Queue in Pause status is detected |

**GMAC_MTL_TxQ1_ETS_Control**

Address: Operational Base + offset (0x0d50)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6:4 | RW | 0x0 | SLC<br>Slot Count<br>If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH[n]_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_Tx[n]_ETS_Status register, need to be computed for Queue. The encoding is as follows:<br>Values:<br>0x0 (1_SLOT): 1 slot<br>0x1 (2_SLOT): 2 slots<br>0x2 (4_SLOT): 4 slots<br>0x3 (8_SLOT): 8 slots<br>0x4 (16_SLOT): 16 slots<br>0x5 (Reserved): Reserved |
| 3 | RW | 0x0 | CC<br>Credit Control<br>When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting.<br>When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated.<br>Values:<br>0x0 (DISABLE): Credit Control is disabled<br>0x1 (ENABLE): Credit Control is enabled |
| 2 | RW | 0x0 | AVALG<br>AV Algorithm<br>When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue:<br>This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected.<br>Values:<br>0x0 (DISABLE): CBS Algorithm is disabled<br>0x1 (ENABLE): CBS Algorithm is enabled |

**GMAC_MTL_TxQ1_ETS_Status**

Address: Operational Base + offset (0x0d54)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RO | 0x0 | ABS<br>Average Bits per Slot<br>This field contains the average transmitted bits per slot. When the DCB operation is enabled for Queue 0, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680. |

**GMAC_MTL_TxQ1_Quantum_Weight**

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

Address: Operational Base + offset (0x0d58)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x000 | reserved |
| 20:0 | RW | 0x000000 | ISCQW<br>idleSlopeCredit, Quantum or Weights<br>1.idleSlopeCredit<br>When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero.<br>2.Quantum<br>When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes.<br>3.Weights<br>When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero.<br><br>Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register.<br>Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size))<br>Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time. |

**GMAC_MTL_TxQ1_SendSlopeCredit**

Address: Operational Base + offset (0x0d5c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RO | 0x00000 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:0 | RW | 0x0000 | SSC<br>sendSlopeCredit Value<br>When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing.<br>The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission. |

**GMAC_MTL_TxQ1_HiCredit**

Address: Operational Base + offset (0x0d60)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | HC<br>hiCredit Value<br>When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024.<br>The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is 131,072 * 1,024 = 134,217,728 or 0x0800_0000. |

**GMAC_MTL_TxQ1_LoCredit**

Address: Operational Base + offset (0x0d64)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:0 | RW | 0x00000000 | LC<br>loCredit Value<br>When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then (8192*2) * 8 * 1024 = 134,217,728 or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000. |

**GMAC_MTL_Q1_Interrupt_Ctrl_Status**

Address: Operational Base + offset (0x0d6c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x00 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 24 | RW | 0x0 | RXOIE<br>Receive Queue Overflow Interrupt Enable<br>When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled.<br>Values:<br>1'b0: Receive Queue Overflow Interrupt is disabled<br>1'b1: Receive Queue Overflow Interrupt is enabled |
| 23:17 | RO | 0x00 | reserved |
| 16 | RW | 0x0 | RXOVFIS<br>Receive Queue Overflow Interrupt Status<br>This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit.<br>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.<br>Values:<br>1'b0: Receive Queue Overflow Interrupt Status not detected<br>1'b1: Receive Queue Overflow Interrupt Status detected |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | ABPSIE<br>Average Bits Per Slot Interrupt Enable<br>When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated.<br>When this bit is cleared, the interrupt is not asserted for such an event.<br>Values:<br>0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled<br>0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled |
| 8 | RW | 0x0 | TXUIE<br>Transmit Queue Underflow Interrupt Enable<br>When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled.<br>Values:<br>1'b0: Transmit Queue Underflow Interrupt Status is disabled<br>1'b1: Transmit Queue Underflow Interrupt Status is enabled |
| 7:2 | RO | 0x00 | reserved |
| 1 | RW | 0x0 | ABPSIS<br>Average Bits Per Slot Interrupt Status<br>When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br>Values:<br>0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected<br>0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | TXUNFIS<br>Transmit Queue Underflow Interrupt Status<br>This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit.<br>Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.<br>Values:<br>1'b0: Transmit Queue Underflow Interrupt Status not detected<br>1'b1: Transmit Queue Underflow Interrupt Status detected |

**GMAC_MTL_RxQ1_Operation_Mode**

Address: Operational Base + offset (0x0d70)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:27 | RO | 0x00 | reserved |
| 26:20 | RW | 0x00 | RQS<br>Receive Queue Size<br>This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes.<br>When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value.<br>The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits |
| 19:14 | RW | 0x00 | RFD<br>Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes)<br>These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation:<br>0: Full minus 1 KB, that is, FULL 1 KB<br>1: Full minus 1.5 KB, that is, FULL 1.5 KB<br>2: Full minus 2 KB, that is, FULL 2 KB<br>3: Full minus 2.5 KB, that is, FULL 2.5 KB<br>...<br>62: Full minus 32 KB, that is, FULL 32 KB<br>63: Full minus 32.5 KB, that is, FULL 32.5 KB<br>The de-assertion is effective only after flow control is asserted.<br>Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:8 | RW | 0x00 | RFA<br>Threshold for Activating Flow Control (in half-duplex and full-duplex)<br>These bits control the threshold (fill-level of Rx queue) at which the flow control is activated:For more information on encoding for this field, see RFD. |
| 7 | RW | 0x0 | EHFC<br>Enable Hardware Flow Control<br>When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled.<br>Values:<br>1'b0: Hardware Flow Control is disabled<br>1'b1: Hardware Flow Control is enabled |
| 6 | RW | 0x0 | DIS_TCP_EF<br>Disable Dropping of TCP/IP Checksum Error Packets<br>When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset.<br>Values:<br>1'b0: Dropping of TCP/IP Checksum Error Packets is enabled<br>1'b1: Dropping of TCP/IP Checksum Error Packets is disabled |
| 5 | RW | 0x0 | RSF<br>Receive Queue Store and Forward<br>When this bit is set, the GMAC reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register.<br>Values:<br>1'b0: Receive Queue Store and Forward is disabled<br>1'b1: Receive Queue Store and Forward is enabled |
| 4 | RW | 0x0 | FEP<br>Forward Error Packets<br>When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped.<br>When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet may be forwarded to the application or DMA.<br>Values:<br>1'b0: Forward Error Packets is disabled<br>1'b1: Forward Error Packets is enabled |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | FUP<br>Forward Undersized Good Packets<br>When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01.<br>Values:<br>1'b0: Forward Undersized Good Packets is disabled<br>1'b1: Forward Undersized Good Packets is enabled |
| 2 | RO | 0x0 | reserved |
| 1:0 | RW | 0x0 | RTC<br>Receive Queue Threshold Control<br>These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1. |

**GMAC_MTL_RxQ1_Miss_Pkt_Ovf_Cnt**

Address: Operational Base + offset (0x0d74)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27 | RO | 0x0 | MISCNTOVF<br>Missed Packet Counter Overflow Bit<br>When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: Missed Packet Counter overflow not detected<br>1'b1: Missed Packet Counter overflow detected |
| 26:16 | RO | 0x000 | MISPKTCNT<br>Missed Packet Counter<br>This field indicates the number of packets missed by the GMAC because the application asserted ari_pkt_flush_i[] for this queue. This counter is incremented each time the application issues ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. In EQOS-DMA, EQOS-AXI, and EQOS-AHB configurations, This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event. |
| 15:12 | RO | 0x0 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11 | RO | 0x0 | OVFCNTOVF<br>Overflow Counter Overflow Bit<br>When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br>Values:<br>1'b0: Overflow Counter overflow not detected<br>1'b1: Overflow Counter overflow detected |
| 10:0 | RO | 0x000 | OVFPKTCNT<br>Overflow Packet Counter<br>This field indicates the number of packets discarded by the GMAC because of Receive queue overflow. This counter is incremented each time the GMAC discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event. |

**GMAC_MTL_RxQ1_Debug**

Address: Operational Base + offset (0x0d78)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:16 | RO | 0x0 | PRXQ<br>Number of Packets in Receive Queue<br>This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/Min_Packet_Size. |
| 15:6 | RO | 0x000 | reserved |
| 5:4 | RO | 0x0 | RXQSTS<br>MTL Rx Queue Fill-Level Status<br>This field gives the status of the fill-level of the Rx Queue:<br>Values:<br>2'b00: Rx Queue empty<br>2'b01: Rx Queue fill-level below flow-control deactivate threshold<br>2'b10: Rx Queue fill-level above flow-control activate threshold<br>2'b11: Rx Queue full |
| 3 | RO | 0x0 | reserved |
| 2:1 | RO | 0x0 | RRCSTS<br>MTL Rx Queue Read Controller State<br>This field gives the state of the Rx queue Read controller:<br>Values:<br>2'b00: Idle state<br>2'b01: Reading packet data<br>2'b10: Reading packet status (or timestamp)<br>2'b11: Flushing the packet data and status |
| 0 | RO | 0x0 | RWCSTS<br>MTL Rx Queue Write Controller Active Status<br>When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue.<br>Values:<br>1'b0: MTL Rx Queue Write Controller Active Status not detected<br>1'b1: MTL Rx Queue Write Controller Active Status detected |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**GMAC_MTL_RxQ1_Control**

Address: Operational Base + offset (0x0d7c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3 | RW | 0x0 | RXQ_FRM_ARBIT<br>Receive Queue Packet Arbitration<br>When this bit is set, the GMAC drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue.<br>When this bit is reset, the GMAC drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue:<br>1.PBL amount of data (indicated by ari_qN_pbl_i[])<br>2.Complete data of a packet<br>The status and the timestamp are not a part of the PBL data. Therefore, the GMAC drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode).<br>Values:<br>0x0 (DISABLE): Receive Queue Packet Arbitration is disabled<br>0x1 (ENABLE): Receive Queue Packet Arbitration is enabled |
| 2:0 | RW | 0x0 | RXQ_WEGT<br>Receive Queue Weight<br>This field indicates the weight assigned to the Rx Queue 0. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. |

**GMAC_DMA_CH1_Control**

Address: Operational Base + offset (0x1180)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x000 | reserved |
| 20:18 | RW | 0x0 | DSL<br>Descriptor Skip Length<br>This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor.<br>When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous. |
| 17 | RO | 0x0 | reserved |
| 16 | RW | 0x0 | PBLx8<br>8xPBL mode<br>When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH1_Tx_Control and Bits[21:16] in DMA_CH1_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value.<br>0x0 (DISABLE): 8xPBL mode is disabled<br>0x1 (ENABLE): 8xPBL mode is enabled |
| 15:14 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:0 | RW | 0x0000 | MSS<br>Maximum Segment Size<br>This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH1_Tx_Control register is set.<br>The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more. |

**GMAC_DMA_CH1_Tx_Control**

Address: Operational Base + offset (0x1184)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:16 | RW | 0x00 | TxPBL<br>Transmit Programmable Burst Length<br>These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior.<br>To transfer more than 32 beats, perform the following steps:<br>1. Set the 8xPBL mode in DMA_CH0_Control register.<br>2. Set the TxPBL.<br>Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ[n]_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32. |
| 15 | RW | 0x0 | IPBL<br>Ignore PBL Requirement<br>When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL may use handshaking to slow the DMA.<br>Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it may block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer.<br>0x0 (DISABLE): Ignore PBL Requirement is disabled<br>0x1 (ENABLE): Ignore PBL Requirement is enabled |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 14:13 | RW | 0x0 | TSE_MODE<br>TSE Mode<br>00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation.<br>01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets.<br>10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets.<br>11: Reserved<br><br>0x0 (TSO_USO): TSO/USO<br>0x1 (UFOWC): UFO with Checksum<br>0x2 (UFOWOC): UFO without Checksum<br>0x3 (Reserved): Reserved |
| 12 | RW | 0x0 | TSE<br>TCP Segmentation Enabled<br>When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4.<br>0x0 (DISABLE): TCP Segmentation is disabled<br>0x1 (ENABLE): TCP Segmentation is enabled |
| 11:5 | RO | 0x00 | reserved |
| 4 | RW | 0x0 | OSF<br>Operate on Second Packet<br>When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained.<br>0x0 (DISABLE): Operate on Second Packet disabled<br>0x1 (ENABLE): Operate on Second Packet enabled |
| 3:1 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | ST<br>Start or Stop Transmission Command<br>When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted.<br>The DMA tries to acquire descriptor from either of the following positions:<br>1.The current position in the list<br>This is the base address of the Transmit list set by the DMA_CH1_TxDesc_List_Address register.<br>2.The position at which the transmission was previously stopped<br><br>If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH1_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH1_TxDesc_List_Address register, the DMA behavior is unpredictable.<br>When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH1_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state.<br>0x0 (STOP): Stop Transmission Command<br>0x1 (START): Start Transmission Command |

**GMAC_DMA_CH1_Rx_Control**

Address: Operational Base + offset (0x1188)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | RPF<br>Rx Packet Flush<br>When this bit is set to 1, then GMAC automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue.<br>When this bit is set to 0, the GMAC not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This may in turn cause head-of-line blocking in the corresponding RxQueue.<br>0x0 (DISABLE): Rx Packet Flush is disabled<br>0x1 (ENABLE): Rx Packet Flush is enabled |
| 30:22 | RO | 0x000 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 21:16 | RW | 0x00 | RxPBL<br>Receive Programmable Burst Length<br>These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior.<br>To transfer more than 32 beats, perform the following steps:<br>1. Set the 8xPBL mode in the DMA_CH0_Control register.<br>2. Set the RxPBL.<br>Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ[n]_Operation_Mode register) in terms of beats.<br>This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32. |
| 15 | RO | 0x0 | reserved |
| 14:4 | RW | 0x000 | RBSZ_13_y<br>Receive Buffer size High<br>RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_3_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled.<br><br>Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_3_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width). |
| 3:1 | RO | 0x0 | RBSZ_3_0<br>Receive Buffer size Low<br>RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_3_0. The RBSZ_3_0 is the lower field whose width is based on data bus width of the configuration.<br>This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO) |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | SR<br>Start or Stop Receive<br>When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets.The DMA tries to acquire descriptor from either of the following positions:<br>1.The current position in the list<br>This is the address set by the DMA_CH1_RxDesc_List_Address register.<br>2.The position at which the Rx process was previously stopped<br>If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH1_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH1_RxDesc_List_Address register, the DMA behavior is unpredictable.<br>When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state.<br>0x0 (STOP): Stop Receive<br>0x1 (START): Start Receive |

**GMAC_DMA_CH1_TxDesc_List_Address**

Address: Operational Base + offset (0x1194)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RW | 0x00000000 | TDESLA<br>Start of Transmit List<br>This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO).<br>The width of this field depends on the configuration:<br>31:2 for 32-bit configuration<br>31:3 for 64-bit configuration<br>31:4 for 128-bit configuration |

**GMAC_DMA_CH1_RxDesc_List_Address**

Address: Operational Base + offset (0x119c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RW | 0x00000000 | RDESLA<br>Start of Receive List<br>This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO).<br>The width of this field depends on the configuration:<br>31:2 for 32-bit configuration<br>31:3 for 64-bit configuration<br>31:4 for 128-bit configuration |

**GMAC_DMA_CH1_TxDesc_Tail_Pointer**

Address: Operational Base + offset (0x11a0)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RW | 0x00000000 | TDTP<br>Transmit Descriptor Tail Pointer<br>This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers.<br>The width of this field depends on the configuration:<br>31:2 for 32-bit configuration<br>31:3 for 64-bit configuration<br>31:4 for 128-bit configuration |

**GMAC_DMA_CH1_RxDesc_Tail_Pointer**

Address: Operational Base + offset (0x11a8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RW | 0x00000000 | RDRT<br>Receive Descriptor Tail Pointer<br>This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers.<br>The width of this field depends on the configuration:<br>31:2 for 32-bit configuration<br>31:3 for 64-bit configuration<br>31:4 for 128-bit configuration |

**GMAC_DMA_CH1_TxDesc_Ring_Length**

Address: Operational Base + offset (0x11ac)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9:0 | RW | 0x000 | TDRL<br>Transmit Descriptor Ring Length<br>This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. we recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9. |

**GMAC_DMA_CH1_RxDesc_Ring_Length**

Address: Operational Base + offset (0x11b0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9:0 | RW | 0x000 | RDRL<br>Receive Descriptor Ring Length<br>This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9. |

**GMAC_DMA_CH1_Interrupt_Enable**

Address: Operational Base + offset (0x11b4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15 | RW | 0x0 | NIE<br>Normal Interrupt Summary Enable<br>When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH1_Status register:<br>Bit 0: Transmit Interrupt<br>Bit 2: Transmit Buffer Unavailable<br>Bit 6: Receive Interrupt<br>Bit 11: Early Receive Interrupt<br>When this bit is reset, the normal interrupt summary is disabled.<br>0x0 (DISABLE): Normal Interrupt Summary is disabled<br>0x1 (ENABLE): Normal Interrupt Summary is enabled |
| 14 | RW | 0x0 | AIE<br>Abnormal Interrupt Summary Enable<br>When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH1_Status register:<br>Bit 1: Transmit Process Stopped<br>Bit 7: Rx Buffer Unavailable<br>Bit 8: Receive Process Stopped<br>Bit 9: Receive Watchdog Timeout<br>Bit 10: Early Transmit Interrupt<br>Bit 12: Fatal Bus Error<br>Bit 13: Context Descriptor Error<br>When this bit is reset, the abnormal interrupt summary is disabled.<br>0x0 (DISABLE): Abnormal Interrupt Summary is disabled<br>0x1 (ENABLE): Abnormal Interrupt Summary is enabled |
| 13 | RW | 0x0 | CDEE<br>Context Descriptor Error Enable<br>When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled.<br>0x0 (DISABLE): Context Descriptor Error is disabled<br>0x1 (ENABLE): Context Descriptor Error is enabled |
| 12 | RW | 0x0 | FBEE<br>Fatal Bus Error Enable<br>When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled.<br>0x0 (DISABLE): Fatal Bus Error is disabled<br>0x1 (ENABLE): Fatal Bus Error is enabled |
| 11 | RW | 0x0 | ERIE<br>Early Receive Interrupt Enable<br>When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled.<br>0x0 (DISABLE): Early Receive Interrupt is disabled<br>0x1 (ENABLE): Early Receive Interrupt is enabled |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10 | RW | 0x0 | ETIE<br>Early Transmit Interrupt Enable<br>When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled.<br>0x0 (DISABLE): Early Transmit Interrupt is disabled<br>0x1 (ENABLE): Early Transmit Interrupt is enabled |
| 9 | RW | 0x0 | RWTE<br>Receive Watchdog Timeout Enable<br>When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled.<br>0x0 (DISABLE): Receive Watchdog Timeout is disabled<br>0x1 (ENABLE): Receive Watchdog Timeout is enabled |
| 8 | RW | 0x0 | RSE<br>Receive Stopped Enable<br>When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled. |
| 7 | RW | 0x0 | RBUE<br>Receive Buffer Unavailable Enable<br>When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled.<br>0x0 (DISABLE): Receive Buffer Unavailable is disabled<br>0x1 (ENABLE): Receive Buffer Unavailable is enabled |
| 6 | RW | 0x0 | RIE<br>Receive Interrupt Enable<br>When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled.<br>0x0 (DISABLE): Receive Interrupt is disabled<br>0x1 (ENABLE): Receive Interrupt is enabled |
| 5:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | TBUE<br>Transmit Buffer Unavailable Enable<br>When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled.<br>0x0 (DISABLE): Transmit Buffer Unavailable is disabled<br>0x1 (ENABLE): Transmit Buffer Unavailable is enabled |
| 1 | RW | 0x0 | TXSE<br>Transmit Stopped Enable<br>When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled.<br>0x0 (DISABLE): Transmit Stopped is disabled<br>0x1 (ENABLE): Transmit Stopped is enabled |
| 0 | RW | 0x0 | TIE<br>Transmit Interrupt Enable<br>When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled.<br>0x0 (DISABLE): Transmit Interrupt is disabled<br>0x1 (ENABLE): Transmit Interrupt is enabled |

Copyright 2022 © Rockchip Electronics Co., Ltd.

**GMAC_DMA_CH1_Rx_Interrupt_WD_Timer**

Address: Operational Base + offset (0x11b8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17:16 | RW | 0x0 | RWTU<br>Receive Interrupt Watchdog Timer Count Units<br>This fields indicates the number of system clock cycles corresponding to one unit in RWT field.<br>2'b00: 256<br>2'b01: 512<br>2'b10: 1024<br>2'b11: 2048<br>For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles. |
| 15:8 | RO | 0x00 | reserved |
| 7:0 | RW | 0x00 | RWT<br>Receive Interrupt Watchdog Timer Count<br>This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set.<br>The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30].<br>When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet. |

**GMAC_DMA_CH1_Slot_Func_Ctrl_Status**

Address: Operational Base + offset (0x11bc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:16 | RO | 0x0 | RSN<br>Reference Slot Number<br>This field gives the current value of the reference slot number in the DMA. It is used for slot comparison. |
| 15:4 | RW | 0x07c | SIV<br>Slot Interval Value<br>This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us. |
| 3:2 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | ASC<br>Advance Slot Check<br>When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is<br>1.equal to the reference slot number given in the RSN field<br>2.ahead of the reference slot number by up to two slots<br>This bit is applicable only when the ESC bit is set.<br>Values:<br>0x0 (DISABLE): Advance Slot Check is disabled<br>0x1 (ENABLE): Advance Slot Check is |
| 0 | RW | 0x0 | ESC<br>Enable Slot Comparison<br>When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is<br>1.equal to the reference slot number<br>2.ahead of the reference slot number by one slot<br>When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed.<br>Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets.<br>Values:<br>0x0 (DISABLE): Slot Comparison is disabled<br>0x1 (ENABLE): Slot Comparison is enabled |

**GMAC_DMA_CH1_Current_App_TxDesc**

Address: Operational Base + offset (0x11c4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | CURTDESAPTR<br>Application Transmit Descriptor Address Pointer<br>The DMA updates this pointer during Tx operation. This pointer is cleared on reset. |

**GMAC_DMA_CH1_Current_App_RxDesc**

Address: Operational Base + offset (0x11cc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | CURRDESAPTR<br>Application Receive Descriptor Address Pointer<br>The DMA updates this pointer during Rx operation. This pointer is cleared on reset. |

**GMAC_DMA_CH1_Current_App_TxBuffer**

Address: Operational Base + offset (0x11d4)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | CURTBUFAPTR<br>Application Transmit Buffer Address Pointer<br>The DMA updates this pointer during Tx operation. This pointer is cleared on reset. |

**GMAC_DMA_CH1_Current_App_RxBuffer**

Address: Operational Base + offset (0x11dc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | CURRBUFAPTR<br>Application Receive Buffer Address Pointer<br>The DMA updates this pointer during Rx operation. This pointer is cleared on reset. |

**GMAC_DMA_CH1_Status**

Address: Operational Base + offset (0x11e0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:19 | RO | 0x0 | REB<br>Rx DMA Error Bits<br>This field indicates the type of error that caused a Bus Error.<br>For example, error response on the AHB or AXI interface.<br>1.Bit 21<br>1'b1: Error during data transfer by Rx DMA<br>1'b0: No Error during data transfer by Rx DMA<br>2.Bit 20<br>1'b1: Error during descriptor access<br>1'b0: Error during data buffer access<br>3.Bit 19<br>1'b1: Error during read transfer<br>1'b0: Error during write transfer<br>This field is valid only when the FBE bit is set. This field does not generate an interrupt. |
| 18:16 | RO | 0x0 | TEB<br>Tx DMA Error Bits<br>This field indicates the type of error that caused a Bus Error.<br>For example, error response on the AHB or AXI interface.<br>1.Bit 18<br>1'b1: Error during data transfer by Tx DMA<br>1'b0: No Error during data transfer by Tx DMA<br>2.Bit 17<br>1'b1: Error during descriptor access<br>1'b0: Error during data buffer access<br>3.Bit 16<br>1'b1: Error during read transfer<br>1'b0: Error during write transfer<br>This field is valid only when the FBE bit is set. This field does not generate an interrupt. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x0 | NIS<br>Normal Interrupt Summary<br>Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH1_Interrupt_Enable register:<br>Bit 0: Transmit Interrupt<br>Bit 2: Transmit Buffer Unavailable<br>Bit 6: Receive Interrupt<br>Bit 11: Early Receive Interrupt<br>Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit.<br>This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Normal Interrupt Summary status not detected<br>0x1 (ACTIVE): Normal Interrupt Summary status detected |
| 14 | RW | 0x0 | AIS<br>Abnormal Interrupt Summary<br>Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH1_Interrupt_Enable register:<br>Bit 1: Transmit Process Stopped<br>Bit 7: Receive Buffer Unavailable<br>Bit 8: Receive Process Stopped<br>Bit 10: Early Transmit Interrupt<br>Bit 12: Fatal Bus Error<br>Bit 13: Context Descriptor Error<br>Only unmasked bits affect the Abnormal Interrupt Summary bit.<br>This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br>0x0 (INACTIVE): Abnormal Interrupt Summary status not detected<br>0x1 (ACTIVE): Abnormal Interrupt Summary status |
| 13 | RW | 0x0 | CDE<br>Context Descriptor Error<br>This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow ( intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Context Descriptor Error status not detected<br>0x1 (ACTIVE): Context Descriptor Error status detected |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | FBE<br>Fatal Bus Error<br>This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Fatal Bus Error status not detected<br>0x1 (ACTIVE): Fatal Bus Error status detected |
| 11 | RW | 0x0 | ERI<br>Early Receive Interrupt<br>This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer.The setting of RI bit automatically clears this bit.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Early Receive Interrupt status not detected<br>0x1 (ACTIVE): Early Receive Interrupt status detected |
| 10 | RW | 0x0 | ETI<br>Early Transmit Interrupt<br>This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL.<br>When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Early Transmit Interrupt status not detected<br>0x1 (ACTIVE): Early Transmit Interrupt status detected |
| 9 | RW | 0x0 | RWT<br>Receive Watchdog Timeout<br>This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received.<br><br>0x0 (INACTIVE): Receive Watchdog Timeout status not detected<br>0x1 (ACTIVE): Receive Watchdog Timeout status detected |
| 8 | RW | 0x0 | RPS<br>Receive Process Stopped<br>This bit is asserted when the Rx process enters the Stopped state.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Receive Process Stopped status not detected<br>0x1 (ACTIVE): Receive Process Stopped status detected |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x0 | RBU<br>Receive Buffer Unavailable<br>This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Receive Buffer Unavailable status not detected<br>0x1 (ACTIVE): Receive Buffer Unavailable status detected |
| 6 | RW | 0x0 | RI<br>Receive Interrupt<br>This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor.<br>The reception remains in the Running state.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Receive Interrupt status not detected<br>0x1 (ACTIVE): Receive Interrupt status detected |
| 5:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | TBU<br>Transmit Buffer Unavailable<br>This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it.<br>Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions.<br>To resume processing the Transmit descriptors, the application should do the following:<br>1. Change the ownership of the descriptor by setting Bit 31 of TDES3.<br>2. Issue a Transmit Poll Demand command.<br>For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Transmit Buffer Unavailable status not detected<br>0x1 (ACTIVE): Transmit Buffer Unavailable status |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | TPS<br>Transmit Process Stopped<br>This bit is set when the transmission is stopped.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Transmit Process Stopped status not detected<br>0x1 (ACTIVE): Transmit Process Stopped status detected |
| 0 | RW | 0x0 | TI<br>Transmit Interrupt<br>This bit indicates that the packet transmission is complete.<br>When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor.<br>Access restriction applies. Self-set to 1 on internal event.<br>Setting 1 clears. Setting 0 has no effect.<br><br>0x0 (INACTIVE): Transmit Interrupt status not detected<br>0x1 (ACTIVE): Transmit Interrupt status detected |

**GMAC_DMA_CH1_Miss_Frame_Cnt**

Address: Operational Base + offset (0x11e4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15 | RO | 0x0 | MFC0<br>Overflow status of the MFC Counter<br>When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event.<br><br>0x0 (INACTIVE): Miss Frame Counter overflow not occurred<br>0x1 (ACTIVE): Miss Frame Counter overflow occurred |
| 14:11 | RO | 0x0 | reserved |
| 10:0 | RO | 0x000 | MFC<br>Dropped Packet Counters<br>This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH$i_Rx_Control register.<br>The counter gets cleared when this register is read.<br>Access restriction applies. Clears on read. Self-set to 1 on internal event. |

**GMAC_DMA_CH1_RX_ERI_Cnt**

Address: Operational Base + offset (0x11e8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RO | 0x0 | ECNT<br>ERI Counter<br>When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter will get reset at the start of new packet. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

## 25.5 Interface Description

There are two GMAC Controllers in RK3588, and each has one set of IO interface, as shown below:

Table 25-3 GMAC0 Interface

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| RMII/RGMII interface | | | |
| mac_clk | I/O | GMAC0_MCLKINOUT/I2S2_SDO_M0/I2C7_SCL_M1/PWM4_M1/SPI3_CS1_M0/GPIO4_C3_d | BUS_IOC_GPIO4C_IOMUX_SEL_L [15:12] = 4'h1 |
| mac_txen | O | GMAC0_TXEN/I2S2_LRCK_M0/I2C2_SDA_M1/UART1_RTSN_M0/SPI1_CLK_M0/GPIO2_C0_d | BUS_IOC_GPIO2C_IOMUX_SEL_L [3:0] = 4'h1 |
| mac_txd3 | O | GMAC0_TXD3/SDIO_CMD_M0/I2C3_SCL_M3/GPIO2_B2_u | BUS_IOC_GPIO2B_IOMUX_SEL_L [11:8] = 4'h1 |
| mac_txd2 | O | GMAC0_TXD2/SDIO_D3_M0/FSPI_D3_M1/I2C8_SDA_M1/UART6_CTSN_M0/GPIO2_B1_u | BUS_IOC_GPIO2B_IOMUX_SEL_L [7:4] = 4'h1 |
| mac_txd1 | O | GMAC0_TXD1/I2S2_SCLK_M0/I2C5_SDA_M4/UART1_TX_M0/GPIO2_B7_d | BUS_IOC_GPIO2B_IOMUX_SEL_H [15:12] = 4'h1 |
| mac_txd0 | O | GMAC0_TXD0/I2S2_MCLK_M0/I2C5_SCL_M4/UART1_RX_M0/GPIO2_B6_d | BUS_IOC_GPIO2B_IOMUX_SEL_H [11:8] = 4'h1 |
| mac_txclk | O | GMAC0_TXCLK/SDIO_CLK_M0/FSPI_CLK_M1/I2C3_SDA_M3/GPIO2_B3_d | BUS_IOC_GPIO2B_IOMUX_SEL_L [15:12] = 4'h1 |
| mac_txer | O | GMAC0_TXER/I2C0_SDA_M1/UART7_CTSN_M0/PWM7_IR_M3/SPI3_CLK_M0/GPIO4_C6_d | BUS_IOC_GPIO4C_IOMUX_SEL_H [11:8] = 4'h1 |
| mac_rxdv | I | GMAC0_RXDV_CRS/UART7_RTSN_M0/PWM2_M2/SPI3_CS0_M0/GPIO4_C2_d | BUS_IOC_GPIO4C_IOMUX_SEL_L [11:8] = 4'h1 |
| mac_rxd3 | I | GMAC0_RXD3/SDIO_D1_M0/FSPI_D1_M1/UART6_TX_M0/GPIO2_A7_u | BUS_IOC_GPIO2A_IOMUX_SEL_H [15:12] = 4'h1 |
| mac_rxd2 | I | GMAC0_RXD2/SDIO_D0_M0/FSPI_D0_M1/UART6_RX_M0/GPIO2_A6_u | BUS_IOC_GPIO2A_IOMUX_SEL_H [11:8] = 4'h1 |
| mac_rxd1 | I | GMAC0_RXD1/I2C6_SDA_M2/UART9_TX_M0/SPI1_MOSI_M0/GPIO2_C2_d | BUS_IOC_GPIO2C_IOMUX_SEL_L [11:8] = 4'h1 |
| mac_rxd0 | I | GMAC0_RXD0/I2C2_SCL_M1/UART1_CTSN_M0/SPI1_MISO_M0/GPIO2_C1_d | BUS_IOC_GPIO2C_IOMUX_SEL_L [7:4] = 4'h1 |
| mac_rxclk | I | GMAC0_RXCLK/SDIO_D2_M0/FSPI_D2_M1/I2C8_SCL_M1/UART6_RTSN_M0/GPIO2_B0_u | BUS_IOC_GPIO2B_IOMUX_SEL_L [3:0] = 4'h1 |
| mac_ppstrig | I | GMAC0_PPSTRING/FSPI_CS1N_M1/HDMI_TX1_SCL_M0/I2C4_SCL_M1/UART7_TX_M0/GPIO2_B5_u | BUS_IOC_GPIO2B_IOMUX_SEL_H [7:4] = 4'h1 |
| mac_ppsclk | O | GMAC0_PPSCLK/TEST_CLKOUT_M1/HDMI_TX1_CEC_M0/UART9_RX_M0/SPI1_CS1_M0/GPIO2_C4_d | BUS_IOC_GPIO2C_IOMUX_SEL_H [3:0] = 4'h1 |
| mac_ptprefclk | I | GMAC0_PTP_REFCLK/FSPI_CS0N_M1/HDMI_TX1_SDA_M0/I2C4_SDA_M1/UART7_RX_M0/GPIO2_B4_u | BUS_IOC_GPIO2B_IOMUX_SEL_H [3:0] = 4'h1 |
| eth0_refclko25m | O | ETH0_REFCLKO_25M/I2S2_SDI_M0/I2C6_SCL_M2/SPI1_CS0_M0/GPIO2_C3_d | BUS_IOC_GPIO2C_IOMUX_SEL_L [15:12] = 4'h1 |
| Management interface | | | |
| mac_mdio | I/O | GMAC0_MDIO/I2C0_SCL_M1/UART9_CTSN_M0/PWM6_M2/SPI3_MOSI_M0/GPIO4_C5_d | BUS_IOC_GPIO4C_IOMUX_SEL_H [7:4] = 4'h1 |
| mac_mdc | O | GMAC0_MDC/I2C7_SDA_M1/UART9_RTSN_M0/PWM5_M2/SPI3_MISO_M0/GPIO4_C4_d | BUS_IOC_GPIO4C_IOMUX_SEL_H [3:0] = 4'h1 |

Table 25-4 GMAC1 Interface

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| RMII/RGMII interface | | | |
| mac_clk | I/O | GMAC1_MCLKINOUT/II2S2_LRCK_M1/CAN1_TX_M0/UART3_RX_M1/PWM13_M0/GPIO3_B6_d | BUS_IOC_GPIO3B_IOMUX_SEL_H[11:8] = 4'h1 |
| mac_txen | O | GMAC1_TXEN/I2S2_SCLK_M1/CAN1_RX_M0/UART3_TX_M1/PWM12_M0/GPIO3_B5_u | BUS_IOC_GPIO3B_IOMUX_SEL_H[7:4] = 4'h1 |
| mac_txd3 | O | GMAC1_TXD3/SDIO_D1_M1/I2S3_SCLK/AUDDSM_LN/FSPI_D1_M2/I2C6_SCL_M4/PWM11_IR_M0/SPI4_MOSI_M1/GPIO3_A1_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[7:4] = 4'h1 |
| mac_txd2 | O | GMAC1_TXD2/SDIO_D0_M1/I2S3_MCLK/FSPI_D0_M2/I2C6_SDA_M4/PWM10_M0/SPI4_MISO_M1/GPIO3_A0_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[3:0] = 4'h1 |
| mac_txd1 | O | GMAC1_TXD1/I2S2_MCLK_M1/UART2_CTSN/GPIO3_B4_u | BUS_IOC_GPIO3B_IOMUX_SEL_H[3:0] = 4'h1 |
| mac_txd0 | O | GMAC1_TXD0/I2S2_SDO_M1/UART2_RTSN/GPIO3_B3_u | BUS_IOC_GPIO3B_IOMUX_SEL_L[15:12] = 4'h1 |
| mac_txclk | O | GMAC1_TXCLK/SDIO_CMD_M1/I2S3_SDI/AUDDSM_RP/UART8_RTSN_M1/SPI4_CS1_M1/GPIO3_A4_d | BUS_IOC_GPIO3A_IOMUX_SEL_H[3:0] = 4'h1 |
| mac_txer | O | GMAC1_TXER/I2S2_SDI_M1/UART2_RX_M2/PWM3_IR_M1/GPIO3_B2_d | BUS_IOC_GPIO3B_IOMUX_SEL_L[11:8] = 4'h1 |
| mac_rxdv | I | GMAC1_RXDV_CRS/MIPI_CAMERA4_CLK_M1/UART2_TX_M2/PWM2_M1/GPIO3_B1_d | BUS_IOC_GPIO3B_IOMUX_SEL_L[7:4] = 4'h1 |
| mac_rxd3 | I | GMAC1_RXD3/SDIO_D3_M1/I2S3_SDO/AUDDSM_RN/FSPI_D3_M2/UART8_RX_M1/SPI4_CS0_M1/GPIO3_A3_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[15:12] = 4'h1 |
| mac_rxd2 | I | GMAC1_RXD2/SDIO_D2_M1/I2S3_LRCK/AUDDSM_LP/FSPI_D2_M2/UART8_TX_M1/SPI4_CLK_M1/GPIO3_A2_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[11:8] = 4'h1 |
| mac_rxd1 | I | GMAC1_RXD1/MIPI_CAMERA3_CLK_M1/PWM9_M0/GPIO3_B0_u | BUS_IOC_GPIO3B_IOMUX_SEL_L[3:0] = 4'h1 |
| mac_rxd0 | I | GMAC1_RXD0/MIPI_CAMERA2_CLK_M1/PWM8_M0/GPIO3_A7_u | BUS_IOC_GPIO3A_IOMUX_SEL_H[15:12] = 4'h1 |
| mac_rxclk | I | GMAC1_RXCLK/SDIO_CLK_M1/MIPI_CAMERA0_CLK_M1/FSPI_CLK_M2/I2C4_SDA_M0/UART8_CTSN_M1/GPIO3_A5_d | BUS_IOC_GPIO3A_IOMUX_SEL_H[7:4] = 4'h1 |
| mac_ppstrig | I | GMAC1_PPSTRIG/I2C3_SDA_M1/UART7_TX_M1/SPI1_MISO_M1/GPIO3_C0_d | BUS_IOC_GPIO3C_IOMUX_SEL_L[3:0] = 4'h1 |
| mac_ppsclk | O | GMAC1_PPSCLK/PCIE30X2_BUTTON_RSTN/UART7_RX_M1/SPI1_CLK_M1/GPIO3_C1_d | BUS_IOC_GPIO3C_IOMUX_SEL_L[7:4] = 4'h1 |
| mac_ptprefclk | I | GMAC1_PTP_REF_CLK/HDMI_TX1_HPD_M1/I2C3_SCL_M1/SPI1_MOSI_M1/GPIO3_B7_d | BUS_IOC_GPIO3B_IOMUX_SEL_H[15:12] = 4'h1 |
| eth1_refclko25m | O | ETH1_REFCLKO_25M/MIPI_CAMERA1_CLK_M1/I2C4_SCL_M0/GPIO3_A6_d | BUS_IOC_GPIO3A_IOMUX_SEL_H[11:8] = 4'h1 |
| Management interface | | | |
| mac_mdio | I/O | GMAC1_MDIO/MIPI_TE1/I2C8_SDA_M4/UART7_CTSN_M1/PWM15_IR_M0/SPI1_CS1_M1/GPIO3_C3_d | BUS_IOC_GPIO3C_IOMUX_SEL_L[15:12] = 4'h1 |
| mac_mdc | O | GMAC1_MDC/MIPI_TE0/I2C8_SCL_M4/UART7_RTSN_M1/PWM14_M0/SPI1_CS0_M1/GPIO3_C2_d | BUS_IOC_GPIO3C_IOMUX_SEL_L[11:8] = 4'h1 |

Copyright 2022 © Rockchip Electronics Co., Ltd.

# 25.6 Application Note

## 25.6.1 Descriptors

The DMA engine uses descriptors to efficiently move data from source to destination with minimal application CPU intervention. The DMA is designed for packet-oriented data transfers such as packets in Ethernet. The DMA controller can be programmed to interrupt the application CPU for situations such as Packet Transmit and Receive Transfer completion, and other normal or error conditions.

The DMA and the application communicate through the following two data structures:

- Control and Status registers (CSR)
- Descriptor lists and data buffers

The base address of each list is written to the respective Tx Descriptor List Address register and Rx Descriptor List Address register. The descriptor list is forward linked and the next descriptor is always considered at a fixed offset to the current one. The offset is controlled by the DSL field of DMA_Ch[n]_Control register. The number of descriptors in the list is programmed in the respective Tx (or Rx) Descriptor Ring Length register. Once the DMA processes the last descriptor in the list, it automatically jumps back to the descriptor in the List Address register to create a descriptor ring.

The descriptor lists reside in the physical memory address space of the application. Each descriptor can point to a maximum of two buffers in the system memory. This enables two buffers to be used, physically addressed, rather than contiguous buffers in memory.

A data buffer resides in the application physical memory space and consists of an entire packet or part of a packet but cannot exceed a single packet. Buffers contain only data. Buffer status is maintained in the descriptor. Data chaining refers to packets that span multiple data buffers. However, a single descriptor cannot span multiple packets. The DMA skips to the data buffer of next packet when EOP is detected.

The GMAC supports the following two types of descriptors:

- Normal Descriptor: Normal descriptors are used for packet data and to provide control information applicable to the packets to be transmitted
- Context Descriptor: Context descriptors are used to provide control information applicable to the packet to be transmitted

The GMAC supports the ring structure for the DMA descriptor.

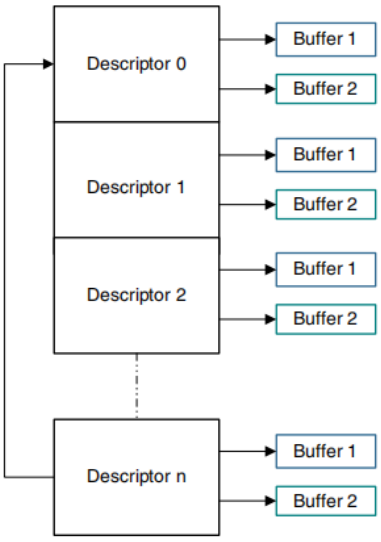



Fig. 25-10 Descriptor Ring Structure

In Ring structure, descriptors are separated by the Word, DWord, or LWord number programmed in the DSL field of the DMA_CH#_Control register. The application needs to program the total ring length, that is, the total number of descriptors in ring span in the following registers of a DMA channel:

- Transmit Descriptor Ring Length Register (DMA_CH#_TxDesc_Ring_Length)
- Receive Descriptor Ring Length Register (DMA_CH#_RxDesc_Ring_Length)

Copyright 2022 © Rockchip Electronics Co., Ltd.

The Descriptor Tail Pointer Register contains the pointer to the descriptor address (N). The base address and the current descriptor pointer decide the address of the current descriptor that the DMA can process.
The descriptors up to one location less than the one indicated by the descriptor tail pointer (N – 1) are owned by the DMA. The DMA continues to process the descriptors until the following condition occurs:

Current Descriptor Pointer == Descriptor Tail Pointer

The DMA goes into the Suspend mode when this condition occurs. The application must perform a write to the Descriptor Tail pointer register and update the tail pointer so that the following condition is true:

Current Descriptor Pointer < Descriptor Tail Pointer

The DMA automatically wraps around the base address when the end of ring is reached.
For descriptors owned by the application, the OWN bit of DES3 is reset to 0. For descriptors owned by the DMA, the OWN bit is set to 1. If the application has only one descriptor in the beginning, the application sets the last descriptor address (tail pointer) to Descriptor Base Address + 1. The DMA processes the first descriptor and then waits for the application to advance the tail pointer.

## 25.6.2 Transmit Descriptors

The DMA in GMAC requires at least one descriptor for a transmit packet. In addition to two buffers, two byte-count buffers, and two address pointers, the transmit descriptor has control fields which can be used to control the MAC operation on per-transmit packet basis. The Transmit Normal descriptor has two formats: Read format and Write-Back format.

## 25.6.3 Transmit Normal Descriptor (Read Format)

Table 25-5 TDES0 Normal Descriptor (Read Format)

| Bit | Name | Description |
|---|---|---|
| 31:0 | BUF1AP | Buffer 1 Address Pointer or TSO Header Address Pointer<br>These bits indicate the physical address of Buffer 1.<br>These bits indicate the TSO Header Address pointer when the following bits are set:<br>■ TSE bit of TDES3<br>■ FD bit of TDES3 |

Table 25-6 TDES1 Normal Descriptor (Read Format)

| Bit | Name | Description |
|---|---|---|
| 31:0 | BUF2AP | Buffer 2 or Buffer 1 Address Pointer<br>This bit indicates the physical address of Buffer 2 when a descriptor ring structure is used. There is no limitation for the buffer address alignment.<br>In 40- or 48-bit addressing mode, these bits indicate the most-significant 8- or 16- bits of the Buffer 1 Address Pointer. |

Table 25-7 TDES2 Normal Descriptor (Read Format)

| Bit | Name | Description |
|---|---|---|
| 31 | IOC | Interrupt on Completion<br>This bit controls the setting of TI and ETI status bits in the DMA_CH#_Status register. When ETIC = 1 and TDES2[LD] = 0, this bit sets the ETI bit. When TDES3[LD] = 1, this bit sets the TI status bit. |
| 30 | TTSE/TMWD | Transmit Timestamp Enable or External TSO Memory Write Enable<br>This bit enables the IEEE1588 time stamping for Transmit packet referenced by the descriptor, if TSE bit is not set.<br>If TSE bit is set and external TSO memory is enabled, setting this bit disables external TSO memory writing for this packet. |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Name | Description |
|---|---|---|
| 29:16 | B2L | Buffer 2 Length<br>The driver sets this field. When set, this field indicates Buffer 2 length |
| 15:14 | VTIR | VLAN Tag Insertion or Replacement<br>These bits request the MAC to perform VLAN tagging or untagging before transmitting the packets. The application must set the CRC Pad Control bits appropriately when VLAN Tag Insertion, Replacement, or Deletion is enabled for the packet. The following list describes the values of these bits:<br>■ 2'b00: Do not add a VLAN tag.<br>■ 2'b01: Remove the VLAN tag from the packets before transmission. This option should be used only with the VLAN packets.<br>■ 2'b10: Insert a VLAN tag with the tag value programmed in the MAC_VLAN_Incl register or context descriptor.<br>■ 2'b11: Replace the VLAN tag in packets with the tag value programmed in the MAC_VLAN_Incl register or context descriptor. This option should be used only with the VLAN packets.<br>These bits are valid when the Enable SA and VLAN Insertion on Tx option is selected while configuring the core |
| 13:0 | HL or B1L | Header Length or Buffer 1 Length<br>For Header length only bits [9:0] are taken. The size 13:0 is applicable only when interpreting buffer 1 length.<br>If the TCP Segmentation Offload feature is enabled through the TSE bit of TDES3, this field is equal to the header length. When the TSE bit is set in TDES3, the header length includes the length in bytes from Ethernet Source address till the end of the TCP header. The maximum header length supported for TSO feature is 1023 bytes. The maximum header length supported for TSO feature is 1023 bytes.<br>If the TCP Segmentation Offload feature is not enabled, this field is equal to Buffer 1 length. |

Table 25-8 TDES3 Normal Descriptor (Read Format)

| Bit | Name | Description |
|---|---|---|
| 31 | OWN | Own Bit<br>When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit after it completes the transfer of data given in the associated buffer(s). |
| 30 | CTXT | Context Type<br>This bit should be set to 1'b0 for normal descriptor. |
| 29 | FD | First Descriptor<br>When this bit is set, it indicates that the buffer contains the first segment of a packet. |
| 28 | LD | Last Descriptor<br>When this bit is set, it indicates that the buffer contains the last segment of the packet. When this bit is set, the B1L or B2L field should have a non-zero value. |
| 27:26 | CPC | CRC Pad Control<br>This field controls the CRC and Pad Insertion for Tx packet. This field is valid only when the first descriptor bit (TDES3[29]) is set. The following list describes the values of Bits[27:26]:<br>■ 2'b00: CRC and Pad Insertion. The MAC appends the cyclic redundancy check (CRC) at the end of the transmitted packet of length greater than or equal to 60 bytes. The MAC automatically appends padding and CRC to a packet with length less than 60 bytes. |

| Bit | Name | Description |
|---|---|---|
| | | ■ 2'b01: CRC Insertion (Disable Pad Insertion). The MAC appends the CRC at the end of the transmitted packet but it does not append padding. The application should ensure that the padding bytes are present in the packet being transferred from the Transmit Buffer, that is, the packet being transferred from the Transmit Buffer is of length greater than or equal to 60 bytes.<br>■ 2'b10: Disable CRC Insertion. The MAC does not append the CRC at the end of the transmitted packet. The application should ensure that the padding and CRC bytes are present in the packet being transferred from the Transmit Buffer.<br>■ 2'b11: CRC Replacement. The MAC replaces the last four bytes of the transmitted packet with recalculated CRC bytes. The application should ensure that the padding and CRC bytes are present in the packet being transferred from the Transmit Buffer.<br>This field is valid only for the first descriptor.<br>Note: When the TSE bit is set, the MAC ignores this field because the CRC and pad insertion is always done for segmentation. |
| 25:23 | SAIC | SA Insertion Control<br>These bits request the MAC to add or replace the Source Address field in the Ethernet packet with the value given in the MAC Address 0 register. The application must set the CRC Pad Control bits appropriately when SA Insertion Control is enabled for the packet. Bit 25 specifies the MAC Address Register (1 or 0) value that is used for Source Address insertion or replacement.<br>The following list describes the values of Bits[24:23]:<br>■ 2'b00: Do not include the source address<br>■ 2'b01: Include or insert the source address. For reliable transmission, the application must provide frames without source addresses.<br>■ 2'b10: Replace the source address. For reliable transmission, the application must provide frames with source addresses.<br>■ 2'b11: Reserved<br>These bits are valid in the EQOS-DMA, EQOS-AXI, and EQOS-AHB configurations when the Enable SA and VLAN Insertion on Tx option is selected while configuring the core and when the First Segment control bit (TDES3 [29]) is set.<br>This field is valid only for the first descriptor. |
| 22:19 | SLOTNUM or THL | SLOTNUM: Slot Number Control Bits in AV Mode<br>These bits indicate the slot interval in which the data should be fetched from the corresponding buffers addressed by TDES0 or TDES1. When the Transmit descriptor is fetched, the DMA compares the slot number value in this field<br>with the slot interval maintained in the RSN field DMA_CH#_Slot_Function_Control_Status. It fetches the data from the buffers only if a value matches. These bits are valid only for the AV channels.<br>THL: TCP/UDP Header Length<br>If the TSE bit is set, this field contains the length of the TCP/UDP header. The minimum value of this field must be 5 for TCP header. The value must be equal to 2 for UDP header.<br>This field is valid only for the first descriptor. |
| 18 | TSE | TCP Segmentation Enable<br>When this bit is set, the DMA performs the TCP/UDP segmentation or UDP fragmentation for a packet depending on the TSE_MODE[1:0] bit of the DMA_CH(#i)_Tx_Control Register. This bit is valid only if the FD bit is set. |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Name | Description |
|---|---|---|
| 17:16 | CIC/TPL | Checksum Insertion Control or TCP Payload Length<br>These bits control the checksum calculation and insertion. The following list describes the bit encoding:<br>■ 2'b00: Checksum Insertion Disabled.<br>■ 2'b01: Only IP header checksum calculation and insertion are enabled.<br>■ 2'b10: IP header checksum and payload checksum calculation and insertion are enabled, but pseudo-header checksum is not calculated in hardware.<br>■ 2'b11: IP Header checksum and payload checksum calculation and insertion are enabled, and pseudo-header checksum is calculated in hardware. This field is valid when the Enable Transmit TCP/IP Checksum Offload option is selected and the TSE bit is reset.<br>When the TSE bit is set, this field contains the upper bits [17:16] of the TCP Payload (or IP Payload for UDP fragmentation). This allows the TCP/UDP packet length field to be spanned across TDES3[17:0] to provide 256 KB packet length support.<br>This field is valid only for the first descriptor. |
| 15 | TPL | Reserved or TCP Payload Length<br>When the TSE bit is reset, this bit is reserved. When the TSE bit is set, this is Bit 15 of the TCP payload length [17:0]. This field is valid only when the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected while configuring the core. |
| 14:0 | FL/TPL | Frame Length or TCP Payload Length<br>This field is equal to the length of the packet to be transmitted in bytes. When the TSE bit is not set, this field is equal to the total length of the packet to be transmitted:<br>Ethernet Header Length + TCP /IP Header Length – Preamble Length – SFD Length + Ethernet Payload Length<br>When the TSE bit is set, this field is equal to the lower 15 bits of the TCP payload length in case of segmentation and IP payload in case of UDP fragmentation. In case of segmentation, this length does not include Ethernet header or TCP/UDP/IP header length. In case of fragmentation, this length does not include Ethernet header and IP header. When DWRR/WFQ algorithm is NOT enabled, value written into this field is not used when TSE = 0. |

### 25.6.4 Transmit Normal Descriptor (Write-back Format)

The write-back format of the Transmit Descriptor includes timestamp low, timestamp high, OWN, and Status bits. The write-back format is applicable only for the last descriptor of the corresponding packet. The LD bit (TDES3[28]) is set in the descriptor where the DMA writes back the status and timestamp information for the corresponding Transmit packet.
this format is only applicable to the last descriptor of a packet.

Table 25-9 TDES0 Normal Descriptor (Write-Back Format)

| Bit | Name | Description |
|---|---|---|
| 31:0 | TTSL | Transmit Packet Timestamp Low<br>The DMA updates this field with least significant 32 bits of the timestamp captured for the corresponding Transmit packet. The DMA writes the timestamp only if TTSE bit of TDES2 is set in the first descriptor of the packet. This field has the timestamp only if the Last Segment bit (LS) in the descriptor is set and the Timestamp status (TTSS) bit is set |

Table 25-10 TDES1 Normal Descriptor (Write-Back Format)

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Name | Description |
|---|---|---|
| 31:0 | TTSH | Transmit Packet Timestamp High<br>The DMA updates this field with the most significant 32 bits of the timestamp captured for corresponding transmit packet. The DMA writes the timestamp only if the TTSE bit of TDES2 is set in the first descriptor of the packet. This field has the timestamp only if the Last Segment bit (LS) in the<br>descriptor is set and Timestamp status (TTSS) bit is set. |

Table 25-11 TDES2 Normal Descriptor (Write-Back Format)

| Bit | Name | Description |
|---|---|---|
| 31:0 | Reserved | Reserved |

Table 25-12 TDES2 Normal Descriptor (Write-Back Format)

| Bit | Name | Description |
|---|---|---|
| 31 | OWN | Own Bit<br>When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit after it completes the transfer of data given in the associated buffer(s). |
| 30 | CTXT | Context Type<br>This bit should be set to 1'b0 for normal descriptor. |
| 29 | FD | First Descriptor<br>When this bit is set, it indicates that the buffer contains the first segment of a packet. |
| 28 | LD | Last Descriptor<br>When this bit is set, it indicates that the buffer contains the last segment of the packet. When this bit is set, the B1L or B2L field should have a non-zero value. |
| 27:24 | Reserved | Reserved |
| 23 | DE | Descriptor Error<br>When this bit is set, it indicates that the descriptor content is incorrect. The DMA sets this bit during write-back while closing the descriptor. Descriptor Errors can be:<br>■ Incorrect sequence from the context descriptor. For example, a location after the first descriptor for a packet<br>■ All 1s<br>■ CTXT, LD, and FD bits set to 1<br>Note 1: When Descriptor Error occurs due to All 1s or CTXT, LD, and FD bits set to 1, the Transmit DMA closes the transmit descriptor with DE and LD bits set to 1. When IOC bit in TDES2 of corresponding first descriptor is set to 1, Transmit DMA will set the TI bit in the DMA_CH#_Status register.<br>Note 2: Based on CTXT, LD, and FD bits of the transmit descriptor, the subsequent descriptor might be considered as the First Descriptor (even if FD bit is not set) and partial packet is sent. |
| 22:18 | Reserved | Reserved |
| 17 | TTSS | Tx Timestamp Status<br>This status bit indicates that a timestamp has been captured for the corresponding transmit packet. When this bit is set, TDES0 and TDES1 have timestamp values that were captured for the Transmit packet. This field is valid only when the Last Segment control bit (TDES3 [28]) in a<br>descriptor is set. This bit is valid only when IEEE1588 timestamping feature is enabled; otherwise, it is reserved. |
| 16 | EUE | ECC Uncorrectable Error Status<br>Indicates the ECC uncorrectable error in the TSO memory. |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Name | Description |
|---|---|---|
| | | Note: Uncorrectable error in Transmit FIFO memory is reported with (Bit 13) FF = 1. This is because, all such packets are flushed by GMAC. |
| 15 | ES | Error Summary<br>This bit indicates the logical OR of the following bits:<br>■ TDES3[0]: IP Header Error<br>■ TDES3[14]: Jabber Timeout<br>■ TDES3[13]: Packet Flush<br>■ TDES3[12]: Payload Checksum Error<br>■ TDES3[11]: Loss of Carrier<br>■ TDES3[10]: No Carrier<br>■ TDES3[9]: Late Collision<br>■ TDES3[8]: Excessive Collision<br>■ TDES3[3]: Excessive Deferral<br>■ TDES3[2]: Underflow Error<br>This bit is also set when EUE (bit 16) is set |
| 14 | JT | Jabber Timeout<br>This bit indicates that the MAC transmitter has experienced a jabber time-out. This bit is set only when the JD bit of the MAC_Configuration register is not set. |
| 13 | PF | Packet Flushed<br>This bit indicates that the DMA or MTL flushed the packet because of a software flush command given by the CPU. |
| 12 | PCE | Payload Checksum Error<br>This bit indicates that the Checksum Offload engine had a failure and did not insert any checksum into the encapsulated TCP, UDP, or ICMP payload. This failure can be either because of insufficient bytes, as indicated by the Payload Length field of the IP Header or the MTL starting to forward the packet to the MAC transmitter in Store-and-Forward mode without the checksum having been calculated yet. This second error condition only occurs when the Transmit FIFO depth is less than the length of the Ethernet packet being transmitted to avoid deadlock, the MTL starts forwarding the packet when the FIFO is full, even in the store-and-forward mode. This error can also occur when Bus Error is detected during packet transfer. When the Full Checksum Offload engine is not enabled, this bit is reserved. |
| 11 | LoC | Loss of Carrier<br>This bit indicates that Loss of Carrier occurred during packet transmission (that is, the gmii_crs_i signal was inactive for one or more transmit clock periods during packet transmission). This is valid only for the packets transmitted without collision and when the MAC operates in the half-duplex mode. |
| 10 | NC | No Carrier<br>This bit indicates that the carrier sense signal form the PHY was not asserted during transmission. |
| 9 | LC | Late Collision<br>This bit indicates that packet transmission was aborted because a collision occurred after the collision window (64 byte times including Preamble in MII mode and 512 byte times including Preamble and Carrier Extension in GMII mode). This bit is not valid if Underflow Error is set. |
| 8 | EC | Excessive Collision<br>This bit indicates that the transmission was aborted after 16 successive collisions while attempting to transmit the current packet. If the DR bit is set in the MAC_Configuration register, this bit is set after first collision and the transmission of the packet is aborted. |
| 7:4 | CC | Collision Count |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Name | Description |
|---|---|---|
| | | This 4-bit counter value indicates the number of collisions occurred before the packet was transmitted. The count is not valid when the EC bit is set. |
| 3 | ED | Excessive Deferral<br>This bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 bits times in 1000 Mbps mode or Jumbo Packet enabled mode) if DC bit is set in the MAC_Configuration register. When TBS is enabled in full duplex mode and this bit is set, it indicates that the frame has been dropped after the expiry time has reached. |
| 2 | UF | Underflow Error<br>This bit indicates that the MAC aborted the packet because the data arrived late from the system<br>memory. The underflow error can occur because of either of the following conditions:<br>■ The DMA encountered an empty Transmit Buffer while transmitting the packet<br>■ The application filled the MTL Tx FIFO slower than the MAC transmit rate<br>The transmission process enter the suspended state and sets the underflow bit corresponding to a queue in the MTL_Interrupt_Status register. |
| 1 | DB | Deferred Bit<br>This bit indicates that the MAC deferred before transmitting because of presence of carrier. This bit is valid only in the half-duplex mode. |
| 0 | IHE | IP Header Error<br>When IP Header Error is set, this bit indicates that the Checksum Offload engine detected an IP header error. This bit is valid only when Tx Checksum Offload is enabled. Otherwise, it is reserved. If COE detects an IP header error, it still inserts an IPv4 header checksum if the Ethernet Type field indicates an IPv4 payload.<br>In full duplex mode, when EST/Qbv is enabled and this bit is set, it indicates the frame drop status due to Frame Size error or Schedule Error. |

## 25.6.5 Programming Guide

### 25.6.5.1 Initializing DMA

Complete the following steps to initialize the DMA:
1. Provide a software reset. This resets all of the MAC internal registers and logic (bit-0 of DMA_Mode).
2. Wait for the completion of the reset process (poll bit 0 of the DMA_Mode, which is only cleared after the reset operation is completed).
3. Program the following fields to initialize the DMA_SysBus_Mode register:
a. AAL
b. Fixed burst or undefined burst
c. Burst mode values in case of AHB bus interface, OSR_LMT in case of AXI bus interface.
d. If fixed length value is enabled, select the maximum burst length possible on the AXI Bus (bits [7:1])
4. Create a descriptor list for transmit and receive. In addition, ensure that the descriptors are owned by DMA (set bit 31 of descriptor TDES3/RDES3). For more information about descriptors, see section “Descriptors”.
5. Program the Transmit and Receive Ring length registers (DMA_CH(#i)_TxDesc_Ring_Length (for i = 0; i <= GMAC_NUM_DMA_TX_CH-1) and DMA_CH(#i)_RxDesc_Ring_Length (for i = 0; i <= GMAC_NUM_DMA_RX_CH-1)). The ring length programmed must be at least 4.

Copyright 2022 © Rockchip Electronics Co., Ltd. 

6. Initialize receive and transmit descriptor list address with the base address of the transmit and receive descriptor (DMA_CH(#i)_TxDesc_List_Address (for i = 0; i <= GMAC_NUM_DMA_TX_CH-1), DMA_CH(#i)_RxDesc_List_Address (for i = 0; i <= GMAC_NUM_DMA_RX_CH-1)). Also, program transmit and receive tail pointer registers indicating to the DMA about the available descriptors (DMA_CH(#i)_TxDesc_Tail_Pointer (for i = 0; i <= GMAC_NUM_DMA_TX_CH-1) and
DMA_CH(#i)_RxDesc_Tail_Pointer (for i = 0; i <= GMAC_NUM_DMA_RX_CH-1)).
7. Program the settings of the following registers for the parameters like maximum burst-length (PBL) initiated by DMA, descriptor skip lengths, OSP in case of TxDMA, RBSZ in case of RxDMA, and so on:
- DMA_CH(#i)_Control (for i = 0; i <= GMAC_NUM_DMA_TX_CH-1)
- DMA_CH(#i)_TX_Control (for i = 0; i <= GMAC_NUM_DMA_TX_CH-1)
- DMA_CH(#i)_RX_Control (for i = 0; i <= GMAC_NUM_DMA_RX_CH-1)

8. Enable the interrupts by programming the DMA_CH(#i)_Interrupt_Enable (for i = 0; i <= GMAC_NUM_DMA_TX_CH-1) register.
9. Start the Receive and Transmit DMAs by setting SR (bit 0) of the DMA_CH(#i)_RX_Control (for i = 0; i <= GMAC_NUM_DMA_RX_CH-1) and ST (bit 0) of the DMA_CH(#i)_TX_Control (for i = 0; i <= GMAC_NUM_DMA_TX_CH-1) register.
10. Repeat steps 4 to 9 for all the Tx DMA and Rx DMA channels selected in the hardware.

### 25.6.5.2 Initializing MTL Registers

The Transaction Layer (MTL) registers must be initialized to establish the transmit and receive operating modes and commands.
Complete the following steps to initialize the MTL registers:
1. Program the Tx Scheduling (SCHALG) and Receive Arbitration Algorithm (RAA) fields in MTL_Operation_Mode to initialize the MTL operation in case of multiple Tx and Rx queues.
2. Program the Receive Queue to DMA mapping in MTL_RxQ_DMA_Map0 and MTL_RxQ_DMA_Map1 registers.
3. Program the following fields to initialize the mode of operation in the MTL_TxQ0_Operation_Mode register.
a. Transmit Store And Forward (TSF) or Transmit Threshold Control (TTC) in case of threshold mode
b. Transmit Queue Enable (TXQEN) to value 2'b10 to enable Transmit Queue0
c. Transmit Queue Size (TQS)
4. Program the following fields to initialize the mode of operation in the MTL_RxQ0_Operation_Mode register:
a. Receive Store and Forward (RSF) or RTC in case of Threshold mode
b. Flow Control Activation and De-activation thresholds for MTL Receive FIFO (RFA and RFD)
c. Error Packet and undersized good Packet forwarding enable (FEP and FUP)
d. Receive Queue Size (RQS)
5. Repeat previous two steps for all MTL Tx and Rx queues selected in the configuration.

### 25.6.5.3 Initializing MAC

The MAC configuration registers establish the operating mode of the MAC. These registers must be initialized before initializing the DMA.
The following MAC Initialization operations can be performed after DMA initialization. If the MAC initialization is completed before the DMA is configured, enable the MAC receiver (last step in the following sequence) only after the DMA is active. Otherwise, received frames fill the Rx FIFO and overflow.
1. Provide the MAC address registers: MAC_Address0_High and MAC_Address0_Low. If more than one MAC address is enabled in your configuration, program the MAC addresses appropriately.
2. Program the following fields to set the appropriate filters for the incoming frames in the MAC_Packet_Filter register:
a. Receive All
b. Promiscuous mode
c. Hash or Perfect Filter

Copyright 2022 © Rockchip Electronics Co., Ltd. 

d. Unicast, multicast, broadcast, and control frames filter settings
3. Program the following fields for proper flow control in the MAC_Q0_Tx_Flow_Ctrl register:
a. Pause time and other Pause frame control bits
b. Transmit Flow control bits
c. Flow Control Busy
4. Program the MAC_Interrupt_Enable register, as required, and if applicable, for your configuration.
5. Program the appropriate fields in the MAC_Configuration register. For ex: Inter-packet gap while transmission and jabber disable.
6. Set bit 0 and 1 in MAC_Configuration registers to start the MAC transmitter and receiver.

#### 25.6.5.4 Performing Normal Receive and Transmit Operation

During normal operation of the GMAC, normal and transmit interrupts are read, descriptors polled, the DMA is suspended (if it does not own descriptors), and values of current host transmitter or receiver descriptor pointers are read for debugging.
For normal operation, complete the following steps:
1. For normal transmit and receive interrupts, read the interrupt status. Then, poll the descriptors, reading the status of the descriptor owned by the Host (either transmit or receive).
2. Set appropriate values for the descriptors, ensuring that transmit and receive descriptors are owned by the DMA to resume the transmission and reception of data.
3. If the descriptors are not owned by the DMA (or no descriptor is available), the DMA goes into SUSPEND state. The transmission or reception can be resumed by freeing the descriptors and writing the descriptor tail pointer to Tx/Rx tail pointer register (DMA_CH[n]_TxDesc_Tail_Pointer and DMA_CH[n]_RxDesc_Tail_Pointer).
4. The values of the current host transmitter or receiver descriptor address pointer can be read for the debug process (DMA_CH[n]_Current_App_TxDesc and DMA_CH[n]_Current_App_RxDesc).
5. The values of the current host transmit buffer address pointer and receive buffer address pointer can be read for the debug process (Register DMA_CH[n]_Current_App_TxBuffer and DMA_CH[n]_Current_App_RxBuffer)

#### 25.6.5.5 Stopping and Starting Transmission

Complete the following steps to pause the transmission for some time.
1. Disable the Transmit DMA (if applicable) by clearing Bit 0 (ST) of DMA_CH(#i)_TX_Control (for i = 0; i <= GMAC_NUM_DMA_TX_CH-1) Register.
2. Wait for any previous frame transmissions to complete. You can check this by reading the appropriate bits of MTL_TxQ0_Debug Register (TRCSTS is not 01 and TXQSTS=0).
3. Disable the MAC transmitter and MAC receiver by clearing Bit (RE) and Bit 1(TE) of the MAC_Configuration Register.
4. Disable the Receive DMA (if applicable), after making sure that the data in the Rx FIFO is transferred to the system memory (by reading the appropriate bits of MTL_TxQ0_Debug Register, PRXQ=0 and RXQSTS=00).
5. Make sure that both Tx Queue and Rx Queue are empty (TXQSTS is 0 in MTL_TxQ0_Debug Register and RXQSTS is 0 in MTL_RxQ0_Debug Register).
6. To restart the operation, first start the DMAs, and then enable the MAC Transmitter and Receiver.

#### 25.6.5.6 Initialization Guidelines for System Time Generation

You can enable the timestamp feature by setting Bit 0 of the MAC_Timestamp_Control Register. However, it is essential that the timestamp counter be initialized after this bit is set. Complete the following steps during GMAC initialization:
1. Mask the Timestamp Trigger interrupt by clearing the bit 16 of MAC_Interrupt_Enable Register.
2. Set Bit 0 of MAC_Timestamp_Control Register to enable timestamping.
3. Program MAC_Sub_Second_Increment Register based on the PTP clock frequency.

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

4. If you are using the Fine Correction approach, program MAC_Timestamp_Addend and set Bit 5 of MAC_Timestamp_Control Register.
5. Poll the MAC_Timestamp_Control Register until Bit 5 is cleared.
6. Program Bit 1 of MAC_Timestamp_Control Register to select the Fine Update method (if required).
7. Program MAC_System_Time_Seconds_Update Register and MAC_System_Time_Nanoseconds_Update Register with the appropriate time value.
8. Set Bit 2 in MAC_Timestamp_Control Register.
The timestamp counter starts operation as soon as it is initialized with the value written in the Timestamp Update registers. If one-step timestamping is enabled
a. To enable one-step timestamping, program Bit 27 of the TDES3 Context Descriptor.
b. Program registers MAC_Timestamp_Ingress_Asym_Corr and MAC_Timestamp_Egress_Asym_Corr to update the correction field in PDelay_Req PTP messages.
9. Enable the MAC receiver and transmitter for proper timestamping.

#### 25.6.5.7 Coarse Correction Method

To synchronize or update the system time in one process (coarse correction method), complete the following steps:
1. Set the offset (positive or negative) in the Timestamp Update registers (MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update).
2. Set Bit 3 (TSUPDT) of MAC_Timestamp_Control Register. The value in the Timestamp Update registers is added to or subtracted from the system time when the TSUPDT bit is cleared.

#### 25.6.5.8 Programming Guidelines for TSO

The TCP Segmentation Offload (TSO) engine is used to offload the TCP segmentation functions to the hardware. To program the TSO, set the TSE bit to enable TCP packet segmentation, and program descriptor fields to enable TSO for the current packet.
Complete the following steps to program TSO:
1. Program the TSE bit of corresponding DMA_CH[n]_Tx_Control register to enable TCP packet segmentation in that DMA.
2. In addition to the normal transfer descriptor setting, the following descriptor fields must be programmed to enable TSO for the current packet:
a. Enable TSE in Bit 18 of TDES3
b. Program the length of the un-segmented TCP/IP packet payload in bits [17:0] of TDES3 and the TCP header in bits [22:19] of TDES3.
c. Program the maximum size of the segment in MSS of DMA_CH[n]_Control register or MSS in the context descriptor. If MSS field is programmed in both DMA_CH[n]_Control register and in the context descriptor, the latest software programmed sequence is considered.
3. The header of the unsegmented TCP/IP packet should be in Buffer 1 of the first descriptor and this buffer must not hold any payload bytes. The payload is allocated to Buffer 2 and the buffers of the subsequent descriptors.

#### 25.6.5.9 Programming Guidelines for Multi-Channel Multi-Queuing Transmit

1. Program the Transmit queue size in the TQS field of MTL_TxQ[n]_Operation_Mode register. Based on the value programmed in the TQS field, the size of the queue is determined.
In the Transmit operation, the number of channels is equal to the number of the queues. Due to this reason, the Channel-to-Queue mapping is fixed.
2. For a queue to be used, the queue needs to be enabled in TXQEN in the corresponding MTL_TxQ[n]_Operation_Mode Register. In DMA configurations, the ST bit of DMA_CH[n]_Tx_Control Register and corresponding TXQEN in MTL_TxQ[n]_Operation Mode Register needs to be enabled.
3. The scheduling method needs to be programmed in SCHALG of MTL_Operation_Mode register.

Copyright 2022 © Rockchip Electronics Co., Ltd. 

4. Program the MTL_TxQ[n]_Quantum_Weight for DCB queue as per the selected algorithm. In case of CBS algorithm in AVB queues, the MTL_TxQ[n]_ETS_Control, MTL_TxQ[n]_SendSlopeCredit, MTL_TxQ[n]_HiCredit and MTL_TxQ[n]_LoCredit registers also need to be programmed as required.
5. If DCB is enabled and PFC function is required, program MAC_TxQ_Prty_Map0 Register to assign a fixed priority to the queue. This priority assigned is used for determining if the corresponding queue should stop transmitting packet based on the received PFC packet.

**Receive**
1. Program the Receive queue size in the RQS field of MTL_RxQ[n]_Operation_Mode Register. Based on the value programmed in RQS field, the size of the queue is determined.
2. Enable the Receive Queues 0 to 7 in the fields RXQ0EN to RXQ7EN in MAC_RxQ_Ctrl0 Register for AV or DCB. In DMA configurations, SR bit of statically or dynamically mapped DMA_CH[n]_Rx_Control Register and corresponding RXQ[n]_EN in MAC_RxQ_Ctrl0 Register needs to be enabled.
3. The MAC routes the Rx packets to the Rx Queues based on following packet types:
   a. AV PTP Packets: Based on the programming of AVPTPQ in MAC_RxQ_Ctrl1 Register.
   b. AV Untagged Control packets: Based on the programming of AVCPQ in MAC_RxQ_Ctrl1 Register.
   c. Data Center Bridging (DCB) related Link Layer Discovery Protocol (LLDP) packets. Program
   DCBCPQ in MAC_RxQ_Ctrl1 Register to indicate to MAC which queue should get the DCB packets.
   d. VLAN Tag Priority field in VLAN Tagged packets: Program PSRQ7-0 of the MAC_RxQ_Ctrl2 and MAC_RxQ_Ctrl3 Register for the routing of tagged packets based on the USP (user Priority) field of the received packets to the Rx Queues 0 to 7.
   e. The AV tagged control and data packets are also routed based on PSRQ field of the MAC_RxQ_Ctrl2 and MAC_RxQ_Ctrl3 registers.
4. If multiple RX DMA channels are enabled, the following programming should be done for proper arbitration and mapping:
   a. Program the RAA field of MTL_Operation_Mode register to select the arbitration algorithm to decide which RxQ is read out from the RxFIFO memory.
   b. Program the MTL_RxQ[n]_Control to decide the weights and the packet arbitration for each RxQ.
   c. If static mapping is programmed in MTL_RxQ_DMA_Map[n] register (RXQ[n]DADMACH is reset to 0), bits RXQx2DMA and others need to be programmed to select the channel for which each queue is mapped.
   d. Set RXQ[n]DADMACH bit in MTL_RxQ_DMA_Map0 Register to select dynamic mapping of
   packets in each RxQueue.
   e. In dynamic channel mapping, the routing of a packet to a specific RxDMA channel is decided by the value of DCS field in the lowest MAC Address Register.

## 25.6.6 Transmit Context Descriptor

The context descriptor is used to provide the timestamps for one-step timestamp correction, VLAN Tag ID for VLAN insertion feature. The Transmit Context descriptor can be provided any time before a packet descriptor. The context is valid for the current packet and subsequent packets. The context descriptor is used to provide the timestamps for one-step timestamp correction and VLAN Tag ID for VLAN insertion feature. Write back is done on a context descriptor only to reset the OWN bit.

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

Table 25-13 TDES0 Context Descriptor

| Bit | Name | Description |
|---|---|---|
| 31:0 | TTSL | Transmit Packet Timestamp Low<br>For one-step correction, the driver can provide the lower 32 bits of timestamp in this descriptor word.<br>The DMA uses this value as the low word for doing one-step timestamp correction. This field is valid only if the OSTC and TCMSSV bits of TDES3 context descriptor are set. |

Table 25-14 TDES1 Context Descriptor

| Bit | Name | Description |
|---|---|---|
| 31:0 | TTSH | Transmit Packet Timestamp High<br>For one-step correction, the driver can provide the upper 32 bits of timestamp in this descriptor. The DMA uses this value as the high word for doing one-step timestamp correction. This field is valid only if the OSTC and TCMSSV bits of TDES3 context descriptor are set. |

Table 25-15 TDES2 Context Descriptor

| Bit | Name | Description |
|---|---|---|
| 31:16 | IVT | Inner VLAN Tag<br>When the IVLTV bit of TDES3 context descriptor is set and the TCMSSV and OSTC bits of TDES3 context descriptor are reset, TDES2[31:16] contains the inner VLAN Tag to be inserted in the subsequent Transmit packets. |
| 15:14 | Reserved | Reserved |
| 13:0 | MSS | Maximum Segment Size<br>When the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected, the driver can provide maximum segment size in this field. This segment size is used while segmenting the TCP/IP payload. This field is valid only if the TCMSSV bit of TDES3 context descriptor is set and the OSTC bit of the TDES3 context descriptor is reset. |

Table 25-16 TDES3 Context Descriptor

| Bit | Name | Description |
|---|---|---|
| 31 | OWN | Own Bit<br>When this bit is set, it indicates that the GMAC DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit immediately after the read. |
| 30 | CTXT | Context Type<br>This bit should be set to 1'b1 for Context descriptor. |
| 29:28 | Reserved | Reserved |
| 27 | OSTC | One-Step Timestamp Correction Enable<br>When this bit is set, the DMA performs a one-step timestamp correction with reference to the timestamp values provided in TDES0 and TDES1. |
| 26 | TCMSSV | One-Step Timestamp Correction Input or MSS Valid<br>When this bit and the OSTC bit are set, it indicates that the Timestamp Correction input provided in TDES0 and TDES1 is valid.<br>When the OSTC bit is reset and this bit and the TSE bit of TDES3 are set in subsequent normal descriptor, it indicates that the MSS input in TDES2 is valid. |
| 25:24 | Reserved | Reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Name | Description |
|---|---|---|
| 23 | DE | Descriptor Error<br>When this bit is set, it indicates that the descriptor content is incorrect.The DMA sets this bit during write-back while closing the context descriptor.<br>Descriptor Errors can be:<br>■ Incorrect sequence from the context descriptor. For example, a location before the first descriptor for a packet<br>■ All 1s<br>■ CD, LD, and FD bits set to 1<br>Note 1: When Descriptor Error occurs due to All 1s or CTXT, LD, and FD bits set to 1, the Transmit DMA closes the transmit descriptor with DE and LD bits set to 1. When IOC bit in TDES2 of corresponding first descriptor is set to 1, Transmit DMA will set the TI bit in the DMA_CH#_Status<br>Register.<br>Note 2: Based on CTXT, LD, and FD bits of the transmit descriptor, the subsequent descriptor might be considered as the First Descriptor (even if FD bit is not set) and partial packet is sent. |
| 22:20 | Reserved | Reserved |
| 19:18 | IVTIR | Inner VLAN Tag Insert or Replace<br>When this bit is set, these bits request the MAC to perform Inner VLAN tagging or un-tagging before transmitting the packets. If the packet is modified for VLAN tags, the MAC automatically recalculates and replaces the CRC bytes.<br>The following list describes the values of these bits:<br>■ 2'b00: Do not add the inner VLAN tag.<br>■ 2'b01: Remove the inner VLAN tag from the packets before transmission. This option should be used only with the VLAN frames.<br>■ 2'b10: Insert an inner VLAN tag with the tag value programmed in the MAC_Inner_VLAN_Incl register or context descriptor.<br>■ 2'b11: Replace the inner VLAN tag in packets with the tag value programmed in the MAC_Inner_VLAN_Incl register or context descriptor. This option should be used only with the VLAN frames.<br>These bits are valid when the Enable SA and VLAN Insertion on Tx and Enable Double VLAN Processing options are selected. |
| 17 | IVLTV | Inner VLAN Tag Valid<br>When this bit is set, it indicates that the IVT field of TDES2 is valid. |
| 16 | VLTV | VLAN Tag Valid<br>When this bit is set, it indicates that the VT field of TDES3 is valid. |
| 15:0 | VT | VLAN Tag<br>This field contains the VLAN Tag to be inserted or replaced in the packet. This field is used as VLAN Tag only when the VLTI bit of the MAC_VLAN_Incl register is reset. |

### 25.6.7 Receive Descriptors

The DMA in GMAC attempts to read a descriptor only if the Tail Pointer is different from the Base Pointer or current pointer. It is recommended to have a descriptor ring with a length that can accommodate at least two complete packets received by the MAC. Otherwise, the performance of the DMA is impacted greatly because of the unavailability of the descriptors. In such situations, the RxFIFO in MTL becomes full and starts dropping packets.

The following Receive Descriptors are present:

- Normal descriptors
- Context descriptors

All RX descriptors are prepared by the software and given to the DMA as “Normal” Descriptors with the content as shown in Receive Normal Descriptor (Read Format). The DMA reads this descriptor and after transferring a received packet (or part of) to the buffers indicated by the descriptor, the Rx DMA will close the descriptor with the corresponding

Copyright 2022 © Rockchip Electronics Co., Ltd.

packet status. The format of this status is given in the "Receive Normal Descriptor (Write-Back Format)". For some packets, the normal descriptor bits are not enough to write the complete status. For such packets, the RX DMA writes the extended status to the next descriptor (without processing or using the Buffers/ Pointers embedded in that descriptor). The format and content of the descriptor write back is described in "Receive Context Descriptor".

## 25.6.8 Receive Normal Descriptors(Read Format)

Table 25-17 TDES0 Normal Descriptor(Read Format)

| Bit | Name | Description |
|---|---|---|
| 31:0 | BUF1AP | Header or Buffer 1 Address Pointer<br>When the SPH bit of Control register of a channel is reset, these bits indicate the physical address of Buffer 1. When the SPH bit is set, these bits indicate the physical address of Header Buffer where the Rx DMA writes the L2/L3/L4 header bytes of the received packet.<br>The application can program a byte-aligned address for this buffer which means that the LS bits of this field can be non-zero. However, while transferring the start of packet, the DMA performs a Write operation with RDES0[1:0] (or RDES0[2:0]/[3:0] in case of 64-/128-bit configuration) as zero. However, the packet data is shifted as per actual offset as given by buffer address pointer.<br>If the address pointer points to a buffer where the middle or last part of the packet is stored, the DMA ignores the offset address and writes to the full location as indicated by the data-width. |

Table 25-18 TDES1 Normal Descriptor(Read Format)

| Bit | Name | Description |
|---|---|---|
| 31:0 | Reserved or BUF1AP | In 64-bit addressing mode, this field contains the most-significant 32 bits of the Buffer 1 Address Pointer. Otherwise, this field is reserved. |

Table 25-19 TDES2 Normal Descriptor(Read Format)

| Bit | Name | Description |
|---|---|---|
| 31:0 | Reserved or BUF1AP | In 64-bit addressing mode, this field contains the most-significant 32 bits of the Buffer 1 Address Pointer. Otherwise, this field is reserved. |

Table 25-20 TDES3 Normal Descriptor(Read Format)

| Bit | Name | Description |
|---|---|---|
| 31 | OWN | Own Bit<br>When this bit is set, it indicates that the GMAC DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true:<br>■ The DMA completes the packet reception<br>■ The buffers associated with the descriptor are full |
| 30 | IOC | Interrupt Enabled on Completion<br>When this bit is set, an interrupt is issued to the application when the DMA closes this descriptor. |
| 29:26 | Reserved | Reserved |
| 25 | BUF2V | Buffer 2 Address Valid<br>When this bit is set, it indicates to the DMA that the buffer 2 address specified in RDES2 is valid. |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Name | Description |
|---|---|---|
| | | The application must set this bit so that the DMA can use the address, to which the Buffer 2 address in RDES2 is pointing, to write received packet data. |
| 24 | BUF1V | Buffer 1 Address Valid<br>When set, this indicates to the DMA that the buffer 1 address specified in RDES1 is valid.<br>The application must set this value if the address pointed to by Buffer 1 address in RDES1 can be used by the DMA to write received packet data. |
| 23:0 | Reserved | Reserved |

### 25.6.9 Receive Normal Descriptors(Write-Back Format)

Table 25-21 TDES0 Normal Descriptor(Write-Back Format)

| Bit | Name | Description |
|---|---|---|
| 31:16 | IVT | Inner VLAN Tag<br>This field contains the Inner VLAN tag of the received packet if the RS0V bit of RDES3 is set.<br>This is valid only when Double VLAN tag processing and VLAN tag stripping are enabled. |
| 15:0 | OVT | Outer VLAN Tag<br>This field contains the Outer VLAN tag of the received packet if the RS0V bit of RDES3 is set. |

Table 25-22 TDES1 Normal Descriptor(Write-Back Format)

| Bit | Name | Description |
|---|---|---|
| 31:16 | OPC | OAM Sub-Type Code, or MAC Control Packet opcode<br>OAM Sub-Type Code<br>If Bits[18:16] of RDES3 are set to 3'b111, this field contains the OAM sub-type and code fields.<br>MAC Control Packet opcode<br>If Bits[18:16] of RDES3 are set to 3'b110, this field contains the MAC Control packet opcode field. |
| 15 | TD | Timestamp Dropped<br>This bit indicates that the timestamp was captured for this packet but it got dropped in the MTL Rx FIFO because of overflow.<br>This bit is available only when you select the Timestamp feature. Otherwise, this bit is reserved. |
| 14 | TSA | Timestamp Available<br>When Timestamp is present, this bit indicates that the timestamp value is available in a context descriptor word 2 (RDES2) and word 1(RDES1).<br>This is valid only when the Last Descriptor bit (RDES3 [28]) is set.<br>The context descriptor is written in the next descriptor just after the last normal descriptor for a packet. |
| 13 | PV | PTP Version<br>This bit indicates that the received PTP message has the IEEE 1588 version 2 format. When this bit is reset, it indicates the IEEE 1588 version 1 format.<br>This bit is available only when you select the Timestamp feature. Otherwise, this bit is reserved. |
| 12 | PFT | PTP Packet Type<br>This bit indicates that the PTP message is sent directly over Ethernet.<br>This bit is available only when you select the Timestamp feature. Otherwise, this bit is reserved. |
| 11:8 | PMT | PTP Message Type<br>These bits are encoded to give the type of the message received:<br>■ 0000: No PTP message received |

| Bit | Name | Description |
|---|---|---|
| | | ■ 0001: SYNC (all clock types)<br>■ 0010: Follow_Up (all clock types)<br>■ 0011: Delay_Req (all clock types)<br>■ 0100: Delay_Resp (all clock types)<br>■ 0101: Pdelay_Req (in peer-to-peer transparent clock)<br>■ 0110: Pdelay_Resp (in peer-to-peer transparent clock)<br>■ 0111: Pdelay_Resp_Follow_Up (in peer-to-peer transparent clock)<br>■ 1000: Announce<br>■ 1001: Management<br>■ 1010: Signaling<br>■ 1011–1110: Reserved<br>■ 1111: PTP packet with Reserved message type<br>These bits are available only when you select the Timestamp feature. |
| 7 | IPCE | IP Payload Error<br>When this bit is set, it indicates either of the following:<br>■ The 16-bit IP payload checksum (that is, the TCP, UDP, or ICMP checksum) calculated by the MAC does not match the corresponding checksum field in the received segment.<br>■ The TCP, UDP, or ICMP segment length does not match the payload length value in the IP Header field.<br>■ The TCP, UDP, or ICMP segment length is less than minimum allowed segment length for TCP, UDP, or ICMP.<br>Bit 15 (ES) of RDES3 is not set when this bit is set. |
| 6 | IPCB | IP Checksum Bypassed<br>This bit indicates that the checksum offload engine is bypassed. This bit is available when you select the Enable Receive TCP/IP Checksum Check feature. |
| 5 | IPV6 | IPv6 header Present<br>This bit indicates that an IPV6 header is detected. When the Enable Split Header Feature option is selected and the SPH bit of Control Register of a channel is set, the IPV6 header is available in the header buffer area to which RDES0 is pointing. |
| 4 | IPV4 | IPV4 Header Present<br>This bit indicates that an IPV4 header is detected. When the SPH bit of RDES3 is set, the IPV4 header is available in the header buffer area to which RDES0 is pointing. |
| 3 | IPHE | IP Header Error<br>When this bit is set, it indicates either of the following:<br>■ The 16-bit IPv4 header checksum calculated by the MAC does not match the received checksum bytes.<br>■ The IP datagram version is not consistent with the Ethernet Type value.<br>■ Ethernet packet does not have the expected number of IP header bytes.<br>This bit is valid when either Bit 5 or Bit 4 is set. This bit is available when you select the Enable Receive TCP/IP Checksum Check feature. |
| 2:0 | PT | Payload Type<br>These bits indicate the type of payload encapsulated in the IP datagram processed by the Receive Checksum Offload Engine (COE):<br>■ 3'b000: Unknown type or IP/AV payload not processed<br>■ 3'b001: UDP<br>■ 3'b010: TCP<br>■ 3'b011: ICMP<br>■ 3'b110: AV Tagged Data Packet<br>■ 3'b111: AV Tagged Control Packet<br>■ 3'b101: AV Untagged Control Packet |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Name | Description |
|---|---|---|
| | | ■ 3'b100: IGMP if IPV4 Header Present bit is set else DCB (LLDP) Control Packet<br>If the COE does not process the payload of an IP datagram because there is an IP header error or fragmented IP, it sets these bits to 3'b000. |

Table 25-23 TDES2 Normal Descriptor(Write-Back Format)

| Bit | Name | Description |
|---|---|---|
| 31:29 | L3L4FM | Layer 3 and Layer 4 Filter Number Matched<br>These bits indicate the number of the Layer 3 and Layer 4 Filter that matched the received packet:<br>■ 000: Filter 0<br>■ 001: Filter 1<br>■ 010: Filter 2<br>■ 011: Filter 3<br>■ 100: Filter 4<br>■ 101: Filter 5<br>■ 110: Filter 6<br>■ 111: Filter 7<br>This field is valid only when Bit 28 or Bit 27 is set high. When more than one filter matches, these bits give the number of lowest filter.<br>Note: This status is not available when Flexible RX Parser is enabled. |
| 28 | L4FM | Layer 4 Filter Match<br>When this bit is set, it indicates that the received packet matches one of the enabled Layer 4 Port Number fields. This status is given only when one of the following conditions is true:<br>■ Layer 3 fields are not enabled and all enabled Layer 4 fields match<br>■ All enabled Layer 3 and Layer 4 filter fields match<br>When more than one filter matches, this bit gives the layer 4 filter status of filter indicated by Bits[31:29].<br>Note: This status is not available when Flexible RX Parser is enabled. |
| 27 | L3FM | Layer 3 Filter Match<br>When this bit is set, it indicates that the received packet matches one of the enabled Layer 3 IP Address fields. This status is given only when one of the following conditions is true:<br>■ All enabled Layer 3 fields match and all enabled Layer 4 fields are bypassed<br>■ All enabled filter fields match<br>When more than one filter matches, this bit gives the layer 3 filter status of filter indicated by Bits[31:29].<br>Note: This status is not available when Flexible RX Parser is enabled. |
| 26:19 | MADRM | MAC Address Match or Hash Value<br>When the HF bit is reset, this field contains the MAC address register number that matched the Destination address of the received packet. This field is valid only if the DAF bit is reset.<br>When the HF bit is set, this field contains the hash value computed by the MAC. A packet passes the hash filter when the bit corresponding to the hash value is set in the hash filter register.<br>Note: This status is not available when Flexible RX Parser is enabled. |
| 18 | HF | Hash Filter Status<br>When this bit is set, it indicates that the packet passed the MAC address hash filter. Bits[26:19] indicate the hash value.<br>Note: This status is not available when Flexible RX Parser is enabled. |
| 17 | DAF/RXPI | Destination Address Filter Fail<br>When Flexible RX Parser is disabled, and this bit is set, it indicates that the packet failed the DA Filter in the MAC. |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Name | Description |
|---|---|---|
| | | When Flexible RX Parser is enabled, this bit is set to indicate that the packet parsing is incomplete (RXPI) due to ECC error.<br>Note: When this bit is set, ES bit of RDES3 is also set. |
| 16 | SAF/RXPD | SA Address Filter Fail<br>When Flexible RX Parser is disabled, and this bit is set, it indicates that the packet failed the SA Filter in the MAC.<br>When Flexible RX Parser is enabled, this bit is set to indicate that the packet is dropped (RXPD) by the parser.<br>Note: When this bit is set, ES bit of RDES3 is also set. |
| 15 | OTS | VLAN Filter Status<br>When set, this bit indicates that the VLAN Tag of the received packed passed the VLAN filter.<br>This bit is valid only when GMAC_ERVFE is not enabled.<br>If GMAC_ERVFE is enabled, the bit is redefined as Outer VLAN Tag Filter Status (OTS).<br>This bit is valid for both Single and Double VLAN Tagged frames. |
| 14 | ITS | Inner VLAN Tag Filter Status (ITS)<br>This bit is valid only when GMAC_ERVFE is enabled.<br>This bit is valid only for Double VLAN Tagged frames, when Double VLAN Processing is enabled.<br>For more information, see the Filter Status topic. |
| 13:11 | Reserved | Reserved |
| 10 | ARPNR | ARP Reply Not Generated<br>When this bit is set, it indicates that the MAC did not generate the ARP Reply for received ARP Request packet. This bit is set when the MAC is busy transmitting ARP reply to earlier ARP request (only one ARP request is processed at a time).<br>This bit is reserved when the Enable IPv4 ARP Offload option is not selected. |
| 9:0 | HL | L3/L4 Header Length<br>This field contains the length of the header of the packet split by the MAC at L3 or L4 header.<br>boundary as identified by the MAC receiver. This field is valid only when the first descriptor bit is set (FD = 1).<br>The header data is written to the Buffer 1 address of corresponding descriptor. If header length is zero, this field is not valid. It implies that the MAC did not identify and split the header.<br>This field is valid when the Enable Split Header Feature option is selected. |

Table 25-24 TDES3 Normal Descriptor(Write-Back Format)

| Bit | Name | Description |
|---|---|---|
| 31 | OWN | Own Bit<br>When this bit is set, it indicates that the GMAC DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true:<br>■ The DMA completes the packet reception<br>■ The buffers associated with the descriptor are full |
| 30 | CTXT | Receive Context Descriptor<br>When this bit is set, it indicates that the current descriptor is a context type descriptor. The DMA writes 1'b0 to this bit for normal receive descriptor.<br>When CTXT and FD bits are used together, {CTXT, FD}<br>■ 2’b00: Intermediate Descriptor<br>■ 2’b01: First Descriptor<br>■ 2’b10: Reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Name | Description |
|---|---|---|
| | | ■ 2'b11: Descriptor Error (due to all 1s)<br>Note: When Descriptor Error occurs, the Receive DMA closes the receive descriptor indicating Descriptor Error. This receive descriptor is skipped and the buffer addresses are not used to write the packet data Receive DMA will set the CDE bit in DMA_CH#_Status register but not the RI bit even when IOC is set, as this is not marked as last receive descriptor for the packet. The subsequent valid receive descriptor is used to write the packet data. |
| 29 | FD | First Descriptor<br>When this bit is set, it indicates that this descriptor contains the first buffer of the packet. If the size of the first buffer is 0, the second buffer contains the beginning of the packet. If the size of the second buffer is also 0, the next descriptor contains the beginning of the packet.<br>See the CTXT bit description for details of using the CTXT bit and FD bit together. |
| 28 | LD | Last Descriptor<br>When this bit is set, it indicates that the buffers to which this descriptor is pointing are the last buffers of the packet. |
| 27 | RS2V | Receive Status RDES2 Valid<br>When this bit is set, it indicates that the status in RDES2 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set. |
| 26 | RS1V | Receive Status RDES1 Valid<br>When this bit is set, it indicates that the status in RDES1 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set. |
| 25 | RS0V | Receive Status RDES0 Valid<br>When this bit is set, it indicates that the status in RDES0 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set. |
| 24 | CE | CRC Error<br>When this bit is set, it indicates that a Cyclic Redundancy Check (CRC) Error occurred on the received packet. This field is valid only when the LD bit of RDES3 is set. |
| 23 | GP | Giant Packet<br>When this bit is set, it indicates that the packet length exceeds the specified maximum Ethernet size of 1518, 1522, or 2000 bytes (9018 or 9022 bytes if jumbo packet enable is set).<br>Note: Giant packet indicates only the packet length. It does not cause any packet truncation. |
| 22 | RWT | Receive Watchdog Timeout<br>When this bit is set, it indicates that the Receive Watchdog Timer has expired while receiving the current packet. The current packet is truncated after watchdog timeout. |
| 21 | OE | Overflow Error<br>When this bit is set, it indicates that the received packet is damaged because of buffer overflow in Rx FIFO.<br>Note: This bit is set only when the DMA transfers a partial packet to the application. This happens only when the Rx FIFO is operating in the threshold mode. In the store-and-forward mode, all partial packets are dropped completely in Rx FIFO. |
| 20 | RE | Receive Error<br>When this bit is set, it indicates that the gmii_rxer_i signal is asserted while the gmii_rxdv_i signal is asserted during packet reception. This error also includes carrier extension error in the GMII and half-duplex |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Name | Description |
|---|---|---|
| | | mode. Error can be of less or no extension, or error (rxd!= 0f) during extension. |
| 19 | DE | Dribble Bit Error<br>When this bit is set, it indicates that the received packet has a non-integer multiple of bytes (odd nibbles). This bit is valid only in the MII Mode. |
| 18:16 | LT | Length/Type Field<br>This field indicates if the packet received is a length packet or a type packet. The encoding of the 3<br>bits is as follows:<br>■ 3'b000: The packet is a length packet<br>■ 3'b001: The packet is a type packet.<br>■ 3'b011: The packet is a ARP Request packet type<br>■ 3'b100: The packet is a type packet with VLAN Tag<br>■ 3'b101: The packet is a type packet with Double VLAN Tag<br>■ 3'b110: The packet is a MAC Control packet type<br>■ 3'b111: The packet is a OAM packet type<br>■ 3'b010: Reserved |
| 15 | ES | Error Summary<br>When this bit is set, it indicates the logical OR of the following bits:<br>■ RDES3[24]: CRC Error<br>■ RDES3[19]: Dribble Error<br>■ RDES3[20]: Receive Error<br>■ RDES3[22]: Watchdog Timeout<br>■ RDES3[21]: Overflow Error<br>■ RDES3[23]: Giant Packet<br>■ RDES2[17]: Destination Address Filter Fail, when Flexible RX Parser is enabled<br>■ RDES2[16]: SA Address Filter Fail, when Flexible RX Parser is enabled<br>This field is valid only when the LD bit of RDES3 is set. |
| 14 | PL | Packet Length<br>These bits indicate the byte length of the received packet that was transferred to system memory (including CRC).<br>This field is valid when the LD bit of RDES3 is set and Overflow Error bits are reset. The packet length also includes the two bytes appended to the Ethernet packet when IP checksum calculation is enabled and the received packet is not a MAC control packet.<br>This field is valid when the LD bit of RDES3 is set. When the Last Descriptor and Error Summary bits are not set, this field indicates the accumulated number of bytes that have been transferred for the current packet. |

### 25.6.10 Receive Context Descriptor

This descriptor is read-only for the application. Only the DMA can write to this descriptor. The context descriptor provides information about the extended status related to the last received packet. The Bit 30 of RDES3 indicates the context type descriptor.

Table 25-25 TDES0 Context Descriptor

| Bit | Name | Description |
|---|---|---|
| 31:0 | RSTL | Receive Packet Timestamp Low<br>The DMA updates this field with least significant 32 bits of the timestamp captured for corresponding Receive packet. When this field and the RTSH field of RDES1 show all-ones value, the timestamp must be considered as corrupt. |

Table 25-26 TDES1 Context Descriptor

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Name | Description |
|---|---|---|
| 31:0 | RSTH | Receive Packet Timestamp High<br>The DMA updates this field with most significant 32 bits of the timestamp captured for corresponding receive packet. When this field and the RTSL field of RDES0 show all-ones value, the timestamp must be considered as corrupt. |

Table 25-27 TDES2 Context Descriptor

| Bit | Name | Description |
|---|---|---|
| 31:0 | Reserved | Reserved |

Table 25-28 TDES3 Context Descriptor

| Bit | Name | Description |
|---|---|---|
| 31 | OWN | Own Bit<br>When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true:<br>■ The DMA completes the packet reception<br>■ The buffers associated with the descriptor are full |
| 30 | CTXT | Receive Context Descriptor<br>When this bit is set, it indicates that the current descriptor is a context descriptor. The DMA writes 1'b1 to this bit for context descriptor. DMA writes 2'b11 to indicate a descriptor error due to all 1s.<br>When CTXT and DE bits are used together, {CTXT, DE}<br>■ 2'b00: Reserved<br>■ 2'b01: Reserved<br>■ 2'b10: Context Descriptor<br>■ 2'b11: Descriptor Error<br>Note: When Descriptor Error occurs, the Receive DMA closes the receive descriptor indicating Descriptor Error. This receive descriptor is skipped and the buffer addresses are not used to write the packet data Receive DMA will set the CDE bit in DMA_CH#_Status register but not the RI bit even when IOC is set, as this is not marked as last receive descriptor for the packet. The subsequent valid receive descriptor is used to write the packet data. |
| 29 | DE | Descriptor Error<br>See the CTXT bit description for details of using theDE bit along with CTXT bit. |
| 28:0 | Reserved | Reserved |

## 25.6.11 Clock Architecture

In RMII mode, reference clock and TX/RX clock can be from CRU or external OSC as following figure. The mux selecting rmii_speed is PHP_GRF_CLK_CON1[2]/PHP_GRF_CLK_CON1[7].

Copyright 2022 © Rockchip Electronics Co., Ltd.

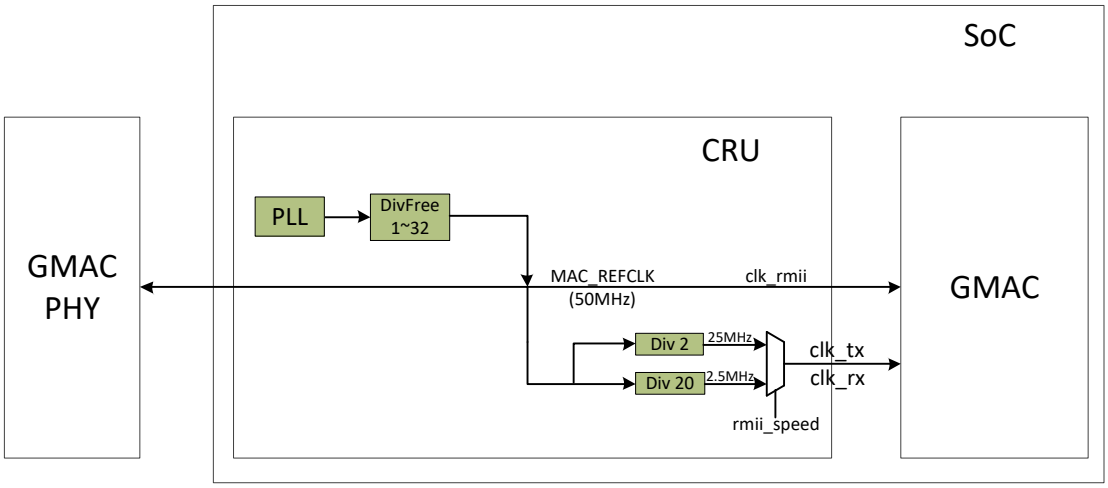



Fig. 25-11 RMII Clock Architecture When Clock Source From CRU

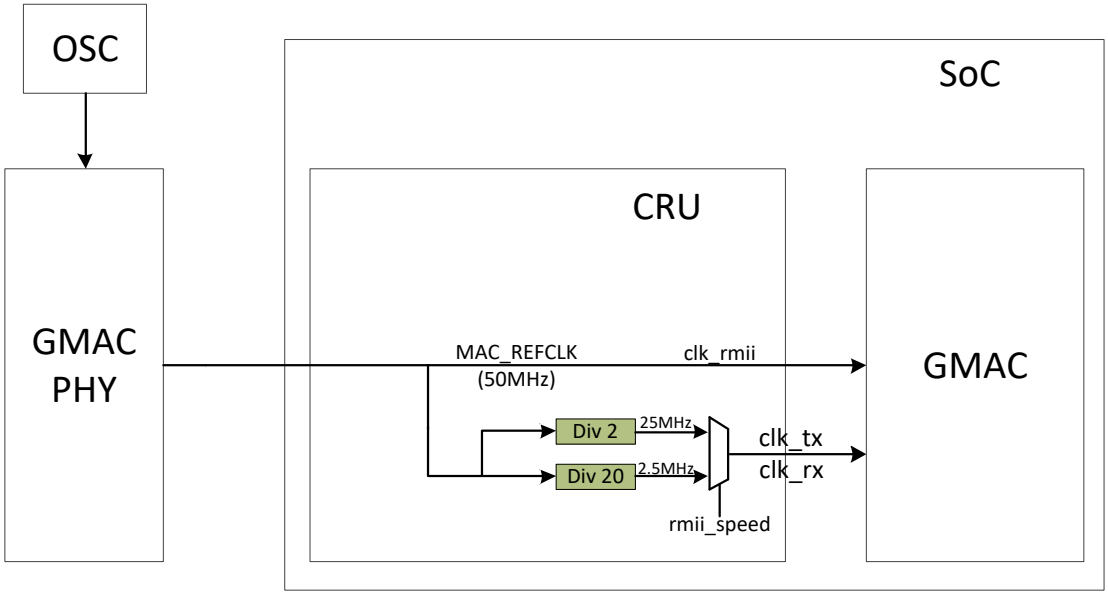



Fig. 25-12 RMII Clock Architecture When Clock Source From External OSC

In RGMII mode, clock architecture only supports that TX clock source is from CRU as following figure.In order to dynamically adjust the timing between TX/RX clocks with data, delayline is integrated in TX and RX clock path. Register SYS_GRF_SOC_CON7[5:2] can enable the delayline and SYS_GRF_SOC_CON8[15:0]/SYS_GRF_SOC_CON9[15:0] is used to determine the delay length. There are 200 delay elements in each delayline.

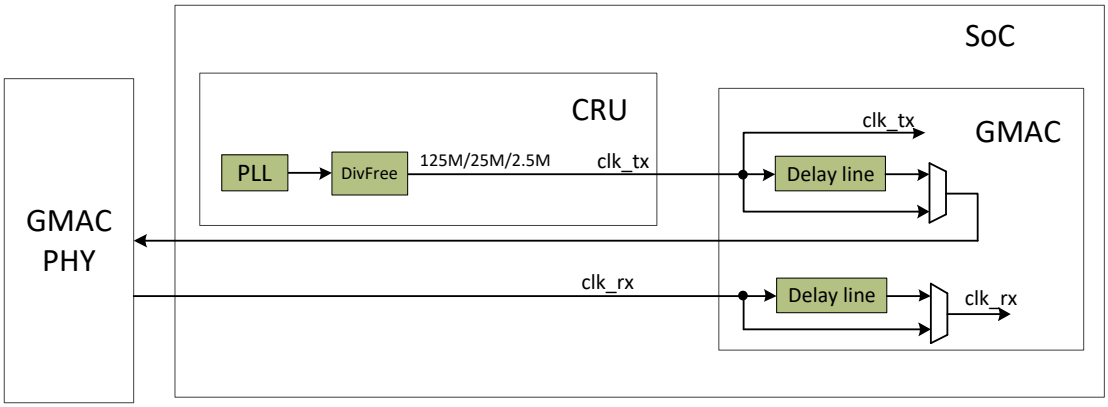



Fig. 25-13 RGMII Clock Architecture When Clock Source From CRU

Copyright 2022 © Rockchip Electronics Co., Ltd.

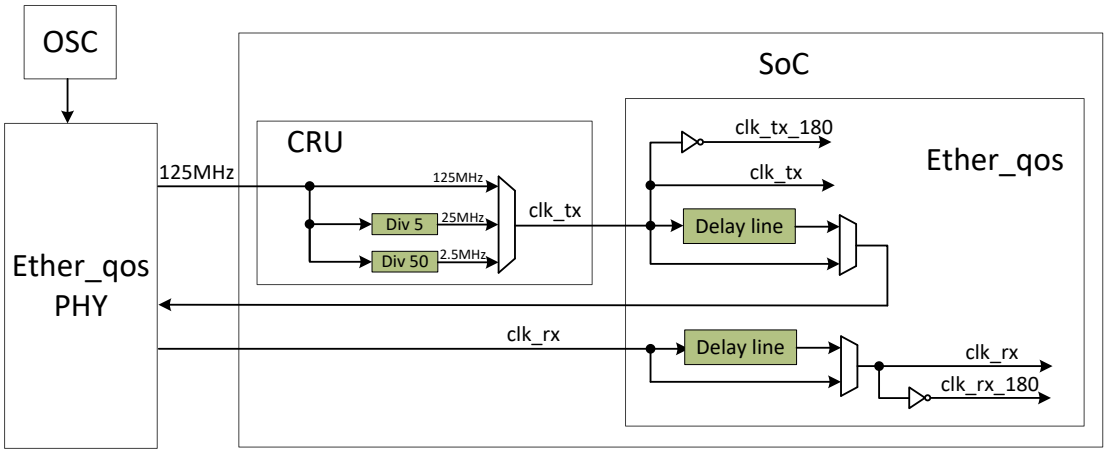



Fig. 25-14 RGMII Clock Architecture When Clock Source From External OSC

Copyright 2022 © Rockchip Electronics Co., Ltd.

# Chapter 26 SAR-ADC

## 26.1 Overview

The ADC is an 8-channel single-ended 12-bit Successive Approximation Register (SAR) A/D Converter. It uses the supply and ground as its reference which avoid the use of any external reference. It converts the analog input signal into 12-bit binary digital codes at maximum conversion rate of 1MSPS with 20MHz A/D converter clock. The input range is typically 0V to 1.8V.

SAR-ADC controller supports the following features:

- Support single mode and series conversion mode.
- In single mode, the conversion operates once each software access.
- In series conversion, controller samples each channel then loops until software stop conversion.
- High/low threshold can be set, higher/lower/between high-low-threshold interrupt can be enabled

## 26.2 Block Diagram

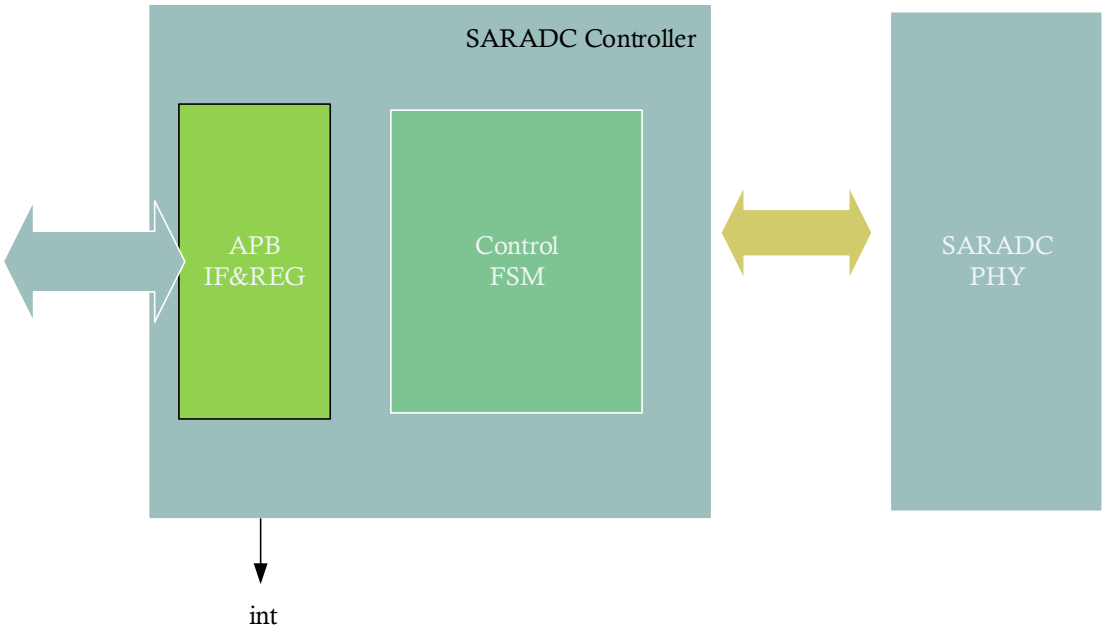



Fig. 26-1 SAR-ADC Block Diagram

SAR-ADC block shows in Fig.1-1. This includes:

- APB Interface
- Control FSM
- SAR-ADC PHY

Software can configure SAR-ADC controller by APB interface, then the inter FSM will communicate with SAR-ADC PHY for limited timing request.

## 26.3 Function Description

SAR-ADC block includes controller and PHY, user cannot directly access SAR-ADC PHY. Software access the SAR-ADC through SAR-ADC controller by APB interface. SAR-ADC controller will sample the conversion result from SAR-ADC PHY.

## 26.4 Register Description

### 26.4.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| SARADC_CONV_CON | 0x0000 | W | 0x00000000 | Conversion control |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| SARADC_T_PD_SOC | 0x0004 | W | 0x00026000 | Timing control for PD to SOC |
| SARADC_T_AS_SOC | 0x0008 | W | 0x00000005 | Timing control for assert SOC |
| SARADC_T_DAS_SOC | 0x000C | W | 0x00000007 | Timing control from dis-assert SOC to change channel |
| SARADC_T_SEL_SOC | 0x0010 | W | 0x00000003 | Timimg control from change channel sel to assert SOC |
| SARADC_HIGH_COMP0 | 0x0014 | W | 0x00000000 | High threshold for ADC output data |
| SARADC_HIGH_COMP1 | 0x0018 | W | 0x00000000 | High threshold for ADC output data |
| SARADC_HIGH_COMP2 | 0x001C | W | 0x00000000 | High threshold for ADC output data |
| SARADC_HIGH_COMP3 | 0x0020 | W | 0x00000000 | High threshold for ADC output data |
| SARADC_HIGH_COMP4 | 0x0024 | W | 0x00000000 | High threshold for ADC output data |
| SARADC_HIGH_COMP5 | 0x0028 | W | 0x00000000 | High threshold for ADC output data |
| SARADC_HIGH_COMP7 | 0x0030 | W | 0x00000000 | High threshold for ADC output data |
| SARADC_HIGH_COMP8 | 0x0034 | W | 0x00000000 | High threshold for ADC output data |
| SARADC_HIGH_COMP9 | 0x0038 | W | 0x00000000 | High threshold for ADC output data |
| SARADC_HIGH_COMP10 | 0x003C | W | 0x00000000 | High threshold for ADC output data |
| SARADC_HIGH_COMP11 | 0x0040 | W | 0x00000000 | High threshold for ADC output data |
| SARADC_HIGH_COMP12 | 0x0044 | W | 0x00000000 | High threshold for ADC output data |
| SARADC_HIGH_COMP13 | 0x0048 | W | 0x00000000 | High threshold for ADC output data |
| SARADC_HIGH_COMP14 | 0x004C | W | 0x00000000 | High threshold for ADC output data |
| SARADC_HIGH_COMP15 | 0x0050 | W | 0x00000000 | High threshold for ADC output data |
| SARADC_LOW_COMP0 | 0x0054 | W | 0x00000000 | Low threshold for ADC output data |
| SARADC_LOW_COMP1 | 0x0058 | W | 0x00000000 | Low threshold for ADC output data |
| SARADC_LOW_COMP2 | 0x005C | W | 0x00000000 | Low threshold for ADC output data |
| SARADC_LOW_COMP3 | 0x0060 | W | 0x00000000 | Low threshold for ADC output data |
| SARADC_LOW_COMP4 | 0x0064 | W | 0x00000000 | Low threshold for ADC output data |
| SARADC_LOW_COMP5 | 0x0068 | W | 0x00000000 | Low threshold for ADC output data |
| SARADC_LOW_COMP6 | 0x006C | W | 0x00000000 | Low threshold for ADC output data |
| SARADC_LOW_COMP7 | 0x0070 | W | 0x00000000 | Low threshold for ADC output data |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| SARADC_LOW_COMP8 | 0x0074 | W | 0x00000000 | Low threshold for ADC output data |
| SARADC_LOW_COMP9 | 0x0078 | W | 0x00000000 | Low threshold for ADC output data |
| SARADC_LOW_COMP10 | 0x007C | W | 0x00000000 | Low threshold for ADC output data |
| SARADC_LOW_COMP11 | 0x0080 | W | 0x00000000 | Low threshold for ADC output data |
| SARADC_LOW_COMP12 | 0x0084 | W | 0x00000000 | Low threshold for ADC output data |
| SARADC_LOW_COMP13 | 0x0088 | W | 0x00000000 | Low threshold for ADC output data |
| SARADC_LOW_COMP14 | 0x008C | W | 0x00000000 | Low threshold for ADC output data |
| SARADC_LOW_COMP15 | 0x0090 | W | 0x00000000 | Low threshold for ADC output data |
| SARADC_DEBOUNCE | 0x0094 | W | 0x00000003 | Threshold debounce |
| SARADC_HT_INT_EN | 0x0098 | W | 0x00000000 | High threshold int enable |
| SARADC_LT_INT_EN | 0x009C | W | 0x00000000 | Low threshold int enable |
| SARADC_MT_INT_EN | 0x0100 | W | 0x00000000 | Middle threshold int enable |
| SARADC_END_INT_EN | 0x0104 | W | 0x00000000 | End conversion int enable |
| SARADC_ST_CON | 0x0108 | W | 0x0000001C | ADC static control |
| SARADC_STATUS | 0x010C | W | 0x00000002 | ADC status |
| SARADC_END_INT_ST | 0x0110 | W | 0x00000000 | End conversion int state |
| SARADC_HT_INT_ST | 0x0114 | W | 0x00000000 | High threshold int state |
| SARADC_LT_INT_ST | 0x0118 | W | 0x00000000 | Low threshold int state |
| SARADC_MT_INT_ST | 0x011C | W | 0x00000000 | Middle threshold int state |
| SARADC_DATA0 | 0x0120 | W | 0x00000000 | ADC output data |
| SARADC_DATA1 | 0x0124 | W | 0x00000000 | ADC output data |
| SARADC_DATA2 | 0x0128 | W | 0x00000000 | ADC output data |
| SARADC_DATA3 | 0x012C | W | 0x00000000 | ADC output data |
| SARADC_DATA4 | 0x0130 | W | 0x00000000 | ADC output data |
| SARADC_DATA5 | 0x0134 | W | 0x00000000 | ADC output data |
| SARADC_DATA6 | 0x0138 | W | 0x00000000 | ADC output data |
| SARADC_DATA7 | 0x013C | W | 0x00000000 | ADC output data |
| SARADC_DATA8 | 0x0140 | W | 0x00000000 | ADC output data |
| SARADC_DATA9 | 0x0144 | W | 0x00000000 | ADC output data |
| SARADC_DATA10 | 0x0148 | W | 0x00000000 | ADC output data |
| SARADC_DATA11 | 0x014C | W | 0x00000000 | ADC output data |
| SARADC_DATA12 | 0x0150 | W | 0x00000000 | ADC output data |
| SARADC_DATA13 | 0x0154 | W | 0x00000000 | ADC output data |
| SARADC_DATA14 | 0x0158 | W | 0x00000000 | ADC output data |
| SARADC_DATA15 | 0x015C | W | 0x00000000 | ADC output data |
| SARADC_AUTO_CH_EN | 0x0160 | W | 0x00000000 | Channel enable in auto channel mode |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

### 26.4.2 Detail Register Description

**SARADC_CONV_CON**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |
| 9 | RW | 0x0 | int_lock<br>This is used to lock the sample data when interrupt happened.<br>1'b1: Enable lock.<br>1'b0: Disable lock. |
| 8 | RW | 0x0 | as_pd_mode<br>If this bit is set to 1'b1, each time conversion ends, PD will be asserted. Then next time conversion starts, PD will be set to low auto automaticly. This is not used in single mode. |
| 7 | W1C | 0x0 | end_conv<br>End conversion, this is not used when CONV_CON[5] is set to 1'b1. If this bit set to 1'b1, PD will set to 1'b1 after the last conversion and this bit will be cleared to 1'b0. |
| 6 | RW | 0x0 | auto_channel_mode<br>Auto channel mode.<br>If this is enable, channel will be round auto according which is set in AUTO_CH_EN. |
| 5 | RW | 0x0 | single_pd_mode<br>Single conversion mode. If this bit is set to 1, conversion only operate once, then PD single will be set to 1. |
| 4 | W1C | 0x0 | start_adc<br>Enable ADC, if this bit set to one, conversion will start. Then this bit will be clear to 0. |
| 3:0 | RW | 0x0 | channel_sel<br>Channel for SARADC, 8 channels are supported. This fileld is not used when CONV_CON[6] is set to 1.<br>4'd0: sel channel 0.<br>4'd1: sel channel 1.<br>4'd2: sel channel 2.<br>4'd3: sel channel 3.<br>4'd4: sel channel 4.<br>4'd5: sel channel 5.<br>4'd6: sel channel 6.<br>4'd7: sel channel 7. |

**SARADC_T_PD_SOC**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x000 | reserved |
| 7:0 | RW | 0x13 | t_pd_soc<br>Timing control between power up to start-of-conversion. |

**SARADC_T_AS_SOC**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000005 | t_as_soc<br>Timing control for assert SOC signal. |

**SARADC_T_DAS_SOC**

Address: Operational Base + offset (0x000C)

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000007 | t_das_soc<br>Timing from dis-assret SOC to channel sel change. |

**SARADC_T_SEL_SOC**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0003 | t_sel_soc<br>Timing from channel load to SOC assert. |

**SARADC_HIGH_COMP0**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | high_comp0<br>High threshold for ADC output data for channel 0. |

**SARADC_HIGH_COMP1**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | high_comp1<br>High threshold for ADC output data for channel 1. |

**SARADC_HIGH_COMP2**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | high_comp2<br>High threshold for ADC output data for channel 2. |

**SARADC_HIGH_COMP3**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | high_comp3<br>High threshold for ADC output data for channel 3. |

**SARADC_HIGH_COMP4**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | high_comp4<br>High threshold for ADC output data for channel 4. |

**SARADC_HIGH_COMP5**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | high_comp5<br>High threshold for ADC output data for channel 5. |

**SARADC_HIGH_COMP7**

Address: Operational Base + offset (0x0030)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | high_comp7<br>High threshold for ADC output data for channel 7. |

**SARADC_HIGH_COMP8**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | high_comp8<br>Not used in this application. |

**SARADC_HIGH_COMP9**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | high_comp9<br>Not used in this application. |

**SARADC_HIGH_COMP10**

Address: Operational Base + offset (0x003C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | high_comp10<br>Not used in this application. |

**SARADC_HIGH_COMP11**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | high_comp11<br>Not used in this application. |

**SARADC_HIGH_COMP12**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | high_comp12<br>Not used in this application. |

**SARADC_HIGH_COMP13**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | high_comp13<br>Not used in this application. |

**SARADC_HIGH_COMP14**

Address: Operational Base + offset (0x004C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | high_comp14<br>Not used in this application. |

**SARADC_HIGH_COMP15**

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | high_comp15<br>Not used in this application. |

**SARADC_LOW_COMP0**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | low_comp0<br>Low threshold for ADC output data for channel 0. |

**SARADC_LOW_COMP1**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | low_comp1<br>Low threshold for ADC output data for channel 1. |

**SARADC_LOW_COMP2**

Address: Operational Base + offset (0x005C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | low_comp2<br>Low threshold for ADC output data for channel 2. |

**SARADC_LOW_COMP3**

Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | low_comp3<br>Low threshold for ADC output data for channel 3. |

**SARADC_LOW_COMP4**

Address: Operational Base + offset (0x0064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | low_comp4<br>Low threshold for ADC output data for channel 4. |

**SARADC_LOW_COMP5**

Address: Operational Base + offset (0x0068)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | low_comp5<br>Low threshold for ADC output data for channel 5. |

**SARADC_LOW_COMP6**

Address: Operational Base + offset (0x006C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | low_comp6<br>Low threshold for ADC output data for channel 6. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**SARADC_LOW_COMP7**

Address: Operational Base + offset (0x0070)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | low_comp7<br>Low threshold for ADC output data for channel 7. |

**SARADC_LOW_COMP8**

Address: Operational Base + offset (0x0074)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | low_comp8<br>Not used in this application. |

**SARADC_LOW_COMP9**

Address: Operational Base + offset (0x0078)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | low_comp9<br>Not used in this application. |

**SARADC_LOW_COMP10**

Address: Operational Base + offset (0x007C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | low_comp10<br>Not used in this application. |

**SARADC_LOW_COMP11**

Address: Operational Base + offset (0x0080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | low_comp11<br>Not used in this application. |

**SARADC_LOW_COMP12**

Address: Operational Base + offset (0x0084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | low_comp12<br>Not used in this application. |

**SARADC_LOW_COMP13**

Address: Operational Base + offset (0x0088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | low_comp13<br>Not used in this application. |

**SARADC_LOW_COMP14**

Address: Operational Base + offset (0x008C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | low_comp14<br>Not used in this application. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**SARADC_LOW_COMP15**

Address: Operational Base + offset (0x0090)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RW | 0x000 | low_comp15<br>Not used in this application. |

**SARADC_DEBOUNCE**

Address: Operational Base + offset (0x0094)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x03 | debounce<br>ADC controller will only generate interrupt data is higher/lower/between setting threshold for "debounce" times. |

**SARADC_HT_INT_EN**

Address: Operational Base + offset (0x0098)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | ht_int_en15<br>Not used in this application. |
| 14 | RW | 0x0 | ht_int_en14<br>Not used in this application. |
| 13 | RW | 0x0 | ht_int_en13<br>Not used in this application. |
| 12 | RW | 0x0 | ht_int_en12<br>Not used in this application. |
| 11 | RW | 0x0 | ht_int_en11<br>Not used in this application. |
| 10 | RW | 0x0 | ht_int_en10<br>Not used in this application. |
| 9 | RW | 0x0 | ht_int_en9<br>Not used in this application. |
| 8 | RW | 0x0 | ht_int_en8<br>Not used in this application. |
| 7 | RW | 0x0 | ht_int_en7<br>High threshold interrupt for channel7.<br>1'b1: Enable ht intr.<br>1'b0: Disable ht intr. |
| 6 | RW | 0x0 | ht_int_en6<br>High threshold interrupt for channel6.<br>1'b1: Enable ht intr.<br>1'b0: Disable ht intr. |
| 5 | RW | 0x0 | ht_int_en5<br>High threshold interrupt for channel5.<br>1'b1: Enable ht intr.<br>1'b0: Disable ht intr. |
| 4 | RW | 0x0 | ht_int_en4<br>High threshold interrupt for channel4.<br>1'b1: Enable ht intr.<br>1'b0: Disable ht intr. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | ht_int_en3<br>High threshold interrupt for channel3.<br>1'b1: Enable ht intr.<br>1'b0: Disable ht intr. |
| 2 | RW | 0x0 | ht_int_en2<br>High threshold interrupt for channel2.<br>1'b1: Enable ht intr.<br>1'b0: Disable ht intr. |
| 1 | RW | 0x0 | ht_int_en1<br>High threshold interrupt for channel1.<br>1'b1: Enable ht intr.<br>1'b0: Disable ht intr. |
| 0 | RW | 0x0 | ht_int_en0<br>High threshold interrupt for channel0.<br>1'b1: Enable ht intr.<br>1'b0: Disable ht intr. |

**SARADC_LT_INT_EN**

Address: Operational Base + offset (0x009C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | lt_int_en15<br>Not used in this application. |
| 14 | RW | 0x0 | lt_int_en14<br>Not used in this application. |
| 13 | RW | 0x0 | lt_int_en13<br>Not used in this application. |
| 12 | RW | 0x0 | lt_int_en12<br>Not used in this application. |
| 11 | RW | 0x0 | lt_int_en11<br>Not used in this application. |
| 10 | RW | 0x0 | lt_int_en10<br>Not used in this application. |
| 9 | RW | 0x0 | lt_int_en9<br>Not used in this application. |
| 8 | RW | 0x0 | lt_int_en8<br>Not used in this application. |
| 7 | RW | 0x0 | lt_int_en7<br>Low threshold interrupt for channel7.<br>1'b1: Enable lt intr.<br>1'b0: Disable lt intr. |
| 6 | RW | 0x0 | lt_int_en6<br>Low threshold interrupt for channel6.<br>1'b1: Enable lt intr.<br>1'b0: Disable lt intr. |
| 5 | RW | 0x0 | lt_int_en5<br>Low threshold interrupt for channel5.<br>1'b1: Enable lt intr.<br>1'b0: Disable lt intr. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | lt_int_en4<br>Low threshold interrupt for channel4.<br>1'b1: Enable lt intr.<br>1'b0: Disable lt intr. |
| 3 | RW | 0x0 | lt_int_en3<br>Low threshold interrupt for channel3.<br>1'b1: Enable lt intr.<br>1'b0: Disable lt intr. |
| 2 | RW | 0x0 | lt_int_en2<br>Low threshold interrupt for channel2.<br>1'b1: Enable lt intr.<br>1'b0: Disable lt intr. |
| 1 | RW | 0x0 | lt_int_en1<br>Low threshold interrupt for channel1.<br>1'b1: Enable lt intr.<br>1'b0: Disable lt intr. |
| 0 | RW | 0x0 | lt_int_en0<br>Low threshold interrupt for channel0.<br>1'b1: Enable lt intr.<br>1'b0: Disable lt intr. |

**SARADC_MT_INT_EN**

Address: Operational Base + offset (0x0100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | mt_int_en15<br>Not used in this application. |
| 14 | RW | 0x0 | mt_int_en14<br>Not used in this application. |
| 13 | RW | 0x0 | mt_int_en13<br>Not used in this application. |
| 12 | RW | 0x0 | mt_int_en12<br>Not used in this application. |
| 11 | RW | 0x0 | mt_int_en11<br>Not used in this application. |
| 10 | RW | 0x0 | mt_int_en10<br>Not used in this application. |
| 9 | RW | 0x0 | mt_int_en9<br>Not used in this application. |
| 8 | RW | 0x0 | mt_int_en8<br>Not used in this application. |
| 7 | RW | 0x0 | mt_int_en7<br>Middle threshold interrupt for channel7.<br>1'b1: Enable mt intr.<br>1'b0: Disable mt intr. |
| 6 | RW | 0x0 | mt_int_en6<br>Middle threshold interrupt for channel6.<br>1'b1: Enable mt intr.<br>1'b0: Disable mt intr. |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | mt_int_en5<br>Middle threshold interrupt for channel5.<br>1'b1: Enable mt intr.<br>1'b0: Disable mt intr. |
| 4 | RW | 0x0 | mt_int_en4<br>Middle threshold interrupt for channel4.<br>1'b1: Enable mt intr.<br>1'b0: Disable mt intr. |
| 3 | RW | 0x0 | mt_int_en3<br>Middle threshold interrupt for channel3.<br>1'b1: Enable mt intr.<br>1'b0: Disable mt intr. |
| 2 | RW | 0x0 | mt_int_en2<br>Middle threshold interrupt for channel2.<br>1'b1: Enable mt intr.<br>1'b0: Disable mt intr. |
| 1 | RW | 0x0 | mt_int_en1<br>Middle threshold interrupt for channel1.<br>1'b1: Enable mt intr.<br>1'b0: Disable mt intr. |
| 0 | RW | 0x0 | mt_int_en0<br>Middle threshold interrupt for channel0.<br>1'b1: Enable mt intr.<br>1'b0: Disable mt intr. |

**SARADC_END_INT_EN**

Address: Operational Base + offset (0x0104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | end_int_en<br>1'b1: Enable end conversion intr.<br>1'b0: Disable end conversion intr. |

**SARADC_ST_CON**

Address: Operational Base + offset (0x0108)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5:3 | RW | 0x3 | ictrl<br>Control the bias current of the preamplifier in the SAR-ADC |
| 2:0 | RW | 0x4 | cctrl<br>Control the capacitance of the capacitor DAC array, which is related to the linearity of the SAR-ADC. |

**SARADC_STATUS**

Address: Operational Base + offset (0x010C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5:2 | RO | 0x0 | sel<br>Adc channel sel. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RO | 0x1 | pd<br>1'b1: ADC is power down.<br>1'b0: ADC is power up and in conversion. |
| 0 | RO | 0x0 | conv_st<br>Conversion status<br>1'b1: ADC controller fsm is busy.<br>1'b0: ADC controller fsm is idle. |

**SARADC_END_INT_ST**

Address: Operational Base + offset (0x0110)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | W1C | 0x0 | end_int_st<br>ADC end conversion interrupt status.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |

**SARADC_HT_INT_ST**

Address: Operational Base + offset (0x0114)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | W1C | 0x0000 | reserved |
| 15 | W1C | 0x0 | ht_int_st15<br>Not used in this application. |
| 14 | W1C | 0x0 | ht_int_st14<br>Not used in this application. |
| 13 | W1C | 0x0 | ht_int_st13<br>Not used in this application. |
| 12 | W1C | 0x0 | ht_int_st12<br>Not used in this application. |
| 11 | W1C | 0x0 | ht_int_st11<br>Not used in this application. |
| 10 | W1C | 0x0 | ht_int_st10<br>Not used in this application. |
| 9 | W1C | 0x0 | ht_int_st9<br>Not used in this application. |
| 8 | W1C | 0x0 | ht_int_st8<br>Not used in this application. |
| 7 | W1C | 0x0 | ht_int_st7<br>High threshold interrupt state for channel7.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |
| 6 | W1C | 0x0 | ht_int_st6<br>High threshold interrupt state for channel6.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |
| 5 | W1C | 0x0 | ht_int_st5<br>High threshold interrupt state for channel5.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |
| 4 | W1C | 0x0 | ht_int_st4<br>High threshold interrupt state for channel4.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | W1C | 0x0 | ht_int_st3<br>High threshold interrupt state for channel3.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |
| 2 | W1C | 0x0 | ht_int_st2<br>High threshold interrupt state for channel2.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |
| 1 | W1C | 0x0 | ht_int_st1<br>High threshold interrupt state for channel1.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |
| 0 | W1C | 0x0 | ht_int_st0<br>High threshold interrupt state for channel0.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |

**SARADC_LT_INT_ST**

Address: Operational Base + offset (0x0118)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15 | W1C | 0x0 | lt_int_st15<br>Not used in this application. |
| 14 | W1C | 0x0 | lt_int_st14<br>Not used in this application. |
| 13 | W1C | 0x0 | lt_int_st13<br>Not used in this application. |
| 12 | W1C | 0x0 | lt_int_st12<br>Not used in this application. |
| 11 | W1C | 0x0 | lt_int_st11<br>Not used in this application. |
| 10 | W1C | 0x0 | lt_int_st10<br>Not used in this application. |
| 9 | W1C | 0x0 | lt_int_st9<br>Not used in this application. |
| 8 | W1C | 0x0 | lt_int_st8<br>Not used in this application. |
| 7 | W1C | 0x0 | lt_int_st7<br>Low threshold interrupt state for channel7.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |
| 6 | W1C | 0x0 | lt_int_st6<br>Low threshold interrupt state for channel6.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |
| 5 | W1C | 0x0 | lt_int_st5<br>Low threshold interrupt state for channel5.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |
| 4 | W1C | 0x0 | lt_int_st4<br>Low threshold interrupt state for channel4.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | W1C | 0x0 | lt_int_st3<br>Low threshold interrupt state for channel3.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |
| 2 | W1C | 0x0 | lt_int_st2<br>Low threshold interrupt state for channel2.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |
| 1 | W1C | 0x0 | lt_int_st1<br>Low threshold interrupt state for channel1.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |
| 0 | W1C | 0x0 | lt_int_st0<br>Low threshold interrupt state for channel0.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |

**SARADC_MT_INT_ST**

Address: Operational Base + offset (0x011C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15 | W1C | 0x0 | mt_int_st15<br>Not used in this application. |
| 14 | W1C | 0x0 | mt_int_st14<br>Not used in this application. |
| 13 | W1C | 0x0 | mt_int_st13<br>Not used in this application. |
| 12 | W1C | 0x0 | mt_int_st12<br>Not used in this application. |
| 11 | W1C | 0x0 | mt_int_st11<br>Not used in this application. |
| 10 | W1C | 0x0 | mt_int_st10<br>Not used in this application. |
| 9 | W1C | 0x0 | mt_int_st9<br>Not used in this application. |
| 8 | W1C | 0x0 | mt_int_st8<br>Not used in this application. |
| 7 | W1C | 0x0 | mt_int_st7<br>Between high and low threshold interrupt state for channel7.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |
| 6 | W1C | 0x0 | mt_int_st6<br>Between high and low threshold interrupt state for channel6.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |
| 5 | W1C | 0x0 | mt_int_st5<br>Between high and low threshold interrupt state for channel5.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |
| 4 | W1C | 0x0 | mt_int_st4<br>Between high and low threshold interrupt state for channel4.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | W1C | 0x0 | mt_int_st3<br>Between high and low threshold interrupt state for channel3.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |
| 2 | W1C | 0x0 | mt_int_st2<br>Between high and low threshold interrupt state for channel2.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |
| 1 | W1C | 0x0 | mt_int_st1<br>Between high and low threshold interrupt state for channel1.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |
| 0 | W1C | 0x0 | mt_int_st0<br>Between high and low threshold interrupt state for channel0.<br>1'b1: Interrupt happened.<br>1'b0: Interrupt not happened. |

**SARADC_DATA0**

Address: Operational Base + offset (0x0120)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | data0<br>ADC channel 0 data. |

**SARADC_DATA1**

Address: Operational Base + offset (0x0124)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | data1<br>ADC channel 1 data. |

**SARADC_DATA2**

Address: Operational Base + offset (0x0128)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | data2<br>ADC channel 2 data. |

**SARADC_DATA3**

Address: Operational Base + offset (0x012C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | data3<br>ADC channel 3 data. |

**SARADC_DATA4**

Address: Operational Base + offset (0x0130)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | data4<br>ADC channel 4 data. |

**SARADC_DATA5**

Address: Operational Base + offset (0x0134)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | data5<br>ADC channel 5 data. |

**SARADC_DATA6**

Address: Operational Base + offset (0x0138)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | data6<br>ADC channel 6 data. |

**SARADC_DATA7**

Address: Operational Base + offset (0x013C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | data7<br>ADC channel 7 data. |

**SARADC_DATA8**

Address: Operational Base + offset (0x0140)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | data8<br>Not used in this application. |

**SARADC_DATA9**

Address: Operational Base + offset (0x0144)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | data9<br>Not used in this application. |

**SARADC_DATA10**

Address: Operational Base + offset (0x0148)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | data10<br>Not used in this application. |

**SARADC_DATA11**

Address: Operational Base + offset (0x014C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | data11<br>Not used in this application. |

**SARADC_DATA12**

Address: Operational Base + offset (0x0150)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | data12<br>Not used in this application. |

**SARADC_DATA13**

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

Address: Operational Base + offset (0x0154)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | data13<br>Not used in this application. |

**SARADC_DATA14**

Address: Operational Base + offset (0x0158)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | data14<br>Not used in this application. |

**SARADC_DATA15**

Address: Operational Base + offset (0x015C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:0 | RO | 0x000 | data15<br>Not used in this application. |

**SARADC_AUTO_CH_EN**

Address: Operational Base + offset (0x0160)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | WO | 0x0000 | write_enable<br>Write enable for lower 16bits, each bit is individual.<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15 | RW | 0x0 | auto_ch15_en<br>Not used in this application. |
| 14 | RW | 0x0 | auto_ch14_en<br>Not used in this application. |
| 13 | RW | 0x0 | auto_ch13_en<br>Not used in this application. |
| 12 | RW | 0x0 | auto_ch12_en<br>Not used in this application. |
| 11 | RW | 0x0 | auto_ch11_en<br>Not used in this application. |
| 10 | RW | 0x0 | auto_ch10_en<br>Not used in this application. |
| 9 | RW | 0x0 | auto_ch9_en<br>Not used in this application. |
| 8 | RW | 0x0 | auto_ch8_en<br>Not used in this application. |
| 7 | RW | 0x0 | auto_ch7_en<br>Enable channel 7 in auto channel mode. |
| 6 | RW | 0x0 | auto_ch6_en<br>Enable channel 6 in auto channel mode. |
| 5 | RW | 0x0 | auto_ch5_en<br>Enable channel 5 in auto channel mode. |
| 4 | RW | 0x0 | auto_ch4_en<br>Enable channel 4 in auto channel mode. |
| 3 | RW | 0x0 | auto_ch3_en<br>Enable channel 3 in auto channel mode. |
| 2 | RW | 0x0 | auto_ch2_en<br>Enable channel 2 in auto channel mode. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | auto_ch1_en<br>Enable channel 1 in auto channel mode. |
| 0 | RW | 0x0 | auto_ch0_en<br>Enable channel 0 in auto channel mode. |

## 26.5 Timing Diagram

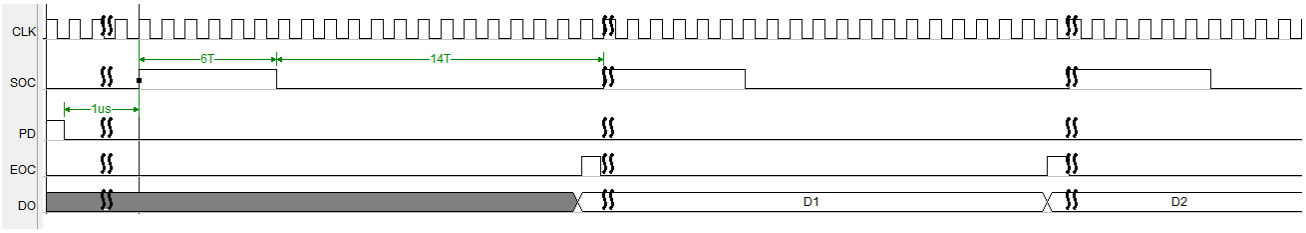



Fig. 26-2 SAR-ADC Timing Diagram

SAR-ADC timing diagram is shown in Fig.1-2. When PD (power down) comes to low, wait 1us then assert SOC to start conversion. SOC should hold for 6 clock cycles (CLK), then after 14 clock cycle EOC pulse with conversion data (DO). CLK is suggested to be 20MHz, if frequency could not meet, set frequency close to 20MHz but not over 20MHz.

Don't need to care the channel changing, this will be met by internal FSM. Also if software want to end conversion by setting register SARADC_CONV_CON, PD may not be asserted immediately but wait the latest conversion ends.

## 26.6 Application Notes

**Steps of ADC conversion in series conversion mode:**

- Decide which channel should be used and whether auto_channel mode should be set. In auto_channel mode channel will be changed from 0-7 then to 0. Please refer to SARADC_CONV_CON register.
- Set SARADC_CONV_CON[4] to 1'b1, then conversion will start.
- If conversion wants to be ended, set SARADC_CONV_CON[7] to 1'b1.
- Conversion could be read from SARADC_DATAn (n is from 0-7).
- If threshold compare interrupt wants to be used, high/low threshold could be set, and interrupt should be set as application.
- If auto_channel mode is not set, you could set the channel as application.

**Steps of adc conversion in single mode:**

- Decide which channel should be used and set SARADC_CONV_CON[3:0].
- Set SARADC_CONV_CON[5] to 1'b1.
- Set SARADC_CONV_CON[4] to 1'b1, then conversion will start.
- Conversion only operates once then ends. PD will be asserted and PD status could be got by reading SARADC_STATUS.
- Conversion could be read from SARADC_DATAn (n is from 0-7).

Copyright 2022 © Rockchip Electronics Co., Ltd.

# Chapter 27 Digital Audio Codec

## 27.1 Overview

Digital Audio Codec is a 16-bit digital audio encoder which supports multiple sample rates. It is mainly composed of digital DAC. The aim of digital DAC is to process the data received from I2S/PCM interface through filters, volume control and modulation.
The Digital Audio Codec supports the following features.

- Support 8-bit APB bus slave interface
- Support 2-channel digital DAC
- Support I2S/PCM interface
- Support I2S/PCM master and slave mode
- Support 2-channel audio receiving in I2S mode
- Support 2-channel audio receiving in PCM mode
- Support I2S normal, left and right justified mode serial audio data transfer
- Support PCM early, late1, late2, late3 mode serial audio data transfer
- Support MSB or LSB first serial audio data transfer
- Support configurable SCLK and LRCK polarity
- Support 16 bit sample resolution
- Support programmable left and right channel exchangeable in I2S mode and PCM mode
- Support three modes of mixing for every digital DAC channel
- Support volume control
- Support programmable negative and positive volume gain

## 27.2 Block Diagram

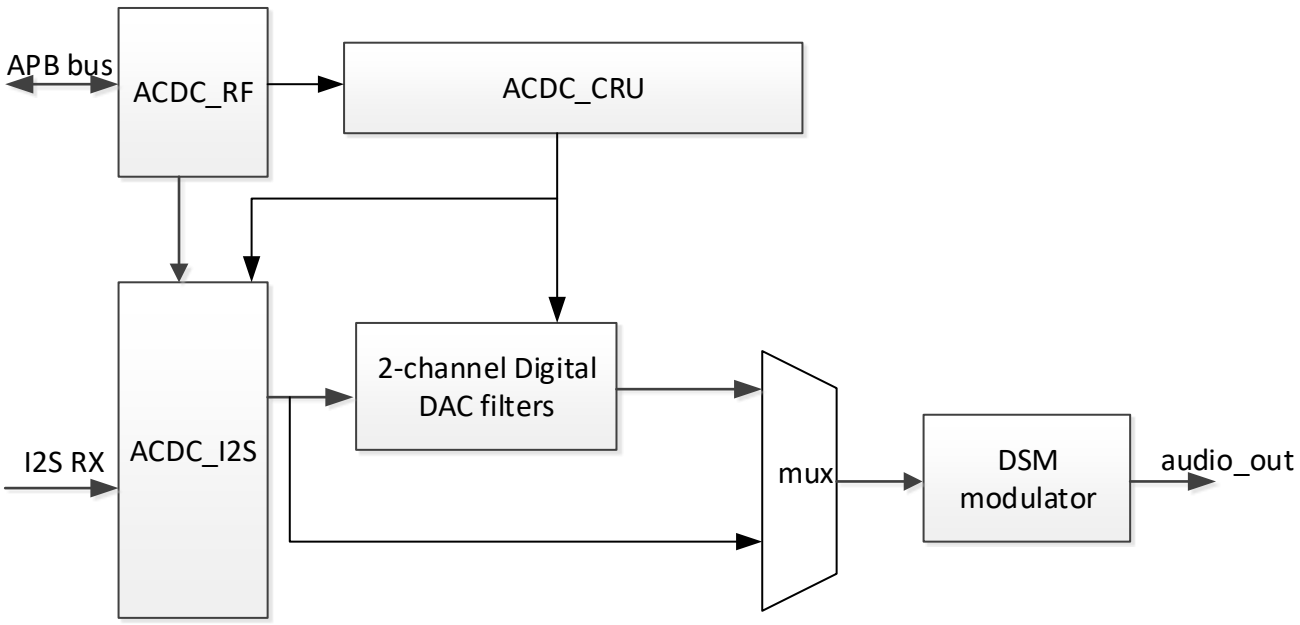



Fig. 27-1 Digital Audio Codec Block Diagram

**ACDC_RF**
The ACDC_RF implements the 8-bit APB slave operation through APB bus. It is responsible for configuring the operation registers of other modules.
**ACDC_CRU**
The ACDC_CRU implements clock and reset generation function. It is responsible for generating sample clock, digital DAC operation clock and I2S operation clock.
**Digital DAC**
There are 2 digital DAC channels. The digital DAC receives audio data from ACDC_I2S module. It includes one CIC filter, one high-pass filter, several low-pass decimation filters

Copyright 2022 © Rockchip Electronics Co., Ltd. 

and other audio signal processing related modules. The output of digital DAC is sent to DSM modular before transmitting outside.

**ACDC_I2S**

The I2S/PCM audio interface can be configured to master mode or slave mode. In Master Mode, SCLK and LRCK are configured as output. In slave mode, SCLK and LRCK are configured as input. The ACDC_I2S module can only operate in RX mode. When in RX mode, it receives audio data from I2S RX interface and sends it to digital DAC.

**DSM Modulator**

It is a modulator that converts 16 bits audio sample data to 1 bit audio data.

# 27.3 Function description

The I2S/PCM interface of Digital Audio Codec is connected to the I2S3 controller. Please refer to the I2S chapter for detailed information about I2S and PCM format that Digital Audio Codec supports.

## 27.3.1 Filters of Digital DAC

I2S module receives two-channel audio data from I2S RX interface and drives it to the digital DAC which supports mixing function or directly to the DSM modulator. How to pour 2-channel audio data into 2-channel digital DAC can be achieved by programming mixing mode.

The 2-channel digital DAC includes a high-pass filter and a maximum of 5 half-band filters. The high-pass filter is used to filter DC components in audio data stream. Result of high-pass filter is sent to the digital DAC volume control module. The input of 5 half-band filters comes from output of volume control module with each perform 2-times interpolation. But not all of them are working all the time. How many of them are needed to work depends on the sample rate of digital DAC. The result of half-band filters is sent to a modulator.

## 27.3.2 Volume Control

For digital DAC, output of high-pass filters is fed into volume control module. The volume control module inside digital DAC contains several sub-modules such as peak detect, frequency cross zero detect, LIMITER and digital gain control. It can be digitally attenuated over a range of -96dB~0dB in 0.375dB/step for negative gain and amplified over a range of 0dB~96dB in 0.375dB/step for positive gain. Whether is attenuated or amplified can be software programmed.

# 27.4 Register Description

## 27.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

## 27.4.2 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| ACDCDIG_DACVUCTL | 0x0140 | W | 0x00000001 | DAC Volume Control Register |
| ACDCDIG_DACVUCTIME | 0x0144 | W | 0x00000000 | DAC Volume Control Time Limit Register |
| ACDCDIG_DACDIGEN | 0x0148 | W | 0x00000000 | DAC Digital Enable Register |
| ACDCDIG_DACCLKCTRL | 0x014C | W | 0x00000000 | DAC Clock Control Register |
| ACDCDIG_DACINT_DIV | 0x0154 | W | 0x00000007 | DAC Integer Clock Divider Register |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| ACDCDIG_DACSCLKRXINT_DIV | 0x0160 | W | 0x0000001F | I2S SCLK RX Integer Divider Register |
| ACDCDIG_DACPWM_DIV | 0x0164 | W | 0x00000003 | PWM Mode Integer Divider Register |
| ACDCDIG_DACPWM_CTRL | 0x0168 | W | 0x00000000 | PWM Mode Control Register |
| ACDCDIG_DACCFG1 | 0x0184 | W | 0x00000004 | DAC Configure Register 1 |
| ACDCDIG_DACMUTE | 0x0188 | W | 0x00000000 | DAC Mute Control Register |
| ACDCDIG_DACMUTEST | 0x018C | W | 0x00000000 | DAC Mute Status Register |
| ACDCDIG_DACVOLL0 | 0x0190 | W | 0x00000000 | Volume of DAC Left Channel 0 Register |
| ACDCDIG_DACVOLR0 | 0x01A0 | W | 0x00000000 | Volume of DAC right Channel 1 Register |
| ACDCDIG_DACVOGP | 0x01B0 | W | 0x00000000 | DAC Volume Gain Polarity Register |
| ACDCDIG_DACRVOLL0 | 0x01B4 | W | 0x000000FF | Internal Volume of DAC Left Channel 0 Register |
| ACDCDIG_DACRVOLR0 | 0x01C4 | W | 0x000000FF | Internal Volume of DAC right Channel 1 Register |
| ACDCDIG_DACLMT0 | 0x01D4 | W | 0x00000000 | DAC Limiter Register 0 |
| ACDCDIG_DACLMT1 | 0x01D8 | W | 0x00000000 | DAC Limiter Register 1 |
| ACDCDIG_DACLMT2 | 0x01DC | W | 0x00000000 | DAC Limiter Register 2 |
| ACDCDIG_DACMIXCTRLL | 0x01E0 | W | 0x00000000 | DAC Mixing Control Register Of Left Channels |
| ACDCDIG_DACMIXCTRLR | 0x01E4 | W | 0x00000000 | DAC Mixing Control Register Of right Channels |
| ACDCDIG_DACHPF | 0x01E8 | W | 0x00000000 | DAC High-pass Filter Control Register |
| ACDCDIG_I2S_RXCR0 | 0x030C | W | 0x0000000F | Receive Operation Control Register 0 |
| ACDCDIG_I2S_RXCR1 | 0x0310 | W | 0x00000000 | Receive Operation Control Register 1 |
| ACDCDIG_I2S_CKR0 | 0x0314 | W | 0x00000000 | Clock Generation Register 0 |
| ACDCDIG_I2S_CKR1 | 0x0318 | W | 0x00000000 | Clock Generation Register 1 |
| ACDCDIG_I2S_XFER | 0x031C | W | 0x00000000 | Transfer Start Register |
| ACDCDIG_I2S_CLR | 0x0320 | W | 0x00000000 | SCLK Domain Logic Clear Register |
| ACDCDIG_VERSION | 0x0380 | W | 0x00000002 | Version Register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 27.4.3 Detail Registers Description

### ACDCDIG_DACVUCTL

Address: Operational Base + offset (0x0140)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | dac_byps<br>Digital DAC volume control bypass.<br>1'b0: Digital DAC volume control enable<br>1'b1: Digital DAC volume control bypass |
| 1 | RW | 0x0 | dacfade<br>Digital DAC volume adjust mode.<br>1'b0: Update to new volume immediately.<br>1'b1: Update volume as daczdt field describes. |
| 0 | RW | 0x1 | daczdt<br>Digital DAC volume cross zero detect enable. It works when dac_byps is 1'b0 and dacfade is 1'b1.<br>1'b0: Volume adjusts every sample.<br>1'b1: Volume adjusts only when audio waveform crosses zero or volume-control time-limit condition meets. |

**ACDCDIG_DACVUCTIME**

Address: Operational Base + offset (0x0144)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | dacvuct<br>Volume control time limit, valid only in fade cross zero mode.<br>Time limit = dacvuct*(1/sample rate)<br>Unit: Sample rate |

**ACDCDIG_DACDIGEN**

Address: Operational Base + offset (0x0148)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4 | RW | 0x0 | dacglben<br>Global enable of all Digital DAC channels. Only when dacglben and the enable signal corresponding to each Digital DAC channel is valid before starting work.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | dacen_l0r1<br>Digital DAC left channel 0 and right channel 1 enable.<br>1'b0: Disable<br>1'b1: Enable |

**ACDCDIG_DACCLKCTRL**

Address: Operational Base + offset (0x014C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | dac_cke<br>Digital DAC operation clock enable.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | i2srx_cke<br>Clock enable of internal I2S RX channel.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | cke_bclkrx<br>Clock enable of sclk_out_rx.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | dac_sync_ena<br>Enable of the synchronization signal used internally generated by Digital DAC.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RO | 0x0 | dac_sync_status<br>There is a counter to generate synchronization signal of Digital DAC. In order to ensure the integrity of synchronization signal, it is necessary to read back dac_sync_status to judge whether the counter stops working when dac_sync_ena is set from 1'b1 to 1'b0. If the signal is read back to 1'b0, it means that the counter stops working and the synchronization signal of Digital DAC is complete. |
| 0 | RW | 0x0 | dac_mod_attenu_en<br>When enabled, the input of the Digital DAC modulator is attenuated by 6dB, and the output of the Digital DAC modulator is increased by 6dB.<br>1'b0: Disable<br>1'b1: Enable |

**ACDCDIG_DACINT_DIV**

Address: Operational Base + offset (0x0154)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x07 | int_div_con<br>Integer clock divider to provide 6.144/5.644/4.096MHz sample clock for internal filters. Make sure that int_div_con is an odd number between 7(8 times division) and 15(16 times division). |

**ACDCDIG_DACSCLKRXINT_DIV**

Address: Operational Base + offset (0x0160)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:0 | RW | 0x1f | sckrxdiv<br>Integer clock divider to generate sclk_out_rx when I2S RX works in master mode. It is ignored when in slave mode.<br>Sckrxdiv=((frequency of input operation clock)/(frequency of sclk_out_rx))-1. Sckrxdiv can be any value from 0 to 255. |

**ACDCDIG_DACPWM_DIV**

Address: Operational Base + offset (0x0164)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x03 | audio_pwm_div<br>PWM mode division of Digital DAC's operation clock.<br>The operation clock frequency of DSM module is equal to the input operation clock frequency of Digital DAC's divided by audio_pwm_div+1. It's recommended that audio_pwm_div is set 8'h3. |

**ACDCDIG_DACPWM_CTRL**

Address: Operational Base + offset (0x0168)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6 | RW | 0x0 | pwm_mode_cke<br>Clock enable of 1-bit PWM modulator<br>1'b0: Disable<br>1'b1: Enable |
| 5:4 | RW | 0x0 | pwm_mode<br>Audio PWM mode selection<br>2'b01: Audio PWM mode 0. The input of 1-bit PWM modulator is from the last filter of Audio DAC.<br>2'b10: Audio PWM mode 1. The input of 1-bit PWM modulator is directly from output of I2S RX inside the ACDCDIG.<br>Others: Reserved |
| 3 | RW | 0x0 | pwm_en<br>1-bit PWM modulator enable<br>1'b0: Disable<br>1'b1: Enable |
| 2:0 | RW | 0x0 | dith_sel<br>Dith mode selection of 1-bit PWM modulator. |

**ACDCDIG_DACCFG1**

Address: Operational Base + offset (0x0184)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4:2 | RW | 0x1 | dacsrt<br>Sample rates of Digital DAC when in audio PWM mode 0. This field is ignored when in audio PWM mode 1.<br>3'b000: 12kHz/11.024kHz/8kHz<br>3'b001: 24kHz/22.05kHz/16kHz<br>3'b010: 32kHz/48kHz/44.1kHz<br>3'b011: 96kHz/88.2kHz/64kHz<br>3'b100: 192kHz/176.4kHz/128kHz<br>3'b101~3'b111: Reserved |
| 1:0 | RO | 0x0 | reserved |

**ACDCDIG_DACMUTE**

Address: Operational Base + offset (0x0188)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | dacunmt<br>1'b0: DAC normal mode<br>1'b1: DAC unmute mode. In this mode, DAC volume control block will adjust volume to match the value in DACVOLL* and DACVOLR*. |
| 0 | RW | 0x0 | dacmt<br>1'b0: DAC normal mode<br>1'b1: DAC mute mode |

**ACDCDIG_DACMUTEST**

Address: Operational Base + offset (0x018C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4 | RO | 0x0 | unmutest_l0r1<br>Unmute status for Digital DAC left channel 0 and right channel 1. When unmute is done, it indicates that internal volume is equal to the value programmed in DACVOLL* and DACVOLR*.<br>1'b0: Unmute not done<br>1'b1: Unmute done |
| 3:1 | RO | 0x0 | reserved |
| 0 | RO | 0x0 | mutest_l0r1<br>Mute status for Digital DAC left channel 0 and right channel 1.<br>1'b0: Not mute<br>1'b1: Mute |

**ACDCDIG_DACVOLL0**

Address: Operational Base + offset (0x0190)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:0 | RW | 0x00 | daclv0<br>Volume of Digital DAC left channel 0.<br>0db~-95.625db, 0.375db/step.<br>8'h0: 0db<br>8'h1: -0.375db<br>8'h2: -0.75db<br>8'h3: -1.125db<br>.....<br>8'hff: -95.625db |

**ACDCDIG_DACVOLR0**

Address: Operational Base + offset (0x01A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | dacrv0<br>Volume of Digital DAC right channel 1.<br>0db~-95.625db, 0.375db/step.<br>8'h0: 0db<br>8'h1: -0.375db<br>8'h2: -0.75db<br>8'h3: -1.125db<br>.....<br>8'hff: -95.625db |

**ACDCDIG_DACVOGP**

Address: Operational Base + offset (0x01B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | volgpr1<br>Gain polarity for the volume of Digital DAC right channel 1.<br>1'b0: Negative gain<br>1'b1: Positive gain |
| 0 | RW | 0x0 | volgpl0<br>Gain polarity for the volume of Digital DAC left channel 0.<br>1'b0: Negative gain<br>1'b1: Positive gain |

**ACDCDIG_DACRVOLL0**

Address: Operational Base + offset (0x01B4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0xff | rvoll0<br>Internal real-time volume of Digital DAC left channel 0. |

**ACDCDIG_DACRVOLR0**

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

Address: Operational Base + offset (0x01C4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0xff | rvolr0<br>Internal real-time volume of Digital DAC right channel 1. |

**ACDCDIG_DACLMT0**

Address: Operational Base + offset (0x01D4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | limen<br>LIMITER enable.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | limdct<br>Limiter detect mode.<br>1'b0: (Left channel + right channel)/2<br>1'b0: Left channel or right channel independently |

**ACDCDIG_DACLMT1**

Address: Operational Base + offset (0x01D8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:4 | RW | 0x0 | atk_rate<br>LIMITER attack rate=(power(2, atk_rate)*(8*clk)), clk is such as 4.096Mhz, 5.6448Mhz, 6.144Mhz. |
| 3:0 | RW | 0x0 | rls_rate<br>LIMITER release rate=(power(2, rls_rate)*(8*clk)), clk is such as 4.096MHz, 5.6448MHz, 6.144MHz. |

**ACDCDIG_DACLMT2**

Address: Operational Base + offset (0x01DC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6:4 | RW | 0x0 | max_lilmt<br>The highest threshold of LIMITER.<br>3'b000~3'b100: 0db~-12db, 3db/step<br>3'b101~3'b111: -18db~-30db, 6db/step |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x0 | min_lilmt<br>The lowest threshold of LIMITER.<br>3'b000~3'b100: 0db~-12db, 3db/step<br>3'b101~3'b111: -18db~-30db, 6db/step |

**ACDCDIG_DACMIXCTRLL**

Address: Operational Base + offset (0x01E0)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1:0 | RW | 0x0 | mixmode_l0<br>Digital DAC left channel 0 mixing mode.<br>2'b00: Left channel<br>2'b01: Right channel<br>2'b10~2'b11: (Left channel + right channel)/2 |

**ACDCDIG_DACMIXCTRLR**

Address: Operational Base + offset (0x01E4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1:0 | RW | 0x0 | mixmode_r0<br>Digital DAC right channel 1 mixing mode.<br>2'b00: Left channel<br>2'b01: Right channel<br>2'b10~2'b11: (Left channel + right channel)/2 |

**ACDCDIG_DACHPF**

Address: Operational Base + offset (0x01E8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5:4 | RW | 0x0 | hpfcf<br>High-pass filter control.<br>2'b00: 80Hz<br>2'b01: 100Hz<br>2'b10: 120Hz<br>2'b11: 140Hz |
| 3:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | hpfen_l0r1<br>High-pass filter enable for left channel 0 and right channel 1.<br>1'b0: High-pass filter is disabled.<br>1'b1: High-pass filter is enabled. |

**ACDCDIG_I2S_RXCR0**

Address: Operational Base + offset (0x030C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:6 | RW | 0x0 | pbm<br>PCM bus mode<br>2'b00: PCM no delay mode<br>2'b01: PCM delay 1 mode<br>2'b10: PCM delay 2 mode<br>2'b11: PCM delay 3 mode |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | tfs<br>Transfer format select<br>1'b0: I2S format<br>1'b1: PCM format |
| 4:0 | RW | 0x0f | vdw<br>Valid data width<br>5'b00000~5'b01110: Reserved<br>5'b01111: 16bit<br>5'b10000: 17bit<br>5'b10001: 18bit<br>5'b10010: 19bit<br>.....<br>5'b11100: 29bit<br>5'b11101: 30bit<br>5'b11110: 31bit<br>5'b11111: 32bit |

**ACDCDIG_I2S_RXCR1**

Address: Operational Base + offset (0x0310)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:6 | RW | 0x0 | rcsr<br>Channel select<br>2'b00: Two channel<br>Others: Reserved |
| 5 | RO | 0x0 | reserved |
| 4 | RW | 0x0 | cex<br>Exchange left channel and right channel in the every receive line.<br>1'b0: Not exchange<br>1'b1: Exchange |
| 3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | fbm<br>First bit mode<br>1'b0: MSB<br>1'b1: LSB |
| 1:0 | RW | 0x0 | ibm<br>I2S bus mode<br>2'b00: I2S normal<br>2'b01: I2S Left justified<br>2'b10: I2S Right justified<br>2'b11: Reserved |

**ACDCDIG_I2S_CKR0**

Address: Operational Base + offset (0x0314)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3:2 | RW | 0x0 | rsd<br>I2S rx sclk divider for rx_lrck generator.<br>2'b00: 64<br>2'b01: 128<br>2'b10~2'b11: 256 |
| 1:0 | RO | 0x0 | reserved |

**ACDCDIG_I2S_CKR1**

Address: Operational Base + offset (0x0318)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3 | RW | 0x0 | mss<br>Master/slave mode select<br>1'b0: Master mode(sclk output)<br>1'b1: Slave mode(sclk input) |
| 2 | RW | 0x0 | ckp<br>Sclk polarity<br>1'b0: Sample data at posedge sclk and drive data at negedge sclk.<br>1'b1: Sample data at negedge sclk and drive data at posedge sclk. |
| 1 | RW | 0x0 | rlp<br>1'b0: Normal polarity<br>(I2S normal: low for left channel, high for right channel<br>I2S left/right just: high for left channel, low for right channel<br>PCM start signal: high valid)<br>1'b1: Opposite polarity<br>(I2S normal: high for left channel, low for right channel<br>I2S left/right just: low for left channel, high for right channel<br>PCM start signal: low valid) |
| 0 | RO | 0x0 | reserved |

**ACDCDIG_I2S_XFER**

Address: Operational Base + offset (0x031C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | rxs<br>1'b0: Stop RX transfer<br>1'b1: Start RX transfer |
| 0 | RO | 0x0 | reserved |

**ACDCDIG_I2S_CLR**

Address: Operational Base + offset (0x0320)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | rxc<br>This is a self-cleared bit. Write 1'b1 to clear all receive logic.<br>This bit can be set only when rxs is 1'b0. After writing rxc to 1'b1, wait until rxc become 1'b0 by polling rxc. |
| 0 | RO | 0x0 | reserved |

**ACDCDIG_VERSION**

Address: Operational Base + offset (0x0380)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x02 | ver<br>Version of ACDCDIG. |

## 27.5 Interface Description

The I2S RX interface of Digital Audio Codec is connected to the TX interface of I2S3 when SYS_GRF_SOC_CON6[11] is set to 1'b1.
When operating in audio PWM mode 0 or 1, Digital Audio Codec outputs two pairs of differential signals encoded in PWM format. The following table shows the Digital Audio Codec interface description for audio PWM mode.

Table 27-1 Digital Audio Codec Interface Description

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| AUDIO_PWM_L_P | O | GMAC1_RXD2/SDIO_D2_M1/I2S3_LRCK/AUDDSM_LP/FSPI_D2_M2/UART8_TX_M1/SPI4_CLK_M1/GPIO3_A2_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[11:8]=4'h4 |
| AUDIO_PWM_L_N | O | GMAC1_TXD3/SDIO_D1_M1/I2S3_SCLK/AUDDSM_LN/FSPI_D1_M2/I2C6_SCL_M4/PWM11_IR_M0/SPI4_MOSI_M1/GPIO3_A1_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[7:4]=4'h4 |
| AUDIO_PWM_R_P | O | GMAC1_TXCLK/SDIO_CMD_M1/I2S3_SDI/AUDDSM_RP/UART8_RTSN_M1/SPI4_CS1_M1/GPIO3_A4_d | BUS_IOC_GPIO3A_IOMUX_SEL_H[3:0]=4'h4 |
| AUDIO_PWM_R_N | O | GMAC1_RXD3/SDIO_D3_M1/I2S3_SDO/AUDDSM_RN/FSPI_D3_M2/UART8_RX_M1/SPI4_CS0_M1/GPIO3_A3_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[15:12]=4'h4 |

## 27.6 Application Notes

### 27.6.1 Software Application Notes

Steps to configure Digital DAC to work in audio PWM mode 0 are as follows.
1. Program CRU in the SOC system to achieve the operation frequency of Digital DAC.
2. Program ACDCDIG_DACINT_DIV to 0x07.
3. Program ACDCDIG_DACCLKCTRL to 0x3d.
4. Program ACDCDIG_DACSCLKRXINT_DIV if Digital DAC I2S RX acts as master.
5. Program ACDCDIG_DACPWM_CTRL to 0x58.
6. Program ACDCDIG_I2S_CKR0 and ACDCDIG_I2S_CKR1 to set I2S RX related registers.
7. Program ACDCDIG_I2S_CLR to clear RX logic.

Copyright 2022 © Rockchip Electronics Co., Ltd.

8. Program ACDCDIG_I2S_RXCR0 and ACDCDIG_I2S_RXCR1.
9. Program SYS_GRF_SOC_CON6[11] to 1'b1 and program registers of I2S3 that is connected to Digital Audio Codec. Don't start transfer at this time.
10. Program DAC related registers such as ACDCDIG_DACHPF, ACDCDIG_DACVUCTL and ACDCDIG_DACCFG1 to achieve basic configuration.
11. Program ACDCDIG_I2S_XFER to start I2S RX.
12. Program registers of I2S3 outside Digital Audio Codec to start TX.
13. Program ACDCDIG_DACDIGEN to enable digital DAC channels. From now on, the Digital Audio Codec begins to work.

Steps to configure Digital Audio Codec to end audio PWM mode 0 transfer are as follows.
1. Program registers of I2S3 to stop TX and ACDCDIG_I2S_XFER to stop RX.
2. Program ACDCDIG_DACPWM_CTRL to 0x0.
3. Program ACDCDIG_DACDIGEN to disable digital DAC channels.
4. Program ACDCDIG_DACCLKCTRL to 0x0. Wait ACDCDIG_DACCLKCTRL.dac_sync_status until read back to be 1'b0.

Steps to configure Digital DAC to work in audio PWM mode 1 are as follows.
1. Program CRU in the SOC system to achieve the operation frequency of Digital DAC.
2. Program ACDCDIG_DACCLKCTRL to 0x3d.
3. Program ACDCDIG_DACSCLKRXINT_DIV if Digital DAC I2S RX acts as master.
4. Program ACDCDIG_DACPWM_CTRL to 0x68.
5. Program ACDCDIG_I2S_CKR0 and ACDCDIG_I2S_CKR1 to set I2S RX related registers.
6. Program ACDCDIG_I2S_CLR to clear RX logic.
7. Program ACDCDIG_I2S_RXCR0 and ACDCDIG_I2S_RXCR1.
8. Program SYS_GRF_SOC_CON6[11] to 1'b1 and program registers of I2S3 to start TX.
9. Program ACDCDIG_I2S_XFER to start I2S RX. From now on, the Digital Audio Codec begins to work.

Steps to configure Digital Audio Codec to end audio PWM mode 1 transfer are as follows.
1. Program registers of I2S3 to stop TX and ACDCDIG_I2S_XFER to stop RX.
2. Program ACDCDIG_DACPWM_CTRL to 0x0.
3. Program ACDCDIG_DACCLKCTRL to 0x0. Wait ACDCDIG_DACCLKCTRL.dac_sync_status until read back to be 1'b0.

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

# Chapter 28 Voice Activity Detect (VAD)

## 28.1 Overview

Voice Activity Detect (VAD) is used to detect the amplitude of voice which is received by Analog Mic, I2S Digital Mic or PDM digital Mic when SoC is in low power mode. If the amplitude of voice is over threshold, the VAD will assert interrupt to wake up SoC, then SoC will exit low power mode.

VAD supports the following features:

- Support AHB bus interface
- Support read voice data from I2S1, PDM0
  - Support to configure the voice source address
  - Support to configure increment or fixed for the direction of voice data address
  - Support DMA request and acknowledge
  - Support transfer 1~8 burst per DMA request
  - Support read 1~8 Mic voice data, and only support single Mic voice detection, user can select any Mic voice data to detect the amplitude of voice
  - Support 16/24 bits voice data
- Support voice amplitude detection
  - Support an Amplifier for the voice data
  - Support a IIR high pass filter for the voice frequency band, and the filter coefficient can be configured
  - Support a voice detect threshold that take the ambient noise to account
- Support Multi-Mic array data storing
  - Buffer memory is shared with Internal SRAM
  - The start and end address of storing can be configured
  - When current storing address is up to end address, it will loop to start address and overlap previous data, it will also assert a flag
  - Support 3 data storing mode: mode 0 start storing data after the voice detect event, mode 1 start storing after VAD is enabled and mode 2 do not storing data
  - Support storing data through bus or ram write interface
- Support a level combined interrupt
  - Support voice detect interrupt
  - Support time out interrupt
  - Support transfer error interrupt
  - Support data transfer interrupt

## 28.2 Block Diagram

VAD comprises with:

- AHB_MASTER: AHB Master Interface
- AHB_SRAM_IF: AHB Slave Interface
- VAD_REG_BANK: Register bank
- DMAC_ENGINE: DMA control engine
- VAD_DET: Voice detection

Copyright 2022 © Rockchip Electronics Co., Ltd.

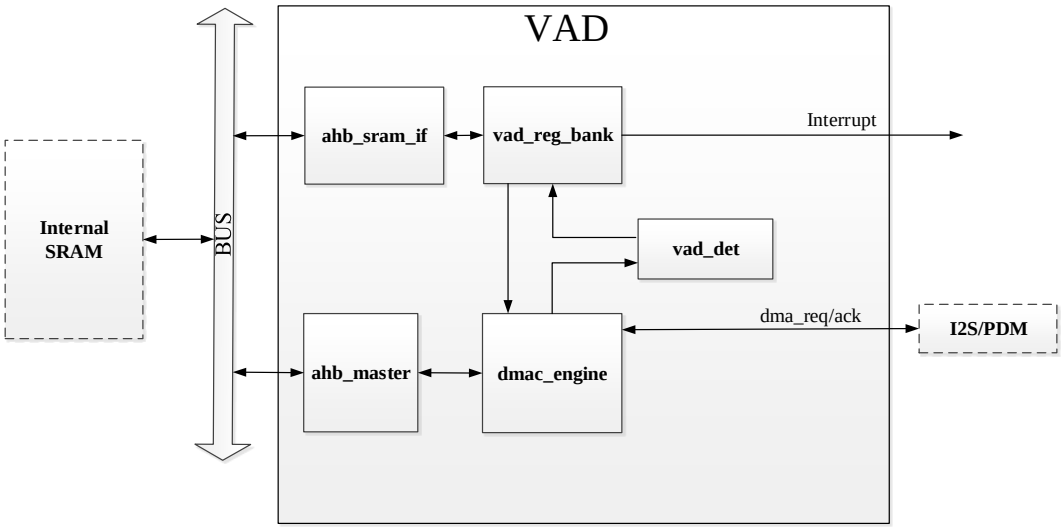



Fig. 28-1 VAD Block Diagram

# 28.3 Function Description

## 28.3.1 DMAC_ENGINE

DMAC_ENGING is used to read voice data from one of I2S_8CH_0 or PDM, and it can store all channels data to Internal SRAM. If the bus can be access, user can configure to store through bus. Otherwise user should configure to store through ram write interface. When VAD is working, user can change the data storing mode dynamically. The storing address can be continuous transition or be spitted.

The voice data can be 16 or 24 bits:

- When it's 16 bits, it must be half word transfer mode that low 16 bits in a word for left channel and high 16 bits in a word for right channel.
- When it's 24bits, it must be word transfer mode that only 24 bits data is valid in a word, and it support left or right justified.

DMAC_ENGING also select and send one channel data to vad_det for voice detection. vad_det only support 16 bits data to detect the amplitude of voice, so when the voice data is 24 bits, user can use the high or low 16 bits in 24 bits.

- When use high bits, the data value will be divided by 256.
- When use low bits, the data value will be saturation to 16 bits.

## 28.3.2 VAD_DET

VAD_DET is used to detect the amplitude of voice.

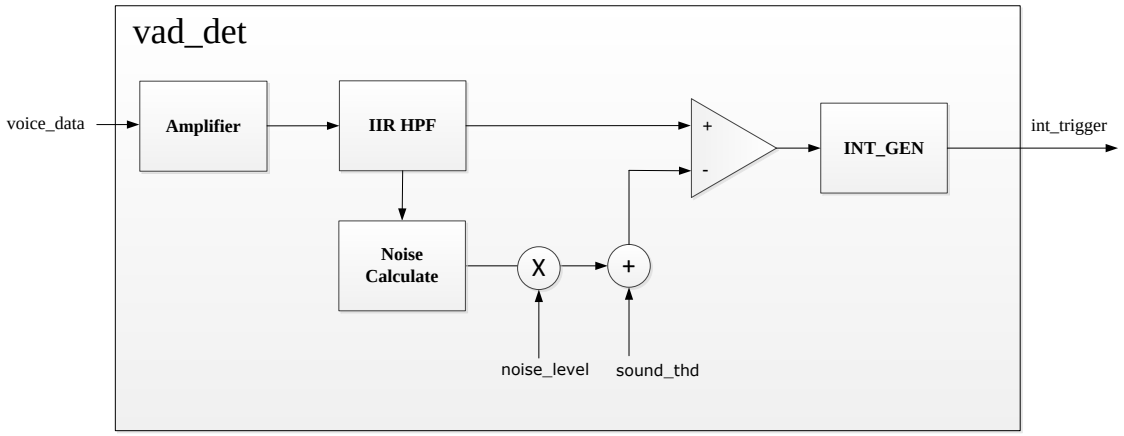


Fig. 28-2 VAD_DET Block Diagram

**Amplifier**

voice_amplitude_amplified=gain*voice_amplitude_original/8.

**IIR HPF**

There is a high pass filter for the human voice frequency band, the filter is a two order direct I type IIR. The following formula describes:

y(n)=-a1*y(n-1)-a2*y(n-2)+b0*x(n)+b1*x(n-1)+b2*x(n-2)

The coefficient a1, a2, b0, b1 and b2 are all quantified by multiplying 16384 and represented as 16 bits, the result in follow registers that can be configured: iir_anum_0, iir_anum_1, iir_anum_2, iir_aden_1 and iir_aden_2.

The output of HPF need some time to achieve convergence after VAD is enabled.

**Noise Calculate**

VAD support a voice detection threshold that take the ambient noise to account:

- VAD calculate the average amplitude of voice data within noise_sample_num samples, the result is regard as the noise value of one frame. The noise value of last 128 frames also can be configured directly.
- VAD find the minimum noise value within noise_frm_num frames, the result is regard as the noise_min(minimum noise value).User can configure min_noise_find_mode to change the mode to find the minimum noise.
- The noise_min will be smooth updated to noise_abs(current noise value), the formula is as follow: noise_abs= (noise_abs * noise_alpha + noise_min * (256-noise_alpha)/256. noise_abs will be updated once every frame. noise_abs also can be configured directly, and it is not clear until VAD is reset.

**Voice Detect Threshold**

The final threshold is sound_thd + noise_abs * noise_level.

**INT_GEN**

VAD support 3 modes to assert the voice detection interrupt.

- Normal mode: When equal or more than a number (vad_con_thd) of continuous samples over the threshold, the voice detection interrupt will be asserted. The vad_con_thd can be configured by register.
- Allow an exception mode: base on normal mode, it can be configured to allow exceptions during continuous sample judgment. The exception number can be configured by register. When the exceptions is more, the voice detect condition is less strict.
- Accumulating mode: A counter is used for accumulating, the counter will plus 1 when current sample is over threshold (it will not plus when it reach maximum value 256), the counter will minus 1 when current sample is not over threshold (it will not minus when it reach 0); When the counter is equal or more than a number (vad_con_thd), the voice detection interrupt will be asserted. Compare with normal mode, the voice detect condition is less strict when use the same value of vad_con_thd.

Copyright 2022 © Rockchip Electronics Co., Ltd.

# 28.4 Register Description

## 28.4.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VAD_CONTROL | 0x0000 | W | 0x03000000 | Control register |
| VAD_VS_ADDR | 0x0004 | W | 0x00000000 | Voice source address register |
| VAD_TIMEOUT | 0x004c | W | 0x00000000 | Timeout register |
| VAD_RAM_START_ADDR | 0x0050 | W | 0xfff88000 | RAM start address register |
| VAD_RAM_END_ADDR | 0x0054 | W | 0xfffbfff8 | RAM end address register |
| VAD_RAM_CUR_ADDR | 0x0058 | W | 0x00000000 | RAM current address register |
| VAD_DET_CON0 | 0x005c | W | 0x01024008 | Detect control register0 |
| VAD_DET_CON1 | 0x0060 | W | 0x04ff0064 | Detect control register1 |
| VAD_DET_CON2 | 0x0064 | W | 0x3bf5e663 | Detect control register2 |
| VAD_DET_CON3 | 0x0068 | W | 0x3bf58817 | Detect control register3 |
| VAD_DET_CON4 | 0x006c | W | 0x382b8858 | Detect control register4 |
| VAD_DET_CON5 | 0x0070 | W | 0x00000000 | Detect control register5 |
| VAD_INT | 0x0074 | W | 0x00000200 | VAD Interrupt register |
| VAD_AUX_CON0 | 0x0078 | W | 0x00000000 | Auxiliary control register0 |
| VAD_SAMPLE_CNT | 0x007c | W | 0x00000000 | Sample counter register |
| VAD_RAM_START_ADDR_BUS | 0x0080 | W | 0xfff88000 | RAM start address register for bus write mode |
| VAD_RAM_END_ADDR_BUS | 0x0084 | W | 0xfffbfff8 | RAM end address register for bus write mode |
| VAD_RAM_CUR_ADDR_BUS | 0x0088 | W | 0x00000000 | RAM current address register for bus write mode |
| VAD_AUX_CON1 | 0x008c | W | 0x00000000 | Auxiliary control register1 |
| VAD_NOISE_FIRST_DATA | 0x0100 | W | 0x00000000 | Noise first data register |
| VAD_NOISE_LAST_DATA | 0x02fc | W | 0x00000000 | Noise last data register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

## 28.4.2 Detail Register Description

**VAD_CONTROL**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RW | 0x0 | vad_det_channel<br>Index of the channal for voice detect, from channel 0 to channel 7 |
| 28 | RW | 0x0 | voice_24bit_sat<br>The mode of voice 24bit data change to 16bit<br>1'b0: Get the high 16bit data(divided by 256)<br>1'b1: Saturation from 24bit to 16bit |
| 27 | RW | 0x0 | voice_24bit_align_mode<br>Align mode of channel 24bit width<br>1'b0: 8~31bits is valid<br>1'b1: 0~23bits is valid |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 26 | RW | 0x0 | voice_channel_bitwidth<br>1'b0: 16bits<br>1'b1: 24bits |
| 25:23 | RW | 0x6 | voice_channel_num<br>Voice channel number, the value N means N+1 channel |
| 22 | RO | 0x0 | reserved |
| 21:20 | RW | 0x0 | vad_mode<br>2'h0: Begin to store the data after voice detect<br>2'h1: Begin to store the data after VAD is enable<br>2'h2: Don't store the data<br>2'h3: Reserved |
| 19:15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | source_fixaddr_en<br>Direction of source address<br>1'b0: Increment<br>1'b1: Fixed |
| 13:10 | RW | 0x0 | incr_length<br>INCR burst length, 0~15 is valid.<br>It is valid when source_burst is set to 3'h1. |
| 9:7 | RW | 0x0 | source_burst_num<br>Source burst number per dma_req, the value N means N+1 burst |
| 6:4 | RW | 0x0 | source_burst<br>3'h0: SINGLE<br>3'h1: INCR<br>3'h3: INCR4<br>3'h5: INCR8<br>3'h7: INCR16<br>Others: Reserved |
| 3:1 | RW | 0x0 | source_select<br>Voice source select<br>3'h0: I2S0<br>3'h1: I2S1<br>3'h2: PDM<br>Others: Reserved |
| 0 | RW | 0x0 | vad_en<br>VAD enable<br>1'b0: Disable<br>1'b1: Enable |

**VAD_VS_ADDR**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | vs_addr<br>Voice source address |

**VAD_TIMEOUT**

Address: Operational Base + offset (0x004c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | work_timeout_en<br>Work timeout enable<br>1'b0: Disable<br>1'b1: Enable |
| 30 | RW | 0x0 | idle_timeout_en<br>Idle timeout enable<br>1'b0: Disable<br>1'b1: Enable |
| 29:20 | RW | 0x000 | work_timeout_thd<br>work timeout threshold, the unit is one cycle of hclk |
| 19:0 | RW | 0x00000 | idle_timeout_thd<br>Idle timeout threshold, the unit is one cycle of hclk |

**VAD_RAM_START_ADDR**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ram_start_addr<br>RAM start address to store voice data, the address must be double word alignment |

**VAD_RAM_END_ADDR**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ram_end_addr<br>RAM end address to store voice data, the address must be double word alignment |

**VAD_RAM_CUR_ADDR**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ram_cur_addr<br>RAM current address to store voice data, The last valid double word data is at address ram_cur_addr-0x8.<br>When the ram_loop_flag is valid, the valid voice data will be ram_cur_addr ~ ram_end_addr ~ loop to ram_begin_addr ~ ram_cur_addr-0x8.<br>When the ramp_loop_flag is not valid, the valid voice data will be ram_begin_addr ~ ram_cur_addr-0x8 |

**VAD_DET_CON0**

Address: Operational Base + offset (0x005c)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:28 | RW | 0x0 | vad_thd_mode<br>Threshold mode for vad_con_thd<br>2'b00: Normal mode<br>2'b01: Allow an exception mode<br>2'b10: Accumulating mode<br>2'b11: Reserved |
| 27:24 | RW | 0x1 | dis_vad_con_thd<br>In the determining of continuous sample number exceed threshold, allow some number of sample as an exception. It's valid only when vad_thd_mode=1.<br>When this value is lower, the voice detect condition is more strict |
| 23:16 | RW | 0x02 | vad_con_thd<br>When continuous sample number(>=vad_con_thd) exceed threshold, then assert the vad_det interrupt, the value N means N+1.<br>When this value is higher, the voice detect condition is more strict |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x4 | noise_level<br>Noise level, valid value is 0x1~0x6<br>when this value is higher, the voice detect condition is more strict |
| 11:0 | RW | 0x008 | gain<br>The gain control of voice data amplifier, the value of gain is unsigned and is valid from 0 to 4095.<br>voice_amplitude_amplified=gain*voice_amplitude_original/8. |

**VAD_DET_CON1**

Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |
| 30 | RW | 0x0 | min_noise_find_mode<br>Minimal noise value find mode<br>1'b0: Always find the value at the range of noise_frm_num<br>1'b1: When receive N frame: if N is less than noise_frm_num, find the value at the range of N; if N is more than noise_frm_num, find the value at the range of noise_frm_num |
| 29 | RW | 0x0 | clean_noise_at_begin<br>1'b0: The noise will be clean only at the begin of the first time VAD is enable after reset<br>1'b1: The noise will be clean every time at the begin of VAD is enable |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 28 | RW | 0x0 | force_noise_clk_en<br>Force noise calculate clk enable<br>1'b0: The clock will be auto gating for low power<br>1'b1: The clock will be always enable |
| 27 | RO | 0x0 | reserved |
| 26 | RW | 0x1 | clean_iir_en<br>Clean IIR filter when VAD is disable<br>1'b0: Not clean<br>1'b1: Clean |
| 25:16 | RW | 0x0ff | noise_sample_num<br>The number of sample in one frame to calculate the noise, the value N means N+1 sample.<br>When this value is higher, the voice detect condition is more strict |
| 15:0 | RW | 0x0064 | sound_thd<br>Initial sound threshold<br>when this value is higher, the voice detect condition is more strict |

**VAD_DET_CON2**

Address: Operational Base + offset (0x0064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x3bf5 | iir_anum_0<br>IIR numerator coefficient b0 |
| 15:8 | RW | 0xe6 | noise_alpha<br>The update smooth speed of noise<br>When this value is lower, the voice detect condition is more strict |
| 7 | RO | 0x0 | reserved |
| 6:0 | RW | 0x63 | noise_frm_num<br>The number of frame to calculate the noise, the value N means N+1 frame.<br>When this value is lower, the voice detect condition is more strict |

**VAD_DET_CON3**

Address: Operational Base + offset (0x0068)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x3bf5 | iir_anum_2<br>IIR numerator coefficient b2 |
| 15:0 | RW | 0x8817 | iir_anum_1<br>IIR numerator coefficient b1 |

**VAD_DET_CON4**

Address: Operational Base + offset (0x006c)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x382b | iir_aden_2<br>IIR demoninator coefficient a2 |
| 15:0 | RW | 0x8858 | iir_aden_1<br>IIR demoninator coefficient a1 |

**VAD_DET_CON5**

Address: Operational Base + offset (0x0070)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | iir_result<br>Voice real time data after IIR filter |
| 15:0 | RW | 0x0000 | noise_abs<br>Noise abs value |

**VAD_INT**

Address: Operational Base + offset (0x0074)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x0 | reserved |
| 12 | RO | 0x0 | ramp_loop_flag_bus<br>RAM adress loop flag for AHB bus interface write mode. Only valid when bus_write_addr_mode=1'b1.<br>1'b0: Not loop<br>1'b1: Loop |
| 11 | W1C | 0x0 | vad_data_trans_int<br>VAD data transfer interrupt<br>1'b0: Interrupt not generated<br>1'b1: Interrupt generated |
| 10 | RW | 0x0 | vad_data_trans_int_en<br>VAD data transfer interrupt enable<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | vad_idle<br>VAD idle flag<br>1'b0: Not idle<br>1'b1: Idle |
| 8 | RO | 0x0 | ramp_loop_flag<br>RAM address loop flag<br>1'b0: Not loop<br>1'b1: Loop |
| 7 | W1C | 0x0 | work_timeout_int<br>Work timeout interrupt<br>1'b0: Interrupt not generated<br>1'b1: Interrupt generated |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | W1C | 0x0 | idle_timeout_int<br>Idle timeout interrupt<br>1'b0: Interrupt not generated<br>1'b1: Interrupt generated |
| 5 | RW | 0x0 | error_int<br>Error interrupt<br>1'b0: Interrupt not generated<br>1'b1: Interrupt generated |
| 4 | W1C | 0x0 | vad_det_int<br>VAD detect interrupt<br>1'b0: Interrupt not generated<br>1'b1: Interrupt generated |
| 3 | RW | 0x0 | work_timeout_int_en<br>Wrok timeout interrupt enable<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | idle_timeout_int_en<br>Idle timeout interrupt enable<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | error_int_en<br>Error interrupt enable<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | vad_det_int_en<br>VAD detect interrupt enable<br>1'b0: Disable<br>1'b1: Enable |

**VAD_AUX_CON0**

Address: Operational Base + offset (0x0078)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29 | RW | 0x0 | sample_cnt_en<br>Sample counter enable<br>1'b0: Disable<br>1'b1: Enable |
| 28 | RW | 0x0 | int_trig_ctrl_en<br>The VAD detection interrupt trigger control enable.<br>1'b0: Disable, the VAD detection interrupt is always trigger<br>1'b1: Enable, the VAD detection interrupt trigger is controlled by int_trig_valid_thd |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 27:16 | RW | 0x000 | int_trig_valid_thd<br>VAD detection interrupt trigger valid threshold. The VAD detection interrupt will be triggered valid after sample_cnt exceed int_trig_valid_thd.<br>The value N means N+1,The unit is one voice sample point. |
| 15 | RO | 0x0 | reserved |
| 14 | RW | 0x0 | ram_write_rework_addr_mode<br>The rework address for RAM interface write mode.<br>1'b0: Store the data from the current address<br>1'b1: Store the data from the start address |
| 13 | RW | 0x0 | bus_write_rework_addr_mode<br>The rework address for bus write mode.<br>1'b0: Store the data from the current address<br>1'b1: Store the data from the start address |
| 12 | RW | 0x0 | bus_write_addr_mode<br>The address selection when use AHB bus interface write mode.<br>1'b0: Use RAM_START_ADDR, RAM_END_ADDR, RAM_CUR_ADDR(same with RAM interface write mode). The internal address will continuous when dynamic change between bus write mode and RAM interface write mode.<br>1'b1: Use RAM_START_ADDR_BUS, RAM_END_ADDR_BUS and RAM_CUR_ADDR_BUS. |
| 11:4 | RW | 0x00 | data_trans_kbyte_thd<br>Data transfer number threshold, the unit is KByte. The value N means N+1 KByte. The interrupt is generated per data_trans_kbyte_thd+1 KBytes. |
| 3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | data_trans_trig_int_en<br>Trigger an interrupt for data transfer, It's valid only when bus_write_en=1'b1.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | dis_ram_itf<br>Disable write voice data to Internal SRAM through RAM interface<br>1'b0: Enable ram interface<br>1'b1: Disable ram interface |
| 0 | RW | 0x0 | bus_write_en<br>Enable write voice data to Internal SRAM through AHB bus interface<br>1'b0: Disable<br>1'b1: Enable |

**VAD_SAMPLE_CNT**

Address: Operational Base + offset (0x007c)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | sample_cnt<br>Sample counter |

**VAD_RAM_START_ADDR_BUS**

Address: Operational Base + offset (0x0080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ram_start_addr_bus<br>RAM start address to store voice data, the address must be double word alignment. Only used for bus write mode and when bus_write_addr_mode=1'b1. |

**VAD_RAM_END_ADDR_BUS**

Address: Operational Base + offset (0x0084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ram_begin_addr_bus<br>RAM start address to store voice data, the address must be double word alignment. Only used for bus write mode and when bus_write_addr_mode=1'b1. |

**VAD_RAM_CUR_ADDR_BUS**

Address: Operational Base + offset (0x0088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ram_cur_addr_bus<br>RAM current address to store voice data. Only used for bus write mode and when bus_write_addr_mode=1'b1. The last valid double word data is at address ram_cur_addr_bus-0x8.<br>When the ram_loop_flag_bus is valid, the valid voice data will be ram_cur_addr_bus ~ ram_end_addr_bus ~ loop to ram_begin_addr_bus ~ ram_cur_addr_bus-0x8.<br>When the ramp_loop_flag is not valid, the valid voice data will be ram_begin_addr_bus ~ ram_cur_addr_bus-0x8 |

**VAD_AUX_CON1**

Address: Operational Base + offset (0x008c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0 | reserved |
| 16 | RW | 0x0 | data_trans_int_mode_sel<br>Data transfer number threshold selection for interrupt trigger<br>1'b0: Data_trans_kbyte_thd<br>1'b1: Data_trans_word_thd |
| 15:0 | RW | 0x0000 | data_trans_word_thd<br>Data transfer number threshold, the unit is word. The value N means N+1 words. The interrupt is generated per trans_word_thd+1 words. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**VAD_NOISE_FIRST_DATA**

Address: Operational Base + offset (0x0100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | reserved |
| 15:0 | RW | 0x0000 | noise_first_data<br>Noise first data |

**VAD_NOISE_LAST_DATA**

Address: Operational Base + offset (0x02fc)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0 | reserved |
| 15:0 | RW | 0x0000 | noise_last_data<br>Noise last data |

# 28.5 Application Notes

## 28.5.1 VAD usage flow

VAD usage flow is shown as following figures.

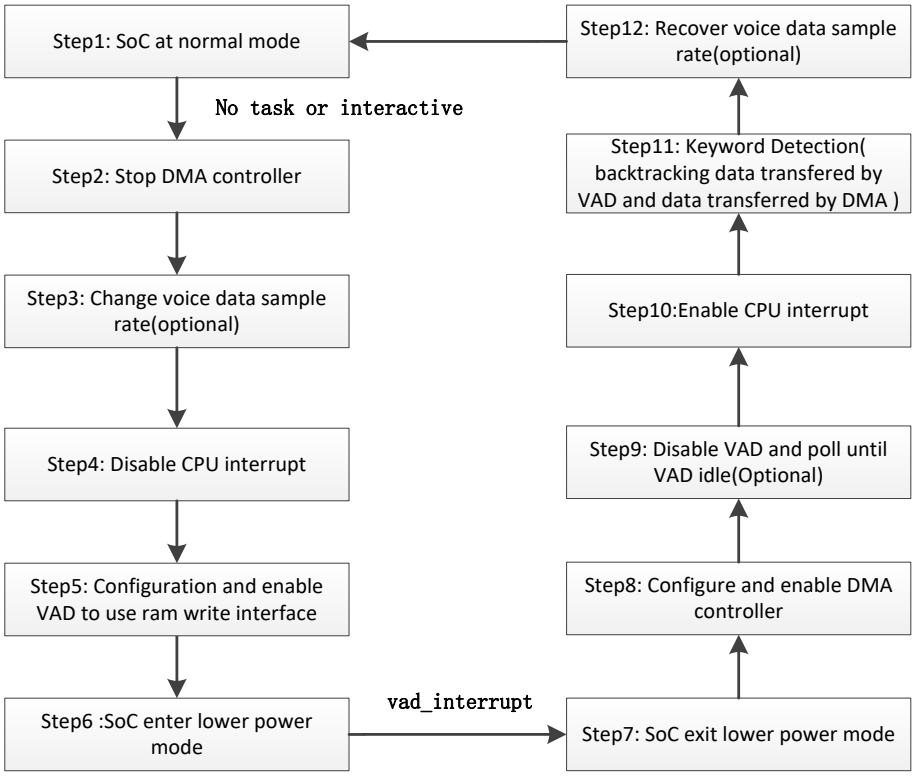



Fig. 28-3 VAD usage flow (only used ram write interface mode)

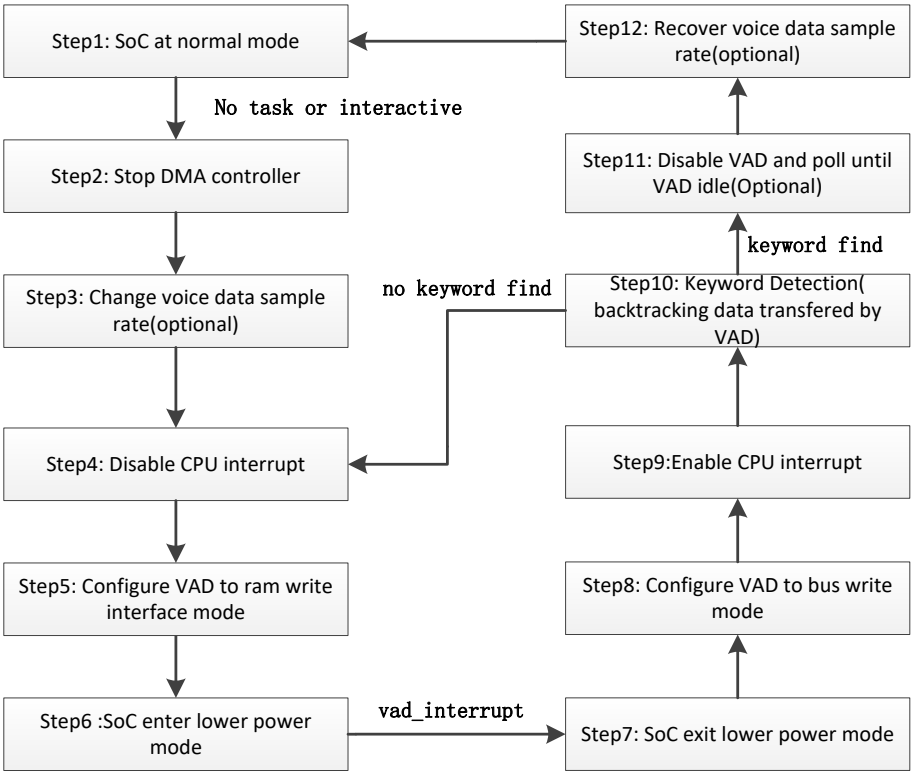



Fig. 28-4 VAD usage flow (use bus mode and ram write interface mode)

- Step3, step12 are optional, user should consider the power consumption and keyword detection accuracy for these steps.
- Disable VAD step is optional, user can keep VAD working, and use it as a DMA Controller.

## 28.5.2 VAD configuration usage flow

- Set VAD_VS_ADDR.vs_addr=I2S_8CH_0 base address + I2S_8CH_INCR_RXDR.
- Set VAD_RAM_BEGIN_ADDR.ram_begin_addr and VAD_RAM_END_ADDR.ram_end_addr, the address should match with the Internal SRAM sharing scheme.
- Set to bus write mode or ram interface mode when enable VAD
  Set VAD_AUX_CON0.bus_write_en=0, and VAD_AUX_CON0.dis_ram_itf =0 toenable VAD as ram interface write mode.
  Set VAD_AUX_CON0.bus_write_en=1, and VAD_AUX_CON0.dis_ram_itf =1 to enable VAD as bus write mode.
- Adjust the sensitivity of voice activity detect by setting follow registers:
  VAD_DET_CON0.noise_level
  VAD_DET_CON0.vad_con_thd
  VAD_DET_CON0.dis_vad_con_thd
  VAD_DET_CON0.vad_thd_mode
  VAD_DET_CON1.noise_sample_num
  VAD_DET_CON1.sound_thd
  VAD_DET_CON2.noise_frm_num
  VAD_DET_CON2.noise_alpha
- Set the iir_anum_0~3 and iir_aden_1~2 to adjust the IIR HPF coefficient.
  For 48Khz sample rate:
  iir_anum_0: 0x382d
  iir_anum_1: 0x8fa5
  iir_anum_2: 0x382d
  iir_aden_1: 0x909b
  iir_aden_2: 0x3150
  For 16Khz sample rate (default):
  iir_anum_0: 0x3bf5
  iir_anum_1: 0x8817
  iir_anum_2: 0x3bf5

Copyright 2022 © Rockchip Electronics Co., Ltd. 

iir_aden_1: 0x8858
iir_aden_2: 0x382b
For 8Khz sample rate:
iir_anum_0: 0x3e9f
iir_anum_1: 0x82c2
iir_anum_2:0x3e9f
iir_aden_1: 0x82c9
iir_aden_2: 0x3d46

- Set DET_CON5.noise_abs to ambient noise which is calculated by software.
  Set VAD_NOISE_DATA+offset to initial the noise data of all frames. The frame number is VAD_DET_CON2.noise_frm_num.
  The first frame noise data address is VAD_NOISE_DATA, the second frame noise data address is VAD_NOISE_DATA+0x4, and so on.
- Set VAD_INT.vad_det_int_en=0x1 to enable the interrupt.
- Set VAD_AUX_CONTROL to disable detection at the beginning after VAD is enabled.
  Set sample_cnt_en=0x1
  Set int_trig_ctrl_en=0x1
  Set int_trig_valid_thd to appropriate value, it recommended configuration to 4ms.
  For 48Khz sample rate: int_trig_valid_thd= 0xc0
  For 16Khz sample rate: int_trig_valid_thd= 0x40
  For 8Khz sample rate: int_trig_valid_thd= 0x20
- Set VAD_CONTROL register:
  Set source_select=0x1, select I2S_8CH_0
  Set source_burst=0x3, select INCR4 burst type
  Set source_burst_num=0x0, select 1 burst transfer per DMA request
  Set vad_mode=0x0, select Mode 0
  Set voice_channel_num=0x7, all voice channel number is 8
  Set voice_channel_bitwidth=0x0, voice data width is 16 bits
  Set vad_det_channel=0x0, use channel 0 to voice activity detect
  Set vad_en=0x1, enable VAD
- After above setting, VAD will start to work and system can enter low power mode.
  When VAD is working, user can configure the VAD_AUX_CON0.bus_write_en and VAD_AUX_CON0.ram_itf_dis to change the data storing mode dynamically. The storing address can be continuous transition or be spitted. It's controlled by following bits:
  VAD_AUX_CON0.bus_write_addr_mode
  VAD_AUX_CON0. bus_write_rework_addr_mode
  VAD_AUX_CON0. ram_write_rework_addr_mode

### 28.5.3 Data Transfer Interrupt usage flow

When VAD is working at bus write mode. User can get data transfer interrupt by following additional configuration.

- Set VAD_AUX_CONTROL.data_trans_trig_int_en=0x1
- Set VAD_AUX_CONTROL.data_trans_kbyte_thd at appropriate value
- Set VAD_INT.vad_data_trans_int_en=0x1

### 28.5.4 Timeout configuration usage flow

- Set VAD_TIMEOUT.idle_timeout_thd=0xfffff, set VAD_TIMEOUT.idle_timeout_en=0x1, set VAD_INT.idle_timeout_int=0x1. After above setting, a counter is increase at AHB clock when dmac_engine is idle, the counter will be clear to 0 once dmac_engine start to read voice data. An interrupt will be asserted when the counter up to idle_timeout_thd. This idle timeout is used for I2S/PDM work fail (Don't assert DMA request for a long time).
- Set VAD_TIMEOUT.work_timeout_thd=0x3ff, set VAD_TIMEOUT.work_timeout_en=0x1, set VAD_INT.work_timeout_int=0x1. After above setting, a counter is increase at AHB clock when dmac_engine is busy, the counter will be clear to 0 once dmac_engine is idle. An interrupt will be asserted when the counter up to work_timeout_thd. This work timeout is used for bus transmission congestion (a burst transferring is not completed for a long time).

Copyright 2022 © Rockchip Electronics Co., Ltd.

# Chapter 29 CAN

## 29.1 Overview

CAN (Controller Area Network) bus is a robust vehicle bus standard designed to allow microcontrollers and devices to communicate with each other in applications without a host computer. It is a message-based protocol, designed originally for multiplex electrical wiring within automobiles to save on copper, but is also used in many other contexts.

## 29.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.
CAN controller supports the following features:

- Support CAN 2.0B protocol
- Support 32-bit APB bus
- Support transmit or receive CAN standard frame
- Support transmit or receive CAN extended frame
- Support transmit or receive data frame, remote frame, overload frame, error frame and frame interval
- Support transmit or receive error count
- Support acceptance filtering
- Support Bit error, Bit stuffing error, Form error, ACK error and CRC error
- Support multiple types of interrupt and all interrupt can be masked
- Support CAN controller status query
- Support capture the bit position of arbitration section where the arbitration was lost
- Support error code check
- Support self-test mode
- Support single sample and three sample configurable
- Support SJW(Resynchronization Jump Width) configurable
- Support BRP(system prescale coefficient) configurable
- Support bit timing configurable
- Support loop-back mode for self-test operation
- Support silent mode for debug
- Support receive self-transmit data mode(rxstx_mode)
- Support TX data and RX data order select
- Support RX data cover mode
- Support auto retransmission mode
- Support auto bus on after bus-off state
- Support space_rx_mode
- Support transmitter delay compensation and SSP position configurable
- Support sleep mode
- Support timestamp
- Support transmit event FIFO
- Support 2 transmit buffers
- Support receive buffer/FIFO mode
- Support protocol exception event
- Support DMA

Copyright 2022 © Rockchip Electronics Co., Ltd. 

# 29.3 Function Description

## 29.3.1 Block Diagram

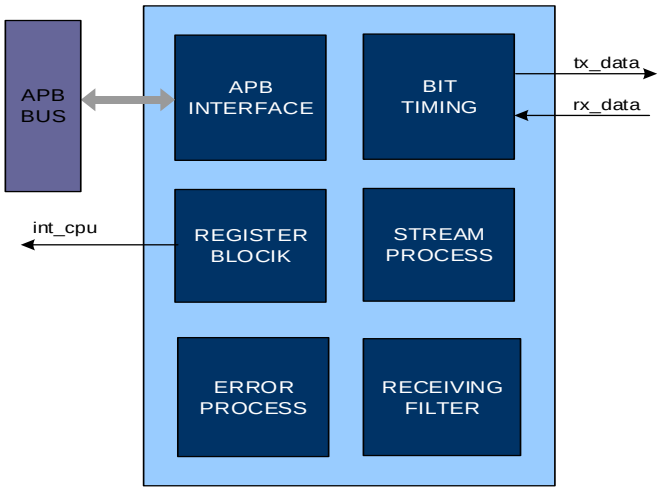



Fig. 29-1 CAN Controller Block Diagram

This version of CAN controller includes the previous version of CAN logic in compliance with old software application and new version of CAN logic with new software application.

## 29.3.2 ACCEPTANCE FILTER

The acceptance filter performs filtering using the acceptance ID register and the ID mask register. The acceptance filter uses multiple-time filtering. It includes the old version receiving filter and five addition ID filters. Each ID filter pair has a Filter Mask register and a Filter ID register. Each filter pair is controlled by corresponding FILTER CTRL bit in AFR register. For each pair using ID register and ID mask register (controlled by acceptance filter register) sampling all the bits of the ID, it is compared with the ID register. It is not a comparison every time a bit is sampled. And don't check the bit in the ID mask register that is 1. Once all the ID bits have passed the filtering, the controller considers the frame data as the desired ID, thereby performing the next operation.

## 29.3.3 BIT TIMING

### 29.3.3.1 Bit Timing Logic

The bit timing logic controls the sampling point position through the buffer bits in the timing register to ensure the accuracy of the data sampling. The bit timing logic receives the clock frequency division signal for identification, sets the bus timing parameters, establishes synchronization parameters, and adjusts the bus transmission rate. At the same time, the bus is monitored and the message to be sent is transmitted to the bus at the set timing. According to the provisions of the CAN protocol: the CAN bus is always at a high level when no message is sent, and the continuous recessive bit is monitored on the bus. At this time, the bus is in an idle state, and the arbitration priority is low, ready to receive data at any time. When the bus detects a transition from a recessive bit to a dominant bit, it is proved that the frame start bit starts transmitting, and the bus performs a hard synchronization in the bit start sync segment. Then, in the process of receiving the message, once the edge of the transition close to the sampling point is detected and the edge of the edge and the synchronization segment have a phase error lower than the synchronization width (SJW is taken when the value exceeds SJW), the controller executes once resynchronization, resynchronization can be performed multiple times during one data transmission.

### 29.3.3.2 Bit Timing Definition

The transmission time of each bit is divided into 4 parts:

$$t_{nbt} = t_{sync_seg} + t_{prop_seg} + t_{phase_seg1} + t_{phase_seg2}$$

$t_{sync_seg}$, $t_{prop_seg}$, $t_{phase_seg1}$ and $t_{phase_seg2}$ are integer multiples of the unit time($t_{sclk}$), and

Copyright 2022 © Rockchip Electronics Co., Ltd.

this unit time is a specific multiple of the system clock, which is determined by the division factor BRP in the bus timing register: 1. The counter is obtained by the BRP operation; 2. The system clock is counted by the counter; 3. When the limit is reached, a clock with a period of $t_{sclk}$ is generated.
In the system design, considering the cyclical occurrence of each time period, a state machine with three states is used in the bit timing design. The three states correspond to the sync segment(sync_seg) and the phase buffer segment 1 (phase_seg1=phase_seg1+prog_seg) and the phase buffer segment 2 (phase_seg2), respectively. Where PHASE_SEG1 range: 1~16; PHASE_SEG2 range: 1~8; BRP range: 1~64.

$$t_{sync_seg} = 1 \times t_{sclk}$$

$$t_{prop_seg} + t_{phase_seg1} = t_{sclk} \times (8 \times TSEG1.3 + 4 \times TSEG1.2 + 2 \times TSEG1.1 + TSEG1.0 + 1)$$

$$t_{phase_seg2} = t_{sclk} \times (4 \times TSEG2.2 + 2 \times TSEG2.1 + TSEG1.0 + 1)$$

Define a counter to count $t_{sclk}$. When the count reaches the TSEG1, TSEG2 defined in the bus timing register and the length of the synchronization segment defined in the design, the system will generate the corresponding transition conditions: go_seg1, go_seg2, go_sync. By judging these transition conditions, the control state machine cycles through the above three states.

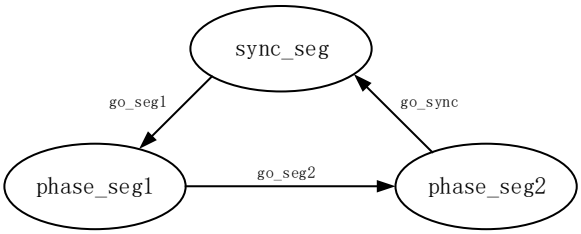



Fig. 29-2 Bit timing FSM

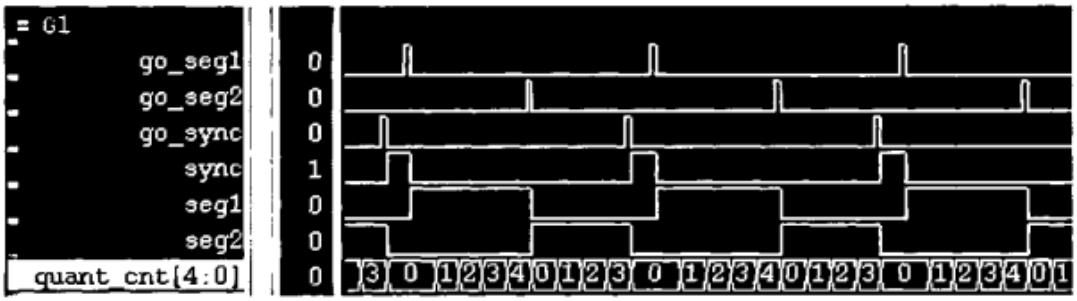
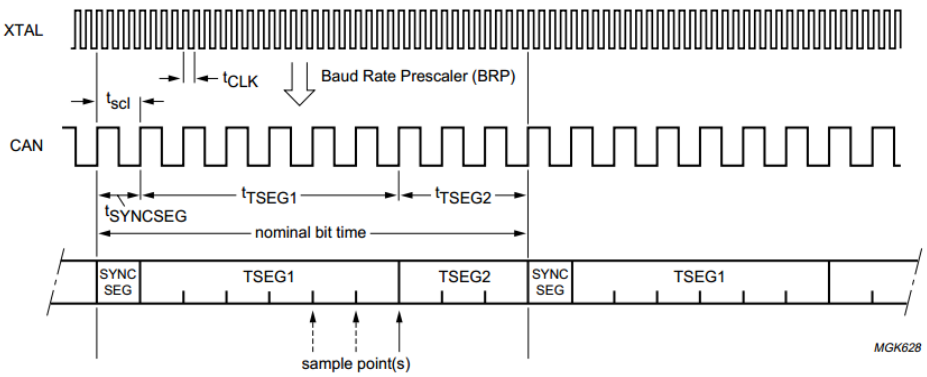



Fig. 29-3 Bit timing waveform diagram

#### 29.3.3.3 Sampling Point and Sending Point

**Sampling Point:** According to the agreement, the sample point should be between phase_seg1 and phase_seg2. It is designed to be in the position of phase_seg2 synchronization. The sampling pulse width is defined as one system clock cycle. Considering the accuracy of sampling, you can use the method of taking three samples to take the mean. The interval between each sample point is one $t_{sclk}$.

Copyright 2022 © Rockchip Electronics Co., Ltd.




Possible values are BRP = 000001, TSEG1 = 0101 and TSEG2 = 010.

Fig. 29-4 Three sampling diagram

**Sending Point:** The location of the transmit point should be at the beginning of each bit time according to the protocol, and it is designed to synchronize it with the go_sync signal. In addition, if it is in sync or resynchronize, transmit point will be valid immediately.

#### 29.3.3.4 Bit Synchronization

With the synchronization method, one or more nodes that satisfy the synchronization condition align their synchronization segments with the transmission data on the bus at a specific time. Synchronization occurs on the 1-to-0 transition edge in order to control the distance from the transition edge to the sample point. Two synchronization methods are defined in the CAN bus communication protocol: hard synchronization and resynchronization.

**Hard sync**: All nodes must be synchronized to the leading edge of the starting frame of the node that first started transmitting the message. At the beginning of each frame of data, a synchronization action is taken between the nodes.

Hard synchronization implementation method: determine whether the bus state meets the frame start condition specified in the protocol, and the node is not in the state of the data to be transmitted. At this time, a hard synchronization flag signal hard sync is generated, and the pulse width is a system clock; The hard sync entry is added to the control condition of the go_seg1 signal, and go_seg1 is valid immediately when the hard sync signal is '1'. Therefore, once the hard synchronization condition is met, the system enters the phase_seg1 segment, thereby achieving synchronization.

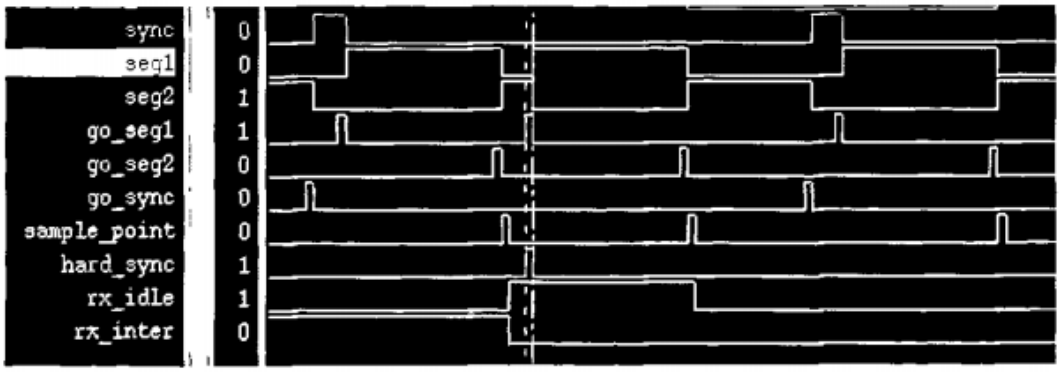



Fig. 29-5 Hard sync waveform diagram

**Resynchronization**: In addition to generating hard synchronization at the beginning of each frame of data, the CAN bus communication protocol also specifies the transmission of data for each frame. When the timing coordination between the nodes is not ideal, it will be resynchronized, so that the cooperation between the nodes is in a good state.

For the receiver, the bus changes it received should occur in the sync segment. Once the receiver's status violates this rule, the receiver will perform a resynchronization.

Two situations that require resynchronization:

- The jump of the bus value '1' to '0' occurs between the sync segment and the sample

Copyright 2022 © Rockchip Electronics Co., Ltd. 

point, which is a delay jump;
- The jump of the bus value '1' to '0' occurs between the sample point and the sync segment, which is an early jump.

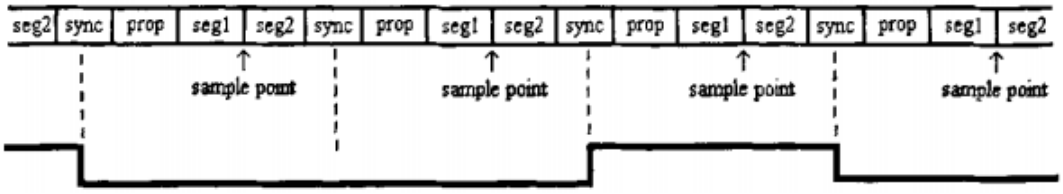



Fig. 29-6 Resynchronization

Resynchronization method:
1. Condition for resynchronization: the receiver is in a mode of receiving data (not inter-frame space or bus idle), and a resynchronization flag signal 'resync' is generated when a jump of the bus value '1' to '0' occurs;
2. According to the position of the resynchronization flag signal, it is determined that the abnormal jump is a delay jump or an early jump;
3. Counting the delay or the length of the advance by the counter;
4. In this bit, phase_seg1 is added with a delay time or phase_seg2 is subtracted from the advance time to obtain a new phase buffer time for the bit, thereby achieving synchronization.

## 29.3.4 STREAM PROCESS

### 29.3.4.1 Data Buffering

The data cache includes two parts: a transmit buffer and a receive buffer. The data to be sent on the CAN bus is loaded into the buffer area. This buffer area is called the "transmission buffer"; The data received from the CAN bus is also stored in the buffer area, which is called the "receiver buffer". The size of the buffer is 13 bytes, including one-byte frame information, 2 to 4 bytes identifiers (standard or extended frame), and 8 bytes of data.
CPU configures the transmission of the data information (frame information, identification code, data), and then enable the transmit bit. The transmit data information is spliced into a parallel complete data to be transmitted (including the CRC check code) according to the current frame information and stored in transmission buffer. Stream process unit wait for the appropriate time to send data to the bit timing unit.
The received message is placed in the receiving buffer. After receiving, the receiving completion interrupt will be generated. After receiving the interrupt, the CPU will read the data in the receiving buffer and clear the receiving buffer, and STATE [0] will be 0. If the CPU does not read in time, STATE [1] will remain at 1. If a new message is received at this time, overflow will occur and not respond with ack by default.
In new design, there is another independent transmit buffer which has another corresponding transmit request bit. Besides, there is a receive FIFO can be configured to use. Rx data has a RDATA address to be read by host. The size of data is 18 word (one-word frame information, one-word Id, 16-words data) for transmit and 19 word (1-word timestamp additional) for receive. Rx FIFO has 32bits×128 memory space which allow to contain 6 receive message.
Two transmit request bit in CAN_CMD corresponds to two transmit buffers. Transmit message must written to registers before setting transmit request bit. After setting transmit request bit, transmit messages in registers stores in corresponding transmit buffer. When the RKCAN buffer1 transmission frame complete, 'tx_req_1' is automatically cleared to 0.
CAN support RX FIFO. When FIFO enabled, receive data stored in FIFO as Receive FIFO message format shown below. Receive data should read from the RXFIFO entrance. IF FIFO is disabled, receive data stored in RXDATA registers and should read from those registers every time.

Copyright 2022 © Rockchip Electronics Co., Ltd. 

Table 29-1 Receive FIFO message format

| NAME | Offset | Access | Description |
|---|---|---|---|
| RX FIFO RB0-INFO | 0x0000 | RO | Same as CAN_RXFRAMEINFO |
| RX FIFO RB0-ID | 0x0004 | RO | Same as CAN_RXID |
| RX FIFO TB0-TIMESTAMP | 0x0008 | RO | RX TIMESTAMP VALUE |
| RX FIFO RB0-DATA0 | 0x000c | RO | Same as CAN_RXDATA |
| RX FIFO RB0-DATA1 | 0x0010 | RO | Same as CAN_RXDATA |
| RX FIFO RB0-DATA2 | 0x0014 | RO | Same as CAN_RXDATA |
| … | … | … | … |
| RX FIFO RB0-DATA15 | 0x0048 | RO | Same as CAN_RXDATA |

### 29.3.4.2 Receive Data

According to the bus protocol, taking the data frame of the extended frame format as an example, the receiving data state machine is as follows:

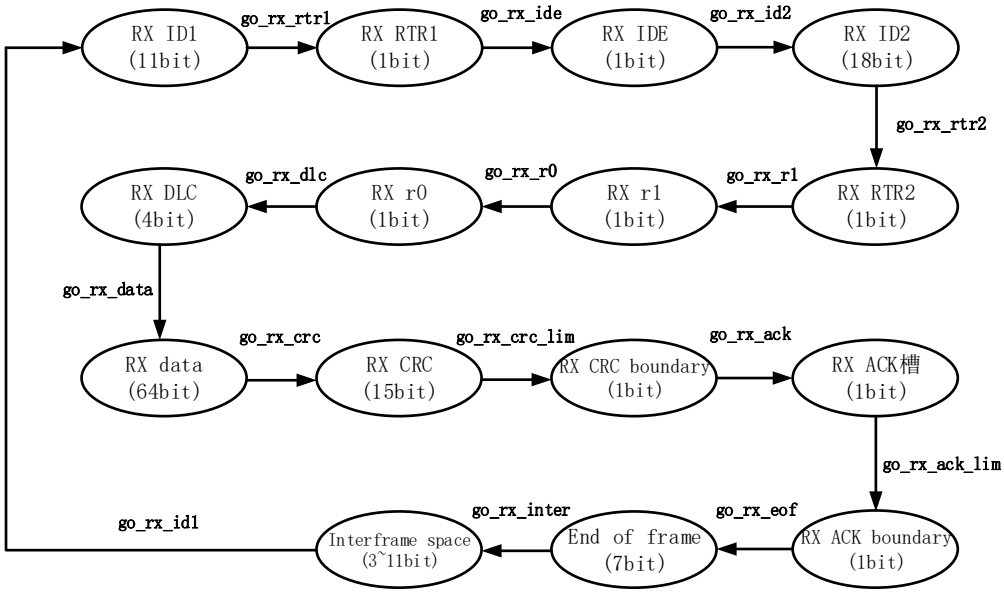



Fig. 29-7 Receive data state diagram

Each state of the state machine corresponds to which "field" of the frame data the receiver is in when receiving data, and only one of all state flags is valid at the same time. The method of implementation is as follows: Define a bit counter, add one to each sample point (provided by the bit timing module). At the same time, according to the current state of the state machine, it is determined in this state that the bit counter needs to count to what value (determined by the length of each field defined in the protocol) to generate a jump signal to the next state transition. Whenever a hopping signal is generated, the counter is cleared and ready to begin counting for the next state.

The receiving state machine ensures that the bus controller can automatically recognize the current receiving state when receiving data. After that, the data of each data field needs to be stored in the corresponding register according to different states, and then the next operation is performed.

### 29.3.4.3 Transmit Data

CAN accesses message element space of a buffer in TX block only if the respective request bit is set. The Host must respect access rules to avoid memory collisions, that is, after the Host sets a buffer ready request through the CMD register, it should not read or write the respective message element space until the respective request bit is in a clear/unset state.

Copyright 2022 © Rockchip Electronics Co., Ltd. 

Parallel data is serially transmitted to the bus according to a specific timing. The sending point is the tx_point. The transmit counter is self-added in the valid data portion of the data frame, and is cleared when one frame of data is transmitted or the bus is in an error state. The implementation is as follows: Combine all the data to be sent into a completely parallel data chain according to the currently set frame type; Using tx_pointer as a data link pointer, obtaining a serial data signal (tx_bit) to be transmitted; Determine what type of data to send according to the current state, and determine the data tx_next to be sent at the next transmission time; Synchronize the data transmission signal tx with the tx_next through the transmission point tx_point to obtain a true transmission signal tx.

#### 29.3.4.4 Bit Stuffing

Bit stuffing is a function set to prevent burst errors. Add a bit of inversion data when the same level lasts 5 bits.

- **Sending unit**

The data between the SOF and CRC segments when transmitting data frames and remote frames. If the same level lasts for 5 bits, the next bit (bit 6) is inserted with the level of the 1st bit and the first 5 bits.

- **Receiving unit**

Data between SOF and CRC segments when receiving data frames and remote frames. If the same level lasts for 5 digits, the next bit (bit 6) needs to be deleted and received. If the 6th bit is the same level as the first 5 bits, it will be treated as an error and an error frame will be sent.

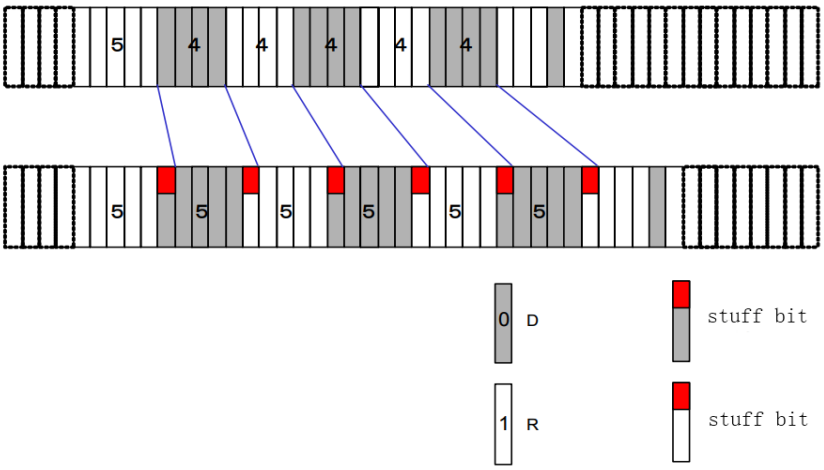



Fig. 29-8 Bit Stuffing

#### 29.3.4.5 Transmit Event FIFO

The Transmit Event FIFO (TEF) allows the application to keep track of the order and time the messages were transmitted. The TEF works similar to a Receive FIFO, which is a 32bits×16 FIFO. Instead of storing received messages, it stores transmitted messages. Messages are only saved if TEF enable is set. The Sequence Number (SEQ) of the transmitted message is copied into the TEF Object. The payload data are not stored. Transmitted messages are timestamped if TEFTSEN is set. Transmit message format store in TXE FIFO as follow:

Copyright 2022 © Rockchip Electronics Co., Ltd.

Table 29-2 TXE FIFO message format

| NAME | Offset | Access | Description |
|---|---|---|---|
| TXE FIFO TB0-INFO | 0x0000 | RO | Same as CAN_TXFRAMEINFO |
| TXE FIFO TB0-ID | 0x0004 | RO | Same as CAN_TXID |
| TXE FIFO TB0-TIMESTAMP | 0x0008 | RO | TX TIMESTAMP VALUE |
| TXE FIFO TB1-INFO | 0x000c | RO | Same as CAN_TXFRAMEINFO |
| TXE FIFO TB1-ID | 0x0010 | RO | Same as CAN_TXID |
| TXE FIFO TB1-TIMESTAMP | 0x0014 | RO | TX TIMESTAMP VALUE |
| … | … | … | … |

#### 29.3.4.6 TIMESTAMP

CAN Controller module contains a Time Base Counter(TBC). The TBC is a 32-bit free-running counter that increments on multiples of CAN clock and rolls over to zero. TBC can be cleared by writing any value to TBC.

- TIMESTAMP_CTRL is used to configure the prescale for the TBC.
- Setting TIMESTAMP_CTRL.TBCEN enables the TBC.
- Clearing TBCEN disables, stops and resets the TBC.
- The TBC has to be disabled before writing to TBC by clearing TBCEN.
- The application can read TBC at any time. Like with any multibyte counter, the application has to consider that the counter increments and might rollover between reading the different bytes of the counter. A rollover of the TBC will generate an interrupt.

Capturing of time stamps at the sample points of the Start of Frame bits of received and transmitted frames.

### 29.3.5 ERROR PROCESS

There are five types of errors. Multiple errors can occur at the same time.

- **BIT ERROR**:

A unit that is sending a bit on the bus also monitors the bus. A BIT ERROR has to be detected at that bit time, when the bit value that is monitored is different form the bit value that is sent. An exception is the sending of a 'recessive' bit during the stuffed bit stream of the ARBITRATION FIELD of during the ACK SLOT. Then no BIT ERROR occurs when a 'dominant' bit is monitored. A TRANSMITTER sending a PASSIVE ERROR FLAG and detecting a 'dominant' bit does not interpret this as a BIT ERROR.

- **BIT STUFF ERROR**:

A STUFF ERROR has to be detected at the bit time of the $6^{th}$ consecutive equal bit level in a message field that should be coded by the method of bit stuffing.

- **FORM ERROR**:

A FORM ERROR has to be detected when a fixed-form bit field contains one or more illegal bits. (Exception is the detection of a dominant bit during the last bit of END OF FRAME by a RECEIVER, or the detection of a dominant bit during the last bit of ERROR DELIMITER or OVERLOAD DELIMITER by any node). FORM-ERROR.

- **ACK ERROR**:

An ACK ERROR has to be detected by a transmitter whenever it does not monitor a 'dominant' bit during the ACK SLOT.

- **CRC ERROR**:

The CRC sequence consists of the result of the CRC calculation by the transmitter. The receivers calculate the CRC in the same way as the transmitter. A CRC ERROR has to be detected, if the calculated result is not the same as that received in the CRC sequence.

## 29.4 Register Description

### 29.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as

follows.

### 29.4.2 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CAN_MODE | 0x0000 | W | 0x00000000 | Mode Configure Register |
| CAN_CMD | 0x0004 | W | 0x00000000 | Request Command Register |
| CAN_STATE | 0x0008 | W | 0x00000000 | Controller State Register |
| CAN_INT | 0x000C | W | 0x00000000 | Interrupt State Register |
| CAN_INT_MASK | 0x0010 | W | 0x00000000 | Interrupt Mask Registers |
| CAN_DMA_CTRL | 0x0014 | W | 0x00000000 | DMA Mode Control Register |
| CAN_BITTIMING | 0x0018 | W | 0x00000000 | Bit Timing Configure Register. This register work in CAN mode. |
| CAN_ARBITFAIL | 0x0028 | W | 0x00000000 | Arbiter Fail Code Register |
| CAN_ERROR_CODE | 0x002C | W | 0x00000000 | Error Code Register |
| CAN_RXERRORCNT | 0x0034 | W | 0x00000000 | Receive Error Counter Register |
| CAN_TXERRORCNT | 0x0038 | W | 0x00000000 | Transmit Error Counter Register |
| CAN_IDCODE | 0x003C | W | 0x00000000 | ID Code Register |
| CAN_IDMASK | 0x0040 | W | 0x00000000 | ID Code Bit Mask Register |
| CAN_TXFRAMEINFO | 0x0050 | W | 0x00000000 | CAN Mode TX Frame Information Configuration Register |
| CAN_TXID | 0x0054 | W | 0x00000000 | CAN Mode Transmit ID Code Register. |
| CAN_TXDATA0 | 0x0058 | W | 0x00000000 | CAN Mode Transmit Data0 Register. |
| CAN_TXDATA1 | 0x005C | W | 0x00000000 | CAN Mode Transmit Data1 Register. |
| CAN_RXFRAMEINFO | 0x0060 | W | 0x00000000 | CAN Mode RX Frame Information Register |
| CAN_RXID | 0x0064 | W | 0x00000000 | CAN Mode Receive ID. |
| CAN_RXDATA0 | 0x0068 | W | 0x00000000 | CAN Mode Receive Data Reg0. |
| CAN_RXDATA1 | 0x006C | W | 0x00000000 | CAN Mode Receive Data Reg1. |
| CAN_RTL_VERSION | 0x0070 | W | 0x00000022 | CAN RTL version |
| CAN_FD_NOMINAL_BITTIMING | 0x0100 | W | 0x00000000 | CAN Nominal Bit Timing Configure Register |
| CAN_TIMESTAMP_CTRL | 0x010C | W | 0x00000000 | Timestamp Counter Configure Register |
| CAN_TIMESTAMP | 0x0110 | W | 0x00000000 | Timestamp Counter |
| CAN_TXEVENT_FIFO_CTRL | 0x0114 | W | 0x00000000 | Tx Event FIFO Configure register |
| CAN_RX_FIFO_CTRL | 0x0118 | W | 0x00000000 | Rx FIFO Configure Register |
| CAN_AFR_CTRL | 0x011C | W | 0x00000000 | Acceptance Filter Register Control |
| CAN_IDCODE0 | 0x0120 | W | 0x00000000 | ID Code Register 0 |
| CAN_IDMASK0 | 0x0124 | W | 0x00000000 | ID Mask Register 0 |
| CAN_IDCODE1 | 0x0128 | W | 0x00000000 | ID Code Register 1 |
| CAN_IDMASK1 | 0x012C | W | 0x00000000 | ID Mask Register 1 |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| CAN_IDCODE2 | 0x0130 | W | 0x00000000 | ID Code Register 2 |
| CAN_IDMASK2 | 0x0134 | W | 0x00000000 | ID Mask Register 2 |
| CAN_IDCODE3 | 0x0138 | W | 0x00000000 | ID Code Register 3 |
| CAN_IDMASK3 | 0x013C | W | 0x00000000 | ID Mask Register 3 |
| CAN_IDCODE4 | 0x0140 | W | 0x00000000 | ID Code Register 4 |
| CAN_IDMASK4 | 0x0144 | W | 0x00000000 | ID Mask Register 4 |
| CAN_NEW_TXFRAMEINFO | 0x0200 | W | 0x00000000 | CAN TX Frame Information Configuration Register |
| CAN_NEW_TXID | 0x0204 | W | 0x00000000 | CAN Transmit ID Register |
| CAN_NEW_TXDATA0 | 0x0208 | W | 0x00000000 | CAN Transmit DATA0 |
| CAN_NEW_TXDATA1 | 0x020C | W | 0x00000000 | CAN Transmit DATA1 |
| CAN_NEW_RXFRAMEINFO | 0x0300 | W | 0x00000000 | CAN RX Frame Information Configuration Register |
| CAN_NEW_RXID | 0x0304 | W | 0x00000000 | CAN Receive ID |
| CAN_NEW_RXTIMESTAMP | 0x0308 | W | 0x00000000 | CAN Receive Timestamp |
| CAN_NEW_RXDATA0 | 0x030C | W | 0x00000000 | CAN Receive Data Reg0. |
| CAN_NEW_RXDATA1 | 0x0310 | W | 0x00000000 | CAN Receive Data Reg1. |
| CAN_RX_FIFO_RDATA | 0x0400 | W | 0x00000000 | Rx FIFO Read Data |
| CAN_TXE_FIFO_RDATA | 0x0500 | W | 0x00000000 | Tx Event FIFO Read Data |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 29.4.3 Detail Registers Description

**CAN_MODE**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x0000 | reserved |
| 12 | RW | 0x0 | space_rx_mode<br>Interframe Spacing RX Mode.<br>1'b0: Enable.<br>1'b1: Disable. |
| 11 | RW | 0x0 | auto_bus_on<br>Auto Bus on Enable.<br>1'b0: After the RKCAN has entered bus_off state, the software can start a bus_off_recovery sequence by resetting the work_mode to 0.<br>1'b1: Automatic reset TEC/REC to bus_on after 128 occurrences of 11 consecutive recessive bits have been monitored on the bus. |
| 10 | RW | 0x0 | auto_retx_mode<br>Auto Retransmission Mode.<br>1'b0: Disable. RKCAN return to idle state after transmit DATA/RTR frame failed, and set tx_req to 0.<br>1'b1: Enable. The RKCAN automatically retransmit frames which have lost arbitration or have been disturbed by errors during transmission. |
| 9 | RW | 0x0 | ovld_mode<br>Overload Mode.<br>1'b0: overload lite mode.<br>1'b1: overload extended mode. RKCAN |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | cover_mode<br>Rx Data Cover Mode.<br>1'b0: RKCAN can't receive new frame before receive registers cleared.<br>1'b1: RKCAN can receive new frame before receive registers cleared, and new rxdata will cover old rxdata. |
| 7 | RW | 0x0 | rxsort_mode<br>RX Data Sort Mode.<br>1'b0: The data received first is placed in the lower address.<br>1'b1: The data received first moves to the upper address, and the data received later is placed at the lower address. |
| 6 | RW | 0x0 | txorder_mode<br>TX Data Order Mode.<br>1'b0: tx_data1[7:0] --> tx_data1[15:8] --> tx_data1[23:16] --> tx_data1[31:24] -->tx_data2[7:0] --> tx_data2[15:8] --> tx_data2[23:16] --> tx_data2[31:24].<br>1'b1: tx_data2[31:0] --> tx_data1[31:0]. |
| 5 | RW | 0x0 | rxstx_mode<br>Receive Self Transmit data mode.<br>1'b0: Disable;<br>1'b1: Enable. When the RKCAN sends data, it can also receive the data sent by itself. |
| 4 | RW | 0x0 | lback_mode<br>Loopback Mode.<br>1'b0: Disable.<br>1'b1: Enable. |
| 3 | RW | 0x0 | silent_mode<br>Silent Mode.<br>1'b0: Disable.<br>1'b1: Enable. |
| 2 | RW | 0x0 | self_test<br>Self check ACK slot when TX frame.<br>1'b0: Normal<br>1'b1: Self-test mode. When in self_test mode, the receiver does not need to return an ACK signal when receiving data. Therefore, no error ack will occur in self_test mode. When in lback_mode or silent_mode, it needs to enable self_test mode when sending frame. |
| 1 | RW | 0x0 | sleep_mode<br>Sleep Mode<br>This is the Sleep mode request bit.<br>1'b0: No such request.<br>1'b1: Request core to be in Sleep mode.<br>This bit is cleared when the core wakes up from Sleep mode. |
| 0 | RW | 0x0 | work_mode<br>Work Mode.<br>1'b0: Idle mode, CAN stop transmit and registers can be configured.<br>1'b1: Work mode, CAN enter the working mode, Receive/transmit data. |

**CAN_CMD**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | R/W SC | 0x0 | tx1_req<br>Transmit request enable<br>1'b0: Disable<br>1'b1: Enable<br>When 'tx1_req' is enable, the RKCAN buffer1 is in the transmit mode and cannot receive frames from other CANs. When the RKCAN buffer1 transmission frame complete, 'tx1_req' is automatically cleared to 0. Also, when RKCAN is set 'work_mode' to 'reset_mode', tx_req' is cleared to 0. |
| 0 | R/W SC | 0x0 | tx0_req<br>Transmit request enable<br>1'b0: Disable<br>1'b1: Enable<br>When 'tx0_req' is enable, the RKCAN buffer0 is in the transmit mode and cannot receive frames from other CANs. When the RKCAN buffer0 transmission frame complete, 'tx0_req' is automatically cleared to 0. Also, when RKCAN is set 'work_mode' to 'reset_mode', tx_req' is cleared to 0. |

**CAN_STATE**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6 | RO | 0x0 | sleep_state<br>Sleep state<br>1'b0: None<br>1'b1: CAN controller is in the sleep state |
| 5 | RO | 0x0 | bus_off_state<br>Bus off state<br>1'b0: None<br>1'b1: Bus off state: When the error counter is incremented to 255, the CAN controller will enter the bus off state, generate an error warning interrupt and enter reset mode, waiting for the CPU to restart. (rx/tx_err_cnt >=32'd255) |
| 4 | RO | 0x0 | error_warning_state<br>Error warning state<br>1'b0: None<br>1'b1: Error state: At least one error counter has reached the error warning threshold (rx/tx_err_cnt >=32'd96) |
| 3 | RO | 0x0 | tx_period<br>Transmit state<br>1'b0: Not in transmit state<br>1'b1: CAN controller is in the transmit state |
| 2 | RO | 0x0 | rx_period<br>Receive state<br>1'b0: Not in receive state<br>1'b1: CAN controller is in the receive state |
| 1 | RO | 0x0 | tx_buffer_full<br>Transmit buffer full flag bit<br>1'b0: Not full<br>1'b1: TX buffer is full. There is data in buffer waiting to be sent or being sent. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RO | 0x0 | rx_buffer_full<br>Receive buffer full flag bit<br>1'b0: Not full<br>1'b1: RX buffer is full. A complete message is stored in the buffer. |

**CAN_INT**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:15 | RO | 0x00000 | reserved |
| 14 | W1C | 0x0 | wakeup_int<br>Wakeup Interrupt<br>1'b0: None<br>1'b1: Indicates that the core entered Normal mode from Sleep mode. Write 1 then clear. |
| 13 | W1C | 0x0 | txe_fifo_full_int<br>TXE FIFO Full Interrupt<br>1'b0: None<br>1'b1: Indicates that TX Event FIFO is full based on watermark programming.<br>The interrupt continues to assert as long as the TX Event FIFO Full Level is above TX Event FIFO Full watermark. |
| 12 | W1C | 0x0 | tx_event_fifo_overflow_int<br>TXE FIFO Overflow Interrupt<br>1'b0 None<br>1'b1 Indicates that a message has been lost. This condition occurs when the core has successfully transmitted a message for which an event store is requested but the TX Event FIFO is full. |
| 11 | W1C | 0x0 | timestamp_counter_overflow_int<br>Timestamp Overflow Interrupt<br>1'b0: None<br>1'b1: Indicates that Timestamp counter rolled over (from 0xffff to 0x0). Write 1 then clear. |
| 10 | W1C | 0x0 | bus_off_recovery_int<br>Bus off Recover Interrupt<br>1'b0: None<br>1'b1: Indicates that the core is recovered from Bus-off mode. Write 1 then clear. |
| 9 | W1C | 0x0 | bus_off_int<br>Bus Off Interrupt<br>1'b0: None<br>1'b1: Indicates that the CAN core entered Bus-off mode. Write 1 then clear. |
| 8 | W1C | 0x0 | rx_fifo_overflow_int<br>RX FIFO Overflow Interrupt (RX FIFO ENABLE).<br>1'b0: None<br>1'b1: Indicates that a message has been lost. This condition occurs<br>when a new message with ID matching to Receive FIFO is received and the Receive FIFO is full. |
| 7 | W1C | 0x0 | rx_fifo_full_int<br>RX FIFO full Interrupt (FIFO Mode enable).<br>1'b0: None<br>1'b1: Indicates that RX FIFO is full based on watermark setting. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | W1C | 0x0 | error_int<br>Bus Error Interrupt<br>1'b0: None<br>1'b1: CAN bus error interrupt. This interrupt is generated when a bus error is detected. Error details can refer to the ERROR_CODE register. Write 1 then clear. |
| 5 | W1C | 0x0 | tx_arbit_fail_int<br>Transmit Arbitration loss Interrupt<br>1'b0: None<br>1'b1: Arbitration loss interrupt. This interrupt is generated when the loss of arbitration is turned into a receiver. Write 1 then clear. |
| 4 | W1C | 0x0 | passive_error_int<br>Passive Error Interrupt<br>1'b0: None<br>1'b1: Passive error interrupt. This interrupt is generated when the controller enters an error passive state (at least one error counter reaches 127) or returns from the error passive state to the error active state. Write 1 then clear. |
| 3 | W1C | 0x0 | overload_int<br>Overload Interrupt<br>1'b0: None<br>1'b1: CAN bus overload interrupt. This interrupt is generated when a overload frame is generated. |
| 2 | W1C | 0x0 | error_warning_int<br>Error warning interrupt<br>1'b0: None<br>1'b1: Error_warning_int. This interrupt is generated when the error_warning_state bits change. Write 1 then clear. |
| 1 | W1C | 0x0 | tx_finish_int<br>Transmit finish interrupt<br>1'b0: None<br>1'b1: Transmit finish interrupt. CAN controller sends the message. Write 1 then clear. |
| 0 | W1C | 0x0 | rx_finish_int<br>Receive Finish Interrupt<br>1'b0: None<br>1'b1: Receive finish int. CAN controller has received the message and the rx_buffer is full. Write 1 then clear. |

**CAN_INT_MASK**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:15 | RO | 0x00000 | reserved |
| 14 | RW | 0x0 | wakeup_int_mask<br>1'b0: Unmasked<br>1'b1: Masked |
| 13 | RW | 0x0 | txe_fifo_full_int_mask<br>1'b0: Unmasked<br>1'b1: Masked |
| 12 | RW | 0x0 | txe_fifo_overflow_int_mask<br>1'b0: Unmasked<br>1'b1: Masked |
| 11 | RW | 0x0 | timestamp_cnt_overflow_int_mask<br>1'b0: Unmasked<br>1'b1: Masked |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10 | RW | 0x0 | bus_off_recovery_int_mask<br>1'b0: Unmasked<br>1'b1: Masked |
| 9 | RW | 0x0 | bus_off_int_mask<br>1'b0: Unmasked<br>1'b1: Masked |
| 8 | RW | 0x0 | rx_fifo_overflow_int_mask<br>1'b0: Unmasked<br>1'b1: Masked |
| 7 | RW | 0x0 | rx_fifo_full_int_mask<br>1'b0: Unmasked<br>1'b1: Masked |
| 6 | RW | 0x0 | error_int_mask<br>1'b0: Unmasked<br>1'b1: Masked |
| 5 | RW | 0x0 | tx_arbit_fail_int_mask<br>1'b0: Unmasked<br>1'b1: Masked |
| 4 | RW | 0x0 | passive_error_int_mask<br>1'b0: Unmasked<br>1'b1: Masked |
| 3 | RW | 0x0 | rx_buffer_overflow_int_mask<br>1'b0: Unmasked<br>1'b1: Masked |
| 2 | RW | 0x0 | error_warning_int_mask<br>1'b0: Unmasked<br>1'b1: Masked |
| 1 | RW | 0x0 | tx_finish_int_mask<br>1'b0: Unmasked<br>1'b1: Masked |
| 0 | RW | 0x0 | rx_finish_int_mask<br>1'b0: Unmasked<br>1'b1: Masked |

**CAN_DMA_CTRL**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | dma_rx_mode<br>DMA receive request enable<br>1'b0: Disable<br>1'b1: Enable<br>When dma_rx_mode is enabled, the RKCAN is in the DMA receive mode. Also, when RKCAN is set work_mode to reset_mode, tx_req is clear. |
| 0 | RW | 0x0 | dma_tx_mode<br>DMA Transmit request enable<br>1'b0: Disable<br>1'b1: Enable<br>When dma_tx_mode is enabled, the RKCAN is in the DMA transmit mode. When RKCAN is set work_mode to reset_mode, tx_req is cleared to 0. |

**CAN_BITTIMING**

Address: Operational Base + offset (0x0018)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16 | RW | 0x0 | sample_mode<br>CAN controller sampling mode configuration register.<br>1'b0: Single sample mode<br>1'b1: Three sample mode |
| 15:14 | RW | 0x0 | sjw<br>SJW: Resynchronization Jump Width<br>Each unit has a synchronization error due to a clock frequency deviation or a transmission delay. SJW is to compensate for the maximum value of this error. |
| 13:8 | RW | 0x00 | brp<br>brp: system prescale coefficient<br>Tsclk = 2 x Tclk x (brp + 1). |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x0 | tseg2<br>Phase buffer segment 2<br>Tphase_seg2 = Tsclk x (tseg2 + 1) |
| 3:0 | RW | 0x0 | tseg1<br>Phase buffer segment 1<br>Tphase_seg1 = Tsclk x (tseg1 + 1) |

**CAN_ARBITFAIL**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6:0 | RO | 0x00 | arbit_fail_code<br>This register indicates the bit position of arbitration section where the arbitration was lost. |

**CAN_ERROR_CODE**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29 | RO | 0x0 | error_phase<br>1'b0: Arbitration Phase<br>1'b1: Data Phase |
| 28:26 | RO | 0x0 | error_type<br>Error type:<br>3'b000: BIT ERROR<br>3'b001: BIT STUFF ERROR<br>3'b010: FORM ERROR<br>3'b011: ACK ERROR<br>3'b100: CRC ERROR |
| 25 | RO | 0x0 | error_direction<br>1'b0: TX error<br>1'b1: RX error |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 24:16 | RO | 0x000 | tx_error_position<br>Indicate transmit error position.<br>9'b000000001: TRANSMIT_IDLE.<br>9'b000000010: TRANSMIT_SOF_DLC.<br>9'b000000100: TRANSMIT_DATA.<br>9'b000001000: TRANSMIT_STUFF_COUNT.<br>9'b000010000: TRANSMIT_CRC.<br>9'b000100000: TRANSMIT_ACK_EOF.<br>9'b001000000: TRANSMIT_ACK.<br>9'b010000000: TRANSMIT_ERROR.<br>9'b100000000: TRANSMIT_OVERLOAD. |
| 15:0 | RO | 0x0000 | rx_error_position<br>Indicate receive error position<br>16'b0000000000000001: RECEIVE_IDLE<br>16'b0000000000000010: RECEIVE_SOF_IDE<br>16'b0000000000000100: RECEIVE_ID2_RTR<br>16'b0000000000001000: RECEIVE_FDF<br>16'b0000000000010000: RECEIVE_RES<br>16'b0000000000100000: RECEIVE_BRS_ESI<br>16'b0000000001000000: RECEIVE_DLC<br>16'b0000000010000000: RECEIVE_DATA<br>16'b0000000100000000: RECEIVE_STUFF_COUNT<br>16'b0000001000000000: RECEIVE_CRC<br>16'b0000010000000000: RECEIVE_CRC_LIM<br>16'b0000100000000000: RECEIVE_ACK<br>16'b0001000000000000: RECEIVE_ACK_LIM<br>16'b0010000000000000: RECEIVE_EOF<br>16'b0100000000000000: RECEIVE_SPACE<br>16'b1000000000000000: RECEIVE_BUF_INT |

**CAN_RXERRORCNT**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | rx_err_cnt<br>Receive Error Counter (REC).<br>Actual state of the Receive Error Counter. Value between 0 and 127. |

**CAN_TXERRORCNT**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:9 | RO | 0x000000 | reserved |
| 8:0 | RO | 0x000 | tx_err_cnt<br>Transmit Error Counter (TEC).<br>Actual state of the Transmit Error Counter. Value between 0 and 255. |

**CAN_IDCODE**

Address: Operational Base + offset (0x003C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 28:0 | RW | 0x00000000 | id_code<br>CAN controller ID code:<br>Standard frame ID: id_code[10:0];<br>Extended frame ID: id_code[28:0]. |

**CAN_IDMASK**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:0 | RW | 0x00000000 | id_mask<br>ID mask for each ID code bit<br>1'b0: Unmasked<br>1'b1: Masked |

**CAN_TXFRAMEINFO**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RW | 0x0 | txframe_format<br>1'b0: Standard frame<br>1'b1: Extended frame |
| 6 | RW | 0x0 | tx_rtr<br>1'b0: Data frame<br>1'b1: Remote frame |
| 5:4 | RO | 0x0 | reserved |
| 3:0 | RW | 0x0 | txdata_length<br>Transmit data length configure register. (unit: byte)<br>4'b0000: 0byte<br>4'b0001: 1byte<br>4'b0010: 2byte<br>4'b0011: 3byte<br>4'b0100: 4byte<br>4'b0101: 5byte<br>4'b0110: 6byte<br>4'b0111: 7byte<br>4'b1000: 8byte<br>others: reserved |

**CAN_TXID**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:0 | RW | 0x00000000 | tx_id<br>can_tx_id[28:0] |

**CAN_TXDATA0**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | tx_data0<br>tx_data0 |

**CAN_TXDATA1**

Address: Operational Base + offset (0x005C)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | tx_data1<br>tx_data1 |

**CAN_RXFRAMEINFO**

Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RC | 0x0 | rxframe_format<br>1'b0: Standard frame<br>1'b1: Extended frame<br>This register needs to be read(clear) before receiving the next frame. |
| 6 | RC | 0x0 | rx_rtr<br>1'b0: Data frame<br>1'b1: Remote frame<br>This register needs to be read(clear) before receiving the next frame. |
| 5:4 | RO | 0x0 | reserved |
| 3:0 | RC | 0x0 | rxdata_length<br>Receive data length register. (unit: byte)<br>4'b0000: 0byte<br>4'b0001: 1byte<br>4'b0010: 2byte<br>4'b0011: 3byte<br>4'b0100: 4byte<br>4'b0101: 5byte<br>4'b0110: 6byte<br>4'b0111: 7byte<br>4'b1000: 8byte<br>others: reserved<br>This register needs to be read(clear) before receiving the next frame. |

**CAN_RXID**

Address: Operational Base + offset (0x0064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:0 | RC | 0x00000000 | rx_id<br>rx_id[28:0]<br>This register needs to be read(clear) before receiving the next frame. |

**CAN_RXDATA0**

Address: Operational Base + offset (0x0068)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RC | 0x00000000 | rx_data0<br>rx_data0[31:0]<br>This register needs to be read(clear) before receiving the next frame. |

**CAN_RXDATA1**

Address: Operational Base + offset (0x006C)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RC | 0x00000000 | rx_data1<br>rx_data1[31:0]<br>This register needs to be read(clear) before receiving the next frame. |

**CAN_RTL_VERSION**

Address: Operational Base + offset (0x0070)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000022 | version<br>CAN rtl version = 32'h22 |

**CAN_FD_NOMINAL_BITTIMING**

Address: Operational Base + offset (0x0100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | sample_mode<br>CAN controller sampling mode configuration register.<br>1'b0: Single sample mode<br>1'b1: Three sample mode |
| 30:24 | RW | 0x00 | sjw<br>SJW: Resynchronization Jump Width<br>Each unit has a synchronization error due to a clock frequency deviation or a transmission delay. SJW is to compensate for the maximum value of this error. |
| 23:16 | RW | 0x00 | brq<br>brp: system prescale coefficient<br>Tsclk = 2 x Tclk x (brp + 1). |
| 15 | RO | 0x0 | reserved |
| 14:8 | RW | 0x00 | tseg2<br>Phase buffer segment 2<br>Tphase_seg2 = Tsclk x (tseg2 + 1) |
| 7:0 | RW | 0x00 | tseg1<br>Phase buffer segment 1<br>Tphase_seg1 = Tsclk x (tseg1 + 1) |

**CAN_FD_DATA_BITTIMING**

Address: Operational Base + offset (0x0104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21 | RW | 0x0 | sample_mode<br>CAN controller sampling mode configuration register.<br>1'b0: Single sample mode<br>1'b1: Three sample mode |
| 20:17 | RW | 0x0 | sjw<br>SJW: Resynchronization Jump Width<br>Each unit has a synchronization error due to a clock frequency deviation or a transmission delay. SJW is to compensate for the maximum value of this error. |
| 16:9 | RW | 0x00 | brq<br>brp: system prescale coefficient<br>Tsclk = 2 x Tclk x (brp + 1). |
| 8:5 | RW | 0x0 | tseg2<br>Phase buffer segment 2<br>Tphase_seg2 = Tsclk x (tseg2 + 1) |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4:0 | RW | 0x00 | tseg1<br>Phase buffer segment 1<br>Tphase_seg1 = Tsclk x (tseg1 + 1) |

**CAN_TRANSMIT_DELAY_COMPENSATION**

Address: Operational Base + offset (0x0108)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6:1 | RW | 0x00 | tdc_offset<br>Transmitter Delay Compensation Offset<br>This offset is specified in CAN clock cycles and is added to the measured transmitter delay to place the Secondary Sample Point (SSP) at appropriate position (for example, set this to half data bit time in terms of CAN clock cycles to place SSP in the middle of the data bit). |
| 0 | RW | 0x0 | tdc_enable<br>Transmitter Delay Compensation (TDC) Enable<br>1'b0: TDC is disabled<br>1'b1: Enables TDC function as specified in the CAN FD standard |

**CAN_TIMESTAMP_CTRL**

Address: Operational Base + offset (0x010C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6:1 | RW | 0x00 | time_base_counter_prescale<br>Time Base Counter Prescaler bit<br>0: TBC increments every 1 clock<br>1: TBC increments every 2 clocks<br>...<br>32: TBC increments every 32 clocks |
| 0 | RW | 0x0 | time_base_counter_enable<br>Time Base Counter (TBC) Enable<br>1'b0: Disable and reset TBC<br>1'b1: Enables TBC |

**CAN_TIMESTAMP**

Address: Operational Base + offset (0x0110)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | time_base_counter<br>This Status field gives running value of the timestamp counter. |

**CAN_TXEVENT_FIFO_CTRL**

Address: Operational Base + offset (0x0114)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:9 | RO | 0x000000 | reserved |
| 8:5 | RO | 0x0 | txe_fifo_cnt<br>TXE_FIFO_FRAME_CNT<br>This field represents number of frames in TXE FIFO |
| 4:1 | RW | 0x0 | txe_fifo_watermark<br>TX Event FIFO generates FULL interrupt based on the value programmed in this field.<br>Set it within (1-15) range.<br>The TX FIFO Full Watermark interrupt in the ISR register continues to assert as long as the TX Event FIFO Fill Level is above TX Event FIFO Full watermark. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | txe_fifo_enable<br>transmit event FIFO enable<br>1'b0: Disable<br>1'b1: Enable |

**CAN_RX_FIFO_CTRL**

Address: Operational Base + offset (0x0118)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x0000000 | reserved |
| 7:5 | RO | 0x0 | rx_fifo_cnt<br>RX_FIFO_FRAME_CNT<br>This field represents number of frames in Rx FIFO |
| 6 | RO | 0x0 | reserved |
| 3:1 | RW | 0x0 | rx_fifo_full_watermark<br>RX FIFO Full Watermark.<br>RX FIFO generates FULL interrupt based on the value programmed in this field.<br>Set it within (1-5) range.<br>The RX FIFO Full Watermark interrupt in the ISR register continues to assert as long as the RX FIFO-0 Fill Level is above RX FIFO Full watermark.<br>This field can be written to only when CEN bit in SRR is 0. |
| 0 | RW | 0x0 | rx_fifo_enable<br>receive FIFO enable bit<br>1'b0: Disable<br>1'b1: Enable |

**CAN_AFR_CTRL**

Address: Operational Base + offset (0x011C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4 | RW | 0x0 | UAF5<br>Enable the use of acceptance filter pair 5<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | UAF4<br>Enable the use of acceptance filter pair 4<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | UAF3<br>Enable the use of acceptance filter pair 3<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | UAF2<br>Enable the use of acceptance filter pair 2<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | UAF1<br>Enable the use of acceptance filter pair 1<br>1'b0: Disable<br>1'b1: Enable |

**CAN_IDCODE0**

Address: Operational Base + offset (0x0120)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:0 | RW | 0x00000000 | id_code<br>CAN controller ID code:<br>Standard frame ID: id_code[10:0];<br>Extended frame ID: id_code[28:0]. |

**CAN_IDMASK0**

Address: Operational Base + offset (0x0124)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:0 | RW | 0x00000000 | id_mask<br>ID mask for each bit of ID code<br>1'b0: Unmasked<br>1'b1: Masked |

**CAN_IDCODE1**

Address: Operational Base + offset (0x0128)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:0 | RW | 0x00000000 | id_code<br>CAN controller ID code:<br>Standard frame ID: id_code[10:0];<br>Extended frame ID: id_code[28:0]. |

**CAN_IDMASK1**

Address: Operational Base + offset (0x012C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:0 | RW | 0x00000000 | id_mask<br>ID mask for each bit of ID code<br>1'b0: Unmasked<br>1'b1: Masked |

**CAN_IDCODE2**

Address: Operational Base + offset (0x0130)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:0 | RW | 0x00000000 | id_code<br>CAN controller ID code:<br>Standard frame ID: id_code[10:0];<br>Extended frame ID: id_code[28:0]. |

**CAN_IDMASK2**

Address: Operational Base + offset (0x0134)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:0 | RW | 0x00000000 | id_mask<br>ID mask for each bit of ID code<br>1'b0: Unmasked<br>1'b1: Masked |

**CAN_IDCODE3**

Address: Operational Base + offset (0x0138)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:0 | RW | 0x00000000 | id_code<br>CAN controller ID code:<br>Standard frame ID: id_code[10:0];<br>Extended frame ID: id_code[28:0]. |

**CAN_IDMASK3**

Address: Operational Base + offset (0x013C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:0 | RW | 0x00000000 | id_mask<br>ID mask for each bit of ID code<br>1'b0: Unmasked<br>1'b1: Masked |

**CAN_IDCODE4**

Address: Operational Base + offset (0x0140)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:0 | RW | 0x00000000 | id_code<br>CAN controller ID code:<br>Standard frame ID: id_code[10:0];<br>Extended frame ID: id_code[28:0]. |

**CAN_IDMASK4**

Address: Operational Base + offset (0x0144)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:0 | RW | 0x00000000 | id_mask<br>ID mask for each bit of ID code<br>1'b0: Unmasked<br>1'b1: Masked |

**CAN_NEW_TXFRAMEINFO**

Address: Operational Base + offset (0x0200)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RW | 0x0 | txframe_format<br>1'b0: Standard frame<br>1'b1: Extended frame |
| 6 | RW | 0x0 | tx_rtr<br>1'b0: Data frame<br>1'b1: Remote frame |
| 5 | RW | 0x0 | reserved |
| 4 | RW | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RW | 0x0 | txdata_length<br>Transmit data length configure register. (unit: byte)<br>4'b0000: 0byte<br>4'b0001: 1byte<br>4'b0010: 2byte<br>4'b0011: 3byte<br>4'b0100: 4byte<br>4'b0101: 5byte<br>4'b0110: 6byte<br>4'b0111: 7byte<br>4'b1000: 8byte<br>4'b1001:12byte<br>4'b1010:16byte<br>4'b1011:20byte<br>4'b1100:24byte<br>4'b1101:32byte<br>4'b1110:48byte<br>4'b1111:64byte |

**CAN_NEW_TXID**

Address: Operational Base + offset (0x0204)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:0 | RW | 0x00000000 | tx_id<br>can_tx_id[28:0] |

**CAN_NEW_TXDATA0**

Address: Operational Base + offset (0x0208)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | tx_data0<br>tx_data0 |

**CAN_NEW_TXDATA1**

Address: Operational Base + offset (0x020C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | tx_data1<br>tx_data1 |

**CAN_NEW_RXFRAMEINFO**

Address: Operational Base + offset (0x0300)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RO | 0x0 | rxframe_format<br>1'b0: Standard frame<br>1'b1: Extended frame |
| 6 | RO | 0x0 | rx_rtr<br>1'b0: Data frame<br>1'b1: Remote frame |
| 5 | RO | 0x0 | reserved |
| 4 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RO | 0x0 | rxdata_length<br>Transmit data length configure register. (unit: byte)<br>4'b0000: 0byte<br>4'b0001: 1byte<br>4'b0010: 2byte<br>4'b0011: 3byte<br>4'b0100: 4byte<br>4'b0101: 5byte<br>4'b0110: 6byte<br>4'b0111: 7byte<br>4'b1000: 8byte<br>4'b1001:12byte<br>4'b1010:16byte<br>4'b1011:20byte<br>4'b1100:24byte<br>4'b1101:32byte<br>4'b1110:48byte<br>4'b1111:64byte |

**CAN_NEW_RXID**

Address: Operational Base + offset (0x0304)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:0 | RO | 0x00000000 | rx_id<br>can_rx_id[28:0] |

**CAN_RXTIMESTAMP**

Address: Operational Base + offset (0x0308)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | timestamp<br>rx_timestamp |

**CAN_NEW_RXDATA0**

Address: Operational Base + offset (0x030C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | rx_data0<br>rx_data0[31:0]<br>This register refresh after receiving the next frame. |

**CAN_NEW_RXDATA1**

Address: Operational Base + offset (0x0310)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | rx_data1<br>rx_data1[31:0]<br>This register refresh after receiving the next frame. |

**CAN_RX_FIFO_RDATA**

Address: Operational Base + offset (0x0400)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | rx_fifo_rdata<br>Receive FIFO read data value |

**CAN_TXE_FIFO_RDATA**

Address: Operational Base + offset (0x0500)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | txe_fifo_rdata<br>Transmit event FIFO read data value |

## 29.5 Interface Description

Table 29-3 CAN Interface Description

| Module Pin | Direction | Pad Name | IOMUX Setting |
|---|---|---|---|
| **CAN0mux0 Interface** | | | |
| can0_rx | I | I2S1_SCLK_RX_M1/PDM0_CLK0_M1/PWM1_M0/I2C2_SDA_M0/CAN0_RX_M0/SPI0_MOSI_M0/PCIE30X1_0_CLKREQN_M0/GPIO0_C0_d | BUS_IOC_GPIO0C_IOMUX_SEL_L[3:0]=4'hb |
| can0_tx | O | I2S1_LRCK_TX_M1/PWM0_M0/I2C2_SCL_M0/CAN0_TX_M0/SPI0_CS1_M0/PCIE30X1_1_PERSTN_M0/GPIO0_B7_d | BUS_IOC_GPIO0B_IOMUX_SEL_H[15:12]=4’hb |
| **CAN0mux1 Interface** | | | |
| can0_rx | I | SDMMC_CLK/PDM1_CLK0_M0/TEST_CLKOUT_M0/MCU_JTAG_TMS_M0/CAN0_RX_M1/UART5_TX_M0/GPIO4_D5_d | BUS_IOC_GPIO4D_IOMUX_SEL_H[7:4]=4'h9 |
| can0_tx | O | SDMMC_CMD/PDM1_CLK1_M0/MCU_JTAG_TCK_M0/CAN0_TX_M1/UART5_RX_M0/PWM7_IR_M1/GPIO4_D4_u | BUS_IOC_GPIO4D_IOMUX_SEL_H[3:0]=4'h9 |
| **CAN1mux0 Interface** | | | |
| can1_rx | I | GMAC1_TXEN/I2S2_SCLK_TX_M1/CAN1_RX_M0/UART3_TX_M1/PWM12_M0/GPIO3_B5_u | BUS_IOC_GPIO3B_IOMUX_SEL_H[7:4]=4'h9 |
| can1_tx | O | GMAC1_MCLKINOUT/I2S2_LRCK_TX_M1/CAN1_TX_M0/UART3_RX_M1/PWM13_M0/GPIO3_B6_d | BUS_IOC_GPIO3B_IOMUX_SEL_H[11:8]=4'h9 |
| **CAN1mux1 Interface** | | | |
| can1_rx | I | CIF_HREF/BT1120_D8/I2S1_SDO1_M0/PCIE30X1_1_BUTTON_RSTN/I2C7_SCL_M3/UART8_RTSN_M0/PWM14_M1/SPI0_CS0_M1/CAN1_RX_M1/GPIO4_B2_u | BUS_IOC_GPIO4B_IOMUX_SEL_L[11:8]=4'hc |
| can1_tx | O | CIF_VSYNC/BT1120_D9/I2S1_SDO2_M0/PCIE20X1_2_BUTTON_RSTN/I2C7_SDA_M3/UART8_CTSN_M0/PWM15_IR_M1/CAN1_TX_M1/GPIO4_B3_u | BUS_IOC_GPIO4B_IOMUX_SEL_L[15:12]=4'hc |
| **CAN2mux0 Interface** | | | |
| can2_rx | I | CIF_D8/FSPI_CS0N_M2/PCIE30X4_CLKREQN_M2/HDMI_TX1_CEC_M2/CAN2_RX_M0/UART5_TX_M1/SPI3_CS0_M3/GPIO3_C4_u | BUS_IOC_GPIO3C_IOMUX_SEL_H[3:0]=4'h9 |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| | | | |
|---|---|---|---|
| can2_tx | O | CIF_D9/FSPI_CS1N_M2/PCIE30X4_WAKEN_M2/HDMI_TX1_SDA_M1/CAN2_TX_M0/UART5_RX_M1/SPI3_CS1_M3/GPIO3_C5_u | BUS_IOC_GPIO3C_IOMUX_SEL_H[7:4]=4'h9 |
| **CAN2mux1 Interface** | | | |
| can2_rx | I | I2S1_SDO2_M1/PDM0_SDI2_M1/PWM3_IR_M0/I2C1_SCL_M2/CAN2_RX_M1/HDMI_TX0_SDA_M1/SPI3_CS0_M2/PCIE30X2_PERSTN_M0/SATA_CPDET/GPIO0_D4_u | BUS_IOC_GPIO0D_IOMUX_SEL_H[3:0]=4'ha |
| can2_tx | O | I2S1_SDO3_M1/CPU_BIG1_AVS/I2C1_SDA_M2/CAN2_TX_M1/HDMI_TX0_SCL_M1/SPI3_CS1_M2/SATA_MP_SWITCH/GPIO0_D5_u | BUS_IOC_GPIO0D_IOMUX_SEL_H[7:4]=4'ha |

## 29.6 Application Notes

### 29.6.1 Controller initialization flow

The controller must configure the registers after power-up or hardware reset. During the operation of the controller, a software reset request may be sent and reconfigured (re-initialized) as shown below.

After the initialization is completed, the controller enters the working mode, sends the frame to be sent to the buffer, and then sets the "send request" flag of the command register to start transmitting.

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

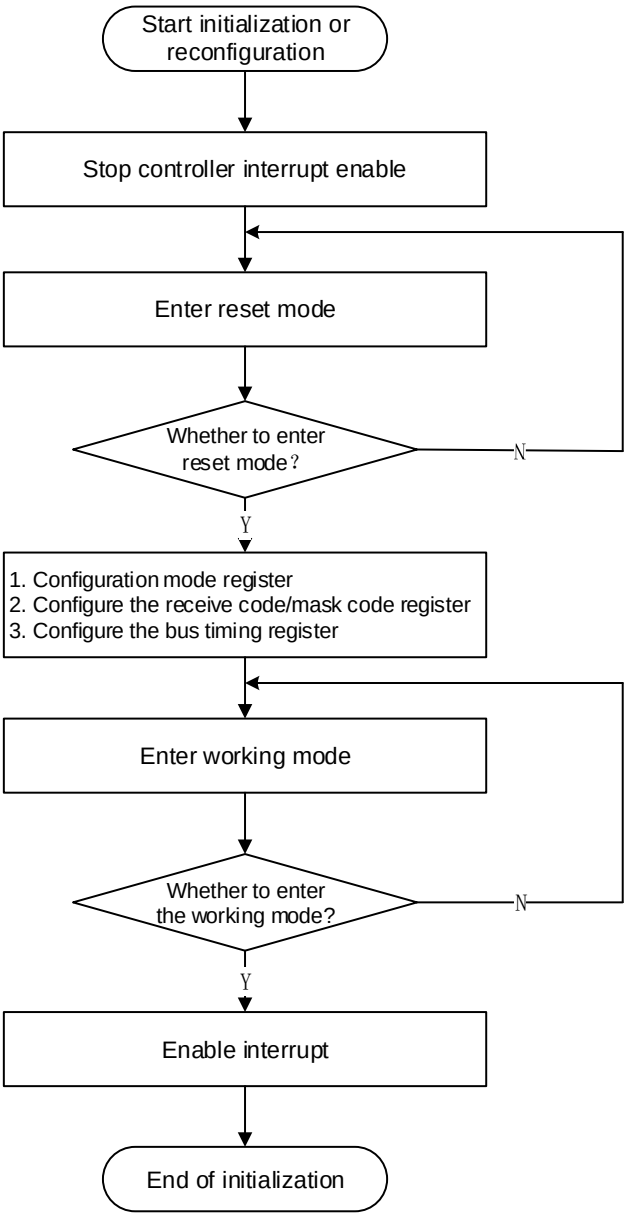



Fig 1-1 CAN Initialization Flow

## 29.6.2 Loop-back Mode

The controller must configure the registers after power-up or hardware reset. During the operation of the controller, a software reset request may be sent and reconfigured (re-initialized) as shown below.

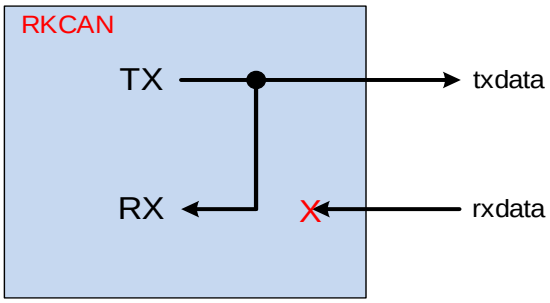



Fig 1-2 Loopback Mode

## 29.6.3 Silent Mode

The controller must configure the registers after power-up or hardware reset. During the operation of the controller, a software reset request may be sent and reconfigured (re-initialized) as shown below.

Copyright 2022 © Rockchip Electronics Co., Ltd.

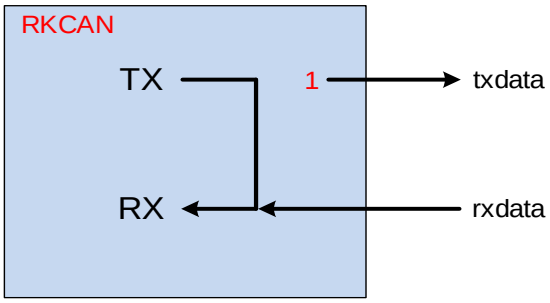



Fig 1-3 Silent Mode

### 29.6.4 Rxstx Mode

- 1'b0: RKCAN cannot receive the data sent by itself;
- 1'b1: RKCAN can receive the data sent by itself, and when the ID of the frame is the same as the ID_CODE of RKCAN itself, RKCAN will store the frame information into CAN_RXDATA1/2.

### 29.6.5 Txorder Mode

The Txorder Mode is used to determine the order in which data is sent.

- 1'b0: Data transmission order is "tx_data1[7:0] --> tx_data1[15:8] --> tx_data1[23:16] --> tx_data1[31:24] -->tx_data2[7:0] --> tx_data2[15:8] --> tx_data2[23:16] --> tx_data2[31:24]";
- 1'b1: Data transmission order is "tx_data2[31:0] --> tx_data1[31:0]".

### 29.6.6 Rxsort Mode

The Rxsort Mode is used to determine how the received data is stored.

- 1'b0: The data received first is placed in the lower address;
- 1'b1: The data received first moves to the upper address, and the data received later is placed at the lower address.

### 29.6.7 Cover Mode

- 1'b0: RKCAN can't receive new frame before receive registers cleared.
- 1'b1: RKCAN can receive new frame before receive registers cleared, and new RXDATA will cover old RXDATA.

### 29.6.8 Overload Mode

According to the CAN protocol, a CAN transceiver will generate an OVERLOAD frame in three cases:

- When the CAN is used as a receiver, if it is necessary to delay the next frame.
- Detection of a dominant bit at the first and second bit of Intermission.
- If an CAN node samples a dominant bit at the eight bits (the last bit) of an ERROR DELIMITER or OVERLOAD DELIMITER.
  1'b0: Overload Lite Mode: RKCAN only generates overload frames in the CASE2.
  1'b1: Overload Extended Mode: RKCAN can generates overload frames in all three cases.

### 29.6.9 Auto Retx Mode

Auto Retransmission Mode.

- 1'b0: Disable. RKCAN return to idle state after transmit DATA/RTR frame failed, and set tx_req to 0.
- 1'b1: Enable. The RKCAN automatically retransmit frames which have lost arbitration or have been disturbed by errors during transmission.

### 29.6.10 Auto Bus On

Auto Bus on Enable.

- 1'b0: After the RKCAN has entered bus_off state, the software can start a bus-off recovery sequence by resetting the work_mode to 0.
- 1'b1: Automatic reset TEC/REC to bus_on after 128 occurrences of 11 consecutive recessive bits have been monitored on the bus.

### 29.6.11 Sleep Mode

The core enters Sleep mode from Configuration or Normal mode when the SLEEP bit is 1 in the CAN_MODE register, the CAN bus is idle, and there are no pending transmission

Copyright 2022 © Rockchip Electronics Co., Ltd.

requests.
The core enters Configuration mode when any configuration condition is satisfied. The core enters Normal mode (clearing the SLEEP request bit in the sleep register and also clearing the corresponding status bit) under the following (wake-up) conditions:

- Whenever the SLEEP bit is set to 0.
- Whenever the SLEEP bit is 1, and bus activity is detected.
- Whenever there is a new message for transmission.

Interrupts are generated when the core enters Sleep mode or wakes up from Sleep mode.

### 29.6.12 DMA Support

The CAN supports DMA signaling with the use of two output signals (dma_tx_mode and dma_rx_mode) to indicate when transmit buffer is empty or when the receive FIFO is full. The controller uses two DMA channels, one for the transmit data and one for the receive data.
DMA transmit and receive support enabled by setting corresponding bit in CAN_DMA_CTRL register. Once enabled whenever both transmit buffer is empty dma_tx_mode is set, DMA should write transmit message. At last CPU set transmit request bit to initiate CAN.

- If RX FIFO is disabled, dma_rx_mode is set when message received successfully, DMA should read RXDATA from receive registers.
- If RX FIFO is enabled, dma_rx_mode is set when message received and FIFO reached watermark，DMA should read RXDATA from Rx FIFO entrance.

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

# Chapter 30 Flexible Serial Peripheral Interface (FSPI )

## 30.1 Overview

The FSPI is a flexible serial peripheral interface host controller to interface with external device.

The FSPI supports the following features:

- Support various vendor devices with flexible command sequencer engine
  - Serial NOR Flash
  - Serial NAND Flash
  - Serial pSRAM
  - Serial SRAM
- Support SDR mode
- Support Single/Dual/Quad IO mode
- Support a 32-bit AHB slave to read and write controller register bank and initiate command sequence, including transfer data from/to external device indirectly
- Support a 32-bit AHB master with embedded DMA engine to transfer data from/to external device indirectly
- Support independent clock for system bus HCLK and controller core SCLK
- Support maskable interrupts generation
- Support sampling clock with optionally configurable delay line
- Support 2 CS# operation

## 30.2 Block Diagram

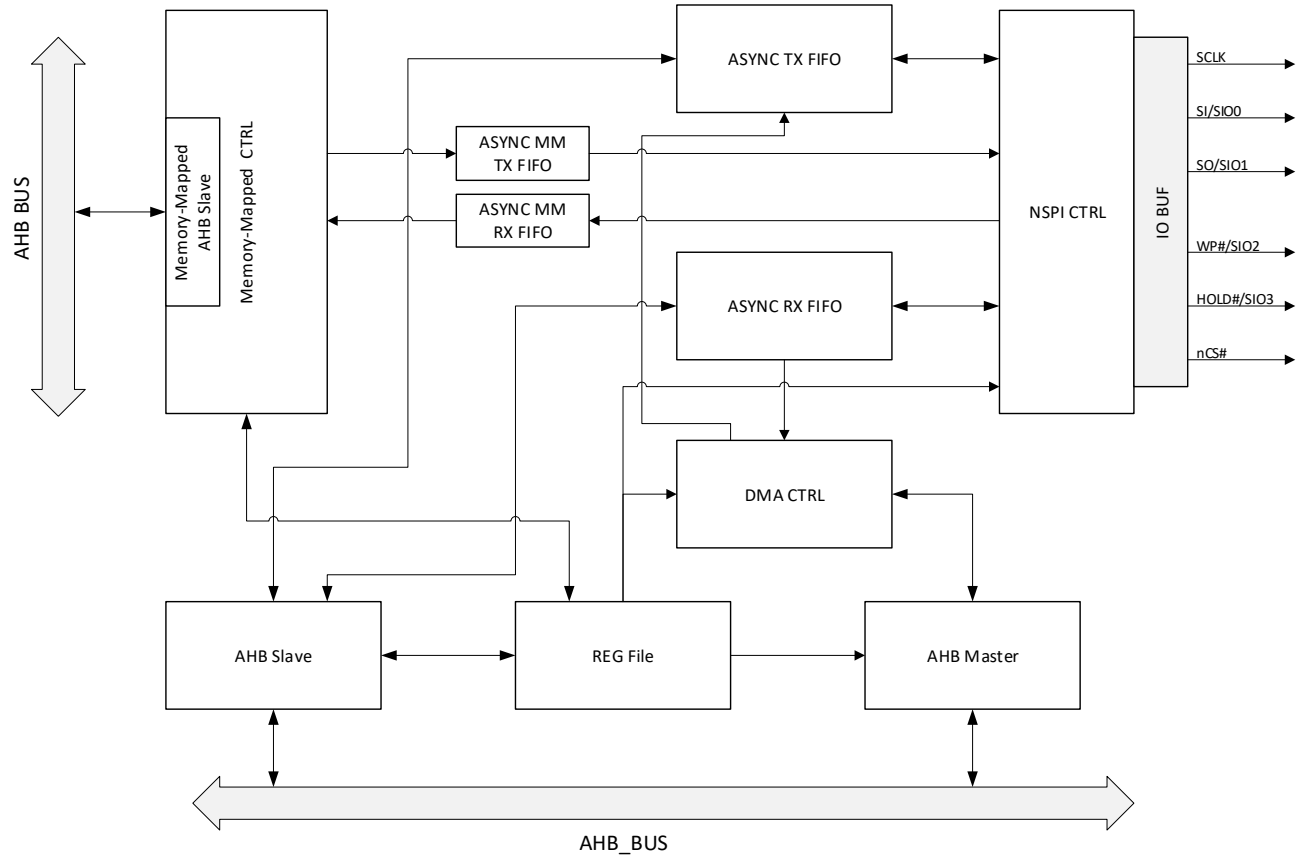



Fig. 30-1 FSPI Architecture

Memory-Mapped AHB slave is available when XIP feature is present. In current chip, this feature is not provided.

## 30.3 Function Description

### 30.3.1 AHB Slave

The AHB slave block is used to configure the register of controller to generate flexible

command sequence, process the interrupt exception, target various device feature and AC timing specification. It is also used to write CMD/ADDR/DATA to TX FIFO and read DATA from RX FIFO which buffer the DATA from external device.

### 30.3.2 AHB Master

When the embedded DMA CTRL is used to transfer DATA, the AHB master is used to transfer data to other system region, such as internal SRAM, peripheral, external DRAM.

### 30.3.3 Memory-Mapped AHB Slave

After the software initialize the controller based on the specialized memory device, CPU and other system bus masters can read data from external memory directly. If the external memory is SRAM or pSRAM, it also supports write data to it. The Memory-Mapped AHB Slave module can generate the relative CS# based on the access address from system address, example CS#0 and CS#1. Non-Supported in this chip.

### 30.3.4 REG File

The REG File is configurable register bank to control the store the static configuration and dynamic status of controller.

### 30.3.5 DMA CTRL

A block takes responsible for splitting a long length transfer trans into AHB bus transaction and interfacing with ASYNC TX or RX FIFO.

### 30.3.6 FIFO

There are four FIFO in the FSPI controller. ASYNC TX FIFO and ASYNC RX FIFO is for normal transaction that initiated by command sequence driver. The ASYNC MM (Memory-Mapped) TX FIFO and ASYNC MM (Memory-Mapped) RX FIFO is only used to buffer DATA from or to external device initiated by system bus master directly.

### 30.3.7 NSPI CTRL

Sequence decode engine which generates specialized timing sequence for various device. The NSPI decode the transaction from TX FIFO and Memory-Mapped Controller and convert it to relative CMD/ADDR/DATA frame based on the configuration.

## 30.4 Register Description

### 30.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 30-1 FSPI Address Mapping Table

| Name | Address Base | Size |
|---|---|---|
| FSPI CFG | 0xFE2B0000 | 0x10000(64KB) |

### 30.4.2 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| FSPI_CTRL0 | 0x0000 | W | 0x00000000 | Control Register for CS0 Device |
| FSPI_IMR | 0x0004 | W | 0x000001FF | Interrupt Mask Register |
| FSPI_ICLR | 0x0008 | W | 0x00000000 | Interrupt Clear Register |
| FSPI_FTLR | 0x000C | W | 0x00001010 | FIFO Threshold Level Register |
| FSPI_RCVR | 0x0010 | W | 0x00000000 | FSPI Recover Register |
| FSPI_AX0 | 0x0014 | W | 0x00000000 | FSPI Auxiliary Data Value for CS0 Device |
| FSPI_ABIT0 | 0x0018 | W | 0x00000000 | Extend Address Bits for CS0 Device |
| FSPI_ISR | 0x001C | W | 0x00000000 | Interrupt Status |
| FSPI_FSR | 0x0020 | W | 0x00000001 | FIFO Status Register |
| FSPI_SR | 0x0024 | W | 0x00000000 | FSPI Status Register |
| FSPI_RISR | 0x0028 | W | 0x00000000 | Raw Interrupt Status Register |
| FSPI_VER | 0x002C | W | 0x00000004 | Version Register |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| FSPI_QOP | 0x0030 | W | 0x00000000 | Quad Line Operation IO Level Pre-set Register |
| FSPI_EXT_CTRL | 0x0034 | W | 0x00004023 | Extend Control Register |
| FSPI_DLL_CTRL0 | 0x003C | W | 0x00000001 | Delay Line Control Register for CS0 Device |
| FSPI_EXT_AX | 0x0044 | W | 0x0000F0FF | Extend Auxiliary Data Control Register |
| FSPI_SCLK_INATM_CNT | 0x0048 | W | 0xFFFFFFFF | SCLK Inactive Timeout Counter |
| FSPI_XMMC_WCMD0 | 0x0050 | W | 0x00000000 | Memory Mapped Control Write Command Register for CS0 Device |
| FSPI_XMMC_RCMD0 | 0x0054 | W | 0x00000000 | Memory Mapped Control Read Command Register for CS0 Device |
| FSPI_XMMC_CTRL | 0x0058 | W | 0x000072E0 | Memory Mapped Control Register |
| FSPI_MODE | 0x005C | W | 0x00000000 | Controller Working Mode Register |
| FSPI_DEVRGN | 0x0060 | W | 0x00000017 | Device Region Size Register |
| FSPI_DEVSIZE0 | 0x0064 | W | 0x00000012 | Device Size Register for CS0 Device |
| FSPI_TME0 | 0x0068 | W | 0x00000000 | Timeout Enable Control Register for CS0 Device |
| FSPI_XMMC_RX_WTMRK | 0x0070 | W | 0x00000002 | Memory Mapped Mode Receiver FIFO Water Mark Register |
| FSPI_DMATR | 0x0080 | W | 0x00000000 | DMA Trigger Register |
| FSPI_DMAADDR | 0x0084 | W | 0x00000000 | DMA Address Register |
| FSPI_LEN_CTRL | 0x0088 | W | 0x00000000 | Length Control Register |
| FSPI_LEN_EXT | 0x008C | W | 0x00000000 | Length Extended Register |
| FSPI_XMMCSR | 0x0094 | W | 0x00000000 | Memory Mapped Status Register |
| FSPI_CMD | 0x0100 | W | 0x00000000 | Indirect Command Register |
| FSPI_ADDR | 0x0104 | W | 0x00000000 | Address Register |
| FSPI_DATA | 0x0108 | W | 0x00000000 | Data Register |
| FSPI_CTRL1 | 0x0200 | W | 0x00000000 | Control Register for CS1 Device |
| FSPI_AX1 | 0x0214 | W | 0x00000000 | FSPI Auxiliary Data Value for CS1 Device |
| FSPI_ABIT1 | 0x0218 | W | 0x00000000 | Extend Address Bits for CS1 Device |
| FSPI_DLL_CTRL1 | 0x023C | W | 0x00000001 | Delay Line Control Register for CS1 Device |
| FSPI_XMMC_WCMD1 | 0x0250 | W | 0x00000000 | Memory Mapped Control Write Command Register for CS1 Device |
| FSPI_XMMC_RCMD1 | 0x0254 | W | 0x00000000 | Memory-Mapped Command Control Register for CS1 Device |
| FSPI_DEVSIZE1 | 0x0264 | W | 0x00000012 | Device Size Register for CS1 Device |
| FSPI_TME1 | 0x0268 | W | 0x00000000 | Timeout Enable Control Register for CS1 Device |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

### 30.4.3 Detail Registers Description

**FSPI_CTRL0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RO | 0x00000 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:12 | RW | 0x0 | DATB<br>Data Line Width<br>2'b00: 1 bit, x1 mode<br>2'b01: 2 bits, x2 mode<br>2'b10: 4 bits, x4 mode<br>2'b11: Reserved<br>Set this DATB to match the CMD sequence before doing indirect access mode and memory mapped access mode. |
| 11:10 | RW | 0x0 | ADRB<br>Address Line Width<br>2'b00: 1 bit, x1 mode<br>2'b01: 2 bits, x2 mode<br>2'b10: 4 bits, x4 mode<br>2'b11: Reserved<br>Set this ADRB to match the CMD sequence before doing indirect access mode and memory mapped access mode. |
| 9:8 | RW | 0x0 | CMDB<br>Command Line Width<br>2'b00: 1 bit, x1 mode<br>2'b01: 2 bits, x2 mode<br>2'b10: 4 bits, x4 mode<br>2'b11: Reserved<br>Set this CMDB to match the CMD sequence before doing indirect access mode and memory mapped access mode. |
| 7:4 | RW | 0x0 | IDLE_CYCLE<br>Idle Cycles When Switching IO from Output to Input<br>4'h0: Idle hold is disable<br>4'h1: Hold the SCLK in idle for 2 cycles when switch to shift in<br>...<br>4'hf: Hold the SCLK in idle for 16 cycles when switch to shift in<br>To improve the transform IO timing, the application can set this register to hold the SCLK in low state or high state. |
| 3:2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | SHIFTPHASE<br>Shift Phase of Data Input in Controller<br>1'b0: Shift input data at posedge SCLK<br>1'b1: Shift input data at negedge SCLK<br>The application can select the input data captured by posedge of SCLK when "0" or negedge of SCLK when "1". |
| 0 | RW | 0x0 | SPIM<br>Serial Peripheral Interface Mode<br>1'b0: Mode 0<br>1'b1: Mode 3<br>SPIM is used to control the serial mode (CPOL and CPHA). CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported. |

**FSPI_IMR**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x1 | DMAM<br>DMA Finish Interrupt Mask<br>1'b0: DMA finish interrupt is not masked<br>1'b1: DMA finish interrupt is masked<br>Only valid in indirect access mode. |
| 6 | RW | 0x1 | NSPIM<br>NSPI Interrupt Mask<br>1'b0: NSPI interrupt is not masked<br>1'b1: NSPI interrupt is masked<br>Valid in indirect access mode and memory mapped mode. |
| 5 | RW | 0x1 | AHBM<br>AMBA AHB Error Interrupt Mask<br>1'b0: AMBA AHB Error interrupt is not masked<br>1'b1: AMBA AHB Error interrupt is masked<br>Only valid in indirect access mode. |
| 4 | RW | 0x1 | TRANSM<br>Transfer Finish Interrupt Mask<br>1'b0: Transfer finish interrupt is not masked<br>1'b1: Transfer finish interrupt is masked<br>Only valid in indirect access mode. |
| 3 | RW | 0x1 | TXEM<br>Transmit FIFO Empty Interrupt Mask<br>1'b0: Transmit FIFO empty interrupt is not masked<br>1'b1: Transmit FIFO empty interrupt is masked<br>Only valid in indirect access mode. |
| 2 | RW | 0x1 | TXOM<br>Transmit FIFO Overflow Interrupt Mask<br>1'b0: Transmit FIFO overflow interrupt is not masked<br>1'b1: Transmit FIFO overflow interrupt is masked<br>Only valid in indirect access mode. |
| 1 | RW | 0x1 | RXUM<br>Receive FIFO Underflow Interrupt Mask<br>1'b0: Receive FIFO underflow interrupt is not masked<br>1'b1: Receive FIFO underflow interrupt is masked<br>Only valid in indirect access mode. |
| 0 | RW | 0x1 | RXFM<br>Receive FIFO Full Interrupt Mask<br>1'b0: Receive FIFO full interrupt is not masked<br>1'b1: Receive FIFO full interrupt is masked<br>Only valid in indirect access mode. |

**FSPI_ICLR**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | W1C | 0x0 | DMAC<br>DMA Finish Interrupt Clear<br>1'b0: No action<br>1'b1: Clear interrupt<br>Write "1" to clear the DMAS |
| 6 | W1C | 0x0 | NSPIC<br>NSPI Error Interrupt Clear<br>1'b0: No action<br>1'b1: Clear interrupt<br>Write "1" to clear the NSPIS. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | W1C | 0x0 | AHBC<br>AMBA AHB Error Interrupt Clear<br>1'b0: No action<br>1'b1: Clear interrupt<br>Write "1" to clear the AHBS. |
| 4 | W1C | 0x0 | TRANSC<br>Transfer Finish Interrupt Clear<br>1'b0: No action<br>1'b1: Clear interrupt<br>Write "1" to clear the TRANSS. |
| 3 | W1C | 0x0 | TXEC<br>Transmit FIFO Empty Interrupt Clear<br>1'b0: No action<br>1'b1: Clear interrupt<br>Write "1" to clear the TXES. |
| 2 | W1C | 0x0 | TXOC<br>Transmit FIFO Overflow Interrupt Clear<br>1'b0: No action<br>1'b1: Clear interrupt<br>Write "1" to clear the TXOS. |
| 1 | W1C | 0x0 | RXUC<br>Receive FIFO Underflow Interrupt Clear<br>1'b0: No action<br>1'b1: Clear interrupt<br>Write "1" to clear the RXUS. |
| 0 | W1C | 0x0 | RXFC<br>Receive FIFO Full Interrupt Clear<br>1'b0: No action<br>1'b1: Clear interrupt<br>Write "1" to clear the RXFS. |

**FSPI_FTLR**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:8 | RW | 0x10 | RXFTLR<br>Receive FIFO Threshold Level<br>8'h0: 0 entry level<br>8'h1: 1 entry level<br>...<br>8'h10: 16 entry level(default)<br>...<br>When the number of receive FIFO entries is bigger than or equal to this value, the receive FIFO full interrupt is triggered. |
| 7:0 | RW | 0x10 | TXFTLR<br>Transmit FIFO Threshold Level<br>8'h0: 0 entry level<br>8'h1: 1 entry level<br>...<br>8'h10: 16 entry level(default)<br>...<br>When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered. |

**FSPI_RCVR**

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | R/WSC | 0x0 | RCVR<br>FSPI Recover<br>Write any values to trigger the recovery of SMC NSPI state machine, FIFO state and other logic state. |

**FSPI_AX0**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | AX<br>Auxiliary Data<br>The AX value when doing the continuous read (enhance mode or XIP mode). That is M7-M0 in "Continuous Read Mode". |

**FSPI_ABIT0**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4:0 | RW | 0x00 | ABIT<br>Address Bits Extend<br>5'h0: 1 bit<br>5'h1: 2 bits<br>...<br>5'h1f: 32 bits<br>Only valid when ADDRB is set to 2'b11. |

**FSPI_ISR**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RO | 0x0 | DMAS<br>DMA Finish Interrupt Status<br>1'b0: No interrupt<br>1'b1: Active interrupt generated |
| 6 | RO | 0x0 | NSPIS<br>NSPI Transaction Decode Error Interrupt Status<br>1'b0: No interrupt<br>1'b1: Active interrupt generated |
| 5 | RO | 0x0 | AHBS<br>AMBA AHB Error Interrupt Status<br>1'b0: No interrupt<br>1'b1: Active interrupt generated |
| 4 | RO | 0x0 | TRANSS<br>Transfer Finish Interrupt Status<br>1'b0: No interrupt<br>1'b1: Active interrupt generated |
| 3 | RO | 0x0 | TXES<br>Transmit FIFO Empty Interrupt Status<br>1'b0: No interrupt<br>1'b1: Active interrupt generated |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RO | 0x0 | TXOS<br>Transmit FIFO Overflow Interrupt Status<br>1'b0: No interrupt<br>1'b1: Active interrupt generated |
| 1 | RO | 0x0 | RXUS<br>Receive FIFO Underflow Interrupt Status<br>1'b0: No interrupt<br>1'b1: Active interrupt generated |
| 0 | RW | 0x0 | RXFS<br>Receive FIFO Full Interrupt Status<br>1'b0: No interrupt<br>1'b1: Active interrupt generated |

**FSPI_FSR**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:21 | RO | 0x000 | reserved |
| 20:16 | RW | 0x00 | RXWLVL<br>RX FIFO Water Level<br>5'h0: FIFO is empty<br>5'h1: 1 entry is taken<br>...<br>5'h10: 16 entry is taken, FIFO is full |
| 15:13 | RO | 0x0 | reserved |
| 12:8 | RO | 0x00 | TXWLVL<br>TX FIFO Water Level<br>5'h0: FIFO is full<br>5'h1: 1 entry is left<br>...<br>5'h10: 16 entry is left, FIFO is empty |
| 7:4 | RO | 0x0 | reserved |
| 3 | RO | 0x0 | RXFS<br>Receive FIFO Full Status<br>1'b0: RX FIFO is not full<br>1'b1: RX FIFO is full |
| 2 | RO | 0x0 | RXES<br>Receive FIFO Empty Status<br>1'b0: RX FIFO is not empty<br>1'b1: RX FIFO is empty |
| 1 | RO | 0x0 | TXES<br>Transmit FIFO Empty Status<br>1'b0: TX FIFO is not empty<br>1'b1: TX FIFO is empty |
| 0 | RO | 0x1 | TXFS<br>Transmit FIFO Full Status<br>1'b0: TX FIFO is not full<br>1'b1: TX FIFO is full |

**FSPI_SR**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RO | 0x0 | SR<br>Status Register<br>1'b0: NSPI Controller is idle<br>1'b1: NSPI Controller is busy<br>When controller is busy, don't change the setting of control register. When NSPI is idle, the software can initiate new transaction to external device. |

**FSPI_RISR**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RO | 0x0 | DMAS<br>DMA Finish Interrupt Status<br>1'b0: No active raw interrupt<br>1'b1: Active raw interrupt is generated<br>Cleared by writing corresponding ICLR bit to clear raw interrupt status. |
| 6 | RO | 0x0 | NSPIS<br>NSPI Error Interrupt Status<br>1'b0: No active raw interrupt<br>1'b1: Active raw interrupt is generated<br>Cleared by writing corresponding ICLR bit to clear raw interrupt status. |
| 5 | RO | 0x0 | AHBS<br>AMBA AHB Error Interrupt Status<br>1'b0: No active raw interrupt<br>1'b1: Active raw interrupt is generated<br>Cleared by writing corresponding ICLR bit to clear raw interrupt status. |
| 4 | RO | 0x0 | TRANSS<br>Transfer Finish Interrupt Status<br>1'b0: No active raw interrupt<br>1'b1: Active raw interrupt is generated<br>Cleared by writing corresponding ICLR bit to clear raw interrupt status. |
| 3 | RO | 0x0 | TXES<br>Transmit FIFO Empty Interrupt Status<br>1'b0: No active raw interrupt<br>1'b1: Active raw interrupt is generated<br>Cleared by writing corresponding ICLR bit to clear raw interrupt status. |
| 2 | RO | 0x0 | TXOS<br>Transmit FIFO Overflow Interrupt Status<br>1'b0: No active raw interrupt<br>1'b1: Active raw interrupt is generated<br>Cleared by writing corresponding ICLR bit to clear raw interrupt status. |
| 1 | RO | 0x0 | RXUS<br>Receive FIFO Underflow Interrupt Status<br>1'b0: No active raw interrupt<br>1'b1: Active raw interrupt is generated<br>Cleared by writing corresponding ICLR bit to clear raw interrupt status. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RO | 0x0 | RXFS<br>Receive FIFO Full Interrupt Status<br>1'b0: No active raw interrupt<br>1'b1: Active raw interrupt is generated<br>Cleared by writing corresponding ICLR bit to clear raw interrupt status. |

**FSPI_VER**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RO | 0x0005 | VER<br>The Version ID of FSPI |

**FSPI_QOP**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | SO123BP<br>SO123 Bypass Mode<br>1'b0: Disable bypass<br>1'b1: Enable bypass<br>Default is enabled. |
| 0 | RW | 0x0 | SO123<br>D1/D2/D3 Data Value During Inactive When CS is Active<br>1'b0: Set to "0"<br>1'b1: Set to "1"<br>The value of SO1, SO2 and SO3 during command and address bits input. |

**FSPI_EXT_CTRL**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:15 | RO | 0x00000 | reserved |
| 14 | RW | 0x1 | SR_GEN_MODE<br>Status Register Generation Mode<br>1'b0: Compatible mode with old controller<br>1'b1: Robust generation to indicates the status of controller<br>If set to "1", the controller will only clear the SR bit after operation sequence done and CS is high. |
| 13 | RW | 0x0 | TRANS_INT_MODE<br>Transmit Done Interrupt Generation Mode<br>1'b0: Trigger NSPI end in data done<br>1'b1: Trigger NSPI end in CS inactive<br>Default Generation is compatible with old controller. |
| 12 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:8 | RW | 0x0 | SWITCH_IO_O2I_CNT<br>Switch IO Attribute Cycles in O2I Idle Phase<br>4'h0: 1st cycle<br>4'h1: 2nd cycle<br>4'h2: 3rd cycle<br>4'h3: 4th cycle<br>...<br>4'hf: 16th cycle<br>The target cycle when switching from output to input in O2I idle phase. |
| 7:4 | RW | 0x2 | SWITCH_IO_DUMM_CNT<br>Switch IO Attribute Cycles in Dummy Phase<br>4'h0: 1st cycle<br>4'h1: 2nd cycle<br>4'h2: 3rd cycle<br>4'h3: 4th cycle<br>...<br>4'hf: 16th cycle<br>The target cycle when switching from output to input in Dummy data phase. |
| 3:0 | RW | 0x3 | CS_DESEL_CTRL<br>CS Inactive Control<br>4'h0: 1 cycle<br>4'h1: 2 cycles<br>4'h2: 3 cycles<br>4'h3: 4 cycles<br>...<br>4'hf: 16 cycles<br>The target cycles to hold CS inactive after de-assert the CS.<br>Default value are 4 SCLK cycles that is enough for normal device. |

**FSPI_DLL_CTRL0**

Address: Operational Base + offset (0x003C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15 | RW | 0x0 | SCLK_SMP_SEL<br>SCLK Sampling Selection<br>1'b0: Bypass DLL<br>1'b1: From DLL<br>The sampling SCLK source selection. |
| 14:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x001 | SMP_DLL_CFG<br>Sample Delay Line Configuration<br>9'h0: 1 DLL element cell<br>9'h1: 1 DLL element cell<br>9'h2: 2 DLL element cells<br>...<br>9'h1ff: 511 DLL element cells<br>This register to control the sampling delay line cell used. The maximum DLL element cells is decided by process. |

**FSPI_EXT_AX**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:8 | RW | 0xf0 | AX_SETUP_PAT<br>Auxiliary Setup Data Pattern<br>The AX data pattern that setup the continuous/enhance/XIP read mode |
| 7:0 | RW | 0xff | AX_CANCEL_PAT<br>Auxiliary Cancel Data Pattern<br>The AX data pattern that cancel the continuous/enhance/XIP read mode. |

**FSPI_SCLK_INATM_CNT**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0xffffffff | SCLK_INATM_CNT<br>SCLK Inactive Timeout Counter<br>When CS is active and SCLK is hold in high or low due to TX FIFO is empty or RX FIFO is full, if SCLK_INATM_EN is enabled, and timeout occurs, the controller will go back to idle and RX FIFO is flushed. |

**FSPI_XMMC_WCMD0**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:14 | WO | 0x0 | ADDRB<br>Address Bits<br>2'b00: 0 bit<br>2'b01: 24 bits<br>2'b10: 32 bits<br>2'b11: From the ABIT register<br>Address bits number select in memory mapped mode, if there is not address command to send, set to zero. |
| 13 | WO | 0x0 | CONT<br>Continuous<br>1'b0: Disable continuous mode<br>1'b1: Enable continuous mode<br>AX mode or Continuous mode or XIP mode for device which begins with address. |
| 12 | RO | 0x0 | reserved |
| 11:8 | WO | 0x0 | DUMM<br>Dummy Cycles<br>4'h0: No dummy cycle<br>...<br>4'h8: 8 cycles<br>...<br>Dummy bit cycles in memory mapped mode. |
| 7:0 | WO | 0x00 | CMD<br>Command<br>Command data in memory mapped access mode. |

**FSPI_XMMC_RCMD0**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:14 | WO | 0x0 | ADDRB<br>Address Bits<br>2'b00: 0 bit<br>2'b01: 24 bits<br>2'b10: 32 bits<br>2'b11: From the ABIT register<br>Address bits number select in memory mapped mode, if there is not address command to send, set to zero. |
| 13 | WO | 0x0 | CONT<br>Continuous<br>1'b0: Disable continuous mode<br>1'b1: Enable continuous mode<br>AX mode or Continuous mode or XIP mode for device which begins with address. |
| 12 | RO | 0x0 | reserved |
| 11:8 | WO | 0x0 | DUMM<br>Dummy Cycles<br>4'h0: No dummy cycle<br>...<br>4'h8: 8 cycles<br>...<br>Dummy bit cycles in memory mapped mode. |
| 7:0 | WO | 0x00 | CMD<br>Command<br>Command data in memory mapped access mode. |

**FSPI_XMMC_CTRL**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0 | reserved |
| 6 | RW | 0x1 | PFT_EN<br>Prefetch Enable<br>1'b0: Disable<br>1'b1: Enable<br>Should disable prefetch if controller communicate with pSRAM which need refresh. |
| 5 | RW | 0x1 | DEV_HWEN<br>Device AMBA AHB HWRITE Enable<br>1'b0: Disable<br>1'b1: Enable |
| 4:0 | RO | 0x00 | reserved |

**FSPI_MODE**

Address: Operational Base + offset (0x005C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | XMMC_MODE_EN<br>Memory Mapped Mode Enable<br>1'b0: Disable, indirect access mode<br>1'b1: Enable, Memory-Mapped mode<br>Before switching from indirect access mode to Memory-Mapped mode, the application should make sure the controller is in idle state and no pending transaction. If switch from Memory-Mapped to indirect access mode, software should initiate a dummy read by CPU before that. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**FSPI_DEVRGN**

Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9:8 | RW | 0x0 | DEC_CTRL<br>Decode Control<br>2'b00: 1 CS#<br>2'b01: 2 CS#<br>2'b10: 4 CS#<br>2'b11: Reserved<br>Only valid in XMMC mode. |
| 7:5 | RO | 0x0 | reserved |
| 4:0 | RW | 0x17 | RSIZE<br>Region Size<br>5'd0: 1 byte<br>5'd1: 2 bytes<br>5'd2: 4 bytes<br>.....<br>5'd10: 1K bytes<br>.....<br>5'd20: 1M bytes<br>.....<br>5'd31: 4G bytes<br>In Memory-Mapped mode, the CS is controlled by AHB address bus, region size is used to generate CS. |

**FSPI_DEVSIZE0**

Address: Operational Base + offset (0x0064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4:0 | RW | 0x12 | DSIZE<br>Device Size<br>5'd0: 1 byte<br>5'd1: 2 bytes<br>5'd2: 4 bytes<br>.....<br>5'd10: 1K bytes<br>.....<br>5'd20: 1M bytes<br>.....<br>5'd31: 4G byte<br>Device size is used to generate slop over status. |

**FSPI_TME0**

Address: Operational Base + offset (0x0068)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | SCLK_INATM_EN<br>SCLK Inactive Timeout Enable<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RO | 0x0 | reserved |

**FSPI_XMMC_RX_WTMRK**

Address: Operational Base + offset (0x0070)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x02 | RX_FULL_WTMRK<br>Memory Mapped Mode Receiver FIFO Water Mark.<br>Default is enough. |

**FSPI_DMATR**

Address: Operational Base + offset (0x0080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | W1C | 0x0 | DMATR<br>DMA Trigger<br>Write "1" to start the DMA transfer. |

**FSPI_DMAADDR**

Address: Operational Base + offset (0x0084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | DMAADDR<br>DMA Address<br>The destination or source data address in current system. |

**FSPI_LEN_CTRL**

Address: Operational Base + offset (0x0088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | TRB_SEL<br>Total Transfer Bytes Selection<br>1'b0: TRB controlled by CMD[TRB]<br>1'b1: TRB controlled by LEN_EXT |

**FSPI_LEN_EXT**

Address: Operational Base + offset (0x008C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | TRB_EXT<br>Total Transfer Bytes Extended<br>32'd0: No data<br>32'd1: 1 Byte<br>32'd2: 2 Bytes<br>...<br>Total data bytes number that will write to /read from the device. |

**FSPI_XMMCSR**

Address: Operational Base + offset (0x0094)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | R/WSC | 0x0 | SLOPOVER1<br>Slop Over Register for CS1<br>1'b0: Normal state<br>1'b1: Address slop over<br>When the access address in memory map mode is bigger than DEVSIZE, this bit will be set. Write "1" to clear this bit. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | R/W SC | 0x0 | SLOPOVER0<br>Slop Over Register for CS0<br>1'b0: Normal state<br>1'b1: Address slop over<br>When the access address in memory map mode is bigger than DEVSIZE, this bit will be set. Write "1" to clear this bit. |

**FSPI_CMD**

Address: Operational Base + offset (0x0100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | WO | 0x0 | CS<br>Device Chip Select.<br>2'b00: Chip select 0<br>2'b01: Chip select 1<br>2'b10: Reserved<br>2'b11: Reserved |
| 29:16 | WO | 0x0000 | TRB<br>Total Transfer Bytes<br>14'd0: No data<br>14'd1: 1 Byte<br>14'd2: 2 Bytes<br>...<br>Total data bytes number that will write to or read from the device. |
| 15:14 | WO | 0x0 | ADDRB<br>Address Bits<br>2'b00: 0 bit<br>2'b01: 24 bits<br>2'b10: 32 bits<br>2'b11: From the ABIT register<br>Address bits number select in indirect access mode. If there is not address command to send, set to zero. |
| 13 | WO | 0x0 | CONT<br>Continuous<br>1'b0: Disable continuous mode<br>1'b1: Enable continuous mode<br>AX mode or Continuous mode or XIP mode for device which begins with address. |
| 12 | WO | 0x0 | WR<br>Write or Read<br>1'b0: Read<br>1'b1: Write |
| 11:8 | WO | 0x0 | DUMM<br>Dummy Cycles<br>4'h0: No dummy cycle<br>...<br>4'h8: 8 cycles<br>...<br>Dummy bit cycles in indirect access mode. |
| 7:0 | WO | 0x00 | CMD<br>Command<br>Command data in indirect access mode. |

**FSPI_ADDR**

Address: Operational Base + offset (0x0104)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | WO | 0x00000000 | ADDR<br>Address Register<br>Indirect access start address data for current command sequence. |

**FSPI_DATA**

Address: Operational Base + offset (0x0108)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | DATA<br>Data Register<br>Device data read or write from/to device. |

**FSPI_CTRL1**

Address: Operational Base + offset (0x0200)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RO | 0x00000 | reserved |
| 13:12 | RW | 0x0 | DATB<br>Data Line Width<br>2'b00: 1 bit, x1 mode<br>2'b01: 2 bits, x2 mode<br>2'b10: 4 bits, x4 mode<br>2'b11: Reserved<br>Set this DATB to match the CMD sequence before doing indirect access mode and memory mapped access mode. |
| 11:10 | RW | 0x0 | ADRB<br>Address Line Width<br>2'b00: 1 bit, x1 mode<br>2'b01: 2 bits, x2 mode<br>2'b10: 4 bits, x4 mode<br>2'b11: Reserved<br>Set this ADRB to match the CMD sequence before doing indirect access mode and memory mapped access mode. |
| 9:8 | RW | 0x0 | CMDB<br>Command Line Width<br>2'b00: 1 bit, x1 mode<br>2'b01: 2 bits, x2 mode<br>2'b10: 4 bits, x4 mode<br>2'b11: Reserved<br>Set this CMDB to match the CMD sequence before doing indirect access mode and memory mapped access mode. |
| 7:4 | RW | 0x0 | IDLE_CYCLE<br>Idle Cycles When Switching IO from Output to Input<br>4'h0: Idle hold is disable<br>4'h1: Hold the SCLK in idle for 2 cycles when switch to shift in<br>...<br>4'hf: Hold the SCLK in idle for 16 cycles when switch to shift in<br>To improve the transform IO timing, the application can set this register to hold the SCLK in low state or high state. |
| 3:2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | SHIFTPHASE<br>Shift Phase of Data Input in Controller<br>1'b0: Shift input data at posedge SCLK<br>1'b1: Shift input data at negedge SCLK<br>The application can select the input data captured by posedge of SCLK when "0" or negedge of SCLK when "1". |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | SPIM<br>Serial Peripheral Interface Mode<br>1'b0: Mode 0<br>1'b1: Mode 3<br>SPIM is used to control the serial mode (CPOL and CPHA). CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported. |

**FSPI_AX1**

Address: Operational Base + offset (0x0214)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | AX<br>Auxiliary Data<br>The AX value when doing the continuous read (enhance mode or XIP mode). That is M7-M0 in "Continuous Read Mode". |

**FSPI_ABIT1**

Address: Operational Base + offset (0x0218)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4:0 | RW | 0x00 | ABIT<br>Address Bits Extend<br>5'h0: 1 bit<br>5'h1: 2 bits<br>...<br>5'h1f: 32 bits<br>Only valid when ADDRB is set to 2'b11. |

**FSPI_DLL_CTRL1**

Address: Operational Base + offset (0x023C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15 | RW | 0x0 | SCLK_SMP_SEL<br>SCLK sampling selection<br>1'b0: Bypass DLL<br>1'b1: From DLL<br>The sampling SCLK source selection. |
| 14:9 | RO | 0x00 | reserved |
| 8:0 | RW | 0x001 | SMP_DLL_CFG<br>Sample Delay Line Configuration<br>9'h0: 1 DLL element cell<br>9'h1: 1 DLL element cell<br>9'h2: 2 DLL element cells<br>...<br>9'h1ff: 511 DLL element cells<br>This register to control the sampling delay line cell used. The maximum DLL element cells is decided by process. |

**FSPI_XMMC_WCMD1**

Address: Operational Base + offset (0x0250)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:14 | WO | 0x0 | ADDRB<br>Address Bits<br>2'b00: 0 bit<br>2'b01: 24 bits<br>2'b10: 32 bits<br>2'b11: From the ABIT register<br>Address bits number select in memory mapped mode, if there is not address command to send, set to zero. |
| 13 | WO | 0x0 | CONT<br>Continuous<br>1'b0: Disable continuous mode<br>1'b1: Enable continuous mode<br>AX mode or Continuous mode or XIP mode for device which begins with address. |
| 12 | RO | 0x0 | reserved |
| 11:8 | WO | 0x0 | DUMM<br>Dummy Cycles<br>4'h0: No dummy cycle<br>...<br>4'h8: 8 cycles<br>...<br>Dummy bit cycles in memory mapped mode. |
| 7:0 | WO | 0x00 | CMD<br>Command<br>Command data in memory mapped access mode. |

**FSPI_XMMC_RCMD1**

Address: Operational Base + offset (0x0254)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:14 | WO | 0x0 | ADDRB<br>Address Bits<br>2'b00: 0 bit<br>2'b01: 24 bits<br>2'b10: 32 bits<br>2'b11: From the ABIT register<br>Address bits number select in memory mapped mode, if there is not address command to send, set to zero. |
| 13 | WO | 0x0 | CONT<br>Continuous<br>1'b0: Disable continuous mode<br>1'b1: Enable continuous mode<br>AX mode or Continuous mode or XIP mode for device which begins with address. |
| 12 | RO | 0x0 | reserved |
| 11:8 | WO | 0x0 | DUMM<br>Dummy Cycles<br>4'h0: No dummy cycle<br>...<br>4'h8: 8 cycles<br>...<br>Dummy bit cycles in memory mapped mode. |
| 7:0 | WO | 0x00 | CMD<br>Command<br>Command data in memory mapped access mode. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**FSPI_DEVSIZE1**

Address: Operational Base + offset (0x0264)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4:0 | RW | 0x12 | DSIZE<br>Device Size<br>5'd0: 1 byte<br>5'd1: 2 bytes<br>5'd2: 4 bytes<br>.....<br>5'd10: 1K bytes<br>.....<br>5'd20: 1M bytes<br>.....<br>5'd31: 4G bytes<br>Device size is used to generate slop over status. |

**FSPI_TME1**

Address: Operational Base + offset (0x0268)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | SCLK_INATM_EN<br>SCLK Inactive Timeout Enable<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RO | 0x0 | reserved |

# 30.5 Interface Description

Table 30-2 FSPI IO M0 Group Interface Description

| Module Pin | Dir | Pin Name | IOMUX Setting |
|---|---|---|---|
| sfc_sclk | O | EMMC_CMD/FSPI_CLK_M0/GPIO2_A0_u | BUS_IOC_GPIO2A_IOMUX_SEL_L[3:0]=4'h2 |
| sfc_csn0 | O | EMMC_D6/FSPI_CS0N_M0/GPIO2_D6_u | BUS_IOC_GPIO2D_IOMUX_SEL_H[11:8]=4'h2 |
| sfc_csn1 | O | EMMC_D7/FSPI_CS1N_M0/GPIO2_D7_u | BUS_IOC_GPIO2D_IOMUX_SEL_H[15:12]=4'h2 |
| sfc_sio0 | I/O | EMMC_D0/FSPI_D0_M0/GPIO2_D0_u | BUS_IOC_GPIO2D_IOMUX_SEL_L[3:0]=4'h2 |
| sfc_sio1 | I/O | EMMC_D1/FSPI_D1_M0/GPIO2_D1_u | BUS_IOC_GPIO2D_IOMUX_SEL_L[7:4]=4'h2 |
| sfc_sio2 | I/O | EMMC_D2/FSPI_D2_M0/GPIO2_D2_u | BUS_IOC_GPIO2D_IOMUX_SEL_L[11:8]=4'h2 |
| sfc_sio3 | I/O | EMMC_D3/FSPI_D3_M0/GPIO2_D3_u | BUS_IOC_GPIO2D_IOMUX_SEL_L[15:12]=4'h2 |

*Notes: **I**=input, **O**=output, **I/O**=input/output, bidirectional.*

Table 30-3 FSPI M1 Group Interface Description

| Module Pin | Dir | Pin Name | IOMUX Setting |
|---|---|---|---|
| sfc_sclk | O | GMAC0_TXCLK/SDIO_CLK_M0/FSPI_CLK_M1/I2C3_SDA_M3/GPIO2_B3_d | BUS_IOC_GPIO2B_IOMUX_SEL_L[15:12]=4'h3 |
| sfc_csn0 | O | GMAC0_PTP_REFCLK/FSPI_CS0N_M1/HDMI_TX1_SDA_M0/I2C4_SDA_M1/UART7_RX_M0/GPIO2_B4_u | BUS_IOC_GPIO2B_IOMUX_SEL_H[3:0]=4'h3 |
| sfc_csn1 | O | GMAC0_PPSTRING/FSPI_CS1N_M1/HDMI_TX1_SCL_M0/I2C4_SCL_M1/UART7_TX_M0/GPIO2_B5_u | BUS_IOC_GPIO2B_IOMUX_SEL_H[7:4]=4'h3 |
| sfc_sio0 | I/O | GMAC0_RXD2/SDIO_D0_M0/FSPI_D0_M1/UART6_RX_M0/GPIO2_A6_u | BUS_IOC_GPIO2A_IOMUX_SEL_H[11:8]=4'h3 |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Module Pin | Dir | Pin Name | IOMUX Setting |
|---|---|---|---|
| sfc_sio1 | I/O | GMAC0_RXD3/SDIO_D1_M0/FSPI_D1_M1/UART6_TX_M0/GPIO2_A7_u | BUS_IOC_GPIO2A_IOMUX_SEL_H[15:12]=4'h3 |
| sfc_sio2 | I/O | GMAC0_RXCLK/SDIO_D2_M0/FSPI_D2_M1/I2C8_SCL_M1/UART6_RTSN_M0/GPIO2_B0_u | BUS_IOC_GPIO2B_IOMUX_SEL_L[3:0]=4'h3 |
| sfc_sio3 | I/O | GMAC0_TXD2/SDIO_D3_M0/FSPI_D3_M1/I2C8_SDA_M1/UART6_CTSN_M0/GPIO2_B1_u | BUS_IOC_GPIO2B_IOMUX_SEL_L[7:4]=4'h3 |

*Notes: **I**=input, **O**=output, **I/O**=input/output, bidirectional.*

Table 30-4 FSPI M2 Group Interface Description

| Module Pin | Dir | Pin Name | IOMUX Setting |
|---|---|---|---|
| sfc_sclk | O | GMAC1_RXCLK/SDIO_CLK_M1/MIPI_CAMERA0_CLK_M1/FSPI_CLK_M2/I2C4_SDA_M0/UART8_CTSN_M1/GPIO3_A5_d | BUS_IOC_GPIO3A_IOMUX_SEL_H[7:4]=4'h5 |
| sfc_csn0 | O | CIF_D8/FSPI_CS0N_M2/PCIE30X4_CLKREQN_M2/HDMI_TX1_CEC_M2/CAN2_RX_M0/UART5_TX_M1/SPI3_CS0_M3/GPIO3_C4_u | BUS_IOC_GPIO3C_IOMUX_SEL_H[3:0]=4'h2 |
| sfc_csn1 | O | CIF_D9/FSPI_CS1N_M2/PCIE30X4_WAKEN_M2/HDMI_TX1_SDA_M1/CAN2_TX_M0/UART5_RX_M1/SPI3_CS1_M3/GPIO3_C5_u | BUS_IOC_GPIO3C_IOMUX_SEL_H[7:4]=4'h2 |
| sfc_sio0 | I/O | GMAC1_TXD2/SDIO_D0_M1/I2S3_MCLK/FSPI_D0_M2/I2C6_SDA_M4/PWM10_M0/SPI4_MISO_M1/GPIO3_A0_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[3:0]=4'h5 |
| sfc_sio1 | I/O | GMAC1_TXD3/SDIO_D1_M1/I2S3_SCLK/AUDDSM_LN/FSPI_D1_M2/I2C6_SCL_M4/PWM11_IR_M0/SPI4_MOSI_M1/GPIO3_A1_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[7:4]=4'h5 |
| sfc_sio2 | I/O | GMAC1_RXD2/SDIO_D2_M1/I2S3_LRCK/AUDDSM_LP/FSPI_D2_M2/UART8_TX_M1/SPI4_CLK_M1/GPIO3_A2_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[11:8]=4'h5 |
| sfc_sio3 | I/O | GMAC1_RXD3/SDIO_D3_M1/I2S3_SDO/AUDDSM_RN/FSPI_D3_M2/UART8_RX_M1/SPI4_CS0_M1/GPIO3_A3_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[15:12]=4'h5 |

*Notes: **I**=input, **O**=output, **I/O**=input/output, bidirectional.*

Copyright 2022 © Rockchip Electronics Co., Ltd.

# 30.6 Application Notes

## 30.6.1 Typical Program Flow Without DMA

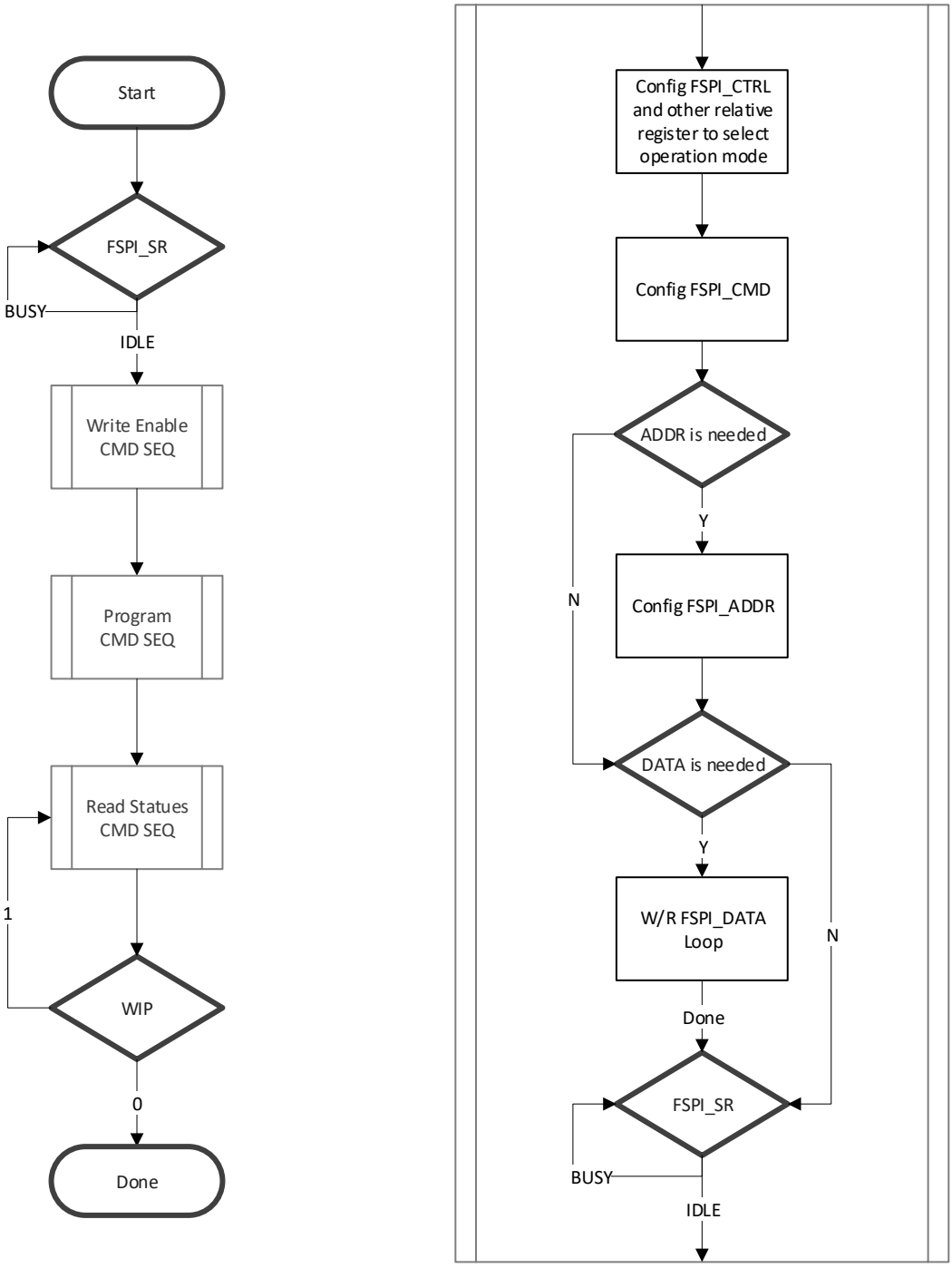



Fig. 30-2 Program Flow

All the AHB bus write data to FSPI_CMD, FSPI_ADDR and FSPI_DATA will be marked with different header and then pushed into transmit FIFO by writing order.

Copyright 2022 © Rockchip Electronics Co., Ltd.

## 30.6.2 Typical READ Flow Without DMA

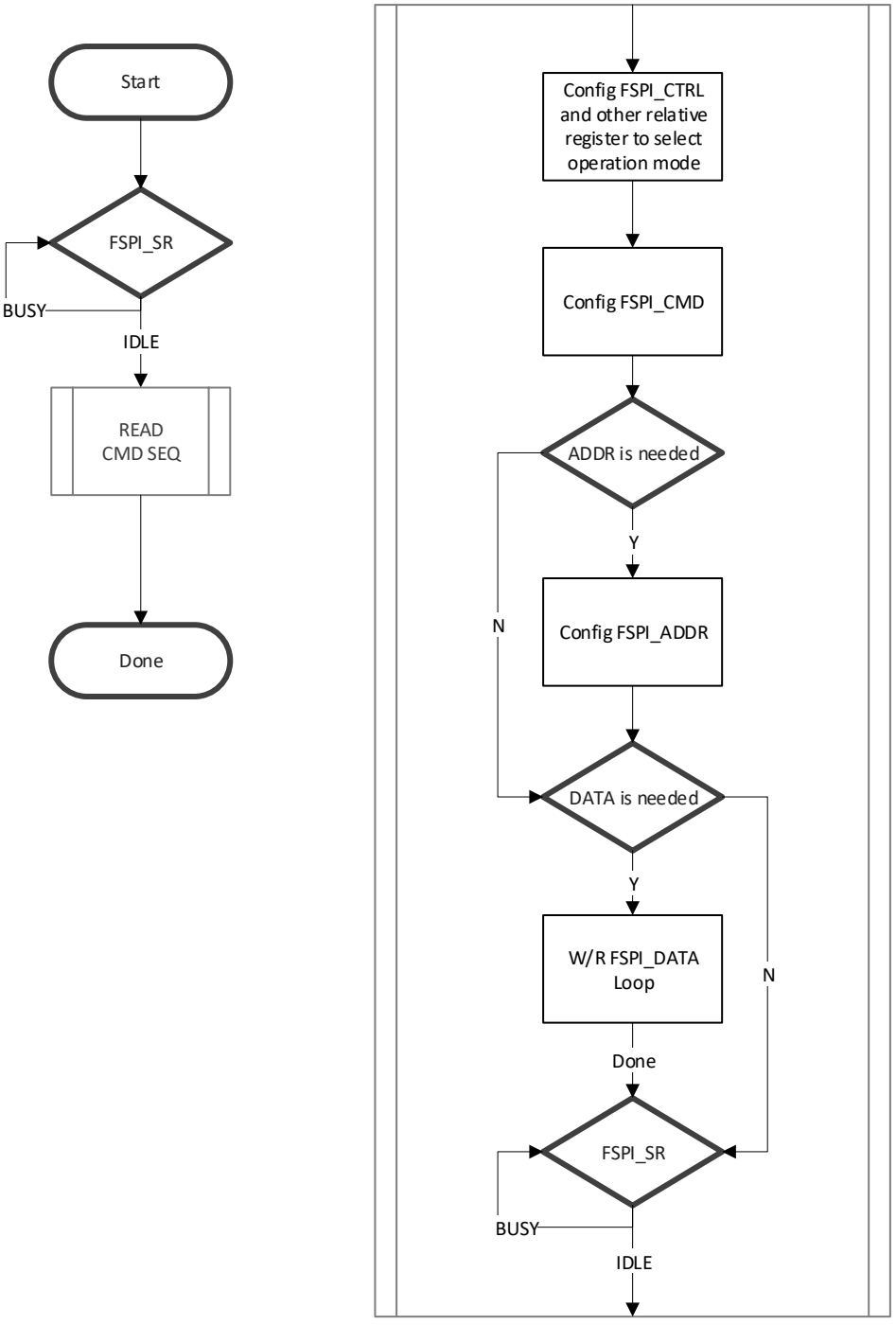



Fig. 30-3 Read Flow

### 30.6.3 Command Flow with DMA

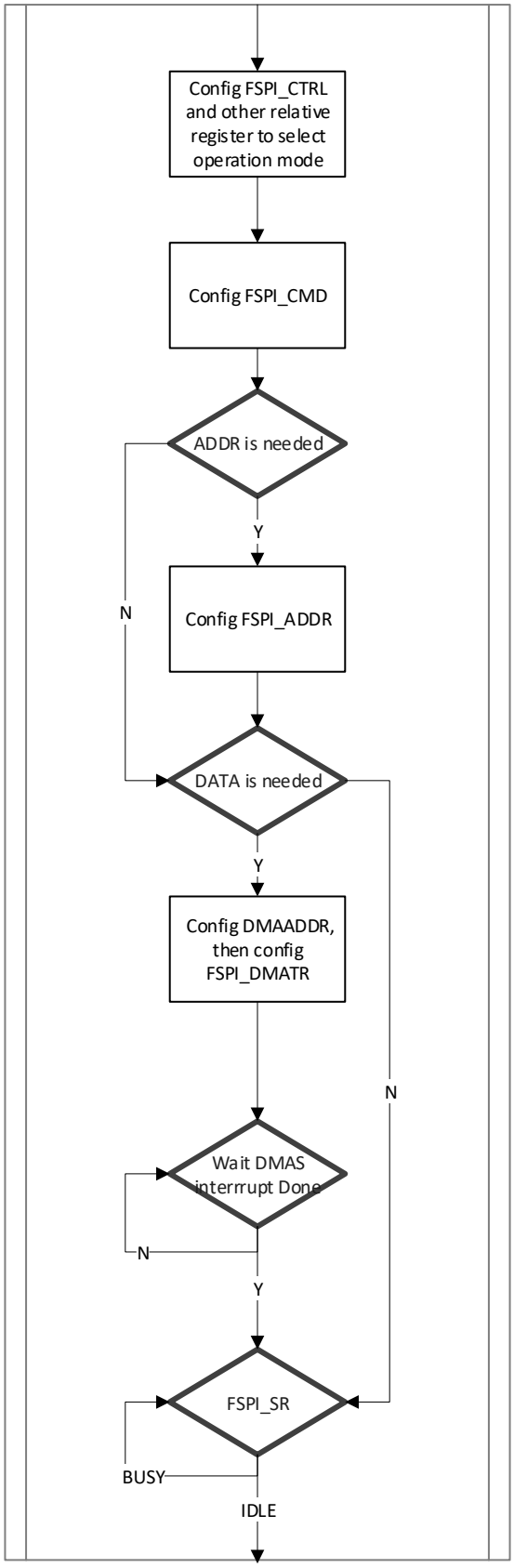



Fig. 30-4 Command with DMA Flow

The total transfer bytes is decided by TRB register in FSPI_CMD and must be aligned to 2 bytes.

Copyright 2022 © Rockchip Electronics Co., Ltd.

### 30.6.4 SPI Mode and Sampling Phase Control

The register SPIM in FSPI_CTRL will decide the default value of SCLK when CS# is inactive. When SPIM=0, the default value is 0, means Mode 0. When SPIM=1, the default value is 1, means SPI Mode 3.

The register SHIFTPAHSE in FSPI_CTRL will decide when to sample the SIO data. If SHIFTPAHSE=0, it will sample the data at the posedge of SCLK sampling clock. If SHIFTPHASE=1, it will sample the data at the negedge of SCLK sampling. The phase delay of sampling clock SCLK is configurable by SMP_DLL_CFG. It is strongly recommended that the SMP_DLL_CFG is set to 1 when SCLK_SMP_SEL is in bypass mode.

Individual FSPI_DLL_CTRL[n] allows flexibly control the DLL for each CSn channel, and the DLL is switched dynamically when the CSn is in operation.

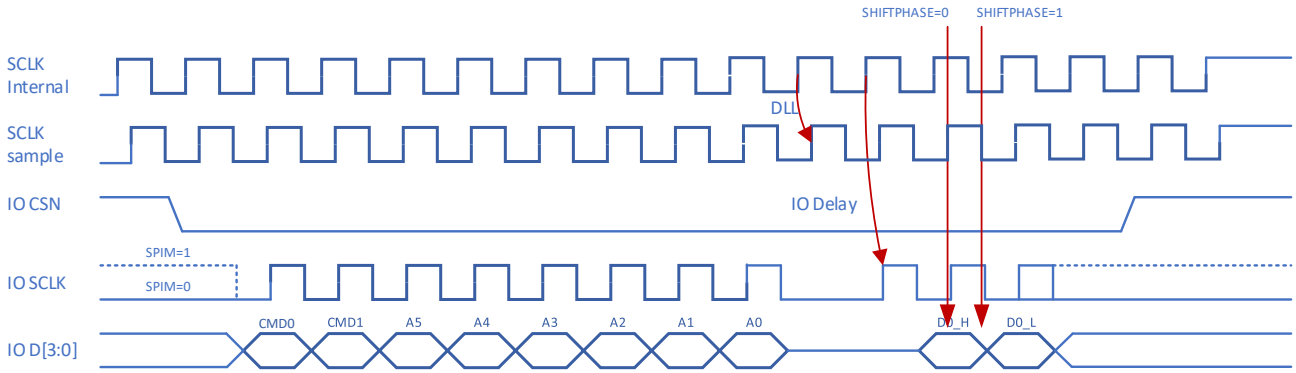



Fig. 30-5 SPI mode

### 30.6.5 Idle Cycles

The FSPI_CTRL register is a global control register, when the controller is in busy state (FSPI_SR), FSPI_CTRL cannot be set. The field IDLE_CYCLE (FSPI_CTRL[7:4]) of this register are used to configure the idle level cycles of FSPI core clock (SCLK) before reading the first bit of the read command.

Like the following picture shows, the highlighted line of the SCLK is the idle cycles, during these cycles, the chip pad is switched to output. When IDLE_CYCLE =0, it means there will be no idle level cycles.

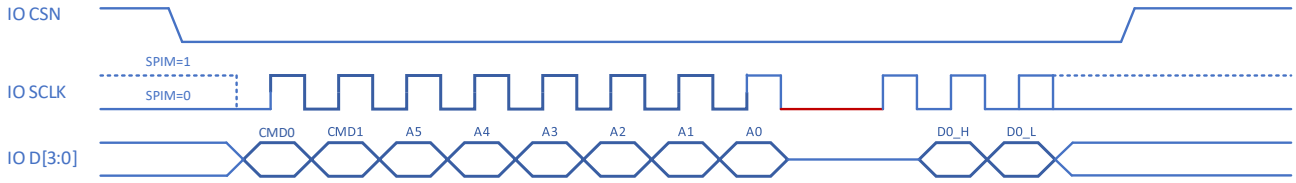



Fig. 30-6 Idle cycles

### 30.6.6 Memory-Mapped Mode

After the Controller is configured as Memory-Mapped mode, the normal operation mode is not allowed which means indirect command transaction is forbidden unless software configures the FSPI_MODE back to indirect access mode.

Before switching into Memory-Mapped mode, the software should initiate some transactions to configure the external device, such as Quad IO enable and IO Drive Strength.

In Memory-Mapped mode, it supports read transaction from serial NOR Flash and serial pSRAM, but only support write transaction into serial pSRAM.

Copyright 2022 © Rockchip Electronics Co., Ltd.

# Chapter 31 Serial Peripheral Interface (SPI)

## 31.1 Overview

The serial peripheral interface is an APB slave device. There are four possible combinations for the serial clock phase and polarity. The clock phase (SCPH) determines whether the serial transfer begins with the falling edge of slave select signals or the first edge of the serial clock. The slave select line is held high when the SPI is idle or disabled. This SPI controller can work as either master or slave mode.

SPI Controller supports the following features:
- Support Motorola SPI, TI Synchronous Serial Protocol and National Semiconductor Micro wire interface
- Support 32-bit APB bus
- Support two internal 16-bit wide and 64-location deep FIFOs, one for transmitting and the other for receiving serial data
- Support two chip select signals in master mode
- Support 4,8,16 bit serial data transfer
- Support configurable interrupt polarity
- Support asynchronous APB bus and SPI clock
- Support master and slave mode
- Support DMA handshake interface and configurable DMA water level
- Support transmit FIFO empty, underflow, receive FIFO full, overflow, interrupt and all interrupts can be masked
- Support configurable water level of transmit FIFO empty and receive FIFO full interrupt
- Support combine interrupt output
- Support up to half of SPI clock frequency transfer in master mode and one quarter of SPI clock frequency transfer in slave mode
- Support full and half duplex mode transfer
- Stop transmitting SCLK if transmit FIFO is empty or receive FIFO is full in master mode
- Support configurable delay from chip select active to SCLK active in master mode
- Support configurable period of chip select inactive between two parallel data in master mode
- Support big and little endian, MSB and LSB first transfer
- Support two 8-bit audio data store together in one 16-bit wide location
- Support sample RXD 0~3 SPI clock cycles later
- Support configurable SCLK polarity and phase
- Support fix and incremental address access to transmit and receive FIFO
- Support timeout mechanism in slave mode
- Support BYPASS slave mode, in which RX and TX logic is drive by SCLK_IN directly instead of spi_clk

## 31.2 Block Diagram

The SPI Controller comprises with:
- AMBA APB interface and DMA Controller Interface
- Transmit and receive FIFO controllers and an FSM controller
- Register block
- Shift control and interrupt

Copyright 2022 © Rockchip Electronics Co., Ltd. 

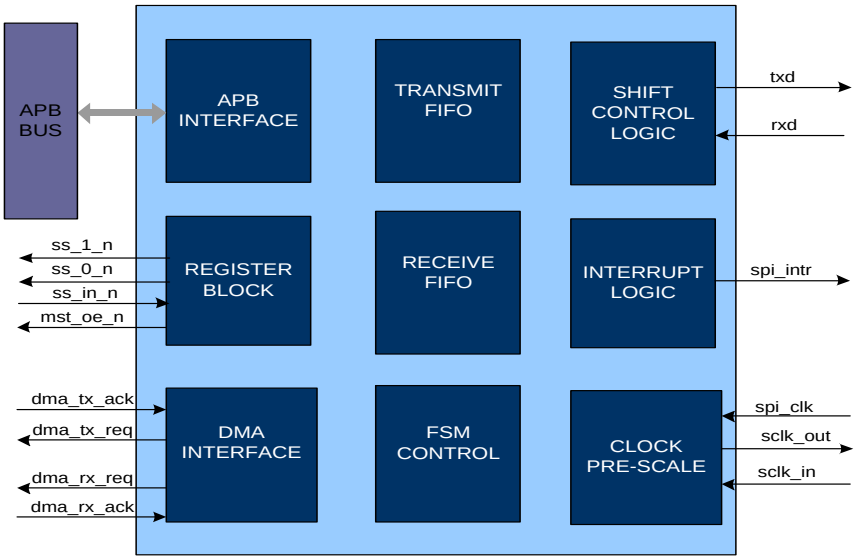



Fig. 31-1 SPI Controller Block Diagram

**APB INTERFACE**

The host processor accesses data, control, and status information on the SPI through the APB interface. The SPI supports APB data bus widths of 32 bits and 8 or 16 bits when reading or writing internal FIFO if data frame size(SPI_CTRL0[1:0]) is set to 8 bits.

**DMA INTERFACE**

This block has a handshaking interface to a DMA Controller to request and control transfers. The APB bus is used to perform the data transfer to or from the DMA Controller.

**FIFO LOGIC**

For transmit and receive transfers, data transmitted from the SPI to the external serial device is written into the transmit FIFO. Data received from the external serial device into the SPI is pushed into the receive FIFO. Both FIFOs are 64x16bits.

**FSM CONTROL**

Control the state's transformation of the design.

**REGISTER BLOCK**

All registers in the SPI are addressed at 32-bit boundaries to remain consistent with the APB bus. Where the physical size of any register is less than 32-bits wide, the upper unused bits of the 32-bit boundary are reserved. Writing to these bits has no effect; reading from these bits returns 0.

**SHIFT CONTROL**

Shift control logic shift the data from the transmit FIFO or to the receive FIFO. This logic automatically right-justifies receive data in the receive FIFO buffer.

**INTERRUPT CONTROL**

The SPI supports combined and individual interrupt requests, each of which can be masked. The combined interrupt request is the OR relationship between all other SPI interrupts after masking.

Copyright 2022 © Rockchip Electronics Co., Ltd.

## 31.3 Function Description

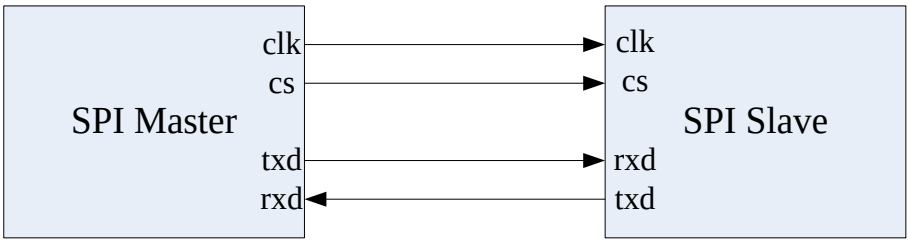



Fig. 31-2 SPI Master and Slave Interconnection

The SPI controller support dynamic switching between master and slave in a system. The diagram show how the SPI controller connects with other SPI devices.

**Operation Modes**

The SPI can be configured in the following two fundamental modes of operation: Master Mode when SPI_CTRLR0 [20] is 1'b0, Slave Mode when SPI_CTRLR0 [20] is 1'b1.

**Transfer Modes**

The SPI operates in the following three modes when transferring data on the serial bus.
1). Transmit and Receive
When SPI_CTRLR0 [19:18] == 2'b00, both transmit and receive logic are valid.
2). Transmit Only
When SPI_CTRLR0 [19:18] == 2'b01, the receive data are invalid and should not be stored in the receive FIFO.
3). Receive Only
When SPI_CTRLR0 [19:18] == 2'b10, the transmit data are invalid.

**Clock Ratios**

A summary of the frequency ratio restrictions between the bit-rate clock (sclk_out/sclk_in) and the SPI peripheral clock (spi_clk) are described as:
When SPI Controller works as master, the $F_{spi_clk}$>= 2 × (maximum $F_{sclk_out}$)
When SPI Controller works as slave, the $F_{spi_clk}$>= 6 × (maximum $F_{sclk_in}$)

With the SPI, the clock polarity (SCPOL) configuration parameter determines whether the inactive state of the serial clock is high or low. To transmit data, both SPI peripherals must have identical serial clock phase (SCPH) and clock polarity (SCPOL) values. The data frame can be 4/8/16 bits in length.

When the configuration parameter SCPH = 0, data transmission begins on the falling edge of the slave select signal. The first data bit is captured by the master and slave peripherals on the first edge of the serial clock; therefore, valid data must be present on the txd and rxd lines prior to the first serial clock edge. The following two figures show a timing diagram for a single SPI data transfer with SCPH = 0. The serial clock is shown for configuration parameters SCPOL = 0 and SCPOL = 1.

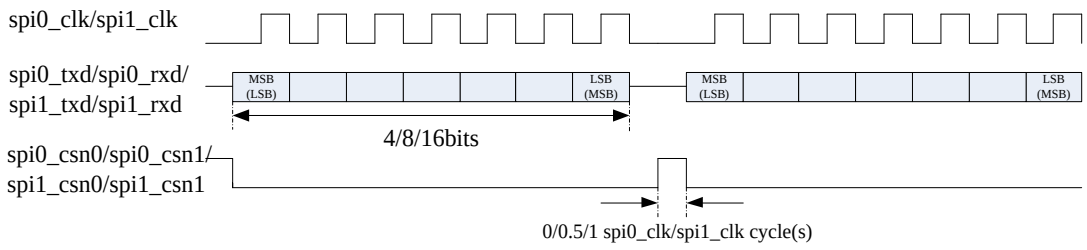



Fig. 31-3 SPI Format (SCPH=0 SCPOL=0)

Copyright 2022 © Rockchip Electronics Co., Ltd.

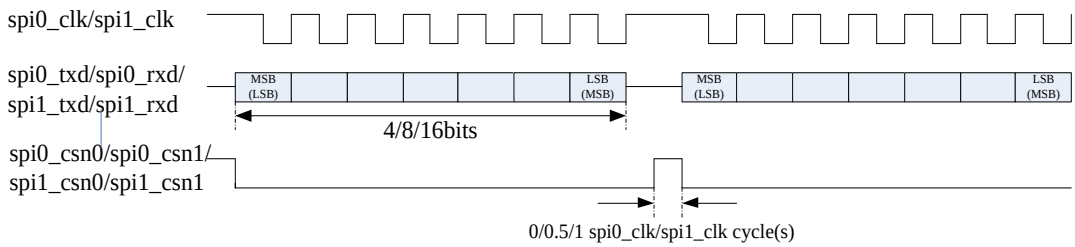



Fig. 31-4 SPI Format (SCPH=0 SCPOL=1)

When the configuration parameter SCPH = 1, both master and slave peripherals begin transmitting data on the first serial clock edge after the slave select line is activated. The first data bit is captured on the second (trailing) serial clock edge. Data are propagated by the master and slave peripherals on the leading edge of the serial clock. During continuous data frame transfers, the slave select line may be held active-low until the last bit of the last frame has been captured. The following two figures show the timing diagram for the SPI format when the configuration parameter SCPH = 1.

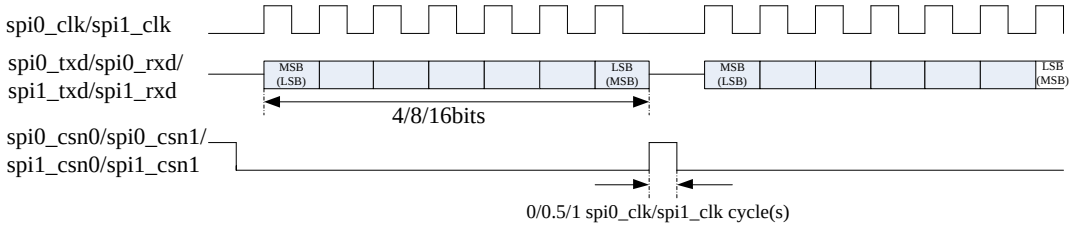



Fig. 31-5 SPI Format (SCPH=1 SCPOL=0)

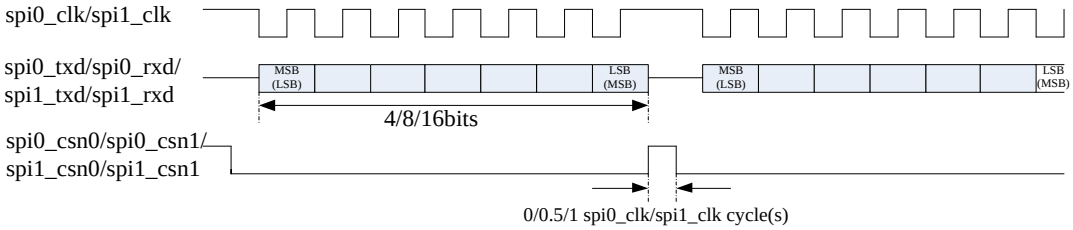



Fig. 31-6 SPI Format (SCPH=1 SCPOL=1)

# 31.4 Register Description

## 31.4.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| SPI_CTRLR0 | 0x0000 | W | 0x00000002 | Control Register 0 |
| SPI_CTRLR1 | 0x0004 | W | 0x00000000 | Control Register 1 |
| SPI_ENR | 0x0008 | W | 0x00000000 | SPI Enable Register |
| SPI_SER | 0x000C | W | 0x00000000 | Slave Enable Register |
| SPI_BAUDR | 0x0010 | W | 0x00000000 | Baud Rate Select |
| SPI_TXFTLR | 0x0014 | W | 0x00000000 | Transmit FIFO Threshold Level |
| SPI_RXFTLR | 0x0018 | W | 0x00000000 | Receive FIFO Threshold Level |
| SPI_TXFLR | 0x001C | W | 0x00000000 | Transmit FIFO Level |
| SPI_RXFLR | 0x0020 | W | 0x00000000 | Receive FIFO Level |
| SPI_SR | 0x0024 | W | 0x0000004C | SPI Status |
| SPI_IPR | 0x0028 | W | 0x00000000 | Interrupt Polarity |
| SPI_IMR | 0x002C | W | 0x00000000 | Interrupt Mask |
| SPI_ISR | 0x0030 | W | 0x00000000 | Interrupt Status |
| SPI_RISR | 0x0034 | W | 0x00000001 | Raw Interrupt Status |
| SPI_ICR | 0x0038 | W | 0x00000000 | Interrupt Clear |
| SPI_DMACR | 0x003C | W | 0x00000000 | DMA Control |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| SPI_DMATDLR | 0x0040 | W | 0x00000000 | DMA Transmit Data Level |
| SPI_DMARDLR | 0x0044 | W | 0x00000000 | DMA Receive Data Level |
| SPI_VERSION | 0x0048 | W | 0x00110002 | IP version |
| SPI_TIMEOUT | 0x004C | W | 0x00000000 | Timeout control register |
| SPI_BYPASS | 0x0050 | W | 0x00000000 | BYPASS control register |
| SPI_TXDR | 0x0400 | W | 0x00000000 | Transmit FIFO Data |
| SPI_RXDR | 0x0800 | W | 0x00000000 | Receive FIFO Data |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 31.4.2 Detail Registers Description

**SPI_CTRLR0**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |
| 25 | RW | 0x0 | lbk<br>Loop back mode select.<br>1'b0: Normal mode.<br>1'b1: Loop back mode, rxd is connected to txd. |
| 24:23 | RW | 0x0 | soi<br>SS_N output inverted.<br>1'b0: Corresponding bit of ss_in is not inverted.<br>1'b1: Corresponding bit of ss_in is inverted. |
| 22 | RW | 0x0 | sm<br>SCLK_IN is masked by SS_N or not.<br>1'b0: SCLK_IN is masked<br>1'b1: SCLK_IN is not masked |
| 21 | RW | 0x0 | mtm<br>Valid when frame format is set to National Semiconductors Microwire.<br>1'b0: Non-sequential transfer<br>1'b1: Sequential transfer |
| 20 | RW | 0x0 | opm<br>Master and slave mode select.<br>1'b0: Master Mode<br>1'b1: Slave Mode |
| 19:18 | RW | 0x0 | xfm<br>Transmit and receive mode select.<br>2'b00 : Transmit & Receive<br>2'b01 : Transmit Only<br>2'b10 : Receive Only<br>2'b11 : Reserved |
| 17:16 | RW | 0x0 | frf<br>2'b00: Motorola SPI<br>2'b01: Texas Instruments SSP<br>2'b10: National Semiconductors Microwire<br>2'b11: Reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:14 | RW | 0x0 | rsd<br>When SPI is configured as a master, if the rxd data cannot be sampled by the sclk_out edge at the right time, this register should be configured to define the number of the spi_clk cycles after the active sclk_out edge to sample rxd data later when SPI works at high frequency.<br>2'b00: Do not delay<br>2'b01: 1 cycle delay<br>2'b10: 2 cycles delay<br>2'b11: 3 cycles delay |
| 13 | RW | 0x0 | bht<br>Valid when data frame size is 8bit.<br>1'b0: APB 16bit write/read, spi 8bit write/read.<br>1'b1: APB 8bit write/read, spi 8bit write/read. |
| 12 | RW | 0x0 | fbm<br>1'b0: First bit is MSB.<br>1'b1: First bit is LSB. |
| 11 | RW | 0x0 | em<br>Serial endian mode can be configured by this bit. APB endian mode is always little endian.<br>1'b0: Little endian<br>1'b1: Big endian |
| 10 | RW | 0x0 | ssd<br>Valid when the frame format is set to Motorola SPI and SPI used as a master.<br>1'b0: The period between ss_n active and sclk_out active is half sclk_out cycles.<br>1'b1: The period between ss_n active and sclk_out active is one sclk_out cycle. |
| 9:8 | RW | 0x0 | csm<br>Valid when the frame format is set to Motorola SPI and SPI used as a master.<br>2'b00: ss_n keep low after every frame data is transferred.<br>2'b01: ss_n be high for half sclk_out cycles after every frame data is transferred.<br>2'b10: ss_n be high for one sclk_out cycle after every frame data is transferred.<br>2'b11: Reserved |
| 7 | RW | 0x0 | scpol<br>Valid when the frame format is set to Motorola SPI.<br>1'b0: Inactive state of serial clock is low.<br>1'b1: Inactive state of serial clock is high. |
| 6 | RW | 0x0 | scph<br>Valid when the frame format is set to Motorola SPI.<br>1'b0: Serial clock toggles in middle of first data bit.<br>1'b1: Serial clock toggles at start of first data bit. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5:2 | RW | 0x0 | cfs<br>Selects the length of the control word for the Microwire frame format.<br>4'b0000~4'b0010: Reserved<br>4'b0011: 4-bit serial data transfer<br>4'b0100: 5-bit serial data transfer<br>4'b0101: 6-bit serial data transfer<br>4'b0110: 7-bit serial data transfer<br>4'b0111: 8-bit serial data transfer<br>4'b1000: 9-bit serial data transfer<br>4'b1001: 10-bit serial data transfer<br>4'b1010: 11-bit serial data transfer<br>4'b1011: 12-bit serial data transfer<br>4'b1100: 13-bit serial data transfer<br>4'b1101: 14-bit serial data transfer<br>4'b1110: 15-bit serial data transfer<br>4'b1111: 16-bit serial data transfer |
| 1:0 | RW | 0x2 | dfs<br>Selects the data frame length.<br>2'b00: 4bit data<br>2'b01: 8bit data<br>2'b10: 16bit data<br>2'b11: Reserved |

**SPI_CTRLR1**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ndm<br>When Transfer Mode is receive only, this register field sets the number of data frames to be continuously received by the SPI. The SPI continues to receive serial data until the number of data frames received is equal to this register value plus 1, which enables you to receive up to 4GB of data in a continuous transfer. |

**SPI_ENR**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | enr<br>Enables and disables all SPI operations. Transmit and receive FIFO buffers are cleared when the device is disabled. |

**SPI_SER**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1:0 | RW | 0x0 | ser<br>Slave enable register. The register enable the individual slave select output lines, 2 slave-select output pins are available. This register is valid only when SPI is configured as a master device. |

**SPI_BAUDR**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0000 | baudr<br>SPI Clock Divider. This register is valid only when the SPI is configured as a master device. The LSB for this field is always set to 0 and is unaffected by a write operation, which ensures an even value is held in this register. If the value is 0, the serial output clock (sclk_out) is disabled. The frequency of the sclk_out is derived from the following equation:<br>Fsclk_out = Fspi_clk/ SCKDV<br>Where SCKDV is any even value between 2 and 65534.<br>For example:<br>for Fspi_clk = 3.6864MHz and SCKDV =2<br>Fsclk_out = 3.6864/2= 1.8432MHz |

**SPI_TXFTLR**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5:0 | RW | 0x00 | xftlr<br>When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered. |

**SPI_RXFTLR**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5:0 | RW | 0x00 | rxftlr<br>When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO full interrupt is triggered. |

**SPI_TXFLR**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6:0 | RO | 0x00 | txflr<br>Contains the number of valid data entries in the transmit FIFO. |

**SPI_RXFLR**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6:0 | RO | 0x00 | rxflr<br>Contains the number of valid data entries in the receive FIFO. |

**SPI_SR**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6 | RO | 0x1 | ssi<br>1'b0: ss_in_n is low.<br>1'b1: ss_in_n is high. |
| 5 | RO | 0x0 | stb<br>1'b0: Slave tx not busy.<br>1'b1: Slave tx busy. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RO | 0x0 | rff<br>1'b0: Receive FIFO is not full.<br>1'b1: Receive FIFO is full. |
| 3 | RO | 0x1 | rfe<br>1'b0: Receive FIFO is not empty.<br>1'b1: Receive FIFO is empty. |
| 2 | RO | 0x1 | tfe<br>1'b0: Transmit FIFO is not empty.<br>1'b1: Transmit FIFO is empty. |
| 1 | RO | 0x0 | tff<br>1'b0: Transmit FIFO is not full.<br>1'b1: Transmit FIFO is full. |
| 0 | RO | 0x0 | bsf<br>When set, indicates that a serial transfer is in progress; when cleared, indicates that the SPI is idle or disabled.<br>1'b0: SPI is idle or disabled.<br>1'b1: SPI is actively transferring data. |

**SPI_IPR**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | ipr<br>Interrupt Polarity Register.<br>1'b0: Active Interrupt Polarity Level is HIGH.<br>1'b1: Active Interrupt Polarity Level is LOW. |

**SPI_IMR**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RW | 0x0 | txfim<br>1'b0: TX finish interrupt is masked.<br>1'b1: TX finish interrupt is not masked. |
| 6 | RW | 0x0 | sspim<br>1'b0: ss_in_n posedege interrupt is masked.<br>1'b1: ss_in_n posedege interrupt is not masked. |
| 5 | RW | 0x0 | toim<br>1'b0: spi timeout interrupt is masked.<br>1'b1: spi timeout interrupt is not masked. |
| 4 | RW | 0x0 | rffim<br>1'b0: spi_rxf_intr interrupt is masked.<br>1'b1: spi_rxf_intr interrupt is not masked. |
| 3 | RW | 0x0 | rfoim<br>1'b0: spi_rxo_intr interrupt is masked.<br>1'b1: spi_rxo_intr interrupt is not masked. |
| 2 | RW | 0x0 | rfuim<br>1'b0: spi_rxu_intr interrupt is masked.<br>1'b1: spi_rxu_intr interrupt is not masked. |
| 1 | RW | 0x0 | tfoim<br>1'b0: spi_txo_intr interrupt is masked.<br>1'b1: spi_txo_intr interrupt is not masked. |
| 0 | RW | 0x0 | tfeim<br>1'b0: spi_txe_intr interrupt is masked.<br>1'b1: spi_txe_intr interrupt is not masked. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**SPI_ISR**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RW | 0x0 | txfis<br>1'b0: TX finish interrupt is not active after masking.<br>1'b1: TX finish interrupt is active after masking. |
| 6 | RW | 0x0 | sspis<br>1'b0: ss_in_n posedege interrupt is not active after masking.<br>1'b1: ss_in_n posedege interrupt is active after masking. |
| 5 | RW | 0x0 | tois<br>1'b0: spi timeout interrupt is not active after masking.<br>1'b1: spi timeout interrupt is active after masking. |
| 4 | RO | 0x0 | rffis<br>1'b0: spi_rxf_intr interrupt is not active after masking.<br>1'b1: spi_rxf_intr interrupt is full after masking. |
| 3 | RO | 0x0 | rfois<br>1'b0: spi_rxo_intr interrupt is not active after masking.<br>1'b1: spi_rxo_intr interrupt is active after masking. |
| 2 | RO | 0x0 | rfuis<br>1'b0: spi_rxu_intr interrupt is not active after masking.<br>1'b1: spi_rxu_intr interrupt is active after masking. |
| 1 | RO | 0x0 | tfois<br>1'b0: spi_txo_intr interrupt is not active after masking.<br>1'b1: spi_txo_intr interrupt is active after masking. |
| 0 | RO | 0x0 | tfeis<br>1'b0: spi_txe_intr interrupt is not active after masking.<br>1'b1: spi_txe_intr interrupt is active after masking. |

**SPI_RISR**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RW | 0x0 | txfris<br>1'b0: TX finish interrupt is not active prior to masking.<br>1'b1: TX finish interrupt is active prior to masking. |
| 6 | RW | 0x0 | sspris<br>1'b0: ss_in_n posedege interrupt is not active prior to masking.<br>1'b1: ss_in_n posedege interrupt is active prior to masking. |
| 5 | RW | 0x0 | toris<br>1'b0: spi_timeout interrupt is not active prior to masking.<br>1'b1: spi_timeout interrupt is active prior to masking. |
| 4 | RO | 0x0 | rffris<br>1'b0: spi_rxf_intr interrupt is not active prior to masking.<br>1'b1: spi_rxf_intr interrupt is full prior to masking. |
| 3 | RO | 0x0 | rforis<br>1'b0: spi_rxo_intr interrupt is not active prior to masking.<br>1'b1: spi_rxo_intr interrupt is active prior to masking. |
| 2 | RO | 0x0 | rfuris<br>1'b0: spi_rxu_intr interrupt is not active prior to masking.<br>1'b1: spi_rxu_intr interrupt is active prior to masking. |
| 1 | RO | 0x0 | tforis<br>1'b0: spi_txo_intr interrupt is not active prior to masking.<br>1'b1: spi_txo_intr interrupt is active prior to masking. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RO | 0x1 | tferis<br>1'b0: spi_txe_intr interrupt is not active prior to masking.<br>1'b1: spi_txe_intr interrupt is active prior to masking. |

**SPI_ICR**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6 | WO | 0x0 | ctxfi<br>Write 1 to Clear tx finish Interrupt. |
| 5 | WO | 0x0 | csspi<br>Write 1 to Clear ss_in_n posedge Interrupt. |
| 4 | WO | 0x0 | ctoi<br>Write 1 to Clear Timeout Interrupt. |
| 3 | WO | 0x0 | ctfoi<br>Write 1 to Clear Transmit FIFO Overflow Interrupt. |
| 2 | WO | 0x0 | crfoi<br>Write 1 to Clear Receive FIFO Overflow Interrupt. |
| 1 | WO | 0x0 | crfui<br>Write 1 to Clear Receive FIFO Underflow Interrupt. |
| 0 | WO | 0x0 | cci<br>Write 1 to Clear Combined Interrupt. |

**SPI_DMACR**

Address: Operational Base + offset (0x003C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | tde<br>1'b0: Transmit DMA disabled.<br>1'b1: Transmit DMA enabled. |
| 0 | RW | 0x0 | rde<br>1'b0: Receive DMA disabled.<br>1'b1: Receive DMA enabled. |

**SPI_DMATDLR**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5:0 | RW | 0x00 | tdl<br>This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and transmit DMA is enabled (DMACR[1] = 1). |

**SPI_DMARDLR**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5:0 | RW | 0x00 | rdl<br>This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1, and receive DMA is enabled(DMACR[0]=1). |

**SPI_VERSION**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00110002 | version<br>IP version |

**SPI_TIMEOUT**

Address: Operational Base + offset (0x004C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16 | RW | 0x0 | toe<br>Timeout enable.<br>1'b0: Timeout counter is inactive.<br>1'b1: Timeout counter will be active after the first rising edge of sclk_in. |
| 15:0 | RW | 0x0000 | tov<br>Timeout threshold value. If sclk_in keep inactive for a threshold time, timeout interrupt will be triggered. The timeout threshold time is TOV*pclk_perid*16. |

**SPI_BYPASS**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4 | RW | 0x0 | txcp<br>TX clock polarity.This bit is only valid in bypass mode.<br>1'b0: TX logic use raw SCLK.<br>1'b1: TX logic use inverted SCLK. |
| 3 | RW | 0x0 | rxcp<br>RX clock polarity.This bit is only valid in bypass mode.<br>1'b0: RX logic use raw SCLK.<br>1'b1: RX logic use inverted SCLK. |
| 2 | RW | 0x0 | end<br>Endian mode.This bit is only valid in bypass mode.<br>1'b0: Work in little endian mode.<br>1'b1: Work in big endian mode. |
| 1 | RW | 0x0 | fbm<br>First bit mode.This bit is only valid in bypass mode.<br>1'b0: First bit is LSB.<br>1'b1: First bit is MSB. |
| 0 | RW | 0x0 | byen<br>Bypass enable.<br>1'b0: Normal mode.<br>1'b1: Bypass mode, SPI serial/parallel convert logic is drive by SCLK. |

**SPI_TXDR**

Address: Operational Base + offset (0x0400)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | WO | 0x0000 | txdr<br>When it is written to, data are moved into the transmit FIFO. |

**SPI_RXDR**

Address: Operational Base + offset (0x0800)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RO | 0x0000 | rxdr<br>When the register is read, data in the receive FIFO is accessed. |

## 31.5 Interface Description

Table 31-1 SPI0 interface description

| Module Pin | Direction | Pin Name | IOMUX Setting |
|---|---|---|---|
| **IOMUX0** | | | |
| spi_sclk | I/O | I2S1_SDI1_M1/NPU_AVS/UART0_RTSN/PWM5_M1/SPI0_CLK_M0/PCIE30X4_CLKREQN_M0/SATA_CP_POD/GPIO0_C6_u | BUS_IOC_GPIO0C_IOMUX_SEL_H[11:8] = 4'h8<br>PMU2_IOC_GPIO0C_IOMUX_SEL_H[11:8] = 4'h8 |
| spi_mosi | I | PDM0_CLK0_M1/PWM1_M0/I2C2_SDA_M0/CAN0_RX_M0/SPI0_MOSI_M0/PCIE30X1_0_CLKREQN_M0/GPIO0_C0_d | BUS_IOC_GPIO0C_IOMUX_SEL_L[3:0] = 4'h8<br>PMU2_IOC_GPIO0C_IOMUX_SEL_L[3:0] = 4'h8 |
| spi_miso | O | I2S1_SDI2_M1/PDM0_SDI0_M1/I2C6_SDA_M0/UART1_RTSN_M2/PWM6_M0/SPI0_MISO_M0/PCIE30X4_WAKEN_M0/GPIO0_C7_d | BUS_IOC_GPIO0C_IOMUX_SEL_H[15:12] = 4'h8<br>PMU2_IOC_GPIO0C_IOMUX_SEL_H[15:12] = 4'h8 |
| spi_csn0 | I/O | I2S1_SDO0_M1/CPU_BIG0_AVS/I2C0_SCL_M2/UART0_CTSN/UART1_TX_M2/HDMI_RX_SDA_M0/SPI0_CS0_M0/PCIE30X2_CLKREQN_M0/HDMI_TX0_CEC_M1/GPIO0_D1_u | BUS_IOC_GPIO0D_IOMUX_SEL_L[7:4] = 4'h8<br>PMU2_IOC_GPIO0D_IOMUX_SEL_L[7:4] = 4'h8 |
| spi_csn1 | O | I2S1_LRCK_M1/PWM0_M0/I2C2_SCL_M0/CAN0_TX_M0/SPI0_CS1_M0/PCIE30X1_1_PERSTN_M0/GPIO0_B7_d | BUS_IOC_GPIO0B_IOMUX_SEL_H[15:12] = 4'h8<br>PMU2_IOC_GPIO0B_IOMUX_SEL_H[15:12] = 4'h8 |
| **IOMUX1** | | | |
| spi_sclk | I/O | CIF_D2/BT1120_D2/I2S1_LRCK_M0/PCIE30X1_1_PERSTN_M1/SPI0_CLK_M1/GPIO4_A2_d | BUS_IOC_GPIO4A_IOMUX_SEL_L[11:8] = 4'h8 |
| spi_mosi | I | CIF_D1/BT1120_D1/I2S1_SCLK_M0/PCIE30X1_1_WAKEN_M1/UART9_CTSN_M1/SPI0_MOSI_M1/GPIO4_A1_d | BUS_IOC_GPIO4A_IOMUX_SEL_L[7:4] = 4'h8 |
| spi_miso | O | CIF_D0/BT1120_D0/I2S1_MCLK_M0/PCIE30X1_1_CLKREQN_M1/UART9_RTSN_M1/SPI0_MISO_M1/GPIO4_A0_d | BUS_IOC_GPIO4A_IOMUX_SEL_L[3:0] = 4'h8 |
| spi_csn0 | I/O | CIF_HREF/BT1120_D8/I2S1_SDO1_M0/PCIE30X1_1_BUTTON_RSTN/I2C7_SCL_M3/UART8_RTSN_M0/PWM14_M1/SPI0_CS0_M1/CAN1_RX_M1/GPIO4_B2_u | BUS_IOC_GPIO4B_IOMUX_SEL_L[11:8] = 4'h8 |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| | | | |
|---|---|---|---|
| spi_csn1 | O | MIPI_CAMERA0_CLK_M0/SPDIF1_TX_M1/I2S1_SDO0_M0/PCIE30X1_0_BUTTON_RSTN/SATA2_ACT_LED_M0/I2C6_SCL_M3/UART8_RX_M0/SPI0_CS1_M1/GPIO4_B1_u | BUS_IOC_GPIO4B_IOMUX_SEL_L[7:4] = 4'h8 |
| **IOMUX2** | | | |
| spi_sclk | I/O | PDM1_CLK1_M1/PCIE30X1_0_WAKEN_M2/SATA0_ACT_LED_M1/UART4_TX_M2/SPI0_CLK_M2/GPIO1_B3_d | BUS_IOC_GPIO1B_IOMUX_SEL_L[15:12] = 4'h8 |
| spi_mosi | I | PDM1_SDI3_M1/PCIE30X4_PERSTN_M3/UART4_RX_M2/SPI0_MOSI_M2/GPIO1_B2_d | BUS_IOC_GPIO1B_IOMUX_SEL_L[11:8] = 4'h8 |
| spi_miso | O | PDM1_SDI2_M1/PCIE30X4_WAKEN_M3/SPI0_MISO_M2/GPIO1_B1_d | BUS_IOC_GPIO1B_IOMUX_SEL_L[7:4] = 4'h8 |
| spi_csn0 | I/O | PDM1_CLK0_M1/PCIE30X1_0_PERSTN_M2/UART7_RX_M2/SPI0_CS0_M2/GPIO1_B4_u | BUS_IOC_GPIO1B_IOMUX_SEL_H[3:0] = 4'h8 |
| spi_csn1 | O | PCIE30X1_0_CLKREQN_M2/UART7_TX_M2/SPI0_CS1_M2/GPIO1_B5_u | BUS_IOC_GPIO1B_IOMUX_SEL_H[7:4] = 4'h8 |
| **IOMUX3** | | | |
| spi_sclk | I/O | CIF_D15/PCIE30X2_WAKEN_M2/HDMI_RX_SDA_M1/I2C7_SDA_M2/UART9_CTSN_M2/PWM10_M2/SPI0_CLK_M3/GPIO3_D3_d | BUS_IOC_GPIO3D_IOMUX_SEL_L[15:12] = 4'h8 |
| spi_mosi | I | CIF_D14/PCIE30X2_CLKREQN_M2/HDMI_RX_SCL_M1/I2C7_SCL_M2/UART9_RTSN_M2/SPI0_MOSI_M3/GPIO3_D2_d | BUS_IOC_GPIO3D_IOMUX_SEL_L[11:8] = 4'h8 |
| spi_miso | O | CIF_D13/PCIE20X1_2_PERSTN_M0/HDMI_RX_CEC_M1/UART4_TX_M1/PWM9_M2/SPI0_MISO_M3/GPIO3_D1_d | BUS_IOC_GPIO3D_IOMUX_SEL_L[7:4] = 4'h8 |
| spi_csn0 | I/O | HDMI_TX0_HPD_M1/PCIE30X2_PERSTN_M2/HDMI_RX_HPDOUT_M1/MCU_JTAG_TCK_M1/UART9_RX_M2/SPI0_CS0_M3/GPIO3_D4_d | BUS_IOC_GPIO3D_IOMUX_SEL_H[3:0] = 4'h8 |
| spi_csn1 | O | PCIE30X4_BUTTON_RSTN/DP1_HPDIN_M0/MCU_JTAG_TMS_M1/UART9_TX_M2/PWM11_IR_M3/SPI0_CS1_M3/GPIO3_D5_d | BUS_IOC_GPIO3D_IOMUX_SEL_H[7:4] = 4'h8 |

*Notes: I=input, O=output, I/O=input/output, bidirectional.*

Table 31-2 SPI1 interface description

| Module Pin | Direction | Pin Name | IOMUX Setting |
|---|---|---|---|
| **IOMUX0** | | | |
| spi_sclk | I/O | GMAC0_TXEN/I2S2_LRCK_M0/I2C2_SDA_M1/UART1_RTSN_M0/SPI1_CLK_M0/GPIO2_C0_d | BUS_IOC_GPIO2C_IOMUX_SEL_L[3:0] = 4'h8 |
| spi_mosi | I | GMAC0_RXD1/I2C6_SDA_M2/UART9_TX_M0/SPI1_MOSI_M0/GPIO2_C2_d | BUS_IOC_GPIO2C_IOMUX_SEL_L[11:8] = 4'h8 |
| spi_miso | O | GMAC0_RXD0/I2C2_SCL_M1/UART1_CTSN_M0/SPI1_MISO_M0/GPIO2_C1_d | BUS_IOC_GPIO2C_IOMUX_SEL_L[7:4] = 4'h8 |
| spi_csn0 | I/O | ETH0_REFCLKO_25M/I2S2_SDI_M0/ | BUS_IOC_GPIO2C_IOMU |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| | | | |
|---|---|---|---|
| | | I2C6_SCL_M2/SPI1_CS0_M0/GPIO2_C3_d | X_SEL_L[15:12] = 4'h8 |
| spi_csn1 | O | GMAC0_PPSCLK/TEST_CLKOUT_M1/HDMI_TX1_CEC_M0/UART9_RX_M0/SPI1_CS1_M0/GPIO2_C4_d | BUS_IOC_GPIO2C_IOMUX_SEL_H[3:0] = 4'h8 |
| **IOMUX1** | | | |
| spi_sclk | I/O | GMAC1_PPSCLK/PCIE30X2_BUTTON_RSTN/UART7_RX_M1/SPI1_CLK_M1/GPIO3_C1_d | BUS_IOC_GPIO3C_IOMUX_SEL_L[7:4] = 4'h8 |
| spi_mosi | I | GMAC1_PTP_REF_CLK/HDMI_TX1_HPD_M1/I2C3_SCL_M1/SPI1_MOSI_M1/GPIO3_B7_d | BUS_IOC_GPIO3B_IOMUX_SEL_H[15:12] = 4'h8 |
| spi_miso | O | GMAC1_PPSTRIG/I2C3_SDA_M1/UART7_TX_M1/SPI1_MISO_M1/GPIO3_C0_d | BUS_IOC_GPIO3C_IOMUX_SEL_L[3:0] = 4'h8 |
| spi_csn0 | I/O | GMAC1_MDC/MIPI_TE0/I2C8_SCL_M4/UART7_RTSN_M1/PWM14_M0/SPI1_CS0_M1/GPIO3_C2_d | BUS_IOC_GPIO3C_IOMUX_SEL_L[11:8] = 4'h8 |
| spi_csn1 | O | GMAC1_MDIO/MIPI_TE1/I2C8_SDA_M4/UART7_CTSN_M1/PWM15_IR_M0/SPI1_CS1_M1/GPIO3_C3_d | BUS_IOC_GPIO3C_IOMUX_SEL_L[15:12] = 4'h8 |
| **IOMUX2** | | | |
| spi_sclk | I/O | I2S0_SDO3/I2S0_SDI2/PDM0_SDI2_M0/I2C1_SCL_M4/UART4_TX_M0/PWM0_M1/SPI1_CLK_M2/GPIO1_D2_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[11:8] = 4'h8 |
| spi_mosi | I | I2S0_SDO2/I2S0_SDI3/PDM0_SDI1_M0/I2C7_SDA_M0/UART6_RX_M2/SPI1_MOSI_M2/GPIO1_D1_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[7:4] = 4'h8 |
| spi_miso | O | I2S0_SDO1/I2C7_SCL_M0/UART6_TX_M2/SPI1_MISO_M2/GPIO1_D0_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[3:0] = 4'h8 |
| spi_csn0 | I/O | I2S0_SDI1/PDM0_SDI3_M0/I2C1_SDA_M4/UART4_RX_M0/PWM1_M1/SPI1_CS0_M2/GPIO1_D3_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[15:12] = 4'h8 |
| spi_csn1 | O | PDM0_SDI0_M0/SPI1_CS1_M2/GPIO1_D5_d | BUS_IOC_GPIO1D_IOMUX_SEL_H[7:4] = 4'h8 |

Table 31-3 SPI2 interface description

| Module Pin | Directon | Pin Name | IOMUX Setting |
|---|---|---|---|
| **IOMUX0** | | | |
| spi_sclk | I/O | HDMI_TX1_HPD_M0/SPI2_CLK_M0/GPIO1_A6_d | BUS_IOC_GPIO1A_IOMUX_SEL_H[11:8] = 4'h8 |
| spi_mosi | I | HDMI_TX0_HPD_M0/SPI2_MOSI_M0/GPIO1_A5_d | BUS_IOC_GPIO1A_IOMUX_SEL_H[7:4] = 4'h8 |
| spi_miso | O | HDMI_TX1_SCL_M2/SPI2_MISO_M0/GPIO1_A4_d | BUS_IOC_GPIO1A_IOMUX_SEL_H[3:0] = 4'h8 |
| spi_csn0 | I/O | PDM1_SDI0_M1/PCIE30X1_1_PERSTN_M2/PWM3_IR_M3/SPI2_CS0_M0/GPIO1_A7_u | BUS_IOC_GPIO1A_IOMUX_SEL_H[15:12] = 4'h8 |
| spi_csn1 | O | PDM1_SDI1_M1/PCIE30X4_CLKREQN_M3/SPI2_CS1_M0/GPIO1_B0_u | BUS_IOC_GPIO1B_IOMUX_SEL_L[3:0] = 4'h8 |
| **IOMUX1** | | | |
| spi_sclk | I/O | CIF_D6/BT1120_D6/I2S1_SDI1_M0/PCIE30X2_CLKREQN_M1/I2C5_SCL_M2/UART3_RX_M2/SPI2_CLK_M1/GPIO4_A6_d | BUS_IOC_GPIO4A_IOMUX_SEL_H[11:8] = 4'h8 |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| | | | |
|---|---|---|---|
| spi_mosi | I | CIF_D5/BT1120_D5/I2S1_SDI0_M0/PCIE30X1_0_PERSTN_M1/I2C3_SDA_M2/UART3_TX_M2/SPI2_MOSI_M1/GPIO4_A5_d | BUS_IOC_GPIO4A_IOMUX_SEL_H[7:4] = 4'h8 |
| spi_miso | O | CIF_D4/BT1120_D4/PCIE30X1_0_WAKEN_M1/I2C3_SCL_M2/UART0_RX_M2/SPI2_MISO_M1/GPIO4_A4_d | BUS_IOC_GPIO4A_IOMUX_SEL_H[3:0] = 4'h8 |
| spi_csn0 | I/O | CIF_D7/BT1120_D7/I2S1_SDI2_M0/PCIE30X2_WAKEN_M1/I2C5_SDA_M2/SPI2_CS0_M1/GPIO4_A7_d | BUS_IOC_GPIO4A_IOMUX_SEL_H[15:12] = 4'h8 |
| spi_csn1 | O | CIF_CLKIN/BT1120_CLKOUT/I2S1_SDI3_M0/PCIE30X2_PERSTN_M1/I2C6_SDA_M3/UART8_TX_M0/SPI2_CS1_M1/GPIO4_B0_d | BUS_IOC_GPIO4B_IOMUX_SEL_L[3:0] = 4'h8 |
| **IOMUX2** | | | |
| spi_sclk | I/O | SPI2_CLK_M2/SDMMC_PWREN/PMU_DEBUG/GPIO0_A5_d | PMU0_IOC_GPIO0A_IOMUX_SEL_H[7:4] = 4'h1 |
| spi_mosi | I | SPI2_MOSI_M2/I2C0_SDA_M0/GPIO0_A6_z | PMU0_IOC_GPIO0A_IOMUX_SEL_H[11:8] = 4'h1 |
| spi_miso | O | SPI2_MISO_M2/I2C0_SCL_M0/GPIO0_B3_z | PMU0_IOC_GPIO0B_IOMUX_SEL_L[15:12] = 4'h1 |
| spi_csn0 | I/O | SPI2_CS0_M2/I2C1_SDA_M1/PWM5_M0/UART0_TX_M1/GPIO0_B1_z | PMU0_IOC_GPIO0B_IOMUX_SEL_L[7:4] = 4'h1 |
| spi_csn1 | O | SPI2_CS1_M2/I2C1_SCL_M1/UART0_RX_M1/GPIO0_B0_z | PMU0_IOC_GPIO0B_IOMUX_SEL_L[3:0] = 4'h1 |

Table 31-4 SPI3 interface description

| Module Pin | Direction | Pin Name | IOMUX Setting |
|---|---|---|---|
| **IOMUX0** | | | |
| spi_sclk | I/O | GMAC0_TXER/I2C0_SDA_M1/UART7_CTSN_M0/PWM7_IR_M3/SPI3_CLK_M0/GPIO4_C6_d | BUS_IOC_GPIO4C_IOMUX_SEL_H[11:8] = 4'h8 |
| spi_mosi | I | GMAC0_MDIO/I2C0_SCL_M1/UART9_CTSN_M0/PWM6_M2/SPI3_MOSI_M0/GPIO4_C5_d | BUS_IOC_GPIO4C_IOMUX_SEL_H[7:4] = 4'h8 |
| spi_miso | O | GMAC0_MDC/I2C7_SDA_M1/UART9_RTSN_M0/PWM5_M2/SPI3_MISO_M0/GPIO4_C4_d | BUS_IOC_GPIO4C_IOMUX_SEL_H[3:0] = 4'h8 |
| spi_csn0 | I/O | GMAC0_RXDV_CRS/UART7_RTSN_M0/PWM2_M2/SPI3_CS0_M0/GPIO4_C2_d | BUS_IOC_GPIO4C_IOMUX_SEL_L[11:8] = 4'h8 |
| spi_csn1 | O | GMAC0_MCLKINOUT/I2S2_SDO_M0/I2C7_SCL_M1/PWM4_M1/SPI3_CS1_M0/GPIO4_C3_d | BUS_IOC_GPIO4C_IOMUX_SEL_L[15:12] = 4'h8 |
| **IOMUX1** | | | |
| spi_sclk | I/O | BT1120_D13/PCIE20X1_2_CLKREQN_M1/HDMI_TX0_SCL_M0/I2C5_SDA_M1/SPI3_CLK_M1/GPIO4_B7_u | BUS_IOC_GPIO4B_IOMUX_SEL_H[15:12] = 4'h8 |
| spi_mosi | I | BT1120_D12/PCIE30X4_PERSTN_M1/HDMI_RX_HPDOUT_M0/SATA0_ACT_LED_M0/I2C5_SCL_M1/PWM13_M1/SPI3_MOSI_M1/GPIO4_B6_d | BUS_IOC_GPIO4B_IOMUX_SEL_H[11:8] = 4'h8 |
| spi_miso | O | BT1120_D11/PCIE30X4_WAKEN_M1/HDMI_RX_CEC_M0/SATA1_ACT_LED_M0/UART9_RX_M1/PWM12_M1/SPI3_MISO_M1/GPIO4_B5_d | BUS_IOC_GPIO4B_IOMUX_SEL_H[7:4] = 4'h8 |
| spi_csn0 | I/O | BT1120_D14/PCIE20X1_2_WAKEN_ | BUS_IOC_GPIO4C_IOMU |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| | | | |
|---|---|---|---|
| | | M1/HDMI_TX0_SDA_M0/I2C8_SCL_M3/SPI3_CS0_M1/GPIO4_C0_u | X_SEL_L[3:0] = 4'h8 |
| spi_csn1 | O | BT1120_D15/SPDIF1_TX_M2/PCIE20X1_2_PERSTN_M1/HDMI_TX0_CEC_M0/I2C8_SDA_M3/PWM6_M1/SPI3_CS1_M1/GPIO4_C1_d | BUS_IOC_GPIO4C_IOMUX_SEL_L[7:4] = 4'h8 |
| **IOMUX2** | | | |
| spi_sclk | I/O | LITCPU_AVS/SPI3_CLK_M2/GPIO0_D3_u | BUS_IOC_GPIO0D_IOMUX_SEL_L[15:12] = 4'h8<br>PMU2_IOC_GPIO0D_IOMUX_SEL_L[15:12] = 4'h8 |
| spi_mosi | I | I2S1_SDO1_M1/I2C0_SDA_M2/UART1_RX_M2/HDMI_RX_SCL_M0/SPI3_MOSI_M2/PCIE30X2_WAKEN_M0/HDMI_TX1_CEC_M1/GPIO0_D2_u | BUS_IOC_GPIO0D_IOMUX_SEL_L[11:8] = 4'h8<br>PMU2_IOC_GPIO0D_IOMUX_SEL_L[11:8] = 4'h8 |
| spi_miso | O | I2S1_SDI3_M1/PDM0_SDI1_M1/I2C6_SCL_M0/UART1_CTSN_M2/PWM7_IR_M0/SPI3_MISO_M2/PCIE30X4_PERSTN_M0/GPIO0_D0_d | BUS_IOC_GPIO0D_IOMUX_SEL_L[3:0] = 4'h8 |
| spi_csn0 | I/O | I2S1_SDO2_M1/PDM0_SDI2_M1/PWM3_IR_M0/I2C1_SCL_M2/CAN2_RX_M1/HDMI_TX0_SDA_M1/SPI3_CS0_M2/PCIE30X2_PERSTN_M0/SATA_CPDET/GPIO0_D4_u | BUS_IOC_GPIO0D_IOMUX_SEL_H[3:0] = 4'h8<br>PMU2_IOC_GPIO0D_IOMUX_SEL_H[3:0] = 4'h8 |
| spi_csn1 | O | I2S1_SDO3_M1/CPU_BIG1_AVS/I2C1_SDA_M2/CAN2_TX_M1/HDMI_TX0_SCL_M1/SPI3_CS1_M2/SATA_MP_SWITCH/GPIO0_D5_u | BUS_IOC_GPIO0D_IOMUX_SEL_H[7:4] = 4'h8<br>PMU2_IOC_GPIO0D_IOMUX_SEL_H[7:4] = 4'h8 |
| **IOMUX3** | | | |
| spi_sclk | I/O | CIF_D12/PCIE20X1_2_WAKEN_M0/HDMI_TX0_SDA_M2/I2C5_SDA_M0/UART4_RX_M1/PWM8_M2/SPI3_CLK_M3/GPIO3_D0_u | BUS_IOC_GPIO3D_IOMUX_SEL_L[3:0] = 4'h8 |
| spi_mosi | I | CIF_D11/PCIE20X1_2_CLKREQN_M0/HDMI_TX0_SCL_M2/I2C5_SCL_M0/SPI3_MOSI_M3/GPIO3_C7_u | BUS_IOC_GPIO3C_IOMUX_SEL_H[15:12] = 4'h8 |
| spi_miso | O | CIF_D10/PCIE30X4_PERSTN_M2/HDMI_TX1_SCL_M1/SPI3_MISO_M3/GPIO3_C6_u | BUS_IOC_GPIO3C_IOMUX_SEL_H[11:8] = 4'h8 |
| spi_csn0 | I/O | CIF_D8/FSPI_CS0N_M2/PCIE30X4_CLKREQN_M2/HDMI_TX1_CEC_M2/CAN2_RX_M0/UART5_TX_M1/SPI3_CS0_M3/GPIO3_C4_u | BUS_IOC_GPIO3C_IOMUX_SEL_H[3:0] = 4'h8 |
| spi_csn1 | O | CIF_D9/FSPI_CS1N_M2/PCIE30X4_WAKEN_M2/HDMI_TX1_SDA_M1/CAN2_TX_M0/UART5_RX_M1/SPI3_CS1_M3/GPIO3_C5_u | BUS_IOC_GPIO3C_IOMUX_SEL_H[7:4] = 4'h8 |

Table 31-5 SPI4 interface description

| Module Pin | Dir | Pin Name | IOMUX Setting |
|---|---|---|---|
| **IOMUX0** | | | |
| spi_sclk | I/O | I2S0_MCLK/I2C6_SDA_M1/UART3_RTSN/PWM3_IR_M2/SPI4_CLK_M0/GPIO1_C2__d | BUS_IOC_GPIO1C_IOMUX_SEL_L[11:8] = 4'h8 |
| spi_mosi | I | I2C3_SCL_M0/UART3_TX_M0/SPI4_MOSI_M0/GPIO1_C1_z | BUS_IOC_GPIO1C_IOMUX_SEL_L[7:4] = 4'h8 |
| spi_miso | O | I2C3_SDA_M0/UART3_RX_M0/SPI4_ | BUS_IOC_GPIO1C_IOMU |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| | | | |
|---|---|---|---|
| | | MISO_M0/GPIO1_C0_z | X_SEL_L[3:0] = 4'h8 |
| spi_csn0 | I/O | I2S0_SCLK/I2C6_SCL_M1/UART3_CTSN/PWM7_IR_M2/SPI4_CS0_M0/GPIO1_C3_d | BUS_IOC_GPIO1C_IOMUX_SEL_L[15:12] = 4'h8 |
| spi_csn1 | O | PDM0_CLK1_M0/PCIE30PHY_DTB0/I2C2_SDA_M3/PWM11_IR_M2/SPI4_CS1_M0/GPIO1_C4_d | BUS_IOC_GPIO1C_IOMUX_SEL_H[3:0] = 4'h8 |
| **IOMUX1** | | | |
| spi_sclk | I/O | GMAC1_RXD2/SDIO_D2_M1/I2S3_LRCK/AUDDSM_LP/FSPI_D2_M2/UART8_TX_M1/SPI4_CLK_M1/GPIO3_A2_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[11:8] = 4'h8 |
| spi_mosi | I | GMAC1_TXD3/SDIO_D1_M1/I2S3_SCLK/AUDDSM_LN/FSPI_D1_M2/I2C6_SCL_M4/PWM11_IR_M0/SPI4_MOSI_M1/GPIO3_A1_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[7:4] = 4'h8 |
| spi_miso | O | GMAC1_TXD2/SDIO_D0_M1/I2S3_MCLK/FSPI_D0_M2/I2C6_SDA_M4/PWM10_M0/SPI4_MISO_M1/GPIO3_A0_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[3:0] = 4'h8 |
| spi_csn0 | I/O | GMAC1_RXD3/SDIO_D3_M1/I2S3_SDO/AUDDSM_RN/FSPI_D3_M2/UART8_RX_M1/SPI4_CS0_M1/GPIO3_A3_u | BUS_IOC_GPIO3A_IOMUX_SEL_L[15:12] = 4'h8 |
| spi_csn1 | O | GMAC1_TXCLK/SDIO_CMD_M1/I2S3_SDI/AUDDSM_RP/UART8_RTSN_M1/SPI4_CS1_M1/GPIO3_A4_d | BUS_IOC_GPIO3A_IOMUX_SEL_H[3:0] = 4'h8 |
| **IOMUX2** | | | |
| spi_sclk | I/O | VOP_POST_EMPTY/I2C4_SDA_M3/UART6_RTSN_M1/PWM0_M2/SPI4_CLK_M2/GPIO1_A2_d | BUS_IOC_GPIO1A_IOMUX_SEL_L[11:8] = 4'h8 |
| spi_mosi | I | PCIE30X1_1_WAKEN_M2/DP1_HPDIN_M2/SATA1_ACT_LED_M1/I2C2_SCL_M4/UART6_TX_M1/SPI4_MOSI_M2/GPIO1_A1_d | BUS_IOC_GPIO1A_IOMUX_SEL_L[7:4] = 4'h8 |
| spi_miso | O | PCIE30X1_1_CLKREQN_M2/DP0_HPDIN_M2/HDMI_RX_DEBUG6/I2C2_SDA_M4/UART6_RX_M1/SPI4_MISO_M2/GPIO1_A0_d | BUS_IOC_GPIO1A_IOMUX_SEL_L[3:0] = 4'h8 |
| spi_csn0 | I/O | HDMI_TX1_SDA_M2/I2C4_SCL_M3/UART6_CTSN_M1/PWM1_M2/SPI4_CS0_M2/GPIO1_A3_d | BUS_IOC_GPIO1A_IOMUX_SEL_L[15:12] = 4'h8 |

## 31.6 Application Notes

**Clock Ratios**

A summary of the frequency ratio restrictions between the bit-rate clock (sclk_out/sclk_in) and the SPI peripheral clock (spi_clk) are described as:

When SPI Controller works as master, the Fspi_clk>= 2 × (maximum Fsclk_out)

When SPI Controller works as slave, the Fspi_clk>= 4 × (maximum Fsclk_in)

**Master Transfer Flow**

When configured as a serial-master device, the SPI initiates and controls all serial transfers. The serial bit-rate clock, generated and controlled by the SPI, is driven out on the sclk_out line. When the SPI is disabled (SPI_ENR = 0), no serial transfers can occur and sclk_out is held in "inactive" state, as defined by the serial protocol under which it operates.

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

**Slave Transfer Flow**

When the SPI is configured as a slave device, all serial transfers are initiated and controlled by the serial bus master.

When the SPI serial slave is selected during configuration, it enables its txd data onto the serial bus. All data transfers to and from the serial slave are regulated on the serial clock line (sclk_in), driven from the serial-master device. Data are propagated from the serial slave on one edge of the serial clock line and sampled on the opposite edge.

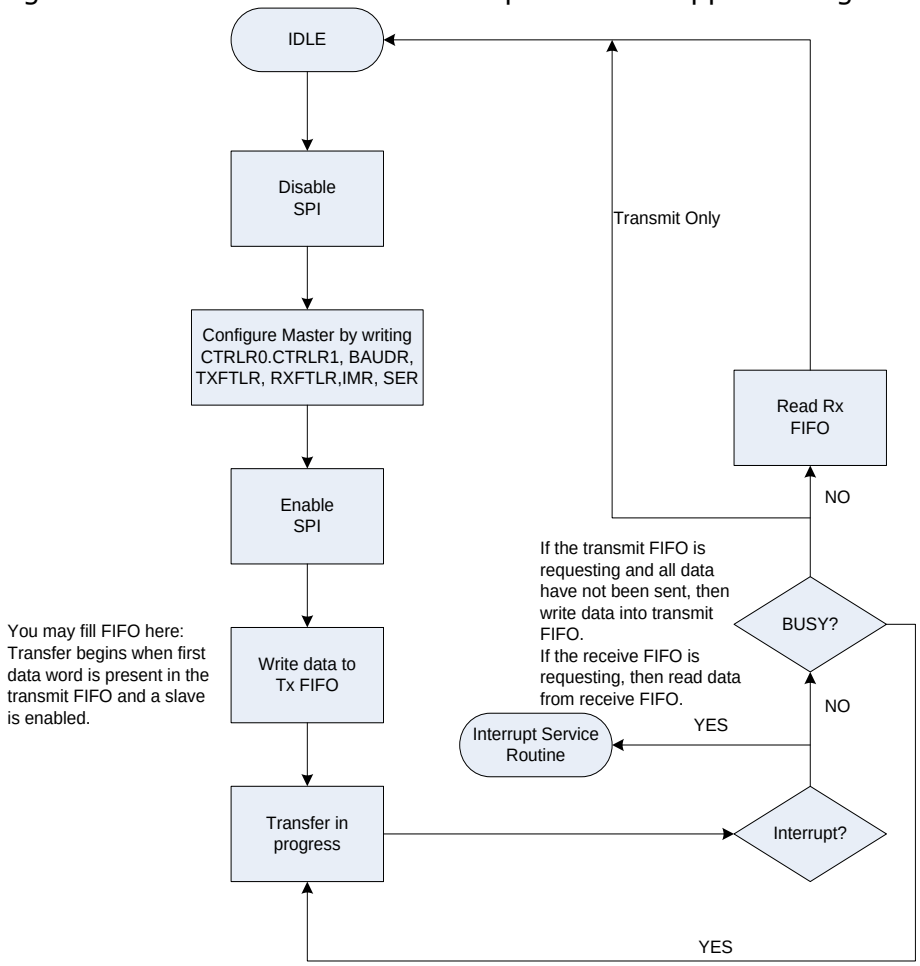



Fig. 31-7 SPI Master transfer flow diagram

Copyright 2022 © Rockchip Electronics Co., Ltd.

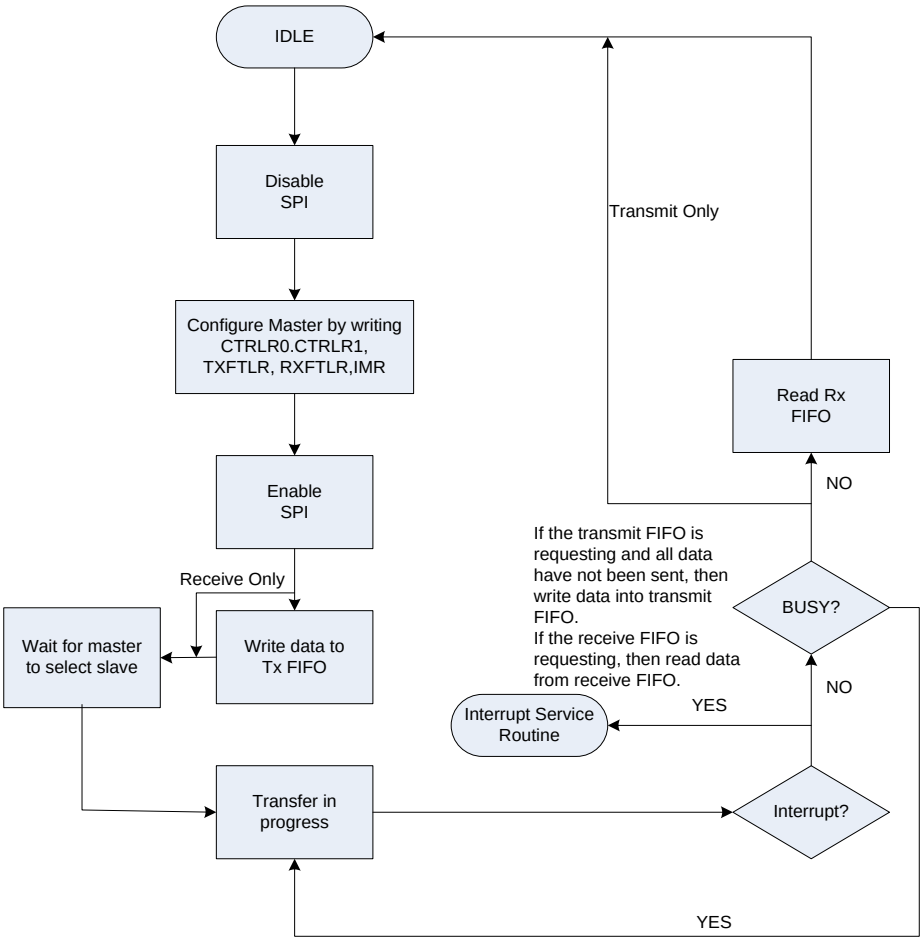



Fig. 31-8 SPI Slave transfer flow diagram

Copyright 2022 © Rockchip Electronics Co., Ltd.

# Chapter 32 SPINLOCK

## 32.1 Overview

The hardware spinlock used for spinlock status storage. All the CPU can access spinlock to get the lock status.

## 32.2 Block Diagram

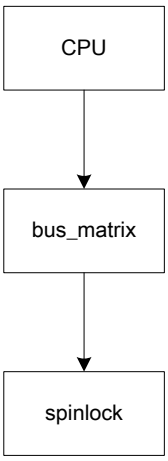



Fig. 32-1 Spinlock in System

## 32.3 Register Description

### 32.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

### 32.3.2 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| SPINLOCK_STATUS_N (range of n is 0~63) | 0x0+4*n | W | 0x00000000 | spinlock status controller register_n |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

### 32.3.3 Detail Register Description

**SPINLOCK_STATUS_N**

Address: Operational Base + offset (0x0000+4*n)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x000000 | reserved |
| 3:0 | RW | 0x0 | spinlock_status<br>when 4bits is 0, 4bits can be written with new value.<br>when 4bits is not 0, 4bits cannot be written.<br>when write data is 0x0000, 4bits clean to 0. |

Copyright 2022 © Rockchip Electronics Co., Ltd.

# Chapter 33 KEYLAD

## 33.1 Overview

KEYLAD is used to securely protect the transmission and operation of the KEY and ensure that other masters cannot access the KEY.
The KEYLAD supports following features:

- Support Link List Item (LLI) DMA transfer
- Support AES-128, AES-192, AES-256 encrypt & decrypt cipher
- Support DES & TDES cipher
- Support AES ECB/CBC/OFB/CFB mode
- Support SM4 ECB/CBC/OFB/CFB mode
- Support DES/TDES ECB/CBC/OFB/CFB mode
- Support for caching OTP or TRNG specific data and deriving it
- Support writing KEY Table data to some specific modules
- Support AES/SM4/DES/TDES lockstep error monitoring

## 33.2 Block Diagram

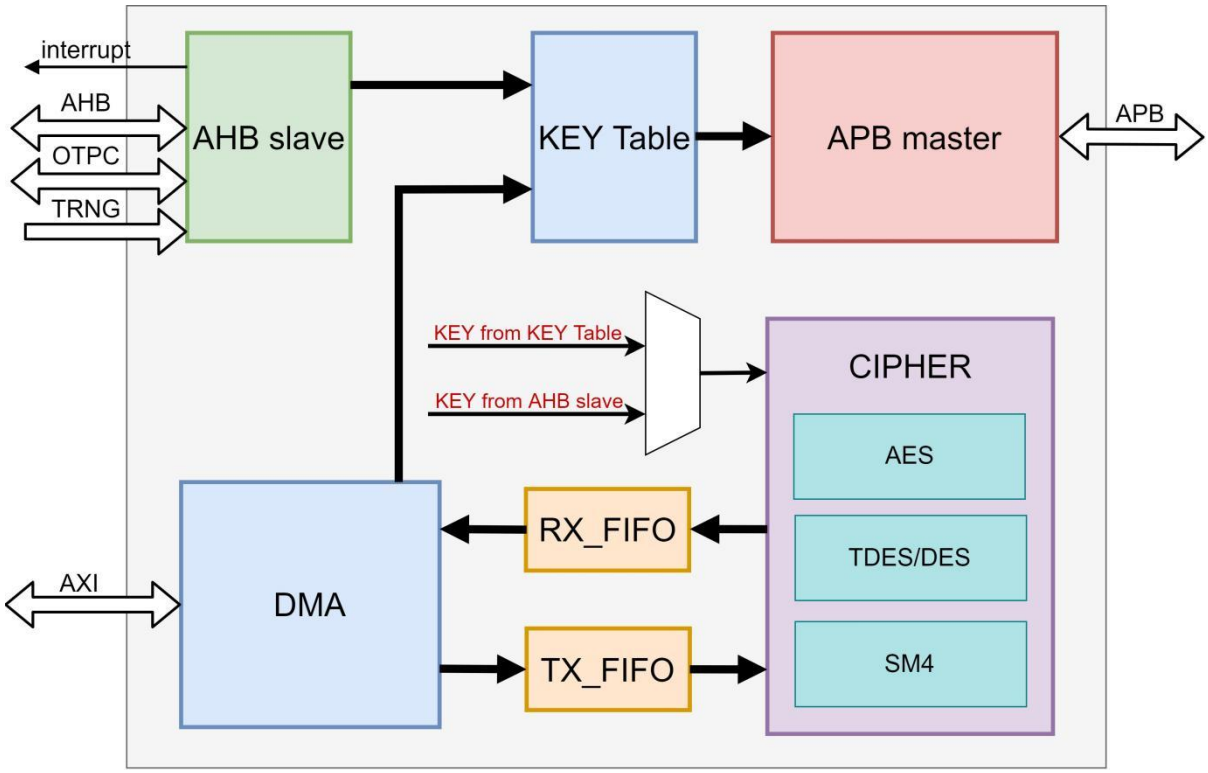



Fig. 33-1 KEYLAD Architecture

KEYLAD contains several modules: AHB_Slave, DMA, CIPHER, Key_table, APB_master.

**AHB_Slave**
AHB_Slave is used to configure registers. This module is in HCLK domain.

**DMA**
DMA is used to transfer data from external memory to RX_FIFO, or from TX_FIFO to KEY Table. DMA uses 64-bits AXI3 protocol with max burst length to 16. LLI transfer is also supported for performance and convenience consideration. This module is in ACLK domain.

**CIPHER**
CIPHER contains AES, SM4, DES/TDES engines. And it also supports various mode operations. The source data is either from RX_FIFO, or from other engine output. The result

Copyright 2022 © Rockchip Electronics Co., Ltd.

data is sending to TX_FIFO. This module is in CLK_CORE domain.

**KEY_Table**
The KEY table is used to store OTP KEY, TRNG data and CIPHER calculate result. KEY table's content can't be see by CPU. This module is in ACLK domain.

**APB_master**
APB_master is used to write data to module configurations that require secret configuration data. This APB_master is write-only APB master. This module is in PCLK domain.

# 33.3 Function Description

## 33.3.1 KEY Table

The KEY Table consists of 32 registers. The 32 word registers are numbered 0~31 one by one.

- Copy data into KEY Table

KEYLAD can copy 8 words OTP KEY or TRNG data to the KEY Table at one time. To copy data to KEY Table, the following steps should be followed:

1. Clear KEYLAD_SRC_NUM_DONE register;
2. Configure the KEYLAD_SRC_NUM_SEL register to select data source;
3. Configure OTPC or TRNG_S to generate data source for KEYLAD;
4. Waiting for KEYLAD_SRC_NUM_DONE register to set;
5. Configure the KEYLAD_OTP_COPY register to copy the data to the specified location in the KEY Table;
6. Waiting for KEYLAD_OTP_COPY register to clear indicates that data is written to KEY Table

- Internal data copy

KEYLAD can also copy the key table data internally, 8 words at a time, by configuring the KEYLAD_INTER_COPY register.

- Copy the KEY Table data to a specific module

KEYLAD has a set of write only APB interfaces, which can write the data in the KEY Table to SCRYPTO, SCRYAMBLE_KEY and HDCP_KEY, one word at a time. To write the data in the KEY Table to a specific module, the following steps should be followed:

1. Configure the KEYLAD_APB_PADDR register to select the destination address;
2. Configure KEYLAD_APB_PWDATA register to select word data corresponding to KEY Table;
3. Configure KEYLAD_APB_CMD register to start data writing;
4. Wait for the KEYLAD_APB_CMD register to clear, indicating that the data has been written to the destination.

## 33.3.2 KEY derivation

KEYLAD can derive the KEY in the KEY Table. If you need to use the data in the KEY Table as the KEY of the operation, you need to configure register KEYLAD_KEY_SEL.

# 33.4 Register Description

## 33.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

## 33.4.2 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| KEYLAD_CLK_CTL | 0x0000 | W | 0x00000001 | Clock Control Register |
| KEYLAD_RST_CTL | 0x0004 | W | 0x00000000 | Reset Control Register |
| KEYLAD_DMA_INT_EN | 0x0008 | W | 0x00000000 | DMA Interrupt Enable Register |
| KEYLAD_DMA_INT_ST | 0x000C | W | 0x00000000 | DMA Interrupt Status Register |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| KEYLAD_DMA_CTL | 0x0010 | W | 0x00000000 | DMA Control Register |
| KEYLAD_DMA_LLI_ADDR | 0x0014 | W | 0x00000000 | DMA LIST Start Address Register |
| KEYLAD_DMA_ST | 0x0018 | W | 0x00000000 | DMA Status Register |
| KEYLAD_DMA_STATE | 0x001C | W | 0x00000000 | DMA State Register |
| KEYLAD_DMA_LLI_RADDR | 0x0020 | W | 0x00000000 | DMA LLI Read Address Register |
| KEYLAD_DMA_SRC_RADDR | 0x0024 | W | 0x00000000 | DMA Source Data Read Address Register |
| KEYLAD_DMA_DST_WADDR | 0x0028 | W | 0x00000000 | DMA Destination Data Read Address Register |
| KEYLAD_DMA_ITEM_ID | 0x002C | W | 0x00000000 | DMA Descriptor ID Register |
| KEYLAD_FIFO_CTL | 0x0040 | W | 0x00000003 | FIFO Control Register |
| KEYLAD_BC_CTL | 0x0044 | W | 0x00000000 | Block Cipher Control Register |
| KEYLAD_CIPHER_ST | 0x004C | W | 0x00000000 | Cipher Status Register |
| KEYLAD_CIPHER_STATE | 0x0050 | W | 0x00000400 | Cipher Current State Register |
| KEYLAD_CH0_IV_0 | 0x0100 | W | 0x00000000 | iv 0 |
| KEYLAD_CH0_IV_1 | 0x0104 | W | 0x00000000 | iv 1 |
| KEYLAD_CH0_IV_2 | 0x0108 | W | 0x00000000 | iv 2 |
| KEYLAD_CH0_IV_3 | 0x010C | W | 0x00000000 | iv 3 |
| KEYLAD_CH0_KEY_0 | 0x0180 | W | 0x00000000 | key 0 |
| KEYLAD_CH0_KEY_1 | 0x0184 | W | 0x00000000 | key 1 |
| KEYLAD_CH0_KEY_2 | 0x0188 | W | 0x00000000 | key 2 |
| KEYLAD_CH0_KEY_3 | 0x018C | W | 0x00000000 | key 3 |
| KEYLAD_APB_CMD | 0x0450 | W | 0x00000000 | apb master command enable |
| KEYLAD_APB_PADDR | 0x0454 | W | 0x00000000 | apb paddr |
| KEYLAD_APB_PWDATA | 0x0458 | W | 0x00000000 | apb pwdata |
| KEYLAD_APB_PWRITE | 0x045C | W | 0x00000000 | apb pwrite |
| KEYLAD_INTER_COPY | 0x0608 | W | 0x00000000 | key table internal copy |
| KEYLAD_OTP_COPY | 0x060C | W | 0x00000000 | OTP key COPY |
| KEYLAD_KEY_SEL | 0x0610 | W | 0x00000000 | Operation key select |
| KEYLAD_LOCKSTEP_FLAG | 0x0618 | W | 0x00000000 | Lockstep mistake flag |
| KEYLAD_LOCKSTEP_EN | 0x061C | W | 0x00000000 | Lockstep check enable |
| KEYLAD_SRC_NUM_SEL | 0x0620 | W | 0x00000000 | Source key select |
| KEYLAD_SRC_NUM_DONE | 0x0624 | W | 0x00000000 | Source key cache flag |
| KEYLAD_AES_VERSION | 0x0680 | W | 0x00070033 | AES version code is 0x0007_0033 |
| KEYLAD_DES_VERSION | 0x0684 | W | 0x00030033 | DES version code is 0x0003_0033 |
| KEYLAD_SM4_VERSION | 0x0688 | W | 0x00000033 | SM4 version code is 0x0000_0033 |
| KEYLAD_HASH_VERSION | 0x068C | W | 0x00000000 | HASH version code is 0x0000_0000 |
| KEYLAD_HMAC_VERSION | 0x0690 | W | 0x00000000 | HMAC version code is 0x0000_0000 |
| KEYLAD_RNG_VERSION | 0x0694 | W | 0x02000000 | RNG version code is 0x0200_0000 |
| KEYLAD_PKA_VERSION | 0x0698 | W | 0x00000000 | PKA version code is 0x0000_0000 |
| KEYLAD_CRYPTO_VERSION | 0x06F0 | W | 0x02000003 | KEYLAD version code is 0x0200_0003 |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

### 33.4.3 Detail Registers Description

**KEYLAD_CLK_CTL**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16 | WO | 0x0 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x1 | auto_clkgate_en<br>KEYLAD will gate unused Block Cipher module automatically<br>1'b0: Disable<br>1'b1: Enable |

**KEYLAD_RST_CTL**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:19 | RO | 0x0000 | reserved |
| 18:16 | RW | 0x0 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | R/WSC | 0x0 | sw_rng_reset<br>Software set this bit to start a reset to TRNG module. After the reset is done, KEYLAD will clear this bit. |
| 0 | R/WSC | 0x0 | sw_cc_reset<br>Software set this bit to start a reset to Symmetric Cipher module. After the reset is done, KEYLAD will clear this bit. |

**KEYLAD_DMA_INT_EN**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RW | 0x0 | lockstep_int_en<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | zero_len_int_en<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | list_err_int_en<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | src_err_int_en<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | dst_err_int_en<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | src_item_done_int_en<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | dst_item_done_int_en<br>1'b0: Disable<br>1'b1: Enable |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | list_done_int_en<br>1'b0: Disable<br>1'b1: Enable |

**KEYLAD_DMA_INT_ST**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RW | 0x0 | lockstep_flag<br>1'b0: Nothing<br>1'b1: Indicate that KEYLAD was attacked |
| 6 | W1C | 0x0 | zero_len<br>1'b0: Nothing<br>1'b1: Indicate that DMA has met an 0 byte source transfer length in list descriptors. After the bit is read, the application should write 1 to clear this bit for next time use |
| 5 | RW | 0x0 | list_err<br>1'b0: Nothing<br>1'b1: Indicate that DMA has met an error response when transfer list descriptors. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use |
| 4 | W1C | 0x0 | src_err<br>1'b0: Nothing<br>1'b1: Indicate that DMA has met an error response when transfer source data. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use |
| 3 | W1C | 0x0 | dst_err<br>1'b0: Nothing<br>1'b1: Indicate that DMA has met an error response when transfer destination data. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use |
| 2 | W1C | 0x0 | src_item_done<br>1'b0: Nothing<br>1'b1: Indicate that DMA has completed a read transfers which the current list descriptor pointed to. After the bit is read, the application should write 1 to clear this bit for next time use |
| 1 | W1C | 0x0 | dst_item_done<br>1'b0: Nothing<br>1'b1: Indicate that DMA has completed a write transfers which the current list descriptor pointed to. After the bit is read, the application should write 1 to clear this bit for next time use |
| 0 | W1C | 0x0 | list_done<br>1'b0: Nothing<br>1'b1: Indicate that DMA has completed all the transfers which the list descriptors pointed to. After the bit is read, the application should write 1 to clear this bit for next time use |

**KEYLAD_DMA_CTL**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17:16 | WO | 0x0 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1'b0: Write access disable<br>1'b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | R/WSC | 0x0 | dma_restart<br>If DMA data for next stage is not ready, application could pause DMA by descriptor commands. DMA will stop prefetching next descriptor. The application could restart DMA by asserting this bit when DMA data for next state is ready. KEYLAD will continue with previous transfer, and clear the bit automatically. |
| 0 | R/WSC | 0x0 | dma_start<br>DMA asserts the bit to start DMA transfer, then KEYLAD will clear the bit automatically. |

**KEYLAD_DMA_LLI_ADDR**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | dma_lli_addr<br>When DMA_CTL start asserted, KEYLAD will read the address to get the 1'st descriptor. It should be 8-bytes align. We suggest dma_lli_addr 64-byte align for best performance consideration. |

**KEYLAD_DMA_ST**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RO | 0x0 | dma_busy<br>1'b0: DMA idle<br>1'b1: DMA busy |

**KEYLAD_DMA_STATE**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5:4 | RO | 0x0 | dma_lli_state<br>For debug use only<br>2'b00: IDLE STATE<br>2'b01: FETCH STATE<br>2'b10: WORK STATE<br>Others: Reserved |
| 3:2 | RO | 0x0 | dma_src_state<br>For debug use only<br>2'b00: IDLE STATE<br>2'b01: LOAD STATE<br>2'b10: WORK STATE<br>Others: Reserved |
| 1:0 | RO | 0x0 | dma_dst_state<br>For debug use only<br>2'b00: IDLE STATE<br>2'b01: LOAD STATE<br>2'b10: WORK STATE<br>Others: Reserved |

**KEYLAD_DMA_LLI_RADDR**

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | dma_lli_raddr<br>For debug use only<br>It indicates the current DMA LLI read address |

**KEYLAD_DMA_SRC_RADDR**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | dma_src_raddr<br>For debug use only<br>It indicates the current DMA source read address |

**KEYLAD_DMA_DST_WADDR**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | dma_dst_waddr<br>For debug use only<br>It indicates the current DMA destination write address |

**KEYLAD_DMA_ITEM_ID**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RO | 0x00 | dma_item_id<br>For debug use only<br>It indicates the current descriptor ID |

**KEYLAD_FIFO_CTL**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17:16 | WO | 0x0 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1’b0: Write access disable<br>1’b1: Write access enable |
| 15:2 | RO | 0x0000 | reserved |
| 1 | RW | 0x1 | dout_byteswap<br>1'b0: Little endian<br>1'b1: Big endian |
| 0 | RW | 0x1 | din_byteswap<br>1'b0: Little endian<br>1'b1: Big endian |

**KEYLAD_BC_CTL**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |
| 25:16 | WO | 0x000 | write_enable<br>Write enable for lower 16bits, each bit is individual<br>1’b0: Write access disable<br>1’b1: Write access enable |
| 15:10 | RO | 0x00 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9:8 | RW | 0x0 | bc_cipher_sel<br>2'b00: AES<br>2'b01: SM4<br>2'b10: DES<br>2'b11: TDES<br>Others: Reserved |
| 7:4 | RW | 0x0 | mode<br>For AES<br>4'h0: ECB<br>4'h1: CBC<br>4'h4: CFB<br>4'h5: OFB<br>Others: Reserved<br>For TDES/DES<br>4'h0: ECB<br>4'h1: CBC<br>4'h4: CFB<br>4'h5: OFB<br>Others: Reserved |
| 3:2 | RW | 0x0 | key_size<br>For AES<br>2'b00: 128 bit<br>2'b01: 192 bit<br>2'b10: 256 bit<br>2'b11: reserved<br>For TDES/DES, it is reserved |
| 1 | RW | 0x0 | decrypt<br>1'b0: Encrypt<br>1'b1: Decrypt |
| 0 | RW | 0x0 | bc_enable<br>1'b0: Disable<br>1'b1: Enable |

**KEYLAD_CIPHER_ST**

Address: Operational Base + offset (0x004C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2 | RO | 0x0 | otp_key_valid<br>Indicate if otp_key is valid<br>1'b0: Invalid<br>1'b1: Valid |
| 0 | RO | 0x0 | block_cipher_busy<br>1'b0: Idle<br>1'b1: Busy |

**KEYLAD_CIPHER_STATE**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:15 | RO | 0x00000 | reserved |
| 5:4 | RO | 0x0 | parallel_state<br>For debug use only<br>2'b00: IDLE State<br>2'b01: PRE State<br>2'b10: BULK State<br>Others: Reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1:0 | RO | 0x0 | serial_state<br>For debug use only<br>2'b00: IDLE State<br>2'b01: PRE State<br>2'b10: BULK State<br>2'b11: Reserved |

**KEYLAD_CH0_IV_0**

Address: Operational Base + offset (0x0100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ch0_iv_0<br>Channel 0 IV[127:96] |

**KEYLAD_CH0_IV_1**

Address: Operational Base + offset (0x0104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ch0_iv_1<br>Channel 0 IV[95:64] |

**KEYLAD_CH0_IV_2**

Address: Operational Base + offset (0x0108)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ch0_iv_2<br>Channel 0 IV[63:32] |

**KEYLAD_CH0_IV_3**

Address: Operational Base + offset (0x010C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ch0_iv_3<br>Channel 0 IV[31:0] |

**KEYLAD_CH0_KEY_0**

Address: Operational Base + offset (0x0180)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ch0_key_0<br>Channel 0 Key[127:96] |

**KEYLAD_CH0_KEY_1**

Address: Operational Base + offset (0x0184)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ch0_key_1<br>Channel 0 Key[95:64] |

**KEYLAD_CH0_KEY_2**

Address: Operational Base + offset (0x0188)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ch0_key_2<br>Channel 0 Key[63:32] |

**KEYLAD_CH0_KEY_3**

Address: Operational Base + offset (0x018C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ch0_key_3<br>Channel 0 Key[31:0] |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**KEYLAD_APB_CMD**

Address: Operational Base + offset (0x0450)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | apb_cmd_en<br>APB master command enable<br>1'b0: Disable<br>1'b1: Enable |

**KEYLAD_APB_PADDR**

Address: Operational Base + offset (0x0454)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | apb_paddr<br>Where to write out |

**KEYLAD_APB_PWDATA**

Address: Operational Base + offset (0x0458)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | apb_pwdata<br>Chose which 32 bits data in key table will be write out<br>0: Chose key_tab[31:0]<br>1: Chose key_tab[63:32]<br>n: Chose key_tab[(n*32+31):(n*32)] |

**KEYLAD_APB_PWRITE**

Address: Operational Base + offset (0x045C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | apb_pwrite<br>APB pwrite |

**KEYLAD_INTER_COPY**

Address: Operational Base + offset (0x0608)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | inter_copy_en<br>internal key copy enable<br>1'b0: Disable<br>1'b1: Enable |
| 30:29 | RO | 0x0 | reserved |
| 28:16 | RW | 0x0000 | inter_copy_des_addr<br>OTP key copy destination address (dword count). |
| 15:13 | RO | 0x0 | reserved |
| 12:0 | RW | 0x0000 | inter_copy_src_addr<br>OTP key copy source address (dword count). |

**KEYLAD_OTP_COPY**

Address: Operational Base + offset (0x060C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2 | RW | 0x0 | otp_key_copy_en<br>OTP key copy enable<br>1'b0: Disable<br>1'b1: Enable |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1:0 | RW | 0x0 | otp_key_copy_sel<br>OTP key copy select<br>2'b00: select the first 256 bits of key table<br>2'b01: select the second 256 bits of key table<br>2'b10: select the third 256 bits of key table<br>2'b11: select the fourth 256 bits of key table |

**KEYLAD_KEY_SEL**

Address: Operational Base + offset (0x0610)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | kl_high_sel<br>Swap high and low word pair keys per 64 bits.<br>1'b0: Nothing<br>1'b1: Swap |
| 30:0 | RW | 0x00000000 | kl_key_sel<br>Select the operation key.<br>31'h5a5a5a5a: Select key table key<br>Others: Select normal key |

**KEYLAD_LOCKSTEP_FLAG**

Address: Operational Base + offset (0x0618)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | lockstep_flag<br>lock step status<br>1'b0: No mistake<br>1'b1: Mistake happened |

**KEYLAD_LOCKSTEP_EN**

Address: Operational Base + offset (0x061C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | lockstep_en<br>Enable lockstep check<br>1'b0: Disable<br>1'b1: Enable |

**KEYLAD_SRC_NUM_SEL**

Address: Operational Base + offset (0x0620)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | src_num_sel<br>Select which key to write to the key table<br>1'b0: Select OTP value<br>1'b1: Select TRNG value |

**KEYLAD_SRC_NUM_DONE**

Address: Operational Base + offset (0x0624)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | W1C | 0x0 | src_num_done<br>Indicates whether the key reaches the port<br>1'b0: Not reach the port<br>1'b1: Reach the port |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**KEYLAD_AES_VERSION**

Address: Operational Base + offset (0x0680)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:19 | RO | 0x0000 | reserved |
| 18 | RO | 0x1 | aes256_flag<br>Whether the AES supports AES256<br>1'b0: No support<br>1'b1: Support |
| 17 | RO | 0x1 | aes192_flag<br>Whether the AES supports AES192<br>1'b0: No support<br>1'b1: Support |
| 16 | RO | 0x1 | aes128_flag<br>Whether the AES supports AES128<br>1'b0: No support<br>1'b1: Support |
| 15:11 | RO | 0x00 | reserved |
| 10 | RO | 0x0 | cbc-mac_flag<br>Whether the AES supports CBC-MAC<br>1'b0: No support<br>1'b1: Support |
| 9 | RO | 0x0 | cmac_flag<br>Whether the AES supports CMAC<br>1'b0: No support<br>1'b1: Support |
| 8 | RO | 0x0 | gcm_flag<br>Whether the AES supports GCM<br>1'b0: No support<br>1'b1: Support |
| 7 | RO | 0x0 | ccm_flag<br>Whether the AES supports CCM<br>1'b0: No support<br>1'b1: Support |
| 6 | RO | 0x0 | xts_flag<br>Whether the AES supports XTS<br>1'b0: No support<br>1'b1: Support |
| 5 | RO | 0x1 | ofb_flag<br>Whether the AES supports OFB<br>1'b0: No support<br>1'b1: Support |
| 4 | RO | 0x1 | cfb_flag<br>Whether the AES supports CFB<br>1'b0: No support<br>1'b1: Support |
| 3 | RO | 0x0 | ctr_flag<br>Whether the AES supports CTR<br>1'b0: No support<br>1'b1: Support |
| 2 | RO | 0x0 | cts_flag<br>Whether the AES supports CTS<br>1'b0: No support<br>1'b1: Support |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RO | 0x1 | cbc_flag<br>Whether the AES supports CBC<br>1'b0: No support<br>1'b1: Support |
| 0 | RO | 0x1 | ecb_flag<br>Whether the AES supports ECB<br>1'b0: No support<br>1'b1: Support |

**KEYLAD_DES_VERSION**

Address: Operational Base + offset (0x0684)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17 | RO | 0x1 | eee_flag<br>Whether the DES supports EEE mode<br>1'b0: No support<br>1'b1: Support |
| 16 | RO | 0x1 | tdes_flag<br>Whether the DES supports TDES<br>1'b0: No support<br>1'b1: Support |
| 15:6 | RO | 0x000 | reserved |
| 5 | RO | 0x1 | ofb_flag<br>Whether the DES supports OFB<br>1'b0: No support<br>1'b1: Support |
| 4 | RO | 0x1 | cfb_flag<br>Whether the DES supports CFB<br>1'b0: No support<br>1'b1: Support |
| 3:2 | RO | 0x0 | reserved |
| 1 | RO | 0x1 | cbc_flag<br>Whether the DES supports CBC<br>1'b0: No support<br>1'b1: Support |
| 0 | RO | 0x1 | ecb_flag<br>Whether the DES supports ECB<br>1'b0: No support<br>1'b1: Support |

**KEYLAD_SM4_VERSION**

Address: Operational Base + offset (0x0688)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:11 | RO | 0x000000 | reserved |
| 10 | RO | 0x0 | cbc-mac_flag<br>Whether the SM4 supports CBC-MAC<br>1'b0: No support<br>1'b1: Support |
| 9 | RO | 0x0 | cmac_flag<br>Whether the SM4 supports CMAC<br>1'b0: No support<br>1'b1: Support |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RO | 0x0 | gcm_flag<br>Whether the SM4 supports GCM<br>1'b0: No support<br>1'b1: Support |
| 7 | RO | 0x0 | ccm_flag<br>Whether the SM4 supports CCM<br>1'b0: No support<br>1'b1: Support |
| 6 | RO | 0x0 | xts_flag<br>Whether the SM4 supports XTS<br>1'b0: No support<br>1'b1: Support |
| 5 | RO | 0x1 | ofb_flag<br>Whether the SM4 supports OFB<br>1'b0: No support<br>1'b1: Support |
| 4 | RO | 0x1 | cfb_flag<br>Whether the SM4 supports CFB<br>1'b0: No support<br>1'b1: Support |
| 3 | RO | 0x0 | ctr_flag<br>Whether the SM4 supports CTR<br>1'b0: No support<br>1'b1: Support |
| 2 | RO | 0x0 | cts_flag<br>Whether the SM4 supports CTS<br>1'b0: No support<br>1'b1: Support |
| 1 | RO | 0x1 | cbc_flag<br>Whether the SM4 supports CBC<br>1'b0: No support<br>1'b1: Support |
| 0 | RO | 0x1 | ecb_flag<br>Whether the SM4 supports ECB<br>1'b0: No support<br>1'b1: Support |

**KEYLAD_HASH_VERSION**

Address: Operational Base + offset (0x068C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:9 | RO | 0x000000 | reserved |
| 8 | RO | 0x0 | sm3_flag<br>Whether the HASH supports SM3<br>1'b0: No support<br>1'b1: Support |
| 7 | RO | 0x0 | md5_flag<br>Whether the HASH supports MD5<br>1'b0: No support<br>1'b1: Support |
| 6 | RO | 0x0 | sha512-256_flag<br>Whether the HASH supports SHA-512/256<br>1'b0: No support<br>1'b1: Support |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RO | 0x0 | sha512-224_flag<br>Whether the HASH supports SHA-512/224<br>1'b0: No support<br>1'b1: Support |
| 4 | RO | 0x0 | sha512_flag<br>Whether the HASH supports SHA-512<br>1'b0: No support<br>1'b1: Support |
| 3 | RO | 0x0 | sha384_flag<br>Whether the HASH supports SHA-384<br>1'b0: No support<br>1'b1: Support |
| 2 | RO | 0x0 | sha256_flag<br>Whether the HASH supports SHA-256<br>1'b0: No support<br>1'b1: Support |
| 1 | RO | 0x0 | sha224_flag<br>Whether the HASH supports SHA-224<br>1'b0: No support<br>1'b1: Support |
| 0 | RO | 0x0 | sha1_flag<br>Whether the HASH supports SHA-1<br>1'b0: No support<br>1'b1: Support |

**KEYLAD_HMAC_VERSION**

Address: Operational Base + offset (0x0690)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4 | RO | 0x0 | sm3_flag<br>Whether the HMAC supports SM3<br>1'b0: No support<br>1'b1: Support |
| 3 | RO | 0x0 | md5_flag<br>Whether the HMAC supports MD5<br>1'b0: No support<br>1'b1: Support |
| 2 | RO | 0x0 | sha512_flag<br>Whether the HMAC supports SHA-512<br>1'b0: No support<br>1'b1: Support |
| 1 | RO | 0x0 | sha256_flag<br>Whether the HMAC supports SHA-256<br>1'b0: No support<br>1'b1: Support |
| 0 | RO | 0x0 | sha1_flag<br>Whether the HMAC supports SHA-1<br>1'b0: No support<br>1'b1: Support |

**KEYLAD_RNG_VERSION**

Address: Operational Base + offset (0x0694)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x02000000 | rng_version_code<br>RNG version code is 0x0200_0000. |

**KEYLAD_PKA_VERSION**

Address: Operational Base + offset (0x0698)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | pka_version_code<br>PKA version code is 0x0000_0000. |

**KEYLAD_CRYPTO_VERSION**

Address: Operational Base + offset (0x06F0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x02000003 | keylad_version_code<br>KEYLAD version code is 0x0200_0003. |

## 33.5 Application Note

- KEYLAD lockstep function refers to “Chapter CRYPTO”.
- The cipher function configuration of KEYLAD refers to “Chapter CRYPTO”.
- When performing KEY derivation, you need to configure the dout_byteswap bit segment of KEYLAD_FIFO_CTL to '0'.
- When KEYLAD copies the data in KEY Table to SCRYPTO, the base address of SCRYPTO shall be regarded as 0xfe420000.

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

# Chapter 34 Share Memory

## 34.1 Overview

The Share Memory is a general memory module which can be accessed by several masters at the same time. And it can be programmed through the APB Slave interface.
The Share Memory supports the following features:

- Support four AXI Slave interfaces with 256 bits data bus width
- Support total 1024KB memory comprised of four memory blocks
- Support shut down and deep sleep mode for each memory block
- Support auto clock gating
- Support weighted Round-Robin arbiter
- Support APB Slave interface for software configuration and status query

## 34.2 Block Diagram

The following figure shows the block diagram of Share Memory.

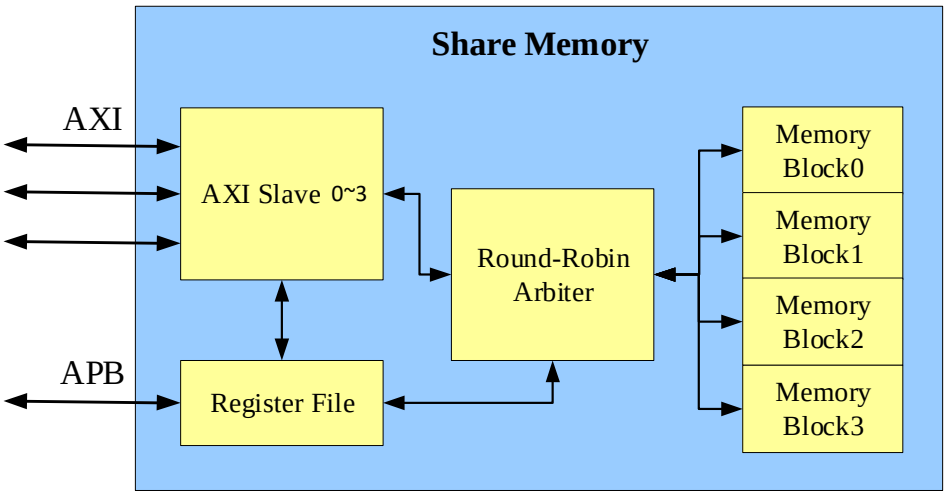



Fig. 34-1 Block Diagram of Share Memory

## 34.3 Function Description

### 34.3.1 Memory Access

There are four memory blocks, and each 256KB block consists of four SRAM banks. That is, the valid address range of the Share Memory is 0xFF000000~0xFF0FFFFF, and the base address of the Memory Block0~3 is 0xFF000000/0xFF040000/0xFF080000/0xFF0C0000.

### 34.3.2 Round-Robin Arbiter

In order to program the priority attribute for every AXI Slave interface, you should configure the following registers of the internal Round-Robin arbiter: SHAREMEM_RRA_SLT, SHAREMEM_RRA_WEIGHT, and SHAREMEM_RRA_SLT_PRI, and then enable the configuration by writing 1 to SHAREMEM_CTRL.cfg_load_en.

## 34.4 Register Description

This section describes the control/status registers of the design. Software should read and write these registers using 32-bits accesses.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| SHAREMEM_RRA_SLT | 0x0000 | W | 0x76543210 | RRA slot assignment register |
| SHAREMEM_RRA_WEIGHT | 0x0008 | W | 0x00000000 | RRA arbitration weight register |
| SHAREMEM_RRA_SLT_PRI | 0x0010 | W | 0x00000000 | RRA slot priority register |
| SHAREMEM_CTRL | 0x0020 | W | 0x00000000 | Global control register |
| SHAREMEM_STATUS | 0x0024 | W | 0x00000000 | Status register |

Copyright 2022 © Rockchip Electronics Co., Ltd.

*Notes: Size: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

### 34.4.1 Detail Register Description

**SHAREMEM_RRA_SLT**

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RW | 0x7 | req_slot7<br>Initial assignment to slot 7.<br>4'h0: AXIS0 Read requester<br>4'h1: AXIS0 Write requester<br>4'h2: AXIS1 Read requester<br>4'h3: AXIS1 Write requester<br>4'h4: AXIS2 Read requester<br>4'h5: AXIS2 Write requester<br>4'h6: AXIS3 Read requester<br>4'h7: AXIS3 Write requester<br>Others: Reserved |
| 27:24 | RW | 0x6 | req_slot6<br>Initial assignment to slot 6.<br>4'h0: AXIS0 Read requester<br>4'h1: AXIS0 Write requester<br>4'h2: AXIS1 Read requester<br>4'h3: AXIS1 Write requester<br>4'h4: AXIS2 Read requester<br>4'h5: AXIS2 Write requester<br>4'h6: AXIS3 Read requester<br>4'h7: AXIS3 Write requester<br>Others: Reserved |
| 23:20 | RW | 0x5 | req_slot5<br>Initial assignment to slot 5.<br>4'h0: AXIS0 Read requester<br>4'h1: AXIS0 Write requester<br>4'h2: AXIS1 Read requester<br>4'h3: AXIS1 Write requester<br>4'h4: AXIS2 Read requester<br>4'h5: AXIS2 Write requester<br>4'h6: AXIS3 Read requester<br>4'h7: AXIS3 Write requester<br>Others: Reserved |
| 19:16 | RW | 0x4 | req_slot4<br>Initial assignment to slot 4.<br>4'h0: AXIS0 Read requester<br>4'h1: AXIS0 Write requester<br>4'h2: AXIS1 Read requester<br>4'h3: AXIS1 Write requester<br>4'h4: AXIS2 Read requester<br>4'h5: AXIS2 Write requester<br>4'h6: AXIS3 Read requester<br>4'h7: AXIS3 Write requester<br>Others: Reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:12 | RW | 0x3 | req_slot3<br>Initial assignment to slot 3.<br>4'h0: AXIS0 Read requester<br>4'h1: AXIS0 Write requester<br>4'h2: AXIS1 Read requester<br>4'h3: AXIS1 Write requester<br>4'h4: AXIS2 Read requester<br>4'h5: AXIS2 Write requester<br>4'h6: AXIS3 Read requester<br>4'h7: AXIS3 Write requester<br>Others: Reserved |
| 11:8 | RW | 0x2 | req_slot2<br>Initial assignment to slot 2.<br>4'h0: AXIS0 Read requester<br>4'h1: AXIS0 Write requester<br>4'h2: AXIS1 Read requester<br>4'h3: AXIS1 Write requester<br>4'h4: AXIS2 Read requester<br>4'h5: AXIS2 Write requester<br>4'h6: AXIS3 Read requester<br>4'h7: AXIS3 Write requester<br>Others: Reserved |
| 7:4 | RW | 0x1 | req_slot1<br>Initial assignment to slot 1.<br>4'h0: AXIS0 Read requester<br>4'h1: AXIS0 Write requester<br>4'h2: AXIS1 Read requester<br>4'h3: AXIS1 Write requester<br>4'h4: AXIS2 Read requester<br>4'h5: AXIS2 Write requester<br>4'h6: AXIS3 Read requester<br>4'h7: AXIS3 Write requester<br>Others: Reserved |
| 3:0 | RW | 0x0 | req_slot0<br>Initial assignment to slot 0.<br>4'h0: AXIS0 Read requester<br>4'h1: AXIS0 Write requester<br>4'h2: AXIS1 Read requester<br>4'h3: AXIS1 Write requester<br>4'h4: AXIS2 Read requester<br>4'h5: AXIS2 Write requester<br>4'h6: AXIS3 Read requester<br>4'h7: AXIS3 Write requester<br>Others: Reserved |

**SHAREMEM_RRA_WEIGHT**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |
| 30:28 | RW | 0x0 | weight_axis3wr<br>AXIS3 write port arbitration weight |
| 27 | RO | 0x0 | reserved |
| 26:24 | RW | 0x0 | weight_axis3rd<br>AXIS3 read port arbitration weight |
| 23 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 22:20 | RW | 0x0 | weight_axis2wr<br>AXIS2 write port arbitration weight |
| 19 | RO | 0x0 | reserved |
| 18:16 | RW | 0x0 | weight_axis2rd<br>AXIS2 read port arbitration weight |
| 15 | RO | 0x0 | reserved |
| 14:12 | RW | 0x0 | weight_axis1wr<br>AXIS1 write port arbitration weight |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x0 | weight_axis1rd<br>AXIS1 read port arbitration weight |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x0 | weight_axis0wr<br>AXIS0 write port arbitration weight |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x0 | weight_axis0rd<br>AXIS0 read port arbitration weight |

**SHAREMEM_RRA_SLT_PRI**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:12 | RO | 0x00000 | reserved |
| 11:8 | RW | 0x0 | rra_firstslot_region3<br>The number of the lowest priority slot in the RRA priority region 3 |
| 7:4 | RW | 0x0 | rra_firstslot_region2<br>The number of the lowest priority slot in the RRA priority region 2 |
| 3:0 | RW | 0x0 | rra_firstslot_region1<br>The number of the lowest priority slot in the RRA priority region 1 |

**SHAREMEM_CTRL**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6:2 | RW | 0x00 | addr_round_en<br>AXIS0~AXIS3 address round enable, high active.<br>[0] for slave0, [1] for slave1 and so on. |
| 1 | RW | 0x0 | free_run_mode<br>Free run mode enable.<br>1'b0: Low power mode<br>1'b1: Free run mode |
| 0 | R/W SC | 0x0 | cfg_load_en<br>RRA configuration load enable, high active. |

**SHAREMEM_STATUS**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27:24 | R/W SC | 0x0 | axislv_addr_round<br>AXI slave0~slave3 address round status. [0] for slave0, [1] for slave1 and so on. |
| 23:20 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19:16 | R/WSC | 0x0 | axislv_wresperr<br>AXI slave write response error indication. [0] for slave0, [1] for slave1 and so on.<br>1'b1: Response error<br>1'b0: Response ok |
| 15:12 | RO | 0x0 | reserved |
| 11:8 | R/WSC | 0x0 | axislv_rresperr<br>AXI slave read response error indication. [0] for slave0, [1] for slave1 and so on.<br>1'b1: Response error<br>1'b0: Response ok |
| 7:4 | RO | 0x0 | reserved |
| 3:0 | RO | 0x0 | axislv_active<br>AXI slave status. [0] for slave0, [1] for slave1 and so on.<br>1'b1: Active<br>1'b0: Inactive |

# 34.5 Application Notes

## 34.5.1 Power Control Flow

Share Memory supports shutdown and deep sleep mode for each memory block, which can be controlled by software.

**1. Enter Shut Down Mode Flow:**

(1) Select shut down mode for specified memory block:

Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[0] to 1 for block 0
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[1] to 1 for block 1
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[2] to 1 for block 2
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[3] to 1 for block 3

(2) Enable shut down mode for specified memory block:

Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[8] to 1 for block 0
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[9] to 1 for block 1
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[10] to 1 for block 2
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[11] to 1 for block 3

(3) Check memory power state:

Query until PMU_SUBMEM_PWR_GATE_STS bit[0] equals to 1, to make sure block 0 enters shut down mode
Query until PMU_SUBMEM_PWR_GATE_STS bit[1] equals to 1, to make sure block 1 enters shut down mode
Query until PMU_SUBMEM_PWR_GATE_STS bit[2] equals to 1, to make sure block 2 enters shut down mode
Query until PMU_SUBMEM_PWR_GATE_STS bit[3] equals to 1, to make sure block 3 enters shut down mode

**2. Exit Shut Down Mode Flow:**

(1) Disable shut down mode for specified memory block:

Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[8] to 0 for block 0
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[9] to 0 for block 1
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[10] to 0 for block 2
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[11] to 0 for block 3

(2) Deselect shut down mode for specified memory block:

Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[0] to 0 for block 0
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[1] to 0 for block 1
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[2] to 0 for block 2
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[3] to 0 for block 3

(3) Check memory power state:

Query until PMU_SUBMEM_PWR_GATE_STS bit[0] equals to 0, to make sure block 0 exits

Copyright 2022 © Rockchip Electronics Co., Ltd.

shut down mode
Query until PMU_SUBMEM_PWR_GATE_STS bit[1] equals to 0, to make sure block 1 exits shut down mode
Query until PMU_SUBMEM_PWR_GATE_STS bit[2] equals to 0, to make sure block 2 exits shut down mode
Query until PMU_SUBMEM_PWR_GATE_STS bit[3] equals to 0, to make sure block 3 exits shut down mode

**3. Enter Deep Sleep Mode Flow:**

(1) Select deep sleep mode for specified memory block:
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[4] to 1 for block 0
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[5] to 1 for block 1
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[6] to 1 for block 2
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[7] to 1 for block 3

(2) Enable deep sleep mode for specified memory block:
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[12] to 1 for block 0
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[13] to 1 for block 1
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[14] to 1 for block 2
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[15] to 1 for block 3

(3) Check memory power state:
Query until PMU_SUBMEM_PWR_GATE_STS bit[0] equals to 1, to make sure block 0 enters deep sleep mode
Query until PMU_SUBMEM_PWR_GATE_STS bit[1] equals to 1, to make sure block 1 enters deep sleep mode
Query until PMU_SUBMEM_PWR_GATE_STS bit[2] equals to 1, to make sure block 2 enters deep sleep mode
Query until PMU_SUBMEM_PWR_GATE_STS bit[3] equals to 1, to make sure block 3 enters deep sleep mode

**4. Exit Deep Sleep Mode Flow:**

(1) Disable deep sleep mode for specified memory block:
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[12] to 0 for block 0
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[13] to 0 for block 1
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[14] to 0 for block 2
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[15] to 0 for block 3

(2) Deselect deep sleep mode for specified memory block:
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[4] to 0 for block 0
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[5] to 0 for block 1
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[6] to 0 for block 2
Set PMU_SUBMEM_PWR_GATE_SFTCON0 bit[7] to 0 for block 3

(3) Check memory power state:
Query until PMU_SUBMEM_PWR_GATE_STS bit[0] equals to 0, to make sure block 0 exits deep sleep mode
Query until PMU_SUBMEM_PWR_GATE_STS bit[1] equals to 0, to make sure block 1 exits deep sleep mode
Query until PMU_SUBMEM_PWR_GATE_STS bit[2] equals to 0, to make sure block 2 exits deep sleep mode
Query until PMU_SUBMEM_PWR_GATE_STS bit[3] equals to 0, to make sure block 3 exits deep sleep mode

## 34.5.2 Other Notes

- If SHAREMEM_CTRL.addr_round_en is set to 1, you can access the Share Memory using out-of-bounds address such as 0xFF100000~0xFF1FFFFF as the mirror address of 0xFF000000~0xFF0FFFFF, and there is no error response.
- If SHAREMEM_CTRL.addr_round_en is set to 0, when the read or write address exceeds the address boundary, the AXI bus will respond a read or write error. You can read the response status from the register SHAREMEM_STATUS.
- If configure SHAREMEM_CTRL.free_run_mode to 1, internal auto clock gating will be

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

turned off.

- The programmable slot0 always has the highest priority in the Memory Block0, which is mentioned as the RRA priority region 0.
- The register bit SHAREMEM_CTRL.cfg_load_en is auto clear, so the readvalue is always 0.

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

# Chapter 35 DECOM

## 35.1 Overview

DECOM can decompress compressed files in GZIP, LZ4, DEFALTE and ZLIB formats. DECOM controller supports the following features:

- Support for decompressing GZIP files
- Support for decompressing LZ4 files, including the General Structure of LZ4 Frame format and the Legacy Frame format
- Support for decompressing data in DEFLATE format
- Support for decompressing data in ZLIB format
- There is a 32bit APB slave interface for configuring decompression parameters and querying register status
- There is a 128-bit AXI master interface for reading compressed data and outputting decompressed data. The AXI master interface supports burst 4/8/16 and single transmissions
- Support one internal 128-bit wide and 64-location deep FIFO(RX_FIFO) for caching source compressed data
- Support one internal 24-bit wide and 64-location deep FIFO(HF_FIFO) for caching intermediate data during decompression
- Built-in a 32KB two-port RAM for storing decompressed data
- Support complete interrupt and error interrupt output
- Support Hash32 check in LZ4 decompression process
- Support the limit_size function of the decompressed data to prevent the memory from being maliciously destroyed during the decompression process
- Support software to stop the decompression process

## 35.2 Block Diagram

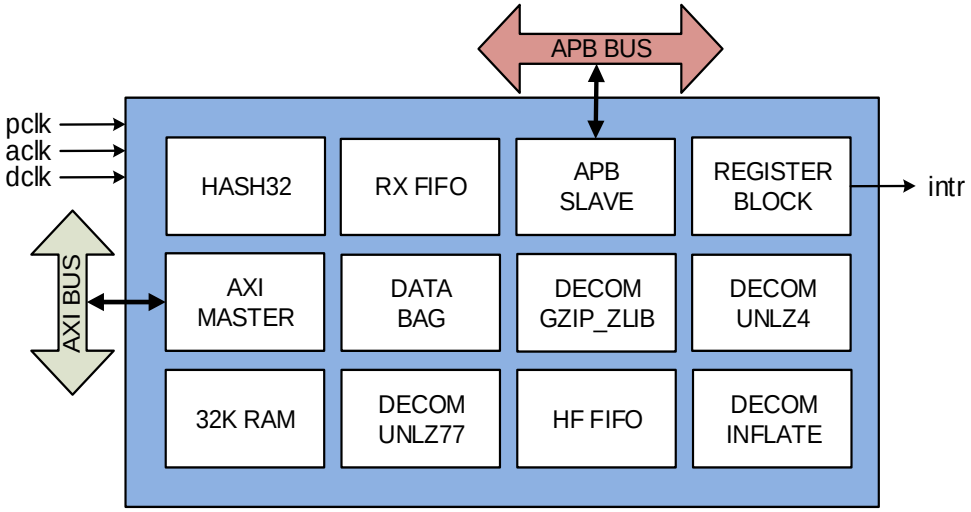



Fig. 35-1 DECOM Block Diagram

## 35.3 Function Description

### 35.3.1 Module Introduction

#### 35.3.1.1 APB INTERFACE

The APB slave interface is used for registers configuration, decompression file parameter reading and interrupt status query, etc.

#### 35.3.1.2 AXI MASTER INTERFACE

The AXI master interface is used to read compressed file data from external storage into the RX_FIFO and output the decompressed data to external storage. When decompressing the

Copyright 2022 © Rockchip Electronics Co., Ltd.

LZ4 file, it is also used to read back data with a matching distance of more than 32 KB from the external storage.

#### 35.3.1.3 RX_FIFO

The RX_FIFO is used to buffer the source compressed file data read back through the AXI master interface. The RX_FIFO is an asynchronous FIFO, the write interface uses aclk, and the read interface uses dclk.

#### 35.3.1.4 Data Bag

The Data Bag reads and bites the data in the RX_FIFO, and extracts the corresponding number of bits according to the needs of the decompression module.

#### 35.3.1.5 UNLZ4 Module

The UNLZ4 module performs file header parsing on the compressed file of LZ4 format, and decompresses the data into LZ77 format (match length-matching distance) data pair or character data, and stores it in HF_FIFO.

#### 35.3.1.6 GZIP_ZLIB

The GZIP_ZLIB module is used to perform file header and file end parsing for compressed files in GZIP format and compressed data in ZLIB format, and the compressed data portion is decompressed by the INFLATE module. The GZIP or ZLIB decompression mode can be configured by configuring the CTRL register.

#### 35.3.1.7 INFLATE Module

INFLATE Module is used to decompress compressed files in DEFLATE format, implement static/dynamic huffman decoding, decompress compressed data in DEFLATE format into LZ77 format (match length-match distance) data pairs or character data, and store them in HF_FIFO.

#### 35.3.1.8 HF_FIFO

The HF_FIFO is used to buffer the LZ77 format (match length-match distance) data pair or character data decompressed by the UNLZ4 module and the INFLATE module, and wait for the UNLZ77 module to further decompress the intermediate data. The HF_FIFO is an asynchronous FIFO, the write interface uses dclk, and the read interface uses aclk.

#### 35.3.1.9 UNLZ77 Module

UNLZ77 is used to implement LZ77 decoding and store the decompressed data in 32K RAM. When the matching distance is less than 32k byte, matching replication is performed in 32K RAM. When the matching distance is greater than 32k byte, the AXI master interface is controlled to perform matching replication in the external storage.

#### 35.3.1.10 32K-RAM

The 32K RAM is used to buffer the decompressed data. During the decompression process, the UNLZ77 module also performs read access to the RAM to complete the data matching.

#### 35.3.1.11 HASH32 Module

In the process of decompressing the LZ4 compressed file, the HASH32 module is used to calculate the hash32 check value of the file header, data block and decompressed data.

#### 35.3.1.12 Interface and Clock

The 32-bit APB Slave interface in DECOM is used for register configuration and interrupt status query interface, using pclk as the interface clock.

DECOM uses 128bit AXI master interface to realize the functions of reading the data to be compressed, decompressing the data output and decompressing LZ4 external matching data; it should be noted that the AXI master interface supports Single and Burst transmission, which only supports incr4, incr8 and Incr16 three transmission types, does not support Wrap transmission. DECOM automatically configures the burst type according to the length of the transmitted data and the starting address. The software configuration is not supported to select the burst type.

DECOM has three sets of clock and reset inputs, pclk and presetn, dclk and drstn, aclk and aresetn. Among them pclk and aclk are APB and AXI bus clocks respectively, and dclk is decompression clock.

Copyright 2022 © Rockchip Electronics Co., Ltd.

### 35.3.2 Data Flow

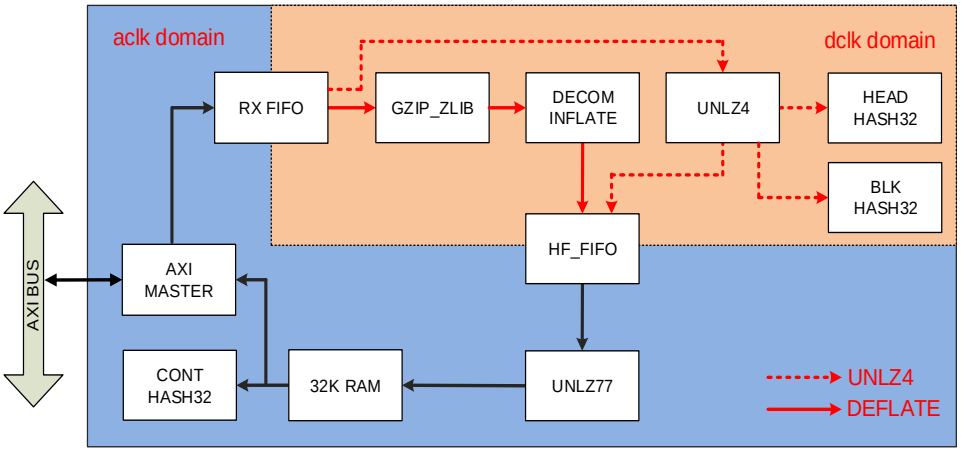



Fig. 35-2 DECOM Data Flow

## 35.4 Register Description

### 35.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

### 35.4.2 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| DECOM_CTRL | 0x0000 | W | 0x00000000 | Control Register |
| DECOM_ENR | 0x0004 | W | 0x00000000 | Enable Register |
| DECOM_RADDR | 0x0008 | W | 0x00000000 | Read Address |
| DECOM_WADDR | 0x000C | W | 0x00000000 | Write Address |
| DECOM_UDDSL | 0x0010 | W | 0xFFFFFFFF | Undecompressed Data Size |
| DECOM_UDDSH | 0x0014 | W | 0xFFFFFFFF | Undecompressed Data Size |
| DECOM_TXTHR | 0x0018 | W | 0x00000100 | Transmit Threshold Level |
| DECOM_SLEN | 0x0020 | W | 0x00000000 | INFLATE Store Length |
| DECOM_STAT | 0x0024 | W | 0x00000000 | DECOM Status Register |
| DECOM_ISR | 0x0028 | W | 0x00000000 | Interrupt Status Register |
| DECOM_IEN | 0x002C | W | 0x00000000 | Interrupt Enable Register |
| DECOM_AXI_STAT | 0x0030 | W | 0x00000010 | AXI Master Interface State |
| DECOM_TSIZEL | 0x0034 | W | 0x00000000 | Decompressed Data Total Size Lower 32bit |
| DECOM_TSIZEH | 0x0038 | W | 0x00000000 | Decompressed Data Total Size Upper 32bit |
| DECOM_MGNUM | 0x003C | W | 0x00000000 | LZ4 File Magic Number |
| DECOM_FRAME | 0x0040 | W | 0x00000000 | LZ4 File Frame Descriptor |
| DECOM_DICTID | 0x0044 | W | 0x00000000 | Dictionary ID |
| DECOM_CSL | 0x0048 | W | 0x00000000 | LZ4 Content Size(CS) Lower 32-bits |
| DECOM_CSH | 0x004C | W | 0x00000000 | LZ4 Content Size(CS) Upper 32-bits |
| DECOM_LMTSL | 0x0050 | W | 0xFFFFFFFF | Limit Size of Decompressed Data |
| DECOM_LMTSH | 0x0054 | W | 0xFFFFFFFF | Limit Size of Decompressed Data |
| DECOM_GZFHD | 0x0058 | W | 0x00000000 | GZIP/ZLIB File Header Information |
| DECOM_VERSION | 0x00F0 | W | 0x00000926 | DECOM Version Number |

Copyright 2022 © Rockchip Electronics Co., Ltd.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 35.4.3 Detail Registers Description

### DECOM_CTRL

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5 | RW | 0x0 | ZLIBM<br>ZLIB mode.<br>1'b0: Disable<br>1'b1: Enable<br>When decompressing ZLIB compressed data, ZLIBM must be enabled and DEM should be set to 1. |
| 4 | RW | 0x0 | GZIPM<br>GZIP mode.<br>1'b0: Disable<br>1'b1: Enable<br>When decompressing GZIP files, GZIPM must be enabled and DEM should be set to 1. |
| 3 | RW | 0x0 | CCEN<br>LZ4 content checksum check enable.<br>1'b0: Disable<br>1'b1: Enable<br>In LZ4 files, a 32-bits content checksum will be appended at the end of the file. When CCEN is enabled, DECOM will verify the content checksum to check if the decompressed data is correct. Only valid when decompressing LZ4 files. |
| 2 | RW | 0x0 | BCEN<br>LZ4 block checksum check enable.<br>1'b0: Disable<br>1'b1: Enable<br>In LZ4 files, each data block will be followed by a 4-bytes checksum, calculated by using the xxHash-32 algorithm on the compressed data block. The intention is to detect data corruption(storage or transmission errors) immediately, before decoding. When BCEN is enabled, DECOM will check the block checksum to determine if the block to be decompressed is correct. Only valid when decompressing LZ4 files. |
| 1 | RW | 0x0 | HCEN<br>LZ4 header checksum check enable.<br>1'b0: Disable<br>1'b1: Enable<br>The LZ4 header contains a 1-byte xxh32 checksum value(HC). When HCEN is enabled, DECOM will check the HC to check if the header is correct. Only valid when decompressing LZ4 files. |
| 0 | RW | 0x0 | DEM<br>DECOM mode select.<br>1'b0: UNLZ4 mode. Decompress the file in LZ4 format.<br>1'b1: INFLATE mode. Decompress the file in INFLATE format. If GZIPM=1'b1 or GZLIBM=1'b1, DEM must be set 1. |

### DECOM_ENR

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | R/WSC | 0x0 | ENR<br>Enables and disables all decompress operations.<br>1'b0: Disable decompressor<br>1'b1: Enable decompressor to work<br>All FIFO buffers and aclk/dclk domain work registers are cleared when the device is disabled. Self clear when decompression is complete.<br>The ENR should be enabled after the other registers are configured. |

**DECOM_RADDR**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | RADDR<br>Read address.<br>This register is used to configure the starting address of the file to be decompressed. |

**DECOM_WADDR**

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | WADDR<br>Write address.<br>This register is used to configure the starting address of the location where the decompressed data is written.<br>Note: WADDR[31:0] must be configured with a 128bit aligned address (WADDR[3:0]==4'b0). |

**DECOM_UDDSL**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0xffffffff | UDDSL<br>Undecompressed data size lower 32bits. (Unit:byte)<br>UDDS[63:0] is the total size of undecompressed file. DECOM will read the compressed file data according to the value of UDDS[63:0], but the configuration of this register is optional. If this register is not configured, DECOM will use the default value of 64'hffff_ffff_ffff_ffff, and DECOM will keep reading data until the current decompression process ends. |

**DECOM_UDDSH**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0xffffffff | UDDSH<br>Undecompressed data size higher 32bits. |

**DECOM_TXTHR**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000100 | TXTHR<br>When the number of 32K_MEM entries is greater than or equal to this value, the DECOM will automatically transfer the data in the 32K_MEM to the external via the AXI Master interface. The value ranges is 0~32256.(Unit:byte) |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**DECOM_SLEN**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | SLEN<br>INFLATE store block size. (Unit:byte)<br>Indicate the block size when decompressing the store block of INFALTE file. For debugging SLC_ERR. |

**DECOM_STAT**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RO | 0x0 | LAST<br>Used to indicate whether the currently processed compressed data block is the last one.<br>1'b0: Not last block<br>1'b1: Last block |
| 0 | RO | 0x0 | COMPLETE<br>DECOM complete flag.<br>1'b0: Not complete<br>1'b1: Decompress is complete with no error<br>Only decompress total complete with no error, this flag is set to 1. |

**DECOM_ISR**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19 | W1C | 0x0 | DSOLI<br>Decompressed data size over limit_size interrupt.<br>1'b0: Interrupt is not active<br>1'b1: Interrupt is active |
| 18 | W1C | 0x0 | ZDICTEI<br>ZLIB dictionary error interrupt.<br>1'b0: Interrupt is not active<br>1'b1: Interrupt is active |
| 17 | W1C | 0x0 | GCMEI<br>GZIP/ZLIB compression method check error interrupt.<br>1'b0: Interrupt is not active<br>1'b1: Interrupt is active |
| 16 | W1C | 0x0 | GIDEI<br>GZIP ID error interrupt.<br>1'b0: Interrupt is not active<br>1'b1: Interrupt is active |
| 15 | W1C | 0x0 | CCCEI<br>UNLZ4 content checksum check error interrupt.<br>1'b0: ccc_err interrupt is not active<br>1'b1: ccc_err interrupt is active |
| 14 | W1C | 0x0 | BCCEI<br>UNLZ4 block checksum check error interrupt.<br>1'b0: bcc_err interrupt is not active<br>1'b1: bcc_err interrupt is active |
| 13 | W1C | 0x0 | HCCEI<br>UNLZ4 header checksum check error interrupt.<br>1'b0: hcc_err interrupt is not active<br>1'b1: hcc_err interrupt is active |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | W1C | 0x0 | CSEI<br>UNLZ4 content size (or GZIP isize) error interrupt.<br>1'b0: cs_err interrupt is not active<br>1'b1: cs_err interrupt is active |
| 11 | W1C | 0x0 | DICTEI<br>UNLZ4 dictionary error interrupt.<br>1'b0: Interrupt is not active<br>1'b1: Interrupt is active |
| 10 | W1C | 0x0 | VNEI<br>UNLZ4 version number error interrupt.<br>1'b0: vn_err interrupt is not active<br>1'b1: vn_err interrupt is active |
| 9 | W1C | 0x0 | MNEI<br>UNLZ4 magic number error interrupt.<br>1'b0: mn_err interrupt is not active<br>1'b1: mn_err interrupt is active |
| 8 | W1C | 0x0 | RDCEI<br>AXI read channel error interrupt.<br>1'b0: INFLATE AXI RDC_ERR interrupt is not active<br>1'b1: INFLATE AXI RDC_ERR interrupt is active |
| 7 | W1C | 0x0 | WRCEI<br>AXI write channel error interrupt.<br>1'b0: INFLATE AXI WRC_ERR interrupt is not active<br>1'b1: INFLATE AXI WRC_ERR interrupt is active |
| 6 | W1C | 0x0 | DISEI<br>INFLATE huffman distance error interrupt.<br>1'b0: INFLATE HFDIS_ERR interrupt is not active<br>1'b1: INFLATE HFDIS_ERR interrupt is active |
| 5 | W1C | 0x0 | LENEI<br>INFLATE huffman length error interrupt.<br>1'b0: INFLATE HFLEN_ERR interrupt is not active<br>1'b1: INFLATE HFLEN_ERR interrupt is active |
| 4 | W1C | 0x0 | LITEI<br>INFLATE huffman literal error interrupt.<br>1'b0: INFLATE HFLIT_ERR interrupt is not active<br>1'b1: INFLATE HFLIT_ERR interrupt is active |
| 3 | W1C | 0x0 | SQMEI<br>INFLATE SQ match error interrupt.<br>1'b0: INFLATE SQM_ERR interrupt is not active<br>1'b1: INFLATE SQM_ERR interrupt is active |
| 2 | W1C | 0x0 | SLCEI<br>INFLATE store block length check error interrupt.<br>1'b0: INFLATE SLC_ERR interrupt is not active<br>1'b1: INFLATE SLC_ERR interrupt is active |
| 1 | W1C | 0x0 | HDEI<br>INFLATE file header error interrupt.<br>1'b0: INFLATE header error interrupt is not active<br>1'b1: INFLATE header error interrupt is active |
| 0 | W1C | 0x0 | DSI<br>DECOM stop interrupt.<br>1'b0: Decompression stop interrupt is not active<br>1'b1: Decompression stop interrupt is active<br>This interrupt indicates that DECOM has stopped working. Including decompression completion or decompression encountered an error. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**DECOM_IEN**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19 | RW | 0x0 | DSOLIEN<br>Decompressed data size over limit_size interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 18 | RW | 0x0 | ZDICTEIEN<br>ZLIB dictionary error interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 17 | RW | 0x0 | GCMEIEN<br>GZIP/ZLIB compression method error interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 16 | RW | 0x0 | GIDEIEN<br>GZIP ID error interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 15 | RW | 0x0 | CCCEIEN<br>UNLZ4 content checksum check error interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | BCCEIEN<br>UNLZ4 block checksum check error interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | HCCEIEN<br>UNLZ4 header checksum check error interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | CSEIEN<br>UNLZ4 content size (or GZIP isize) error interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | DICTEIEN<br>UNLZ4 dictionary error interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | VNEIEN<br>UNLZ4 version number error interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | WNEIEN<br>UNLZ4 magic number error interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | RDCEIEN<br>AXI read channel error interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RW | 0x0 | WRCEIEN<br>AXI write channel error interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | DISEIEN<br>INFLATE huffman distance error interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | LENEIEN<br>INFLATE huffman length error interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | LITEIEN<br>INFLATE huffman literal error interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | SQMEIEN<br>INFLATE SQ match error interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | SLCIEN<br>INFLATE store block length check error interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | HDEIEN<br>INFLATE file header error interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | DSIEN<br>DECOM stop interrupt enable.<br>1'b0: Disable<br>1'b1: Enable |

**DECOM_AXI_STAT**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4 | RO | 0x1 | AXI_IDLE<br>AXI master idle state register.<br>1'b0: AXI master is busy<br>1'b1: AXI master is idle<br>When the decompression is aborted, DECOM will wait for AXI master's current read/write transfer to complete, that is, wait for AXI_IDLE=1, then reset DECOM, otherwise the uncompleted AXI transmission will cause AXI bus exception.<br>It should be noted that after the decompression is abnormal, the AXI master's unfinished write operation will continue, but the output value of wstrb[15:0] will become 16'b0. |
| 3:2 | RO | 0x0 | RRESP<br>AXI read channel response state. |
| 1:0 | RO | 0x0 | BRESP<br>AXI write channel response state. |

**DECOM_TSIZEL**

Address: Operational Base + offset (0x0034)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | TSIZEL<br>The total size of the data after decompression.<br>TSIZE[63:0]. (Unit:byte) |

**DECOM_TSIZEH**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | TSIZEH<br>The total size of the data after decompression. |

**DECOM_MGNUM**

Address: Operational Base + offset (0x003C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | MGNUM<br>Magic number of LZ4 is 0x184D2204.<br>If the MGNUM is not 0x184D2204, a magic number error(mn_err) will be generated. And DECOM will stop decompressing. |

**DECOM_FRAME**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23:16 | RO | 0x00 | HCC<br>Header checksum byte.<br>One-byte checksum of combined descriptor fields, including optional ones. The value is the second byte of xxh32() using zero as a see, and the full frame descriptor as an input (including optional fields when they are present). A wrong checksum indicates an error in the descriptor. Header checksum is informational and can be skipped.<br>The header checksum check function can be enabled by controlling the HCEN enable signal in the CTRL register. After being turned on, DECOM calculates the hash32 check value based on the data of the frame descriptor part of the LZ4 compressed file, and performs the header checksum byte in the file. In contrast, if they are not equal, an HCC error will be generated and an interrupt will be generated. |
| 15:8 | RO | 0x00 | BD<br>BD byte.<br>Including Block Maximum Size information. This information is useful to help the decoder allocate memory. Size here refers to the original(uncompressed) data size. |
| 7:6 | RO | 0x0 | VN_NUM<br>Version number.<br>2-bits field, must be set to 2'b01. Any other value cannot be decoded by this version of the specification. If the version number is error, Version number error(VNE) will be generated. |
| 5 | RO | 0x0 | BCC_FLG<br>Block checksum flag.<br>If this flag is set, each data block will be followed by a 4-bytes checksum, calculated by using the xxHash-32 algorithm on the raw (compressed) data block. The intention is to detect data corruption (storage or transmission errors) immediately, before decoding. Block checksum usage is optional. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RO | 0x0 | BIND_FLG<br>Block independence flag.<br>If this flag is set to "1", blocks are independent. If this flag is set to "0", each block depends on previous ones (up to LZ4 window size, which is 64 KB). In such case, it's necessary to decode all blocks in sequence. Block dependency improves compression ratio, especially for small blocks. On the other hand, it makes random access or multi-threaded decoding impossible. For debugging. |
| 3 | RO | 0x0 | CS_FLG<br>Content size flag.<br>If this flag is set, the uncompressed size of data included within the frame will be present as an 8 bytes unsigned little endian value, after the flags. Content size usage is optional. |
| 2 | RO | 0x0 | CCC_FLG<br>Content checksum flag.<br>If this flag is set, a 32-bits content checksum will be appended after the EndMark. |
| 1 | RO | 0x0 | reserved |
| 0 | RO | 0x0 | DICT_FLG<br>Dictionary ID flag.<br>If this flag is set, a 4-bytes Dict-ID field will be present, after the descriptor flags and the Content Size. If this flag is set, Dictionary ID error will be generated. DECOM will stop decompressing. |

**DECOM_DICTID**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | DICTID<br>Dictionary ID in the compressed file header.<br>Dictionary ID is only present if the DID_FLG is set. It works as a kind of "known prefix" which is used by both the compressor and the decompressor to "warm-up" reference tables. |

**DECOM_CSL**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | CSL<br>Content size(CS) lower 32-bits. (Unit:byte)<br>CS[63:0] is the original(uncompressed) size. This information is optional in LZ4 file header, and only present if CS_FLG is set.<br>CS[63:0]={CSH, CSL}; |

**DECOM_CSH**

Address: Operational Base + offset (0x004C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RO | 0x0 | CSH<br>Content size(CS) upper 32-bits. |

**DECOM_LMTSL**

Address: Operational Base + offset (0x0050)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0xffffffff | LMTSL<br>Limit size of decompressed data lower 32bits. (Unit:byte)<br>When the amount of decompressed data is greater than the LMTS, DSOLI interrupt is generated and the decompression process is stopped. |

**DECOM_LMTSH**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0xffffffff | LMTSH<br>Limit size of decompressed data higher 32bits. |

**DECOM_GZFHD**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RO | 0x0 | GZFHD<br>GZIP/ZLIB file header information.<br>When GZIPM = 1, GZFHD is GZIP file header information.<br>When ZLIBM = 1, GZFHD is ZLIB file header information. |

**DECOM_VERSION**

Address: Operational Base + offset (0x00F0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000926 | VERSION<br>Version number = 32'h0000_0926. |

## 35.5 Application Notes

- After configuring the decompression mode and other decompression parameters, configure the decompression enable register ENR
- When the decompression is not completed, setting ENR from 1 to 0 will force the decompression process to stop and DECOM will return to the IDLE state. Need to reconfigure and enable DECOM to start the next decompression
- When an error is encountered in the decompression, DECOM will immediately stop the decompression process, set the relevant status register, and generate the corresponding interrupt
- After the decompression process is stopped, ENR will automatically change to 0
- After the decompression process is stopped, DSI will be set to 1. If DSIEN is 1, an interrupt will be generated; if DSIEN is 0, no interrupt will be generated
- After the decompression process is stopped, COMPLETE (STAT[0]) is not set to 1 if there is an error in the decompression process; COMPLETE is set to 1 only when the decompression is complete and there are no errors

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

# Chapter 36 RKNN

## 36.1 Overview

RKNN is the process unit which is dedicated to neural network. It is designed to accelerate the neural network arithmetic in field of AI (artificial intelligence) such as machine vision and natural language processing. The variety of applications for AI is expanding, and currently provides functionality in a variety of areas, including face tracking as well as gesture and body tracking, image classification, video surveillance, automatic speech recognition (ASR) and advanced driver assistance systems (ADAS).
RKNN supports the following features:

- Include triple NPU CORE
- Support triple core co-work, dual core co-work, and work independently
- AHB interface used for configuration only support single
- AXI interface used to fetch data from memory
- Support integer 4, integer 8, integer 16, float 16, Bfloat 16 and tf32 operation
- 1024x3 integer 8 MAC operations per cycle
- 512x3 integer 16 MAC operations per cycle
- 512x3 float 16 MAC operations per cycle
- 512x3 bfloat 16 MAC operations per cycle
- 256x3 tf32 MAC operation per cycle
- 2048x3 integer 4 MAC operation per cycle
- 384KBx3 internal buffer
- Inference Engine: TensorFlow, Caffe, Tflite, Pytorch, Onnx NN, Android NN, etc.

## 36.2 Block Diagram

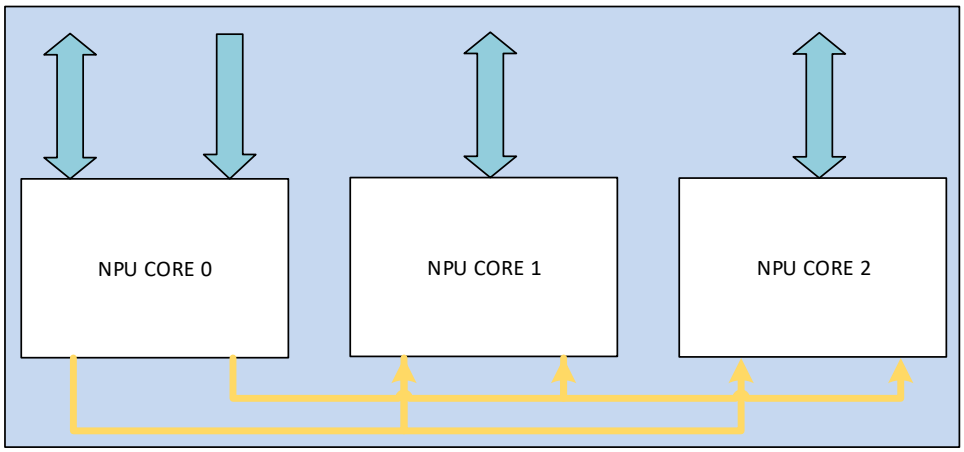



Fig. 36-1 RKNN Triple Core Architecture

Copyright 2022 © Rockchip Electronics Co., Ltd.

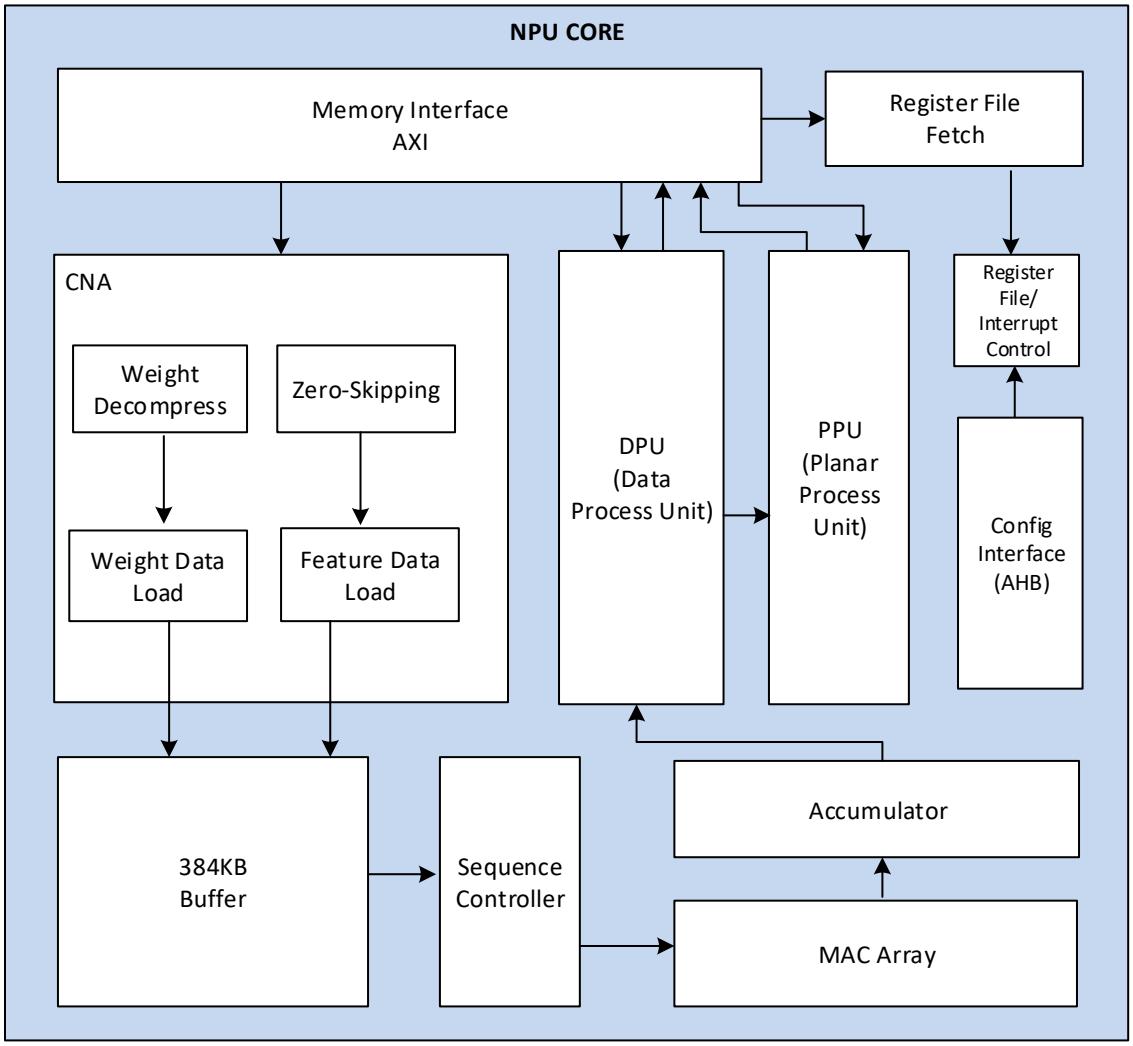



Fig. 36-2 RKNN Single Core Architecture

# 36.3 Function Description

### 36.3.1 1.3.1 AHB/AXI Interface

The AXI master interface is used to fetch data from memory that is attached to the Soc AXI interconnect. The AHB slave interface is used to access the registers for configuration, debug and test.

### 36.3.2 1. 3. 2 Neural Network Accelerating Engine

As the unit name, this engine is the main process unit for Neural Network arithmetic. This unit include convolution pre-process controller, internal buffer, mac array, accumulator. It provides parallel convolution MAC for recognition functions and int4, int8, int16, fp16, bfloat16 and tf16 are supported.

### 36.3.3 1. 3. 3 Data Processing Unit

Data Processing Unit mainly process the single data calculate, such as leaky_relu, relu, relux, sigmoid, tanh…etc. It also provides function: softmax, transpose, data format conversion, …etc.

### 36.3.4 1. 3. 4 Planar Processing Unit

Planar Processing Unit mainly provide planar function followed by output data from Data Processing Unit, such as average pooling, max pooling, min pooling… are supported.

Copyright 2022 © Rockchip Electronics Co., Ltd.

### 36.3.5 1. 3. 5 Register File Fetch Unit

Register File Fetch Unit fetch register configuration from external system memory through AXI
interface.

## 36.4 Register Description

### 36.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 1- 1 RKNN Address Mapping

| Base Address[15:12] | Device | Address Length | Offset Address Range |
|---|---|---|---|
| 4'h0 | PC | 4K BYTE | 0x0000 ~ 0x0fff |
| 4'h1 | CNA | 4K BYTE | 0x1000 ~ 0x1fff |
| 4'h3 | CORE | 4K BYTE | 0x3000 ~ 0x3fff |
| 4'h4 | DPU | 4K BYTE | 0x4000 ~ 0x4fff |
| 4'h5 | DPU_RDMA | 4K BYTE | 0x5000 ~ 0x5fff |
| 4'h6 | PPU | 4K BYTE | 0x6000 ~ 0x6fff |
| 4'h7 | PPU_RDMA | 4K BYTE | 0x7000 ~ 0x7fff |
| 4'h8 | DDMA | 4K BYTE | 0x8000 ~ 0x8fff |
| 4'h9 | SDMA | 4K BYTE | 0x9000 ~ 0x9fff |
| 4'hf | GLOBAL | 4 BYTE | 0xf000 ~ 0xf004 |

### 36.4.2 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKNN_pc_operation_enable | 0x0008 | W | 0x00000000 | Operation Enable |
| RKNN_pc_base_address | 0x0010 | W | 0x00000000 | PC address register |
| RKNN_pc_register_amounts | 0x0014 | W | 0x00000000 | Register amount for each task |
| RKNN_pc_interrupt_mask | 0x0020 | W | 0x0001FFFF | Interrupt Mask |
| RKNN_pc_interrupt_clear | 0x0024 | W | 0x00000000 | Interrupt clear |
| RKNN_pc_interrupt_status | 0x0028 | W | 0x00000000 | Interrupt status |
| RKNN_pc_interrupt_raw_status | 0x002C | W | 0x00000000 | Interrupt raw status |
| RKNN_pc_task_con | 0x0030 | W | 0x00000000 | Task control register |
| RKNN_pc_task_dma_base_addr | 0x0034 | W | 0x00000000 | Task Base address |
| RKNN_pc_task_status | 0x003C | W | 0x00000000 | Task status register |
| RKNN_cna_s_status | 0x1000 | W | 0x00000000 | Single register group status |
| RKNN_cna_s_pointer | 0x1004 | W | 0x00000000 | Single register group pointer |
| RKNN_cna_operation_enable | 0x1008 | W | 0x00000000 | Operation Enable |
| RKNN_cna_conv_con1 | 0x100C | W | 0x00000000 | Convolution control register1 |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKNN_cna_conv_con2 | 0x1010 | W | 0x00000000 | Convolution control register2 |
| RKNN_cna_conv_con3 | 0x1014 | W | 0x00000000 | Convolution control register3 |
| RKNN_cna_data_size0 | 0x1020 | W | 0x00000000 | Feature data size control register0 |
| RKNN_cna_data_size1 | 0x1024 | W | 0x00000000 | Feature data size control register1 |
| RKNN_cna_data_size2 | 0x1028 | W | 0x00000000 | Feature data size control register2 |
| RKNN_cna_data_size3 | 0x102C | W | 0x00000000 | Feature data size control register3 |
| RKNN_cna_weight_size0 | 0x1030 | W | 0x00000000 | Weight size control 0 |
| RKNN_cna_weight_size1 | 0x1034 | W | 0x00000000 | Weight size control 1 |
| RKNN_cna_weight_size2 | 0x1038 | W | 0x00000000 | Weight size control 2 |
| RKNN_cna_cbuf_con0 | 0x1040 | W | 0x00000000 | CBUF control register 0 |
| RKNN_cna_cbuf_con1 | 0x1044 | W | 0x00000000 | CBUF control register 1 |
| RKNN_cna_cvt_con0 | 0x104C | W | 0x00000000 | Input convert control register0 |
| RKNN_cna_cvt_con1 | 0x1050 | W | 0x00000000 | Input convert control register1 |
| RKNN_cna_cvt_con2 | 0x1054 | W | 0x00000000 | Input convert control register2 |
| RKNN_cna_cvt_con3 | 0x1058 | W | 0x00000000 | Input convert control register3 |
| RKNN_cna_cvt_con4 | 0x105C | W | 0x00000000 | Input convert control register4 |
| RKNN_cna_fc_con0 | 0x1060 | W | 0x00000000 | Full connected control register0 |
| RKNN_cna_fc_con1 | 0x1064 | W | 0x00000000 | Full connected control register1 |
| RKNN_cna_pad_con0 | 0x1068 | W | 0x00000000 | Pad control register0 |
| RKNN_cna_feature_data_addr | 0x1070 | W | 0x00000000 | Base address for input feature data |
| RKNN_cna_fc_con2 | 0x1074 | W | 0x00000000 | Full connected control register2 |
| RKNN_cna_dma_con0 | 0x1078 | W | 0x00000000 | AXI control register 0 |
| RKNN_cna_dma_con1 | 0x107C | W | 0x00000000 | AXI control register 1 |
| RKNN_cna_dma_con2 | 0x1080 | W | 0x00000000 | AXI control register 2 |
| RKNN_cna_fc_data_size0 | 0x1084 | W | 0x00000000 | Full connected data size control register0 |
| RKNN_cna_fc_data_size1 | 0x1088 | W | 0x00000000 | Full connected data size control register1 |
| RKNN_cna_clk_gate | 0x1090 | W | 0x00000000 | Clock gating control register |
| RKNN_cna_dcomp_ctrl | 0x1100 | W | 0x00000000 | Weight decompress control register |
| RKNN_cna_dcomp_regnum | 0x1104 | W | 0x00000000 | Weight decompress register number |
| RKNN_cna_dcomp_addr0 | 0x1110 | W | 0x00000000 | Base address of the weight |
| RKNN_cna_dcomp_amount0 | 0x1140 | W | 0x00000000 | Amount of the weight decompress for the 0 decompress |
| RKNN_cna_dcomp_amount1 | 0x1144 | W | 0x00000000 | Amount of the weight decompress for the 1 decompress |
| RKNN_cna_dcomp_amount2 | 0x1148 | W | 0x00000000 | Amount of the weight decompress for the 2 decompress |
| RKNN_cna_dcomp_amount3 | 0x114C | W | 0x00000000 | Amount of the weight decompress for the 3 decompress |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKNN_cna_dcomp_amount4 | 0x1150 | W | 0x00000000 | Amount of the weight decompress for the 4 decompress |
| RKNN_cna_dcomp_amount5 | 0x1154 | W | 0x00000000 | Amount of the weight decompress for the 5 decompress |
| RKNN_cna_dcomp_amount6 | 0x1158 | W | 0x00000000 | Amount of the weight decompress for the 6 decompress |
| RKNN_cna_dcomp_amount7 | 0x115C | W | 0x00000000 | Amount of the weight decompress for the 7 decompress |
| RKNN_cna_dcomp_amount8 | 0x1160 | W | 0x00000000 | Amount of the weight decompress for the 8 decompress |
| RKNN_cna_dcomp_amount9 | 0x1164 | W | 0x00000000 | Amount of the weight decompress for the 9 decompress |
| RKNN_cna_dcomp_amount10 | 0x1168 | W | 0x00000000 | Amount of the weight decompress for the 10 decompress |
| RKNN_cna_dcomp_amount11 | 0x116C | W | 0x00000000 | Amount of the weight decompress for the 11 decompress |
| RKNN_cna_dcomp_amount12 | 0x1170 | W | 0x00000000 | Amount of the weight decompress for the 12 decompress |
| RKNN_cna_dcomp_amount13 | 0x1174 | W | 0x00000000 | Amount of the weight decompress for the 13 decompress |
| RKNN_cna_dcomp_amount14 | 0x1178 | W | 0x00000000 | Amount of the weight decompress for the 14 decompress |
| RKNN_cna_dcomp_amount15 | 0x117C | W | 0x00000000 | Amount of the weight decompress for the 15 decompress |
| RKNN_cna_cvt_con5 | 0x1180 | W | 0x00000000 | Input convert control register5 |
| RKNN_cna_pad_con1 | 0x1184 | W | 0x00000000 | Pad controller register1 |
| RKNN_core_s_status | 0x3000 | W | 0x00000000 | Single register group status |
| RKNN_core_s_pointer | 0x3004 | W | 0x00000000 | Single register group pointer |
| RKNN_core_operation_enable | 0x3008 | W | 0x00000000 | Operation Enable |
| RKNN_core_mac_gating | 0x300C | W | 0x07800800 | MAC gating register |
| RKNN_core_misc_cfg | 0x3010 | W | 0x00000000 | Misc configuration register |
| RKNN_core_dataout_size_0 | 0x3014 | W | 0x00000000 | Feature size register 0 of output |
| RKNN_core_dataout_size_1 | 0x3018 | W | 0x00000000 | Feature size register 1 of output |
| RKNN_core_clip_truncate | 0x301C | W | 0x00000000 | Shift value register |
| RKNN_dpu_s_status | 0x4000 | W | 0x00000000 | Single register group status |
| RKNN_dpu_s_pointer | 0x4004 | W | 0x00000000 | Single register group pointer |
| RKNN_dpu_operation_enable | 0x4008 | W | 0x00000000 | Operation Enable |
| RKNN_dpu_feature_mode_cfg | 0x400C | W | 0x00000000 | Configuration of the feature mode |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKNN_dpu_data_format | 0x4010 | W | 0x00000000 | Configuration of the data format |
| RKNN_dpu_offset_pend | 0x4014 | W | 0x00000000 | Value of the offset pend |
| RKNN_dpu_dst_base_addr | 0x4020 | W | 0x00000000 | Destination base address |
| RKNN_dpu_dst_surf_stride | 0x4024 | W | 0x00000000 | Destination surface size |
| RKNN_dpu_data_cube_width | 0x4030 | W | 0x00000000 | Width of the input cube |
| RKNN_dpu_data_cube_height | 0x4034 | W | 0x00000000 | Height of the input cube |
| RKNN_dpu_data_cube_notch_addr | 0x4038 | W | 0x00000000 | Notch signal of the input cube |
| RKNN_dpu_data_cube_channel | 0x403C | W | 0x00000000 | Channel of the input cube |
| RKNN_dpu_bs_cfg | 0x4040 | W | 0x00000000 | Configuration of the BS |
| RKNN_dpu_bs_alu_cfg | 0x4044 | W | 0x00000000 | Configuration of the BS ALU |
| RKNN_dpu_bs_mul_cfg | 0x4048 | W | 0x00000000 | Configuration of the BS MUL |
| RKNN_dpu_bs_relux_cmp_value | 0x404C | W | 0x00000000 | Value of the RELUX compare with |
| RKNN_dpu_bs_ow_cfg | 0x4050 | W | 0x00000000 | Configuration of the BS OW |
| RKNN_dpu_bs_ow_op | 0x4054 | W | 0x00000000 | Ow op of the BS OW |
| RKNN_dpu_wdma_size_0 | 0x4058 | W | 0x00000000 | Size 0 of the WDMA |
| RKNN_dpu_wdma_size_1 | 0x405C | W | 0x00000000 | Size 1 of the WDMA |
| RKNN_dpu_bn_cfg | 0x4060 | W | 0x00000000 | Configuration of BN |
| RKNN_dpu_bn_alu_cfg | 0x4064 | W | 0x00000000 | Configuration of the BN ALU |
| RKNN_dpu_bn_mul_cfg | 0x4068 | W | 0x00000000 | Configuration of the BN MUL |
| RKNN_dpu_bn_relux_cmp_value | 0x406C | W | 0x00000000 | Value of the RELUX compare with |
| RKNN_dpu_ew_cfg | 0x4070 | W | 0x00000000 | Configuration of EW |
| RKNN_dpu_ew_cvt_offset_value | 0x4074 | W | 0x00000000 | Offset of the EW input convert |
| RKNN_dpu_ew_cvt_scale_value | 0x4078 | W | 0x00000000 | Scale of the EW input convert |
| RKNN_dpu_ew_relux_cmp_value | 0x407C | W | 0x00000000 | Value of the RELUX compare with |
| RKNN_dpu_out_cvt_offset | 0x4080 | W | 0x00000000 | Offset of the output converter |
| RKNN_dpu_out_cvt_scale | 0x4084 | W | 0x00000000 | Scale of the output converter |
| RKNN_dpu_out_cvt_shift | 0x4088 | W | 0x00000000 | Shift of the output converter |
| RKNN_dpu_ew_op_value_0 | 0x4090 | W | 0x00000000 | Configure operand0 of the EW |
| RKNN_dpu_ew_op_value_1 | 0x4094 | W | 0x00000000 | Configure operand1 of the EW |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKNN_dpu_ew_op_value_2 | 0x4098 | W | 0x00000000 | Configure operand2 of the EW |
| RKNN_dpu_ew_op_value_3 | 0x409C | W | 0x00000000 | Configure operand3 of the EW |
| RKNN_dpu_ew_op_value_4 | 0x40A0 | W | 0x00000000 | Configure operand4 of the EW |
| RKNN_dpu_ew_op_value_5 | 0x40A4 | W | 0x00000000 | Configure operand5 of the EW |
| RKNN_dpu_ew_op_value_6 | 0x40A8 | W | 0x00000000 | Configure operand6 of the EW |
| RKNN_dpu_ew_op_value_7 | 0x40AC | W | 0x00000000 | Configure operand7 of the EW |
| RKNN_dpu_surface_add | 0x40C0 | W | 0x00000000 | Value of the surface adder |
| RKNN_dpu_lut_access_cfg | 0x4100 | W | 0x00000000 | LUT access address and type |
| RKNN_dpu_lut_access_data | 0x4104 | W | 0x00000000 | Configuration of LUT access data |
| RKNN_dpu_lut_cfg | 0x4108 | W | 0x00000000 | Configuration of the LUT |
| RKNN_dpu_lut_info | 0x410C | W | 0x00000000 | LUT information register |
| RKNN_dpu_lut_le_start | 0x4110 | W | 0x00000000 | LE LUT start point |
| RKNN_dpu_lut_le_end | 0x4114 | W | 0x00000000 | LE LUT end point |
| RKNN_dpu_lut_lo_start | 0x4118 | W | 0x00000000 | LO LUT start point |
| RKNN_dpu_lut_lo_end | 0x411C | W | 0x00000000 | LO LUT end point |
| RKNN_dpu_lut_le_slope_scale | 0x4120 | W | 0x00000000 | LE LUT slope scale |
| RKNN_dpu_lut_le_slope_shift | 0x4124 | W | 0x00000000 | LE LUT slope shift |
| RKNN_dpu_lut_lo_slope_scale | 0x4128 | W | 0x00000000 | LO LUT slope scale |
| RKNN_dpu_lut_lo_slope_shift | 0x412C | W | 0x00000000 | LO LUT slope shift |
| RKNN_dpu_rdma_s_status | 0x5000 | W | 0x00000000 | Single register group status |
| RKNN_dpu_rdma_s_pointer | 0x5004 | W | 0x00000000 | Single register group pointer |
| RKNN_dpu_rdma_operation_enable | 0x5008 | W | 0x00000000 | Operation Enable |
| RKNN_dpu_rdma_data_cube_width | 0x500C | W | 0x00000000 | Input cube width |
| RKNN_dpu_rdma_data_cube_height | 0x5010 | W | 0x00000000 | Input cube height |
| RKNN_dpu_rdma_data_cube_channel | 0x5014 | W | 0x00000000 | Input cube channel |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKNN_dpu_rdma_src_base_addr | 0x5018 | W | 0x00000000 | Base address of the input cube |
| RKNN_dpu_rdma_brdma_cfg | 0x501C | W | 0x00000000 | Configurations of BRDMA |
| RKNN_dpu_rdma_bs_base_addr | 0x5020 | W | 0x00000000 | Source base address of BRDMA |
| RKNN_dpu_rdma_nrdma_cfg | 0x5028 | W | 0x00000000 | Configurations of NRDMA |
| RKNN_dpu_rdma_bn_base_addr | 0x502C | W | 0x00000000 | Source base address of NRDMA |
| RKNN_dpu_rdma_erdma_cfg | 0x5034 | W | 0x00000000 | Configurations of ERDMA |
| RKNN_dpu_rdma_ew_base_addr | 0x5038 | W | 0x00000000 | Source base address of ERDMA |
| RKNN_dpu_rdma_ew_surf_stride | 0x5040 | W | 0x00000000 | Surface size of the cube that the ERDMA read |
| RKNN_dpu_rdma_feature_mode_cfg | 0x5044 | W | 0x00000000 | Configuration of the feature mode |
| RKNN_dpu_rdma_src_dma_cfg | 0x5048 | W | 0x00000000 | Configuration of the source read DMA |
| RKNN_dpu_rdma_surf_notch | 0x504C | W | 0x00000000 | Surface notch |
| RKNN_dpu_rdma_pad_cfg | 0x5064 | W | 0x00000000 | Configuration of the pad |
| RKNN_dpu_rdma_weight | 0x5068 | W | 0x00000000 | Weight of the arbiter |
| RKNN_dpu_rdma_ew_surf_notch | 0x506C | W | 0x00000000 | Surface notch |
| RKNN_ppu_s_status | 0x6000 | W | 0x00000000 | Single register group status |
| RKNN_ppu_s_pointer | 0x6004 | W | 0x00000000 | Single register group pointer |
| RKNN_ppu_operation_enable | 0x6008 | W | 0x00000000 | Operation Enable |
| RKNN_ppu_data_cube_in_width | 0x600C | W | 0x00000000 | Width of the input cube |
| RKNN_ppu_data_cube_in_height | 0x6010 | W | 0x00000000 | Height of the input cube |
| RKNN_ppu_data_cube_in_channel | 0x6014 | W | 0x00000000 | Channel of the input cube |
| RKNN_ppu_data_cube_out_width | 0x6018 | W | 0x00000000 | Width of the output cube |
| RKNN_ppu_data_cube_out_height | 0x601C | W | 0x00000000 | Height of the output cube |
| RKNN_ppu_data_cube_out_channel | 0x6020 | W | 0x00000000 | Channel of the output cube |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKNN_ppu_operation_mode_cfg | 0x6024 | W | 0x00000000 | Configuration of the operation mode |
| RKNN_ppu_pooling_kernel_cfg | 0x6034 | W | 0x00000000 | Configuration of the pooling kernel size |
| RKNN_ppu_recip_kernel_width | 0x6038 | W | 0x00000000 | The reciprocal of the kernel width |
| RKNN_ppu_recip_kernel_height | 0x603C | W | 0x00000000 | The reciprocal of the kernel height |
| RKNN_ppu_pooling_padding_cfg | 0x6040 | W | 0x00000000 | Configuration of the pooling pad |
| RKNN_ppu_padding_value_1_cfg | 0x6044 | W | 0x00000000 | Pad Value register0 |
| RKNN_ppu_padding_value_2_cfg | 0x6048 | W | 0x00000000 | Pad Value register1 |
| RKNN_ppu_dst_base_addr | 0x6070 | W | 0x00000000 | Destination address of the output cube |
| RKNN_ppu_dst_surf_stride | 0x607C | W | 0x00000000 | Destination surface size |
| RKNN_ppu_data_format | 0x6084 | W | 0x00000000 | Configuration of the data format |
| RKNN_ppu_misc_ctrl | 0x60DC | W | 0x00000000 | Misc configuration |
| RKNN_ppu_rdma_s_status | 0x7000 | W | 0x00000000 | Single register group status |
| RKNN_ppu_rdma_s_pointer | 0x7004 | W | 0x00000000 | Single register group pointer |
| RKNN_ppu_rdma_operation_enable | 0x7008 | W | 0x00000000 | Operation Enable |
| RKNN_ppu_rdma_cube_in_width | 0x700C | W | 0x00000000 | Input cube width |
| RKNN_ppu_rdma_cube_in_height | 0x7010 | W | 0x00000000 | Input cube height |
| RKNN_ppu_rdma_cube_in_channel | 0x7014 | W | 0x00000000 | Input cube channel |
| RKNN_ppu_rdma_src_base_addr | 0x701C | W | 0x00000000 | Source base address for input feature |
| RKNN_ppu_rdma_src_line_stride | 0x7024 | W | 0x00000000 | Source line number including Virtual box |
| RKNN_ppu_rdma_src_surf_stride | 0x7028 | W | 0x00000000 | Source surface size including Virtual box |
| RKNN_ppu_rdma_data_format | 0x7030 | W | 0x00000000 | Data format for the input feature |
| RKNN_ddma_cfg_outstanding | 0x8000 | W | 0x00000000 | Outstanding config register |
| RKNN_ddma_rd_weight_0 | 0x8004 | W | 0x00000000 | Weight of read arbiter |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| RKNN_ddma_wr_weight_0 | 0x8008 | W | 0x00000000 | Weight of write arbiter |
| RKNN_ddma_cfg_id_error | 0x800C | W | 0x00000000 | Id where error happened |
| RKNN_ddma_rd_weight_1 | 0x8010 | W | 0x00000000 | Weight of read arbiter register1 |
| RKNN_ddma_cfg_dma_fifo_clr | 0x8014 | W | 0x00000000 | Clear DMA FIFO |
| RKNN_ddma_cfg_dma_arb | 0x8018 | W | 0x00000000 | DMA arbiter configuration register |
| RKNN_ddma_cfg_dma_rd_qos | 0x8020 | W | 0x00000000 | Read Qos for DMA |
| RKNN_ddma_cfg_dma_rd_cfg | 0x8024 | W | 0x00000000 | Read configuration for AXI signals |
| RKNN_ddma_cfg_dma_wr_cfg | 0x8028 | W | 0x00000000 | Write configuration for AXI signals |
| RKNN_ddma_cfg_dma_wstrb | 0x802C | W | 0x00000000 | Write strobe signal for AXI |
| RKNN_ddma_cfg_status | 0x8030 | W | 0x00000000 | AXI status signal |
| RKNN_sdma_cfg_outstanding | 0x9000 | W | 0x00000000 | Outstanding configuration register |
| RKNN_sdma_rd_weight_0 | 0x9004 | W | 0x00000000 | Weight of read arbiter |
| RKNN_sdma_wr_weight_0 | 0x9008 | W | 0x00000000 | Weight of write arbiter |
| RKNN_sdma_cfg_id_error | 0x900C | W | 0x00000000 | Id where error happened |
| RKNN_sdma_rd_weight_1 | 0x9010 | W | 0x00000000 | Weight of read arbiter register1 |
| RKNN_sdma_cfg_dma_fifo_clr | 0x9014 | W | 0x00000000 | Clear DMA FIFO |
| RKNN_sdma_cfg_dma_arb | 0x9018 | W | 0x00000000 | DMA arbiter configuration register |
| RKNN_sdma_cfg_dma_rd_qos | 0x9020 | W | 0x00000000 | Read Qos for DMA |
| RKNN_sdma_cfg_dma_rd_cfg | 0x9024 | W | 0x00000000 | Read configuration for AXI signals |
| RKNN_sdma_cfg_dma_wr_cfg | 0x9028 | W | 0x00000000 | Write configuration for AXI signals |
| RKNN_sdma_cfg_dma_wstrb | 0x902C | W | 0x00000000 | Write strobe signal for AXI |
| RKNN_sdma_cfg_status | 0x9030 | W | 0x00000000 | AXI status signal |
| RKNN_global_operation_enable | 0xF008 | W | 0x00000000 | Combine Operation Enable |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 36.4.3 Detail Registers Description

**RKNN_pc_operation_enable**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | op_en<br>PC operation enable.<br>1'd0: Disable PC module;<br>1'd1: Enable PC module to fetch register for each task. |

**RKNN_pc_base_address**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | pc_source_addr<br>PC base address.<br>This is the address of DMA instruction where it located. |
| 3:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | pc_sel<br>PC mode enable.<br>1'd0: PC mode, use AXI DMA to fetch register config;<br>1'd1: Slave mode, use AHB to set register. |

**RKNN_pc_register_amounts**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | pc_data_amount<br>Data amount.<br>The register number need to be fetched of one task. Each register takes 64 bits, it is combined as following:<br>bit[63:48] indicates which block the register forward to.<br>bit[47:16] the register's value<br>bit[15: 0] the register's offset address in each block.<br>bit[56]= 1 means this register is for pc block.<br>bit[57]= 1 CNA<br>bit[59]= 1 CORE<br>bit[60]= 1 DPU<br>bit[61]= 1 DPU_RDMA<br>bit[62]= 1 PPU<br>bit[63]= 1 PPU_RDMA<br>bit[55]= 1 to set each block's op_en<br>eg. 64'h0081_0000_007f_0008 will set each block's op_en(CNA, CORE, ..., PPU_RDMA).<br>note: op_en is strongly recommended set at the end of register list.<br>before op_en, 64'h0041_xxxx_xxxx_xxxx must be set. |

**RKNN_pc_interrupt_mask**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16:0 | RW | 0x1ffff | int_mask<br>Interrupt mask.<br>mask[0 ]: CNA feature group 0 interrupt mask. set 1 to enable interrupt;<br>mask[1 ]: CNA feature group 1;<br>mask[2 ]: CNA weight group 0;<br>mask[3 ]: CNA weight group 1;<br>mask[4 ]: CNA csc group 0;<br>mask[5 ]: CNA csc group 1;<br>mask[6 ]: CORE group 0;<br>mask[7 ]: CORE group 1;<br>mask[8 ]: DPU group 0;<br>mask[9 ]: DPU group 1;<br>mask[10]: PPU group 0;<br>mask[11]: PPU group 1;<br>mask[12]: DMA read error;<br>mask[13]: DMA write error;<br>Note: In pc mode, int mask set the last one task's interrupt masking. |

**RKNN_pc_interrupt_clear**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16:0 | W1C | 0x00000 | int_clr<br>Interrupt clear.<br>done_clr[0 ]: CNA feature group 0 interrupt clear;<br>done_clr[1 ]: CNA feature group 1;<br>done_clr[2 ]: CNA weight group 0;<br>done_clr[3 ]: CNA weight group 1;<br>done_clr[4 ]: CNA csc group 0;<br>done_clr[5 ]: CNA csc group 1;<br>done_clr[6 ]: CORE group 0;<br>done_clr[7 ]: CORE group 1;<br>done_clr[8 ]: DPU group 0;<br>done_clr[9 ]: DPU group 1;<br>done_clr[10]: PPU group 0;<br>done_clr[11]: PPU group 1;<br>done_clr[12]: DMA read error;<br>done_clr[13]: DMA write error. |

**RKNN_pc_interrupt_status**

Address: Operational Base + offset (0x0028)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16:0 | W1C | 0x00000 | int_st<br>Interrupt status.<br>int_st[0 ]: CNA feature group 0 interrupt status, which and with mask bit;<br>int_st[1 ]: CNA feature group 1;<br>int_st[2 ]: CNA weight group 0;<br>int_st[3 ]: CNA weight group 1;<br>int_st[4 ]: CNA csc group 0;<br>int_st[5 ]: CNA csc group 1;<br>int_st[6 ]: CORE group 0;<br>int_st[7 ]: CORE group 1;<br>int_st[8 ]: DPU group 0;<br>int_st[9 ]: DPU group 1;<br>int_st[10]: PPU group 0;<br>int_st[11]: PPU group 1;<br>int_st[12]: DMA read error;<br>int_st[13]: DMA write error. |

**RKNN_pc_interrupt_raw_status**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16:0 | W1C | 0x00000 | int_raw_st<br>Interrupt raw status.<br>int_st[0 ]: CNA feature group 0 interrupt raw status;<br>int_st[1 ]: CNA feature group 1;<br>int_st[2 ]: CNA weight group 0;<br>int_st[3 ]: CNA weight group 1;<br>int_st[4 ]: CNA csc group 0;<br>int_st[5 ]: CNA csc group 1;<br>int_st[6 ]: CORE group 0;<br>int_st[7 ]: CORE group 1;<br>int_st[8 ]: DPU group 0;<br>int_st[9 ]: DPU group 1;<br>int_st[10]: PPU group 0;<br>int_st[11]: PPU group 1;<br>int_st[12]: DMA read error;<br>int_st[13]: DMA write error. |

**RKNN_pc_task_con**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RO | 0x00000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | W1C | 0x0 | task_count_clear<br>Task counter clear register.<br>Clear the counter that counting current task. Before task started, it is suggested to clear. |
| 12 | RW | 0x0 | task_pp_en<br>PC task ping-pong mode enable.<br>1'd0: Ping-pong mode off. The second group register setting is fetched after first group task operation is finished;<br>1'd1: Tasks' registers are fetched in ping-pong mode. The second group register setting is fetched immediately after first group's register fetching is finished. |
| 11:0 | RW | 0x000 | task_number<br>PC task number.<br>Set the total task number to be executed. |

**RKNN_pc_task_dma_base_addr**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | dma_base_addr<br>Task base address.<br>This is for each DMA's base address.<br>For feature DMA, weight DMA, DPU DMA, PPU DMA, the address is set as offset address. Final address appear on AXI bus is base address + offset address. |
| 3:0 | RO | 0x0 | reserved |

**RKNN_pc_task_status**

Address: Operational Base + offset (0x003C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27:0 | RW | 0x0000000 | task_status<br>Task status.<br>[11:0]: Current task counter value;<br>[12]: Indicate the first task is operating;<br>[13]: Indicate the last task is operating;<br>[12]: Indicate the first task's register is fetching;<br>[13]: Indicate the last task's register is fetching. |

**RKNN_cna_s_status**

Address: Operational Base + offset (0x1000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17:16 | RO | 0x0 | status_1<br>Executer 1 status.<br>2'd0: Executer 1 is in idle state;<br>2'd1: Executer 1 is operating;<br>2'd2: Executer 1 is operating, executer 1 is waiting to operate;<br>2'd3: Reserved. |
| 15:2 | RO | 0x0000 | reserved |
| 1:0 | RO | 0x0 | status_0<br>Executer 0 status.<br>2'd0: Executer 0 is in idle state;<br>2'd1: Executer 0 is operating;<br>2'd2: Executer 0 is operating, executer 1 is waiting to operate;<br>2'd3: Reserved. |

**RKNN_cna_s_pointer**

Address: Operational Base + offset (0x1004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16 | RO | 0x0 | executer<br>Which register group to be used.<br>1'd0: Executer group 0;<br>1'd1: Executer group 1. |
| 15:6 | RO | 0x000 | reserved |
| 5 | W1C | 0x0 | executer_pp_clear<br>Clear executer group pointer.<br>Set this bit to 1 to clear pointer to 0. |
| 4 | W1C | 0x0 | pointer_pp_clear<br>Clear register group pointer.<br>Set this bit to 1 to clear pointer to 0. |
| 3 | RW | 0x0 | pointer_pp_mode<br>Register group ping-pong mode.<br>1'd0: Pointer ping-pong by executer;<br>eg. if current executer is 0, next pointer will toggle to 1;<br>1'd1: Pointer ping-pong by pointer;<br>eg. if current pointer is 0, next pointer will toggle to 1. |
| 2 | RW | 0x0 | executer_pp_en<br>Executer group ping-pong enable.<br>1'd0: Disable;<br>1'd1: Enable. |
| 1 | RW | 0x0 | pointer_pp_en<br>Register group ping-pong enable.<br>1'd0: Disable;<br>1'd1: Enable. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | pointer<br>Which register group ready to be set.<br>1'd0: Register group 0;<br>1'd1: Register group 1. |

**RKNN_cna_operation_enable**

Address: Operational Base + offset (0x1008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | op_en<br>Set this register will trigger CNA block operate.<br>This register and after this are all shadowed for ping-pong operation.<br>1'd0: Disable;<br>1'd1: Enable. |

**RKNN_cna_conv_con1**

Address: Operational Base + offset (0x100C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |
| 30 | RW | 0x0 | nonalign_dma<br>CNA DMA non-align mode.<br>1'd0: Disable;<br>1'd1: Enable, please enable this bit under ARGB mode.<br>Enable this bit will enable DMA fetching feature data continuously. |
| 29 | RW | 0x0 | group_line_off<br>Group line fetch off.<br>1'd0: Enable group line fetch;<br>1'd1: Disable.<br>This setting only influence line fetch efficiency. |
| 28:17 | RO | 0x000 | reserved |
| 16 | RW | 0x0 | deconv<br>Enable deconvolution function.<br>1'd0: Disable;<br>1'd1: Enable. |
| 15:12 | RW | 0x0 | argb_in<br>Non-align channel layer control register.<br>4'd8: 1 channel input mode;<br>4'd9: 2 channel input mode;<br>4'd10: 3 channel input mode;<br>4'd11: 4 channel input mode. |
| 11:10 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9:7 | RW | 0x0 | proc_precision<br>Process precision.<br>3'd0: Input precision is int 8;<br>3'd1: Input data precision is int 16;<br>3'd2: Input data precision is float 16;<br>3'd3: Input data precision is bfloat 16;<br>3'd4: Reserved;<br>3'd5: Reserved;<br>3'd6: Input data precision is int4;<br>3'd7: Input data precision is tf32. |
| 6:4 | RW | 0x0 | in_precision<br>Input precision.<br>3'd0: Input precision is int 8;<br>3'd1: Input data precision is int 16;<br>3'd2: Input data precision is float 16;<br>3'd3: Input data precision is bfloat 16;<br>3'd4: Reserved;<br>3'd5: Reserved;<br>3'd6: Input data precision is int4;<br>3'd7: Input data precision is tf32. |
| 3:0 | RW | 0x0 | conv_mode<br>Convolution mode.<br>2'd0: Direct convolution;<br>2'd1: Reserved;<br>2'd2: Reserved;<br>2'd3: Depthwise convolution. |

**RKNN_cna_conv_con2**

Address: Operational Base + offset (0x1010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23:16 | RW | 0x00 | kernel_group<br>Kernels group.<br>In int8, 32 kernels form 1 group, in int16 or fp16, 16 kernels form 1 group.<br>eg, weight kernel is 256, in int8, you can set this register to be 256/32 -1 = 15. |
| 15:14 | RO | 0x0 | reserved |
| 13:4 | RW | 0x000 | feature_grains<br>Feature data rows needs to be buffered before convolution start.<br>It's suggested to set this field as y_stride+weight_height+1. |
| 3 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | csc_wo_en<br>Do weight scan.<br>1'd0: Enable csc output weight data to core;<br>1'd1: Disable. |
| 1 | RW | 0x0 | csc_do_en<br>Do data scan.<br>1'd0: Enable csc output feature data to core;<br>1'd1: Disable. |
| 0 | RW | 0x0 | cmd_fifo_srst<br>Command FIFO soft reset.<br>Reserved for debug purpose. |

**RKNN_cna_conv_con3**

Address: Operational Base + offset (0x1014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |
| 30:28 | RW | 0x0 | nn_mode<br>co-work mode.<br>3'd0: Int8 mac array 32x32 mode;<br>3'd1: 64x32 mode;<br>3'd2: 96x32 mode;<br>3'd3: Reserved;<br>3'd4: 32x64 mode;<br>3'd5: 32x96 mode;<br>3'd6: Reserved;<br>3'd7: Reserved.<br>This register is target for multicore mode. By single core mode keep it at 3'd0. |
| 27:26 | RO | 0x0 | reserved |
| 25:21 | RW | 0x00 | atrous_y_dilation<br>Atrous x dilation.<br>Pad numbers inserted in feature map column between 2 pixels. |
| 20:16 | RW | 0x00 | atrous_x_dilation<br>Atrous x dilation.<br>Pad numbers inserted in feature map row between 2 pixels.<br>Set this register value >0 will enable atrous convolution. |
| 15:14 | RO | 0x0 | reserved |
| 13:11 | RW | 0x0 | deconv_y_stride<br>Deconvolution y stride.<br>Pad numbers inserted in feature map column between 2 pixels. |
| 10:8 | RW | 0x0 | deconv_x_stride<br>Deconvolution x stride.<br>Pad numbers inserted in feature map row between 2 pixels. |
| 7:6 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5:3 | RW | 0x0 | conv_y_stride<br>Convolution y stride.<br>Stride value in y direction. |
| 2:0 | RW | 0x0 | conv_x_stride<br>Convolution x stride.<br>Stride value in x direction. |

**RKNN_cna_data_size0**

Address: Operational Base + offset (0x1020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:27 | RO | 0x00 | reserved |
| 26:16 | RW | 0x000 | datain_width<br>Input feature data width. |
| 15:11 | RO | 0x00 | reserved |
| 10:0 | RW | 0x000 | datain_height<br>Input feature data height. |

**RKNN_cna_data_size1**

Address: Operational Base + offset (0x1024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | datain_channel_real<br>Real channel number.<br>If the input channel is not integer times of 8(int8) or 4(int 16/float 16), set the real channel number in this field. |
| 15:0 | RW | 0x0000 | datain_channel<br>Input feature data channel number;<br>Int 8 mode, this number should be integer times of 8;<br>Int 16/float 16 mode, should be integer times of 4. |

**RKNN_cna_data_size2**

Address: Operational Base + offset (0x1028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:11 | RO | 0x000000 | reserved |
| 10:0 | RW | 0x000 | dataout_width<br>Data width after convolution. |

**RKNN_cna_data_size3**

Address: Operational Base + offset (0x102C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:22 | RW | 0x0 | surf_mode<br>Surface serial mode.<br>2'd0: 1surf series;<br>2'd1: 1surf series;<br>2'd2: 2 surf series;<br>2'd3: 4 surf series. |
| 21:0 | RW | 0x000000 | dataout_atomics<br>Data atomics after convolution which is data out total pixels number. |

**RKNN_cna_weight_size0**

Address: Operational Base + offset (0x1030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | weight_bytes<br>Weight bytes in total for this convolution. |

**RKNN_cna_weight_size1**

Address: Operational Base + offset (0x1034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:19 | RO | 0x0000 | reserved |
| 18:0 | RW | 0x00000 | weight_bytes_per_kernel<br>Weight bytes for one kernel. |

**RKNN_cna_weight_size2**

Address: Operational Base + offset (0x1038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:24 | RW | 0x00 | weight_width<br>Kernel width. |
| 23:21 | RO | 0x0 | reserved |
| 20:16 | RW | 0x00 | weight_height<br>Kernel height. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | weight_kernels<br>Weight kernels. |

**RKNN_cna_cbuf_con0**

Address: Operational Base + offset (0x1040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RO | 0x00000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13 | RW | 0x0 | weight_reuse<br>Weight data reuse enable.<br>1'd0: Disable;<br>1'd1: Enable data reuse. fetching weight directly from internal buffer. |
| 12 | RW | 0x0 | data_reuse<br>Feature data reuse enable.<br>1'd0: Disable;<br>1'd1: Enable data reuse. fetching data directly from internal buffer. |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x0 | fc_data_bank<br>Bank numbers for fc zero-skipping feature data. In FC zero-skipping mode, set to be 1, Otherwise, must set to be 0. |
| 7:4 | RW | 0x0 | weight_bank<br>Bank numbers for weight data.<br>4'd1: Bank 7 occupied by weight data;<br>4'd2: Bank 6/7 occupied by weight data;<br>...<br>4'd7: Bank 1-7 occupied by weight data. |
| 3:0 | RW | 0x0 | data_bank<br>Bank numbers for feature data.<br>4'd0: Bank 0 occupied by feature data;<br>4'd1: Bank 0 and bank 1 occupied by feature data;<br>4'd2: Bank 0/1/2 occupied by feature data;<br>...<br>4'd6: Bank 0-6 occupied by feature data. |

**RKNN_cna_cbuf_con1**

Address: Operational Base + offset (0x1044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |
| 12:0 | RW | 0x0000 | data_entries<br>How many banks space needed to store one feature map row. |

**RKNN_cna_cvt_con0**

Address: Operational Base + offset (0x104C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27:22 | RW | 0x00 | cvt_truncate_3<br>CVT truncate value 3. |
| 21:16 | RW | 0x00 | cvt_truncate_2<br>CVT truncate value 2. |
| 15:10 | RW | 0x00 | cvt_truncate_1<br>CVT truncate value 1. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9:4 | RW | 0x00 | cvt_truncate_0<br>CVT truncate value 0. |
| 3 | RW | 0x0 | data_sign<br>Feature data is signed or unsigned.<br>1'd0: Unsigned;<br>1'd1: Signed. |
| 2 | RW | 0x0 | round_type<br>Rounding type of the input convert.<br>1'd0: Odd in, even not;<br>1'd1: Round-up 0.5 to 1. |
| 1 | RW | 0x0 | cvt_type<br>Cal type of the input convert.<br>1'd0: Multiply first, then add;<br>1'd1: CVT function will do add first, then multiply. |
| 0 | RW | 0x0 | cvt_bypass<br>Bypass input convert.<br>1'd0: Enable CVT function;<br>1'd1: Disable CVT function. |

**RKNN_cna_cvt_con1**

Address: Operational Base + offset (0x1050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | cvt_scale0<br>CVT scale 0.<br>Multiplier operand for 1st channel. |
| 15:0 | RW | 0x0000 | cvt_offset0<br>CVT offset 0.<br>Adder operand for 1st channel. |

**RKNN_cna_cvt_con2**

Address: Operational Base + offset (0x1054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | cvt_scale1<br>CVT scale 1<br>Multiplier operand for 2nd channel. |
| 15:0 | RW | 0x0000 | cvt_offset1<br>CVT offset 1.<br>Adder operand for 2nd channel. |

**RKNN_cna_cvt_con3**

Address: Operational Base + offset (0x1058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | cvt_scale2<br>CVT scale 2.<br>Multiplier operand for 3rd channel. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:0 | RW | 0x0000 | cvt_offset2<br>CVT offset 2.<br>Adder operand for 3rd channel. |

**RKNN_cna_cvt_con4**

Address: Operational Base + offset (0x105C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | cvt_scale3<br>CVT scale 3.<br>Multiplier operand for 4th channel. |
| 15:0 | RW | 0x0000 | cvt_offset3<br>CVT offset 3.<br>Adder operand for 4th channel. |

**RKNN_cna_fc_con0**

Address: Operational Base + offset (0x1060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | fc_skip_data<br>FC zero skipping data<br>Skipped feature data value, normally set to 0. |
| 15:1 | RO | 0x0000 | reserved |
| 0 | RW | 0x0 | fc_skip_en<br>FC zero skipping enable<br>1'd0: Disable;<br>1'd1: Enable skip some feature data value, normally skip zero. When one pixel feature data is 0, the corresponding weight data is not fetched from system memory. |

**RKNN_cna_fc_con1**

Address: Operational Base + offset (0x1064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16:0 | RW | 0x00000 | data_offset<br>FC zero skipping data offset.<br>Feature data offset in fc skip mode. |

**RKNN_cna_pad_con0**

Address: Operational Base + offset (0x1068)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:4 | RW | 0x0 | pad_left<br>Pad left<br>Pad numbers in left of the feature map. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:0 | RW | 0x0 | pad_top<br>PAD top<br>Pad numbers in top of the feature map. |

**RKNN_cna_feature_data_addr**

Address: Operational Base + offset (0x1070)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | feature_base_addr<br>Feature data address. |

**RKNN_cna_fc_con2**

Address: Operational Base + offset (0x1074)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16:0 | RW | 0x00000 | weight_offset<br>Weight data address. |

**RKNN_cna_dma_con0**

Address: Operational Base + offset (0x1078)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | ov4k_bypass<br>Separate the burst command of over 4k to 2 independent burst commands.<br>1'd0: Enable this feature;<br>1'd1: Bypass this feature. |
| 30:20 | RO | 0x000 | reserved |
| 19:16 | RW | 0x0 | weight_burst_len<br>AXI burst length for weight data DMA.<br>4'd3: Burst length is 4;<br>4'd7: Burst length is 8;<br>4'd15: Burst length is 16. |
| 15:4 | RO | 0x000 | reserved |
| 3:0 | RW | 0x0 | data_burst_len<br>AXI burst length for feature data DMA.<br>4'd3: Burst length is 4;<br>4'd7: Burst length is 8;<br>4'd15: Burst length is 16. |

**RKNN_cna_dma_con1**

Address: Operational Base + offset (0x107C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27:0 | RW | 0x0000000 | line_stride<br>Line stride<br>Feature width with Virtual box. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

**RKNN_cna_dma_con2**

Address: Operational Base + offset (0x1080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27:0 | RW | 0x0000000 | surf_stride<br>Surface stride<br>Feature map actual surface area. |

**RKNN_cna_fc_data_size0**

Address: Operational Base + offset (0x1084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | dma_width<br>Feature input width for AXI DMA. |
| 15:11 | RO | 0x00 | reserved |
| 10:0 | RW | 0x000 | dma_height<br>Feature input height for AXI DMA. |

**RKNN_cna_fc_data_size1**

Address: Operational Base + offset (0x1088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | dma_channel<br>Feature input channel for AXI DMA. |

**RKNN_cna_clk_gate**

Address: Operational Base + offset (0x1090)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4 | RW | 0x0 | cbuf_cs_disable_clkgate<br>Cache auto gating.<br>1'd0: Auto clock gate is enabled;<br>1'd1: Disable CBUF clock auto gate. |
| 3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | csc_disable_clkgate<br>Sequence scan auto gating.<br>1'd0: Auto clock gate is enabled;<br>1'd1: Disable csc block clock gate. |
| 1 | RW | 0x0 | cna_weight_disable_clkgate<br>Weight fetch auto gating.<br>1'd0: Auto clock gate is enabled;<br>1'd1: Disable weight block clock gate. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | cna_feature_disable_clkgate<br>Feature fetch auto gating.<br>1'd0: Auto clock gate is enabled;<br>1'd1: Disable feature block clock gate. |

**RKNN_cna_dcomp_ctrl**

Address: Operational Base + offset (0x1100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3 | RW | 0x0 | wt_dec_bypass<br>Bypass weight decompress. |
| 2:0 | RW | 0x0 | decomp_control<br>Control register for weight decompress. |

**RKNN_cna_dcomp_regnum**

Address: Operational Base + offset (0x1104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | dcomp_regnum<br>Weight decompress register number. |

**RKNN_cna_dcomp_addr0**

Address: Operational Base + offset (0x1110)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | decompress_addr0<br>Base address of the weight. |
| 3:0 | RO | 0x0 | reserved |

**RKNN_cna_dcomp_amount0**

Address: Operational Base + offset (0x1140)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | dcomp_amount0<br>Amount of the weight decompress for the 0 decompress. |

**RKNN_cna_dcomp_amount1**

Address: Operational Base + offset (0x1144)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | dcomp_amount1<br>Amount of the weight decompress for the 1 decompress. |

**RKNN_cna_dcomp_amount2**

Address: Operational Base + offset (0x1148)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | dcomp_amount2<br>Amount of the weight decompress for the 2 decompress. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

**RKNN_cna_dcomp_amount3**

Address: Operational Base + offset (0x114C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | dcomp_amount3<br>Amount of the weight decompress for the 3 decompress. |

**RKNN_cna_dcomp_amount4**

Address: Operational Base + offset (0x1150)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | dcomp_amount4<br>Amount of the weight decompress for the 4 decompress. |

**RKNN_cna_dcomp_amount5**

Address: Operational Base + offset (0x1154)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | dcomp_amount5<br>Amount of the weight decompress for the 5 decompress. |

**RKNN_cna_dcomp_amount6**

Address: Operational Base + offset (0x1158)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | dcomp_amount6<br>Amount of the weight decompress for the 6 decompress. |

**RKNN_cna_dcomp_amount7**

Address: Operational Base + offset (0x115C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | dcomp_amount7<br>Amount of the weight decompress for the 7 decompress. |

**RKNN_cna_dcomp_amount8**

Address: Operational Base + offset (0x1160)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | dcomp_amount8<br>Amount of the weight decompress for the 8 decompress. |

**RKNN_cna_dcomp_amount9**

Address: Operational Base + offset (0x1164)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | dcomp_amount9<br>Amount of the weight decompress for the 9 decompress. |

**RKNN_cna_dcomp_amount10**

Address: Operational Base + offset (0x1168)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | dcomp_amount10<br>Amount of the weight decompress for the 10 decompress. |

**RKNN_cna_dcomp_amount11**

Address: Operational Base + offset (0x116C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | dcomp_amount11<br>Amount of the weight decompress for the 11 decompress. |

**RKNN_cna_dcomp_amount12**

Address: Operational Base + offset (0x1170)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | dcomp_amount12<br>Amount of the weight decompress for the 12 decompress. |

**RKNN_cna_dcomp_amount13**

Address: Operational Base + offset (0x1174)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | dcomp_amount13<br>Amount of the weight decompress for the 13 decompress. |

**RKNN_cna_dcomp_amount14**

Address: Operational Base + offset (0x1178)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | dcomp_amount14<br>Amount of the weight decompress for the 14 decompress. |

**RKNN_cna_dcomp_amount15**

Address: Operational Base + offset (0x117C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | dcomp_amount15<br>Amount of the weight decompress for the 15 decompress. |

**RKNN_cna_cvt_con5**

Address: Operational Base + offset (0x1180)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | per_channel_cvt_en<br>convert enable.<br>Per channel enable CVT function.<br>Int 4 has 32 channels in total for 128 bits.<br>Int 8 16 channel... |

**RKNN_cna_pad_con1**

Address: Operational Base + offset (0x1184)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | pad_value<br>Pad value. |

**RKNN_core_s_status**

Address: Operational Base + offset (0x3000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17:16 | RO | 0x0 | status_1<br>Executer 1 status.<br>2'd0: Executer 1 is in idle state;<br>2'd1: Executer 1 is operating;<br>2'd2: Executer 1 is operating, executer 1 is waiting to operate;<br>2'd3: Reserved. |
| 15:2 | RO | 0x0000 | reserved |
| 1:0 | RO | 0x0 | status_0<br>Executer 0 status.<br>2'd0: Executer 0 is in idle state;<br>2'd1: Executer 0 is operating;<br>2'd2: Executer 0 is operating, executer 1 is waiting to operate;<br>2'd3: Reserved. |

**RKNN_core_s_pointer**

Address: Operational Base + offset (0x3004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16 | RO | 0x0 | executer<br>Which register group to be used.<br>1'd0: Executer group 0;<br>1'd1: Executer group 1. |
| 15:6 | RO | 0x000 | reserved |
| 5 | W1C | 0x0 | executer_pp_clear<br>Clear executer group pointer.<br>Set this bit to 1 to clear pointer to 0. |
| 4 | W1C | 0x0 | pointer_pp_clear<br>Clear register group pointer.<br>Set this bit to 1 to clear pointer to 0. |
| 3 | RW | 0x0 | pointer_pp_mode<br>Register group ping-pong mode.<br>1'd0: Pointer ping-pong by executer;<br>eg. if current executer is 0, next pointer will toggle to 1;<br>1'd1: Pointer ping-pong by pointer;<br>eg. if current pointer is 0, next pointer will toggle to 1. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | executer_pp_en<br>Executer group ping-pong enable.<br>1'd0: Disable;<br>1'd1: Enable. |
| 1 | RW | 0x0 | pointer_pp_en<br>Register group ping-pong enable.<br>1'd0: Disable;<br>1'd1: Enable. |
| 0 | RW | 0x0 | pointer<br>Which register group ready to be set.<br>1'd0: Register group 0;<br>1'd1: Register group 1. |

**RKNN_core_operation_enable**

Address: Operational Base + offset (0x3008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | op_en<br>Set this register will trigger core block operate.<br>This register and after this are all shadowed for ping-pong operation.<br>1'd0: Disable;<br>1'd1: Enable. |

**RKNN_core_mac_gating**

Address: Operational Base + offset (0x300C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:27 | RO | 0x00 | reserved |
| 26:0 | RW | 0x7800800 | slcg_op_en<br>Soft clock gating signals. |

**RKNN_core_misc_cfg**

Address: Operational Base + offset (0x3010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:14 | RW | 0x00 | soft_gating<br>Accumulate soft gating signal. |
| 13:11 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 10:8 | RW | 0x0 | proc_precision<br>Process precision<br>3'd0: Input precision is int 8;<br>3'd1: Input data precision is int 16;<br>3'd2: Input data precision is float 16;<br>3'd3: Input data precision is bfloat 16;<br>3'd4: Reserved;<br>3'd5: Reserved;<br>3'd6: Input data precision is int4;<br>3'd7: Input data precision is tf32. |
| 7:2 | RO | 0x00 | reserved |
| 1 | RW | 0x0 | dw_en<br>Depthwise enable<br>1'd0: Disable;<br>1'd1: Depthwise mode enable. |
| 0 | RW | 0x0 | qd_en<br>Quantify feature data calculate enable<br>1'd0: Disable;<br>1'd1: Enable. |

**RKNN_core_dataout_size_0**

Address: Operational Base + offset (0x3014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | dataout_height<br>Data out height<br>Data height after activation. |
| 15:0 | RW | 0x0000 | dataout_width<br>Data out width.<br>Data width after activation. |

**RKNN_core_dataout_size_1**

Address: Operational Base + offset (0x3018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | dataout_channel<br>Data out channel number<br>Data channel number after activation. |

**RKNN_core_clip_truncate**

Address: Operational Base + offset (0x301C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 6 | RW | 0x0 | round_type<br>Rounding type<br>1'b0: Odd in, even not;<br>1'b1: Round-up 0.5 to 1. |
| 5 | RO | 0x0 | reserved |
| 4:0 | RW | 0x00 | clip_truncate<br>Truncate bits number. |

**RKNN_dpu_s_status**

Address: Operational Base + offset (0x4000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17:16 | RO | 0x0 | status_1<br>Executer 1 status.<br>2'd0: Executer 1 is in idle state;<br>2'd1: Executer 1 is operating;<br>2'd2: Executer 1 is operating, executer 1 is waiting to operate;<br>2'd3: Reserved. |
| 15:2 | RO | 0x0000 | reserved |
| 1:0 | RO | 0x0 | status_0<br>Executer 0 status.<br>2'd0: Executer 0 is in idle state;<br>2'd1: Executer 0 is operating;<br>2'd2: Executer 0 is operating, executer 1 is waiting to operate;<br>2'd3: Reserved. |

**RKNN_dpu_s_pointer**

Address: Operational Base + offset (0x4004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16 | RO | 0x0 | executer<br>Which register group to be used.<br>1'd0: Executer group 0;<br>1'd1: Executer group 1. |
| 15:6 | RO | 0x000 | reserved |
| 5 | W1C | 0x0 | executer_pp_clear<br>Clear executer group pointer.<br>Set this bit to 1 to clear pointer to 0. |
| 4 | W1C | 0x0 | pointer_pp_clear<br>Clear register group pointer.<br>Set this bit to 1 to clear pointer to 0. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RW | 0x0 | pointer_pp_mode<br>Register group ping-pong mode.<br>1'd0: Pointer ping-pong by executer;<br>eg. if current executer is 0, next pointer will toggle to 1;<br>1'd1: Pointer ping-pong by pointer;<br>eg. if current pointer is 0, next pointer will toggle to 1. |
| 2 | RW | 0x0 | executer_pp_en<br>Executer group ping-pong enable.<br>1'd0: Disable;<br>1'd1: Enable. |
| 1 | RW | 0x0 | pointer_pp_en<br>Register group ping-pong enable.<br>1'd0: Disable;<br>1'd1: Enable. |
| 0 | RW | 0x0 | pointer<br>Which register group ready to be set.<br>1'd0: Register group 0;<br>1'd1: Register group 1. |

**RKNN_dpu_operation_enable**

Address: Operational Base + offset (0x4008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | op_en<br>Set this register will trigger DPU block operate.<br>This register and after this are all shadowed for ping-pong operation.<br>1'd0: Disable;<br>1'd1: Enable. |

**RKNN_dpu_feature_mode_cfg**

Address: Operational Base + offset (0x400C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | comb_use<br>Combine use, same as DPU_RDMA comb_use[0]. |
| 30 | RW | 0x0 | tp_en<br>If enable transpose. |
| 29:26 | RW | 0x0 | rgp_type<br>Regroup type.<br>4'd0: Cut all input (128bit);<br>4'd1: Cut 4bit;<br>4'd2: Cut 8bit;<br>4'd3: Cut 16bit;<br>4'd4: Cut 32bit;<br>4'd5: Cut 64bit. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 25 | RW | 0x0 | nonalign<br>If non-align mode is enabled.<br>If the output data flow is the same as the input data flow, this mode can be used. |
| 24:9 | RW | 0x0000 | surf_len<br>In non-align mode, how many 8bytes to be stored. |
| 8:5 | RW | 0x0 | burst_len<br>Burst length.<br>4'd3: Burst4;<br>4'd7: Burst8;<br>4'd15: Burst16. |
| 4:3 | RW | 0x0 | conv_mode<br>Convolution mode.<br>2'd0: Normal convolution mode;<br>2'd1: Reserved;<br>2'd2: Reserved;<br>2'd3: Depthwise convolution mode. |
| 2:1 | RW | 0x0 | output_mode<br>Where the DPU core output goes.<br>[0]: If the output goes to PPU, high is active;<br>[1]: If the output goes to outside, high is active. |
| 0 | RW | 0x0 | flying_mode<br>Flying mode enable.<br>1'd0: DPU core main data is from convolution output;<br>1'd1: DPU core main data is from MRDMA; |

**RKNN_dpu_data_format**

Address: Operational Base + offset (0x4010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RW | 0x0 | out_precision<br>Output precision.<br>3'd0: Integer 8bit;<br>3'd1: Integer 16bit;<br>3'd2: Float point 16bit;<br>3'd3: Bfloat 16bit;<br>3'd4: Integer 32bit;<br>3'd5: Float point 32bit;<br>3'd6: Integer 4bit. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 28:26 | RW | 0x0 | in_precision<br>Input precision same with DPU_RDMA.<br>3'd0: Integer 8bit;<br>3'd1: Integer 16bit;<br>3'd2: Float point 16bit;<br>3'd3: Bfloat 16bit;<br>3'd4: Integer 32bit;<br>3'd5: Float point 32bit;<br>3'd6: Integer 4bit. |
| 25:16 | RW | 0x000 | ew_truncate_neg<br>Shift value in EW core for negative data. |
| 15:10 | RW | 0x00 | bn_mul_shift_value_neg<br>Shift value in BN core for negative data. |
| 9:4 | RW | 0x00 | bs_mul_shift_value_neg<br>Shift value in BS core for negative data. |
| 3 | RW | 0x0 | mc_surf_out<br>How many surfaces serial the DPU output.<br>1'd0: Output feature obey the rule of 16byte align for one pixel;<br>1'd1: Output feature can output 2 surface serial or 4 surf serials. |
| 2:0 | RW | 0x0 | proc_precision<br>Proc precision.<br>3'd0: Integer 8bit;<br>3'd1: Integer 16bit;<br>3'd2: Float point 16bit;<br>3'd3: Bfloat 16bit;<br>3'd4: Integer 32bit;<br>3'd5: Float point 32bit;<br>3'd6: Integer 4bit. |

**RKNN_dpu_offset_pend**

Address: Operational Base + offset (0x4014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | offset_pend<br>What value the extra channel be set. |

**RKNN_dpu_dst_base_addr**

Address: Operational Base + offset (0x4020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | dst_base_addr<br>Destination base address. |
| 3:0 | RO | 0x0 | reserved |

**RKNN_dpu_dst_surf_stride**

Address: Operational Base + offset (0x4024)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | dst_surf_stride<br>Output shape surface stride. |
| 3:0 | RO | 0x0 | reserved |

**RKNN_dpu_data_cube_width**

Address: Operational Base + offset (0x4030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |
| 12:0 | RW | 0x0000 | width<br>Width of the input cube. |

**RKNN_dpu_data_cube_height**

Address: Operational Base + offset (0x4034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:25 | RO | 0x00 | reserved |
| 24:22 | RW | 0x0 | minmax_ctl<br>Configuration of the minmax op.<br>[0]: Enable minmax op;<br>[1]: Minmax type;<br>[2]: Probability only. |
| 21:13 | RO | 0x000 | reserved |
| 12:0 | RW | 0x0000 | height<br>Height of the input cube. |

**RKNN_dpu_data_cube_notch_addr**

Address: Operational Base + offset (0x4038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:16 | RW | 0x0000 | notch_addr_1<br>How many pixels from the end of width to the end of the shape line end. |
| 15:13 | RO | 0x0 | reserved |
| 12:0 | RW | 0x0000 | notch_addr_0<br>How many pixels from the end of width to the end of the shape line end. |

**RKNN_dpu_data_cube_channel**

Address: Operational Base + offset (0x403C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:16 | RW | 0x0000 | orig_channel<br>Original output channel. |
| 15:13 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12:0 | RW | 0x0000 | channel<br>Cube channel. |

**RKNN_dpu_bs_cfg**

Address: Operational Base + offset (0x4040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:16 | RW | 0x0 | bs_alu_algo<br>BS core ALU op type.<br>4'd0: Reserved;<br>4'd1: Reserved;<br>4'd2: Add<br>4'd3: Reserved;<br>4'd4: Minus;<br>4'd5: Reserved;<br>4'd6: Reserved;<br>4'd7: Reserved;<br>4'd8: Reserved. |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | bs_alu_src<br>Where the ALU operand from.<br>1'd0: From configure register;<br>1'd1: From outside. |
| 7 | RW | 0x0 | bs_relux_en<br>If enable RELUX.<br>1'd0: Disable;<br>1'd1: Enable. |
| 6 | RW | 0x0 | bs_relu_bypass<br>If bypass BS core RELU op.<br>1'd0: Do not bypass;<br>1'd1: Bypass. |
| 5 | RW | 0x0 | bs_mul_prelu<br>If enable MUL PRELU.<br>1'd0: Disable;<br>1'd1: Enable. |
| 4 | RW | 0x0 | bs_mul_bypass<br>If bypass BS core MUL op.<br>1'd0: Do not bypass;<br>1'd1: Bypass. |
| 3:2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | bs_alu_bypass<br>If bypass BS core ALU op.<br>1'd0: Do not bypass;<br>1'd1: Bypass. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | bs_bypass<br>If bypass BS core.<br>1'd0: Do not bypass bs core;<br>1'd1: Bypass bs core. |

**RKNN_dpu_bs_alu_cfg**

Address: Operational Base + offset (0x4044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | bs_alu_operand<br>Bs core ALU operand. |

**RKNN_dpu_bs_mul_cfg**

Address: Operational Base + offset (0x4048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | bs_mul_operand<br>BS core MUL operand. |
| 15:14 | RO | 0x0 | reserved |
| 13:8 | RW | 0x00 | bs_mul_shift_value<br>Shift value in BS core for positive data. |
| 7:2 | RO | 0x00 | reserved |
| 1 | RW | 0x0 | bs_truncate_src<br>Where the shift value from.<br>1'd0: From configure register;<br>1'd1: From outside. |
| 0 | RW | 0x0 | bs_mul_src<br>Where the MUL operand from.<br>1'd0: From configure register;<br>1'd1: From outside. |

**RKNN_dpu_bs_relux_cmp_value**

Address: Operational Base + offset (0x404C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | bs_relux_cmp_dat<br>Value of the RELUX compare with. |

**RKNN_dpu_bs_ow_cfg**

Address: Operational Base + offset (0x4050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RW | 0x0 | rgp_cnter<br>Regroup counter.<br>4'd0: Select all data;<br>4'd1: Select 1 from every 2;<br>4'd2: Select 1 from every 4;<br>4'd3: Select 1 from every 8;<br>Else: Reserved. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 27 | RW | 0x0 | tp_org_en<br>If enable original transpose.<br>1'd0: Disable;<br>1'd1: Enable. |
| 26:11 | RO | 0x0000 | reserved |
| 10:8 | RW | 0x0 | size_e_2<br>How many 8 channels in a row the last output line (minus 1). |
| 7:5 | RW | 0x0 | size_e_1<br>How many 8 channels in a row the middle output line (minus 1). |
| 4:2 | RW | 0x0 | size_e_0<br>How many 8 channels in a row the first output line (minus 1). |
| 1 | RW | 0x0 | od_bypass<br>If bypass CPEND.<br>1'd0: Do not bypass;<br>1'd1: Bypass. |
| 0 | RW | 0x0 | ow_src<br>Where the CPEND operand from.<br>1'd0: From configure register;<br>1'd1: From outside. |

**RKNN_dpu_bs_ow_op**

Address: Operational Base + offset (0x4054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | ow_op<br>CPEND operand. |

**RKNN_dpu_wdma_size_0**

Address: Operational Base + offset (0x4058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27 | RW | 0x0 | tp_precision<br>Transpose precision.<br>1'd0: 8bit;<br>1'd1: 16bit. |
| 26:16 | RW | 0x000 | size_c_wdma<br>Size_c for DPU_WDMA. |
| 15:13 | RO | 0x0 | reserved |
| 12:0 | RW | 0x0000 | channel_wdma<br>Channel for DPU_WDMA. |

**RKNN_dpu_wdma_size_1**

Address: Operational Base + offset (0x405C)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:16 | RW | 0x0000 | height_wdma<br>Height for DPU_WDMA. |
| 15:13 | RO | 0x0 | reserved |
| 12:0 | RW | 0x0000 | width_wdma<br>Width for DPU_WDMA. |

**RKNN_dpu_bn_cfg**

Address: Operational Base + offset (0x4060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:16 | RW | 0x0 | bn_alu_algo<br>BS core ALU op type.<br>4'd0: Reserved;<br>4'd1: Reserved;<br>4'd2: Add<br>4'd3: Reserved;<br>4'd4: Minus;<br>4'd5: Reserved;<br>4'd6: Reserved;<br>4'd7: Reserved;<br>4'd8: Reserved. |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | bn_alu_src<br>Where the ALU operand from<br>1'd0: From configure register;<br>1'd1: From outside. |
| 7 | RW | 0x0 | bn_relux_en<br>If enable RELUX.<br>1'd0: Disable;<br>1'd1: Enable. |
| 6 | RW | 0x0 | bn_relu_bypass<br>If bypass BN core RELU op.<br>1'd0: Do not bypass;<br>1'd1: Bypass. |
| 5 | RW | 0x0 | bn_mul_prelu<br>If enable MUL PRELU.<br>1'd0: Disable;<br>1'd1: Enable. |
| 4 | RW | 0x0 | bn_mul_bypass<br>If bypass BN core MUL op.<br>1'd0: Do not bypass;<br>1'd1: Bypass. |
| 3:2 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | bn_alu_bypass<br>If bypass BN core ALU op.<br>1'd0: Do not bypass;<br>1'd1: Bypass. |
| 0 | RW | 0x0 | bn_bypass<br>If bypass BN core.<br>1'd0: Do not bypass BN core;<br>1'd1: Bypass BN core. |

**RKNN_dpu_bn_alu_cfg**

Address: Operational Base + offset (0x4064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | bn_alu_operand<br>BN core ALU operand. |

**RKNN_dpu_bn_mul_cfg**

Address: Operational Base + offset (0x4068)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | bn_mul_operand<br>BN core MUL operand. |
| 15:14 | RO | 0x0 | reserved |
| 13:8 | RW | 0x00 | bn_mul_shift_value<br>Shift value in BN core for positive data. |
| 7:2 | RO | 0x00 | reserved |
| 1 | RW | 0x0 | bn_truncate_src<br>Where the shift value from<br>1'd0: From configure register;<br>1'd1: From outside. |
| 0 | RW | 0x0 | bn_mul_src<br>Where the MUL operand from.<br>1'd0: From configure register;<br>1'd1: From outside. |

**RKNN_dpu_bn_relux_cmp_value**

Address: Operational Base + offset (0x406C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | bn_relux_cmp_dat<br>RELUX compare data in BN core. |

**RKNN_dpu_ew_cfg**

Address: Operational Base + offset (0x4070)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | ew_cvt_type<br>Convert type of EW input convert when if 0.5<br>1'd0: Mul first;<br>1'd1: Add first. |
| 30 | RW | 0x0 | ew_cvt_round<br>Rounding type of EW input convert when if 0.5<br>1'd0: If the integer is odd, carry 1;<br>1'd1: Carry 1 no matter what the integer is. |
| 29:28 | RW | 0x0 | ew_data_mode<br>Data mode of the data from ERDMA. |
| 27:24 | RO | 0x0 | reserved |
| 23:22 | RW | 0x0 | edata_size<br>Data size of the cube from ERDMA.<br>2'd0: 4bit;<br>2'd1: 8bit;<br>2'd2: 16bit;<br>2'd3: 32bit. |
| 21 | RW | 0x0 | ew_equal_en<br>Min max equal enable.<br>1'd0: Disable;<br>1'd1: Enable. |
| 20 | RW | 0x0 | ew_binary_en<br>Min max binary enable.<br>1'd0: Disable;<br>1'd1: Enable. |
| 19:16 | RW | 0x0 | ew_alu_algo<br>EW core ALU op type.<br>4'd0: Max;<br>4'd1: Min;<br>4'd2: Add;<br>4'd3: Div;<br>4'd4: Minus;<br>4'd5: Abs;<br>4'd6: Neg;<br>4'd7: Floor;<br>4'd8: Ceil. |
| 15:11 | RO | 0x00 | reserved |
| 10 | RW | 0x0 | ew_relux_en<br>If enable RELUX.<br>1'd0: Disable;<br>1'd1: Enable. |
| 9 | RW | 0x0 | ew_relu_bypass<br>If bypass EW core RELU op.<br>1'd0: Do not bypass;<br>1'd1: Bypass. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RW | 0x0 | ew_op_cvt_bypass<br>If bypass EW input converter.<br>1'd0: Do not bypass;<br>1'd1: Bypass. |
| 7 | RW | 0x0 | ew_lut_bypass<br>If bypass LUT.<br>1'd0: Do not bypass;<br>1'd1: Bypass. |
| 6 | RW | 0x0 | ew_op_src<br>Where the operand from<br>1'd0: From configure register;<br>1'd1: From outside. |
| 5 | RW | 0x0 | ew_mul_prelu<br>If enable MUL PRELU.<br>1'd0: Disable;<br>1'd1: Enable. |
| 4:3 | RO | 0x0 | reserved |
| 2 | RW | 0x0 | ew_op_type<br>Operator type.<br>1'd0: ALU;<br>1'd1: MUL. |
| 1 | RW | 0x0 | ew_op_bypass<br>If bypass EW core ALU and MUL op.<br>1'd0: Do not bypass;<br>1'd1: Bypass. |
| 0 | RW | 0x0 | ew_bypass<br>If bypass EW core.<br>1'd0: Do not bypass EW core;<br>1'd1: Bypass EW core. |

**RKNN_dpu_ew_cvt_offset_value**

Address: Operational Base + offset (0x4074)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ew_op_cvt_offset<br>EW convert offset. |

**RKNN_dpu_ew_cvt_scale_value**

Address: Operational Base + offset (0x4078)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RW | 0x000 | ew_truncate<br>EW core shift value. |
| 21:16 | RW | 0x00 | ew_op_cvt_shift<br>EW convert shift value. |
| 15:0 | RW | 0x0000 | ew_op_cvt_scale<br>EW convert scale. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

**RKNN_dpu_ew_relux_cmp_value**

Address: Operational Base + offset (0x407C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ew_relux_cmp_dat<br>EW RELUX compare data. |

**RKNN_dpu_out_cvt_offset**

Address: Operational Base + offset (0x4080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | out_cvt_offset<br>Offset of the output converter. |

**RKNN_dpu_out_cvt_scale**

Address: Operational Base + offset (0x4084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16 | RW | 0x0 | fp32tofp16_en<br>If enable output from fp32 to fp16.<br>1'd0: Disable;<br>1'd1: Enable. |
| 15:0 | RW | 0x0000 | out_cvt_scale<br>Scale of the output converter. |

**RKNN_dpu_out_cvt_shift**

Address: Operational Base + offset (0x4088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | cvt_type<br>Convert type of out convert when if 0.5.<br>1'd0: MUL first;<br>1'd1: ALU first. |
| 30 | RW | 0x0 | cvt_round<br>Rounding type of out convert when if 0.5.<br>1'd0: If the integer is odd, carry 1;<br>1'd1: Carry 1 no matter what the integer is. |
| 29:20 | RO | 0x000 | reserved |
| 19:12 | RW | 0x00 | minus_exp<br>Minus exp of out CVT. |
| 11:0 | RW | 0x000 | out_cvt_shift<br>Shift of the output converter. |

**RKNN_dpu_ew_op_value_0**

Address: Operational Base + offset (0x4090)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ew_operand_0<br>The 1st EW operand for EW core op. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

**RKNN_dpu_ew_op_value_1**

Address: Operational Base + offset (0x4094)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ew_operand_1<br>The 2nd EW operand for EW core op. |

**RKNN_dpu_ew_op_value_2**

Address: Operational Base + offset (0x4098)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ew_operand_2<br>the 3thd EW operand for EW core op. |

**RKNN_dpu_ew_op_value_3**

Address: Operational Base + offset (0x409C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ew_operand_3<br>the 4th EW operand for EW core op. |

**RKNN_dpu_ew_op_value_4**

Address: Operational Base + offset (0x40A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ew_operand_4<br>the 5th EW operand for EW core op. |

**RKNN_dpu_ew_op_value_5**

Address: Operational Base + offset (0x40A4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ew_operand_5<br>The 6th EW operand for EW core op. |

**RKNN_dpu_ew_op_value_6**

Address: Operational Base + offset (0x40A8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ew_operand_6<br>The 7th EW operand for EW core op. |

**RKNN_dpu_ew_op_value_7**

Address: Operational Base + offset (0x40AC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ew_operand_7<br>The 8th EW operand for EW core op. |

**RKNN_dpu_surface_add**

Address: Operational Base + offset (0x40C0)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | surf_add<br>How many surfaces in a row. |
| 3:0 | RO | 0x0 | reserved |

**RKNN_dpu_lut_access_cfg**

Address: Operational Base + offset (0x4100)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17 | RW | 0x0 | lut_access_type<br>Access type.<br>1'd0: Read;<br>1'd1: Write. |
| 16 | RW | 0x0 | lut_table_id<br>Access Id.<br>1'd0: LE LUT;<br>1'd1: LO LUT. |
| 15:10 | RO | 0x00 | reserved |
| 9:0 | RW | 0x000 | lut_addr<br>Access address. |

**RKNN_dpu_lut_access_data**

Address: Operational Base + offset (0x4104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:0 | RW | 0x0000 | lut_access_data<br>Configuration of LUT access data. |

**RKNN_dpu_lut_cfg**

Address: Operational Base + offset (0x4108)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7 | RW | 0x0 | lut_cal_sel<br>LUT calculate sel.<br>Only useful when lut_expand_en is 1. |
| 6 | RW | 0x0 | lut_hybrid_priority<br>LUT hybrid flow priority.<br>1'd0: LE LUT;<br>1'd1: LO LUT. |
| 5 | RW | 0x0 | lut_oflow_priority<br>Priority when over flow happened.<br>1'd0: LE LUT;<br>1'd1: LO LUT. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | lut_uflow_priority<br>Priority when under flow happened.<br>1'd0: LE LUT;<br>1'd1: LO LUT. |
| 3:2 | RW | 0x0 | lut_lo_le_mux<br>LO LUT and LE LUT mux. |
| 1 | RW | 0x0 | lut_expand_en<br>If expand two small LUT to a larger LUT.<br>1'd0: Disable;<br>1'd1: Enable. |
| 0 | RW | 0x0 | lut_road_sel<br>LUT road sel.<br>1'd0: 1st;<br>1'd1: 2nd. |

**RKNN_dpu_lut_info**

Address: Operational Base + offset (0x410C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23:16 | RW | 0x00 | lut_lo_index_select<br>LUT LO index selected.<br>Used in index generator, choose some bits to be the index. |
| 15:8 | RW | 0x00 | lut_le_index_select<br>LUT LE index selected.<br>Used in index generator, choose some bits to be the index. |
| 7:0 | RO | 0x00 | reserved |

**RKNN_dpu_lut_le_start**

Address: Operational Base + offset (0x4110)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | lut_le_start<br>LE LUT start point. |

**RKNN_dpu_lut_le_end**

Address: Operational Base + offset (0x4114)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | lut_le_end<br>LE LUT end point. |

**RKNN_dpu_lut_lo_start**

Address: Operational Base + offset (0x4118)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | lut_lo_start<br>LO LUT start point. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**RKNN_dpu_lut_lo_end**

Address: Operational Base + offset (0x411C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | lut_lo_end<br>LO LUT end point. |

**RKNN_dpu_lut_le_slope_scale**

Address: Operational Base + offset (0x4120)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | lut_le_slope_oflow_scale<br>LE LUT slope scale if over flow. |
| 15:0 | RW | 0x0000 | lut_le_slope_uflow_scale<br>LE LUT slope scale if under flow. |

**RKNN_dpu_lut_le_slope_shift**

Address: Operational Base + offset (0x4124)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9:5 | RW | 0x00 | lut_le_slope_oflow_shift<br>LE LUT slope shift if over flow. |
| 4:0 | RW | 0x00 | lut_le_slope_uflow_shift<br>LE LUT slope shift if under flow. |

**RKNN_dpu_lut_lo_slope_scale**

Address: Operational Base + offset (0x4128)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | lut_lo_slope_oflow_scale<br>LO LUT slope scale if over flow. |
| 15:0 | RW | 0x0000 | lut_lo_slope_uflow_scale<br>LO LUT slope scale if under flow. |

**RKNN_dpu_lut_lo_slope_shift**

Address: Operational Base + offset (0x412C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9:5 | RW | 0x00 | lut_lo_slope_oflow_shift<br>LO LUT slope shift if over flow. |
| 4:0 | RW | 0x00 | lut_lo_slope_uflow_shift<br>LO LUT slope shift if under flow. |

**RKNN_dpu_rdma_s_status**

Address: Operational Base + offset (0x5000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17:16 | RO | 0x0 | status_1<br>Executer 1 status.<br>2'd0: Executer 1 is in idle state;<br>2'd1: Executer 1 is operating;<br>2'd2: Executer 1 is operating, executer 1 is waiting to operate;<br>2'd3: Reserved. |
| 15:2 | RO | 0x0000 | reserved |
| 1:0 | RO | 0x0 | status_0<br>Executer 0 status.<br>2'd0: Executer 0 is in idle state;<br>2'd1: Executer 0 is operating;<br>2'd2: Executer 0 is operating, executer 1 is waiting to operate;<br>2'd3: Reserved. |

**RKNN_dpu_rdma_s_pointer**

Address: Operational Base + offset (0x5004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16 | RO | 0x0 | executer<br>Which register group to be used.<br>1'd0: Executer group 0;<br>1'd1: Executer group 1. |
| 15:6 | RO | 0x000 | reserved |
| 5 | W1C | 0x0 | executer_pp_clear<br>Clear executer group pointer.<br>Set this bit to 1 to clear pointer to 0. |
| 4 | W1C | 0x0 | pointer_pp_clear<br>Clear register group pointer.<br>Set this bit to 1 to clear pointer to 0. |
| 3 | RW | 0x0 | pointer_pp_mode<br>Register group ping-pong mode.<br>1'd0: Pointer ping-pong by executer;<br>eg. if current executer is 0, next pointer will toggle to 1;<br>1'd1: Pointer ping-pong by pointer;<br>eg. if current pointer is 0, next pointer will toggle to 1. |
| 2 | RW | 0x0 | executer_pp_en<br>Executer group ping-pong enable.<br>1'd0: Disable;<br>1'd1: Enable. |
| 1 | RW | 0x0 | pointer_pp_en<br>Register group ping-pong enable.<br>1'd0: Disable;<br>1'd1: Enable. |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | pointer<br>Which register group ready to be set.<br>1'd0: Register group 0;<br>1'd1: Register group 1. |

**RKNN_dpu_rdma_operation_enable**

Address: Operational Base + offset (0x5008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | op_en<br>Set this register will trigger DPU_RDMA block operate.<br>This register and after this are all shadowed for ping-pong operation.<br>1'd0: Disable;<br>1'd1: Enable. |

**RKNN_dpu_rdma_data_cube_width**

Address: Operational Base + offset (0x500C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |
| 12:0 | RW | 0x0000 | width<br>Input feature width (need to minus 1). |

**RKNN_dpu_rdma_data_cube_height**

Address: Operational Base + offset (0x5010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:16 | RW | 0x0000 | ew_line_notch_addr<br>Line notch of EW. |
| 15:13 | RO | 0x0 | reserved |
| 12:0 | RW | 0x0000 | height<br>Input feature height (need to minus 1). |

**RKNN_dpu_rdma_data_cube_channel**

Address: Operational Base + offset (0x5014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |
| 12:0 | RW | 0x0000 | channel<br>Input feature channel (need to minus 1). |

**RKNN_dpu_rdma_src_base_addr**

Address: Operational Base + offset (0x5018)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | src_base_addr<br>Fly mode source address. |

**RKNN_dpu_rdma_brdma_cfg**

Address: Operational Base + offset (0x501C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4:1 | RW | 0x0 | brdma_data_use<br>How many data type need to be read.<br>[0]: If read ALU operand, set 1 to enable;<br>[1]: If read CPEND operand, set 1 to enable;<br>[2]: If read MUL operand, set 1 to enable;<br>[3]: If read TRT operand, set 1 to enable. |
| 0 | RO | 0x0 | reserved |

**RKNN_dpu_rdma_bs_base_addr**

Address: Operational Base + offset (0x5020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | bs_base_addr<br>Base address to read BS ALU, BS CPEND, BS MUL operand. |

**RKNN_dpu_rdma_nrdma_cfg**

Address: Operational Base + offset (0x5028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:5 | RO | 0x0000000 | reserved |
| 4:1 | RW | 0x0 | nrdma_data_use<br>How many data type need to be read.<br>[0]: If read ALU operand, set 1 to enable;<br>[1]: If read CPEND operand, set 1 to enable, (tie to 0, cause BN do not have CPEND);<br>[2]: If read MUL operand, set 1 to enable;<br>[3]: If read TRT operand, set 1 to enable. |
| 0 | RO | 0x0 | reserved |

**RKNN_dpu_rdma_bn_base_addr**

Address: Operational Base + offset (0x502C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | bn_base_addr<br>Base address to read BN ALU, BN MUL operand. |

**RKNN_dpu_rdma_erdma_cfg**

Address: Operational Base + offset (0x5034)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | erdma_data_mode<br>If the read data is per channel or per pixel<br>2'd0: Per channel;<br>2'd1: Per pixel;<br>2'd2: Per channel by pixel;<br>2'd3: Reserved. |
| 29 | RW | 0x0 | erdma_surf_mode<br>Surface mode of the EW cube.<br>1'd0: 1 surface series;<br>1'd1: 2 surface series. |
| 28 | RW | 0x0 | erdma_nonalign<br>If read the EW cube in non-align mode.<br>1'd0: Do not use non-align mode;<br>1'd1: Use non-align mode. |
| 27:4 | RO | 0x000000 | reserved |
| 3:2 | RW | 0x0 | erdma_data_size<br>What the precision of the cube that the ERDMA read.<br>2'd0: 4bit;<br>2'd1: 8bit;<br>2'd2: 16bit;<br>2'd3: 32bit. |
| 1 | RW | 0x0 | ov4k_bypass<br>Separate the burst command of over 4k to 2 independent burst commands.<br>1'd0: Enable this feature;<br>1'd1: Bypass this feature. |
| 0 | RW | 0x0 | erdma_disable<br>If disable ERDMA.<br>1'd0: Do not disable ERDMA;<br>1'd1: Disable ERDMA. |

**RKNN_dpu_rdma_ew_base_addr**

Address: Operational Base + offset (0x5038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | ew_base_addr<br>Base address to read EW operand. |

**RKNN_dpu_rdma_ew_surf_stride**

Address: Operational Base + offset (0x5040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | ew_surf_stride<br>The surface stride of the element wise feature map;<br>If erdma_data_mode is per channel, it need set to be 1. |
| 3:0 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**RKNN_dpu_rdma_feature_mode_cfg**

Address: Operational Base + offset (0x5044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17:15 | RW | 0x0 | in_precision<br>Input data precision.<br>3'd0: Integer 8bit;<br>3'd1: Integer 16bit;<br>3'd2: Gloat point 16bit;<br>3'd3: Bfloat 16bit;<br>3'd4: Integer 32bit;<br>3'd5: Float point 32bit;<br>3'd6: Integer 4bit. |
| 14:11 | RW | 0x0 | burst_len<br>Burst length.<br>4'd3: Burst4;<br>4'd7: Burst8;<br>4'd15: Burst16. |
| 10:8 | RW | 0x0 | comb_use<br>[0]: If enable MRDMA and ERDMA to read the same data;<br>[1]: Read the data to MRDMA;<br>[2]: Read the data to ERDMA. |
| 7:5 | RW | 0x0 | proc_precision<br>Process precision.<br>3'd0: Integer 8bit;<br>3'd1: Integer 16bit;<br>3'd2: Float point 16bit;<br>3'd3: Bfloat 16bit;<br>3'd4: Integer 32bit;<br>3'd5: Float point 32bit;<br>3'd6: Integer 4bit. |
| 4 | RW | 0x0 | mrdma_disable<br>If disable MRDMA.<br>1'd0: Do not disable MRDMA;<br>1'd1: Disable MRDMA. |
| 3 | RW | 0x0 | mrdma_fp16tofp32_en<br>If enable DPU input from fp16 to fp32. |
| 2:1 | RW | 0x0 | conv_mode<br>Convolution mode.<br>2'd0: Dc;<br>2'd1: Reserved;<br>2'd2: Reserved;<br>2'd3: Depthwise. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | flying_mode<br>Flying mode enable.<br>1'd0: DPU core main data is from convolution output;<br>1'd1: DPU core main data is from MRDMA. |

**RKNN_dpu_rdma_src_dma_cfg**

Address: Operational Base + offset (0x5048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:19 | RW | 0x0000 | line_notch_addr<br>How many pixels from the end of width end to the shape feature line end. |
| 18:14 | RO | 0x00 | reserved |
| 13 | RW | 0x0 | pooling_method<br>Pooling method<br>1'd0: Average pooling (up sampling can use this mode);<br>1'd1: Min or max pooling. |
| 12 | RW | 0x0 | unpooling_en<br>If enable un-pooling. |
| 11:9 | RW | 0x0 | kernel_stride_height<br>Un-pooling kernel stride height (minus 1). |
| 8:6 | RW | 0x0 | kernel_stride_width<br>Un-pooling kernel stride width (minus 1). |
| 5:3 | RW | 0x0 | kernel_height<br>Un-pooling kernel height (minus 1). |
| 2:0 | RW | 0x0 | kernel_width<br>Un-pooling kernel width (minus 1). |

**RKNN_dpu_rdma_surf_notch**

Address: Operational Base + offset (0x504C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | surf_notch_addr<br>How many pixels from the end of this process feature map to the end of the shape feature map. |
| 3:0 | RO | 0x0 | reserved |

**RKNN_dpu_rdma_pad_cfg**

Address: Operational Base + offset (0x5064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | pad_value<br>Pad value. |
| 15:7 | RO | 0x000 | reserved |
| 6:4 | RW | 0x0 | pad_top<br>Un-pooling top pad. |
| 3 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2:0 | RW | 0x0 | pad_left<br>Un-pooling left pad. |

**RKNN_dpu_rdma_weight**

Address: Operational Base + offset (0x5068)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | e_weight<br>The arbiter weight for ERDMA. |
| 23:16 | RW | 0x00 | n_weight<br>The arbiter weight for NRDMA. |
| 15:8 | RW | 0x00 | b_weight<br>The arbiter weight for BRDMA. |
| 7:0 | RW | 0x00 | m_weight<br>The arbiter weight for MRDMA. |

**RKNN_dpu_rdma_ew_surf_notch**

Address: Operational Base + offset (0x506C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | ew_surf_notch<br>Surface notch of EW. |
| 3:0 | RO | 0x0 | reserved |

**RKNN_ppu_s_status**

Address: Operational Base + offset (0x6000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |
| 17:16 | RO | 0x0 | status_1<br>Executer 1 status.<br>2'd0: Executer 1 is in idle state;<br>2'd1: Executer 1 is operating;<br>2'd2: Executer 1 is operating, executer 1 is waiting to operate;<br>2'd3: Reserved. |
| 15:2 | RO | 0x0000 | reserved |
| 1:0 | RO | 0x0 | status_0<br>Executer 0 status.<br>2'd0: Executer 0 is in idle state;<br>2'd1: Executer 0 is operating;<br>2'd2: Executer 0 is operating, executer 1 is waiting to operate;<br>2'd3: Reserved. |

**RKNN_ppu_s_pointer**

Address: Operational Base + offset (0x6004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 16 | RO | 0x0 | executer<br>Which register group to be used.<br>1'd0: Executer group 0;<br>1'd1: Executer group 1. |
| 15:6 | RO | 0x000 | reserved |
| 5 | W1C | 0x0 | executer_pp_clear<br>Clear executer group pointer.<br>Set this bit to 1 to clear pointer to 0. |
| 4 | W1C | 0x0 | pointer_pp_clear<br>Clear register group pointer.<br>Set this bit to 1 to clear pointer to 0. |
| 3 | RW | 0x0 | pointer_pp_mode<br>Register group ping-pong mode.<br>1'd0: Pointer ping-pong by executer;<br>eg. if current executer is 0, next pointer will toggle to 1;<br>1'd1: Pointer ping-pong by pointer;<br>eg. if current pointer is 0, next pointer will toggle to 1. |
| 2 | RW | 0x0 | executer_pp_en<br>Executer group ping-pong enable.<br>1'd0: Disable;<br>1'd1: Enable. |
| 1 | RW | 0x0 | pointer_pp_en<br>Register group ping-pong enable.<br>1'd0: Disable;<br>1'd1: Enable. |
| 0 | RW | 0x0 | pointer<br>Which register group ready to be set.<br>1'd0: Register group 0;<br>1'd1: Register group 1. |

**RKNN_ppu_operation_enable**

Address: Operational Base + offset (0x6008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | op_en<br>Set this register will trigger PPU block operate.<br>This register and after this are all shadowed for ping-pong operation.<br>1'd0: Disable;<br>1'd1: Enable. |

**RKNN_ppu_data_cube_in_width**

Address: Operational Base + offset (0x600C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12:0 | RW | 0x0000 | cube_in_width<br>Pooling cube width (need to minus 1). |

**RKNN_ppu_data_cube_in_height**

Address: Operational Base + offset (0x6010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |
| 12:0 | RW | 0x0000 | cube_in_height<br>Pooling cube height (need to minus 1). |

**RKNN_ppu_data_cube_in_channel**

Address: Operational Base + offset (0x6014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |
| 12:0 | RW | 0x0000 | cube_in_channel<br>Pooling cube channel (need to minus 1). |

**RKNN_ppu_data_cube_out_width**

Address: Operational Base + offset (0x6018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |
| 12:0 | RW | 0x0000 | cube_out_width<br>Pooling output cube width (need to minus 1). |

**RKNN_ppu_data_cube_out_height**

Address: Operational Base + offset (0x601C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |
| 12:0 | RW | 0x0000 | cube_out_height<br>Pooling output cube height (need to minus 1). |

**RKNN_ppu_data_cube_out_channel**

Address: Operational Base + offset (0x6020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |
| 12:0 | RW | 0x0000 | cube_out_channel<br>Pooling output cube channel (need to minus 1). |

**RKNN_ppu_operation_mode_cfg**

Address: Operational Base + offset (0x6024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 30 | RW | 0x0 | index_en<br>If enable output the position of each kernel.<br>1'd0: Disable;<br>1'd1: Enable. |
| 29 | RO | 0x0 | reserved |
| 28:16 | RW | 0x0000 | notch_addr<br>How many pixels from the end of the width end to the shape line end. |
| 15:8 | RO | 0x00 | reserved |
| 7:5 | RW | 0x0 | use_cnt<br>Use_cnt. |
| 4 | RW | 0x0 | flying_mode<br>Where the pooling cube from.<br>1'd0: DPU;<br>1'd1: Outside. |
| 3:2 | RO | 0x0 | reserved |
| 1:0 | RW | 0x0 | pooling_method<br>Pooling method.<br>2'd0: Average pooling;<br>2'd1: Max pooling;<br>2'd2: Min pooling;<br>2'd3: Reserved. |

**RKNN_ppu_pooling_kernel_cfg**

Address: Operational Base + offset (0x6034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RO | 0x00 | reserved |
| 23:20 | RW | 0x0 | kernel_stride_height<br>Pooling kernel stride height (need to minus 1). |
| 19:16 | RW | 0x0 | kernel_stride_width<br>Pooling kernel stride width (need to minus 1). |
| 15:12 | RO | 0x0 | reserved |
| 11:8 | RW | 0x0 | kernel_height<br>Pooling kernel height (need to minus 1). |
| 7:4 | RO | 0x0 | reserved |
| 3:0 | RW | 0x0 | kernel_width<br>Pooling kernel width (need to minus 1). |

**RKNN_ppu_recip_kernel_width**

Address: Operational Base + offset (0x6038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16:0 | RW | 0x00000 | recip_kernel_width<br>The Reciprocal of the shape kernel width multiple 2^16. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**RKNN_ppu_recip_kernel_height**

Address: Operational Base + offset (0x603C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16:0 | RW | 0x00000 | recip_kernel_height<br>The Reciprocal of the shape kernel height multiple 2^16. |

**RKNN_ppu_pooling_padding_cfg**

Address: Operational Base + offset (0x6040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:15 | RO | 0x00000 | reserved |
| 14:12 | RW | 0x0 | pad_bottom<br>Pooling bottom pad. |
| 11 | RO | 0x0 | reserved |
| 10:8 | RW | 0x0 | pad_right<br>Pooling right pad. |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x0 | pad_top<br>Pooling top pad. |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x0 | pad_left<br>Pooling left pad. |

**RKNN_ppu_padding_value_1_cfg**

Address: Operational Base + offset (0x6044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | pad_value_0<br>Pad_value*1 [31:0]. |

**RKNN_ppu_padding_value_2_cfg**

Address: Operational Base + offset (0x6048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2:0 | RW | 0x0 | pad_value_1<br>Pad_value*1 [34:32]. |

**RKNN_ppu_dst_base_addr**

Address: Operational Base + offset (0x6070)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | dst_base_addr<br>Base address the output cube goes. |
| 3:0 | RO | 0x0 | reserved |

**RKNN_ppu_dst_surf_stride**

Address: Operational Base + offset (0x607C)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | dst_surf_stride<br>Output shape area. |
| 3:0 | RO | 0x0 | reserved |

**RKNN_ppu_data_format**

Address: Operational Base + offset (0x6084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | index_add<br>If index_en enable, this register is dst_surface_stride x number of cube surface (every 8bytes per surface), else it equals to dst_surface_stride. |
| 3 | RW | 0x0 | dpu_flyin<br>If the data from DPU, and DPU data is from outside, this bit set to be 1. |
| 2:0 | RW | 0x0 | proc_precision<br>Process precision. |

**RKNN_ppu_misc_ctrl**

Address: Operational Base + offset (0x60DC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0000 | surf_len<br>Surface count length. |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | mc_surf_out<br>If enable multiple surfaces out.<br>1'd0: Disable;<br>1'd1: Enable. |
| 7 | RW | 0x0 | nonalign<br>If enable non-align mode.<br>1'd0: Disable;<br>1'd1: Enable. |
| 6:4 | RO | 0x0 | reserved |
| 3:0 | RW | 0x0 | burst_len<br>Burst length<br>4'd3: Burst4;<br>4'd7: Burst8;<br>4'd15: Burst16. |

**RKNN_ppu_rdma_s_status**

Address: Operational Base + offset (0x7000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:18 | RO | 0x0000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17:16 | RO | 0x0 | status_1<br>Executer 1 status.<br>2'd0: Executer 1 is in idle state;<br>2'd1: Executer 1 is operating;<br>2'd2: Executer 1 is operating, executer 1 is waiting to operate;<br>2'd3: Reserved. |
| 15:2 | RO | 0x0000 | reserved |
| 1:0 | RO | 0x0 | status_0<br>Executer 0 status.<br>2'd0: Executer 0 is in idle state;<br>2'd1: Executer 0 is operating;<br>2'd2: Executer 0 is operating, executer 1 is waiting to operate;<br>2'd3: Reserved. |

**RKNN_ppu_rdma_s_pointer**

Address: Operational Base + offset (0x7004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |
| 16 | RO | 0x0 | executer<br>Which register group to be used.<br>1'd0: Executer group 0;<br>1'd1: Executer group 1. |
| 15:6 | RO | 0x000 | reserved |
| 5 | W1C | 0x0 | executer_pp_clear<br>Clear executer group pointer.<br>Set this bit to 1 to clear pointer to 0. |
| 4 | W1C | 0x0 | pointer_pp_clear<br>Clear register group pointer.<br>Set this bit to 1 to clear pointer to 0. |
| 3 | RW | 0x0 | pointer_pp_mode<br>Register group ping-pong mode.<br>1'd0: Pointer ping-pong by executer;<br>eg. if current executer is 0, next pointer will toggle to 1;<br>1'd1: Pointer ping-pong by pointer;<br>eg. if current pointer is 0, next pointer will toggle to 1. |
| 2 | RW | 0x0 | executer_pp_en<br>Executer group ping-pong enable.<br>1'd0: Disable;<br>1'd1: Enable. |
| 1 | RW | 0x0 | pointer_pp_en<br>Register group ping-pong enable.<br>1'd0: Disable;<br>1'd1: Enable. |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | pointer<br>Which register group ready to be set.<br>1'd0: Register group 0;<br>1'd1: Register group 1. |

**RKNN_ppu_rdma_operation_enable**

Address: Operational Base + offset (0x7008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | op_en<br>Set this register will trigger PPU_RDMA block operate.<br>This register and after this are all shadowed for ping-pong operation.<br>1'd0: Disable;<br>1'd1: Enable. |

**RKNN_ppu_rdma_cube_in_width**

Address: Operational Base + offset (0x700C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |
| 12:0 | RW | 0x0000 | cube_in_width<br>Pooling cube width (need to minus 1). |

**RKNN_ppu_rdma_cube_in_height**

Address: Operational Base + offset (0x7010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |
| 12:0 | RW | 0x0000 | cube_in_height<br>Pooling cube height (need to minus 1). |

**RKNN_ppu_rdma_cube_in_channel**

Address: Operational Base + offset (0x7014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |
| 12:0 | RW | 0x0000 | cube_in_channel<br>Pooling cube channel (need to minus 1). |

**RKNN_ppu_rdma_src_base_addr**

Address: Operational Base + offset (0x701C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | src_base_addr<br>Base address of the pooling cube. |

**RKNN_ppu_rdma_src_line_stride**

Address: Operational Base + offset (0x7024)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | src_line_stride<br>Pooling cube shape width. |
| 3:0 | RO | 0x0 | reserved |

**RKNN_ppu_rdma_src_surf_stride**

Address: Operational Base + offset (0x7028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | src_surf_stride<br>Pooling cube shape area. |
| 3:0 | RO | 0x0 | reserved |

**RKNN_ppu_rdma_data_format**

Address: Operational Base + offset (0x7030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1:0 | RW | 0x0 | in_precision<br>Input precision.<br>2'd0: 4bit;<br>2'd1: 8bit;<br>2'd2: 16bit;<br>2'd3: 32bit. |

**RKNN_ddma_cfg_outstanding**

Address: Operational Base + offset (0x8000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:8 | RW | 0x00 | wr_os_cnt<br>Max numbers of write outstanding. |
| 7:0 | RW | 0x00 | rd_os_cnt<br>Max numbers of read outstanding. |

**RKNN_ddma_rd_weight_0**

Address: Operational Base + offset (0x8004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | rd_weight_pdp<br>Weight of PPU read burst. |
| 23:16 | RW | 0x00 | rd_weight_dpu<br>Weight of DPU read burst. |
| 15:8 | RW | 0x00 | rd_weight_kernel<br>Weight of read weight burst. |
| 7:0 | RW | 0x00 | rd_weight_feature<br>Weight of read feature burst. |

**RKNN_ddma_wr_weight_0**

Address: Operational Base + offset (0x8008)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:8 | RW | 0x00 | wr_weight_pdp<br>Write_weight_ppu. |
| 7:0 | RW | 0x00 | wr_weight_dpu<br>Write_weight_dpu. |

**RKNN_ddma_cfg_id_error**

Address: Operational Base + offset (0x800C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9:6 | RW | 0x0 | wr_resp_id<br>Error write id. |
| 5 | RO | 0x0 | reserved |
| 4:0 | RW | 0x00 | rd_resp_id<br>Error read id. |

**RKNN_ddma_rd_weight_1**

Address: Operational Base + offset (0x8010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | rd_weight_pc<br>Weight of PC read burst. |

**RKNN_ddma_cfg_dma_fifo_clr**

Address: Operational Base + offset (0x8014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | dma_fifo_clr<br>Clear DMA FIFO. |

**RKNN_ddma_cfg_dma_arb**

Address: Operational Base + offset (0x8018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9 | RW | 0x0 | wr_arbit_model<br>Write_arbit_model. |
| 8 | RW | 0x0 | rd_arbit_model<br>Read_arbit_model. |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x0 | wr_fix_arb<br>Write_fix_arb. |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x0 | rd_fix_arb<br>Read_fix_arb. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**RKNN_ddma_cfg_dma_rd_qos**

Address: Operational Base + offset (0x8020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9:8 | RW | 0x0 | rd_pc_qos<br>Read_pc_qos. |
| 7:6 | RW | 0x0 | rd_ppu_qos<br>Read_ppu_qos. |
| 5:4 | RW | 0x0 | rd_dpu_qos<br>Read_dpu_qos. |
| 3:2 | RW | 0x0 | rd_kernel_qos<br>Read_kernel_qos. |
| 1:0 | RW | 0x0 | rd_feature_qos<br>Read feature_qos. |

**RKNN_ddma_cfg_dma_rd_cfg**

Address: Operational Base + offset (0x8024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |
| 12 | RW | 0x0 | rd_arlock<br>Read_arlock. |
| 11:8 | RW | 0x0 | rd_arcache<br>Read_arcache. |
| 7:5 | RW | 0x0 | rd_arprot<br>Read_arprot. |
| 4:3 | RW | 0x0 | rd_arburst<br>Read_arburst. |
| 2:0 | RW | 0x0 | rd_arsize<br>Read_arsize. |

**RKNN_ddma_cfg_dma_wr_cfg**

Address: Operational Base + offset (0x8028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |
| 12 | RW | 0x0 | wr_awlock<br>Write_awlock. |
| 11:8 | RW | 0x0 | wr_awcache<br>Write awcache. |
| 7:5 | RW | 0x0 | wr_awprot<br>Write_awprot. |
| 4:3 | RW | 0x0 | wr_awburst<br>Write_awburst. |
| 2:0 | RW | 0x0 | wr_awsize<br>Write_awsize. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**RKNN_ddma_cfg_dma_wstrb**

Address: Operational Base + offset (0x802C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | wr_wstrb<br>Write_wstrb. |

**RKNN_ddma_cfg_status**

Address: Operational Base + offset (0x8030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:9 | RO | 0x000000 | reserved |
| 8 | RW | 0x0 | idel<br>Idel. |
| 7:0 | RO | 0x00 | reserved |

**RKNN_sdma_cfg_outstanding**

Address: Operational Base + offset (0x9000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:8 | RW | 0x00 | wr_os_cnt<br>Max numbers of write outstanding. |
| 7:0 | RW | 0x00 | rd_os_cnt<br>Max numbers of read outstanding. |

**RKNN_sdma_rd_weight_0**

Address: Operational Base + offset (0x9004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | rd_weight_pdp<br>Weight of PPU read burst. |
| 23:16 | RW | 0x00 | rd_weight_dpu<br>Weight of DPU read burst. |
| 15:8 | RW | 0x00 | rd_weight_kernel<br>Weight of read weight burst. |
| 7:0 | RW | 0x00 | rd_weight_feature<br>Weight of read feature burst. |

**RKNN_sdma_wr_weight_0**

Address: Operational Base + offset (0x9008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:8 | RW | 0x00 | wr_weight_pdp<br>Write_weight_ppu. |
| 7:0 | RW | 0x00 | wr_weight_dpu<br>Write_weight_dpu. |

**RKNN_sdma_cfg_id_error**

Address: Operational Base + offset (0x900C)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9:6 | RW | 0x0 | wr_resp_id<br>Error write id. |
| 5 | RO | 0x0 | reserved |
| 4:0 | RW | 0x00 | rd_resp_id<br>Error read id. |

**RKNN_sdma_rd_weight_1**

Address: Operational Base + offset (0x9010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:8 | RO | 0x000000 | reserved |
| 7:0 | RW | 0x00 | rd_weight_pc<br>Weight of PC read burst. |

**RKNN_sdma_cfg_dma_fifo_clr**

Address: Operational Base + offset (0x9014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | dma_fifo_clr<br>Clear DMA FIFO. |

**RKNN_sdma_cfg_dma_arb**

Address: Operational Base + offset (0x9018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9 | RW | 0x0 | wr_arbit_model<br>Write_arbit_model. |
| 8 | RW | 0x0 | rd_arbit_model<br>Read_arbit_model. |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x0 | wr_fix_arb<br>Write_fix_arb. |
| 3 | RO | 0x0 | reserved |
| 2:0 | RW | 0x0 | rd_fix_arb<br>Read_fix_arb. |

**RKNN_sdma_cfg_dma_rd_qos**

Address: Operational Base + offset (0x9020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:10 | RO | 0x000000 | reserved |
| 9:8 | RW | 0x0 | rd_pc_qos<br>Read_pc_qos. |
| 7:6 | RW | 0x0 | rd_ppu_qos<br>Read_ppu_qos. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5:4 | RW | 0x0 | rd_dpu_qos<br>Read_dpu_qos. |
| 3:2 | RW | 0x0 | rd_kernel_qos<br>Read_kernel_qos. |
| 1:0 | RW | 0x0 | rd_feature_qos<br>Read feature_qos. |

**RKNN_sdma_cfg_dma_rd_cfg**

Address: Operational Base + offset (0x9024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |
| 12 | RW | 0x0 | rd_arlock<br>Read_arlock. |
| 11:8 | RW | 0x0 | rd_arcache<br>Read_arcache. |
| 7:5 | RW | 0x0 | rd_arprot<br>Read_arprot. |
| 4:3 | RW | 0x0 | rd_arburst<br>Read_arburst. |
| 2:0 | RW | 0x0 | rd_arsize<br>Read_arsize. |

**RKNN_sdma_cfg_dma_wr_cfg**

Address: Operational Base + offset (0x9028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |
| 12 | RW | 0x0 | wr_awlock<br>Write_awlock. |
| 11:8 | RW | 0x0 | wr_awcache<br>Write awcache. |
| 7:5 | RW | 0x0 | wr_awprot<br>Write_awprot. |
| 4:3 | RW | 0x0 | wr_awburst<br>Write_awburst. |
| 2:0 | RW | 0x0 | wr_awsize<br>Write_awsize. |

**RKNN_sdma_cfg_dma_wstrb**

Address: Operational Base + offset (0x902C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | wr_wstrb<br>Write_wstrb. |

**RKNN_sdma_cfg_status**

Address: Operational Base + offset (0x9030)

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:9 | RO | 0x000000 | reserved |
| 8 | RW | 0x0 | idel<br>Idel. |
| 7:0 | RO | 0x00 | reserved |

**RKNN_global_operation_enable**

Address: Operational Base + offset (0xF008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:7 | RO | 0x0000000 | reserved |
| 6 | RW | 0x0 | ppu_rdma_op_en<br>PPU_RDMA operation enable signal. |
| 5 | RW | 0x0 | ppu_op_en<br>PPU operation enable signal. |
| 4 | RW | 0x0 | dpu_rdma_op_en<br>DPU_RDMA operation enable signal. |
| 3 | RW | 0x0 | dpu_op_en<br>DPU operation enable signal. |
| 2 | RW | 0x0 | core_op_en<br>CORE operation enable signal. |
| 1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | cna_op_en<br>CNA operation enable signal. |

# 36.5 Application Notes

## 36.5.1 Ping-pong registers

In order to reduce the time of fetch registers, every Calculate Core and Control Core of RKNN has its owner ping-pong registers. Configure the group 0 when use the group 1, and configure the group 1 when use group 0. As a result of hiding the time of fetch registers. Writing S_POINTER of every block can enable this function.

## 36.5.2 Clock and Reset

### 1.5.2.1 Clock Domains

RKNN has two clock domains, one is AHB clock, the other is AXI clock. AHB clock, which is the clock for AHB interface, while AXI clock, which is the clock for AXI interface. AXI clock also used for core clock for every Calculate Core and Control Core. Clock frequency can be controlled by CRU, please refer to the relevant sections. Automatic localized clock gating is employed throughout the design in order to minimize the dynamic power consumption. Almost all of the flip-flops are clock gated in the design. Block level clock gating also implemented in every separate block. If a block and the interface to the block are both idle, then the clock of that block will be gated automatically. This feature can be disabled by software.

### 1.5.2.2 NPU Reset

Correspond to the clock domain, there are two reset signals. Aresetn, the reset signal for AXI interface and every Calculate Core and Control Core. Hresetn is the AHB interface reset pin and which is synchronized to the AHB clock domain.

All the two signals must be asserted for a minimum of 32 core clock cycles, using the slowest of the two clocks. Then two signals must be release at the same time.

## 36.5.3 NPU Interrupt Application

Copyright 2022 © Rockchip Electronics Co., Ltd.

RKNN has 3 interrupt output signal and it remains asserted until the host processor clears the interrupt. Each bit of PC_INTERRUPT_STATUS represents one of the 17 possible events that the RKNN can signal to the host processor. By setting the bits of the interrupt enable register (PC_INTERRUPT_MASK) the programmer can control which of those events will generate an interrupt.

### 36.5.4 NPU operate flow

RKNN has two types of work mode: slave configured mode and pc work mode. Pc work mode need to initial register information to the system memory, then obey flowing flows as Figure 1-3 shows.

The information of registers initial to the system memory need to generate by the op you want to specify. And we describe the normal work flows by describe the slave configured mode.

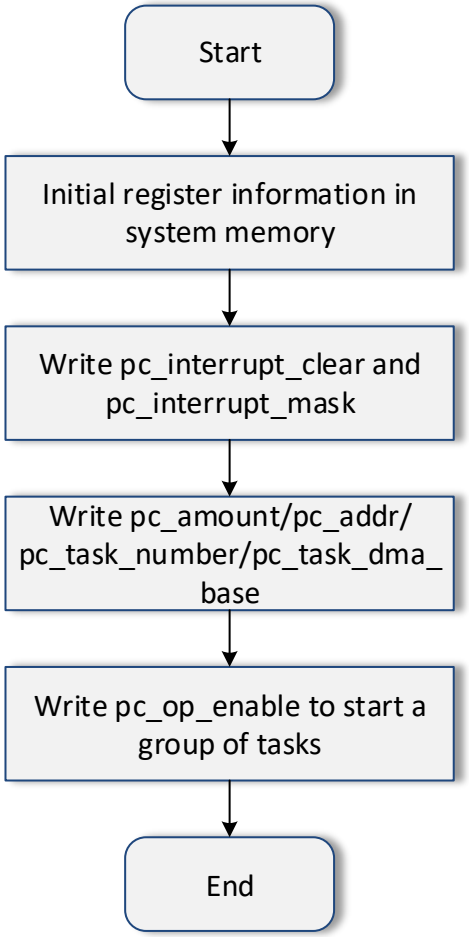



Fig. 36-3 PC flow

Convolution flow

RKNN supports variety of convolution and matrix multiplication. If use the MAC array to calculate, the work flow should obey the Figure 1-4, and if use DPU CORE calculate, work flow should obey the Figure 1-5.

Copyright 2022 © Rockchip Electronics Co., Ltd.

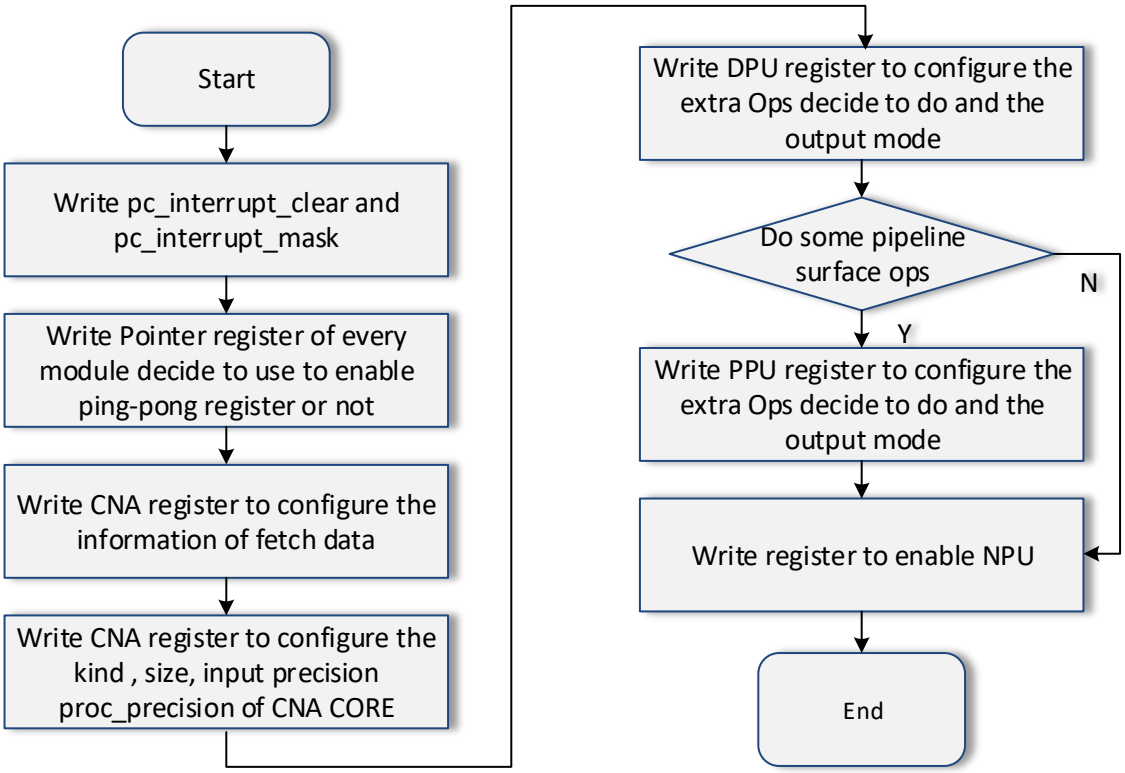



Fig. 36-4 Convolution flow 1

In step 1, do not set PPU mask bit if don't use PPU.

In step 3, you need to configure the size of feature map, and the input precision, process precision, grains, entries and weight size, including weight height, weight width, kernels and weight bytes etc.

In step 4, you need to configure process precision, conv_mode and auto gating registers of CMAC and CNA sequence controller.

In step 5, you can specify some operators to the outputs of convolution according to configure the DPU_CORE. DPU CORE has some fixed operators, also you can specify some programmed operators.

In step 6, you can do some extra operators to the outputs of DPU, pooling for example.

Copyright 2022 © Rockchip Electronics Co., Ltd.

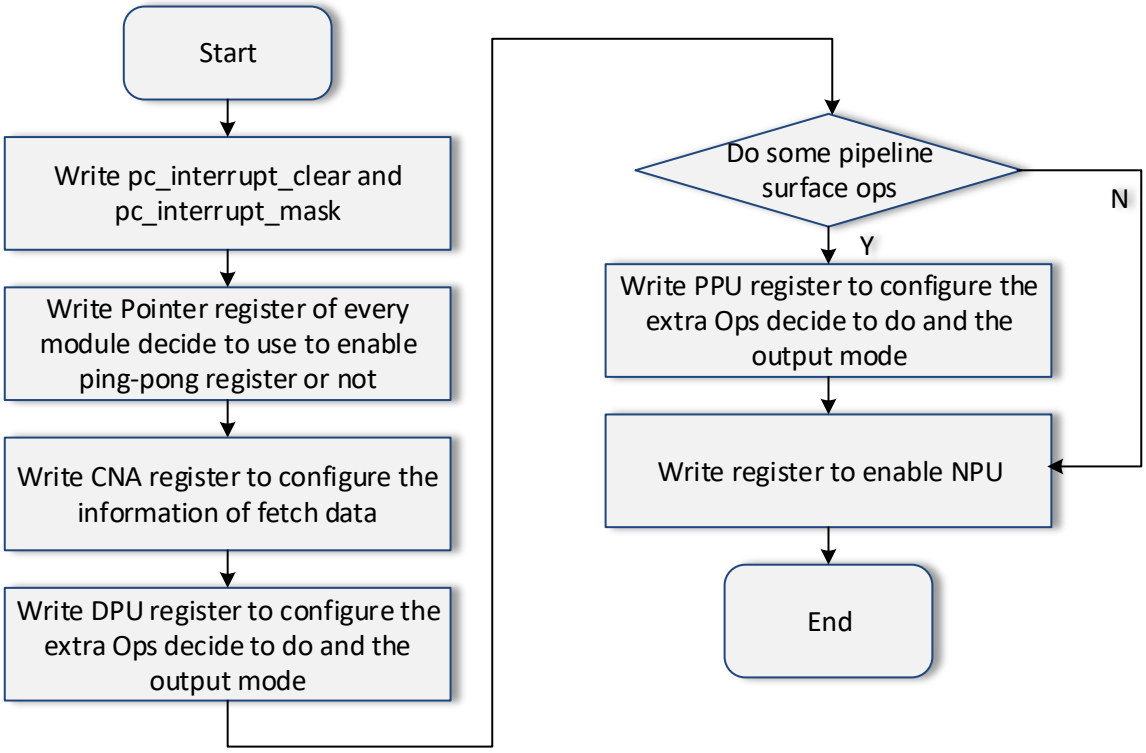



Fig. 36-5 Convolution flow 2

In step 3, you need to configure the size of feature map, and the input precision, process precision, grains, entries and weight size, including height, width, kernels and weight bytes etc. Here we supply zero skipping switch, if there's a lot of zero or some number else in the feature map, you can enable zero skipping by writing cna_fc_con0, cna_fc_con1 and cna_fc_con2, as a result of without reading the weights correspond to the pixel in the feature map. In zero skipping mode, you can specify the feature map size for read different from the feature map size for calculate.

If enable zero skipping, the conv_mode of DPU must configure to be 3, and must bypass the BS_CORE. The alu_src must set to be 0, the mul_src must set to be 1, and the alu_algo must set be 3. We bypass BS_CORE, and use BN_CORE to calculate convolution, so the extra operators have to achieve by EW_CORE. But we use NRDMA to read operands to EW_CORE when ew_src is 1.

Pooling flow

You can use PPU in two ways, pipeline with DPU, and flying mode independently.The first one is described above, we describe the second flow below.

Copyright 2022 © Rockchip Electronics Co., Ltd.

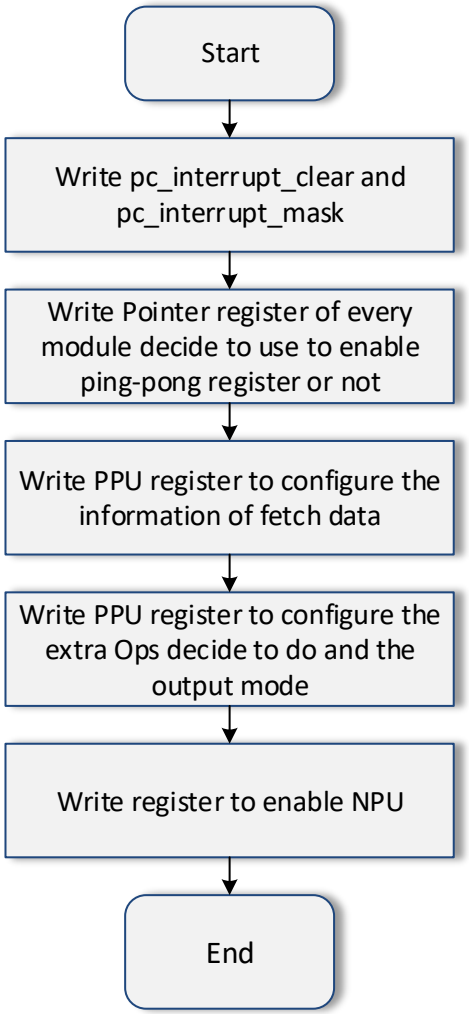



Fig. 36-6 Pooling flow

In step 4, we supply two type of output mode, 8byte align per pixel and non-align mode. In some case with uncomfortable feature map size, you can enable non-align mode by writing ppu_misc_ctrl_nonalign and ppu_misc_ctrl_surf_len.

Separate op flow

As for the operators that RKNN do not fixed, you can combine DPU and PPU to achieve it. Following we describe the DPU flying mode flow.

Copyright 2022 © Rockchip Electronics Co., Ltd.

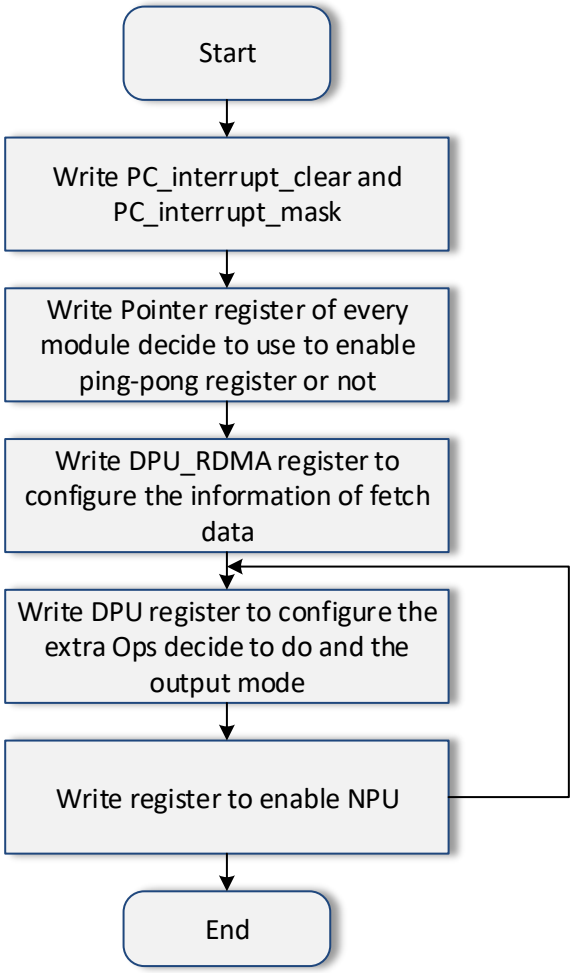



Fig. 36-7 DPU flying mode flow

In step 3, you can enable MRDMA, BRDMA, NRDMA, ERDMA to fetch data. RKNN supports 6 types of data input precision.

In step 4, you can configure BS_ALU_BYPASS, BS_MUL_BYPASS, BS_RELU_BYPASS, BS_MUL_PRELU, BS_MUL_SHIFT, BS_RELUX_EN etc. to specify the operators you want to achieve.

Copyright 2022 © Rockchip Electronics Co., Ltd.

# Chapter 37 Video Capture (VICAP)

## 37.1 Overview

The Video Capture, receives the data from Camera via DVP/MIPI, and transfers the data into system main memory by AXI bus.

- Support BT601 YCbCr 422 8bit input, RAW 8/10/12bit input
- Support BT656 YCbCr 422 8bit progressive/interlace input
- Support BT1120 YCbCr 422 16bit progressive/interlace input, single/dual-edge sampling
- Support 2/4 channels mixed BT656/BT1120 YCbCr 422 8/16bit progressive/interlace input
- Support YUYV sequence configurable
- Support the polarity of hsync and vsync configurable
- Support receiving six interfaces of MIPI CSI/DSI, up to four IDs for each interface
- Support five CSI data formats: RAW8/10/12/14, YUV422
- Support three modes of HDR: virtual channel mode, identification code mode, line counter mode
- Support window cropping
- Support RAW data through to ISP0/1
- Support four channels of 8/16/32 times down-sampling for RAW data
- Support virtual stride when write to DDR
- Support NV16/NV12/YUV400/YUYV output format for YUV data
- Support compact/non-compact output format for RAW data
- Support MMU
- Support soft reset, auto-reset when DMA error

## 37.2 Block Diagram

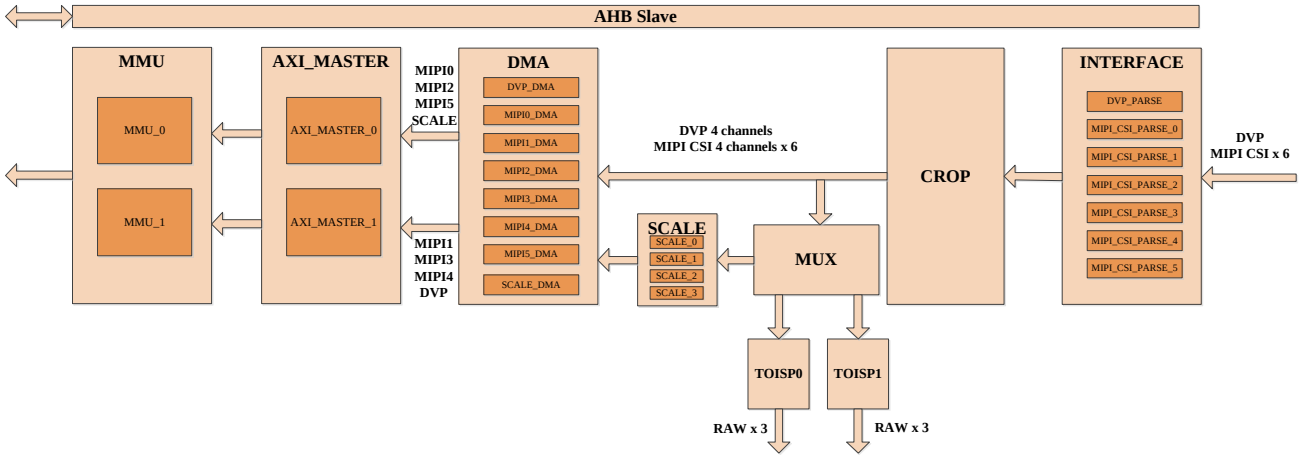



Fig. 37-1 VICAP Block Diagram

VICAP comprises with:

- AHB Slave
- AXI Master
- MMU
- INTERFACE
- CROP
- SCALE
- TOISP0/1
- DMA

## 37.3 Function Description

### 37.3.1 Interface

Translate the input video data(DVP/MIPI CSI) into the requisite data format

- DVP BT656/BT1120 format

Copyright 2022 © Rockchip Electronics Co., Ltd.

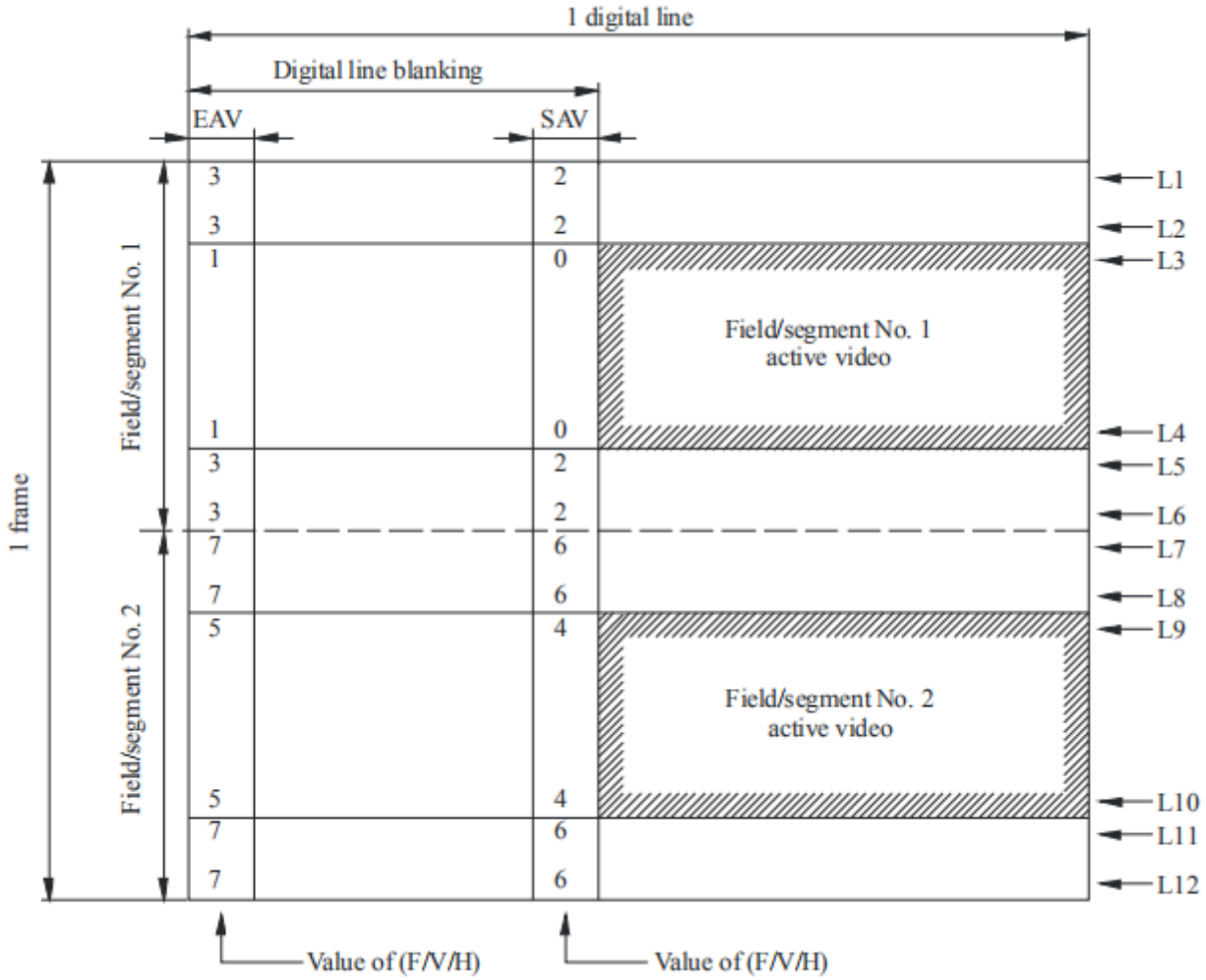



Fig. 37-2 BT656/BT1120 interlace timing relationship

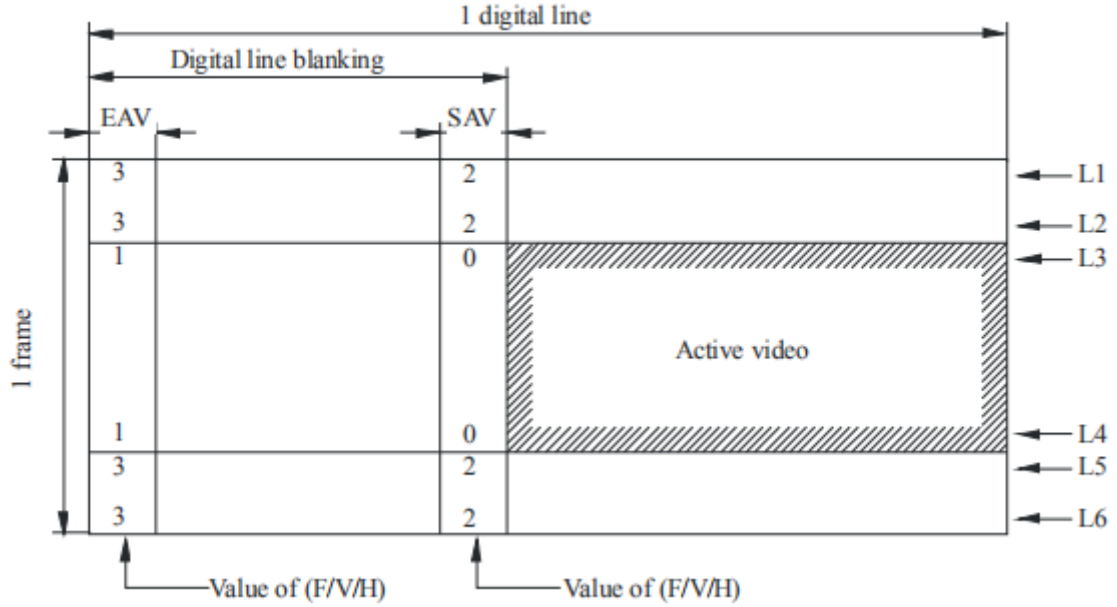



Fig. 37-3 BT656/BT1120 progressive timing relationship

- DVP 2/4 channels mixed BT656/BT1120 format

Copyright 2022 © Rockchip Electronics Co., Ltd.

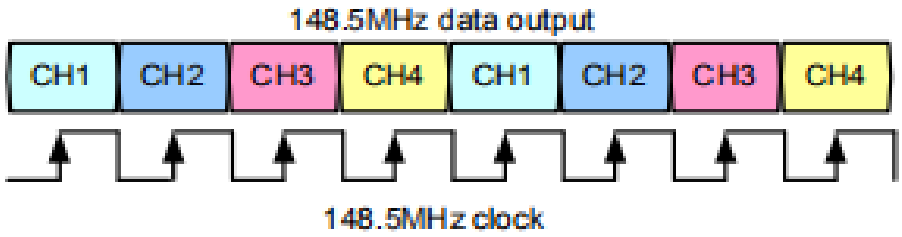



Fig. 37-4 4 channels mixed BT656/BT1120

- DVP BT601 format

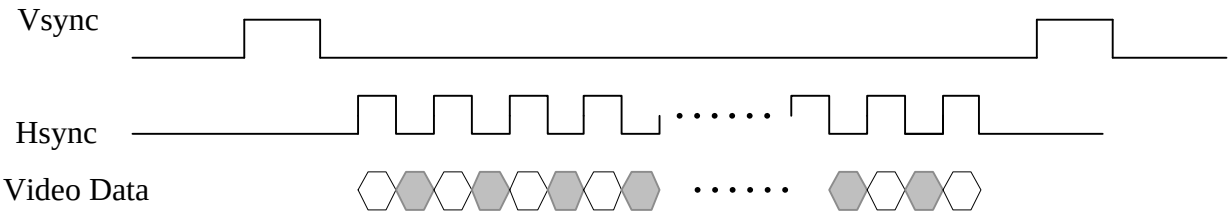



Fig. 37-5 BT656/BT1120 timing relationship

- MIPI CSI RAW8 format

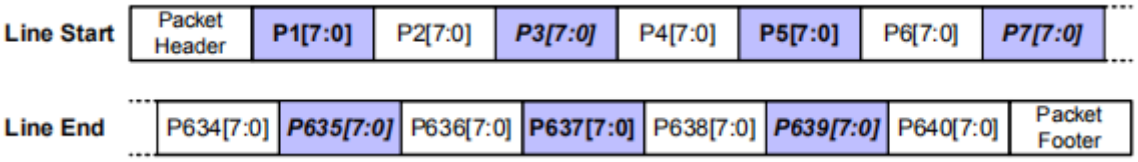



Fig. 37-6 MIPI CSI RAW8 format

- MIPI CSI RAW10 format

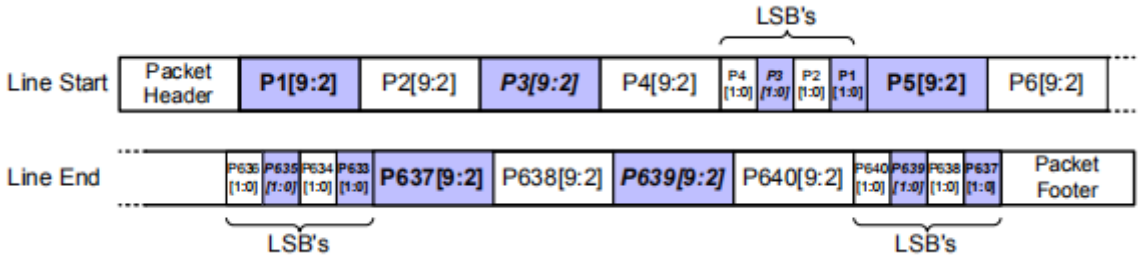



Fig. 37-7 MIPI CSI RAW10 format

- MIPI CSI RAW12 format

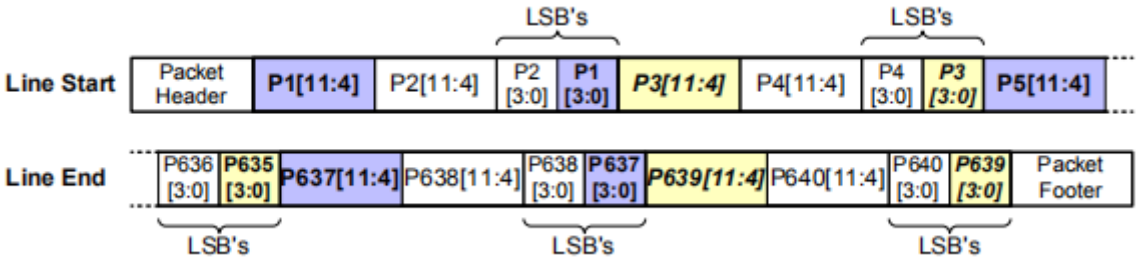



Fig. 37-8 MIPI CSI RAW12 format

- MIPI CSI RAW14 format

Copyright 2022 © Rockchip Electronics Co., Ltd.

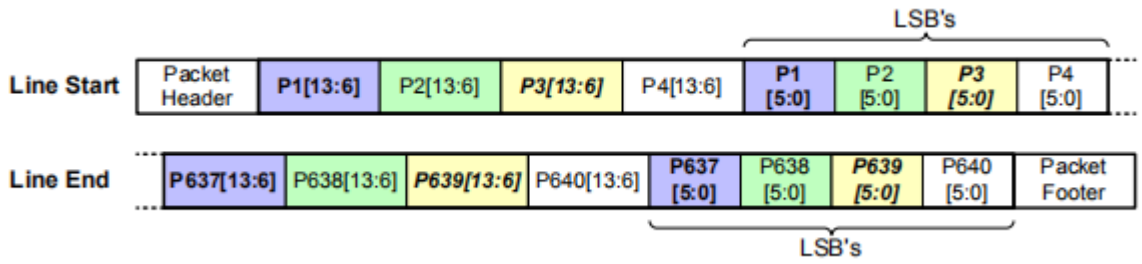



Fig. 37-9 MIPI CSI RAW14 format

- MIPI CSI YUV422 format

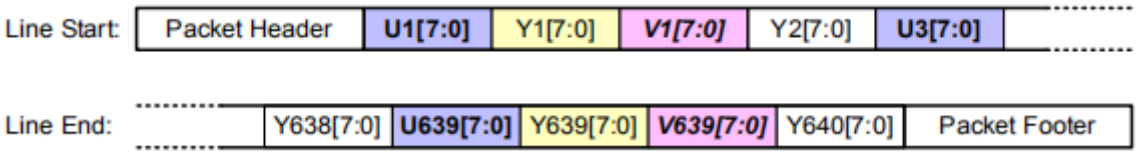



Fig. 37-10 MIPI CSI YUV422 format

## 37.3.2 Crop

Bypass or crop the source video data to a smaller size destination.

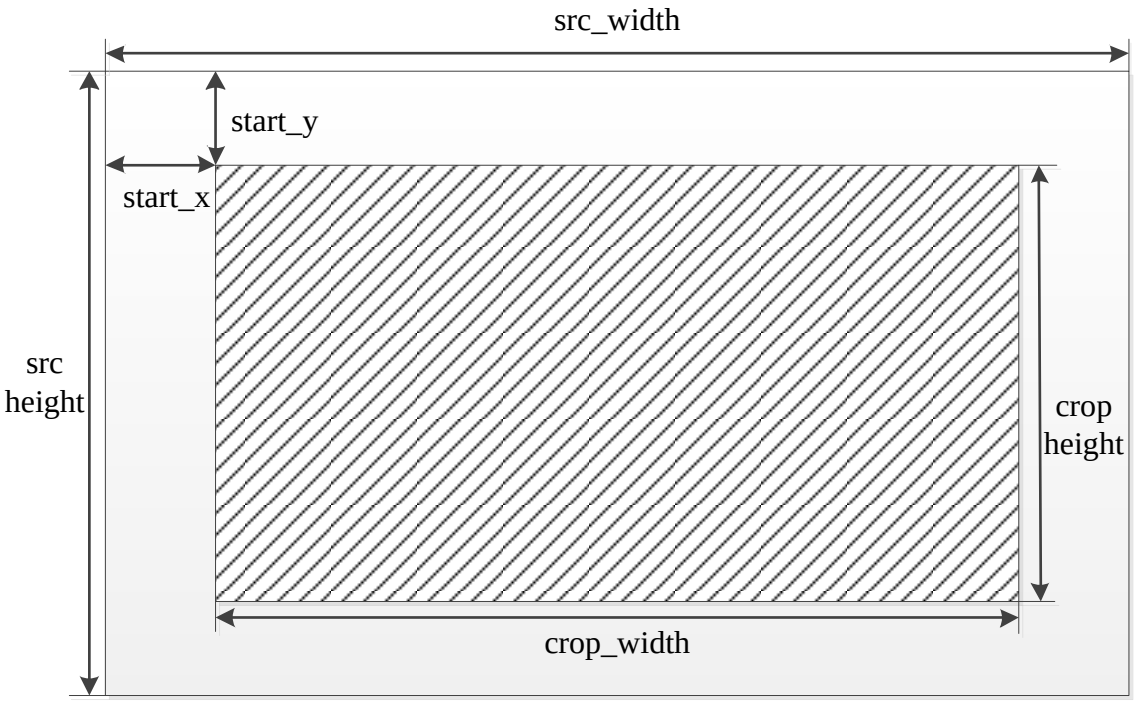



Fig. 37-11 Crop

## 37.3.3 Scale

Scale down for RAW data.

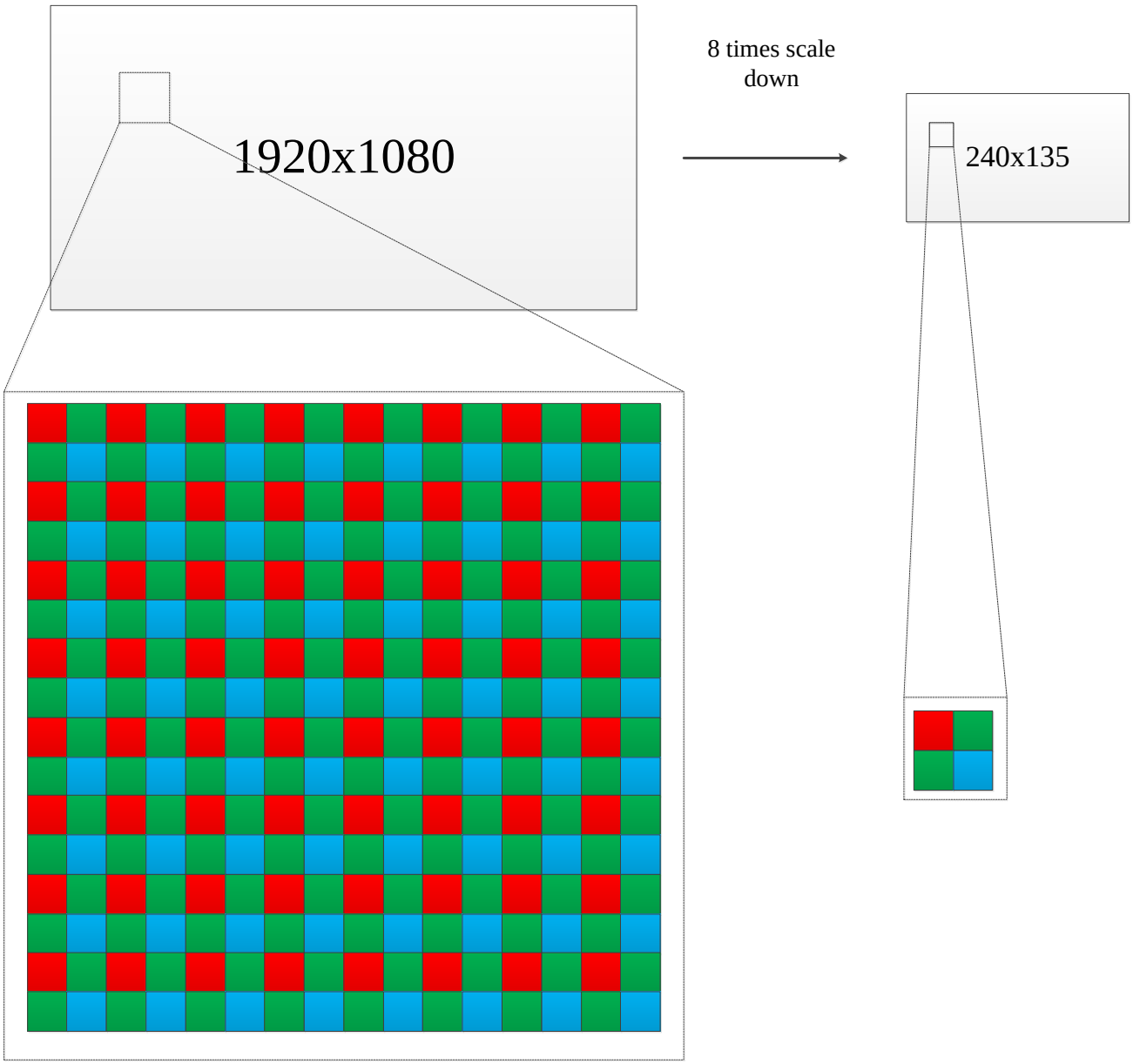



Fig. 37-12 8 times Scale down

### 37.3.4 Toisp

The parsed video data can go straight to ISP0/1 for real-time processing.

### 37.3.5 DMA

The DMA is used to transfer the data from crop module to the AXI master block which will send the data to the AXI bus.

- NV16

Copyright 2022 © Rockchip Electronics Co., Ltd.

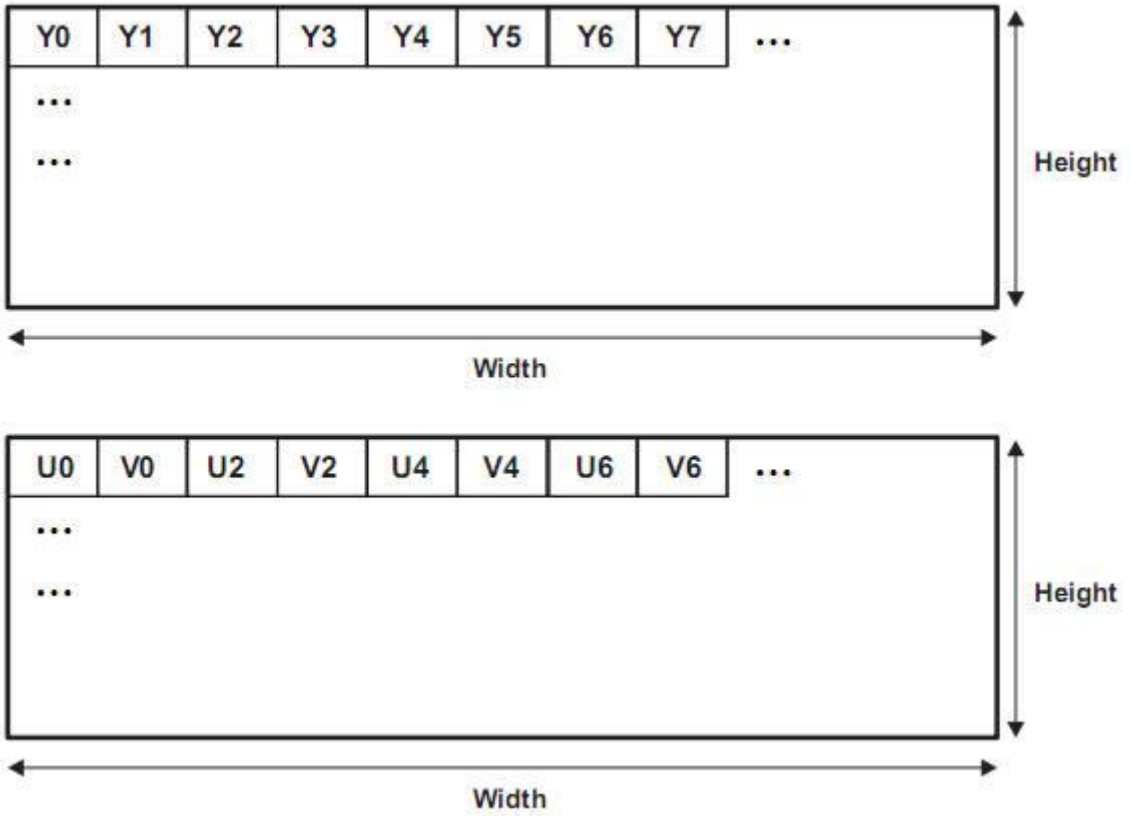



Fig. 37-13 NV16

- NV12

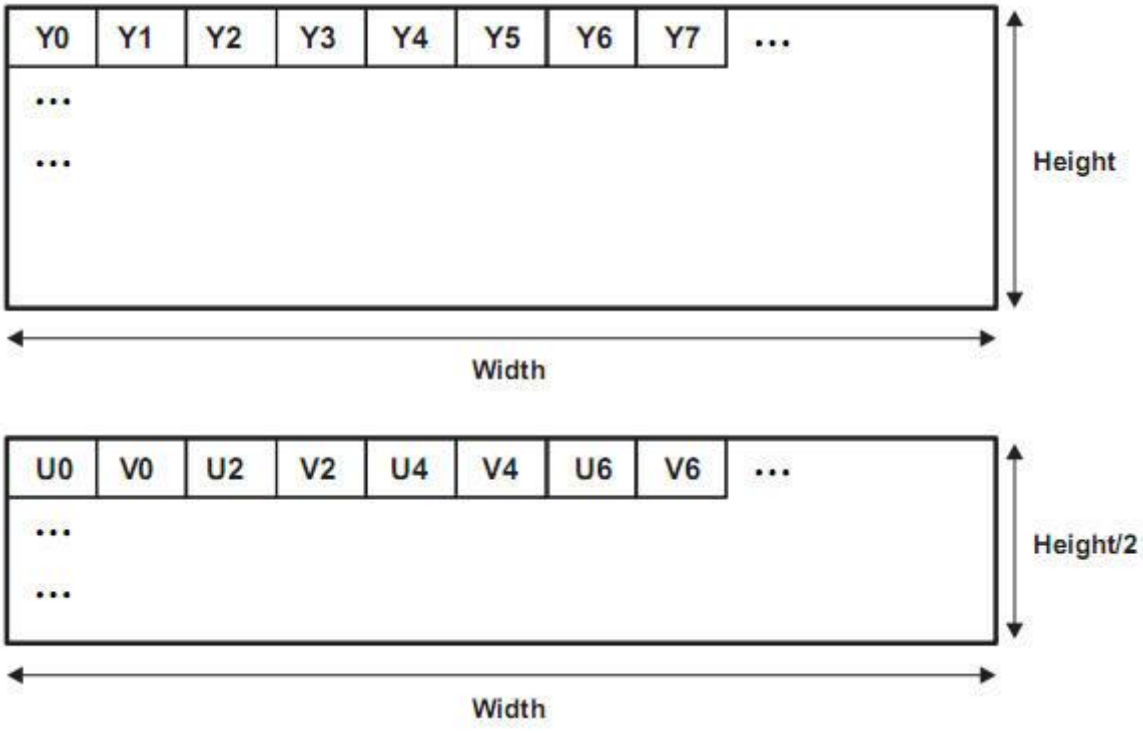



Fig. 37-14 NV12

- YUV400

Copyright 2022 © Rockchip Electronics Co., Ltd. 

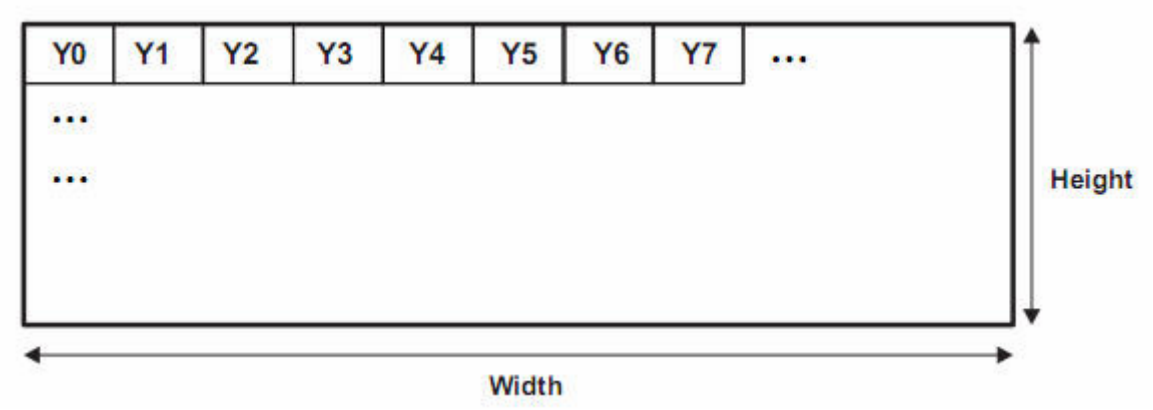



Fig. 37-15 YUV400

- YUYV

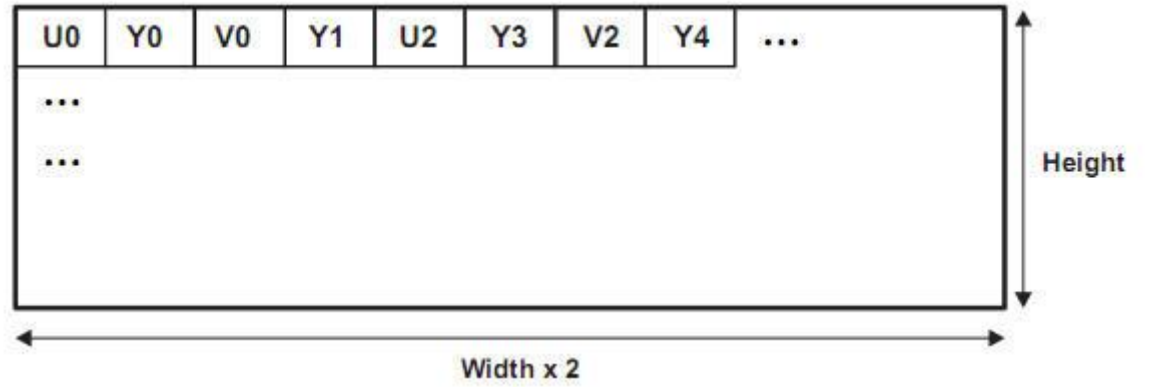



Fig. 37-16 YUYV

- Compact RAW

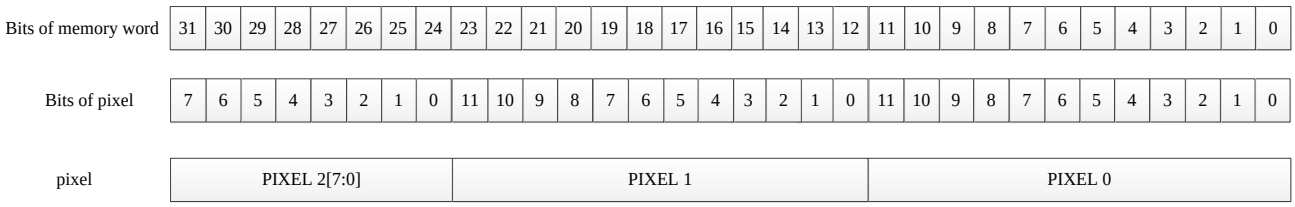



Fig. 37-17 Compact RAW12

- Noncompact RAW

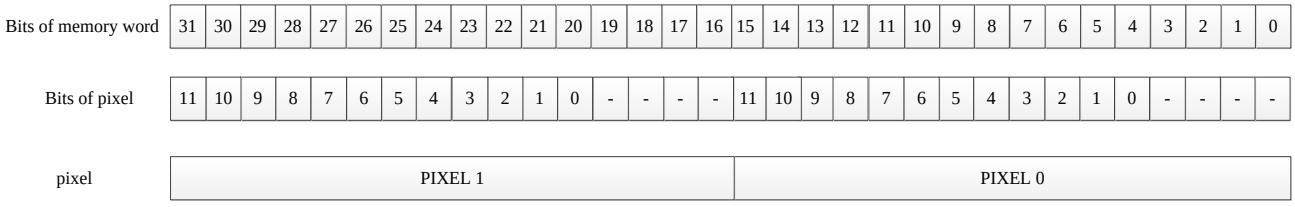



Fig. 37-18 noncompact RAW12(high align)

### 37.3.6 AXI Master

Transmit the data to chip memory via the AXI Master.

### 37.3.7 MMU

Map the virtual address to physical address.

### 37.3.8 AHB Slave

Host configure the registers via the AHB Slave.

Copyright 2022 © Rockchip Electronics Co., Ltd.

# 37.4 VICAP Register Description

## 37.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 37-1 VICAP Address Mapping

| Base Address[11:8] | Device | Address Length | Offset Address Range |
|---|---|---|---|
| 4'b0000 | Global/DVP | 256 BYTE | 0x0000 ~ 0x00ff |
| 4'b0001 | MIPI0 | 256 BYTE | 0x0100 ~ 0x01ff |
| 4'b0010 | MIPI1 | 256 BYTE | 0x0200 ~ 0x02ff |
| 4'b0011 | MIPI2 | 256 BYTE | 0x0300 ~ 0x03ff |
| 4'b0100 | MIPI3 | 256 BYTE | 0x0400 ~ 0x04ff |
| 4'b0101 | MIPI4 | 256 BYTE | 0x0500 ~ 0x05ff |
| 4'b0110 | MIPI5 | 256 BYTE | 0x0600 ~ 0x06ff |
| 4'b0111 | Scale/TOISP | 256 BYTE | 0x0700 ~ 0x07ff |
| 4'b1000 | MMU0 | 256 BYTE | 0x0800 ~ 0x08ff |
| 4'b1001 | MMU1 | 256 BYTE | 0x0900 ~ 0x09ff |

## 37.4.2 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VICAP_GLB_CTRL | 0x0000 | W | 0x00010001 | VICAP global control |
| VICAP_GLB_INTEN | 0x0004 | W | 0x00000000 | VICAP global interrupt enable. |
| VICAP_GLB_INTST | 0x0008 | W | 0x00000000 | VICAP global interrupt status. |
| VICAP_DVP_CTRL | 0x0010 | W | 0x00000000 | DVP path control |
| VICAP_DVP_INTEN | 0x0014 | W | 0x00000000 | DVP path interrupt status |
| VICAP_DVP_INTSTAT | 0x0018 | W | 0x00000000 | DVP path interrupt status |
| VICAP_DVP_FORMAT | 0x001C | W | 0x00000000 | DVP path format |
| VICAP_DVP_MULTI_ID | 0x0020 | W | 0x00000000 | Channel ID for multi-ID mode |
| VICAP_DVP_SAV_EAV | 0x0024 | W | 0xFEDCBA98 | SAV/EAV for ACT/BLK |
| VICAP_DVP_CROP_SIZE | 0x0028 | W | 0x01E002D0 | The expected width and height of received image |
| VICAP_DVP_CROP_START | 0x002C | W | 0x00000000 | The start point of DVP path cropping |
| VICAP_DVP_FRM0_ADDR_Y_ID0 | 0x0030 | W | 0x00000000 | DVP path frame0 y address |
| VICAP_DVP_FRM0_ADDR_UV_ID0 | 0x0034 | W | 0x00000000 | DVP path frame0 uv address |
| VICAP_DVP_FRM1_ADDR_Y_ID0 | 0x0038 | W | 0x00000000 | DVP path frame1 y address |
| VICAP_DVP_FRM1_ADDR_UV_ID0 | 0x003C | W | 0x00000000 | DVP path frame1 uv address |
| VICAP_DVP_FRM0_ADDR_Y_ID1 | 0x0040 | W | 0x00000000 | DVP path frame0 y address for ID1 |
| VICAP_DVP_FRM0_ADDR_UV_ID1 | 0x0044 | W | 0x00000000 | DVP path frame0 uv address for id1 |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VICAP_DVP_FRM1_ADDR_Y_ID1 | 0x0048 | W | 0x00000000 | DVP path frame1 y address for id1 |
| VICAP_DVP_FRM1_ADDR_UV_ID1 | 0x004C | W | 0x00000000 | DVP path frame1 uv address for id1 |
| VICAP_DVP_FRM0_ADDR_Y_ID2 | 0x0050 | W | 0x00000000 | DVP path frame0 y address for id2 |
| VICAP_DVP_FRM0_ADDR_UV_ID2 | 0x0054 | W | 0x00000000 | DVP path frame0 uv address for id2 |
| VICAP_DVP_FRM1_ADDR_Y_ID2 | 0x0058 | W | 0x00000000 | DVP path frame1 y address for id2 |
| VICAP_DVP_FRM1_ADDR_UV_ID2 | 0x005C | W | 0x00000000 | DVP path frame1 uv address for id2 |
| VICAP_DVP_FRM0_ADDR_Y_ID3 | 0x0060 | W | 0x00000000 | DVP path frame0 y address for id3 |
| VICAP_DVP_FRM0_ADDR_UV_ID3 | 0x0064 | W | 0x00000000 | DVP path frame0 uv address for id3 |
| VICAP_DVP_FRM1_ADDR_Y_ID3 | 0x0068 | W | 0x00000000 | DVP path frame1 y address for id3 |
| VICAP_DVP_FRM1_ADDR_UV_ID3 | 0x006C | W | 0x00000000 | DVP path frame1 uv address for id3 |
| VICAP_DVP_VIR_LINE_WIDTH | 0x0070 | W | 0x00000000 | DVP path virtual line width |
| VICAP_DVP_LINE_INT_NUM_ID0_1 | 0x0074 | W | 0x00400040 | DVP path id0/id1 line interrupt number |
| VICAP_DVP_LINE_INT_NUM_ID2_3 | 0x0078 | W | 0x00400040 | DVP path id2/id3 line interrupt number |
| VICAP_DVP_LINE_CNT_ID0_1 | 0x007C | W | 0x00000000 | DVP path id0/id1 line count |
| VICAP_DVP_LINE_CNT_ID2_3 | 0x0080 | W | 0x00000000 | DVP path id2/id3 line count |
| VICAP_DVP_PIX_NUM_ID0 | 0x0084 | W | 0x00000000 | DVP path ID0 PIXEL NUMBER |
| VICAP_DVP_LINE_NUM_ID0 | 0x0088 | W | 0x00000000 | DVP path ID0 LINE NUMBER |
| VICAP_DVP_PIX_NUM_ID1 | 0x008C | W | 0x00000000 | DVP path ID1 PIXEL NUMBER |
| VICAP_DVP_LINE_NUM_ID1 | 0x0090 | W | 0x00000000 | DVP path ID1 LINE NUMBER |
| VICAP_DVP_PIX_NUM_ID2 | 0x0094 | W | 0x00000000 | DVP path ID2 PIXEL NUMBER |
| VICAP_DVP_LINE_NUM_ID2 | 0x0098 | W | 0x00000000 | DVP path ID2 LINE NUMBER |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VICAP_DVP_PIX_NUM_ID3 | 0x009C | W | 0x00000000 | DVP path ID3 PIXEL NUMBER |
| VICAP_DVP_LINE_NUM_ID3 | 0x00A0 | W | 0x00000000 | DVP path ID3 LINE NUMBER |
| VICAP_DVP_SYNC_HEADER | 0x00A4 | W | 0x00000000 | DVP SYNC HEADER FOR BT656/BT1120 |
| VICAP_MIPI0_ID0_CTRL0 | 0x0100 | W | 0x00000000 | MIPI0 path id0 control0 |
| VICAP_MIPI0_ID0_CTRL1 | 0x0104 | W | 0x00000000 | MIPI0 path id0 control1 |
| VICAP_MIPI0_ID1_CTRL0 | 0x0108 | W | 0x00000000 | MIPI0 path id1 control0 |
| VICAP_MIPI0_ID1_CTRL1 | 0x010C | W | 0x00000000 | MIPI0 path id1 control1 |
| VICAP_MIPI0_ID2_CTRL0 | 0x0110 | W | 0x00000000 | MIPI0 path id2 control0 |
| VICAP_MIPI0_ID2_CTRL1 | 0x0114 | W | 0x00000000 | MIPI0 path id2 control1 |
| VICAP_MIPI0_ID3_CTRL0 | 0x0118 | W | 0x00000000 | MIPI0 path id3 control0 |
| VICAP_MIPI0_ID3_CTRL1 | 0x011C | W | 0x00000000 | MIPI0 path id3 control1 |
| VICAP_MIPI0_CTRL | 0x0120 | W | 0x00000000 | MIPI0 path control |
| VICAP_MIPI0_FRAME0_ADDR_Y_ID0 | 0x0124 | W | 0x00000000 | First address of even frame for ID0 Y/RAW/RGB path |
| VICAP_MIPI0_FRAME1_ADDR_Y_ID0 | 0x0128 | W | 0x00000000 | First address of odd frame for ID0 Y path |
| VICAP_MIPI0_FRAME0_ADDR_UV_ID0 | 0x012C | W | 0x00000000 | First address of even frame for ID0 UV path |
| VICAP_MIPI0_FRAME1_ADDR_UV_ID0 | 0x0130 | W | 0x00000000 | First address of odd frame for ID0 UV path |
| VICAP_MIPI0_VLW_ID0 | 0x0134 | W | 0x00000000 | Virtual line width for ID0 |
| VICAP_MIPI0_FRAME0_ADDR_Y_ID1 | 0x0138 | W | 0x00000000 | First address of even frame for ID1 Y/RAW/RGB path |
| VICAP_MIPI0_FRAME1_ADDR_Y_ID1 | 0x013C | W | 0x00000000 | First address of odd frame for ID1 Y/RAW/RGB path |
| VICAP_MIPI0_FRAME0_ADDR_UV_ID1 | 0x0140 | W | 0x00000000 | First address of even frame for ID1 UV path |
| VICAP_MIPI0_FRAME1_ADDR_UV_ID1 | 0x0144 | W | 0x00000000 | First address of odd frame for ID1 UV path |
| VICAP_MIPI0_VLW_ID1 | 0x0148 | W | 0x00000000 | Virtual line width of even frame for ID1 path |
| VICAP_MIPI0_FRAME0_ADDR_Y_ID2 | 0x014C | W | 0x00000000 | First address of even frame for ID2 Y/RAW/RGB path |
| VICAP_MIPI0_FRAME1_ADDR_Y_ID2 | 0x0150 | W | 0x00000000 | First address of odd frame for ID2 Y/RAW/RGB path |
| VICAP_MIPI0_FRAME0_ADDR_UV_ID2 | 0x0154 | W | 0x00000000 | First address of even frame for ID2 UV path |
| VICAP_MIPI0_FRAME1_ADDR_UV_ID2 | 0x0158 | W | 0x00000000 | First address of odd frame for ID2 UV path |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VICAP_MIPI0_VLW_ID2 | 0x015C | W | 0x00000000 | Virtual line width of even frame for ID2 path |
| VICAP_MIPI0_FRAME0_ADDR_Y_ID3 | 0x0160 | W | 0x00000000 | First address of even frame for ID3 Y/RAW/RGB path |
| VICAP_MIPI0_FRAME1_ADDR_Y_ID3 | 0x0164 | W | 0x00000000 | First address of odd frame for ID3 Y/RAW/RGB path |
| VICAP_MIPI0_FRAME0_ADDR_UV_ID3 | 0x0168 | W | 0x00000000 | First address of even frame for ID3 UV path |
| VICAP_MIPI0_FRAME1_ADDR_UV_ID3 | 0x016C | W | 0x00000000 | First address of odd frame for ID3 UV path |
| VICAP_MIPI0_VLW_ID3 | 0x0170 | W | 0x00000000 | Virtual line width of even frame for ID3 path |
| VICAP_MIPI0_INTEN | 0x0174 | W | 0x00000000 | MIPI0 path interrupt enable |
| VICAP_MIPI0_INTSTAT | 0x0178 | W | 0x00000000 | MIPI0 path interrupt status |
| VICAP_MIPI0_LINE_INT_NUM_ID0_1 | 0x017C | W | 0x00400040 | Line number of the MIPI0 path ID0/1 line interrupt |
| VICAP_MIPI0_LINE_INT_NUM_ID2_3 | 0x0180 | W | 0x00400040 | Line number of the MIPI0 path ID2/3 line interrupt |
| VICAP_MIPI0_LINE_CNT_ID0_1 | 0x0184 | W | 0x00000000 | Line count of the MIPI0 path ID0/1 |
| VICAP_MIPI0_LINE_CNT_ID2_3 | 0x0188 | W | 0x00000000 | Line count of the MIPI0 path ID2/3 |
| VICAP_MIPI0_ID0_CROP_START | 0x018C | W | 0x00000000 | The start point of MIPI0 ID0 cropping |
| VICAP_MIPI0_ID1_CROP_START | 0x0190 | W | 0x00000000 | The start point of MIPI0 ID1 cropping |
| VICAP_MIPI0_ID2_CROP_START | 0x0194 | W | 0x00000000 | The start point of MIPI0 ID2 cropping |
| VICAP_MIPI0_ID3_CROP_START | 0x0198 | W | 0x00000000 | The start point of MIPI0 ID3 cropping |
| VICAP_MIPI0_FRAME_NUM_VC0 | 0x019C | W | 0x00000000 | The frame number of virtual channel 0 |
| VICAP_MIPI0_FRAME_NUM_VC1 | 0x01A0 | W | 0x00000000 | The frame number of virtual channel 1 |
| VICAP_MIPI0_FRAME_NUM_VC2 | 0x01A4 | W | 0x00000000 | The frame number of virtual channel 2 |
| VICAP_MIPI0_FRAME_NUM_VC3 | 0x01A8 | W | 0x00000000 | The frame number of virtual channel 3 |
| VICAP_MIPI0_ID0_EFFECT_CODE | 0x01AC | W | 0x00000000 | The effect code of MIPI0 ID0 |
| VICAP_MIPI0_ID1_EFFECT_CODE | 0x01B0 | W | 0x00000000 | The effect code of MIPI0 ID1 |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VICAP_MIPI0_ID2_EFFECT_CODE | 0x01B4 | W | 0x00000000 | The effect code of MIPI0 ID2 |
| VICAP_MIPI0_ID3_EFFECT_CODE | 0x01B8 | W | 0x00000000 | The effect code of MIPI0 ID3 |
| VICAP_MIPI0_ON_PAD_VALUE | 0x01BC | W | 0x00000000 | The ON padding value of MIPI0 |
| VICAP_MIPI0_SIZE_NUM_ID0 | 0x01C0 | W | 0x00000000 | MIPI0 path ID0 SIZE NUMBER |
| VICAP_MIPI0_SIZE_NUM_ID1 | 0x01C4 | W | 0x00000000 | MIPI0 path ID1 SIZE NUMBER |
| VICAP_MIPI0_SIZE_NUM_ID2 | 0x01C8 | W | 0x00000000 | MIPI0 path ID2 SIZE NUMBER |
| VICAP_MIPI0_SIZE_NUM_ID3 | 0x01CC | W | 0x00000000 | MIPI0 path ID3 SIZE NUMBER |
| VICAP_MIPI1_ID0_CTRL0 | 0x0200 | W | 0x00000000 | MIPI1 path id0 control0 |
| VICAP_MIPI1_ID0_CTRL1 | 0x0204 | W | 0x00000000 | MIPI1 path id0 control1 |
| VICAP_MIPI1_ID1_CTRL0 | 0x0208 | W | 0x00000000 | MIPI1 path id1 control0 |
| VICAP_MIPI1_ID1_CTRL1 | 0x020C | W | 0x00000000 | MIPI1 path id1 control1 |
| VICAP_MIPI1_ID2_CTRL0 | 0x0210 | W | 0x00000000 | MIPI1 path id2 control0 |
| VICAP_MIPI1_ID2_CTRL1 | 0x0214 | W | 0x00000000 | MIPI1 path id2 control1 |
| VICAP_MIPI1_ID3_CTRL0 | 0x0218 | W | 0x00000000 | MIPI1 path id3 control0 |
| VICAP_MIPI1_ID3_CTRL1 | 0x021C | W | 0x00000000 | MIPI1 path id3 control1 |
| VICAP_MIPI1_CTRL | 0x0220 | W | 0x00000000 | MIPI1 path control |
| VICAP_MIPI1_FRAME0_ADDR_Y_ID0 | 0x0224 | W | 0x00000000 | First address of even frame for ID0 Y/RAW/RGB path |
| VICAP_MIPI1_FRAME1_ADDR_Y_ID0 | 0x0228 | W | 0x00000000 | First address of odd frame for ID0 Y path |
| VICAP_MIPI1_FRAME0_ADDR_UV_ID0 | 0x022C | W | 0x00000000 | First address of even frame for ID0 UV path |
| VICAP_MIPI1_FRAME1_ADDR_UV_ID0 | 0x0230 | W | 0x00000000 | First address of odd frame for ID0 UV path |
| VICAP_MIPI1_VLW_ID0 | 0x0234 | W | 0x00000000 | Virtual line width for ID0 |
| VICAP_MIPI1_FRAME0_ADDR_Y_ID1 | 0x0238 | W | 0x00000000 | First address of even frame for ID1 Y/RAW/RGB path |
| VICAP_MIPI1_FRAME1_ADDR_Y_ID1 | 0x023C | W | 0x00000000 | First address of odd frame for ID1 Y/RAW/RGB path |
| VICAP_MIPI1_FRAME0_ADDR_UV_ID1 | 0x0240 | W | 0x00000000 | First address of even frame for ID1 UV path |
| VICAP_MIPI1_FRAME1_ADDR_UV_ID1 | 0x0244 | W | 0x00000000 | First address of odd frame for ID1 UV path |
| VICAP_MIPI1_VLW_ID1 | 0x0248 | W | 0x00000000 | Virtual line width of even frame for ID1 path |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VICAP_MIPI1_FRAME0_ADDR_Y_ID2 | 0x024C | W | 0x00000000 | First address of even frame for ID2 Y/RAW/RGB path |
| VICAP_MIPI1_FRAME1_ADDR_Y_ID2 | 0x0250 | W | 0x00000000 | First address of odd frame for ID2 Y/RAW/RGB path |
| VICAP_MIPI1_FRAME0_ADDR_UV_ID2 | 0x0254 | W | 0x00000000 | First address of even frame for ID2 UV path |
| VICAP_MIPI1_FRAME1_ADDR_UV_ID2 | 0x0258 | W | 0x00000000 | First address of odd frame for ID2 UV path |
| VICAP_MIPI1_VLW_ID2 | 0x025C | W | 0x00000000 | Virtual line width of even frame for ID2 path |
| VICAP_MIPI1_FRAME0_ADDR_Y_ID3 | 0x0260 | W | 0x00000000 | First address of even frame for ID3 Y/RAW/RGB path |
| VICAP_MIPI1_FRAME1_ADDR_Y_ID3 | 0x0264 | W | 0x00000000 | First address of odd frame for ID3 Y/RAW/RGB path |
| VICAP_MIPI1_FRAME0_ADDR_UV_ID3 | 0x0268 | W | 0x00000000 | First address of even frame for ID3 UV path |
| VICAP_MIPI1_FRAME1_ADDR_UV_ID3 | 0x026C | W | 0x00000000 | First address of odd frame for ID3 UV path |
| VICAP_MIPI1_VLW_ID3 | 0x0270 | W | 0x00000000 | Virtual line width of even frame for ID3 path |
| VICAP_MIPI1_INTEN | 0x0274 | W | 0x00000000 | MIPI1 path interrupt enable |
| VICAP_MIPI1_INTSTAT | 0x0278 | W | 0x00000000 | MIPI1 path interrupt status |
| VICAP_MIPI1_LINE_INT_NUM_ID0_1 | 0x027C | W | 0x00400040 | Line number of the MIPI1 path ID0/1 line interrupt |
| VICAP_MIPI1_LINE_INT_NUM_ID2_3 | 0x0280 | W | 0x00400040 | Line number of the MIPI1 path ID2/3 line interrupt |
| VICAP_MIPI1_LINE_CNT_ID0_1 | 0x0284 | W | 0x00000000 | Line count of the MIPI1 path ID0/1 |
| VICAP_MIPI1_LINE_CNT_ID2_3 | 0x0288 | W | 0x00000000 | Line count of the MIPI1 path ID2/3 |
| VICAP_MIPI1_ID0_CROP_START | 0x028C | W | 0x00000000 | The start point of MIPI1 ID0 cropping |
| VICAP_MIPI1_ID1_CROP_START | 0x0290 | W | 0x00000000 | The start point of MIPI1 ID1 cropping |
| VICAP_MIPI1_ID2_CROP_START | 0x0294 | W | 0x00000000 | The start point of MIPI1 ID2 cropping |
| VICAP_MIPI1_ID3_CROP_START | 0x0298 | W | 0x00000000 | The start point of MIPI1 ID3 cropping |
| VICAP_MIPI1_FRAME_NUM_VC0 | 0x029C | W | 0x00000000 | The frame number of virtual channel 0 |
| VICAP_MIPI1_FRAME_NUM_VC1 | 0x02A0 | W | 0x00000000 | The frame number of virtual channel 1 |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VICAP_MIPI1_FRAME_NUM_VC2 | 0x02A4 | W | 0x00000000 | The frame number of virtual channel 2 |
| VICAP_MIPI1_FRAME_NUM_VC3 | 0x02A8 | W | 0x00000000 | The frame number of virtual channel 3 |
| VICAP_MIPI1_ID0_EFFECT_CODE | 0x02AC | W | 0x00000000 | The effect code of MIPI1 ID0 |
| VICAP_MIPI1_ID1_EFFECT_CODE | 0x02B0 | W | 0x00000000 | The effect code of MIPI1 ID1 |
| VICAP_MIPI1_ID2_EFFECT_CODE | 0x02B4 | W | 0x00000000 | The effect code of MIPI2 ID2 |
| VICAP_MIPI1_ID3_EFFECT_CODE | 0x02B8 | W | 0x00000000 | The effect code of MIPI1 ID3 |
| VICAP_MIPI1_ON_PAD_VALUE | 0x02BC | W | 0x00000000 | The ON padding value of MIPI1 |
| VICAP_MIPI1_SIZE_NUM_ID0 | 0x02C0 | W | 0x00000000 | MIPI1 path ID0 SIZE NUMBER |
| VICAP_MIPI1_SIZE_NUM_ID1 | 0x02C4 | W | 0x00000000 | MIPI1 path ID1 SIZE NUMBER |
| VICAP_MIPI1_SIZE_NUM_ID2 | 0x02C8 | W | 0x00000000 | MIPI1 path ID2 SIZE NUMBER |
| VICAP_MIPI1_SIZE_NUM_ID3 | 0x02CC | W | 0x00000000 | MIPI1 path ID3 SIZE NUMBER |
| VICAP_MIPI2_ID0_CTRL0 | 0x0300 | W | 0x00000000 | MIPI2 path id0 control0 |
| VICAP_MIPI2_ID0_CTRL1 | 0x0304 | W | 0x00000000 | MIPI2 path id0 control1 |
| VICAP_MIPI2_ID1_CTRL0 | 0x0308 | W | 0x00000000 | MIPI2 path id1 control0 |
| VICAP_MIPI2_ID1_CTRL1 | 0x030C | W | 0x00000000 | MIPI2 path id1 control1 |
| VICAP_MIPI2_ID2_CTRL0 | 0x0310 | W | 0x00000000 | MIPI2 path id2 control0 |
| VICAP_MIPI2_ID2_CTRL1 | 0x0314 | W | 0x00000000 | MIPI2 path id2 control1 |
| VICAP_MIPI2_ID3_CTRL0 | 0x0318 | W | 0x00000000 | MIPI2 path id3 control0 |
| VICAP_MIPI2_ID3_CTRL1 | 0x031C | W | 0x00000000 | MIPI2 path id3 control1 |
| VICAP_MIPI2_CTRL | 0x0320 | W | 0x00000000 | MIPI2 path control |
| VICAP_MIPI2_FRAME0_ADDR_Y_ID0 | 0x0324 | W | 0x00000000 | First address of even frame for ID0 Y/RAW/RGB path |
| VICAP_MIPI2_FRAME1_ADDR_Y_ID0 | 0x0328 | W | 0x00000000 | First address of odd frame for ID0 Y path |
| VICAP_MIPI2_FRAME0_ADDR_UV_ID0 | 0x032C | W | 0x00000000 | First address of even frame for ID0 UV path |
| VICAP_MIPI2_FRAME1_ADDR_UV_ID0 | 0x0330 | W | 0x00000000 | First address of odd frame for ID0 UV path |
| VICAP_MIPI2_VLW_ID0 | 0x0334 | W | 0x00000000 | Virtual line width for ID0 |
| VICAP_MIPI2_FRAME0_ADDR_Y_ID1 | 0x0338 | W | 0x00000000 | First address of even frame for ID1 Y/RAW/RGB path |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VICAP_MIPI2_FRAME1_ADDR_Y_ID1 | 0x033C | W | 0x00000000 | First address of odd frame for ID1 Y/RAW/RGB path |
| VICAP_MIPI2_FRAME0_ADDR_UV_ID1 | 0x0340 | W | 0x00000000 | First address of even frame for ID1 UV path |
| VICAP_MIPI2_FRAME1_ADDR_UV_ID1 | 0x0344 | W | 0x00000000 | First address of odd frame for ID1 UV path |
| VICAP_MIPI2_VLW_ID1 | 0x0348 | W | 0x00000000 | Virtual line width of even frame for ID1 path |
| VICAP_MIPI2_FRAME0_ADDR_Y_ID2 | 0x034C | W | 0x00000000 | First address of even frame for ID2 Y/RAW/RGB path |
| VICAP_MIPI2_FRAME1_ADDR_Y_ID2 | 0x0350 | W | 0x00000000 | First address of odd frame for ID2 Y/RAW/RGB path |
| VICAP_MIPI2_FRAME0_ADDR_UV_ID2 | 0x0354 | W | 0x00000000 | First address of even frame for ID2 UV path |
| VICAP_MIPI2_FRAME1_ADDR_UV_ID2 | 0x0358 | W | 0x00000000 | First address of odd frame for ID2 UV path |
| VICAP_MIPI2_VLW_ID2 | 0x035C | W | 0x00000000 | Virtual line width of even frame for ID2 path |
| VICAP_MIPI2_FRAME0_ADDR_Y_ID3 | 0x0360 | W | 0x00000000 | First address of even frame for ID3 Y/RAW/RGB path |
| VICAP_MIPI2_FRAME1_ADDR_Y_ID3 | 0x0364 | W | 0x00000000 | First address of odd frame for ID3 Y/RAW/RGB path |
| VICAP_MIPI2_FRAME0_ADDR_UV_ID3 | 0x0368 | W | 0x00000000 | First address of even frame for ID3 UV path |
| VICAP_MIPI2_FRAME1_ADDR_UV_ID3 | 0x036C | W | 0x00000000 | First address of odd frame for ID3 UV path |
| VICAP_MIPI2_VLW_ID3 | 0x0370 | W | 0x00000000 | Virtual line width of even frame for ID3 path |
| VICAP_MIPI2_INTEN | 0x0374 | W | 0x00000000 | MIPI2 path interrupt enable |
| VICAP_MIPI2_INTSTAT | 0x0378 | W | 0x00000000 | MIPI2 path interrupt status |
| VICAP_MIPI2_LINE_INT_NUM_ID0_1 | 0x037C | W | 0x00400040 | Line number of the MIPI2 path ID0/1 line interrupt |
| VICAP_MIPI2_LINE_INT_NUM_ID2_3 | 0x0380 | W | 0x00400040 | Line number of the MIPI2 path ID2/3 line interrupt |
| VICAP_MIPI2_LINE_CNT_ID0_1 | 0x0384 | W | 0x00000000 | Line count of the MIPI2 path ID0/1 |
| VICAP_MIPI2_LINE_CNT_ID2_3 | 0x0388 | W | 0x00000000 | Line count of the MIPI2 path ID2/3 |
| VICAP_MIPI2_ID0_CROP_START | 0x038C | W | 0x00000000 | The start point of MIPI2 ID0 cropping |
| VICAP_MIPI2_ID1_CROP_START | 0x0390 | W | 0x00000000 | The start point of MIPI2 ID1 cropping |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VICAP_MIPI2_ID2_CROP_START | 0x0394 | W | 0x00000000 | The start point of MIPI2 ID2 cropping |
| VICAP_MIPI2_ID3_CROP_START | 0x0398 | W | 0x00000000 | The start point of MIPI2 ID3 cropping |
| VICAP_MIPI2_FRAME_NUM_VC0 | 0x039C | W | 0x00000000 | The frame number of virtual channel 0 |
| VICAP_MIPI2_FRAME_NUM_VC1 | 0x03A0 | W | 0x00000000 | The frame number of virtual channel 1 |
| VICAP_MIPI2_FRAME_NUM_VC2 | 0x03A4 | W | 0x00000000 | The frame number of virtual channel 2 |
| VICAP_MIPI2_FRAME_NUM_VC3 | 0x03A8 | W | 0x00000000 | The frame number of virtual channel 3 |
| VICAP_MIPI2_ID0_EFFECT_CODE | 0x03AC | W | 0x00000000 | The effect code of MIPI2 ID0 |
| VICAP_MIPI2_ID1_EFFECT_CODE | 0x03B0 | W | 0x00000000 | The effect code of MIPI2 ID1 |
| VICAP_MIPI2_ID2_EFFECT_CODE | 0x03B4 | W | 0x00000000 | The effect code of MIPI2 ID2 |
| VICAP_MIPI2_ID3_EFFECT_CODE | 0x03B8 | W | 0x00000000 | The effect code of MIPI2 ID3 |
| VICAP_MIPI2_ON_PAD_VALUE | 0x03BC | W | 0x00000000 | The ON padding value of MIPI2 |
| VICAP_MIPI2_SIZE_NUM_ID0 | 0x03C0 | W | 0x00000000 | MIPI2 path ID0 SIZE NUMBER |
| VICAP_MIPI2_SIZE_NUM_ID1 | 0x03C4 | W | 0x00000000 | MIPI2 path ID1 SIZE NUMBER |
| VICAP_MIPI2_SIZE_NUM_ID2 | 0x03C8 | W | 0x00000000 | MIPI2 path ID2 SIZE NUMBER |
| VICAP_MIPI2_SIZE_NUM_ID3 | 0x03CC | W | 0x00000000 | MIPI2 path ID3 SIZE NUMBER |
| VICAP_MIPI3_ID0_CTRL0 | 0x0400 | W | 0x00000000 | MIPI3 path id0 control0 |
| VICAP_MIPI3_ID0_CTRL1 | 0x0404 | W | 0x00000000 | MIPI3 path id0 control1 |
| VICAP_MIPI3_ID1_CTRL0 | 0x0408 | W | 0x00000000 | MIPI3 path id1 control0 |
| VICAP_MIPI3_ID1_CTRL1 | 0x040C | W | 0x00000000 | MIPI3 path id1 control1 |
| VICAP_MIPI3_ID2_CTRL0 | 0x0410 | W | 0x00000000 | MIPI3 path id2 control0 |
| VICAP_MIPI3_ID2_CTRL1 | 0x0414 | W | 0x00000000 | MIPI3 path id2 control1 |
| VICAP_MIPI3_ID3_CTRL0 | 0x0418 | W | 0x00000000 | MIPI3 path id3 control0 |
| VICAP_MIPI3_ID3_CTRL1 | 0x041C | W | 0x00000000 | MIPI3 path id3 control1 |
| VICAP_MIPI3_CTRL | 0x0420 | W | 0x00000000 | MIPI3 path control |
| VICAP_MIPI3_FRAME0_ADDR_Y_ID0 | 0x0424 | W | 0x00000000 | First address of even frame for ID0 Y/RAW/RGB path |
| VICAP_MIPI3_FRAME1_ADDR_Y_ID0 | 0x0428 | W | 0x00000000 | First address of odd frame for ID0 Y path |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VICAP_MIPI3_FRAME0_ADDR_UV_ID0 | 0x042C | W | 0x00000000 | First address of even frame for ID0 UV path |
| VICAP_MIPI3_FRAME1_ADDR_UV_ID0 | 0x0430 | W | 0x00000000 | First address of odd frame for ID0 UV path |
| VICAP_MIPI3_VLW_ID0 | 0x0434 | W | 0x00000000 | Virtual line width for ID0 |
| VICAP_MIPI3_FRAME0_ADDR_Y_ID1 | 0x0438 | W | 0x00000000 | First address of even frame for ID1 Y/RAW/RGB path |
| VICAP_MIPI3_FRAME1_ADDR_Y_ID1 | 0x043C | W | 0x00000000 | First address of odd frame for ID1 Y/RAW/RGB path |
| VICAP_MIPI3_FRAME0_ADDR_UV_ID1 | 0x0440 | W | 0x00000000 | First address of even frame for ID1 UV path |
| VICAP_MIPI3_FRAME1_ADDR_UV_ID1 | 0x0444 | W | 0x00000000 | First address of odd frame for ID1 UV path |
| VICAP_MIPI3_VLW_ID1 | 0x0448 | W | 0x00000000 | Virtual line width of even frame for ID1 path |
| VICAP_MIPI3_FRAME0_ADDR_Y_ID2 | 0x044C | W | 0x00000000 | First address of even frame for ID2 Y/RAW/RGB path |
| VICAP_MIPI3_FRAME1_ADDR_Y_ID2 | 0x0450 | W | 0x00000000 | First address of odd frame for ID2 Y/RAW/RGB path |
| VICAP_MIPI3_FRAME0_ADDR_UV_ID2 | 0x0454 | W | 0x00000000 | First address of even frame for ID2 UV path |
| VICAP_MIPI3_FRAME1_ADDR_UV_ID2 | 0x0458 | W | 0x00000000 | First address of odd frame for ID2 UV path |
| VICAP_MIPI3_VLW_ID2 | 0x045C | W | 0x00000000 | Virtual line width of even frame for ID2 path |
| VICAP_MIPI3_FRAME0_ADDR_Y_ID3 | 0x0460 | W | 0x00000000 | First address of even frame for ID3 Y/RAW/RGB path |
| VICAP_MIPI3_FRAME1_ADDR_Y_ID3 | 0x0464 | W | 0x00000000 | First address of odd frame for ID3 Y/RAW/RGB path |
| VICAP_MIPI3_FRAME0_ADDR_UV_ID3 | 0x0468 | W | 0x00000000 | First address of even frame for ID3 UV path |
| VICAP_MIPI3_FRAME1_ADDR_UV_ID3 | 0x046C | W | 0x00000000 | First address of odd frame for ID3 UV path |
| VICAP_MIPI3_VLW_ID3 | 0x0470 | W | 0x00000000 | Virtual line width of even frame for ID3 path |
| VICAP_MIPI3_INTEN | 0x0474 | W | 0x00000000 | MIPI3 path interrupt enable |
| VICAP_MIPI3_INTSTAT | 0x0478 | W | 0x00000000 | MIPI3 path interrupt status |
| VICAP_MIPI3_LINE_INT_NUM_ID0_1 | 0x047C | W | 0x00400040 | Line number of the MIPI3 path ID0/1 line interrupt |
| VICAP_MIPI3_LINE_INT_NUM_ID2_3 | 0x0480 | W | 0x00400040 | Line number of the MIPI3 path ID2/3 line interrupt |
| VICAP_MIPI3_LINE_CNT_ID0_1 | 0x0484 | W | 0x00000000 | Line count of the MIPI3 path ID0/1 |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VICAP_MIPI3_LINE_CNT_ID2_3 | 0x0488 | W | 0x00000000 | Line count of the MIPI3 path ID2/3 |
| VICAP_MIPI3_ID0_CROP_START | 0x048C | W | 0x00000000 | The start point of MIPI3 ID0 cropping |
| VICAP_MIPI3_ID1_CROP_START | 0x0490 | W | 0x00000000 | The start point of MIPI3 ID1 cropping |
| VICAP_MIPI3_ID2_CROP_START | 0x0494 | W | 0x00000000 | The start point of MIPI3 ID2 cropping |
| VICAP_MIPI3_ID3_CROP_START | 0x0498 | W | 0x00000000 | The start point of MIPI3 ID3 cropping |
| VICAP_MIPI3_FRAME_NUM_VC0 | 0x049C | W | 0x00000000 | The frame number of virtual channel 0 |
| VICAP_MIPI3_FRAME_NUM_VC1 | 0x04A0 | W | 0x00000000 | The frame number of virtual channel 1 |
| VICAP_MIPI3_FRAME_NUM_VC2 | 0x04A4 | W | 0x00000000 | The frame number of virtual channel 2 |
| VICAP_MIPI3_FRAME_NUM_VC3 | 0x04A8 | W | 0x00000000 | The frame number of virtual channel 3 |
| VICAP_MIPI3_ID0_EFFECT_CODE | 0x04AC | W | 0x00000000 | The effect code of MIPI3 ID0 |
| VICAP_MIPI3_ID1_EFFECT_CODE | 0x04B0 | W | 0x00000000 | The effect code of MIPI3 ID1 |
| VICAP_MIPI3_ID2_EFFECT_CODE | 0x04B4 | W | 0x00000000 | The effect code of MIPI3 ID2 |
| VICAP_MIPI3_ID3_EFFECT_CODE | 0x04B8 | W | 0x00000000 | The effect code of MIPI3 ID3 |
| VICAP_MIPI3_ON_PAD_VALUE | 0x04BC | W | 0x00000000 | The ON padding value of MIPI3 |
| VICAP_MIPI3_SIZE_NUM_ID0 | 0x04C0 | W | 0x00000000 | MIPI3 path ID0 SIZE NUMBER |
| VICAP_MIPI3_SIZE_NUM_ID1 | 0x04C4 | W | 0x00000000 | MIPI3 path ID1 SIZE NUMBER |
| VICAP_MIPI3_SIZE_NUM_ID2 | 0x04C8 | W | 0x00000000 | MIPI3 path ID2 SIZE NUMBER |
| VICAP_MIPI3_SIZE_NUM_ID3 | 0x04CC | W | 0x00000000 | MIPI3 path ID3 SIZE NUMBER |
| VICAP_MIPI4_ID0_CTRL0 | 0x0500 | W | 0x00000000 | MIPI4 path id0 control0 |
| VICAP_MIPI4_ID0_CTRL1 | 0x0504 | W | 0x00000000 | MIPI4 path id0 control1 |
| VICAP_MIPI4_ID1_CTRL0 | 0x0508 | W | 0x00000000 | MIPI4 path id1 control0 |
| VICAP_MIPI4_ID1_CTRL1 | 0x050C | W | 0x00000000 | MIPI4 path id1 control1 |
| VICAP_MIPI4_ID2_CTRL0 | 0x0510 | W | 0x00000000 | MIPI4 path id2 control0 |
| VICAP_MIPI4_ID2_CTRL1 | 0x0514 | W | 0x00000000 | MIPI4 path id2 control1 |
| VICAP_MIPI4_ID3_CTRL0 | 0x0518 | W | 0x00000000 | MIPI4 path id3 control0 |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VICAP_MIPI4_ID3_CTRL1 | 0x051C | W | 0x00000000 | MIPI4 path id3 control1 |
| VICAP_MIPI4_CTRL | 0x0520 | W | 0x00000000 | MIPI4 path control |
| VICAP_MIPI4_FRAME0_ADDR_Y_ID0 | 0x0524 | W | 0x00000000 | First address of even frame for ID0 Y/RAW/RGB path |
| VICAP_MIPI4_FRAME1_ADDR_Y_ID0 | 0x0528 | W | 0x00000000 | First address of odd frame for ID0 Y path |
| VICAP_MIPI4_FRAME0_ADDR_UV_ID0 | 0x052C | W | 0x00000000 | First address of even frame for ID0 UV path |
| VICAP_MIPI4_FRAME1_ADDR_UV_ID0 | 0x0530 | W | 0x00000000 | First address of odd frame for ID0 UV path |
| VICAP_MIPI4_VLW_ID0 | 0x0534 | W | 0x00000000 | Virtual line width for ID0 |
| VICAP_MIPI4_FRAME0_ADDR_Y_ID1 | 0x0538 | W | 0x00000000 | First address of even frame for ID1 Y/RAW/RGB path |
| VICAP_MIPI4_FRAME1_ADDR_Y_ID1 | 0x053C | W | 0x00000000 | First address of odd frame for ID1 Y/RAW/RGB path |
| VICAP_MIPI4_FRAME0_ADDR_UV_ID1 | 0x0540 | W | 0x00000000 | First address of even frame for ID1 UV path |
| VICAP_MIPI4_FRAME1_ADDR_UV_ID1 | 0x0544 | W | 0x00000000 | First address of odd frame for ID1 UV path |
| VICAP_MIPI4_VLW_ID1 | 0x0548 | W | 0x00000000 | Virtual line width of even frame for ID1 path |
| VICAP_MIPI4_FRAME0_ADDR_Y_ID2 | 0x054C | W | 0x00000000 | First address of even frame for ID2 Y/RAW/RGB path |
| VICAP_MIPI4_FRAME1_ADDR_Y_ID2 | 0x0550 | W | 0x00000000 | First address of odd frame for ID2 Y/RAW/RGB path |
| VICAP_MIPI4_FRAME0_ADDR_UV_ID2 | 0x0554 | W | 0x00000000 | First address of even frame for ID2 UV path |
| VICAP_MIPI4_FRAME1_ADDR_UV_ID2 | 0x0558 | W | 0x00000000 | First address of odd frame for ID2 UV path |
| VICAP_MIPI4_VLW_ID2 | 0x055C | W | 0x00000000 | Virtual line width of even frame for ID2 path |
| VICAP_MIPI4_FRAME0_ADDR_Y_ID3 | 0x0560 | W | 0x00000000 | First address of even frame for ID3 Y/RAW/RGB path |
| VICAP_MIPI4_FRAME1_ADDR_Y_ID3 | 0x0564 | W | 0x00000000 | First address of odd frame for ID3 Y/RAW/RGB path |
| VICAP_MIPI4_FRAME0_ADDR_UV_ID3 | 0x0568 | W | 0x00000000 | First address of even frame for ID3 UV path |
| VICAP_MIPI4_FRAME1_ADDR_UV_ID3 | 0x056C | W | 0x00000000 | First address of odd frame for ID3 UV path |
| VICAP_MIPI4_VLW_ID3 | 0x0570 | W | 0x00000000 | Virtual line width of even frame for ID3 path |
| VICAP_MIPI4_INTEN | 0x0574 | W | 0x00000000 | MIPI4 path interrupt enable |
| VICAP_MIPI4_INTSTAT | 0x0578 | W | 0x00000000 | MIPI4 path interrupt status |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VICAP_MIPI4_LINE_INT_NUM_ID0_1 | 0x057C | W | 0x00400040 | Line number of the MIPI4 path ID0/1 line interrupt |
| VICAP_MIPI4_LINE_INT_NUM_ID2_3 | 0x0580 | W | 0x00400040 | Line number of the MIPI4 path ID2/3 line interrupt |
| VICAP_MIPI4_LINE_CNT_ID0_1 | 0x0584 | W | 0x00000000 | Line count of the MIPI4 path ID0/1 |
| VICAP_MIPI4_LINE_CNT_ID2_3 | 0x0588 | W | 0x00000000 | Line count of the MIPI4 path ID2/3 |
| VICAP_MIPI4_ID0_CROP_START | 0x058C | W | 0x00000000 | The start point of MIPI4 ID0 cropping |
| VICAP_MIPI4_ID1_CROP_START | 0x0590 | W | 0x00000000 | The start point of MIPI4 ID1 cropping |
| VICAP_MIPI4_ID2_CROP_START | 0x0594 | W | 0x00000000 | The start point of MIPI4 ID2 cropping |
| VICAP_MIPI4_ID3_CROP_START | 0x0598 | W | 0x00000000 | The start point of MIPI4 ID3 cropping |
| VICAP_MIPI4_FRAME_NUM_VC0 | 0x059C | W | 0x00000000 | The frame number of virtual channel 0 |
| VICAP_MIPI4_FRAME_NUM_VC1 | 0x05A0 | W | 0x00000000 | The frame number of virtual channel 1 |
| VICAP_MIPI4_FRAME_NUM_VC2 | 0x05A4 | W | 0x00000000 | The frame number of virtual channel 2 |
| VICAP_MIPI4_FRAME_NUM_VC3 | 0x05A8 | W | 0x00000000 | The frame number of virtual channel 3 |
| VICAP_MIPI4_ID0_EFFECT_CODE | 0x05AC | W | 0x00000000 | The effect code of MIPI4 ID0 |
| VICAP_MIPI4_ID1_EFFECT_CODE | 0x05B0 | W | 0x00000000 | The effect code of MIPI4 ID1 |
| VICAP_MIPI4_ID2_EFFECT_CODE | 0x05B4 | W | 0x00000000 | The effect code of MIPI4 ID2 |
| VICAP_MIPI4_ID3_EFFECT_CODE | 0x05B8 | W | 0x00000000 | The effect code of MIPI4 ID3 |
| VICAP_MIPI4_ON_PAD_VALUE | 0x05BC | W | 0x00000000 | The ON padding value of MIPI4 |
| VICAP_MIPI4_SIZE_NUM_ID0 | 0x05C0 | W | 0x00000000 | MIPI4 path ID0 SIZE NUMBER |
| VICAP_MIPI4_SIZE_NUM_ID1 | 0x05C4 | W | 0x00000000 | MIPI4 path ID1 SIZE NUMBER |
| VICAP_MIPI4_SIZE_NUM_ID2 | 0x05C8 | W | 0x00000000 | MIPI4 path ID2 SIZE NUMBER |
| VICAP_MIPI4_SIZE_NUM_ID3 | 0x05CC | W | 0x00000000 | MIPI4 path ID3 SIZE NUMBER |
| VICAP_MIPI5_ID0_CTRL0 | 0x0600 | W | 0x00000000 | MIPI5 path id0 control0 |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VICAP_MIPI5_ID0_CTRL1 | 0x0604 | W | 0x00000000 | MIPI5 path id0 control1 |
| VICAP_MIPI5_ID1_CTRL0 | 0x0608 | W | 0x00000000 | MIPI5 path id1 control0 |
| VICAP_MIPI5_ID1_CTRL1 | 0x060C | W | 0x00000000 | MIPI5 path id1 control1 |
| VICAP_MIPI5_ID2_CTRL0 | 0x0610 | W | 0x00000000 | MIPI5 path id2 control0 |
| VICAP_MIPI5_ID2_CTRL1 | 0x0614 | W | 0x00000000 | MIPI5 path id2 control1 |
| VICAP_MIPI5_ID3_CTRL0 | 0x0618 | W | 0x00000000 | MIPI5 path id3 control0 |
| VICAP_MIPI5_ID3_CTRL1 | 0x061C | W | 0x00000000 | MIPI5 path id3 control1 |
| VICAP_MIPI5_CTRL | 0x0620 | W | 0x00000000 | MIPI5 path control |
| VICAP_MIPI5_FRAME0_ADDR_Y_ID0 | 0x0624 | W | 0x00000000 | First address of even frame for ID0 Y/RAW/RGB path |
| VICAP_MIPI5_FRAME1_ADDR_Y_ID0 | 0x0628 | W | 0x00000000 | First address of odd frame for ID0 Y path |
| VICAP_MIPI5_FRAME0_ADDR_UV_ID0 | 0x062C | W | 0x00000000 | First address of even frame for ID0 UV path |
| VICAP_MIPI5_FRAME1_ADDR_UV_ID0 | 0x0630 | W | 0x00000000 | First address of odd frame for ID0 UV path |
| VICAP_MIPI5_VLW_ID0 | 0x0634 | W | 0x00000000 | Virtual line width for ID0 |
| VICAP_MIPI5_FRAME0_ADDR_Y_ID1 | 0x0638 | W | 0x00000000 | First address of even frame for ID1 Y/RAW/RGB path |
| VICAP_MIPI5_FRAME1_ADDR_Y_ID1 | 0x063C | W | 0x00000000 | First address of odd frame for ID1 Y/RAW/RGB path |
| VICAP_MIPI5_FRAME0_ADDR_UV_ID1 | 0x0640 | W | 0x00000000 | First address of even frame for ID1 UV path |
| VICAP_MIPI5_FRAME1_ADDR_UV_ID1 | 0x0644 | W | 0x00000000 | First address of odd frame for ID1 UV path |
| VICAP_MIPI5_VLW_ID1 | 0x0648 | W | 0x00000000 | Virtual line width of even frame for ID1 path |
| VICAP_MIPI5_FRAME0_ADDR_Y_ID2 | 0x064C | W | 0x00000000 | First address of even frame for ID2 Y/RAW/RGB path |
| VICAP_MIPI5_FRAME1_ADDR_Y_ID2 | 0x0650 | W | 0x00000000 | First address of odd frame for ID2 Y/RAW/RGB path |
| VICAP_MIPI5_FRAME0_ADDR_UV_ID2 | 0x0654 | W | 0x00000000 | First address of even frame for ID2 UV path |
| VICAP_MIPI5_FRAME1_ADDR_UV_ID2 | 0x0658 | W | 0x00000000 | First address of odd frame for ID2 UV path |
| VICAP_MIPI5_VLW_ID2 | 0x065C | W | 0x00000000 | Virtual line width of even frame for ID2 path |
| VICAP_MIPI5_FRAME0_ADDR_Y_ID3 | 0x0660 | W | 0x00000000 | First address of even frame for ID3 Y/RAW/RGB path |
| VICAP_MIPI5_FRAME1_ADDR_Y_ID3 | 0x0664 | W | 0x00000000 | First address of odd frame for ID3 Y/RAW/RGB path |
| VICAP_MIPI5_FRAME0_ADDR_UV_ID3 | 0x0668 | W | 0x00000000 | First address of even frame for ID3 UV path |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VICAP_MIPI5_FRAME1_ADDR_UV_ID3 | 0x066C | W | 0x00000000 | First address of odd frame for ID3 UV path |
| VICAP_MIPI5_VLW_ID3 | 0x0670 | W | 0x00000000 | Virtual line width of even frame for ID3 path |
| VICAP_MIPI5_INTEN | 0x0674 | W | 0x00000000 | MIPI5 path interrupt enable |
| VICAP_MIPI5_INTSTAT | 0x0678 | W | 0x00000000 | MIPI5 path interrupt status |
| VICAP_MIPI5_LINE_INT_NUM_ID0_1 | 0x067C | W | 0x00400040 | Line number of the MIPI5 path ID0/1 line interrupt |
| VICAP_MIPI5_LINE_INT_NUM_ID2_3 | 0x0680 | W | 0x00400040 | Line number of the MIPI5 path ID2/3 line interrupt |
| VICAP_MIPI5_LINE_CNT_ID0_1 | 0x0684 | W | 0x00000000 | Line count of the MIPI5 path ID0/1 |
| VICAP_MIPI5_LINE_CNT_ID2_3 | 0x0688 | W | 0x00000000 | Line count of the MIPI5 path ID2/3 |
| VICAP_MIPI5_ID0_CROP_START | 0x068C | W | 0x00000000 | The start point of MIPI5 ID0 cropping |
| VICAP_MIPI5_ID1_CROP_START | 0x0690 | W | 0x00000000 | The start point of MIPI5 ID1 cropping |
| VICAP_MIPI5_ID2_CROP_START | 0x0694 | W | 0x00000000 | The start point of MIPI5 ID2 cropping |
| VICAP_MIPI5_ID3_CROP_START | 0x0698 | W | 0x00000000 | The start point of MIPI5 ID3 cropping |
| VICAP_MIPI5_FRAME_NUM_VC0 | 0x069C | W | 0x00000000 | The frame number of virtual channel 0 |
| VICAP_MIPI5_FRAME_NUM_VC1 | 0x06A0 | W | 0x00000000 | The frame number of virtual channel 1 |
| VICAP_MIPI5_FRAME_NUM_VC2 | 0x06A4 | W | 0x00000000 | The frame number of virtual channel 2 |
| VICAP_MIPI5_FRAME_NUM_VC3 | 0x06A8 | W | 0x00000000 | The frame number of virtual channel 3 |
| VICAP_MIPI5_ID0_EFFECT_CODE | 0x06AC | W | 0x00000000 | The effect code of MIPI5 ID0 |
| VICAP_MIPI5_ID1_EFFECT_CODE | 0x06B0 | W | 0x00000000 | The effect code of MIPI5 ID1 |
| VICAP_MIPI5_ID2_EFFECT_CODE | 0x06B4 | W | 0x00000000 | The effect code of MIPI5 ID2 |
| VICAP_MIPI5_ID3_EFFECT_CODE | 0x06B8 | W | 0x00000000 | The effect code of MIPI5 ID3 |
| VICAP_MIPI5_ON_PAD_VALUE | 0x06BC | W | 0x00000000 | The ON padding value of MIPI5 |
| VICAP_MIPI5_SIZE_NUM_ID0 | 0x06C0 | W | 0x00000000 | MIPI5 path ID0 SIZE NUMBER |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VICAP_MIPI5_SIZE_NUM_ID1 | 0x06C4 | W | 0x00000000 | MIPI5 path ID1 SIZE NUMBER |
| VICAP_MIPI5_SIZE_NUM_ID2 | 0x06C8 | W | 0x00000000 | MIPI5 path ID2 SIZE NUMBER |
| VICAP_MIPI5_SIZE_NUM_ID3 | 0x06CC | W | 0x00000000 | MIPI5 path ID3 SIZE NUMBER |
| VICAP_SCL_CH_CTRL | 0x0700 | W | 0x00000000 | Scale channel0 path control |
| VICAP_SCL_CTRL | 0x0704 | W | 0x00000000 | MIPI3 path control |
| VICAP_SCL_FRAME0_ADDR_CH0 | 0x0708 | W | 0x00000000 | First address of even frame for CH0 path |
| VICAP_SCL_FRAME1_ADDR_CH0 | 0x070C | W | 0x00000000 | First address of odd frame for CH0 path |
| VICAP_SCL_VLW_CH0 | 0x0710 | W | 0x00000000 | Virtual line width for CH0 |
| VICAP_SCL_FRAME0_ADDR_CH1 | 0x0714 | W | 0x00000000 | First address of even frame for CH1 path |
| VICAP_SCL_FRAME1_ADDR_CH1 | 0x0718 | W | 0x00000000 | First address of odd frame for CH1 path |
| VICAP_SCL_VLW_CH1 | 0x071C | W | 0x00000000 | Virtual line width for CH0 |
| VICAP_SCL_FRAME0_ADDR_CH2 | 0x0720 | W | 0x00000000 | First address of even frame for CH2 path |
| VICAP_SCL_FRAME1_ADDR_CH2 | 0x0724 | W | 0x00000000 | First address of odd frame for CH2 path |
| VICAP_SCL_VLW_CH2 | 0x0728 | W | 0x00000000 | Virtual line width for CH2 |
| VICAP_SCL_FRAME0_ADDR_CH3 | 0x072C | W | 0x00000000 | First address of even frame for CH3 path |
| VICAP_SCL_FRAME1_ADDR_CH3 | 0x0730 | W | 0x00000000 | First address of odd frame for CH1 path |
| VICAP_SCL_VLW_CH3 | 0x0734 | W | 0x00000000 | Virtual line width for CH3 |
| VICAP_SCL_CH0_BLACK_LEVEL | 0x0738 | W | 0x00000000 | Scale channel0 black level |
| VICAP_SCL_CH1_BLACK_LEVEL | 0x073C | W | 0x00000000 | Scale channel1 black level |
| VICAP_SCL_CH2_BLACK_LEVEL | 0x0740 | W | 0x00000000 | Scale channel2 black level |
| VICAP_SCL_CH3_BLACK_LEVEL | 0x0744 | W | 0x00000000 | Scale channel3 black level |
| VICAP_TOISP0_CH_CTRL | 0x0780 | W | 0x00000000 | TOISP0 path control |
| VICAP_TOISP0_CROP_SIZE | 0x0784 | W | 0x01E002D0 | The expected width and height of received image |
| VICAP_TOISP0_CROP_START | 0x0788 | W | 0x00000000 | The start point of toisp0 path cropping |
| VICAP_TOISP1_CH_CTRL | 0x078C | W | 0x00000000 | TOISP1 path control |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| VICAP_TOISP1_CROP_SIZE | 0x0790 | W | 0x01E002D0 | The expected width and height of received image |
| VICAP_TOISP1_CROP_START | 0x0794 | W | 0x00000000 | The start point of toisp1 path cropping |
| VICAP_MMU0_DTE_ADDR | 0x0800 | W | 0x00000000 | MMU0 current page table address |
| VICAP_MMU0_STATUS | 0x0804 | W | 0x00000000 | MMU0 status register |
| VICAP_MMU0_COMMAND | 0x0808 | W | 0x00000000 | MMU0 command register |
| VICAP_MMU0_PAGE_FAULT_ADDR | 0x080C | W | 0x00000000 | MMU0 logical address of last page fault |
| VICAP_MMU0_ZAP_ONE_LINE | 0x0810 | W | 0x00000000 | MMU0 Zap cache line register |
| VICAP_MMU0_INT_RAWSTAT | 0x0814 | W | 0x00000000 | MMU0 raw interrupt status register |
| VICAP_MMU0_INT_CLEAR | 0x0818 | W | 0x00000000 | MMU0 interrupt status clear |
| VICAP_MMU0_INT_MASK | 0x081C | W | 0x00000000 | MMU0 interrupt mask |
| VICAP_MMU0_INT_STATUS | 0x0820 | W | 0x00000000 | MMU0 interrupt status |
| VICAP_MMU0_AUTO_GATING | 0x0824 | W | 0x00000000 | MMU0 auto gating |
| VICAP_MMU1_DTE_ADDR | 0x0900 | W | 0x00000000 | MMU1 current page table address |
| VICAP_MMU1_STATUS | 0x0904 | W | 0x00000000 | MMU1 status register |
| VICAP_MMU1_COMMAND | 0x0908 | W | 0x00000000 | MMU1 command register |
| VICAP_MMU1_PAGE_FAULT_ADDR | 0x090C | W | 0x00000000 | MMU1 logical address of last page fault |
| VICAP_MMU1_ZAP_ONE_LINE | 0x0910 | W | 0x00000000 | MMU1 Zap cache line register |
| VICAP_MMU1_INT_RAWSTAT | 0x0914 | W | 0x00000000 | MMU1 raw interrupt status register |
| VICAP_MMU1_INT_CLEAR | 0x0918 | W | 0x00000000 | MMU1 interrupt status clear |
| VICAP_MMU1_INT_MASK | 0x091C | W | 0x00000000 | MMU1 interrupt mask |
| VICAP_MMU1_INT_STATUS | 0x0920 | W | 0x00000000 | MMU1 interrupt status |
| VICAP_MMU1_AUTO_GATING | 0x0924 | W | 0x00000000 | MMU1 auto gating |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

## 37.4.3 Detail Registers Description

### VICAP_GLB_CTRL

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:17 | RO | 0x0000 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 16 | RW | 0x1 | ro_axi_idle<br>1'b0: AXI is working<br>1'b1: AXI is idle. |
| 15:9 | RO | 0x00 | reserved |
| 8 | RW | 0x0 | sw_clk_gating_dis<br>1'b0: Enable the auto clk gating<br>1'b1: Disable the auto clk gating |
| 7 | RO | 0x0 | reserved |
| 6:5 | RW | 0x0 | sw_soft_rst_mode<br>2'b00: Soft reset and protect toisp path frame integrity;<br>2'b01: Soft reset and protect toisp path frame integrity and pull down sw_cap_en automatically;<br>2'b10: Soft reset directly;<br>2'b11: Reserved. |
| 4 | RW | 0x0 | sw_soft_rst<br>1'b0: Not reset<br>1'b1: Reset the VICAP(except MMU/AXI MASTER/REG FILE) |
| 3:1 | RO | 0x0 | reserved |
| 0 | RW | 0x1 | sw_cap_en<br>1'b0: Disable all interface capture<br>1'b1: Enable capture(still depends on sw_xxx_cap_en). |

**VICAP_GLB_INTEN**

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27 | RW | 0x0 | toisp1_fifo_overflow_inten<br>Enable the interrupt of fifo overflow of TOISP1 path.<br>1'b0: Disable<br>1'b1: Enable |
| 26 | RW | 0x0 | toisp0_fifo_overflow_inten<br>Enable the interrupt of fifo overflow of TOISP0 path.<br>1'b0: Disable<br>1'b1: Enable |
| 25 | RW | 0x0 | frame_end_toisp1_ch2_inten<br>Enable the interrupt of frame end for TOISP1 channel2.<br>1'b0: Disable<br>1'b1: Enable |
| 24 | RW | 0x0 | frame_end_toisp1_ch1_inten<br>Enable the interrupt of frame end for TOISP1 channel1.<br>1'b0: Disable<br>1'b1: Enable |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23 | RW | 0x0 | frame_end_toisp1_ch0_inten<br>Enable the interrupt of frame end for TOISP1 channel0.<br>1'b0: Disable<br>1'b1: Enable |
| 22 | RW | 0x0 | frame_end_toisp0_ch2_inten<br>Enable the interrupt of frame end for TOISP0 channel2.<br>1'b0: Disable<br>1'b1: Enable |
| 21 | RW | 0x0 | frame_end_toisp0_ch1_inten<br>Enable the interrupt of frame end for TOISP0 channel1.<br>1'b0: Disable<br>1'b1: Enable |
| 20 | RW | 0x0 | frame_end_toisp0_ch0_inten<br>Enable the interrupt of frame end for TOISP0 channel0.<br>1'b0: Disable<br>1'b1: Enable |
| 19 | RW | 0x0 | frame_start_toisp1_ch2_inten<br>Enable the interrupt of frame start for TOISP1 channel2.<br>1'b0: Disable<br>1'b1: Enable |
| 18 | RW | 0x0 | frame_start_toisp1_ch1_inten<br>Enable the interrupt of frame start for TOISP1 channel1.<br>1'b0: Disable<br>1'b1: Enable |
| 17 | RW | 0x0 | frame_start_toisp1_ch0_inten<br>Enable the interrupt of frame start for TOISP1 channel0.<br>1'b0: Disable<br>1'b1: Enable |
| 16 | RW | 0x0 | frame_start_toisp0_ch2_inten<br>Enable the interrupt of frame start for TOISP0 channel2.<br>1'b0: Disable<br>1'b1: Enable |
| 15 | RW | 0x0 | frame_start_toisp0_ch1_inten<br>Enable the interrupt of frame start for TOISP0 channel1.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | frame_start_toisp0_ch0_inten<br>Enable the interrupt of frame start for TOISP0 channel0.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | dma_fifo_overflow_scl_ch3_inten<br>Enable the interrupt of dma fifo overflow of scale path CH3.<br>1'b0: Disable<br>1'b1: Enable |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | RW | 0x0 | dma_fifo_overflow_scl_ch2_inten<br>Enable the interrupt of dma fifo overflow of scale path CH2.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | dma_fifo_overflow_scl_ch1_inten<br>Enable the interrupt of dma fifo overflow of scale path CH1.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | dma_fifo_overflow_scl_ch0_inten<br>Enable the interrupt of dma fifo overflow of scale path CH0.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | frame1_dma_end_scl_ch3_inten<br>Enable the interrupt of end of odd frame for scale CH3.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | frame0_dma_end_scl_ch3_inten<br>Enable the interrupt of end of even frame for scale CH3.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | frame1_dma_end_scl_ch2_inten<br>Enable the interrupt of end of odd frame for scale CH2.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | frame0_dma_end_scl_ch2_inten<br>Enable the interrupt of end of even frame for scale CH2.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | frame1_dma_end_scl_ch1_inten<br>Enable the interrupt of end of odd frame for scale CH1.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | frame0_dma_end_scl_ch1_inten<br>Enable the interrupt of end of even frame for scale CH1.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | frame1_dma_end_scl_ch0_inten<br>Enable the interrupt of end of odd frame for scale CH0.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | frame0_dma_end_scl_ch0_inten<br>Enable the interrupt of end of even frame for scale CH0.<br>1'b0: Disable<br>1'b1: Enable |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | axi1_bus_err_inten<br>Enable the interrupt of axi1 bus error.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | axi0_bus_err_inten<br>Enable the interrupt of axi0 bus error.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_GLB_INTST**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27 | W1C | 0x0 | toisp1_fifo_overflow_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 26 | W1C | 0x0 | toisp0_fifo_overflow_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 25 | W1C | 0x0 | frame_end_toisp1_ch2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 24 | W1C | 0x0 | frame_end_toisp1_ch1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 23 | W1C | 0x0 | frame_end_toisp1_ch0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 22 | W1C | 0x0 | frame_end_toisp0_ch2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 21 | W1C | 0x0 | frame_end_toisp0_ch1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 20 | W1C | 0x0 | frame_end_toisp0_ch0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 19 | W1C | 0x0 | frame_start_toisp1_ch2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 18 | W1C | 0x0 | frame_start_toisp1_ch1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17 | W1C | 0x0 | frame_start_toisp1_ch0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 16 | W1C | 0x0 | frame_start_toisp0_ch2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 15 | W1C | 0x0 | frame_start_toisp0_ch1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 14 | W1C | 0x0 | frame_start_toisp0_ch0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 13 | W1C | 0x0 | dma_fifo_overflow_scl_ch3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 12 | W1C | 0x0 | dma_fifo_overflow_scl_ch2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 11 | W1C | 0x0 | dma_fifo_overflow_scl_ch1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 10 | W1C | 0x0 | dma_fifo_overflow_scl_ch0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 9 | W1C | 0x0 | frame1_dma_end_scl_ch3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 8 | W1C | 0x0 | frame0_dma_end_scl_ch3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 7 | W1C | 0x0 | frame1_dma_end_scl_ch2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 6 | W1C | 0x0 | frame0_dma_end_scl_ch2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 5 | W1C | 0x0 | frame1_dma_end_scl_ch1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 4 | W1C | 0x0 | frame0_dma_end_scl_ch1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 3 | W1C | 0x0 | frame1_dma_end_scl_ch0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | W1C | 0x0 | frame0_dma_end_scl_ch0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 1 | W1C | 0x0 | axi1_bus_err_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 0 | W1C | 0x0 | axi0_bus_err_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |

**VICAP_DVP_CTRL**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:18 | RW | 0x0 | sw_soft_rst_mode<br>2'b00: Soft reset and protect toisp path frame integrity;<br>2'b01: Soft reset and protect toisp path frame integrity and pull down sw_cap_en automatically;<br>2'b10: Soft reset directly;<br>2'b11: Reserved. |
| 17 | RW | 0x0 | sw_soft_rst<br>1'b0: Not reset<br>1'b1: Reset the VICAP DVP path(except MMU/AXI MASTER/REG FILE) |
| 16 | RW | 0x0 | sw_dma_rst<br>Write 1 will reset VICAP DVP path dma.<br>When this bit change to 0,dma is reseted completely. |
| 15:13 | RW | 0x0 | sw_press_value<br>Press value. |
| 12 | RW | 0x0 | sw_press_en<br>1'b0: Disable<br>1'b1: Enable |
| 11:9 | RW | 0x0 | sw_hurry_value<br>Hurry value. |
| 8 | RW | 0x0 | sw_hurry_en<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RO | 0x0 | reserved |
| 6:5 | RW | 0x0 | sw_water_line<br>2'b00: 75%<br>2'b01: 50%<br>2'b10: 25%<br>2'b11: 0% |
| 4:2 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | sw_dma_en<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | sw_cap_en<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_DVP_INTEN**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |
| 25 | RW | 0x0 | size_err_id3_inten<br>1'b0: Disable<br>1'b1: Enable |
| 24 | RW | 0x0 | size_err_id2_inten<br>1'b0: Disable<br>1'b1: Enable |
| 23 | RW | 0x0 | size_err_id1_inten<br>1'b0: Disable<br>1'b1: Enable |
| 22 | RW | 0x0 | size_err_id0_inten<br>1'b0: Disable<br>1'b1: Enable |
| 21 | RW | 0x0 | line_id3_inten<br>1'b0: Disable<br>1'b1: Enable |
| 20 | RW | 0x0 | line_id2_inten<br>1'b0: Disable<br>1'b1: Enable |
| 19 | RW | 0x0 | line_id1_inten<br>1'b0: Disable<br>1'b1: Enable |
| 18 | RW | 0x0 | line_id0_inten<br>1'b0: Disable<br>1'b1: Enable |
| 17 | RW | 0x0 | bandwidth_lack_inten<br>Enable the interrupt of bandwidth lack.<br>1'b0: Disable<br>1'b1: Enable |
| 16 | RW | 0x0 | dma_fifo_overflow_inten<br>Enable the interrupt of dma fifo overflow .<br>1'b0: Disable<br>1'b1: Enable |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15 | RW | 0x0 | frame1_dma_end_id3_inten<br>Enable the interrupt of end of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | frame0_dma_end_id3_inten<br>Enable the interrupt of end of even frame for ID3.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | frame1_dma_end_id2_inten<br>Enable the interrupt of end of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | frame0_dma_end_id2_inten<br>Enable the interrupt of end of even frame for ID2.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | frame1_dma_end_id1_inten<br>Enable the interrupt of end of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | frame0_dma_end_id1_inten<br>Enable the interrupt of end of even frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | frame1_dma_end_id0_inten<br>Enable the interrupt of end of odd frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | frame0_dma_end_id0_inten<br>Enable the interrupt of end of even frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | frame1_start_id3_inten<br>Enable the interrupt of start of odd frame for ID3.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | frame0_start_id3_inten<br>Enable the interrupt of start of even frame for ID3.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | frame1_start_id2_inten<br>Enable the interrupt of start of odd frame for ID2.<br>1'b0: Disable<br>1'b1: Enable |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | RW | 0x0 | frame0_start_id2_inten<br>Enable the interrupt of start of even frame for ID2.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | frame1_start_id1_inten<br>Enable the interrupt of start of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | frame0_start_id1_inten<br>Enable the interrupt of start of even frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | frame1_start_id0_inten<br>Enable the interrupt of start of odd frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | frame0_start_id0_inten<br>Enable the interrupt of start of even frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_DVP_INTSTAT**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:26 | RO | 0x00 | reserved |
| 25 | W1C | 0x0 | size_err_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 24 | W1C | 0x0 | size_err_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 23 | W1C | 0x0 | size_err_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 22 | W1C | 0x0 | size_err_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 21 | W1C | 0x0 | line_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 20 | W1C | 0x0 | line_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19 | W1C | 0x0 | line_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 18 | W1C | 0x0 | line_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 17 | W1C | 0x0 | bandwidth_lack_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 16 | W1C | 0x0 | dma_fifo_overflow_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 15 | W1C | 0x0 | frame1_dma_end_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 14 | W1C | 0x0 | frame0_dma_end_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 13 | W1C | 0x0 | frame1_dma_end_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 12 | W1C | 0x0 | frame0_dma_end_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 11 | W1C | 0x0 | frame1_dma_end_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 10 | W1C | 0x0 | frame0_dma_end_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 9 | W1C | 0x0 | frame1_dma_end_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 8 | W1C | 0x0 | frame0_dma_end_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 7 | W1C | 0x0 | frame1_start_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 6 | W1C | 0x0 | frame0_start_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 5 | W1C | 0x0 | frame1_start_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 4 | W1C | 0x0 | frame0_start_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 3 | W1C | 0x0 | frame1_start_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 2 | W1C | 0x0 | frame0_start_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 1 | W1C | 0x0 | frame1_start_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 0 | W1C | 0x0 | frame0_start_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |

**VICAP_DVP_FORMAT**

Address: Operational Base + offset (0x001C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_multi_id_mode<br>2'd0: 1to1 (ID0 will work)<br>2'd1: 1to2 (ID0/ID1 will work)<br>2'd2: 1to4 (ID0/ID1/ID2/ID3 will work)<br>2'd3: Reserved |
| 29 | RW | 0x0 | sw_multi_id_sel<br>Only for BT1120.<br>1'b0: Parse the id by data[11:8]<br>1'b1: Parse the id by data[3:0] |
| 28 | RW | 0x0 | sw_multi_id_en<br>1'b0: Disable multi-ID bt656/bt1120 received<br>1'b1: Enable multi-ID bt656/bt1120 received |
| 27:22 | RO | 0x00 | reserved |
| 21 | RW | 0x0 | sw_align<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: Hign alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 20:19 | RW | 0x0 | sw_yuv_out_order<br>2'b00: UYVY<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 18:16 | RW | 0x0 | sw_wrddr_type<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 15:14 | RO | 0x0 | reserved |
| 13 | RW | 0x0 | sw_only_sav_mode<br>1'b0: Detect SAV and EAV<br>1'b1: Only detect SAV |
| 12 | RW | 0x0 | sw_yc_swap<br>1'b0: No swap for y and c<br>1'b1: Swap for y and c<br>Only for BT1120 mode. |
| 11 | RW | 0x0 | sw_dualedge_en<br>1'b0: Only use single edge of clock<br>1'b1: Use double edges of clock<br>Only for BT1120 mode. |
| 10 | RW | 0x0 | sw_field_order<br>1'b0: Odd field first<br>1'b1: Even field first. |
| 9 | RW | 0x0 | sw_interlace_en<br>1'b0: Progress<br>1'b1: Interlace |
| 8:7 | RW | 0x0 | sw_raw_width<br>2'b00: 8bit raw data<br>2'b01: 10bit raw data<br>2'b10: 12bit raw data<br>2'b11: Reserved |
| 6:5 | RW | 0x0 | sw_yuv_in_order<br>2'b00: UYVY<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 4:2 | RW | 0x0 | sw_input_mode<br>3'b000: BT601 YUV422<br>3'b001: BT601 RAW<br>3'b010: BT656 YUV422<br>3'b011: BT1120 YUV422<br>3'b100: SONY RAW<br>Others: Reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | sw_href_pol<br>1'b0: High active<br>1'b1: Low active |
| 0 | RW | 0x0 | sw_vsync_pol<br>1'b0: Low active<br>1'b1: High active |

**VICAP_DVP_MULTI_ID**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RW | 0x0 | sw_chid_bit_en_id3<br>Bit enable for chid_id3.<br>Eg: chid_id3 = 4'b1111 and chid_bit_en_id3 = 4'b0011.Then the data[3:0] = 4'bxx11 will be detected. |
| 27:24 | RW | 0x0 | sw_chid_id3<br>The channel id for id3. |
| 23:20 | RW | 0x0 | sw_chid_bit_en_id2<br>Bit enable for chid_id2.<br>Eg: chid_id2 = 4'b1111 and chid_bit_en_id2 = 4'b0011.Then the data[3:0] = 4'bxx11 will be detected. |
| 19:16 | RW | 0x0 | sw_chid_id2<br>The channel id for id2. |
| 15:12 | RW | 0x0 | sw_chid_bit_en_id1<br>Bit enable for chid_id1.<br>Eg: chid_id1 = 4'b1111 and chid_bit_en_id1 = 4'b0011.Then the data[3:0] = 4'bxx11 will be detected. |
| 11:8 | RW | 0x0 | sw_chid_id1<br>The channel id for id1. |
| 7:4 | RW | 0x0 | sw_chid_bit_en_id0<br>Bit enable for chid_id0.<br>Eg: chid_id0 = 4'b1111 and chid_bit_en_id0 = 4'b0011.Then the data[3:0] = 4'bxx11 will be detected. |
| 3:0 | RW | 0x0 | sw_chid_id0<br>The channel id for id0. |

**VICAP_DVP_SAV_EAV**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RW | 0xf | sw_eav_blk1<br>EAV for even field blank. |
| 27:24 | RW | 0xe | sw_sav_blk1<br>SAV for even field blank. |
| 23:20 | RW | 0xd | sw_eav_act1<br>EAV for even field active. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19:16 | RW | 0xc | sw_sav_act1<br>SAV for even field active. |
| 15:12 | RW | 0xb | sw_eav_blk0<br>EAV for odd field blank. |
| 11:8 | RW | 0xa | sw_sav_blk0<br>SAV for odd field blank. |
| 7:4 | RW | 0x9 | sw_eav_act0<br>EAV for odd field active. |
| 3:0 | RW | 0x8 | sw_sav_act0<br>SAV for odd field active. |

**VICAP_DVP_CROP_SIZE**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:16 | RW | 0x01e0 | sw_height<br>The expected height of received image. |
| 15:13 | RO | 0x0 | reserved |
| 12:0 | RW | 0x02d0 | sw_width<br>The expected width of received image. |

**VICAP_DVP_CROP_START**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:16 | RW | 0x0000 | sw_start_y<br>The vertical ordinate of the start point. |
| 15:13 | RO | 0x0 | reserved |
| 12:0 | RW | 0x0000 | sw_start_x<br>The horizontal ordinate of the start point. |

**VICAP_DVP_FRM0_ADDR_Y_ID0**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id0<br>DVP path frame0 y address. |

**VICAP_DVP_FRM0_ADDR_UV_ID0**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id0<br>DVP path frame0 uv address. |

**VICAP_DVP_FRM1_ADDR_Y_ID0**

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id1<br>DVP path frame1 y address. |

**VICAP_DVP_FRM1_ADDR_UV_ID0**

Address: Operational Base + offset (0x003C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id0<br>DVP path frame1 uv address. |

**VICAP_DVP_FRM0_ADDR_Y_ID1**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id1<br>DVP path frame0 y address for id1. |

**VICAP_DVP_FRM0_ADDR_UV_ID1**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id1<br>DVP path frame0 uv address for id1. |

**VICAP_DVP_FRM1_ADDR_Y_ID1**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id1<br>DVP path frame1 y address for id1. |

**VICAP_DVP_FRM1_ADDR_UV_ID1**

Address: Operational Base + offset (0x004C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id1<br>DVP path frame1 uv address for id1. |

**VICAP_DVP_FRM0_ADDR_Y_ID2**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id2<br>DVP path frame0 y address for id2. |

**VICAP_DVP_FRM0_ADDR_UV_ID2**

Address: Operational Base + offset (0x0054)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id2<br>DVP path frame0 uv address for id2. |

**VICAP_DVP_FRM1_ADDR_Y_ID2**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id2<br>DVP path frame1 y address for id2. |

**VICAP_DVP_FRM1_ADDR_UV_ID2**

Address: Operational Base + offset (0x005C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id2<br>DVP path frame1 uv address for id2. |

**VICAP_DVP_FRM0_ADDR_Y_ID3**

Address: Operational Base + offset (0x0060)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id3<br>DVP path frame0 y address for id3. |

**VICAP_DVP_FRM0_ADDR_UV_ID3**

Address: Operational Base + offset (0x0064)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id3<br>DVP path frame0 uv address for id3. |

**VICAP_DVP_FRM1_ADDR_Y_ID3**

Address: Operational Base + offset (0x0068)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id3<br>DVP path frame1 y address for id3. |

**VICAP_DVP_FRM1_ADDR_UV_ID3**

Address: Operational Base + offset (0x006C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id3<br>DVP path frame1 uv address for id3. |

**VICAP_DVP_VIR_LINE_WIDTH**

Address: Operational Base + offset (0x0070)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19:0 | RW | 0x00000 | vir_line_width<br>DVP path virtual line width. |

**VICAP_DVP_LINE_INT_NUM_ID0_1**

Address: Operational Base + offset (0x0074)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | line_int_mode_id1<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 30:29 | RO | 0x0 | reserved |
| 28:16 | RW | 0x0040 | sw_line_int_num_id1<br>For one-time mode, if line_int_num_id1=100, then channel 1 receive 100th line,the line_id1_intst will be 1.<br>For circular mode, if line_int_num_id1=100, then channel 1 receive 100th line200th line300th line.....the line_id1_intst will be 1. |
| 15 | RW | 0x0 | line_int_mode_id0<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 14:13 | RO | 0x0 | reserved |
| 12:0 | RW | 0x0040 | sw_line_int_num_id0<br>For one-time mode, if line_int_num_id0=100, then channel 0 receive 100th line, the line_id0_intst will be 1.<br>For circular mode, if line_int_num_id0=100, then channel 0 receive 100th line200th line300th line.....the line_id0_intst will be 1. |

**VICAP_DVP_LINE_INT_NUM_ID2_3**

Address: Operational Base + offset (0x0078)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | line_int_mode_id3<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 30:29 | RO | 0x0 | reserved |
| 28:16 | RW | 0x0040 | sw_line_int_num_id3<br>For one-time mode, if line_int_num_id3=100, then channel 3 receive 100th line,the line_id3_intst will be 1.<br>For circular mode, if line_int_num_id3=100, then channel 3 receive 100th line200th line300th line.....the line_id3_intst will be 1. |
| 15 | RW | 0x0 | line_int_mode_id2<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 14:13 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12:0 | RW | 0x0040 | sw_line_int_num_id2<br>For one-time mode, if line_int_num_id2=100,then channel 2 receive 100th line, the line_id2_intst will be 1.<br>For circular mode, if line_int_num_id2=100, then channel 2 receive 100th line200th line300th line.....the line_id2_intst will be 1. |

**VICAP_DVP_LINE_CNT_ID0_1**

Address: Operational Base + offset (0x007C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_cnt_id1<br>Current line count. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_line_cnt_id0<br>Current line count. |

**VICAP_DVP_LINE_CNT_ID2_3**

Address: Operational Base + offset (0x0080)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_cnt_id3<br>Current line count. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_line_cnt_id2<br>Current line count. |

**VICAP_DVP_PIX_NUM_ID0**

Address: Operational Base + offset (0x0084)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_uv_pix_num_id0<br>The id0 UV pixel number in one line. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_y_pix_num_id0<br>The id0 Y pixel number in one line. |

**VICAP_DVP_LINE_NUM_ID0**

Address: Operational Base + offset (0x0088)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_uv_line_num_id0<br>The id0 UV line number in one frame. |
| 15:14 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:0 | RO | 0x0000 | ro_y_line_num_id0<br>The id0 Y line number in one frame. |

**VICAP_DVP_PIX_NUM_ID1**

Address: Operational Base + offset (0x008C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_uv_pix_num_id1<br>The id1 UV pixel number in one line. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_y_pix_num_id1<br>The id1 Y pixel number in one line. |

**VICAP_DVP_LINE_NUM_ID1**

Address: Operational Base + offset (0x0090)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_uv_line_num_id1<br>The id1 UV line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_y_line_num_id1<br>The id1 Y line number in one frame. |

**VICAP_DVP_PIX_NUM_ID2**

Address: Operational Base + offset (0x0094)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_uv_pix_num_id2<br>The id2 UV pixel number in one line. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_y_pix_num_id2<br>The id2 Y pixel number in one line. |

**VICAP_DVP_LINE_NUM_ID2**

Address: Operational Base + offset (0x0098)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_uv_line_num_id2<br>The id2 UV line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_y_line_num_id2<br>The id2 Y line number in one frame. |

**VICAP_DVP_PIX_NUM_ID3**

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

Address: Operational Base + offset (0x009C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_uv_pix_num_id3<br>The id3 UV pixel number in one line. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_y_pix_num_id3<br>The id3 Y pixel number in one line. |

**VICAP_DVP_LINE_NUM_ID3**

Address: Operational Base + offset (0x00A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_uv_line_num_id3<br>The id3 UV line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_y_line_num_id3<br>The id3 Y line number in one frame. |

**VICAP_DVP_SYNC_HEADER**

Address: Operational Base + offset (0x00A4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | ro_sync_header_7<br>Sync header 7. |
| 27:24 | RO | 0x0 | ro_sync_header_6<br>Sync header 6. |
| 23:20 | RO | 0x0 | ro_sync_header_5<br>Sync header 5. |
| 19:16 | RO | 0x0 | ro_sync_header_4<br>Sync header 4. |
| 15:12 | RO | 0x0 | ro_sync_header_3<br>Sync header 3. |
| 11:8 | RO | 0x0 | ro_sync_header_2<br>Sync header 2. |
| 7:4 | RO | 0x0 | ro_sync_header_1<br>Sync header 1. |
| 3:0 | RO | 0x0 | ro_sync_header_0<br>Sync header 0.<br>Header 0 is the latest, and header 7 is the earliest. |

**VICAP_MIPI0_ID0_CTRL0**

Address: Operational Base + offset (0x0100)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id0<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id0<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id0<br>Enable dma transport id0.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_align_id0<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when raw uncompacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id0<br>Select command mode for id0.<br>1'b0: Not command mode<br>1'b1: Command mode |
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id0<br>If sw_mipi0_on_hdr_mode_id0=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id0=1, id0 channel will capture the line which line count value equal to 1. |
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id0<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |
| 21:20 | RW | 0x0 | sw_hdr_mode_id0<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id0<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id0<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id0<br>Data type for id0. |
| 9:8 | RW | 0x0 | sw_vc_id0<br>Virtual channel for id0. |
| 7:5 | RW | 0x0 | sw_wrddr_type_id0<br>The write ddr type of id0.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id0<br>Enable to crop for id0.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RW | 0x0 | sw_parse_type_id0<br>The parse type of id0.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |
| 0 | RW | 0x0 | sw_cap_en_id0<br>Enable to capture id0.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI0_ID0_CTRL1**

Address: Operational Base + offset (0x0104)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_height_id0<br>Height for id0. |
| 15:14 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:0 | RW | 0x0000 | sw_width_id0<br>Width for id0. If sw_wrddr_type is rgb888, then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id0 is enable the width value must be 4 aligned. |

**VICAP_MIPI0_ID1_CTRL0**

Address: Operational Base + offset (0x0108)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id1<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id1<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id1<br>Enable dma transport id1.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_align_id1<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id1<br>Select command mode for id1.<br>1'b0: Not command mode<br>1'b1: Command mode |
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id1<br>If sw_mipi0_on_hdr_mode_id1=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id1=1, id1 channel will capture the line which line count value equal to 1. |
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id1<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |
| 21:20 | RW | 0x0 | sw_hdr_mode_id1<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id1<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id1<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id1<br>Data type for id1. |
| 9:8 | RW | 0x0 | sw_vc_id1<br>Virtual channel for id1. |
| 7:5 | RW | 0x0 | sw_wrddr_type_id1<br>The write ddr type of id1.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id1<br>Enable to crop for id1.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RW | 0x0 | sw_parse_type_id1<br>The parse type of id1.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |
| 0 | RW | 0x0 | sw_cap_en_id1<br>Enable to capture id1.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI0_ID1_CTRL1**

Address: Operational Base + offset (0x010C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 29:16 | RW | 0x0000 | sw_height_id1<br>Height for id1. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_width_id1<br>Width for id1.if sw_wrddr_type is rgb888,then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id1 is enable the width value must be 4 aligned. |

**VICAP_MIPI0_ID2_CTRL0**

Address: Operational Base + offset (0x0110)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id2<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id2<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id2<br>Enable dma transport id2.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_align_id2<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id2<br>Select command mode for id2.<br>1'b0: Not command mode<br>1'b1: Command mode |
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id2<br>If sw_mipi0_on_hdr_mode_id2=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id2=1, id2 channel will capture the line which line count value equal to 1. |
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id2<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 21:20 | RW | 0x0 | sw_hdr_mode_id2<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id2<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id2<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id2<br>Data type for id2. |
| 9:8 | RW | 0x0 | sw_vc_id2<br>Virtual channel for id2. |
| 7:5 | RW | 0x0 | sw_wrddr_type_id2<br>The write ddr type of id2.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id2<br>Enable to crop for id2.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RW | 0x0 | sw_parse_type_id2<br>The parse type of id2.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |
| 0 | RW | 0x0 | sw_cap_en_id2<br>Enable to capture id2.<br>1'b0: Disable<br>1'b1: Enable |

Copyright 2022 © Rockchip Electronics Co., Ltd.

**VICAP_MIPI0_ID2_CTRL1**

Address: Operational Base + offset (0x0114)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_height_id2<br>Height for id2. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_width_id2<br>Width for id2.if sw_wrddr_type is rgb888,then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id2 is enable the width value must be 4 aligned. |

**VICAP_MIPI0_ID3_CTRL0**

Address: Operational Base + offset (0x0118)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id3<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id3<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00.<br>And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id3<br>Enable dma transport id3.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_align_id3<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id3<br>Select command mode for id3.<br>1'b0: Not command mode<br>1'b1: Command mode |
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id3<br>If sw_mipi0_on_hdr_mode_id3=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id3=1, id3 channel will capture the line which line count value equal to 1. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id3<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |
| 21:20 | RW | 0x0 | sw_hdr_mode_id3<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id3<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id3<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id3<br>Data type for id3. |
| 9:8 | RW | 0x0 | sw_vc_id3<br>Virtual channel for id3. |
| 7:5 | RW | 0x0 | sw_wrddr_type_id3<br>The write ddr type of id3.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id3<br>Enable to crop for id3.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RW | 0x0 | sw_parse_type_id3<br>The parse type of id3.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | sw_cap_en_id3<br>Enable to capture id3.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI0_ID3_CTRL1**

Address: Operational Base + offset (0x011C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_height_id3<br>Height for id3. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_width_id3<br>Width for id3.if sw_wrddr_type is rgb888,then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id3 is enable the width value must be 4 aligned. |

**VICAP_MIPI0_CTRL**

Address: Operational Base + offset (0x0120)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:18 | RW | 0x0 | sw_soft_rst_mode<br>2'b00: Soft reset and protect toisp path frame integrity<br>2'b01: Soft reset and protect toisp path frame integrity and pull down sw_cap_en automatically<br>2'b10: Soft reset directly<br>2'b11: Reserved |
| 17 | RW | 0x0 | sw_soft_rst<br>1'b0: Not reset<br>1'b1: Reset the VICAP MIPI0 path(except MMU/AXI MASTER/REG FILE) |
| 16 | RW | 0x0 | sw_dma_rst<br>Write 1 will reset VICAP MIPI0 path dma.<br>When this bit change to 0, dma is reseted completely. |
| 15:13 | RW | 0x0 | sw_press_value<br>Press value. |
| 12 | RW | 0x0 | sw_press_en<br>1'b0: Disable press<br>1'b1: Enable press |
| 11:8 | RO | 0x0 | reserved |
| 7:5 | RW | 0x0 | sw_hurry_value<br>Hurry value. |
| 4 | RW | 0x0 | sw_hurry_en<br>1'b0: Disable hurry<br>1'b1: Enable hurry |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RO | 0x0 | reserved |
| 2:1 | RW | 0x0 | sw_water_line<br>2'b00: 75%<br>2'b01: 50%<br>2'b10: 25%<br>2'b11: 0% |
| 0 | RW | 0x0 | sw_cap_en<br>1'b0: Disable capture all id<br>1'b1: Enable capture all id. |

**VICAP_MIPI0_FRAME0_ADDR_Y_ID0**

Address: Operational Base + offset (0x0124)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id0<br>First address of even frame for ID0 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI0_FRAME1_ADDR_Y_ID0**

Address: Operational Base + offset (0x0128)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id0<br>First address of odd frame for ID0 Y path(must be aligned to double word). |

**VICAP_MIPI0_FRAME0_ADDR_UV_ID0**

Address: Operational Base + offset (0x012C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id0<br>First address of even frame for ID0 UV path(must be aligned to double word). |

**VICAP_MIPI0_FRAME1_ADDR_UV_ID0**

Address: Operational Base + offset (0x0130)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id0<br>First address of odd frame for ID0 UV path(must be aligned to double word). |

**VICAP_MIPI0_VLW_ID0**

Address: Operational Base + offset (0x0134)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_id0<br>Virtual line width of even frame for ID0 path(must be aligned to double word). |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**VICAP_MIPI0_FRAME0_ADDR_Y_ID1**

Address: Operational Base + offset (0x0138)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id1<br>First address of even frame for ID1 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI0_FRAME1_ADDR_Y_ID1**

Address: Operational Base + offset (0x013C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id1<br>First address of odd frame for ID1 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI0_FRAME0_ADDR_UV_ID1**

Address: Operational Base + offset (0x0140)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id1<br>First address of even frame for ID1 UV path(must be aligned to double word). |

**VICAP_MIPI0_FRAME1_ADDR_UV_ID1**

Address: Operational Base + offset (0x0144)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id1<br>First address of odd frame for ID1 UV path(must be aligned to double word). |

**VICAP_MIPI0_VLW_ID1**

Address: Operational Base + offset (0x0148)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_id1<br>Virtual line width of even frame for ID1 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI0_FRAME0_ADDR_Y_ID2**

Address: Operational Base + offset (0x014C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id2<br>First address of even frame for ID2 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI0_FRAME1_ADDR_Y_ID2**

Address: Operational Base + offset (0x0150)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id2<br>First address of odd frame for ID2 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI0_FRAME0_ADDR_UV_ID2**

Address: Operational Base + offset (0x0154)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id2<br>First address of even frame for ID2 UV path(must be aligned to double word). |

**VICAP_MIPI0_FRAME1_ADDR_UV_ID2**

Address: Operational Base + offset (0x0158)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id0<br>First address of odd frame for ID2 UV path(must be aligned to double word). |

**VICAP_MIPI0_VLW_ID2**

Address: Operational Base + offset (0x015C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_id2<br>Virtual line width of even frame for ID2 path(must be aligned to double word). |

**VICAP_MIPI0_FRAME0_ADDR_Y_ID3**

Address: Operational Base + offset (0x0160)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id3<br>First address of even frame for ID3 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI0_FRAME1_ADDR_Y_ID3**

Address: Operational Base + offset (0x0164)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id3<br>First address of odd frame for ID3 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI0_FRAME0_ADDR_UV_ID3**

Address: Operational Base + offset (0x0168)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id3<br>First address of even frame for ID3 UV path(must be aligned to double word). |

**VICAP_MIPI0_FRAME1_ADDR_UV_ID3**

Address: Operational Base + offset (0x016C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id3<br>First address of odd frame for ID3 UV path(must be aligned to double word). |

**VICAP_MIPI0_VLW_ID3**

Address: Operational Base + offset (0x0170)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_id3<br>Virtual line width of even frame for ID3 path(must be aligned to double word). |

**VICAP_MIPI0_INTEN**

Address: Operational Base + offset (0x0174)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27 | RW | 0x0 | size_err_id3_inten<br>1'b0: Disable<br>1'b1: Enable |
| 26 | RW | 0x0 | size_err_id2_inten<br>1'b0: Disable<br>1'b1: Enable |
| 25 | RW | 0x0 | size_err_id1_inten<br>1'b0: Disable<br>1'b1: Enable |
| 24 | RW | 0x0 | size_err_id0_inten<br>1'b0: Disable<br>1'b1: Enable |
| 23 | RW | 0x0 | line_id3_inten<br>1'b0: Disable<br>1'b1: Enable |
| 22 | RW | 0x0 | line_id2_inten<br>1'b0: Disable<br>1'b1: Enable |
| 21 | RW | 0x0 | line_id1_inten<br>1'b0: Disable<br>1'b1: Enable |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 20 | RW | 0x0 | line_id0_inten<br>1'b0: Disable<br>1'b1: Enable |
| 19 | RW | 0x0 | csi2rx_fifo_overflow_inten<br>1'b0: Disable<br>1'b1: Enable |
| 18 | RW | 0x0 | bandwidth_lack_inten<br>1'b0: Disable<br>1'b1: Enable |
| 17 | RW | 0x0 | dma_uv_fifo_overflow_inten<br>Enable the interrupt of dma fifo overflow of MIPI uv path or LVDS id1 path.<br>1'b0: Disable<br>1'b1: Enable |
| 16 | RW | 0x0 | dma_y_fifo_overflow_inten<br>Enable the interrupt of dma fifo overflow of MIPI y path or LVDS id0 path.<br>1'b0: Disable<br>1'b1: Enable |
| 15 | RW | 0x0 | frame1_dma_end_id3_inten<br>Enable the interrupt of end of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | frame0_dma_end_id3_inten<br>Enable the interrupt of end of even frame for ID3.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | frame1_dma_end_id2_inten<br>Enable the interrupt of end of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | frame0_dma_end_id2_inten<br>Enable the interrupt of end of even frame for ID2.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | frame1_dma_end_id1_inten<br>Enable the interrupt of end of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | frame0_dma_end_id1_inten<br>Enable the interrupt of end of even frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RW | 0x0 | frame1_dma_end_id0_inten<br>Enable the interrupt of end of odd frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | frame0_dma_end_id0_inten<br>Enable the interrupt of end of even frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | frame1_start_id3_inten<br>Enable the interrupt of start of odd frame for ID3.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | frame0_start_id3_inten<br>Enable the interrupt of start of even frame for ID3.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | frame1_start_id2_inten<br>Enable the interrupt of start of odd frame for ID2.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | frame0_start_id2_inten<br>Enable the interrupt of start of even frame for ID2.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | frame1_start_id1_inten<br>Enable the interrupt of start of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | frame0_start_id1_inten<br>Enable the interrupt of start of even frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | frame1_start_id0_inten<br>Enable the interrupt of start of odd frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | frame0_start_id0_inten<br>Enable the interrupt of start of even frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI0_INTSTAT**

Address: Operational Base + offset (0x0178)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 27 | W1C | 0x0 | size_err_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 26 | W1C | 0x0 | size_err_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 25 | W1C | 0x0 | size_err_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 24 | W1C | 0x0 | size_err_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 23 | W1C | 0x0 | line_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 22 | W1C | 0x0 | line_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 21 | W1C | 0x0 | line_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 20 | W1C | 0x0 | line_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 19 | W1C | 0x0 | csi2rx_fifo_overflow_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 18 | W1C | 0x0 | bandwidth_lack_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 17 | W1C | 0x0 | dma_uv_fifo_overflow_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 16 | W1C | 0x0 | dma_y_fifo_overflow_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 15 | W1C | 0x0 | frame1_dma_end_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 14 | W1C | 0x0 | frame0_dma_end_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 13 | W1C | 0x0 | frame1_dma_end_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | W1C | 0x0 | frame0_dma_end_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 11 | W1C | 0x0 | frame1_dma_end_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 10 | W1C | 0x0 | frame0_dma_end_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 9 | W1C | 0x0 | frame1_dma_end_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 8 | W1C | 0x0 | frame0_dma_end_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 7 | W1C | 0x0 | frame1_start_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 6 | W1C | 0x0 | frame0_start_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 5 | W1C | 0x0 | frame1_start_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 4 | W1C | 0x0 | frame0_start_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 3 | W1C | 0x0 | frame1_start_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 2 | W1C | 0x0 | frame0_start_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 1 | W1C | 0x0 | frame1_start_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 0 | W1C | 0x0 | frame0_start_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |

**VICAP_MIPI0_LINE_INT_NUM_ID0_1**

Address: Operational Base + offset (0x017C)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | line_int_mode_id1<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0040 | line_int_num_id1<br>For one-time mode, if line_int_num_id1=100, then channel 1 receive 100th line,the line_id1_intst will be 1.<br>For circular mode, if line_int_num_id1=100, then channel 1 receive 100th line200th line300th line.....the line_id1_intst will be 1. |
| 15 | RW | 0x0 | line_int_mode_id0<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0040 | line_int_num_id0<br>For one-time mode, if line_int_num_id0=100, then channel 0 receive 100th line,  the line_id0_intst will be 1.<br>For circular mode, if line_int_num_id0=100, then channel 0 receive 100th line200th line300th line.....the line_id0_intst will be 1. |

**VICAP_MIPI0_LINE_INT_NUM_ID2_3**

Address: Operational Base + offset (0x0180)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | line_int_mode_id3<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0040 | line_int_num_id3<br>For one-time mode, if line_int_num_id3=100, then channel 3 receive 100th line, the line_id3_intst will be 1.<br>For circular mode, if line_int_num_id3=100, then channel 3 receive 100th line200th line300th line.....the line_id3_intst will be 1. |
| 15 | RW | 0x0 | line_int_mode_id2<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0040 | line_int_num_id2<br>For one-time mode, if line_int_num_id2=100, then channel 2 receive 100th line,the line_id2_intst will be 1.<br>For circular mode, if line_int_num_id2=100, then channel 2 receive 100th line200th line300th line.....the line_id2_intst will be 1. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

**VICAP_MIPI0_LINE_CNT_ID0_1**

Address: Operational Base + offset (0x0184)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_cnt_id1<br>Current line count for id1. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_line_cnt_id0<br>Current line count for id0. |

**VICAP_MIPI0_LINE_CNT_ID2_3**

Address: Operational Base + offset (0x0188)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_cnt_id3<br>Current line count for id3. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_line_cnt_id2<br>Current line count for id2. |

**VICAP_MIPI0_ID0_CROP_START**

Address: Operational Base + offset (0x018C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id0<br>The start y coordinate for id0. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id0<br>The start x coordinate for id0, if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI0_ID1_CROP_START**

Address: Operational Base + offset (0x0190)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id1<br>The start y coordinate for id1. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id1<br>The start x coordinate for id1,if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI0_ID2_CROP_START**

Address: Operational Base + offset (0x0194)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id2<br>The start y coordinate for id2. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id2<br>The start x coordinate for id2, if sw_wrddr_type is rgb888,then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI0_ID3_CROP_START**

Address: Operational Base + offset (0x0198)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id3<br>The start y coordinate for id3. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id3<br>The start x coordinate for id3, if sw_wrddr_type is rgb888,then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI0_FRAME_NUM_VC0**

Address: Operational Base + offset (0x019C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc0<br>The frame number of frame end of virtual channel 0. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc0<br>The frame number of frame start of virtual channel 0. |

**VICAP_MIPI0_FRAME_NUM_VC1**

Address: Operational Base + offset (0x01A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc1<br>The frame number of frame end of virtual channel 1. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc1<br>The frame number of frame start of virtual channel 1. |

**VICAP_MIPI0_FRAME_NUM_VC2**

Address: Operational Base + offset (0x01A4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc2<br>The frame number of frame end of virtual channel 2. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc2<br>The frame number of frame start of virtual channel 2. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**VICAP_MIPI0_FRAME_NUM_VC3**

Address: Operational Base + offset (0x01A8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc3<br>The frame number of frame end of virtual channel 3. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc3<br>The frame number of frame start of virtual channel 3. |

**VICAP_MIPI0_ID0_EFFECT_CODE**

Address: Operational Base + offset (0x01AC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id0<br>Effect code of id0 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id0<br>Effect code of id0 for sony sensor. |

**VICAP_MIPI0_ID1_EFFECT_CODE**

Address: Operational Base + offset (0x01B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id1<br>Effect code of id1 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id1<br>Effect code of id1 for sony sensor. |

**VICAP_MIPI0_ID2_EFFECT_CODE**

Address: Operational Base + offset (0x01B4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id2<br>Effect code of id2 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id2<br>Effect code of id2 for sony sensor. |

**VICAP_MIPI0_ID3_EFFECT_CODE**

Address: Operational Base + offset (0x01B8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id3<br>Effect code of id3 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id3<br>Effect code of id3 for sony sensor. |

**VICAP_MIPI0_ON_PAD_VALUE**

Address: Operational Base + offset (0x01BC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RO | 0x00000 | reserved |
| 13:0 | RW | 0x0000 | sw_on_pad_value<br>Padding value for ON sensor. |

**VICAP_MIPI0_SIZE_NUM_ID0**

Address: Operational Base + offset (0x01C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_num_id0<br>The id0 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id0<br>The id0 pixel number in one line. |

**VICAP_MIPI0_SIZE_NUM_ID1**

Address: Operational Base + offset (0x01C4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_num_id1<br>The id1 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id1<br>The id1 pixel number in one line. |

**VICAP_MIPI0_SIZE_NUM_ID2**

Address: Operational Base + offset (0x01C8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_num_id2<br>The id2 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id2<br>The id2 pixel number in one line. |

**VICAP_MIPI0_SIZE_NUM_ID3**

Address: Operational Base + offset (0x01CC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 29:16 | RO | 0x0000 | ro_line_num_id3<br>The id3 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id3<br>The id3 pixel number in one line. |

**VICAP_MIPI1_ID0_CTRL0**

Address: Operational Base + offset (0x0200)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id0<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id0<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id0<br>Enable dma transport id0.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_align_id0<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id0<br>Select command mode for id0.<br>1'b0: Not command mode<br>1'b1: Command mode |
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id0<br>If sw_mipi0_on_hdr_mode_id0=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id0=1, id0 channel will capture the line which line count value equal to 1. |
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id0<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 21:20 | RW | 0x0 | sw_hdr_mode_id0<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id0<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id0<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id0<br>Data type for id0. |
| 9:8 | RW | 0x0 | sw_vc_id0<br>Virtual channel for id0. |
| 7:5 | RW | 0x0 | sw_wrddr_type_id0<br>The write ddr type of id0.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id0<br>Enable to crop for id0.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RW | 0x0 | sw_parse_type_id0<br>The parse type of id0.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |
| 0 | RW | 0x0 | sw_cap_en_id0<br>Enable to capture id0.<br>1'b0: Disable<br>1'b1: Enable |

Copyright 2022 © Rockchip Electronics Co., Ltd.

**VICAP_MIPI1_ID0_CTRL1**

Address: Operational Base + offset (0x0204)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_height_id0<br>Height for id0. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_width_id0<br>Width for id0. If sw_wrddr_type is rgb888, then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id0 is enable the width value must be 4 aligned. |

**VICAP_MIPI1_ID1_CTRL0**

Address: Operational Base + offset (0x0208)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id1<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id1<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id1<br>Enable dma transport id1.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_align_id1<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id1<br>Select command mode for id1.<br>1'b0: Not command mode<br>1'b1: Command mode |
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id1<br>If sw_mipi0_on_hdr_mode_id1=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id1=1, id1 channel will capture the line which line count value equal to 1. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id1<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |
| 21:20 | RW | 0x0 | sw_hdr_mode_id1<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id1<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id1<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id1<br>Data type for id1. |
| 9:8 | RW | 0x0 | sw_vc_id1<br>Virtual channel for id1. |
| 7:5 | RW | 0x0 | sw_wrddr_type_id1<br>The write ddr type of id1.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id1<br>Enable to crop for id1.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RW | 0x0 | sw_parse_type_id1<br>The parse type of id1.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | sw_cap_en_id1<br>Enable to capture id1.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI1_ID1_CTRL1**

Address: Operational Base + offset (0x020C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_height_id1<br>Height for id1. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_width_id1<br>Width for id1. If sw_wrddr_type is rgb888, then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id1 is enable the width value must be 4 aligned. |

**VICAP_MIPI1_ID2_CTRL0**

Address: Operational Base + offset (0x0210)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id2<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id2<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00.<br>And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id2<br>Enable dma transport id2.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_align_id2<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id2<br>Select command mode for id2.<br>1'b0: Not command mode<br>1'b1: Command mode |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id2<br>If sw_mipi0_on_hdr_mode_id2=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id2=1, id2 channel will capture the line which line count value equal to 1. |
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id2<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |
| 21:20 | RW | 0x0 | sw_hdr_mode_id2<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id2<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id2<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id2<br>Data type for id2. |
| 9:8 | RW | 0x0 | sw_vc_id2<br>Virtual channel for id2. |
| 7:5 | RW | 0x0 | sw_wrddr_type_id2<br>The write ddr type of id2.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id2<br>Enable to crop for id2.<br>1'b0: Disable<br>1'b1: Enable |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:1 | RW | 0x0 | sw_parse_type_id2<br>The parse type of id2.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |
| 0 | RW | 0x0 | sw_cap_en_id2<br>Enable to capture id2.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI1_ID2_CTRL1**

Address: Operational Base + offset (0x0214)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_height_id2<br>Height for id2. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_width_id2<br>Width for id2. If sw_wrddr_type is rgb888, then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id2 is enable the width value must be 4 aligned. |

**VICAP_MIPI1_ID3_CTRL0**

Address: Operational Base + offset (0x0218)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id3<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id3<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00.<br>And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id3<br>Enable dma transport id3.<br>1'b0: Disable<br>1'b1: Enable |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 27 | RW | 0x0 | sw_align_id3<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id3<br>Select command mode for id3.<br>1'b0: Not command mode<br>1'b1: Command mode |
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id3<br>If sw_mipi0_on_hdr_mode_id3=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id3=1, id3 channel will capture the line which line count value equal to 1. |
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id3<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |
| 21:20 | RW | 0x0 | sw_hdr_mode_id3<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id3<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id3<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id3<br>Data type for id3. |
| 9:8 | RW | 0x0 | sw_vc_id3<br>Virtual channel for id3. |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:5 | RW | 0x0 | sw_wrddr_type_id3<br>The write ddr type of id3.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id3<br>Enable to crop for id3.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RW | 0x0 | sw_parse_type_id3<br>The parse type of id3.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |
| 0 | RW | 0x0 | sw_cap_en_id3<br>Enable to capture id3.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI1_ID3_CTRL1**

Address: Operational Base + offset (0x021C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_height_id3<br>Height for id3. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_width_id3<br>Width for id3. If sw_wrddr_type is rgb888, then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id3 is enable the width value must be 4 aligned. |

**VICAP_MIPI1_CTRL**

Address: Operational Base + offset (0x0220)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19:18 | RW | 0x0 | sw_soft_rst_mode<br>2'b00: Soft reset and protect toisp path frame integrity;<br>2'b01: Soft reset and protect toisp path frame integrity and pull down sw_cap_en automatically;<br>2'b10: Soft reset directly;<br>2'b11: Reserved. |
| 17 | RW | 0x0 | sw_soft_rst<br>1'b0: Not reset<br>1'b1: Reset the VICAP MIPI1 path(except MMU/AXI MASTER/REG FILE) |
| 16 | RW | 0x0 | sw_dma_rst<br>Write 1 will reset VICAP MIPI1 path dma.<br>When this bit change to 0,dma is reseted completely. |
| 15:13 | RW | 0x0 | sw_press_value<br>Press value. |
| 12 | RW | 0x0 | sw_press_en<br>1'b0: Disable press<br>1'b1: Enable press |
| 11:8 | RO | 0x0 | reserved |
| 7:5 | RW | 0x0 | sw_hurry_value<br>Hurry value. |
| 4 | RW | 0x0 | sw_hurry_en<br>1'b0: Disable hurry<br>1'b1: Enable hurry |
| 3 | RO | 0x0 | reserved |
| 2:1 | RW | 0x0 | sw_water_line<br>2'b00: 75%<br>2'b01: 50%<br>2'b10: 25%<br>2'b11: 0% |
| 0 | RW | 0x0 | sw_cap_en<br>1'b0: Disable capture all id<br>1'b1: Enable capture all id. |

**VICAP_MIPI1_FRAME0_ADDR_Y_ID0**

Address: Operational Base + offset (0x0224)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id0<br>First address of even frame for ID0 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI1_FRAME1_ADDR_Y_ID0**

Address: Operational Base + offset (0x0228)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id0<br>First address of odd frame for ID0 Y path(must be aligned to double word). |

**VICAP_MIPI1_FRAME0_ADDR_UV_ID0**

Address: Operational Base + offset (0x022C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id0<br>First address of even frame for ID0 UV path(must be aligned to double word). |

**VICAP_MIPI1_FRAME1_ADDR_UV_ID0**

Address: Operational Base + offset (0x0230)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id0<br>First address of odd frame for ID0 UV path(must be aligned to double word). |

**VICAP_MIPI1_VLW_ID0**

Address: Operational Base + offset (0x0234)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_id0<br>Virtual line width of even frame for ID0 path(must be aligned to double word). |

**VICAP_MIPI1_FRAME0_ADDR_Y_ID1**

Address: Operational Base + offset (0x0238)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id1<br>First address of even frame for ID1 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI1_FRAME1_ADDR_Y_ID1**

Address: Operational Base + offset (0x023C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id1<br>First address of odd frame for ID1 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI1_FRAME0_ADDR_UV_ID1**

Address: Operational Base + offset (0x0240)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id1<br>First address of even frame for ID1 UV path(must be aligned to double word). |

**VICAP_MIPI1_FRAME1_ADDR_UV_ID1**

Address: Operational Base + offset (0x0244)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id1<br>First address of odd frame for ID1 UV path(must be aligned to double word). |

**VICAP_MIPI1_VLW_ID1**

Address: Operational Base + offset (0x0248)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_id1<br>Virtual line width of even frame for ID1 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI1_FRAME0_ADDR_Y_ID2**

Address: Operational Base + offset (0x024C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id2<br>First address of even frame for ID2 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI1_FRAME1_ADDR_Y_ID2**

Address: Operational Base + offset (0x0250)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id2<br>First address of odd frame for ID2 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI1_FRAME0_ADDR_UV_ID2**

Address: Operational Base + offset (0x0254)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id2<br>First address of even frame for ID2 UV path(must be aligned to double word). |

**VICAP_MIPI1_FRAME1_ADDR_UV_ID2**

Address: Operational Base + offset (0x0258)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id0<br>First address of odd frame for ID2 UV path(must be aligned to double word). |

**VICAP_MIPI1_VLW_ID2**

Address: Operational Base + offset (0x025C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_id2<br>Virtual line width of even frame for ID2 path(must be aligned to double word). |

**VICAP_MIPI1_FRAME0_ADDR_Y_ID3**

Address: Operational Base + offset (0x0260)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id3<br>First address of even frame for ID3 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI1_FRAME1_ADDR_Y_ID3**

Address: Operational Base + offset (0x0264)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id3<br>First address of odd frame for ID3 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI1_FRAME0_ADDR_UV_ID3**

Address: Operational Base + offset (0x0268)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id3<br>First address of even frame for ID3 UV path(must be aligned to double word). |

**VICAP_MIPI1_FRAME1_ADDR_UV_ID3**

Address: Operational Base + offset (0x026C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id3<br>First address of odd frame for ID3 UV path(must be aligned to double word). |

**VICAP_MIPI1_VLW_ID3**

Address: Operational Base + offset (0x0270)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19:0 | RW | 0x00000 | sw_vlw_id3<br>Virtual line width of even frame for ID3 path(must be aligned to double word). |

**VICAP_MIPI1_INTEN**

Address: Operational Base + offset (0x0274)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27 | RW | 0x0 | size_err_id3_inten<br>1'b0: Disable<br>1'b1: Enable |
| 26 | RW | 0x0 | size_err_id2_inten<br>1'b0: Disable<br>1'b1: Enable |
| 25 | RW | 0x0 | size_err_id1_inten<br>1'b0: Disable<br>1'b1: Enable |
| 24 | RW | 0x0 | size_err_id0_inten<br>1'b0: Disable<br>1'b1: Enable |
| 23 | RW | 0x0 | line_id3_inten<br>1'b0: Disable<br>1'b1: Enable |
| 22 | RW | 0x0 | line_id2_inten<br>1'b0: Disable<br>1'b1: Enable |
| 21 | RW | 0x0 | line_id1_inten<br>1'b0: Disable<br>1'b1: Enable |
| 20 | RW | 0x0 | line_id0_inten<br>1'b0: Disable<br>1'b1: Enable |
| 19 | RW | 0x0 | csi2rx_fifo_overflow_inten<br>1'b0: Disable<br>1'b1: Enable |
| 18 | RW | 0x0 | bandwidth_lack_inten<br>1'b0: Disable<br>1'b1: Enable |
| 17 | RW | 0x0 | dma_uv_fifo_overflow_inten<br>Enable the interrupt of dma fifo overflow of MIPI uv path or LVDS id1 path.<br>1'b0: Disable<br>1'b1: Enable |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 16 | RW | 0x0 | dma_y_fifo_overflow_inten<br>Enable the interrupt of dma fifo overflow of MIPI y path or LVDS id0 path.<br>1'b0: Disable<br>1'b1: Enable |
| 15 | RW | 0x0 | frame1_dma_end_id3_inten<br>Enable the interrupt of end of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | frame0_dma_end_id3_inten<br>Enable the interrupt of end of even frame for ID3.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | frame1_dma_end_id2_inten<br>Enable the interrupt of end of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | frame0_dma_end_id2_inten<br>Enable the interrupt of end of even frame for ID2.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | frame1_dma_end_id1_inten<br>Enable the interrupt of end of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | frame0_dma_end_id1_inten<br>Enable the interrupt of end of even frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | frame1_dma_end_id0_inten<br>Enable the interrupt of end of odd frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | frame0_dma_end_id0_inten<br>Enable the interrupt of end of even frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | frame1_start_id3_inten<br>Enable the interrupt of start of odd frame for ID3.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | frame0_start_id3_inten<br>Enable the interrupt of start of even frame for ID3.<br>1'b0: Disable<br>1'b1: Enable |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | frame1_start_id2_inten<br>Enable the interrupt of start of odd frame for ID2.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | frame0_start_id2_inten<br>Enable the interrupt of start of even frame for ID2.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | frame1_start_id1_inten<br>Enable the interrupt of start of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | frame0_start_id1_inten<br>Enable the interrupt of start of even frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | frame1_start_id0_inten<br>Enable the interrupt of start of odd frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | frame0_start_id0_inten<br>Enable the interrupt of start of even frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI1_INTSTAT**

Address: Operational Base + offset (0x0278)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27 | W1C | 0x0 | size_err_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 26 | W1C | 0x0 | size_err_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 25 | W1C | 0x0 | size_err_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 24 | W1C | 0x0 | size_err_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 23 | W1C | 0x0 | line_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 22 | W1C | 0x0 | line_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 21 | W1C | 0x0 | line_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 20 | W1C | 0x0 | line_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 19 | W1C | 0x0 | csi2rx_fifo_overflow_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 18 | W1C | 0x0 | bandwidth_lack_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 17 | W1C | 0x0 | dma_uv_fifo_overflow_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 16 | W1C | 0x0 | dma_y_fifo_overflow_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 15 | W1C | 0x0 | frame1_dma_end_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 14 | W1C | 0x0 | frame0_dma_end_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 13 | W1C | 0x0 | frame1_dma_end_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 12 | W1C | 0x0 | frame0_dma_end_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 11 | W1C | 0x0 | frame1_dma_end_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 10 | W1C | 0x0 | frame0_dma_end_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 9 | W1C | 0x0 | frame1_dma_end_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 8 | W1C | 0x0 | frame0_dma_end_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | W1C | 0x0 | frame1_start_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 6 | W1C | 0x0 | frame0_start_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 5 | W1C | 0x0 | frame1_start_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 4 | W1C | 0x0 | frame0_start_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 3 | W1C | 0x0 | frame1_start_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 2 | W1C | 0x0 | frame0_start_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 1 | W1C | 0x0 | frame1_start_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 0 | W1C | 0x0 | frame0_start_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |

**VICAP_MIPI1_LINE_INT_NUM_ID0_1**

Address: Operational Base + offset (0x027C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | line_int_mode_id1<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0040 | line_int_num_id1<br>For one-time mode, if line_int_num_id1=100, then channel 1 receive 100th line,the line_id1_intst will be 1.<br>For circular mode, if line_int_num_id1=100, then channel 1 receive 100th line200th line300th line.....the line_id1_intst will be 1. |
| 15 | RW | 0x0 | line_int_mode_id0<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 14 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:0 | RW | 0x0040 | line_int_num_id0<br>For one-time mode, if line_int_num_id0=100, then channel 0 receive 100th line,the line_id0_intst will be 1.<br>For circular mode, if line_int_num_id0=100, then channel 0 receive 100th line200th line300th line.....the line_id0_intst will be 1. |

**VICAP_MIPI1_LINE_INT_NUM_ID2_3**

Address: Operational Base + offset (0x0280)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | line_int_mode_id3<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0040 | line_int_num_id3<br>For one-time mode, if line_int_num_id3=100, then channel 3 receive 100th line,the line_id3_intst will be 1.<br>For circular mode, if line_int_num_id3=100, then channel 3 receive 100th line200th line300th line.....the line_id3_intst will be 1. |
| 15 | RW | 0x0 | line_int_mode_id2<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0040 | line_int_num_id2<br>For one-time mode, if line_int_num_id2=100, then channel 2 receive 100th line,the line_id2_intst will be 1.<br>For circular mode, if line_int_num_id2=100, then channel 2 receive 100th line200th line300th line.....the line_id2_intst will be 1. |

**VICAP_MIPI1_LINE_CNT_ID0_1**

Address: Operational Base + offset (0x0284)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_cnt_id1<br>Current line count for id1. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_line_cnt_id0<br>Current line count for id0. |

**VICAP_MIPI1_LINE_CNT_ID2_3**

Address: Operational Base + offset (0x0288)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 29:16 | RW | 0x0000 | line_cnt_id3<br>Current line count for id3. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | line_cnt_id2<br>Current line count for id2. |

**VICAP_MIPI1_ID0_CROP_START**

Address: Operational Base + offset (0x028C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id0<br>The start y coordinate for id0. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id0<br>The start x coordinate for id0, if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI1_ID1_CROP_START**

Address: Operational Base + offset (0x0290)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id1<br>The start y coordinate for id1. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id1<br>The start x coordinate for id1, if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI1_ID2_CROP_START**

Address: Operational Base + offset (0x0294)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id2<br>The start y coordinate for id2. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id2<br>The start x coordinate for id2, if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI1_ID3_CROP_START**

Address: Operational Base + offset (0x0298)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id3<br>The start y coordinate for id3. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id3<br>The start x coordinate for id3, if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI1_FRAME_NUM_VC0**

Address: Operational Base + offset (0x029C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc0<br>The frame number of frame end of virtual channel 0. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc0<br>The frame number of frame start of virtual channel 0. |

**VICAP_MIPI1_FRAME_NUM_VC1**

Address: Operational Base + offset (0x02A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc1<br>The frame number of frame end of virtual channel 1. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc1<br>The frame number of frame start of virtual channel 1. |

**VICAP_MIPI1_FRAME_NUM_VC2**

Address: Operational Base + offset (0x02A4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc2<br>The frame number of frame end of virtual channel 2. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc2<br>The frame number of frame start of virtual channel 2. |

**VICAP_MIPI1_FRAME_NUM_VC3**

Address: Operational Base + offset (0x02A8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc3<br>The frame number of frame end of virtual channel 3. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc3<br>The frame number of frame start of virtual channel 3. |

**VICAP_MIPI1_ID0_EFFECT_CODE**

Address: Operational Base + offset (0x02AC)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id0<br>Effect code of id0 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id0<br>Effect code of id0 for sony sensor. |

**VICAP_MIPI1_ID1_EFFECT_CODE**

Address: Operational Base + offset (0x02B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id1<br>Effect code of id1 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id1<br>Effect code of id1 for sony sensor. |

**VICAP_MIPI1_ID2_EFFECT_CODE**

Address: Operational Base + offset (0x02B4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id2<br>Effect code of id2 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id2<br>Effect code of id2 for sony sensor. |

**VICAP_MIPI1_ID3_EFFECT_CODE**

Address: Operational Base + offset (0x02B8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id3<br>Effect code of id3 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id3<br>Effect code of id3 for sony sensor. |

**VICAP_MIPI1_ON_PAD_VALUE**

Address: Operational Base + offset (0x02BC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RO | 0x00000 | reserved |
| 13:0 | RW | 0x0000 | sw_on_pad_value<br>Padding value for ON sensor. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**VICAP_MIPI1_SIZE_NUM_ID0**

Address: Operational Base + offset (0x02C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_num_id0<br>The id0 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id0<br>The id0 pixel number in one line. |

**VICAP_MIPI1_SIZE_NUM_ID1**

Address: Operational Base + offset (0x02C4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_num_id1<br>The id1 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id1<br>The id1 pixel number in one line. |

**VICAP_MIPI1_SIZE_NUM_ID2**

Address: Operational Base + offset (0x02C8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_num_id2<br>The id2 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id2<br>The id2 pixel number in one line. |

**VICAP_MIPI1_SIZE_NUM_ID3**

Address: Operational Base + offset (0x02CC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_num_id3<br>The id3 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id3<br>The id3 pixel number in one line. |

**VICAP_MIPI2_ID0_CTRL0**

Address: Operational Base + offset (0x0300)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id0<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id0<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id0<br>Enable dma transport id0.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_align_id0<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id0<br>Select command mode for id0.<br>1'b0: Not command mode<br>1'b1: Command mode |
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id0<br>If sw_mipi0_on_hdr_mode_id0=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id0=1, id0 channel will capture the line which line count value equal to 1. |
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id0<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |
| 21:20 | RW | 0x0 | sw_hdr_mode_id0<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id0<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id0<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id0<br>Data type for id0. |
| 9:8 | RW | 0x0 | sw_vc_id0<br>Virtual channel for id0. |
| 7:5 | RW | 0x0 | sw_wrddr_type_id0<br>The write ddr type of id0.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id0<br>Enable to crop for id0.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RW | 0x0 | sw_parse_type_id0<br>The parse type of id0.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |
| 0 | RW | 0x0 | sw_cap_en_id0<br>Enable to capture id0.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI2_ID0_CTRL1**

Address: Operational Base + offset (0x0304)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_height_id0<br>Height for id0. |
| 15:14 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:0 | RW | 0x0000 | sw_width_id0<br>Width for id0. If sw_wrddr_type is rgb888, then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id0 is enable the width value must be 4 aligned. |

**VICAP_MIPI2_ID1_CTRL0**

Address: Operational Base + offset (0x0308)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id1<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id1<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id1<br>Enable dma transport id1.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_align_id1<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id1<br>Select command mode for id1.<br>1'b0: Not command mode<br>1'b1: Command mode |
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id1<br>If sw_mipi0_on_hdr_mode_id1=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id1=1, id1 channel will capture the line which line count value equal to 1. |
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id1<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |
| 21:20 | RW | 0x0 | sw_hdr_mode_id1<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id1<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id1<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id1<br>Data type for id1. |
| 9:8 | RW | 0x0 | sw_vc_id1<br>Virtual channel for id1. |
| 7:5 | RW | 0x0 | sw_wrddr_type_id1<br>The write ddr type of id1.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id1<br>Enable to crop for id1.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RW | 0x0 | sw_parse_type_id1<br>The parse type of id1.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |
| 0 | RW | 0x0 | sw_cap_en_id1<br>Enable to capture id1.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI2_ID1_CTRL1**

Address: Operational Base + offset (0x030C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 29:16 | RW | 0x0000 | sw_height_id1<br>Height for id1. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_width_id1<br>Width for id1. If sw_wrddr_type is rgb888, then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id1 is enable the width value must be 4 aligned. |

**VICAP_MIPI2_ID2_CTRL0**

Address: Operational Base + offset (0x0310)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id2<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id2<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id2<br>Enable dma transport id2.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_align_id2<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id2<br>Select command mode for id2.<br>1'b0: Not command mode<br>1'b1: Command mode |
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id2<br>If sw_mipi0_on_hdr_mode_id2=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id2=1, id2 channel will capture the line which line count value equal to 1. |
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id2<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 21:20 | RW | 0x0 | sw_hdr_mode_id2<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id2<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id2<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id2<br>Data type for id2. |
| 9:8 | RW | 0x0 | sw_vc_id2<br>Virtual channel for id2. |
| 7:5 | RW | 0x0 | sw_wrddr_type_id2<br>The write ddr type of id2.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id2<br>Enable to crop for id2.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RW | 0x0 | sw_parse_type_id2<br>The parse type of id2.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |
| 0 | RW | 0x0 | sw_cap_en_id2<br>Enable to capture id2.<br>1'b0: Disable<br>1'b1: Enable |

Copyright 2022 © Rockchip Electronics Co., Ltd.

**VICAP_MIPI2_ID2_CTRL1**

Address: Operational Base + offset (0x0314)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_height_id2<br>Height for id2. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_width_id2<br>Width for id2. If sw_wrddr_type is rgb888, then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id2 is enable the width value must be 4 aligned. |

**VICAP_MIPI2_ID3_CTRL0**

Address: Operational Base + offset (0x0318)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id3<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id3<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id3<br>Enable dma transport id3.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_align_id3<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id3<br>Select command mode for id3.<br>1'b0: Not command mode<br>1'b1: Command mode |
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id3<br>If sw_mipi0_on_hdr_mode_id3=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id3=1, id3 channel will capture the line which line count value equal to 1. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id3<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |
| 21:20 | RW | 0x0 | sw_hdr_mode_id3<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id3<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id3<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id3<br>Data type for id3. |
| 9:8 | RW | 0x0 | sw_vc_id3<br>Virtual channel for id3. |
| 7:5 | RW | 0x0 | sw_wrddr_type_id3<br>The write ddr type of id3.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id3<br>Enable to crop for id3.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RW | 0x0 | sw_parse_type_id3<br>The parse type of id3.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | sw_cap_en_id3<br>Enable to capture id3.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI2_ID3_CTRL1**

Address: Operational Base + offset (0x031C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_height_id3<br>Height for id3. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_width_id3<br>Width for id3. If sw_wrddr_type is rgb888, then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id3 is enable the width value must be 4 aligned. |

**VICAP_MIPI2_CTRL**

Address: Operational Base + offset (0x0320)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:18 | RW | 0x0 | sw_soft_rst_mode<br>2'b00: Soft reset and protect toisp path frame integrity;<br>2'b01: Soft reset and protect toisp path frame integrity and pull down sw_cap_en automatically;<br>2'b10: Soft reset directly;<br>2'b11: Reserved. |
| 17 | RW | 0x0 | sw_soft_rst<br>1'b0: Not reset<br>1'b1: Reset the VICAP MIPI2 path(except MMU/AXI MASTER/REG FILE) |
| 16 | RW | 0x0 | sw_dma_rst<br>Write 1 will reset VICAP MIPI2 path dma.<br>When this bit change to 0,dma is reseted completely. |
| 15:13 | RW | 0x0 | sw_press_value<br>Press value. |
| 12 | RW | 0x0 | sw_press_en<br>1'b0: Disable press<br>1'b1: Enable press |
| 11:8 | RO | 0x0 | reserved |
| 7:5 | RW | 0x0 | sw_hurry_value<br>Hurry value. |
| 4 | RW | 0x0 | sw_hurry_en<br>1'b0: Disable hurry<br>1'b1: Enable hurry |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RO | 0x0 | reserved |
| 2:1 | RW | 0x0 | sw_water_line<br>2'b00: 75%<br>2'b01: 50%<br>2'b10: 25%<br>2'b11: 0% |
| 0 | RW | 0x0 | sw_cap_en<br>1'b0: Disable capture all id<br>1'b1: Enable capture all id. |

**VICAP_MIPI2_FRAME0_ADDR_Y_ID0**

Address: Operational Base + offset (0x0324)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id0<br>First address of even frame for ID0 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI2_FRAME1_ADDR_Y_ID0**

Address: Operational Base + offset (0x0328)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id0<br>First address of odd frame for ID0 Y path(must be aligned to double word). |

**VICAP_MIPI2_FRAME0_ADDR_UV_ID0**

Address: Operational Base + offset (0x032C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id0<br>First address of even frame for ID0 UV path(must be aligned to double word). |

**VICAP_MIPI2_FRAME1_ADDR_UV_ID0**

Address: Operational Base + offset (0x0330)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id0<br>First address of odd frame for ID0 UV path(must be aligned to double word). |

**VICAP_MIPI2_VLW_ID0**

Address: Operational Base + offset (0x0334)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_id0<br>Virtual line width of even frame for ID0 path(must be aligned to double word). |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**VICAP_MIPI2_FRAME0_ADDR_Y_ID1**

Address: Operational Base + offset (0x0338)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id1<br>First address of even frame for ID1 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI2_FRAME1_ADDR_Y_ID1**

Address: Operational Base + offset (0x033C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id1<br>First address of odd frame for ID1 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI2_FRAME0_ADDR_UV_ID1**

Address: Operational Base + offset (0x0340)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id1<br>First address of even frame for ID1 UV path(must be aligned to double word). |

**VICAP_MIPI2_FRAME1_ADDR_UV_ID1**

Address: Operational Base + offset (0x0344)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id1<br>First address of odd frame for ID1 UV path(must be aligned to double word). |

**VICAP_MIPI2_VLW_ID1**

Address: Operational Base + offset (0x0348)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_id1<br>Virtual line width of even frame for ID1 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI2_FRAME0_ADDR_Y_ID2**

Address: Operational Base + offset (0x034C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id2<br>First address of even frame for ID2 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI2_FRAME1_ADDR_Y_ID2**

Address: Operational Base + offset (0x0350)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id2<br>First address of odd frame for ID2 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI2_FRAME0_ADDR_UV_ID2**

Address: Operational Base + offset (0x0354)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id2<br>First address of even frame for ID2 UV path(must be aligned to double word). |

**VICAP_MIPI2_FRAME1_ADDR_UV_ID2**

Address: Operational Base + offset (0x0358)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id0<br>First address of odd frame for ID2 UV path(must be aligned to double word). |

**VICAP_MIPI2_VLW_ID2**

Address: Operational Base + offset (0x035C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_id2<br>Virtual line width of even frame for ID2 path(must be aligned to double word). |

**VICAP_MIPI2_FRAME0_ADDR_Y_ID3**

Address: Operational Base + offset (0x0360)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id3<br>First address of even frame for ID3 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI2_FRAME1_ADDR_Y_ID3**

Address: Operational Base + offset (0x0364)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id3<br>First address of odd frame for ID3 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI2_FRAME0_ADDR_UV_ID3**

Address: Operational Base + offset (0x0368)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id3<br>First address of even frame for ID3 UV path(must be aligned to double word). |

**VICAP_MIPI2_FRAME1_ADDR_UV_ID3**

Address: Operational Base + offset (0x036C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id3<br>First address of odd frame for ID3 UV path(must be aligned to double word). |

**VICAP_MIPI2_VLW_ID3**

Address: Operational Base + offset (0x0370)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_id3<br>Virtual line width of even frame for ID3 path(must be aligned to double word). |

**VICAP_MIPI2_INTEN**

Address: Operational Base + offset (0x0374)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27 | RW | 0x0 | size_err_id3_inten<br>1'b0: Disable<br>1'b1: Enable |
| 26 | RW | 0x0 | size_err_id2_inten<br>1'b0: Disable<br>1'b1: Enable |
| 25 | RW | 0x0 | size_err_id1_inten<br>1'b0: Disable<br>1'b1: Enable |
| 24 | RW | 0x0 | size_err_id0_inten<br>1'b0: Disable<br>1'b1: Enable |
| 23 | RW | 0x0 | line_id3_inten<br>1'b0: Disable<br>1'b1: Enable |
| 22 | RW | 0x0 | line_id2_inten<br>1'b0: Disable<br>1'b1: Enable |
| 21 | RW | 0x0 | line_id1_inten<br>1'b0: Disable<br>1'b1: Enable |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 20 | RW | 0x0 | line_id0_inten<br>1'b0: Disable<br>1'b1: Enable |
| 19 | RW | 0x0 | csi2rx_fifo_overflow_inten<br>1'b0: Disable<br>1'b1: Enable |
| 18 | RW | 0x0 | bandwidth_lack_inten<br>1'b0: Disable<br>1'b1: Enable |
| 17 | RW | 0x0 | dma_uv_fifo_overflow_inten<br>Enable the interrupt of dma fifo overflow of MIPI uv path or LVDS id1 path.<br>1'b0: Disable<br>1'b1: Enable |
| 16 | RW | 0x0 | dma_y_fifo_overflow_inten<br>Enable the interrupt of dma fifo overflow of MIPI y path or LVDS id0 path.<br>1'b0: Disable<br>1'b1: Enable |
| 15 | RW | 0x0 | frame1_dma_end_id3_inten<br>Enable the interrupt of end of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | frame0_dma_end_id3_inten<br>Enable the interrupt of end of even frame for ID3.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | frame1_dma_end_id2_inten<br>Enable the interrupt of end of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | frame0_dma_end_id2_inten<br>Enable the interrupt of end of even frame for ID2.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | frame1_dma_end_id1_inten<br>Enable the interrupt of end of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | frame0_dma_end_id1_inten<br>Enable the interrupt of end of even frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RW | 0x0 | frame1_dma_end_id0_inten<br>Enable the interrupt of end of odd frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | frame0_dma_end_id0_inten<br>Enable the interrupt of end of even frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | frame1_start_id3_inten<br>Enable the interrupt of start of odd frame for ID3.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | frame0_start_id3_inten<br>Enable the interrupt of start of even frame for ID3.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | frame1_start_id2_inten<br>Enable the interrupt of start of odd frame for ID2.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | frame0_start_id2_inten<br>Enable the interrupt of start of even frame for ID2.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | frame1_start_id1_inten<br>Enable the interrupt of start of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | frame0_start_id1_inten<br>Enable the interrupt of start of even frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | frame1_start_id0_inten<br>Enable the interrupt of start of odd frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | frame0_start_id0_inten<br>Enable the interrupt of start of even frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI2_INTSTAT**

Address: Operational Base + offset (0x0378)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 27 | W1C | 0x0 | size_err_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 26 | W1C | 0x0 | size_err_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 25 | W1C | 0x0 | size_err_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 24 | W1C | 0x0 | size_err_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 23 | W1C | 0x0 | line_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 22 | W1C | 0x0 | line_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 21 | W1C | 0x0 | line_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 20 | W1C | 0x0 | line_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 19 | W1C | 0x0 | csi2rx_fifo_overflow_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 18 | W1C | 0x0 | bandwidth_lack_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 17 | W1C | 0x0 | dma_uv_fifo_overflow_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 16 | W1C | 0x0 | dma_y_fifo_overflow_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 15 | W1C | 0x0 | frame1_dma_end_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 14 | W1C | 0x0 | frame0_dma_end_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 13 | W1C | 0x0 | frame1_dma_end_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | W1C | 0x0 | frame0_dma_end_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 11 | W1C | 0x0 | frame1_dma_end_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 10 | W1C | 0x0 | frame0_dma_end_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 9 | W1C | 0x0 | frame1_dma_end_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 8 | W1C | 0x0 | frame0_dma_end_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 7 | W1C | 0x0 | frame1_start_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 6 | W1C | 0x0 | frame0_start_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 5 | W1C | 0x0 | frame1_start_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 4 | W1C | 0x0 | frame0_start_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 3 | W1C | 0x0 | frame1_start_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 2 | W1C | 0x0 | frame0_start_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 1 | W1C | 0x0 | frame1_start_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 0 | W1C | 0x0 | frame0_start_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |

**VICAP_MIPI2_LINE_INT_NUM_ID0_1**

Address: Operational Base + offset (0x037C)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | line_int_mode_id1<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0040 | line_int_num_id1<br>For one-time mode, if line_int_num_id1=100, then channel 1 receive 100th line, the line_id1_intst will be 1.<br>For circular mode, if line_int_num_id1=100, then channel 1 receive 100th line200th line300th line.....the line_id1_intst will be 1. |
| 15 | RW | 0x0 | line_int_mode_id0<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0040 | line_int_num_id0<br>For one-time mode, if line_int_num_id0=100, then channel 0 receive 100th line, the line_id0_intst will be 1.<br>For circular mode, if line_int_num_id0=100, then channel 0 receive 100th line200th line300th line.....the line_id0_intst will be 1. |

**VICAP_MIPI2_LINE_INT_NUM_ID2_3**

Address: Operational Base + offset (0x0380)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | line_int_mode_id3<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0040 | line_int_num_id3<br>For one-time mode, if line_int_num_id3=100, then channel 3 receive 100th line, the line_id3_intst will be 1.<br>For circular mode, if line_int_num_id3=100, then channel 3 receive 100th line200th line300th line.....the line_id3_intst will be 1. |
| 15 | RW | 0x0 | line_int_mode_id2<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0040 | line_int_num_id2<br>For one-time mode, if line_int_num_id2=100, then channel 2 receive 100th line, the line_id2_intst will be 1.<br>For circular mode, if line_int_num_id2=100, then channel 2 receive 100th line200th line300th line.....the line_id2_intst will be 1. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**VICAP_MIPI2_LINE_CNT_ID0_1**

Address: Operational Base + offset (0x0384)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_cnt_id1<br>Current line count for id1. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_line_cnt_id0<br>Current line count for id0. |

**VICAP_MIPI2_LINE_CNT_ID2_3**

Address: Operational Base + offset (0x0388)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_cnt_id3<br>Current line count for id3. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_line_cnt_id2<br>Current line count for id2. |

**VICAP_MIPI2_ID0_CROP_START**

Address: Operational Base + offset (0x038C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id0<br>The start y coordinate for id0. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id0<br>The start x coordinate for id0, if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI2_ID1_CROP_START**

Address: Operational Base + offset (0x0390)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id1<br>The start y coordinate for id1. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id1<br>The start x coordinate for id1, if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI2_ID2_CROP_START**

Address: Operational Base + offset (0x0394)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id2<br>The start y coordinate for id2. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id2<br>The start x coordinate for id2, if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI2_ID3_CROP_START**

Address: Operational Base + offset (0x0398)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id3<br>The start y coordinate for id3. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id3<br>The start x coordinate for id3, if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI2_FRAME_NUM_VC0**

Address: Operational Base + offset (0x039C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc0<br>The frame number of frame end of virtual channel 0. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc0<br>The frame number of frame start of virtual channel 0. |

**VICAP_MIPI2_FRAME_NUM_VC1**

Address: Operational Base + offset (0x03A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc1<br>The frame number of frame end of virtual channel 1. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc1<br>The frame number of frame start of virtual channel 1. |

**VICAP_MIPI2_FRAME_NUM_VC2**

Address: Operational Base + offset (0x03A4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc2<br>The frame number of frame end of virtual channel 2. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc2<br>The frame number of frame start of virtual channel 2. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**VICAP_MIPI2_FRAME_NUM_VC3**

Address: Operational Base + offset (0x03A8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc3<br>The frame number of frame end of virtual channel 3. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc3<br>The frame number of frame start of virtual channel 3. |

**VICAP_MIPI2_ID0_EFFECT_CODE**

Address: Operational Base + offset (0x03AC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id0<br>Effect code of id0 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id0<br>Effect code of id0 for sony sensor. |

**VICAP_MIPI2_ID1_EFFECT_CODE**

Address: Operational Base + offset (0x03B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id1<br>Effect code of id1 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id1<br>Effect code of id1 for sony sensor. |

**VICAP_MIPI2_ID2_EFFECT_CODE**

Address: Operational Base + offset (0x03B4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id2<br>Effect code of id2 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id2<br>Effect code of id2 for sony sensor. |

**VICAP_MIPI2_ID3_EFFECT_CODE**

Address: Operational Base + offset (0x03B8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id3<br>Effect code of id3 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id3<br>Effect code of id3 for sony sensor. |

**VICAP_MIPI2_ON_PAD_VALUE**

Address: Operational Base + offset (0x03BC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RO | 0x00000 | reserved |
| 13:0 | RW | 0x0000 | sw_on_pad_value<br>Padding value for ON sensor. |

**VICAP_MIPI2_SIZE_NUM_ID0**

Address: Operational Base + offset (0x03C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_num_id0<br>The id0 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id0<br>The id0 pixel number in one line. |

**VICAP_MIPI2_SIZE_NUM_ID1**

Address: Operational Base + offset (0x03C4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_num_id1<br>The id1 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id1<br>The id1 pixel number in one line. |

**VICAP_MIPI2_SIZE_NUM_ID2**

Address: Operational Base + offset (0x03C8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_num_id2<br>The id2 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id2<br>The id2 pixel number in one line. |

**VICAP_MIPI2_SIZE_NUM_ID3**

Address: Operational Base + offset (0x03CC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 29:16 | RO | 0x0000 | ro_line_num_id3<br>The id3 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id3<br>The id3 pixel number in one line. |

**VICAP_MIPI3_ID0_CTRL0**

Address: Operational Base + offset (0x0400)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id0<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id0<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id0<br>Enable dma transport id0.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_align_id0<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id0<br>Select command mode for id0.<br>1'b0: Not command mode<br>1'b1: Command mode |
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id0<br>If sw_mipi0_on_hdr_mode_id0=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id0=1, id0 channel will capture the line which line count value equal to 1. |
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id0<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 21:20 | RW | 0x0 | sw_hdr_mode_id0<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id0<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id0<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id0<br>Data type for id0. |
| 9:8 | RW | 0x0 | sw_vc_id0<br>Virtual channel for id0. |
| 7:5 | RW | 0x0 | sw_wrddr_type_id0<br>The write ddr type of id0.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id0<br>Enable to crop for id0.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RW | 0x0 | sw_parse_type_id0<br>The parse type of id0.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |
| 0 | RW | 0x0 | sw_cap_en_id0<br>Enable to capture id0.<br>1'b0: Disable<br>1'b1: Enable |

Copyright 2022 © Rockchip Electronics Co., Ltd.

**VICAP_MIPI3_ID0_CTRL1**

Address: Operational Base + offset (0x0404)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_height_id0<br>Height for id0. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_width_id0<br>Width for id0. If sw_wrddr_type is rgb888, then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id0 is enable the width value must be 4 aligned. |

**VICAP_MIPI3_ID1_CTRL0**

Address: Operational Base + offset (0x0408)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id1<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id1<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id1<br>Enable dma transport id1.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_align_id1<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id1<br>Select command mode for id1.<br>1'b0: Not command mode<br>1'b1: Command mode |
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id1<br>If sw_mipi0_on_hdr_mode_id1=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id1=1, id1 channel will capture the line which line count value equal to 1. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id1<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |
| 21:20 | RW | 0x0 | sw_hdr_mode_id1<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id1<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id1<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id1<br>Data type for id1. |
| 9:8 | RW | 0x0 | sw_vc_id1<br>Virtual channel for id1. |
| 7:5 | RW | 0x0 | sw_wrddr_type_id1<br>The write ddr type of id1.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id1<br>Enable to crop for id1.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RW | 0x0 | sw_parse_type_id1<br>The parse type of id1.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | sw_cap_en_id1<br>Enable to capture id1.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI3_ID1_CTRL1**

Address: Operational Base + offset (0x040C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_height_id1<br>Height for id1. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_width_id1<br>Width for id1. If sw_wrddr_type is rgb888, then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id1 is enable the width value must be 4 aligned. |

**VICAP_MIPI3_ID2_CTRL0**

Address: Operational Base + offset (0x0410)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id2<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id2<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00.<br>And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id2<br>Enable dma transport id2.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_align_id2<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id2<br>Select command mode for id2.<br>1'b0: Not command mode<br>1'b1: Command mode |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id2<br>If sw_mipi0_on_hdr_mode_id2=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id2=1, id2 channel will capture the line which line count value equal to 1. |
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id2<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |
| 21:20 | RW | 0x0 | sw_hdr_mode_id2<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id2<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id2<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id2<br>Data type for id2. |
| 9:8 | RW | 0x0 | sw_vc_id2<br>Virtual channel for id2. |
| 7:5 | RW | 0x0 | sw_wrddr_type_id2<br>The write ddr type of id2.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id2<br>Enable to crop for id2.<br>1'b0: Disable<br>1'b1: Enable |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:1 | RW | 0x0 | sw_parse_type_id2<br>The parse type of id2.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |
| 0 | RW | 0x0 | sw_cap_en_id2<br>Enable to capture id2.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI3_ID2_CTRL1**

Address: Operational Base + offset (0x0414)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_height_id2<br>Height for id2. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_width_id2<br>Width for id2. If sw_wrddr_type is rgb888, then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id2 is enable the width value must be 4 aligned. |

**VICAP_MIPI3_ID3_CTRL0**

Address: Operational Base + offset (0x0418)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id3<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id3<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00.<br>And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id3<br>Enable dma transport id3.<br>1'b0: Disable<br>1'b1: Enable |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 27 | RW | 0x0 | sw_align_id3<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id3<br>Select command mode for id3.<br>1'b0: Not command mode<br>1'b1: Command mode |
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id3<br>If sw_mipi0_on_hdr_mode_id3=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id3=1, id3 channel will capture the line which line count value equal to 1. |
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id3<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |
| 21:20 | RW | 0x0 | sw_hdr_mode_id3<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id3<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id3<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id3<br>Data type for id3. |
| 9:8 | RW | 0x0 | sw_vc_id3<br>Virtual channel for id3. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:5 | RW | 0x0 | sw_wrddr_type_id3<br>The write ddr type of id3.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id3<br>Enable to crop for id3.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RW | 0x0 | sw_parse_type_id3<br>The parse type of id3.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |
| 0 | RW | 0x0 | sw_cap_en_id3<br>Enable to capture id3.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI3_ID3_CTRL1**

Address: Operational Base + offset (0x041C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_height_id3<br>Height for id3. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_width_id3<br>Width for id3. If sw_wrddr_type is rgb888, then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id3 is enable the width value must be 4 aligned. |

**VICAP_MIPI3_CTRL**

Address: Operational Base + offset (0x0420)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19:18 | RW | 0x0 | sw_soft_rst_mode<br>2'b00: Soft reset and protect toisp path frame integrity;<br>2'b01: Soft reset and protect toisp path frame integrity and pull down sw_cap_en automatically;<br>2'b10: Soft reset directly;<br>2'b11: Reserved. |
| 17 | RW | 0x0 | sw_soft_rst<br>1'b0: Not reset<br>1'b1: Reset the VICAP MIPI3 path(except MMU/AXI MASTER/REG FILE) |
| 16 | RW | 0x0 | sw_dma_rst<br>Write 1 will reset VICAP MIPI3 path dma.<br>When this bit change to 0,dma is reseted completely. |
| 15:13 | RW | 0x0 | sw_press_value<br>Press value. |
| 12 | RW | 0x0 | sw_press_en<br>1'b0: Disable press<br>1'b1: Enable press |
| 11:8 | RO | 0x0 | reserved |
| 7:5 | RW | 0x0 | sw_hurry_value<br>Hurry value. |
| 4 | RW | 0x0 | sw_hurry_en<br>1'b0: Disable hurry<br>1'b1: Enable hurry |
| 3 | RO | 0x0 | reserved |
| 2:1 | RW | 0x0 | sw_water_line<br>2'b00: 75%<br>2'b01: 50%<br>2'b10: 25%<br>2'b11: 0% |
| 0 | RW | 0x0 | sw_cap_en<br>1'b0: Disable capture all id<br>1'b1: Enable capture all id. |

**VICAP_MIPI3_FRAME0_ADDR_Y_ID0**

Address: Operational Base + offset (0x0424)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id0<br>First address of even frame for ID0 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI3_FRAME1_ADDR_Y_ID0**

Address: Operational Base + offset (0x0428)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id0<br>First address of odd frame for ID0 Y path(must be aligned to double word). |

**VICAP_MIPI3_FRAME0_ADDR_UV_ID0**

Address: Operational Base + offset (0x042C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id0<br>First address of even frame for ID0 UV path(must be aligned to double word). |

**VICAP_MIPI3_FRAME1_ADDR_UV_ID0**

Address: Operational Base + offset (0x0430)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id0<br>First address of odd frame for ID0 UV path(must be aligned to double word). |

**VICAP_MIPI3_VLW_ID0**

Address: Operational Base + offset (0x0434)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_id0<br>Virtual line width of even frame for ID0 path(must be aligned to double word). |

**VICAP_MIPI3_FRAME0_ADDR_Y_ID1**

Address: Operational Base + offset (0x0438)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id1<br>First address of even frame for ID1 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI3_FRAME1_ADDR_Y_ID1**

Address: Operational Base + offset (0x043C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id1<br>First address of odd frame for ID1 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI3_FRAME0_ADDR_UV_ID1**

Address: Operational Base + offset (0x0440)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id1<br>First address of even frame for ID1 UV path(must be aligned to double word). |

**VICAP_MIPI3_FRAME1_ADDR_UV_ID1**

Address: Operational Base + offset (0x0444)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id1<br>First address of odd frame for ID1 UV path(must be aligned to double word). |

**VICAP_MIPI3_VLW_ID1**

Address: Operational Base + offset (0x0448)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_id1<br>Virtual line width of even frame for ID1 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI3_FRAME0_ADDR_Y_ID2**

Address: Operational Base + offset (0x044C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id2<br>First address of even frame for ID2 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI3_FRAME1_ADDR_Y_ID2**

Address: Operational Base + offset (0x0450)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id2<br>First address of odd frame for ID2 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI3_FRAME0_ADDR_UV_ID2**

Address: Operational Base + offset (0x0454)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id2<br>First address of even frame for ID2 UV path(must be aligned to double word). |

**VICAP_MIPI3_FRAME1_ADDR_UV_ID2**

Address: Operational Base + offset (0x0458)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id0<br>First address of odd frame for ID2 UV path(must be aligned to double word). |

**VICAP_MIPI3_VLW_ID2**

Address: Operational Base + offset (0x045C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_id2<br>Virtual line width of even frame for ID2 path(must be aligned to double word). |

**VICAP_MIPI3_FRAME0_ADDR_Y_ID3**

Address: Operational Base + offset (0x0460)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id3<br>First address of even frame for ID3 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI3_FRAME1_ADDR_Y_ID3**

Address: Operational Base + offset (0x0464)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id3<br>First address of odd frame for ID3 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI3_FRAME0_ADDR_UV_ID3**

Address: Operational Base + offset (0x0468)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id3<br>First address of even frame for ID3 UV path(must be aligned to double word). |

**VICAP_MIPI3_FRAME1_ADDR_UV_ID3**

Address: Operational Base + offset (0x046C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id3<br>First address of odd frame for ID3 UV path(must be aligned to double word). |

**VICAP_MIPI3_VLW_ID3**

Address: Operational Base + offset (0x0470)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19:0 | RW | 0x00000 | sw_vlw_id3<br>Virtual line width of even frame for ID3 path(must be aligned to double word). |

**VICAP_MIPI3_INTEN**

Address: Operational Base + offset (0x0474)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27 | RW | 0x0 | size_err_id3_inten<br>1'b0: Disable<br>1'b1: Enable |
| 26 | RW | 0x0 | size_err_id2_inten<br>1'b0: Disable<br>1'b1: Enable |
| 25 | RW | 0x0 | size_err_id1_inten<br>1'b0: Disable<br>1'b1: Enable |
| 24 | RW | 0x0 | size_err_id0_inten<br>1'b0: Disable<br>1'b1: Enable |
| 23 | RW | 0x0 | line_id3_inten<br>1'b0: Disable<br>1'b1: Enable |
| 22 | RW | 0x0 | line_id2_inten<br>1'b0: Disable<br>1'b1: Enable |
| 21 | RW | 0x0 | line_id1_inten<br>1'b0: Disable<br>1'b1: Enable |
| 20 | RW | 0x0 | line_id0_inten<br>1'b0: Disable<br>1'b1: Enable |
| 19 | RW | 0x0 | csi2rx_fifo_overflow_inten<br>1'b0: Disable<br>1'b1: Enable |
| 18 | RW | 0x0 | bandwidth_lack_inten<br>1'b0: Disable<br>1'b1: Enable |
| 17 | RW | 0x0 | dma_uv_fifo_overflow_inten<br>Enable the interrupt of dma fifo overflow of MIPI uv path or LVDS id1 path.<br>1'b0: Disable<br>1'b1: Enable |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 16 | RW | 0x0 | dma_y_fifo_overflow_inten<br>Enable the interrupt of dma fifo overflow of MIPI y path or LVDS id0 path.<br>1'b0: Disable<br>1'b1: Enable |
| 15 | RW | 0x0 | frame1_dma_end_id3_inten<br>Enable the interrupt of end of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | frame0_dma_end_id3_inten<br>Enable the interrupt of end of even frame for ID3.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | frame1_dma_end_id2_inten<br>Enable the interrupt of end of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | frame0_dma_end_id2_inten<br>Enable the interrupt of end of even frame for ID2.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | frame1_dma_end_id1_inten<br>Enable the interrupt of end of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | frame0_dma_end_id1_inten<br>Enable the interrupt of end of even frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | frame1_dma_end_id0_inten<br>Enable the interrupt of end of odd frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | frame0_dma_end_id0_inten<br>Enable the interrupt of end of even frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | frame1_start_id3_inten<br>Enable the interrupt of start of odd frame for ID3.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | frame0_start_id3_inten<br>Enable the interrupt of start of even frame for ID3.<br>1'b0: Disable<br>1'b1: Enable |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | frame1_start_id2_inten<br>Enable the interrupt of start of odd frame for ID2.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | frame0_start_id2_inten<br>Enable the interrupt of start of even frame for ID2.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | frame1_start_id1_inten<br>Enable the interrupt of start of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | frame0_start_id1_inten<br>Enable the interrupt of start of even frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | frame1_start_id0_inten<br>Enable the interrupt of start of odd frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | frame0_start_id0_inten<br>Enable the interrupt of start of even frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI3_INTSTAT**

Address: Operational Base + offset (0x0478)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27 | W1C | 0x0 | size_err_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 26 | W1C | 0x0 | size_err_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 25 | W1C | 0x0 | size_err_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 24 | W1C | 0x0 | size_err_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 23 | W1C | 0x0 | line_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 22 | W1C | 0x0 | line_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 21 | W1C | 0x0 | line_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 20 | W1C | 0x0 | line_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 19 | W1C | 0x0 | csi2rx_fifo_overflow_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 18 | W1C | 0x0 | bandwidth_lack_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 17 | W1C | 0x0 | dma_uv_fifo_overflow_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 16 | W1C | 0x0 | dma_y_fifo_overflow_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 15 | W1C | 0x0 | frame1_dma_end_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 14 | W1C | 0x0 | frame0_dma_end_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 13 | W1C | 0x0 | frame1_dma_end_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 12 | W1C | 0x0 | frame0_dma_end_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 11 | W1C | 0x0 | frame1_dma_end_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 10 | W1C | 0x0 | frame0_dma_end_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 9 | W1C | 0x0 | frame1_dma_end_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 8 | W1C | 0x0 | frame0_dma_end_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | W1C | 0x0 | frame1_start_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 6 | W1C | 0x0 | frame0_start_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 5 | W1C | 0x0 | frame1_start_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 4 | W1C | 0x0 | frame0_start_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 3 | W1C | 0x0 | frame1_start_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 2 | W1C | 0x0 | frame0_start_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 1 | W1C | 0x0 | frame1_start_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 0 | W1C | 0x0 | frame0_start_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |

**VICAP_MIPI3_LINE_INT_NUM_ID0_1**

Address: Operational Base + offset (0x047C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | line_int_mode_id1<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0040 | line_int_num_id1<br>For one-time mode, if line_int_num_id1=100, then channel 1 receive 100th line, the line_id1_intst will be 1.<br>For circular mode, if line_int_num_id1=100, then channel 1 receive 100th line200th line300th line.....the line_id1_intst will be 1. |
| 15 | RW | 0x0 | line_int_mode_id0<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 14 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:0 | RW | 0x0040 | line_int_num_id0<br>For one-time mode, if line_int_num_id0=100, then channel 0 receive 100th line, the line_id0_intst will be 1.<br>For circular mode, if line_int_num_id0=100, then channel 0 receive 100th line200th line300th line.....the line_id0_intst will be 1. |

**VICAP_MIPI3_LINE_INT_NUM_ID2_3**

Address: Operational Base + offset (0x0480)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | line_int_mode_id3<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0040 | line_int_num_id3<br>For one-time mode, if line_int_num_id3=100, then channel 3 receive 100th line, the line_id3_intst will be 1.<br>For circular mode, if line_int_num_id3=100, then channel 3 receive 100th line200th line300th line.....the line_id3_intst will be 1. |
| 15 | RW | 0x0 | line_int_mode_id2<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0040 | line_int_num_id2<br>For one-time mode, if line_int_num_id2=100, then channel 2 receive 100th line, the line_id2_intst will be 1.<br>For circular mode, if line_int_num_id2=100, then channel 2 receive 100th line200th line300th line.....the line_id2_intst will be 1. |

**VICAP_MIPI3_LINE_CNT_ID0_1**

Address: Operational Base + offset (0x0484)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_cnt_id1<br>Current line count for id1. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_line_cnt_id0<br>Current line count for id0. |

**VICAP_MIPI3_LINE_CNT_ID2_3**

Address: Operational Base + offset (0x0488)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 29:16 | RW | 0x0000 | line_cnt_id3<br>Current line count for id3. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | line_cnt_id2<br>Current line count for id2. |

**VICAP_MIPI3_ID0_CROP_START**

Address: Operational Base + offset (0x048C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id0<br>The start y coordinate for id0. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id0<br>The start x coordinate for id0, if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI3_ID1_CROP_START**

Address: Operational Base + offset (0x0490)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id1<br>The start y coordinate for id1. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id1<br>The start x coordinate for id1, if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI3_ID2_CROP_START**

Address: Operational Base + offset (0x0494)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id2<br>The start y coordinate for id2. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id2<br>The start x coordinate for id2, if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI3_ID3_CROP_START**

Address: Operational Base + offset (0x0498)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id3<br>The start y coordinate for id3. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id3<br>The start x coordinate for id3, if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI3_FRAME_NUM_VC0**

Address: Operational Base + offset (0x049C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc0<br>The frame number of frame end of virtual channel 0. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc0<br>The frame number of frame start of virtual channel 0. |

**VICAP_MIPI3_FRAME_NUM_VC1**

Address: Operational Base + offset (0x04A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc1<br>The frame number of frame end of virtual channel 1. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc1<br>The frame number of frame start of virtual channel 1. |

**VICAP_MIPI3_FRAME_NUM_VC2**

Address: Operational Base + offset (0x04A4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc2<br>The frame number of frame end of virtual channel 2. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc2<br>The frame number of frame start of virtual channel 2. |

**VICAP_MIPI3_FRAME_NUM_VC3**

Address: Operational Base + offset (0x04A8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc3<br>The frame number of frame end of virtual channel 3. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc3<br>The frame number of frame start of virtual channel 3. |

**VICAP_MIPI3_ID0_EFFECT_CODE**

Address: Operational Base + offset (0x04AC)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id0<br>Effect code of id0 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id0<br>Effect code of id0 for sony sensor. |

**VICAP_MIPI3_ID1_EFFECT_CODE**

Address: Operational Base + offset (0x04B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id1<br>Effect code of id1 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id1<br>Effect code of id1 for sony sensor. |

**VICAP_MIPI3_ID2_EFFECT_CODE**

Address: Operational Base + offset (0x04B4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id2<br>Effect code of id2 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id2<br>Effect code of id2 for sony sensor. |

**VICAP_MIPI3_ID3_EFFECT_CODE**

Address: Operational Base + offset (0x04B8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id3<br>Effect code of id3 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id3<br>Effect code of id3 for sony sensor. |

**VICAP_MIPI3_ON_PAD_VALUE**

Address: Operational Base + offset (0x04BC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RO | 0x00000 | reserved |
| 13:0 | RW | 0x0000 | sw_on_pad_value<br>Padding value for ON sensor. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**VICAP_MIPI3_SIZE_NUM_ID0**

Address: Operational Base + offset (0x04C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_num_id0<br>The id0 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id0<br>The id0 pixel number in one line. |

**VICAP_MIPI3_SIZE_NUM_ID1**

Address: Operational Base + offset (0x04C4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_num_id1<br>The id1 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id1<br>The id1 pixel number in one line. |

**VICAP_MIPI3_SIZE_NUM_ID2**

Address: Operational Base + offset (0x04C8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_num_id2<br>The id2 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id2<br>The id2 pixel number in one line. |

**VICAP_MIPI3_SIZE_NUM_ID3**

Address: Operational Base + offset (0x04CC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_num_id3<br>The id3 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id3<br>The id3 pixel number in one line. |

**VICAP_MIPI4_ID0_CTRL0**

Address: Operational Base + offset (0x0500)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id0<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id0<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id0<br>Enable dma transport id0.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_align_id0<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id0<br>Select command mode for id0.<br>1'b0: Not command mode<br>1'b1: Command mode |
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id0<br>If sw_mipi0_on_hdr_mode_id0=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id0=1, id0 channel will capture the line which line count value equal to 1. |
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id0<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |
| 21:20 | RW | 0x0 | sw_hdr_mode_id0<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id0<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id0<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id0<br>Data type for id0. |
| 9:8 | RW | 0x0 | sw_vc_id0<br>Virtual channel for id0. |
| 7:5 | RW | 0x0 | sw_wrddr_type_id0<br>The write ddr type of id0.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id0<br>Enable to crop for id0.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RW | 0x0 | sw_parse_type_id0<br>The parse type of id0.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |
| 0 | RW | 0x0 | sw_cap_en_id0<br>Enable to capture id0.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI4_ID0_CTRL1**

Address: Operational Base + offset (0x0504)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_height_id0<br>Height for id0. |
| 15:14 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:0 | RW | 0x0000 | sw_width_id0<br>Width for id0. If sw_wrddr_type is rgb888, then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id0 is enable the width value must be 4 aligned. |

**VICAP_MIPI4_ID1_CTRL0**

Address: Operational Base + offset (0x0508)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id1<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id1<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id1<br>Enable dma transport id1.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_align_id1<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id1<br>Select command mode for id1.<br>1'b0: Not command mode<br>1'b1: Command mode |
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id1<br>If sw_mipi0_on_hdr_mode_id1=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id1=1, id1 channel will capture the line which line count value equal to 1. |
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id1<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |
| 21:20 | RW | 0x0 | sw_hdr_mode_id1<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id1<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id1<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id1<br>Data type for id1. |
| 9:8 | RW | 0x0 | sw_vc_id1<br>Virtual channel for id1. |
| 7:5 | RW | 0x0 | sw_wrddr_type_id1<br>The write ddr type of id1.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id1<br>Enable to crop for id1.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RW | 0x0 | sw_parse_type_id1<br>The parse type of id1.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |
| 0 | RW | 0x0 | sw_cap_en_id1<br>Enable to capture id1.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI4_ID1_CTRL1**

Address: Operational Base + offset (0x050C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 29:16 | RW | 0x0000 | sw_height_id1<br>Height for id1. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_width_id1<br>Width for id1. If sw_wrddr_type is rgb888, then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id1 is enable the width value must be 4 aligned. |

**VICAP_MIPI4_ID2_CTRL0**

Address: Operational Base + offset (0x0510)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id2<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id2<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id2<br>Enable dma transport id2.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_align_id2<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id2<br>Select command mode for id2.<br>1'b0: Not command mode<br>1'b1: Command mode |
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id2<br>If sw_mipi0_on_hdr_mode_id2=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id2=1, id2 channel will capture the line which line count value equal to 1. |
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id2<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 21:20 | RW | 0x0 | sw_hdr_mode_id2<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id2<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id2<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id2<br>Data type for id2. |
| 9:8 | RW | 0x0 | sw_vc_id2<br>Virtual channel for id2. |
| 7:5 | RW | 0x0 | sw_wrddr_type_id2<br>The write ddr type of id2.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id2<br>Enable to crop for id2.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RW | 0x0 | sw_parse_type_id2<br>The parse type of id2.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |
| 0 | RW | 0x0 | sw_cap_en_id2<br>Enable to capture id2.<br>1'b0: Disable<br>1'b1: Enable |

Copyright 2022 © Rockchip Electronics Co., Ltd.

**VICAP_MIPI4_ID2_CTRL1**

Address: Operational Base + offset (0x0514)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_height_id2<br>Height for id2. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_width_id2<br>Width for id2. If sw_wrddr_type is rgb888, then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id2 is enable the width value must be 4 aligned. |

**VICAP_MIPI4_ID3_CTRL0**

Address: Operational Base + offset (0x0518)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id3<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id3<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id3<br>Enable dma transport id3.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_align_id3<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id3<br>Select command mode for id3.<br>1'b0: Not command mode<br>1'b1: Command mode |
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id3<br>If sw_mipi0_on_hdr_mode_id3=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id3=1, id3 channel will capture the line which line count value equal to 1. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id3<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |
| 21:20 | RW | 0x0 | sw_hdr_mode_id3<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id3<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id3<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id3<br>Data type for id3. |
| 9:8 | RW | 0x0 | sw_vc_id3<br>Virtual channel for id3. |
| 7:5 | RW | 0x0 | sw_wrddr_type_id3<br>The write ddr type of id3.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id3<br>Enable to crop for id3.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RW | 0x0 | sw_parse_type_id3<br>The parse type of id3.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | sw_cap_en_id3<br>Enable to capture id3.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI4_ID3_CTRL1**

Address: Operational Base + offset (0x051C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_height_id3<br>Height for id3. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_width_id3<br>Width for id3. If sw_wrddr_type is rgb888, then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id3 is enable the width value must be 4 aligned. |

**VICAP_MIPI4_CTRL**

Address: Operational Base + offset (0x0520)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:18 | RW | 0x0 | sw_soft_rst_mode<br>2'b00: Soft reset and protect toisp path frame integrity;<br>2'b01: Soft reset and protect toisp path frame integrity and pull down sw_cap_en automatically;<br>2'b10: Soft reset directly;<br>2'b11: Reserved. |
| 17 | RW | 0x0 | sw_soft_rst<br>1'b0: Not reset<br>1'b1: Reset the VICAP MIPI2 path(except MMU/AXI MASTER/REG FILE) |
| 16 | RW | 0x0 | sw_dma_rst<br>Write 1 will reset VICAP MIPI2 path dma.<br>When this bit change to 0,dma is reseted completely. |
| 15:13 | RW | 0x0 | sw_press_value<br>Press value. |
| 12 | RW | 0x0 | sw_press_en<br>1'b0: Disable press<br>1'b1: Enable press |
| 11:8 | RO | 0x0 | reserved |
| 7:5 | RW | 0x0 | sw_hurry_value<br>Hurry value. |
| 4 | RW | 0x0 | sw_hurry_en<br>1'b0: Disable hurry<br>1'b1: Enable hurry |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3 | RO | 0x0 | reserved |
| 2:1 | RW | 0x0 | sw_water_line<br>2'b00: 75%<br>2'b01: 50%<br>2'b10: 25%<br>2'b11: 0% |
| 0 | RW | 0x0 | sw_cap_en<br>1'b0: Disable capture all id<br>1'b1: Enable capture all id. |

**VICAP_MIPI4_FRAME0_ADDR_Y_ID0**

Address: Operational Base + offset (0x0524)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id0<br>First address of even frame for ID0 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI4_FRAME1_ADDR_Y_ID0**

Address: Operational Base + offset (0x0528)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id0<br>First address of odd frame for ID0 Y path(must be aligned to double word). |

**VICAP_MIPI4_FRAME0_ADDR_UV_ID0**

Address: Operational Base + offset (0x052C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id0<br>First address of even frame for ID0 UV path(must be aligned to double word). |

**VICAP_MIPI4_FRAME1_ADDR_UV_ID0**

Address: Operational Base + offset (0x0530)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id0<br>First address of odd frame for ID0 UV path(must be aligned to double word). |

**VICAP_MIPI4_VLW_ID0**

Address: Operational Base + offset (0x0534)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_id0<br>Virtual line width of even frame for ID0 path(must be aligned to double word). |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**VICAP_MIPI4_FRAME0_ADDR_Y_ID1**

Address: Operational Base + offset (0x0538)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id1<br>First address of even frame for ID1 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI4_FRAME1_ADDR_Y_ID1**

Address: Operational Base + offset (0x053C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id1<br>First address of odd frame for ID1 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI4_FRAME0_ADDR_UV_ID1**

Address: Operational Base + offset (0x0540)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id1<br>First address of even frame for ID1 UV path(must be aligned to double word). |

**VICAP_MIPI4_FRAME1_ADDR_UV_ID1**

Address: Operational Base + offset (0x0544)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id1<br>First address of odd frame for ID1 UV path(must be aligned to double word). |

**VICAP_MIPI4_VLW_ID1**

Address: Operational Base + offset (0x0548)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_id1<br>Virtual line width of even frame for ID1 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI4_FRAME0_ADDR_Y_ID2**

Address: Operational Base + offset (0x054C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id2<br>First address of even frame for ID2 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI4_FRAME1_ADDR_Y_ID2**

Address: Operational Base + offset (0x0550)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id2<br>First address of odd frame for ID2 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI4_FRAME0_ADDR_UV_ID2**

Address: Operational Base + offset (0x0554)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id2<br>First address of even frame for ID2 UV path(must be aligned to double word). |

**VICAP_MIPI4_FRAME1_ADDR_UV_ID2**

Address: Operational Base + offset (0x0558)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id0<br>First address of odd frame for ID2 UV path(must be aligned to double word). |

**VICAP_MIPI4_VLW_ID2**

Address: Operational Base + offset (0x055C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_id2<br>Virtual line width of even frame for ID2 path(must be aligned to double word). |

**VICAP_MIPI4_FRAME0_ADDR_Y_ID3**

Address: Operational Base + offset (0x0560)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id3<br>First address of even frame for ID3 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI4_FRAME1_ADDR_Y_ID3**

Address: Operational Base + offset (0x0564)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id3<br>First address of odd frame for ID3 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI4_FRAME0_ADDR_UV_ID3**

Address: Operational Base + offset (0x0568)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id3<br>First address of even frame for ID3 UV path(must be aligned to double word). |

**VICAP_MIPI4_FRAME1_ADDR_UV_ID3**

Address: Operational Base + offset (0x056C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id3<br>First address of odd frame for ID3 UV path(must be aligned to double word). |

**VICAP_MIPI4_VLW_ID3**

Address: Operational Base + offset (0x0570)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_id3<br>Virtual line width of even frame for ID3 path(must be aligned to double word). |

**VICAP_MIPI4_INTEN**

Address: Operational Base + offset (0x0574)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27 | RW | 0x0 | size_err_id3_inten<br>1'b0: Disable<br>1'b1: Enable |
| 26 | RW | 0x0 | size_err_id2_inten<br>1'b0: Disable<br>1'b1: Enable |
| 25 | RW | 0x0 | size_err_id1_inten<br>1'b0: Disable<br>1'b1: Enable |
| 24 | RW | 0x0 | size_err_id0_inten<br>1'b0: Disable<br>1'b1: Enable |
| 23 | RW | 0x0 | line_id3_inten<br>1'b0: Disable<br>1'b1: Enable |
| 22 | RW | 0x0 | line_id2_inten<br>1'b0: Disable<br>1'b1: Enable |
| 21 | RW | 0x0 | line_id1_inten<br>1'b0: Disable<br>1'b1: Enable |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 20 | RW | 0x0 | line_id0_inten<br>1'b0: Disable<br>1'b1: Enable |
| 19 | RW | 0x0 | csi2rx_fifo_overflow_inten<br>1'b0: Disable<br>1'b1: Enable |
| 18 | RW | 0x0 | bandwidth_lack_inten<br>1'b0: Disable<br>1'b1: Enable |
| 17 | RW | 0x0 | dma_uv_fifo_overflow_inten<br>Enable the interrupt of dma fifo overflow of MIPI uv path or LVDS id1 path.<br>1'b0: Disable<br>1'b1: Enable |
| 16 | RW | 0x0 | dma_y_fifo_overflow_inten<br>Enable the interrupt of dma fifo overflow of MIPI y path or LVDS id0 path.<br>1'b0: Disable<br>1'b1: Enable |
| 15 | RW | 0x0 | frame1_dma_end_id3_inten<br>Enable the interrupt of end of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | frame0_dma_end_id3_inten<br>Enable the interrupt of end of even frame for ID3.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | frame1_dma_end_id2_inten<br>Enable the interrupt of end of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | frame0_dma_end_id2_inten<br>Enable the interrupt of end of even frame for ID2.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | frame1_dma_end_id1_inten<br>Enable the interrupt of end of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | frame0_dma_end_id1_inten<br>Enable the interrupt of end of even frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 9 | RW | 0x0 | frame1_dma_end_id0_inten<br>Enable the interrupt of end of odd frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | frame0_dma_end_id0_inten<br>Enable the interrupt of end of even frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | frame1_start_id3_inten<br>Enable the interrupt of start of odd frame for ID3.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | frame0_start_id3_inten<br>Enable the interrupt of start of even frame for ID3.<br>1'b0: Disable<br>1'b1: Enable |
| 5 | RW | 0x0 | frame1_start_id2_inten<br>Enable the interrupt of start of odd frame for ID2.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | frame0_start_id2_inten<br>Enable the interrupt of start of even frame for ID2.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | frame1_start_id1_inten<br>Enable the interrupt of start of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | frame0_start_id1_inten<br>Enable the interrupt of start of even frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | frame1_start_id0_inten<br>Enable the interrupt of start of odd frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | frame0_start_id0_inten<br>Enable the interrupt of start of even frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI4_INTSTAT**

Address: Operational Base + offset (0x0578)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 27 | W1C | 0x0 | size_err_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 26 | W1C | 0x0 | size_err_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 25 | W1C | 0x0 | size_err_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 24 | W1C | 0x0 | size_err_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 23 | W1C | 0x0 | line_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 22 | W1C | 0x0 | line_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 21 | W1C | 0x0 | line_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 20 | W1C | 0x0 | line_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 19 | W1C | 0x0 | csi2rx_fifo_overflow_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 18 | W1C | 0x0 | bandwidth_lack_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 17 | W1C | 0x0 | dma_uv_fifo_overflow_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 16 | W1C | 0x0 | dma_y_fifo_overflow_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 15 | W1C | 0x0 | frame1_dma_end_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 14 | W1C | 0x0 | frame0_dma_end_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 13 | W1C | 0x0 | frame1_dma_end_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 12 | W1C | 0x0 | frame0_dma_end_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 11 | W1C | 0x0 | frame1_dma_end_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 10 | W1C | 0x0 | frame0_dma_end_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 9 | W1C | 0x0 | frame1_dma_end_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 8 | W1C | 0x0 | frame0_dma_end_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 7 | W1C | 0x0 | frame1_start_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 6 | W1C | 0x0 | frame0_start_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 5 | W1C | 0x0 | frame1_start_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 4 | W1C | 0x0 | frame0_start_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 3 | W1C | 0x0 | frame1_start_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 2 | W1C | 0x0 | frame0_start_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 1 | W1C | 0x0 | frame1_start_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 0 | W1C | 0x0 | frame0_start_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |

**VICAP_MIPI4_LINE_INT_NUM_ID0_1**

Address: Operational Base + offset (0x057C)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | line_int_mode_id1<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0040 | line_int_num_id1<br>For one-time mode, if line_int_num_id1=100, then channel 1 receive 100th line, the line_id1_intst will be 1.<br>For circular mode, if line_int_num_id1=100, then channel 1 receive 100th line200th line300th line.....the line_id1_intst will be 1. |
| 15 | RW | 0x0 | line_int_mode_id0<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0040 | line_int_num_id0<br>For one-time mode, if line_int_num_id0=100, then channel 0 receive 100th line, the line_id0_intst will be 1.<br>For circular mode, if line_int_num_id0=100, then channel 0 receive 100th line200th line300th line.....the line_id0_intst will be 1. |

**VICAP_MIPI4_LINE_INT_NUM_ID2_3**

Address: Operational Base + offset (0x0580)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | line_int_mode_id3<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0040 | line_int_num_id3<br>For one-time mode, if line_int_num_id3=100, then channel 3 receive 100th line, the line_id3_intst will be 1.<br>For circular mode ,if line_int_num_id3=100, then channel 3 receive 100th line200th line300th line.....the line_id3_intst will be 1. |
| 15 | RW | 0x0 | line_int_mode_id2<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0040 | line_int_num_id2<br>For one-time mode, if line_int_num_id2=100, then channel 2 receive 100th line, the line_id2_intst will be 1.<br>For circular mode, if line_int_num_id2=100, then channel 2 receive 100th line200th line300th line.....the line_id2_intst will be 1. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**VICAP_MIPI4_LINE_CNT_ID0_1**

Address: Operational Base + offset (0x0584)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_cnt_id1<br>Current line count for id1. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_line_cnt_id0<br>Current line count for id0. |

**VICAP_MIPI4_LINE_CNT_ID2_3**

Address: Operational Base + offset (0x0588)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_cnt_id3<br>Current line count for id3. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_line_cnt_id2<br>Current line count for id2. |

**VICAP_MIPI4_ID0_CROP_START**

Address: Operational Base + offset (0x058C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id0<br>The start y coordinate for id0. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id0<br>The start x coordinate for id0, if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI4_ID1_CROP_START**

Address: Operational Base + offset (0x0590)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id1<br>The start y coordinate for id1. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id1<br>The start x coordinate for id1, if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI4_ID2_CROP_START**

Address: Operational Base + offset (0x0594)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id2<br>The start y coordinate for id2. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id2<br>The start x coordinate for id2, if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI4_ID3_CROP_START**

Address: Operational Base + offset (0x0598)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id3<br>The start y coordinate for id3. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id3<br>The start x coordinate for id3, if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI4_FRAME_NUM_VC0**

Address: Operational Base + offset (0x059C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc0<br>The frame number of frame end of virtual channel 0. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc0<br>The frame number of frame start of virtual channel 0. |

**VICAP_MIPI4_FRAME_NUM_VC1**

Address: Operational Base + offset (0x05A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc1<br>The frame number of frame end of virtual channel 1. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc1<br>The frame number of frame start of virtual channel 1. |

**VICAP_MIPI4_FRAME_NUM_VC2**

Address: Operational Base + offset (0x05A4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc2<br>The frame number of frame end of virtual channel 2. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc2<br>The frame number of frame start of virtual channel 2. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**VICAP_MIPI4_FRAME_NUM_VC3**

Address: Operational Base + offset (0x05A8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc3<br>The frame number of frame end of virtual channel 3. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc3<br>The frame number of frame start of virtual channel 3. |

**VICAP_MIPI4_ID0_EFFECT_CODE**

Address: Operational Base + offset (0x05AC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id0<br>Effect code of id0 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id0<br>Effect code of id0 for sony sensor. |

**VICAP_MIPI4_ID1_EFFECT_CODE**

Address: Operational Base + offset (0x05B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id1<br>Effect code of id1 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id1<br>Effect code of id1 for sony sensor. |

**VICAP_MIPI4_ID2_EFFECT_CODE**

Address: Operational Base + offset (0x05B4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id2<br>Effect code of id2 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id2<br>Effect code of id2 for sony sensor. |

**VICAP_MIPI4_ID3_EFFECT_CODE**

Address: Operational Base + offset (0x05B8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id3<br>Effect code of id3 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id3<br>Effect code of id3 for sony sensor. |

**VICAP_MIPI4_ON_PAD_VALUE**

Address: Operational Base + offset (0x05BC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RO | 0x00000 | reserved |
| 13:0 | RW | 0x0000 | sw_on_pad_value<br>Padding value for ON sensor. |

**VICAP_MIPI4_SIZE_NUM_ID0**

Address: Operational Base + offset (0x05C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_num_id0<br>The id0 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id0<br>The id0 pixel number in one line. |

**VICAP_MIPI4_SIZE_NUM_ID1**

Address: Operational Base + offset (0x05C4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_num_id1<br>The id1 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id1<br>The id1 pixel number in one line. |

**VICAP_MIPI4_SIZE_NUM_ID2**

Address: Operational Base + offset (0x05C8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_num_id2<br>The id2 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id2<br>The id2 pixel number in one line. |

**VICAP_MIPI4_SIZE_NUM_ID3**

Address: Operational Base + offset (0x05CC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 29:16 | RO | 0x0000 | ro_line_num_id3<br>The id3 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id3<br>The id3 pixel number in one line. |

**VICAP_MIPI5_ID0_CTRL0**

Address: Operational Base + offset (0x0600)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id0<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id0<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id0<br>Enable dma transport id0.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_align_id0<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id0<br>Select command mode for id0.<br>1'b0: Not command mode<br>1'b1: Command mode |
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id0<br>If sw_mipi0_on_hdr_mode_id0=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id0=1, id0 channel will capture the line which line count value equal to 1. |
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id0<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 21:20 | RW | 0x0 | sw_hdr_mode_id0<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id0<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id0<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id0<br>Data type for id0. |
| 9:8 | RW | 0x0 | sw_vc_id0<br>Virtual channel for id0. |
| 7:5 | RW | 0x0 | sw_wrddr_type_id0<br>The write ddr type of id0.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id0<br>Enable to crop for id0.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RW | 0x0 | sw_parse_type_id0<br>The parse type of id0.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |
| 0 | RW | 0x0 | sw_cap_en_id0<br>Enable to capture id0.<br>1'b0: Disable<br>1'b1: Enable |

Copyright 2022 © Rockchip Electronics Co., Ltd.

**VICAP_MIPI5_ID0_CTRL1**

Address: Operational Base + offset (0x0604)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_height_id0<br>Height for id0. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_width_id0<br>Width for id0. If sw_wrddr_type is rgb888, then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id0 is enable the width value must be 4 aligned. |

**VICAP_MIPI5_ID1_CTRL0**

Address: Operational Base + offset (0x0608)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id1<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id1<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00. And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id1<br>Enable dma transport id1.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_align_id1<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id1<br>Select command mode for id1.<br>1'b0: Not command mode<br>1'b1: Command mode |
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id1<br>If sw_mipi0_on_hdr_mode_id1=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id1=1, id1 channel will capture the line which line count value equal to 1. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id1<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |
| 21:20 | RW | 0x0 | sw_hdr_mode_id1<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id1<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id1<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id1<br>Data type for id1. |
| 9:8 | RW | 0x0 | sw_vc_id1<br>Virtual channel for id1. |
| 7:5 | RW | 0x0 | sw_wrddr_type_id1<br>The write ddr type of id1.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id1<br>Enable to crop for id1.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RW | 0x0 | sw_parse_type_id1<br>The parse type of id1.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | sw_cap_en_id1<br>Enable to capture id1.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI5_ID1_CTRL1**

Address: Operational Base + offset (0x060C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_height_id1<br>Height for id1. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_width_id1<br>Width for id1. If sw_wrddr_type is rgb888, then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id1 is enable the width value must be 4 aligned. |

**VICAP_MIPI5_ID2_CTRL0**

Address: Operational Base + offset (0x0610)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id2<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id2<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00.<br>And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id2<br>Enable dma transport id2.<br>1'b0: Disable<br>1'b1: Enable |
| 27 | RW | 0x0 | sw_align_id2<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id2<br>Select command mode for id2.<br>1'b0: Not command mode<br>1'b1: Command mode |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id2<br>If sw_mipi0_on_hdr_mode_id2=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id2=1, id2 channel will capture the line which line count value equal to 1. |
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id2<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |
| 21:20 | RW | 0x0 | sw_hdr_mode_id2<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id2<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id2<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id2<br>Data type for id2. |
| 9:8 | RW | 0x0 | sw_vc_id2<br>Virtual channel for id2. |
| 7:5 | RW | 0x0 | sw_wrddr_type_id2<br>The write ddr type of id2.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id2<br>Enable to crop for id2.<br>1'b0: Disable<br>1'b1: Enable |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 3:1 | RW | 0x0 | sw_parse_type_id2<br>The parse type of id2.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |
| 0 | RW | 0x0 | sw_cap_en_id2<br>Enable to capture id2.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI5_ID2_CTRL1**

Address: Operational Base + offset (0x0614)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_height_id2<br>Height for id2. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_width_id2<br>Width for id2.if sw_wrddr_type is rgb888, then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id2 is enable the width value must be 4 aligned. |

**VICAP_MIPI5_ID3_CTRL0**

Address: Operational Base + offset (0x0618)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RW | 0x0 | sw_vc_hdr_id_main_id3<br>The id that is the first coming.<br>Note: This register is available when sw_hdr_mode_idx=2'b00 and sw_vc_hdr_protect=1'b1. |
| 29 | RW | 0x0 | sw_vc_hdr_protect_id3<br>1'b0: Not ensure hdr long exposure frame is captured firstly;<br>1'b1: Ensure hdr long exposure frame is captured firstly.<br>Note: This register is available when sw_hdr_mode_idx=2'b00.<br>And sw_vc_hdr_id_main must be configured correctly(the first coming id). |
| 28 | RW | 0x0 | sw_dma_en_id3<br>Enable dma transport id3.<br>1'b0: Disable<br>1'b1: Enable |

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 27 | RW | 0x0 | sw_align_id3<br>1'b0: Low alignment(raw10/12 will in [9:0]/[11:0])<br>1'b1: High alignment(raw10/12 will in [15:6]/[15:4]<br>Only be used when non-compacted mode. |
| 26 | RW | 0x0 | sw_command_mode_en_id3<br>Select command mode for id3.<br>1'b0: Not command mode<br>1'b1: Command mode |
| 25:24 | RW | 0x0 | sw_on_hdr_line_cnt_id3<br>If sw_mipi0_on_hdr_mode_id3=1(2), the line count value will circulate between 0~1(2). And if sw_mipi0_on_hdr_line_cnt_id3=1, id3 channel will capture the line which line count value equal to 1. |
| 23:22 | RW | 0x0 | sw_on_hdr_mode_id3<br>2'b00: Normal mode(no HDR)<br>2'b01: 2 frames HDR<br>2'b10: 3 frames HDR<br>2'b11: Reserved |
| 21:20 | RW | 0x0 | sw_hdr_mode_id3<br>2'b00: HDR distinguished by virtual channel<br>2'b01: HDR distinguished by line number(ON HDR mode)<br>2'b10: HDR distinguished by first 4pixel(SONY HDR mode)<br>2'b11: Reserved |
| 19:18 | RW | 0x0 | sw_yuyv_out_order_id3<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 17:16 | RW | 0x0 | sw_yuyv_in_order_id3<br>2'b00: UYVY(CSI-2 standard)<br>2'b01: VYUY<br>2'b10: YUYV<br>2'b11: YVYU |
| 15:10 | RW | 0x00 | sw_dt_id3<br>Data type for id3. |
| 9:8 | RW | 0x0 | sw_vc_id3<br>Virtual channel for id3. |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:5 | RW | 0x0 | sw_wrddr_type_id3<br>The write ddr type of id3.<br>3'b000: Raw-compact<br>3'b001: Raw-uncompact<br>3'b010: YUV packet<br>3'b011: YUV 400<br>3'b100: YUV 422sp<br>3'b101: YUV 420sp<br>Others: Reserved |
| 4 | RW | 0x0 | sw_crop_en_id3<br>Enable to crop for id3.<br>1'b0: Disable<br>1'b1: Enable |
| 3:1 | RW | 0x0 | sw_parse_type_id3<br>The parse type of id3.<br>3'b000: For raw8/rgb888<br>3'b001: For raw10<br>3'b010: For raw12<br>3'b011: For raw14(data will be clipped to 12bit)<br>3'b100: For yuv422 8bit<br>Others: Reserved |
| 0 | RW | 0x0 | sw_cap_en_id3<br>Enable to capture id3.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI5_ID3_CTRL1**

Address: Operational Base + offset (0x061C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_height_id3<br>Height for id3. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_width_id3<br>Width for id3.if sw_wrddr_type is rgb888, then the width is equal to the number of bytes(not pixel).<br>If sw_crop_en_id3 is enable the width value must be 4 aligned. |

**VICAP_MIPI5_CTRL**

Address: Operational Base + offset (0x0620)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19:18 | RW | 0x0 | sw_soft_rst_mode<br>2'b00: Soft reset and protect toisp path frame integrity;<br>2'b01: Soft reset and protect toisp path frame integrity and pull down sw_cap_en automatically;<br>2'b10: Soft reset directly;<br>2'b11: Reserved. |
| 17 | RW | 0x0 | sw_soft_rst<br>1'b0: Not reset<br>1'b1: Reset the VICAP MIPI3 path(except MMU/AXI MASTER/REG FILE) |
| 16 | RW | 0x0 | sw_dma_rst<br>Write 1 will reset VICAP MIPI3 path dma.<br>When this bit change to 0,dma is reseted completely. |
| 15:13 | RW | 0x0 | sw_press_value<br>Press value. |
| 12 | RW | 0x0 | sw_press_en<br>1'b0: Disable press<br>1'b1: Enable press |
| 11:8 | RO | 0x0 | reserved |
| 7:5 | RW | 0x0 | sw_hurry_value<br>Hurry value. |
| 4 | RW | 0x0 | sw_hurry_en<br>1'b0: Disable hurry<br>1'b1: Enable hurry |
| 3 | RO | 0x0 | reserved |
| 2:1 | RW | 0x0 | sw_water_line<br>2'b00: 75%<br>2'b01: 50%<br>2'b10: 25%<br>2'b11: 0% |
| 0 | RW | 0x0 | sw_cap_en<br>1'b0: Disable capture all id<br>1'b1: Enable capture all id. |

**VICAP_MIPI5_FRAME0_ADDR_Y_ID0**

Address: Operational Base + offset (0x0624)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id0<br>First address of even frame for ID0 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI5_FRAME1_ADDR_Y_ID0**

Address: Operational Base + offset (0x0628)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id0<br>First address of odd frame for ID0 Y path(must be aligned to double word). |

**VICAP_MIPI5_FRAME0_ADDR_UV_ID0**

Address: Operational Base + offset (0x062C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id0<br>First address of even frame for ID0 UV path(must be aligned to double word). |

**VICAP_MIPI5_FRAME1_ADDR_UV_ID0**

Address: Operational Base + offset (0x0630)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id0<br>First address of odd frame for ID0 UV path(must be aligned to double word). |

**VICAP_MIPI5_VLW_ID0**

Address: Operational Base + offset (0x0634)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_id0<br>Virtual line width of even frame for ID0 path(must be aligned to double word). |

**VICAP_MIPI5_FRAME0_ADDR_Y_ID1**

Address: Operational Base + offset (0x0638)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id1<br>First address of even frame for ID1 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI5_FRAME1_ADDR_Y_ID1**

Address: Operational Base + offset (0x063C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id1<br>First address of odd frame for ID1 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI5_FRAME0_ADDR_UV_ID1**

Address: Operational Base + offset (0x0640)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id1<br>First address of even frame for ID1 UV path(must be aligned to double word). |

**VICAP_MIPI5_FRAME1_ADDR_UV_ID1**

Address: Operational Base + offset (0x0644)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id1<br>First address of odd frame for ID1 UV path(must be aligned to double word). |

**VICAP_MIPI5_VLW_ID1**

Address: Operational Base + offset (0x0648)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_id1<br>Virtual line width of even frame for ID1 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI5_FRAME0_ADDR_Y_ID2**

Address: Operational Base + offset (0x064C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id2<br>First address of even frame for ID2 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI5_FRAME1_ADDR_Y_ID2**

Address: Operational Base + offset (0x0650)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id2<br>First address of odd frame for ID2 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI5_FRAME0_ADDR_UV_ID2**

Address: Operational Base + offset (0x0654)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id2<br>First address of even frame for ID2 UV path(must be aligned to double word). |

**VICAP_MIPI5_FRAME1_ADDR_UV_ID2**

Address: Operational Base + offset (0x0658)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id0<br>First address of odd frame for ID2 UV path(must be aligned to double word). |

**VICAP_MIPI5_VLW_ID2**

Address: Operational Base + offset (0x065C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_id2<br>Virtual line width of even frame for ID2 path(must be aligned to double word). |

**VICAP_MIPI5_FRAME0_ADDR_Y_ID3**

Address: Operational Base + offset (0x0660)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_y_id3<br>First address of even frame for ID3 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI5_FRAME1_ADDR_Y_ID3**

Address: Operational Base + offset (0x0664)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_y_id3<br>First address of odd frame for ID3 Y/RAW/RGB path(must be aligned to double word). |

**VICAP_MIPI5_FRAME0_ADDR_UV_ID3**

Address: Operational Base + offset (0x0668)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_uv_id3<br>First address of even frame for ID3 UV path(must be aligned to double word). |

**VICAP_MIPI5_FRAME1_ADDR_UV_ID3**

Address: Operational Base + offset (0x066C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_uv_id3<br>First address of odd frame for ID3 UV path(must be aligned to double word). |

**VICAP_MIPI5_VLW_ID3**

Address: Operational Base + offset (0x0670)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 19:0 | RW | 0x00000 | sw_vlw_id3<br>Virtual line width of even frame for ID3 path(must be aligned to double word). |

**VICAP_MIPI5_INTEN**

Address: Operational Base + offset (0x0674)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27 | RW | 0x0 | size_err_id3_inten<br>1'b0: Disable<br>1'b1: Enable |
| 26 | RW | 0x0 | size_err_id2_inten<br>1'b0: Disable<br>1'b1: Enable |
| 25 | RW | 0x0 | size_err_id1_inten<br>1'b0: Disable<br>1'b1: Enable |
| 24 | RW | 0x0 | size_err_id0_inten<br>1'b0: Disable<br>1'b1: Enable |
| 23 | RW | 0x0 | line_id3_inten<br>1'b0: Disable<br>1'b1: Enable |
| 22 | RW | 0x0 | line_id2_inten<br>1'b0: Disable<br>1'b1: Enable |
| 21 | RW | 0x0 | line_id1_inten<br>1'b0: Disable<br>1'b1: Enable |
| 20 | RW | 0x0 | line_id0_inten<br>1'b0: Disable<br>1'b1: Enable |
| 19 | RW | 0x0 | csi2rx_fifo_overflow_inten<br>1'b0: Disable<br>1'b1: Enable |
| 18 | RW | 0x0 | bandwidth_lack_inten<br>1'b0: Disable<br>1'b1: Enable |
| 17 | RW | 0x0 | dma_uv_fifo_overflow_inten<br>Enable the interrupt of dma fifo overflow of MIPI uv path or LVDS id1 path.<br>1'b0: Disable<br>1'b1: Enable |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 16 | RW | 0x0 | dma_y_fifo_overflow_inten<br>Enable the interrupt of dma fifo overflow of MIPI y path or LVDS id0 path.<br>1'b0: Disable<br>1'b1: Enable |
| 15 | RW | 0x0 | frame1_dma_end_id3_inten<br>Enable the interrupt of end of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 14 | RW | 0x0 | frame0_dma_end_id3_inten<br>Enable the interrupt of end of even frame for ID3.<br>1'b0: Disable<br>1'b1: Enable |
| 13 | RW | 0x0 | frame1_dma_end_id2_inten<br>Enable the interrupt of end of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 12 | RW | 0x0 | frame0_dma_end_id2_inten<br>Enable the interrupt of end of even frame for ID2.<br>1'b0: Disable<br>1'b1: Enable |
| 11 | RW | 0x0 | frame1_dma_end_id1_inten<br>Enable the interrupt of end of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 10 | RW | 0x0 | frame0_dma_end_id1_inten<br>Enable the interrupt of end of even frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 9 | RW | 0x0 | frame1_dma_end_id0_inten<br>Enable the interrupt of end of odd frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |
| 8 | RW | 0x0 | frame0_dma_end_id0_inten<br>Enable the interrupt of end of even frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |
| 7 | RW | 0x0 | frame1_start_id3_inten<br>Enable the interrupt of start of odd frame for ID3.<br>1'b0: Disable<br>1'b1: Enable |
| 6 | RW | 0x0 | frame0_start_id3_inten<br>Enable the interrupt of start of even frame for ID3.<br>1'b0: Disable<br>1'b1: Enable |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RW | 0x0 | frame1_start_id2_inten<br>Enable the interrupt of start of odd frame for ID2.<br>1'b0: Disable<br>1'b1: Enable |
| 4 | RW | 0x0 | frame0_start_id2_inten<br>Enable the interrupt of start of even frame for ID2.<br>1'b0: Disable<br>1'b1: Enable |
| 3 | RW | 0x0 | frame1_start_id1_inten<br>Enable the interrupt of start of odd frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 2 | RW | 0x0 | frame0_start_id1_inten<br>Enable the interrupt of start of even frame for ID1.<br>1'b0: Disable<br>1'b1: Enable |
| 1 | RW | 0x0 | frame1_start_id0_inten<br>Enable the interrupt of start of odd frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | frame0_start_id0_inten<br>Enable the interrupt of start of even frame for ID0.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_MIPI5_INTSTAT**

Address: Operational Base + offset (0x0678)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:28 | RO | 0x0 | reserved |
| 27 | W1C | 0x0 | size_err_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 26 | W1C | 0x0 | size_err_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 25 | W1C | 0x0 | size_err_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 24 | W1C | 0x0 | size_err_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 23 | W1C | 0x0 | line_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 22 | W1C | 0x0 | line_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 21 | W1C | 0x0 | line_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 20 | W1C | 0x0 | line_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 19 | W1C | 0x0 | csi2rx_fifo_overflow_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 18 | W1C | 0x0 | bandwidth_lack_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 17 | W1C | 0x0 | dma_uv_fifo_overflow_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 16 | W1C | 0x0 | dma_y_fifo_overflow_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 15 | W1C | 0x0 | frame1_dma_end_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 14 | W1C | 0x0 | frame0_dma_end_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 13 | W1C | 0x0 | frame1_dma_end_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 12 | W1C | 0x0 | frame0_dma_end_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 11 | W1C | 0x0 | frame1_dma_end_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 10 | W1C | 0x0 | frame0_dma_end_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 9 | W1C | 0x0 | frame1_dma_end_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 8 | W1C | 0x0 | frame0_dma_end_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | W1C | 0x0 | frame1_start_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 6 | W1C | 0x0 | frame0_start_id3_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 5 | W1C | 0x0 | frame1_start_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 4 | W1C | 0x0 | frame0_start_id2_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 3 | W1C | 0x0 | frame1_start_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 2 | W1C | 0x0 | frame0_start_id1_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 1 | W1C | 0x0 | frame1_start_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |
| 0 | W1C | 0x0 | frame0_start_id0_intst<br>1'b0: No interrupt<br>1'b1: Interrupt |

**VICAP_MIPI5_LINE_INT_NUM_ID0_1**

Address: Operational Base + offset (0x067C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | line_int_mode_id1<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0040 | line_int_num_id1<br>For one-time mode, if line_int_num_id1=100, then channel 1 receive 100th line, the line_id1_intst will be 1.<br>For circular mode, if line_int_num_id1=100, then channel 1 receive 100th line200th line300th line.....the line_id1_intst will be 1. |
| 15 | RW | 0x0 | line_int_mode_id0<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 14 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 13:0 | RW | 0x0040 | line_int_num_id0<br>For one-time mode, if line_int_num_id0=100, then channel 0 receive 100th line, the line_id0_intst will be 1.<br>For circular mode, if line_int_num_id0=100, then channel 0 receive 100th line200th line300th line.....the line_id0_intst will be 1. |

**VICAP_MIPI5_LINE_INT_NUM_ID2_3**

Address: Operational Base + offset (0x0680)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | line_int_mode_id3<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0040 | line_int_num_id3<br>For one-time mode, if line_int_num_id3=100, then channel 3 receive 100th line, the line_id3_intst will be 1.<br>For circular mode, if line_int_num_id3=100, then channel 3 receive 100th line200th line300th line.....the line_id3_intst will be 1. |
| 15 | RW | 0x0 | line_int_mode_id2<br>1'b0: One-time mode<br>1'b1: Circular mode |
| 14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0040 | line_int_num_id2<br>For one-time mode, if line_int_num_id2=100, then channel 2 receive 100th line, the line_id2_intst will be 1.<br>For circular mode, if line_int_num_id2=100, then channel 2 receive 100th line200th line300th line.....the line_id2_intst will be 1. |

**VICAP_MIPI5_LINE_CNT_ID0_1**

Address: Operational Base + offset (0x0684)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_cnt_id1<br>Current line count for id1. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_line_cnt_id0<br>Current line count for id0. |

**VICAP_MIPI5_LINE_CNT_ID2_3**

Address: Operational Base + offset (0x0688)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 29:16 | RO | 0x0000 | ro_line_cnt_id3<br>Current line count for id3. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_line_cnt_id2<br>Current line count for id2. |

**VICAP_MIPI5_ID0_CROP_START**

Address: Operational Base + offset (0x068C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id0<br>The start y coordinate for id0. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id0<br>The start x coordinate for id0, if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI5_ID1_CROP_START**

Address: Operational Base + offset (0x0690)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id1<br>The start y coordinate for id1. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id1<br>The start x coordinate for id1, if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI5_ID2_CROP_START**

Address: Operational Base + offset (0x0694)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id2<br>The start y coordinate for id2. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id2<br>The start x coordinate for id2, if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI5_ID3_CROP_START**

Address: Operational Base + offset (0x0698)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y_id3<br>The start y coordinate for id3. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x_id3<br>The start x coordinate for id3, if sw_wrddr_type is rgb888, then the start x is measured in byte.<br>The start x value must be 4 aligned. |

**VICAP_MIPI5_FRAME_NUM_VC0**

Address: Operational Base + offset (0x069C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc0<br>The frame number of frame end of virtual channel 0. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc0<br>The frame number of frame start of virtual channel 0. |

**VICAP_MIPI5_FRAME_NUM_VC1**

Address: Operational Base + offset (0x06A0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc1<br>The frame number of frame end of virtual channel 1. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc1<br>The frame number of frame start of virtual channel 1. |

**VICAP_MIPI5_FRAME_NUM_VC2**

Address: Operational Base + offset (0x06A4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc2<br>The frame number of frame end of virtual channel 2. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc2<br>The frame number of frame start of virtual channel 2. |

**VICAP_MIPI5_FRAME_NUM_VC3**

Address: Operational Base + offset (0x06A8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | ro_frame_num_end_vc3<br>The frame number of frame end of virtual channel 3. |
| 15:0 | RO | 0x0000 | ro_frame_num_start_vc3<br>The frame number of frame start of virtual channel 3. |

**VICAP_MIPI5_ID0_EFFECT_CODE**

Address: Operational Base + offset (0x06AC)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id0<br>Effect code of id0 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id0<br>Effect code of id0 for sony sensor. |

**VICAP_MIPI5_ID1_EFFECT_CODE**

Address: Operational Base + offset (0x06B0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id1<br>Effect code of id1 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id1<br>Effect code of id1 for sony sensor. |

**VICAP_MIPI5_ID2_EFFECT_CODE**

Address: Operational Base + offset (0x06B4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id2<br>Effect code of id2 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id2<br>Effect code of id2 for sony sensor. |

**VICAP_MIPI5_ID3_EFFECT_CODE**

Address: Operational Base + offset (0x06B8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_sony_effect_code1_id3<br>Effect code of id3 for sony sensor. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_sony_effect_code0_id3<br>Effect code of id3 for sony sensor. |

**VICAP_MIPI5_ON_PAD_VALUE**

Address: Operational Base + offset (0x06BC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RO | 0x00000 | reserved |
| 13:0 | RW | 0x0000 | sw_on_pad_value<br>Padding value for ON sensor. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**VICAP_MIPI5_SIZE_NUM_ID0**

Address: Operational Base + offset (0x06C0)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_num_id0<br>The id0 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id0<br>The id0 pixel number in one line. |

**VICAP_MIPI5_SIZE_NUM_ID1**

Address: Operational Base + offset (0x06C4)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_num_id1<br>The id1 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id1<br>The id1 pixel number in one line. |

**VICAP_MIPI5_SIZE_NUM_ID2**

Address: Operational Base + offset (0x06C8)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_num_id2<br>The id2 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id2<br>The id2 pixel number in one line. |

**VICAP_MIPI5_SIZE_NUM_ID3**

Address: Operational Base + offset (0x06CC)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RO | 0x0000 | ro_line_num_id3<br>The id3 line number in one frame. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RO | 0x0000 | ro_pix_num_id3<br>The id3 pixel number in one line. |

**VICAP_SCL_CH_CTRL**

Address: Operational Base + offset (0x0700)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:27 | RW | 0x00 | sw_scl_mux_ch3<br>5'd0: Select MIPI0 ID0<br>5'd1: Select MIPI0 ID1<br>5'd2: Select MIPI0 ID2<br>5'd3: Select MIPI0 ID3<br>5'd4: Select MIPI1 ID0<br>5'd5: Select MIPI1 ID1<br>5'd6: Select MIPI1 ID2<br>5'd7: Select MIPI1 ID3<br>5'd8: Select MIPI2 ID0<br>5'd9: Select MIPI2 ID1<br>5'd10: Select MIPI2 ID2<br>5'd11: Select MIPI2 ID3<br>5'd12: Select MIPI3 ID0<br>5'd13: Select MIPI3 ID1<br>5'd14: Select MIPI3 ID2<br>5'd15: Select MIPI3 ID3<br>5'd16: Select MIPI4 ID0<br>5'd17: Select MIPI4 ID1<br>5'd18: Select MIPI4 ID2<br>5'd19: Select MIPI4 ID3<br>5'd20: Select MIPI5 ID0<br>5'd21: Select MIPI5 ID1<br>5'd22: Select MIPI5 ID2<br>5'd23: Select MIPI5 ID3<br>5'd24: Select DVP<br>Others: Reserved |
| 26:25 | RW | 0x0 | sw_scl_mode_ch3<br>Scale mode for channel 3.<br>2'b00: 8 times scale<br>2'b01: 16 times scale<br>2'b10: 32 times scale<br>Others: Reserved |
| 24 | RW | 0x0 | sw_scl_en_ch3<br>Enable scale channel3.<br>1'b0: Disable<br>1'b1: Enable |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:19 | RW | 0x00 | sw_scl_mux_ch2<br>5'd0: Select MIPI0 ID0<br>5'd1: Select MIPI0 ID1<br>5'd2: Select MIPI0 ID2<br>5'd3: Select MIPI0 ID3<br>5'd4: Select MIPI1 ID0<br>5'd5: Select MIPI1 ID1<br>5'd6: Select MIPI1 ID2<br>5'd7: Select MIPI1 ID3<br>5'd8: Select MIPI2 ID0<br>5'd9: Select MIPI2 ID1<br>5'd10: Select MIPI2 ID2<br>5'd11: Select MIPI2 ID3<br>5'd12: Select MIPI3 ID0<br>5'd13: Select MIPI3 ID1<br>5'd14: Select MIPI3 ID2<br>5'd15: Select MIPI3 ID3<br>5'd16: Select MIPI4 ID0<br>5'd17: Select MIPI4 ID1<br>5'd18: Select MIPI4 ID2<br>5'd19: Select MIPI4 ID3<br>5'd20: Select MIPI5 ID0<br>5'd21: Select MIPI5 ID1<br>5'd22: Select MIPI5 ID2<br>5'd23: Select MIPI5 ID3<br>5'd24: Select DVP<br>Others: Reserved |
| 18:17 | RW | 0x0 | sw_scl_mode_ch2<br>Scale mode for channel 2.<br>2'b00: 8 times scale<br>2'b01: 16 times scale<br>2'b10: 32 times scale<br>Others: Reserved |
| 16 | RW | 0x0 | sw_scl_en_ch2<br>Enable scale channel2.<br>1'b0: Disable<br>1'b1: Enable |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:11 | RW | 0x00 | sw_scl_mux_ch1<br>5'd0: Select MIPI0 ID0<br>5'd1: Select MIPI0 ID1<br>5'd2: Select MIPI0 ID2<br>5'd3: Select MIPI0 ID3<br>5'd4: Select MIPI1 ID0<br>5'd5: Select MIPI1 ID1<br>5'd6: Select MIPI1 ID2<br>5'd7: Select MIPI1 ID3<br>5'd8: Select MIPI2 ID0<br>5'd9: Select MIPI2 ID1<br>5'd10: Select MIPI2 ID2<br>5'd11: Select MIPI2 ID3<br>5'd12: Select MIPI3 ID0<br>5'd13: Select MIPI3 ID1<br>5'd14: Select MIPI3 ID2<br>5'd15: Select MIPI3 ID3<br>5'd16: Select MIPI4 ID0<br>5'd17: Select MIPI4 ID1<br>5'd18: Select MIPI4 ID2<br>5'd19: Select MIPI4 ID3<br>5'd20: Select MIPI5 ID0<br>5'd21: Select MIPI5 ID1<br>5'd22: Select MIPI5 ID2<br>5'd23: Select MIPI5 ID3<br>5'd24: Select DVP<br>Others: Reserved |
| 10:9 | RW | 0x0 | sw_scl_mode_ch1<br>Scale mode for channel 1.<br>2'b00: 8 times scale<br>2'b01: 16 times scale<br>2'b10: 32 times scale<br>Others: Reserved |
| 8 | RW | 0x0 | sw_scl_en_ch1<br>Enable scale channel1.<br>1'b0: Disable<br>1'b1: Enable |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:3 | RW | 0x00 | sw_scl_mux_ch0<br>5'd0: Select MIPI0 ID0<br>5'd1: Select MIPI0 ID1<br>5'd2: Select MIPI0 ID2<br>5'd3: Select MIPI0 ID3<br>5'd4: Select MIPI1 ID0<br>5'd5: Select MIPI1 ID1<br>5'd6: Select MIPI1 ID2<br>5'd7: Select MIPI1 ID3<br>5'd8: Select MIPI2 ID0<br>5'd9: Select MIPI2 ID1<br>5'd10: Select MIPI2 ID2<br>5'd11: Select MIPI2 ID3<br>5'd12: Select MIPI3 ID0<br>5'd13: Select MIPI3 ID1<br>5'd14: Select MIPI3 ID2<br>5'd15: Select MIPI3 ID3<br>5'd16: Select MIPI4 ID0<br>5'd17: Select MIPI4 ID1<br>5'd18: Select MIPI4 ID2<br>5'd19: Select MIPI4 ID3<br>5'd20: Select MIPI5 ID0<br>5'd21: Select MIPI5 ID1<br>5'd22: Select MIPI5 ID2<br>5'd23: Select MIPI5 ID3<br>5'd24: Select DVP<br>Others: Reserved |
| 2:1 | RW | 0x0 | sw_scl_mode_ch0<br>Scale mode for channel 0.<br>2'b00: 8 times scale<br>2'b01: 16 times scale<br>2'b10: 32 times scale<br>Others: Reserved |
| 0 | RW | 0x0 | sw_scl_en_ch0<br>Enable scale channel0.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_SCL_CTRL**

Address: Operational Base + offset (0x0704)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19 | RW | 0x0 | sw_dma_rst_ch3<br>Write 1 will reset VICAP SCALE channel 3 path dma.<br>When this bit change to 0,dma is reseted completely. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 18 | RW | 0x0 | sw_dma_rst_ch2<br>Write 1 will reset VICAP SCALE channel 2 path dma.<br>When this bit change to 0,dma is reseted completely. |
| 17 | RW | 0x0 | sw_dma_rst_ch1<br>Write 1 will reset VICAP SCALE channel 1 path dma.<br>When this bit change to 0,dma is reseted completely. |
| 16 | RW | 0x0 | sw_dma_rst_ch0<br>Write 1 will reset VICAP SCALE channel 0 path dma.<br>When this bit change to 0,dma is reseted completely. |
| 15:13 | RW | 0x0 | sw_press_value<br>Press value. |
| 12 | RW | 0x0 | sw_press_en<br>1'b0: Disable press<br>1'b1: Enable press |
| 11:8 | RO | 0x0 | reserved |
| 7:5 | RW | 0x0 | sw_hurry_value<br>Hurry value. |
| 4 | RW | 0x0 | sw_hurry_en<br>1'b0: Disable hurry<br>1'b1: Enable hurry |
| 3 | RO | 0x0 | reserved |
| 2:1 | RW | 0x0 | sw_water_line<br>2'b00: 75%<br>2'b01: 50%<br>2'b10: 25%<br>2'b11: 0% |
| 0 | RO | 0x0 | reserved |

**VICAP_SCL_FRAME0_ADDR_CH0**

Address: Operational Base + offset (0x0708)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_ch0<br>First address of even frame for CH0 path(must be aligned to double word). |

**VICAP_SCL_FRAME1_ADDR_CH0**

Address: Operational Base + offset (0x070C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_ch0<br>First address of odd frame for CH0 path(must be aligned to double word). |

**VICAP_SCL_VLW_CH0**

Address: Operational Base + offset (0x0710)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_ch0<br>Virtual line width of even frame for CH0 path(must be aligned to double word). |

**VICAP_SCL_FRAME0_ADDR_CH1**

Address: Operational Base + offset (0x0714)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_ch1<br>First address of even frame for CH1 path(must be aligned to double word). |

**VICAP_SCL_FRAME1_ADDR_CH1**

Address: Operational Base + offset (0x0718)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_ch1<br>First address of odd frame for CH1 path(must be aligned to double word). |

**VICAP_SCL_VLW_CH1**

Address: Operational Base + offset (0x071C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_ch1<br>Virtual line width of even frame for CH1 path(must be aligned to double word). |

**VICAP_SCL_FRAME0_ADDR_CH2**

Address: Operational Base + offset (0x0720)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_ch2<br>First address of even frame for CH2 path(must be aligned to double word). |

**VICAP_SCL_FRAME1_ADDR_CH2**

Address: Operational Base + offset (0x0724)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_ch2<br>First address of odd frame for CH2 path(must be aligned to double word). |

**VICAP_SCL_VLW_CH2**

Address: Operational Base + offset (0x0728)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_ch2<br>Virtual line width of even frame for CH2 path(must be aligned to double word). |

**VICAP_SCL_FRAME0_ADDR_CH3**

Address: Operational Base + offset (0x072C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame0_addr_ch3<br>First address of even frame for CH3 path(must be aligned to double word). |

**VICAP_SCL_FRAME1_ADDR_CH3**

Address: Operational Base + offset (0x0730)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_frame1_addr_ch3<br>First address of odd frame for CH3 path(must be aligned to double word). |

**VICAP_SCL_VLW_CH3**

Address: Operational Base + offset (0x0734)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:0 | RW | 0x00000 | sw_vlw_ch3<br>Virtual line width of even frame for CH3 path(must be aligned to double word). |

**VICAP_SCL_CH0_BLACK_LEVEL**

Address: Operational Base + offset (0x0738)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | sw_scl_ch0_black_11<br>The black level for scale channel0 bayer pattern 11 position. |
| 23:16 | RW | 0x00 | sw_scl_ch0_black_10<br>The black level for scale channel0 bayer pattern 10 position. |
| 15:8 | RW | 0x00 | sw_scl_ch0_black_01<br>The black level for scale channel0 bayer pattern 01 position. |
| 7:0 | RW | 0x00 | sw_scl_ch0_black_00<br>The black level for scale channel0 bayer pattern 00 position. |

**VICAP_SCL_CH1_BLACK_LEVEL**

Address: Operational Base + offset (0x073C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | sw_scl_ch1_black_11<br>The black level for scale channel1 bayer pattern 11 position. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:16 | RW | 0x00 | sw_scl_ch1_black_10<br>The black level for scale channel1 bayer pattern 10 position. |
| 15:8 | RW | 0x00 | sw_scl_ch1_black_01<br>The black level for scale channel1 bayer pattern 01 position. |
| 7:0 | RW | 0x00 | sw_scl_ch1_black_00<br>The black level for scale channel1 bayer pattern 00 position. |

**VICAP_SCL_CH2_BLACK_LEVEL**

Address: Operational Base + offset (0x0740)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | sw_scl_ch2_black_11<br>The black level for scale channel2 bayer pattern 11 position. |
| 23:16 | RW | 0x00 | sw_scl_ch2_black_10<br>The black level for scale channel2 bayer pattern 10 position. |
| 15:8 | RW | 0x00 | sw_scl_ch2_black_01<br>The black level for scale channel2 bayer pattern 01 position. |
| 7:0 | RW | 0x00 | sw_scl_ch2_black_00<br>The black level for scale channel2 bayer pattern 00 position. |

**VICAP_SCL_CH3_BLACK_LEVEL**

Address: Operational Base + offset (0x0744)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:24 | RW | 0x00 | sw_scl_ch3_black_11<br>The black level for scale channel3 bayer pattern 11 position. |
| 23:16 | RW | 0x00 | sw_scl_ch3_black_10<br>The black level for scale channel3 bayer pattern 10 position. |
| 15:8 | RW | 0x00 | sw_scl_ch3_black_01<br>The black level for scale channel3 bayer pattern 01 position. |
| 7:0 | RW | 0x00 | sw_scl_ch3_black_00<br>The black level for scale channel3 bayer pattern 00 position. |

**VICAP_TOISP0_CH_CTRL**

Address: Operational Base + offset (0x0780)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:27 | RO | 0x00 | reserved |
| 26:25 | RW | 0x0 | sw_toisp0_vc_hdr_ch_main<br>Toisp0 vc hdr main channel. |
| 24 | RW | 0x0 | sw_toisp0_vc_hdr_protect<br>Enable toisp0 vc hdr protect.<br>1'b0: Disable<br>1'b1: Enable |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 23:19 | RW | 0x00 | sw_toisp0_mux_ch2<br>5'd0: Select MIPI0 ID0<br>5'd1: Select MIPI0 ID1<br>5'd2: Select MIPI0 ID2<br>5'd3: Select MIPI0 ID3<br>5'd4: Select MIPI1 ID0<br>5'd5: Select MIPI1 ID1<br>5'd6: Select MIPI1 ID2<br>5'd7: Select MIPI1 ID3<br>5'd8: Select MIPI2 ID0<br>5'd9: Select MIPI2 ID1<br>5'd10: Select MIPI2 ID2<br>5'd11: Select MIPI2 ID3<br>5'd12: Select MIPI3 ID0<br>5'd13: Select MIPI3 ID1<br>5'd14: Select MIPI3 ID2<br>5'd15: Select MIPI3 ID3<br>5'd16: Select MIPI4 ID0<br>5'd17: Select MIPI4 ID1<br>5'd18: Select MIPI4 ID2<br>5'd19: Select MIPI4 ID3<br>5'd20: Select MIPI5 ID0<br>5'd21: Select MIPI5 ID1<br>5'd22: Select MIPI5 ID2<br>5'd23: Select MIPI5 ID3<br>5'd24: Select DVP<br>Others: Reserved |
| 18:17 | RO | 0x0 | reserved |
| 16 | RW | 0x0 | sw_toisp0_en_ch2<br>Enable toisp0 channel2.<br>1'b0: Disable<br>1'b1: Enable |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:11 | RW | 0x00 | sw_toisp0_mux_ch1<br>5'd0: Select MIPI0 ID0<br>5'd1: Select MIPI0 ID1<br>5'd2: Select MIPI0 ID2<br>5'd3: Select MIPI0 ID3<br>5'd4: Select MIPI1 ID0<br>5'd5: Select MIPI1 ID1<br>5'd6: Select MIPI1 ID2<br>5'd7: Select MIPI1 ID3<br>5'd8: Select MIPI2 ID0<br>5'd9: Select MIPI2 ID1<br>5'd10: Select MIPI2 ID2<br>5'd11: Select MIPI2 ID3<br>5'd12: Select MIPI3 ID0<br>5'd13: Select MIPI3 ID1<br>5'd14: Select MIPI3 ID2<br>5'd15: Select MIPI3 ID3<br>5'd16: Select MIPI4 ID0<br>5'd17: Select MIPI4 ID1<br>5'd18: Select MIPI4 ID2<br>5'd19: Select MIPI4 ID3<br>5'd20: Select MIPI5 ID0<br>5'd21: Select MIPI5 ID1<br>5'd22: Select MIPI5 ID2<br>5'd23: Select MIPI5 ID3<br>5'd24: Select DVP<br>Others: Reserved |
| 10:9 | RO | 0x0 | reserved |
| 8 | RW | 0x0 | sw_toisp0_en_ch1<br>Enable toisp0 channel1.<br>1'b0: Disable<br>1'b1: Enable |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:3 | RW | 0x00 | sw_toisp0_mux_ch0<br>5'd0: Select MIPI0 ID0<br>5'd1: Select MIPI0 ID1<br>5'd2: Select MIPI0 ID2<br>5'd3: Select MIPI0 ID3<br>5'd4: Select MIPI1 ID0<br>5'd5: Select MIPI1 ID1<br>5'd6: Select MIPI1 ID2<br>5'd7: Select MIPI1 ID3<br>5'd8: Select MIPI2 ID0<br>5'd9: Select MIPI2 ID1<br>5'd10: Select MIPI2 ID2<br>5'd11: Select MIPI2 ID3<br>5'd12: Select MIPI3 ID0<br>5'd13: Select MIPI3 ID1<br>5'd14: Select MIPI3 ID2<br>5'd15: Select MIPI3 ID3<br>5'd16: Select MIPI4 ID0<br>5'd17: Select MIPI4 ID1<br>5'd18: Select MIPI4 ID2<br>5'd19: Select MIPI4 ID3<br>5'd20: Select MIPI5 ID0<br>5'd21: Select MIPI5 ID1<br>5'd22: Select MIPI5 ID2<br>5'd23: Select MIPI5 ID3<br>5'd24: Select DVP<br>Others: Reserved |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | sw_toisp0_en_ch0<br>Enable toisp0 channel0.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_TOISP0_CROP_SIZE**

Address: Operational Base + offset (0x0784)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x01e0 | sw_height<br>The expected height of received image. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x02d0 | sw_width<br>The expected width of received image. |

**VICAP_TOISP0_CROP_START**

Address: Operational Base + offset (0x0788)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:30 | RO | 0x0 | reserved |
| 29:16 | RW | 0x0000 | sw_start_y<br>The vertical ordinate of the start point. |
| 15:14 | RO | 0x0 | reserved |
| 13:0 | RW | 0x0000 | sw_start_x<br>The horizontal ordinate of the start point. |

**VICAP_TOISP1_CH_CTRL**

Address: Operational Base + offset (0x078C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:27 | RO | 0x00 | reserved |
| 26:25 | RW | 0x0 | sw_toisp1_vc_hdr_ch_main<br>Toisp1 vc hdr main channel. |
| 24 | RW | 0x0 | sw_toisp1_vc_hdr_protect<br>Enable toisp1 vc hdr protect.<br>1'b0: Disable<br>1'b1: Enable |
| 23:19 | RW | 0x00 | sw_toisp1_mux_ch2<br>5'd0: Select MIPI0 ID0<br>5'd1: Select MIPI0 ID1<br>5'd2: Select MIPI0 ID2<br>5'd3: Select MIPI0 ID3<br>5'd4: Select MIPI1 ID0<br>5'd5: Select MIPI1 ID1<br>5'd6: Select MIPI1 ID2<br>5'd7: Select MIPI1 ID3<br>5'd8: Select MIPI2 ID0<br>5'd9: Select MIPI2 ID1<br>5'd10: Select MIPI2 ID2<br>5'd11: Select MIPI2 ID3<br>5'd12: Select MIPI3 ID0<br>5'd13: Select MIPI3 ID1<br>5'd14: Select MIPI3 ID2<br>5'd15: Select MIPI3 ID3<br>5'd16: Select MIPI4 ID0<br>5'd17: Select MIPI4 ID1<br>5'd18: Select MIPI4 ID2<br>5'd19: Select MIPI4 ID3<br>5'd20: Select MIPI5 ID0<br>5'd21: Select MIPI5 ID1<br>5'd22: Select MIPI5 ID2<br>5'd23: Select MIPI5 ID3<br>5'd24: Select DVP<br>Others: Reserved |
| 18:17 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 16 | RW | 0x0 | sw_toisp1_en_ch2<br>Enable toisp0 channel2.<br>1'b0: Disable<br>1'b1: Enable |
| 15:11 | RW | 0x00 | sw_toisp1_mux_ch1<br>5'd0: Select MIPI0 ID0<br>5'd1: Select MIPI0 ID1<br>5'd2: Select MIPI0 ID2<br>5'd3: Select MIPI0 ID3<br>5'd4: Select MIPI1 ID0<br>5'd5: Select MIPI1 ID1<br>5'd6: Select MIPI1 ID2<br>5'd7: Select MIPI1 ID3<br>5'd8: Select MIPI2 ID0<br>5'd9: Select MIPI2 ID1<br>5'd10: Select MIPI2 ID2<br>5'd11: Select MIPI2 ID3<br>5'd12: Select MIPI3 ID0<br>5'd13: Select MIPI3 ID1<br>5'd14: Select MIPI3 ID2<br>5'd15: Select MIPI3 ID3<br>5'd16: Select MIPI4 ID0<br>5'd17: Select MIPI4 ID1<br>5'd18: Select MIPI4 ID2<br>5'd19: Select MIPI4 ID3<br>5'd20: Select MIPI5 ID0<br>5'd21: Select MIPI5 ID1<br>5'd22: Select MIPI5 ID2<br>5'd23: Select MIPI5 ID3<br>5'd24: Select DVP<br>Others: Reserved |
| 10:9 | RO | 0x0 | reserved |
| 8 | RW | 0x0 | sw_toisp1_en_ch1<br>Enable toisp1 channel1.<br>1'b0: Disable<br>1'b1: Enable |

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7:3 | RW | 0x00 | sw_toisp1_mux_ch0<br>5'd0: Select MIPI0 ID0<br>5'd1: Select MIPI0 ID1<br>5'd2: Select MIPI0 ID2<br>5'd3: Select MIPI0 ID3<br>5'd4: Select MIPI1 ID0<br>5'd5: Select MIPI1 ID1<br>5'd6: Select MIPI1 ID2<br>5'd7: Select MIPI1 ID3<br>5'd8: Select MIPI2 ID0<br>5'd9: Select MIPI2 ID1<br>5'd10: Select MIPI2 ID2<br>5'd11: Select MIPI2 ID3<br>5'd12: Select MIPI3 ID0<br>5'd13: Select MIPI3 ID1<br>5'd14: Select MIPI3 ID2<br>5'd15: Select MIPI3 ID3<br>5'd16: Select MIPI4 ID0<br>5'd17: Select MIPI4 ID1<br>5'd18: Select MIPI4 ID2<br>5'd19: Select MIPI4 ID3<br>5'd20: Select MIPI5 ID0<br>5'd21: Select MIPI5 ID1<br>5'd22: Select MIPI5 ID2<br>5'd23: Select MIPI5 ID3<br>5'd24: Select DVP<br>Others: Reserved |
| 2:1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | sw_toisp1_en_ch0<br>Enable toisp1 channel0.<br>1'b0: Disable<br>1'b1: Enable |

**VICAP_TOISP1_CROP_SIZE**

Address: Operational Base + offset (0x0790)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:16 | RW | 0x01e0 | sw_height<br>The expected height of received image. |
| 15:13 | RO | 0x0 | reserved |
| 12:0 | RW | 0x02d0 | sw_width<br>The expected width of received image. |

**VICAP_TOISP1_CROP_START**

Address: Operational Base + offset (0x0794)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:16 | RW | 0x0000 | sw_start_y<br>The vertical ordinate of the start point. |
| 15:13 | RO | 0x0 | reserved |
| 12:0 | RW | 0x0000 | sw_start_x<br>The horizontal ordinate of the start point. |

**VICAP_MMU0_DTE_ADDR**

Address: Operational Base + offset (0x0800)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | mmu_dte_addr<br>MMU current page table address. |

**VICAP_MMU0_STATUS**

Address: Operational Base + offset (0x0804)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:11 | RO | 0x000000 | reserved |
| 10:6 | RW | 0x00 | page_fault_bus_id<br>Index of master reponsible for last page fault. |
| 5 | RW | 0x0 | page_fault_is_write<br>The direction of access for last page fault:<br>1'b0: Read<br>1'b1: Write |
| 4 | RW | 0x0 | replay_buffer_empty<br>The MMU replay buffer is empty. |
| 3 | RW | 0x0 | mmu_idle<br>The MMU is idle when accesses are being translated and there are no unfinished translated accesses. |
| 2 | RW | 0x0 | stail_active<br>MMU stall mode currently enabled. The mode is enabled by command. |
| 1 | RW | 0x0 | page_fault_active<br>MMU page fault mode currently enabled . The mode is enabled by command. |
| 0 | RW | 0x0 | paging_enabled<br>Paging is enabled. |

**VICAP_MMU0_COMMAND**

Address: Operational Base + offset (0x0808)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2:0 | RW | 0x0 | mmu_cmd<br>MMU_CMD. This can be:<br>3'b000: MMU_ENABLE_PAGING<br>3'b001: MMU_DISABLE_PAGING<br>3'b010: MMU_ENABLE_STALL<br>3'b011: MMU_DISABLE_STALL<br>3'b100: MMU_ZAP_CACHE<br>3'b101: MMU_PAGE_FAULT_DONE |

**VICAP_MMU0_PAGE_FAULT_ADDR**

Address: Operational Base + offset (0x080C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | page_fault_addr<br>Address of last page fault. |

**VICAP_MMU0_ZAP_ONE_LINE**

Address: Operational Base + offset (0x0810)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | mmu_zap_one_line<br>Address to be invalidated from the page table cache. |

**VICAP_MMU0_INT_RAWSTAT**

Address: Operational Base + offset (0x0814)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | read_bus_error<br>Read bus error. |
| 0 | RW | 0x0 | page_fault<br>Page fault. |

**VICAP_MMU0_INT_CLEAR**

Address: Operational Base + offset (0x0818)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | read_bus_error<br>Read bus error. |
| 0 | RW | 0x0 | page_fault<br>Page fault. |

**VICAP_MMU0_INT_MASK**

Address: Operational Base + offset (0x081C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1 | RW | 0x0 | read_bus_error<br>Read bus error |
| 0 | RW | 0x0 | page_fault<br>Page fault |

**VICAP_MMU0_INT_STATUS**

Address: Operational Base + offset (0x0820)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | read_bus_error<br>Read bus error. |
| 0 | RW | 0x0 | page_fault<br>Page fault. |

**VICAP_MMU0_AUTO_GATING**

Address: Operational Base + offset (0x0824)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | mmu_auto_gating<br>When it is 1'b1, the mmu will auto gating it self |

**VICAP_MMU1_DTE_ADDR**

Address: Operational Base + offset (0x0900)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | mmu_dte_addr<br>MMU current page table address. |

**VICAP_MMU1_STATUS**

Address: Operational Base + offset (0x0904)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:11 | RO | 0x000000 | reserved |
| 10:6 | RW | 0x00 | page_fault_bus_id<br>Index of master reponsible for last page fault. |
| 5 | RW | 0x0 | page_fault_is_write<br>The direction of access for last page fault:<br>1'b0: Read<br>1'b1: Write |
| 4 | RW | 0x0 | replay_buffer_empty<br>The MMU replay buffer is empty. |
| 3 | RW | 0x0 | mmu_idle<br>The MMU is idle when accesses are being translated and there are no unfinished translated accesses. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | stail_active<br>MMU stall mode currently enabled. The mode is enabled by command. |
| 1 | RW | 0x0 | page_fault_active<br>MMU page fault mode currently enabled . The mode is enabled by command. |
| 0 | RW | 0x0 | paging_enabled<br>Paging is enabled. |

**VICAP_MMU1_COMMAND**

Address: Operational Base + offset (0x0908)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2:0 | RW | 0x0 | mmu_cmd<br>MMU_CMD. This can be:<br>3'b000: MMU_ENABLE_PAGING<br>3'b001: MMU_DISABLE_PAGING<br>3'b010: MMU_ENABLE_STALL<br>3'b011: MMU_DISABLE_STALL<br>3'b100: MMU_ZAP_CACHE<br>3'b101: MMU_PAGE_FAULT_DONE |

**VICAP_MMU1_PAGE_FAULT_ADDR**

Address: Operational Base + offset (0x090C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | page_fault_addr<br>Address of last page fault. |

**VICAP_MMU1_ZAP_ONE_LINE**

Address: Operational Base + offset (0x0910)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | mmu_zap_one_line<br>Address to be invalidated from the page table cache. |

**VICAP_MMU1_INT_RAWSTAT**

Address: Operational Base + offset (0x0914)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | read_bus_error<br>Read bus error. |
| 0 | RW | 0x0 | page_fault<br>Page fault. |

**VICAP_MMU1_INT_CLEAR**

Address: Operational Base + offset (0x0918)

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | read_bus_error<br>Read bus error. |
| 0 | RW | 0x0 | page_fault<br>Page fault. |

**VICAP_MMU1_INT_MASK**

Address: Operational Base + offset (0x091C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | read_bus_error<br>Read bus error |
| 0 | RW | 0x0 | page_fault<br>Page fault |

**VICAP_MMU1_INT_STATUS**

Address: Operational Base + offset (0x0920)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | read_bus_error<br>Read bus error. |
| 0 | RW | 0x0 | page_fault<br>Page fault. |

**VICAP_MMU1_AUTO_GATING**

Address: Operational Base + offset (0x0924)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | mmu_auto_gating<br>When it is 1'b1, the mmu will auto gating it self |

# 37.5 Interface Description

Table 37-2 VICAP Interface Description

| Module Pin | Dir | Pad Name | IOMUX Setting |
|---|---|---|---|
| vicap_clkout | O | CIF_CLKOUT/BT1120_D10/I2S1_SDO3_M0/PCIE30X4_CLKREQN_M1/DP0_HPDIN_M0/SPDIF0_TX_M1/UART9_TX_M1/PWM11_IR_M1/GPIO4_B4_u | BUS_IOC_GPIO4B_IOMUX_SEL_H[3:0]=4'h1 |
| vicap_clkin | I | CIF_CLKIN/BT1120_CLKOUT/I2S1_SDI3_M0/PCIE30X2_PERSTN_M1/I2C6_SDA_M3/UART8_TX_M0/SPI2_CS1_M1/GPIO4_B0_d | BUS_IOC_GPIO4B_IOMUX_SEL_L[3:0]=4'h1 |
| vicap_href | I | CIF_HREF/BT1120_D8/I2S1_SDO1_M0/PCIE30X1_1_BUTTON_RSTN/I2C7_SCL_M3/UART8_RTSN_M0/PWM14_M1/SPI0_CS0_M1/CAN1_RX_M1/GPIO4_B2_u | BUS_IOC_GPIO4B_IOMUX_SEL_L[11:8]=4'h1 |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Module Pin | Dir | Pad Name | IOMUX Setting |
|---|---|---|---|
| vicap_vsync | I | CIF_VSYNC/BT1120_D9/I2S1_SDO2_M0/PCIE20X1_2_BUTTON_RSTN/I2C7_SDA_M3/UART8_CTSN_M0/PWM15_IR_M1/CAN1_TX_M1/GPIO4_B3_u | BUS_IOC_GPIO4B_IOMUX_SEL_L[15:12]=4'h1 |
| vicap_data0 | I | CIF_D0/BT1120_D0/I2S1_MCLK_M0/PCIE30X1_1_CLKREQN_M1/UART9_RTSN_M1/SPI0_MISO_M1/GPIO4_A0_d | BUS_IOC_GPIO4A_IOMUX_SEL_L[3:0]=4'h1 |
| vicap_data1 | I | CIF_D1/BT1120_D1/I2S1_SCLK_M0/PCIE30X1_1_WAKEN_M1/UART9_CTSN_M1/SPI0_MOSI_M1/GPIO4_A1_d | BUS_IOC_GPIO4A_IOMUX_SEL_L[7:4]=4'h1 |
| vicap_data2 | I | CIF_D2/BT1120_D2/I2S1_LRCK_M0/PCIE30X1_1_PERSTN_M1/SPI0_CLK_M1/GPIO4_A2_d | BUS_IOC_GPIO4A_IOMUX_SEL_L[11:8]=4'h1 |
| vicap_data3 | I | CIF_D3/BT1120_D3/PCIE30X1_0_CLKREQN_M1/UART0_TX_M2/GPIO4_A3_d | BUS_IOC_GPIO4A_IOMUX_SEL_L[15:12]=4'h1 |
| vicap_data4 | I | CIF_D4/BT1120_D4/PCIE30X1_0_WAKEN_M1/I2C3_SCL_M2/UART0_RX_M2/SPI2_MISO_M1/GPIO4_A4_d | BUS_IOC_GPIO4A_IOMUX_SEL_H[3:0]=4'h1 |
| vicap_data5 | I | CIF_D5/BT1120_D5/I2S1_SDI0_M0/PCIE30X1_0_PERSTN_M1/I2C3_SDA_M2/UART3_TX_M2/SPI2_MOSI_M1/GPIO4_A5_d | BUS_IOC_GPIO4A_IOMUX_SEL_H[7:4]=4'h1 |
| vicap_data6 | I | CIF_D6/BT1120_D6/I2S1_SDI1_M0/PCIE30X2_CLKREQN_M1/I2C5_SCL_M2/UART3_RX_M2/SPI2_CLK_M1/GPIO4_A6_d | BUS_IOC_GPIO4A_IOMUX_SEL_H[11:8]=4'h1 |
| vicap_data7 | I | CIF_D7/BT1120_D7/I2S1_SDI2_M0/PCIE30X2_WAKEN_M1/I2C5_SDA_M2/SPI2_CS0_M1/GPIO4_A7_d | BUS_IOC_GPIO4A_IOMUX_SEL_H[15:12]=4'h1 |
| vicap_data8 | I | CIF_D8/FSPI_CS0N_M2/PCIE30X4_CLKREQN_M2/HDMI_TX1_CEC_M2/CAN2_RX_M0/UART5_TX_M1/SPI3_CS0_M3/GPIO3_C4_u | BUS_IOC_GPIO3C_IOMUX_SEL_H[3:0]=4'h1 |
| vicap_data9 | I | CIF_D9/FSPI_CS1N_M2/PCIE30X4_WAKEN_M2/HDMI_TX1_SDA_M1/CAN2_TX_M0/UART5_RX_M1/SPI3_CS1_M3/GPIO3_C5_u | BUS_IOC_GPIO3C_IOMUX_SEL_H[7:4]=4'h1 |
| vicap_data10 | I | CIF_D10/PCIE30X4_PERSTN_M2/HDMI_TX1_SCL_M1/SPI3_MISO_M3/GPIO3_C6_u | BUS_IOC_GPIO3C_IOMUX_SEL_H[11:8]=4'h1 |
| vicap_data11 | I | CIF_D11/PCIE20X1_2_CLKREQN_M0/HDMI_TX0_SCL_M2/I2C5_SCL_M0/SPI3_MOSI_M3/GPIO3_C7_u | BUS_IOC_GPIO3C_IOMUX_SEL_H[15:12]=4'h1 |
| vicap_data12 | I | CIF_D12/PCIE20X1_2_WAKEN_M0/HDMI_TX0_SDA_M2/I2C5_SDA_M0/UART4_RX_M1/PWM8_M2/SPI3_CLK_M3/GPIO3_D0_u | BUS_IOC_GPIO3D_IOMUX_SEL_L[3:0]=4'h1 |
| vicap_data13 | I | CIF_D13/PCIE20X1_2_PERSTN_M0/HDMI_RX_CEC_M1/UART4_TX_M1/PWM9_M2/SPI0_MISO_M3/GPIO3_D1_d | BUS_IOC_GPIO3D_IOMUX_SEL_L[7:4]=4'h1 |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Module Pin | Dir | Pad Name | IOMUX Setting |
|---|---|---|---|
| vicap_data14 | I | CIF_D14/PCIE30X2_CLKREQN_M2/HDMI_RX_SCL_M1/I2C7_SCL_M2/UART9_RTSN_M2/SPI0_MOSI_M3/GPIO3_D2_d | BUS_IOC_GPIO3D_IOMUX_SEL_L[11:8]=4'h1 |
| vicap_data15 | I | CIF_D15/PCIE30X2_WAKEN_M2/HDMI_RX_SDA_M1/I2C7_SDA_M2/UART9_CTSN_M2/PWM10_M2/SPI0_CLK_M3/GPIO3_D3_d | BUS_IOC_GPIO3D_IOMUX_SEL_L[15:12]=4'h1 |

*Notes: I=input, O=output, I/O=input/output, bidirectional*

Furthermore, different IOs are selected and connected to different flash interface, which is shown as follows.

# 37.6 Application Notes

## 37.6.1 DVP Interface

- The MSB 4 bits of SAV/EAV of BT.656/BT.1120 are configurable, and the default values of SAV/EAV abide by the agreement.
- The sw_only_sav_mode for BT.656/BT.1120 is more robust for the case that the EAV is wrong.
- User can read the register of ro_sync_header_0~ro_sync_header_7 to obtain the recent 8 SAV/EAV.
- In the multi-ID mode the LSB 4 bits of SAV/EAV are used to distinguish ID. In most cases the LSB 2 bits of SAV/EAV are ID number, in these cases the register sw_chid_bit_en should be configured as 4'h3.
- The register sw_yuyv_in_order should be configured correctly. In the BT.1120 case 2'h0/2'h2 are the same for UV sequence and 2'h1/2'h3 are the same for VU sequence.
- In the dual-edge sampling case, the SYS_GRF_SOC_CON2[5] must be set to 1, and the register sw_dualedge_en must be set to 1. The clock phase could be adjusted by setting the SYS_GRF_SOC_CON3[7:0].

## 37.6.2 MIPI Interface

- The register sw_crop_en is suggested to be set to 1. The register sw_width/sw_start_x should be aligned to 4.
- In the sony identification code hdr mode, the register sw_sony_effect_code0/1 should be configured correctly according to the camera manual.
- In the line counter hdr mode, the register sw_on_pad_value should be configured correctly according to the camera manual.
- In the VC hdr mode, the register sw_vc_hdr_protect is suggested to be set to 1, and the register sw_vc_hdr_id_main should be configured as the first coming id that is the long exposure frame id.
- The register sw_cap_en_idx is recommended for static configuration, and the register sw_cap_en is recommended for dynamic configuration.

## 37.6.3 Scale down

- The register sw_scl_chx_black_00/01/10/11 is the black level value for bayer pattern 00/01/10/11 position.
- The bit width of scale down output data is 16. When the max bit width of the scale down output data exceed 16, output data will be clipped. For example, 8 times scale down for RAW12, the bit width is 18, then the result will be clipped to 16 bits.
- When the width is not a multiple of double scale down times,then the result will be rounded up to an integer. For example, the image width is 4656 and 32 times scaling down is performed, the result width equals to (ceil(4656/64)*64)/32.
- When the height is not a multiple of double scale down times, then the result will be rounded down to an integer. For example, the image height is 1080 and 8 times scaling down is performed, the result height equals to (floor(1080/16)*16)/8.

## 37.6.4 TOISP

- The register sw_width/sw_start_x should be aligned to 4.
- Although there are three channels to ISP, user just need enable channel 0 and select the short exposure frame id.

Copyright 2022 © Rockchip Electronics Co., Ltd. 

### 37.6.5 DMA

- The start address/virtual stride should be aligned to 8 at least. And being aligned to 64 is good for DDR.
- User could shut down DMA transferring by setting the register sw_dma_en to 0.
- User could set sw_hurry_en/sw_press_en to 1 for dynamic adjusting the priority of VICAP. And the register sw_water_line is the triggering condition of pulling up hurry/press signal.
- For DVP path the register sw_yuyv_out_order is effective when the register sw_wrddr_type is NV16/NV12/YUYV. And in the NV16/NV12 case, 2'h0/2'h2 are the same for UV sequence and 2'h1/2'h3 are the same for VU sequence.
- For MIPI path the register sw_yuyv_out_order is effective when the register sw_wrddr_type is YUYV. And in the NV16/NV12 case, sw_yuyv_out_order need to be configured as the same as sw_yuyv_in_order.
- There are two modes for line counter interrupt.In one-time mode, if line_int_num =100, the line_intst will be 1 when receive 100th line. In circular mode, if line_int_num =100, the line_intst will be 1 when receive 100th line200th line300th line.....
- There are two AXI masters and two MMUs in VICAP. The AXI_0/MMU_0 are used for MIPI_0/MIPI_2/MIPI_5/SCALE, and the AXI_1/MMU_1 are used for MIPI_1/MIPI_3/MIPI_4/DVP.

### 37.6.6 Reset

- DMA will be auto-reset when DMA goes wrong, for example fifo overflow. And DMA will transfer data from the next frame.
- DMA also could be soft-reset by the register sw_dma_rst.
- User could reset the entire data path (interface/dma) by setting the register sw_soft_rst to 1. And the scale/toisp module will be reset if the sw_scl_mux/sw_toisp_mux is setted to choose the path.

Copyright 2022 © Rockchip Electronics Co., Ltd.

# Chapter 38 FishEye Correction(FEC)

## 38.1 Overview

FEC supports the following features:

- Input mode and data format
  - Support RASTER: YUV422SP, YUV422I, YUV420SP
- Output mode and data format
  - RASTER: YUV422SP, YUV422I, YUV420SP
  - FBCE: YUV422SP, YUV420SP
- Support 16x8, 32x16 two density
- Support up to 4 times reduction factor
  The basic unit of the destination end is 16x16 and 32x32. For the larger distortion uses 16x16, and the smaller distortion uses 32x32. When the corresponding source exceeds 64x64, then directly fills Y=0, U=128, V=128
- Support level interrupt
- Support 32bit AHB
- Support 128bit AXI
- Support 128bit MMU, MMU affect FEC performance, it is recommended to close MMU
- Input resolution 128x128~8188x8188
- Output resolution 128x128~4096x4096
- Source width and height must be x4
- Destination width and height must be x4
- Y Interpolation: Bicubic; C Interpolation: Biliner

## 38.2 Block Diagram

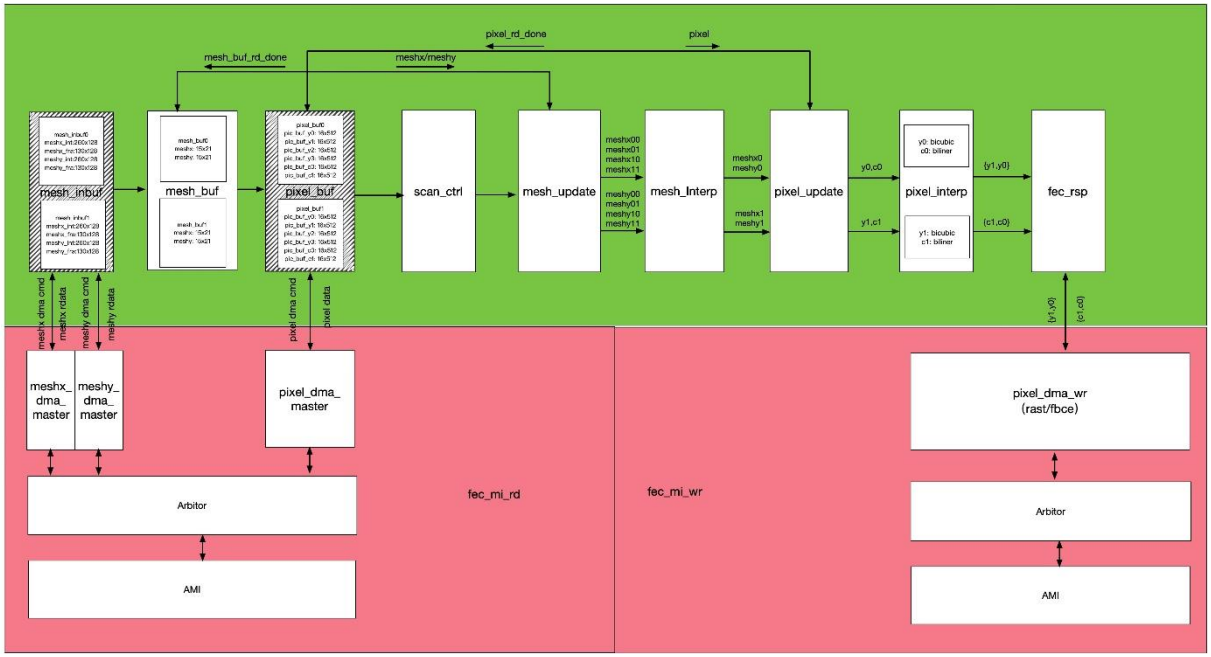



Fig. 38-1 FEC Block Diagram

## 38.3 Function Description

The principle of FEC is to obtain the corresponding source data according to the meshgrid requirements, and then perform interpolation according to the corresponding coefficients, as shown in the following figure:

Copyright 2022 © Rockchip Electronics Co., Ltd. 

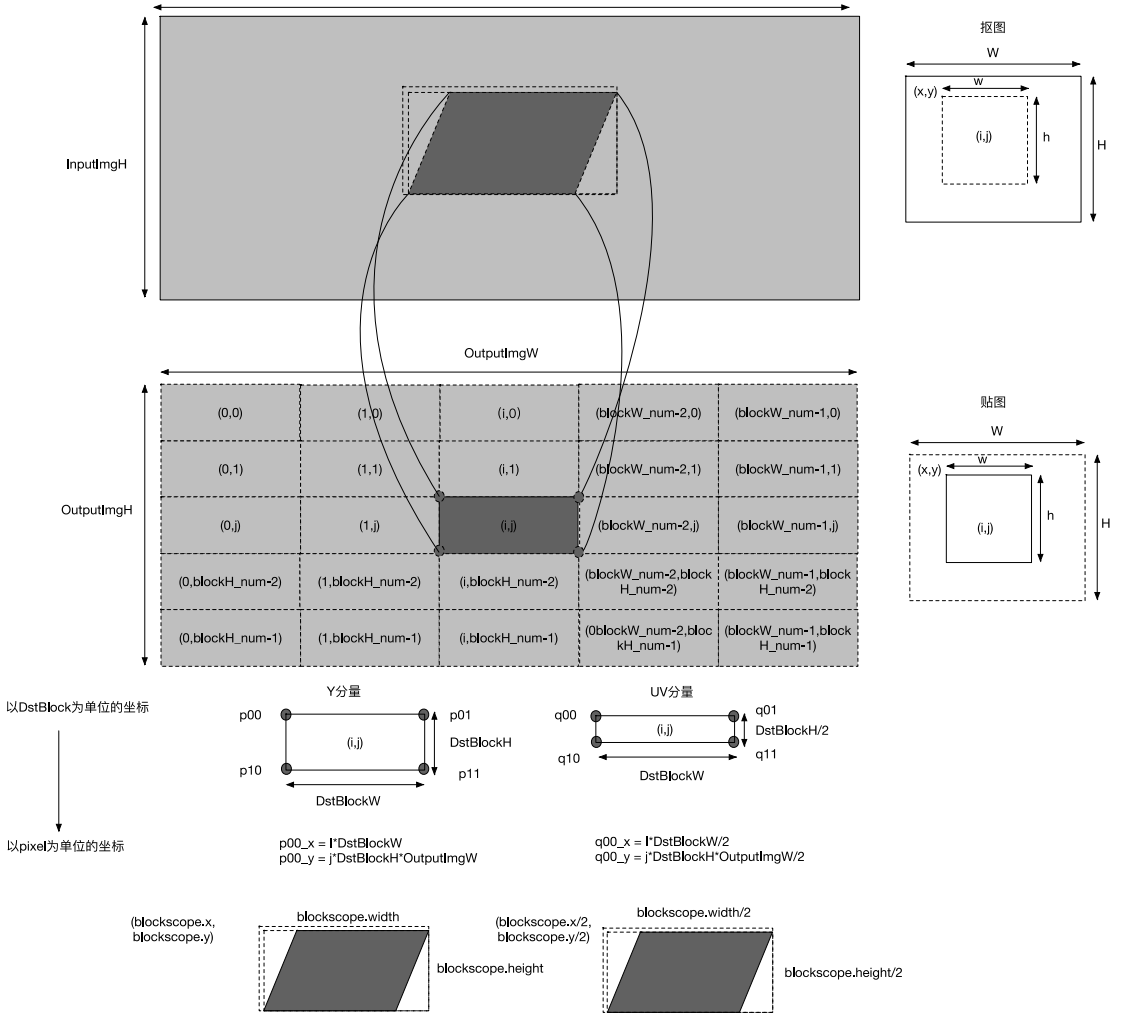



Fig. 38-2 FEC function description

1、 You need to align the resolution to 32x32 firstly, and then down-sample according to the meshgrid density of 16x8 or 32x16

2、 Decimals meshgrid and integer meshgrid are stored separately, and the address must aligned to 16B

3、 And due to the pixel scan, in order to achieve the maximum efficiency of using the grid, the meshgrid timing needs to be overlapped, according to the 32x128 block, as shown in the following figure:

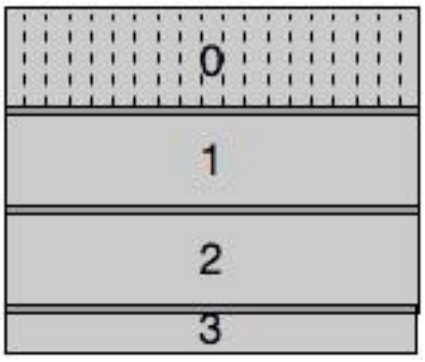



Fig. 38-3 FEC meshgrid overlap

4、Consistent with the pixel scanning, the meshgrid can be used with maximum efficiency

Copyright 2022 © Rockchip Electronics Co., Ltd. 

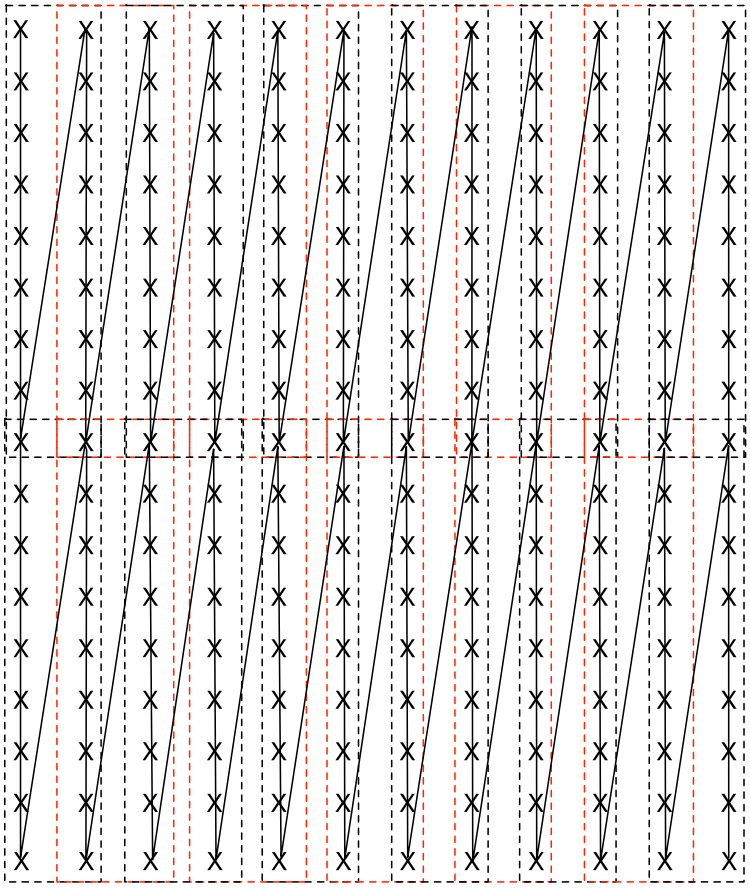


Fig. 38-4 FEC meshgrid order in DDR

## 38.4 Register Description

### 38.4.1 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| FEC_ISPP_START | 0x0000 | W | 0x00000000 | ISPP command start |
| FEC_ISPP_UPDATE | 0x0004 | W | 0x00000004 | ISPP register force update |
| FEC_ISPP_RESET | 0x000C | W | 0x00000000 | ISPP soft reset |
| FEC_ISPP_CLKGATE | 0x0010 | W | 0x00000000 | FEC clock gating |
| FEC_INT_MSK | 0x0020 | W | 0x00000000 | Interrupt mask |
| FEC_INT_RAW | 0x0024 | W | 0x00000000 | Interrupt raw status |
| FEC_INT_STA | 0x0028 | W | 0x00000000 | Interrupt status |
| FEC_INT_SET | 0x002C | W | 0x00000000 | Interrupt enable |
| FEC_INT_CLR | 0x0030 | W | 0x00000000 | Interrupt clear |
| FEC_ISPP_STATUS | 0x0054 | W | 0x00000000 | ISPP status register |
| FEC_MI_CTRL | 0x0C00 | W | 0x00004000 | Memory interface control |
| FEC_RD_VIR_STRIDE | 0x0C04 | W | 0x00000000 | FEC RD virtual stride, 16B aligned, word unit |
| FEC_RD_Y_BASE | 0x0C08 | W | 0x00000000 | FEC DMA read y base address, 16B aligned |
| FEC_RD_UV_BASE | 0x0C0C | W | 0x00000000 | FEC DMA read uv base address, 16B aligned |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| FEC_MESH_XINT_BASE | 0x0C10 | W | 0x00000000 | FEC mesh x integer base address, 16B aligned |
| FEC_MESH_XFRA_BASE | 0x0C14 | W | 0x00000000 | FEC mesh x fraction base address, 16B aligned |
| FEC_MESH_YINT_BASE | 0x0C18 | W | 0x00000000 | FEC mesh y integer base address, 16B aligned |
| FEC_MESH_YFRA_BASE | 0x0C1C | W | 0x00000000 | FEC mesh y fraction base address, 16B aligned |
| FEC_WR_VIR_STRIDE | 0x0C20 | W | 0x00000000 | FEC write virtual stride,16B aligned, word unit |
| FEC_WR_Y_BASE | 0x0C24 | W | 0x00000000 | FEC DMA write y base address, 16B aligned |
| FEC_WR_UV_BASE | 0x0C28 | W | 0x00000000 | FEC DMA write uv base address, 16B aligned |
| FEC_RD_Y_BASE_SHD | 0x0C2C | W | 0x00000000 | FEC DMA read y base address shadow, 16B aligned |
| FEC_RD_UV_BASE_SHD | 0x0C30 | W | 0x00000000 | FEC DMA read uv base address shadow, 16B aligned |
| FEC_MESH_XINT_BASE_SHD | 0x0C34 | W | 0x00000000 | FEC DMA read x integer base address shadow, 16B aligned |
| FEC_MESH_XFRA_BASE_SHD | 0x0C38 | W | 0x00000000 | FEC DMA read x fraction base address shadow, 16B aligned |
| FEC_MESH_YINT_BASE_SHD | 0x0C3C | W | 0x00000000 | FEC DMA read y integer base address shadow, 16B aligned |
| FEC_MESH_YFRA_BASE_SHD | 0x0C40 | W | 0x00000000 | FEC DMA read y fraction base address shadow, 16B aligned |
| FEC_WR_Y_BASE_SHD | 0x0C44 | W | 0x00000000 | FEC DMA write y base address shadow, 16B aligned |
| FEC_WR_UV_BASE_SHD | 0x0C48 | W | 0x00000000 | FEC DMA write uv base address shadow, 16B aligned |
| FEC_AR_QOS_CTRL | 0x0C54 | W | 0x00000030 | FEC read qos control |
| FEC_CORE_CTRL | 0x0C80 | W | 0x00000000 | FEC core control |
| FEC_DST_SIZE | 0x0C88 | W | 0x00000000 | FEC destination size |
| FEC_MESH_SIZE | 0x0C8C | W | 0x00000000 | FEC mesh size |
| FEC_DMA_STATUS | 0x0C90 | W | 0x00000000 | FEC DMA status |
| FEC_SRC_SIZE | 0x0C98 | W | 0x00000000 | FEC source size |
| FEC_MMU_DTE_ADDR | 0x0F00 | W | 0x00000000 | MMU current page Table address |
| FEC_MMU_STATUS | 0x0F04 | W | 0x00000018 | MMU status |
| FEC_MMU_COMMAND | 0x0F08 | W | 0x00000000 | MMU command |
| FEC_MMU_PAGE_FAULT_ADDR | 0x0F0C | W | 0x00000000 | MMU address of last page fault |
| FEC_MMU_ZAP_ONE_LINE | 0x0F10 | W | 0x00000000 | MMU address to be invalidated from the page table cache |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| FEC_MMU_INT_RAWSTAT | 0x0F14 | W | 0x00000000 | MMU raw interrupt |
| FEC_MMU_INT_CLEAR | 0x0F18 | W | 0x00000000 | MMU interrupt clear |
| FEC_MMU_INT_MASK | 0x0F1C | W | 0x00000000 | MMU interrupt mask |
| FEC_MMU_INT_STATUS | 0x0F20 | W | 0x00000000 | MMU interrupt status |
| FEC_MMU_AUTO_GATING | 0x0F24 | W | 0x00000003 | MMU auto gating |
| FEC_MMU_REG_LOAD_EN | 0x0F28 | W | 0x00000000 | MMU register load enable |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

## 38.4.2 Detail Register Description

### FEC_ISPP_START

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2 | W1C | 0x0 | sw_fec_st<br>ISPP command start |
| 1:0 | RO | 0x0 | reserved |

### FEC_ISPP_UPDATE

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2 | W1C | 0x1 | sw_cfg_force_upd<br>ISPP register force update for FEC |
| 1:0 | RO | 0x0 | reserved |

### FEC_ISPP_RESET

Address: Operational Base + offset (0x000C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:16 | RW | 0x00 | sw_glb_init_dis<br>Hardware will reset automatically at frame start if the module Corresponding bit set to 0 |
| 15:12 | RO | 0x0 | reserved |
| 11:8 | RW | 0x0 | sys_reg_msoft_rst<br>Scale hardware will reset automatically at frame start if the module Corresponding bit set to 0 |
| 7:2 | RO | 0x00 | reserved |
| 1 | RW | 0x0 | sw_rst_protect_dis<br>Safety reset select<br>1'b0: Protect reset<br>1'b1: Direct reset |
| 0 | W1C | 0x0 | sw_glb_soft_rst_all<br>FEC soft reset with self-clear |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**FEC_ISPP_CLKGATE**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:6 | RO | 0x0000000 | reserved |
| 5 | RW | 0x0 | sw_glb_ckg_dis<br>Global clk gate_dis |
| 4:0 | RO | 0x00 | reserved |

**FEC_INT_MSK**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:9 | RO | 0x000000 | reserved |
| 8 | RW | 0x0 | bound_cross_p<br>FEC bound cross buffer interrupt mask<br>1'b0: Mask<br>1'b1: Not mask |
| 7 | RW | 0x0 | sw_fec_frame_end<br>FEC frame end interrupt mask<br>1'b0: Mask<br>1'b1: Not mask |
| 6:4 | RO | 0x0 | reserved |
| 3 | RW | 0x0 | esp_fifo_full_err<br>FEC rdata fifo write error when full interrupt mask<br>1'b0: Mask<br>1'b1: Not mask |
| 2:0 | RO | 0x0 | reserved |

**FEC_INT_RAW**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:9 | RO | 0x000000 | reserved |
| 8 | RO | 0x0 | bound_cross_p<br>FEC bound cross buffer interrupt raw status |
| 7 | RO | 0x0 | sw_fec_frame_end<br>FEC frame end interrupt raw status |
| 6:4 | RO | 0x0 | reserved |
| 3 | RO | 0x0 | esp_fifo_full_err<br>FEC rdata fifo write error when full raw status |
| 2:0 | RO | 0x0 | reserved |

**FEC_INT_STA**

Address: Operational Base + offset (0x0028)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:9 | RO | 0x000000 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 8 | RO | 0x0 | bound_cross_p<br>FEC bound cross buffer interrupt status |
| 7 | RO | 0x0 | sw_fec_frame_end<br>FEC frame end interrupt status |
| 6:4 | RO | 0x0 | reserved |
| 3 | RO | 0x0 | esp_fifo_full_err<br>FEC rdata fifo write error when full interrupt status |
| 2:0 | RO | 0x0 | reserved |

**FEC_INT_SET**

Address: Operational Base + offset (0x002C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:9 | RO | 0x000000 | reserved |
| 8 | W1C | 0x0 | bound_cross_p<br>FEC bound cross buffer interrupt set<br>1'b0: Disable<br>1'b1: Enable |
| 7 | W1C | 0x0 | sw_fec_frame_end<br>FEC frame end interrupt set<br>1'b0: Disable<br>1'b1: Enable |
| 6:4 | RO | 0x0 | reserved |
| 3 | W1C | 0x0 | esp_fifo_full_err<br>FEC rdata fifo write error when full interrupt set<br>1'b0: Disable<br>1'b1: Enable |
| 2:0 | RO | 0x0 | reserved |

**FEC_INT_CLR**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:9 | RO | 0x000000 | reserved |
| 8 | W1C | 0x0 | bound_cross_p<br>FEC bound cross buffer interrupt clear<br>1'b0: Not clear<br>1'b1: Clear |
| 7 | W1C | 0x0 | sw_fec_frame_end<br>FEC frame end interrupt clear<br>1'b0: Not clear<br>1'b1: Clear |
| 6:4 | RO | 0x0 | reserved |
| 3 | W1C | 0x0 | esp_fifo_full_err<br>FEC rdata fifo write error when full interrupt clear<br>1'b0: Not clear<br>1'b1: Clear |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2:0 | RO | 0x0 | reserved |

**FEC_ISPP_STATUS**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:23 | RO | 0x000 | reserved |
| 22:16 | RO | 0x00 | fec_tile_lint_cnt<br>FEC tile line counter |
| 15:0 | RO | 0x0000 | reserved |

**FEC_MI_CTRL**

Address: Operational Base + offset (0x0C00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:20 | RO | 0x000 | reserved |
| 19:14 | RW | 0x01 | sw_fec_rd_level_i<br>FEC read level |
| 13 | RW | 0x0 | sw_fec_rd_opt_dis<br>FEC read option disable |
| 12 | RW | 0x0 | sw_fec_fbce_sparse_mode<br>FEC fbce mode sparse_en |
| 11:9 | RO | 0x0 | reserved |
| 8 | RW | 0x0 | sw_fec_wr_yuv_limit<br>FEC write YUV limit |
| 7 | RW | 0x0 | sw_fec_wr_yuyv_ycswap<br>FEC write to DDR y/c swap<br>1'b0: Y/C do not swap<br>1'b1: Y/C swap |
| 6 | RW | 0x0 | sw_fec_wr_yuyv_format<br>FEC write to DDR format<br>1'b0: YUV422 not YUYV format<br>1'b1: YUV422 YUYV forma |
| 5 | RW | 0x0 | sw_fec_wr_yuv_formt<br>FEC write YUV format<br>1'b0: YUV420<br>1'b1: YUV422 |
| 4 | RW | 0x0 | sw_fec_wr_fbce_mode<br>FEC write to DDR mode<br>1'b0: Raster mode<br>1'b1: FBCE mode |
| 3 | RW | 0x0 | sw_fec_rd_yuyv_ycswap<br>FEC read y/c swap<br>1'b0: Y/C do not swap<br>1'b1: Y/C swap |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 2 | RW | 0x0 | sw_fec_rd_yuyv_format<br>FEC read YUYV format<br>1'b0: 422 non YUYV format<br>1'b1: 422 YUYV format |
| 1 | RW | 0x0 | sw_fec_rd_yuv_format<br>FEC read YUV format<br>1'b0: YUV420<br>1'b1: YUV422 |
| 0 | RO | 0x0 | reserved |

**FEC_RD_VIR_STRIDE**

Address: Operational Base + offset (0x0C04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |
| 12:0 | RW | 0x0000 | sw_fec_rd_vir_stride<br>FEC RD virtual stride, 16B aligned, word unit |

**FEC_RD_Y_BASE**

Address: Operational Base + offset (0x0C08)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_fec_rd_y_base<br>FEC DMA read y base address, 16B aligned |

**FEC_RD_UV_BASE**

Address: Operational Base + offset (0x0C0C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_fec_rd_uv_base<br>FEC DMA read uv base address, 16B aligned |

**FEC_MESH_XINT_BASE**

Address: Operational Base + offset (0x0C10)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_fec_mesh_xint_base<br>FEC mesh x integer base address, 16B aligned |

**FEC_MESH_XFRA_BASE**

Address: Operational Base + offset (0x0C14)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_fec_mesh_xfra_base<br>FEC mesh x fraction base address, 16B aligned |

**FEC_MESH_YINT_BASE**

Address: Operational Base + offset (0x0C18)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_fec_mesh_yint_base<br>FEC mesh y integer base address, 16B aligned |

**FEC_MESH_YFRA_BASE**

Address: Operational Base + offset (0x0C1C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_mesh_yfra_base<br>FEC mesh y fraction base address, 16B aligned |

**FEC_WR_VIR_STRIDE**

Address: Operational Base + offset (0x0C20)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:13 | RO | 0x00000 | reserved |
| 12:0 | RW | 0x0000 | sw_fec_wr_vir_stride<br>FEC write virtual stride,16B aligned, word unit |

**FEC_WR_Y_BASE**

Address: Operational Base + offset (0x0C24)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_fec_wr_y_base<br>FEC DMA write y base address, 16B aligned |

**FEC_WR_UV_BASE**

Address: Operational Base + offset (0x0C28)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_fec_wr_uv_base<br>FEC DMA write uv base address, 16B aligned |

**FEC_RD_Y_BASE_SHD**

Address: Operational Base + offset (0x0C2C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | sw_fec_rd_y_base_shd<br>FEC DMA read y base address shadow, 16B aligned |

**FEC_RD_UV_BASE_SHD**

Address: Operational Base + offset (0x0C30)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | sw_fec_rd_uv_base_shd<br>FEC DMA read uv base address shadow, 16B aligned |

**FEC_MESH_XINT_BASE_SHD**

Address: Operational Base + offset (0x0C34)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | sw_fec_mesh_xint_base_shd<br>FEC DMA read x integer base address shadow, 16B aligned |

**FEC_MESH_XFRA_BASE_SHD**

Address: Operational Base + offset (0x0C38)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | sw_fec_mesh_xfra_base_shd<br>FEC DMA read x fraction base address shadow, 16B aligned |

**FEC_MESH_YINT_BASE_SHD**

Address: Operational Base + offset (0x0C3C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | sw_fec_mesh_yint_base_shd<br>FEC DMA read y integer base address shadow, 16B aligned |

**FEC_MESH_YFRA_BASE_SHD**

Address: Operational Base + offset (0x0C40)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | sw_fec_mesh_yfra_base_shd<br>FEC DMA read y fraction base address shadow, 16B aligned |

**FEC_WR_Y_BASE_SHD**

Address: Operational Base + offset (0x0C44)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | sw_fec_wr_y_base_shd<br>FEC DMA write y base address shadow, 16B aligned |

**FEC_WR_UV_BASE_SHD**

Address: Operational Base + offset (0x0C48)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | sw_fec_wr_uv_base_shd<br>FEC DMA write uv base address shadow, 16B aligned |

**FEC_AR_QOS_CTRL**

Address: Operational Base + offset (0x0C54)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:11 | RO | 0x000000 | reserved |
| 10:8 | RW | 0x0 | sw_noc_hurry_value<br>FEC AXI read hurry enable |
| 7 | RO | 0x0 | reserved |
| 6:4 | RW | 0x3 | sw_fec_ar_mmu_qos<br>FEC AXI read qos value |
| 3:1 | RO | 0x0 | reserved |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 0 | RW | 0x0 | sw_fec_ar_qos_en<br>FEC AXI read qos enable<br>1'b0: Disable<br>1'b1: Enable |

**FEC_CORE_CTRL**

Address: Operational Base + offset (0x0C80)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RO | 0x0 | sw_fec_en_shd<br>FEC enable shadow |
| 30 | RO | 0x0 | sw_minbuf_non_update_shd<br>Mesh inbuf no update shadow |
| 29:9 | RO | 0x000000 | reserved |
| 8 | RW | 0x0 | sw_fec_cross_dis<br>FEC cross buffer disable<br>1'b0: FEC cross buffer enable<br>1'b1: FEC do not cross buffer |
| 7 | RO | 0x0 | reserved |
| 6 | RW | 0x0 | sw_minbuf_non_update<br>Mesh inbuf no update<br>1'b0: Mesh update current frame<br>1'b1: Mesh no update current frame |
| 5 | RW | 0x0 | sw_mesh_density<br>Mesh density<br>1'b0: 16x8 mesh density<br>1'b1: 32x16 mesh density |
| 4:3 | RW | 0x0 | sw_fec_bic_mode<br>Bicubic mode<br>2'b00: Precise<br>2'b01: Spline<br>2'b10: Catrom<br>2'b11: Mitchell |
| 2 | RO | 0x0 | reserved |
| 1 | RW | 0x0 | sw_fec2ddr_dis<br>FEC2DDR disable control bit<br>1'b0: Data write to DDR<br>1'b1: Data do not write to DDR |
| 0 | RW | 0x0 | sw_fec_en<br>FEC enable<br>1'b0: Disable<br>1'b1: Enable |

**FEC_DST_SIZE**

Address: Operational Base + offset (0x0C88)

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:16 | RW | 0x0000 | sw_fec_dst_height<br>FEC destination height |
| 15:13 | RO | 0x0 | reserved |
| 12:0 | RW | 0x0000 | sw_fec_dst_width<br>FEC destination width |

**FEC_MESH_SIZE**

Address: Operational Base + offset (0x0C8C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:22 | RO | 0x000 | reserved |
| 21:0 | RW | 0x000000 | sw_mesh_size<br>FEC mesh size<br>act_width_ex = 32*((sw_fec_act_width+31)/32)<br>act_height_ex = 32*((sw_fec_act_height+31)/32)<br>spb_num = (act_height_x+127)/128<br>left_height = ((act_height_ex % 128) == 0) ? 128 :<br>(act_height_ex % 128)<br>mesh_width = (sw_fec_mesh_density == 1) ?<br>(act_width_ex/32+1) : (act_width_ex/16+1)<br>mesh_height = (sw_fec_mesh_density == 1) ? (128/16+1) :<br>(128/8+1)<br>mesh_left_height = (sw_fec_mesh_density == 1) ?<br>(left_height/16+1) : (left_height/8+1)<br>spb_mesh_size = mesh_width * mesh_height<br>mesh_size = (spb_num - 1) * mesh_width * mesh_height +<br>mesh_width * mesh_left_height |

**FEC_DMA_STATUS**

Address: Operational Base + offset (0x0C90)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:14 | RO | 0x00000 | reserved |
| 13 | RO | 0x0 | bound_v_err<br>FEC bound vertical error |
| 12 | RO | 0x0 | bound_h_err<br>FEC bound horizontal error |
| 11 | RO | 0x0 | blkline_err_v<br>FEC blockline vertical error |
| 10 | RO | 0x0 | blkline_err_h<br>FEC blockline horizontal error |
| 9 | RO | 0x0 | blk_err_v<br>FEC blockline vertical error |
| 8 | RO | 0x0 | blk_err_h<br>FEC block horizontal error |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 7 | RO | 0x0 | pbuf_pp_fail<br>FEC pixel buffer ping-pong switch fail |
| 6 | RO | 0x0 | minbuf_pp_fail<br>FEC mesh buffer ping-pong switch fail |
| 5 | RO | 0x0 | reserved |
| 4 | RO | 0x0 | pic_dma_active<br>FEC Pixel DMA active<br>1'b0: DMA is not working<br>1'b1: DMA is working |
| 3 | RO | 0x0 | reserved |
| 2 | RO | 0x0 | mesh_y_dma_active<br>FEC MESH Y DMA active<br>1'b0: DMA is not working<br>1'b1: DMA is working |
| 1 | RO | 0x0 | reserved |
| 0 | RO | 0x0 | mesh_x_dma_active<br>FEC MESH X DMA active<br>1'b0: DMA is not working<br>1'b1: DMA is working |

**FEC_SRC_SIZE**

Address: Operational Base + offset (0x0C98)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:29 | RO | 0x0 | reserved |
| 28:16 | RW | 0x0000 | sw_fec_src_height<br>FEC source height |
| 15:13 | RO | 0x0 | reserved |
| 12:0 | RW | 0x0000 | sw_fec_src_width<br>FEC source width |

**FEC_MMU_DTE_ADDR**

Address: Operational Base + offset (0x0F00)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RW | 0x0000000 | MMU_DTE_ADDR<br>MMU current page Table address |
| 3:0 | RO | 0x0 | reserved |

**FEC_MMU_STATUS**

Address: Operational Base + offset (0x0F04)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:11 | RO | 0x000000 | reserved |
| 10:6 | RO | 0x00 | PAGE_FAULT_BUS_ID<br>Index of master responsible for last page fault |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 5 | RO | 0x0 | PAGE_FAULT_IS_WRITE<br>The direction of access for last page fault:<br>1'b0: Read<br>1'b1: Write |
| 4 | RO | 0x1 | REPLAY_BUFFER_EMPTY<br>The MMU replay buffer is empty |
| 3 | RO | 0x1 | MMU_IDLE<br>The MMU is idle when accesses are being translated and there are no unfinished translated accesses |
| 2 | RO | 0x0 | STAIL_ACTIVE<br>MMU stall mode currently enabled. The mode is enabled by command |
| 1 | RO | 0x0 | PAGE_FAULT_ACTIVE<br>MMU page fault mode currently enabled. The mode is enabled by command |
| 0 | RO | 0x0 | PAGING_ENABLED<br>Paging is enabled |

**FEC_MMU_COMMAND**

Address: Operational Base + offset (0x0F08)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2:0 | WO | 0x0 | MMU_CMD<br>MMU_CMD. This can be:<br>3'b000: MMU_ENABLE_PAGING<br>3'b001: MMU_DISABLE_PAGING<br>3'b010: MMU_ENABLE_STALL<br>3'b011: MMU_DISABLE_STALL<br>3'b100: MMU_ZAP_CACHE<br>3'b101: MMU_PAGE_FAULT_DONE<br>3'b110: MMU_FORCE_RESET |

**FEC_MMU_PAGE_FAULT_ADDR**

Address: Operational Base + offset (0x0F0C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x00000000 | PAGE_FAULT_ADDR<br>MMU address of last page fault |

**FEC_MMU_ZAP_ONE_LINE**

Address: Operational Base + offset (0x0F10)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | WO | 0x00000000 | MMU_ZAP_ONE_LINE<br>MMU address to be invalidated from the page table cache |

**FEC_MMU_INT_RAWSTAT**

*Copyright 2022 © Rockchip Electronics Co., Ltd.* 

Address: Operational Base + offset (0x0F14)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RO | 0x0 | READ_BUS_ERROR<br>Read bus error |
| 0 | RO | 0x0 | PAGE_FAULT<br>Page fault |

**FEC_MMU_INT_CLEAR**

Address: Operational Base + offset (0x0F18)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | WO | 0x0 | READ_BUS_ERROR<br>Read bus error |
| 0 | WO | 0x0 | PAGE_FAULT<br>Page fault |

**FEC_MMU_INT_MASK**

Address: Operational Base + offset (0x0F1C)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | READ_BUS_ERROR<br>Read bus error |
| 0 | RW | 0x0 | PAGE_FAULT<br>Page fault |

**FEC_MMU_INT_STATUS**

Address: Operational Base + offset (0x0F20)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RO | 0x0 | READ_BUS_ERROR<br>Read bus error |
| 0 | RO | 0x0 | PAGE_FAULT<br>Page fault |

**FEC_MMU_AUTO_GATING**

Address: Operational Base + offset (0x0F24)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | mmu_bug_fixed_disable<br>MMU bug fixed disable, must be 1 |
| 30:2 | RO | 0x00000000 | reserved |
| 1 | RO | 0x1 | mmu_cfg_mode<br>MMU configuration mode |
| 0 | RW | 0x1 | mmu_auto_gating<br>When it is 1'b1, the MMU will auto gate itself |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**FEC_MMU_REG_LOAD_EN**

Address: Operational Base + offset (0x0F28)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:1 | RO | 0x00000000 | reserved |
| 0 | RW | 0x0 | reg_load_mmu_en<br>MMU register load enable |

# 38.5 Application Notes

## 38.5.1 Setup Flow

- setting meshgrid information
  - sw_mesh_xint_base, aligned to 16B
  - sw_mesh_xfra_base, aligned to 16B
  - sw_mesh_yint_base, aligned to 16B
  - sw_mesh_yfra_base, aligned to 16B
- setting source information
  - setting sw_pic_y_base/sw_pic_c_base, aligned to 16B
  - setting source format YUV420/YUV422/YUV422I
  - setting sw_fec_src_width, sw_fec_src_height
  - setting sw_rd_vir_stride, word unit, aligned to 16B
- setting destination information
  - setting sw_wr_y_base/sw_wr_uv_base, aligned to 16B
  - setting destination YUV420/YUV422/YUV422I
  - setting sw_fec_act_width, sw_fec_act_height
  - setting sw_wr_vir_stride, word unit, aligned to 16B
- set sw_cfg_force_upd for FEC
- set sw_fec_st

## 38.5.2 Note

- It is recommended malloc one line more than original source buffer in DDR. For example, 1920x1080 source recommended 1920x1081 in DDR. When the boundary is accessed, since the internal DMA accesses at least 16 pixels, it may access the data of the next line.
- It is recommended that MMU is turned off to improve performance.
- Max mesh value must <= 8189

Copyright 2022 © Rockchip Electronics Co., Ltd.

# Chapter 39 Pulse Density Modulation Interface Controller

## 39.1 Overview

The PDM interface controller and decoder support mono PDM format. It integrates a clock generator driving the PDM microphone and embeds filters which decimate the incoming bit stream to obtain most common audio rates.
There are two PDM controllers in the SOC. PDM0/PDM1 both support the following features:

- Support one internal 32-bit wide and 128-location deep FIFOs for receiving audio data
- Support receive FIFO full, overflow interrupt and all interrupts can be masked
- Support configurable water level of receive FIFO full interrupt
- Support combined interrupt output
- Support AHB bus slave interface
- Support DMA handshaking interface and configurable DMA water level
- Support PDM master receive mode
- Support 4 paths. Each path is composed of two digital microphone channels. It can be used with four stereo or eight mono microphones. Each path is enabled or disabled independently
- Support 16~24-bit sample resolution
- Support sample rate: 8kHz,16kHz,32kHz,64kHz,128kHz,11.025kHz,22.05kHz,44.1kHz,88.2kHz,176.4kHz,12kHz,24kHz,48kHz,96kHz,192kHz
- Support two 16-bit audio data store together in one 32-bit wide location
- Support 16 to 31-bit audio data left or right justified in 32-bit wide FIFO
- Support programmable left and right channel exchange

## 39.2 Block Diagram

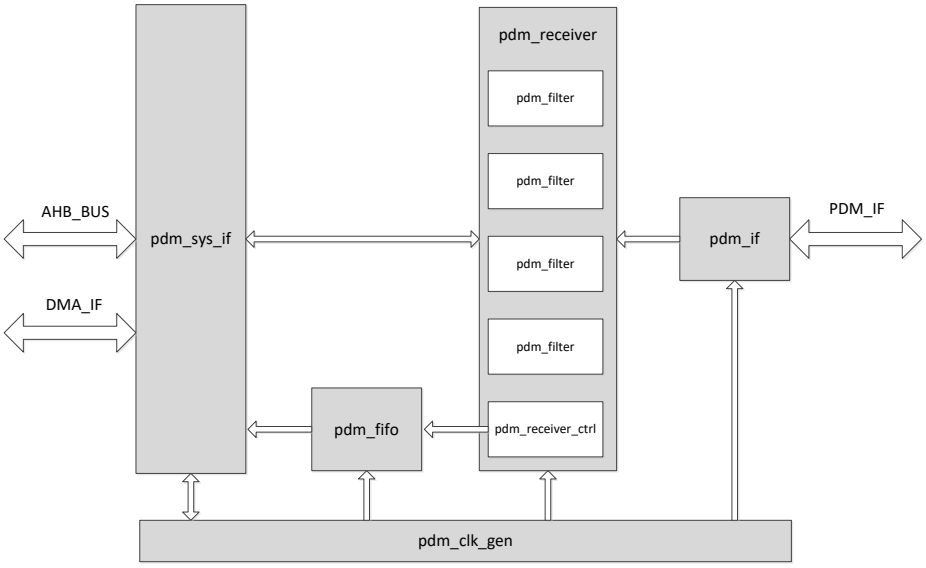



Fig. 39-1 PDM Block Diagram

**System Interface**
The system interface implements the APB slave operation. It contains not only control registers of receiver inside but also interrupt and DMA handshaking interface.
**Clock Generator**
The Clock Generator implements clock generation function. The input source clock to the module is MCLK, and by the divider of the module, the clock generator generates CLK_PDM to receiver.
**Receiver**
The receiver can act as a decimation filter of PDM. And export PCM format data.
**Receive FIFO**
The Receive FIFO is the buffer to store received audio data. The size of the FIFO is 32bits x 128.

Copyright 2022 © Rockchip Electronics Co., Ltd. 

# 39.3 Function Description

## 39.3.1 AHB Interface

There is an AHB slave interface in PDM. It is responsible for accessing registers.

## 39.3.2 PDM Interface

The PDM interface is a 5-wire interface. The PDM module can support up to four external stereo and eight digital microphones.

Following shows two cases of usage of the PDM, but all configurations are possible with stereo and mono digital microphones.

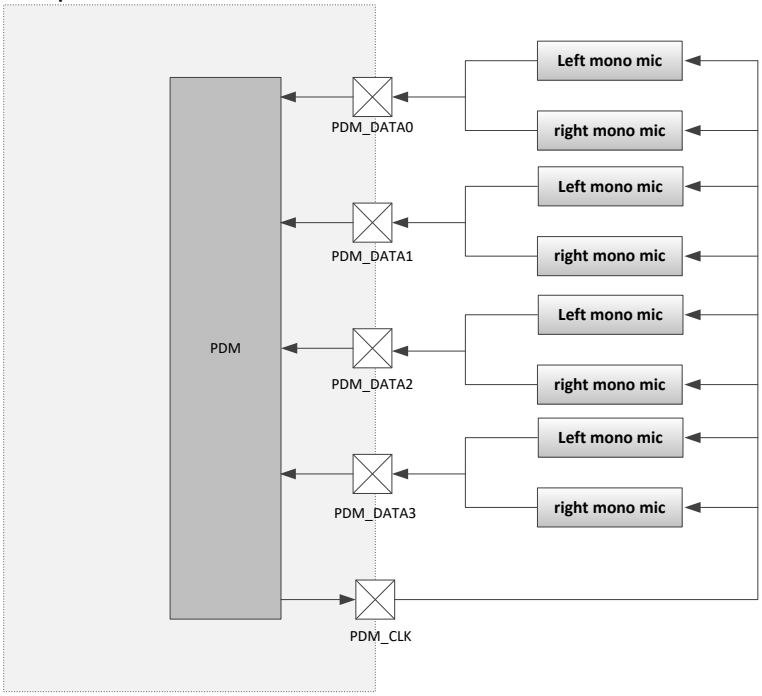



Fig. 39-2 PDM with Eight Mono MIC

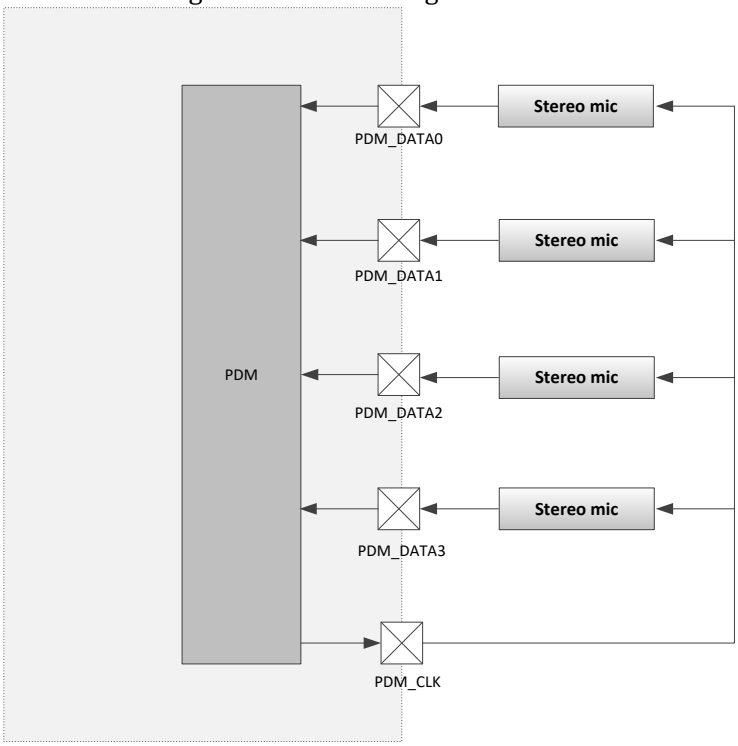



Fig. 39-3 PDM with Four Stereo MIC

The PDM interface consists of a serial-data shift clock output (PDM_CLK) and a serial data input (PDM_DATA). The clock is fanned out to both digital MICs, and both digital MICs' data

Copyright 2022 © Rockchip Electronics Co., Ltd. 

(left channel and right channel) outputs share a single signal line. To share a single line, the digital MICs tri-state their output during one phase of the clock (high or low part of cycle, depending on how they are configured via their L/R input).

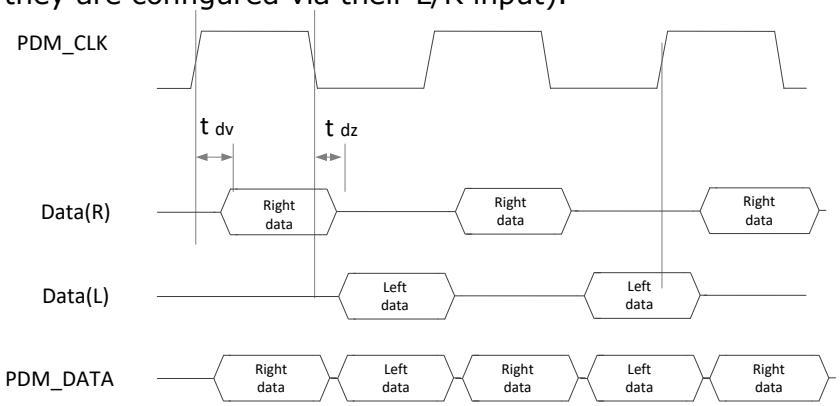



Fig. 39-4 PDM interface diagram with external MIC

### 39.3.3 Digital Filter

The external PDM MIC generates a PDM stream of bits and transfers it in one period or one half-period of the clock provided by the PDM. The aim of the PDM is to process data from the PDM interface, decimate and filter the data, and store the processed data in the FIFO.

The four paths are identical. Each path is composed of a left and a right channel. The PDM interface delivers eight parallel data of 1bit. Each bit goes to a filter. The aim of the filter is to limit the noise and export PCM format audio data.

### 39.3.4 Frequency Configuration

MCLK is the source clock signal. PDM_CLK is the output clocks generated in the PDM and is fed to the external microphones. They are also the internal clock of the external microphones. User must take care about the frequency of PDM_CLK when selecting the source clock (MCLK).

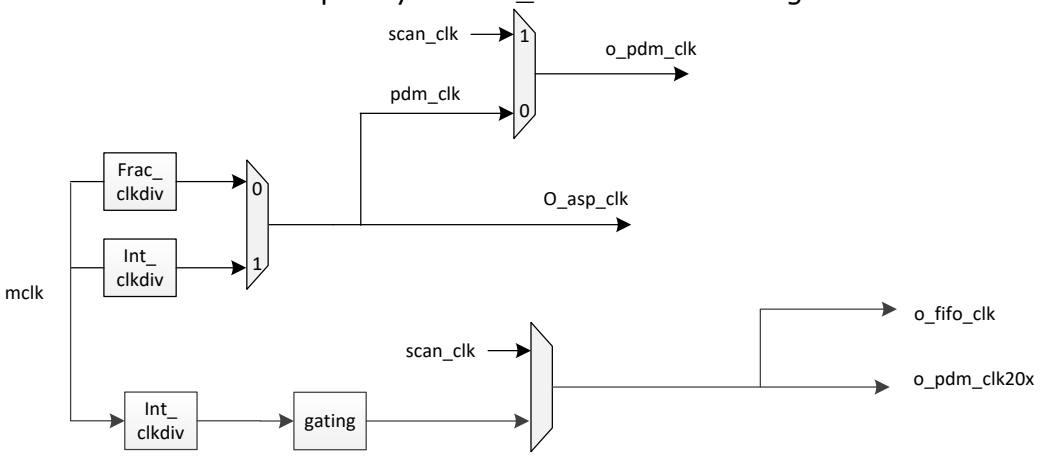



Fig. 39-5 PDM Clock Structure

Table 39-1 Relation between PDM_CLK and Sample Rate

| PDM_CLK | Sample Rate |
|---|---|
| 3.072MHz | 12kHz,24kHz,48kHz,96kHz,192kHz |
| 2.8224MHz | 11.025kHz,22.05kHz,44.1kHz,88.2kHz,176.4kHz |
| 2.048MHz | 8kHz,16kHz,32kHz,64kHz,128kHz |

## 39.4 Register Description

### 39.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Copyright 2022 © Rockchip Electronics Co., Ltd.

## 39.4.2 Registers Summary

| Name | Offset | Size | Reset Value | Description |
|---|---|---|---|---|
| PDM_SYSCONFIG | 0x0000 | W | 0x00000000 | PDM System Configure Register |
| PDM_CTRL0 | 0x0004 | W | 0x78000377 | PDM Control Register 0 |
| PDM_CTRL1 | 0x0008 | W | 0x0bb8ea60 | PDM Control Register 1 |
| PDM_CLK_CTRL | 0x000c | W | 0x0000e401 | PDM Clock Control Register |
| PDM_HPF_CTRL | 0x0010 | W | 0x00000000 | PDM High-pass Filter Control Register |
| PDM_FIFO_CTRL | 0x0014 | W | 0x00000000 | PDM FIFO Control Register |
| PDM_DMA_CTRL | 0x0018 | W | 0x0000001f | PDM DMA Control Register |
| PDM_INT_EN | 0x001c | W | 0x00000000 | PDM Interrupt Enable Register |
| PDM_INT_CLR | 0x0020 | W | 0x00000000 | PDM Interrupt Clear Register |
| PDM_INT_ST | 0x0024 | W | 0x00000000 | PDM Interrupt Status Register |
| PDM_RXFIFO_DATA_REG | 0x0030 | W | 0x00000000 | PDM Receive FIFO Data Register |
| PDM_DATA0R_REG | 0x0034 | W | 0x00000000 | PDM Path0 Right Channel Data Register |
| PDM_DATA0L_REG | 0x0038 | W | 0x00000000 | PDM Path0 Left Channel Data Register |
| PDM_DATA1R_REG | 0x003c | W | 0x00000000 | PDM Path1 Right Channel Data Register |
| PDM_DATA1L_REG | 0x0040 | W | 0x00000000 | PDM Path1 Left Channel Data Register |
| PDM_DATA2R_REG | 0x0044 | W | 0x00000000 | PDM Path2 Right Channel Data Register |
| PDM_DATA2L_REG | 0x0048 | W | 0x00000000 | PDM Path2 Left Channel Data Register |
| PDM_DATA3R_REG | 0x004c | W | 0x00000000 | PDM Path3 Right Channel Data Register |
| PDM_DATA3L_REG | 0x0050 | W | 0x00000000 | PDM Path3 Left Channel Data Register |
| PDM_DATA_VALID | 0x0054 | W | 0x00000000 | PDM Path Data Valid Register |
| PDM_VERSION | 0x0058 | W | 0x59313031 | PDM Version Register |
| PDM_INCR_RXDR | 0x0400 | W | 0x00000000 | Increment Address Receive FIFO Data Register |

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

## 39.4.3 Detail Registers Description

### PDM_SYSCONFIG

Address: Operational Base + offset (0x0000)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:3 | RO | 0x00000000 | reserved |
| 2 | RW | 0x0 | rx_start<br>RX transfer start bit<br>1'b0: Stop RX transfer<br>1'b1: Start RX transfer |
| 1 | RO | 0x0 | reserved |
| 0 | RW | 0x0 | rx_clr<br>PDM RX logic clear<br>This is a self-cleared bit. High active.<br>Write 1'b1: Clear RX logic<br>Write 1'b0: No action<br>Read 1'b1: Clear ongoing<br>Read 1'b0: Clear done |

### PDM_CTRL0

Address: Operational Base + offset (0x0004)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31 | RW | 0x0 | sjm_sel<br>Store justified mode<br>Can be written only when SYSCONFIG[2] is 0.<br>16bit~31bit DATA stored in 32 bits width FIFO.<br>If VDW select 16bit data, this bit is valid only when HWT select 1. Because if HWT is 0, every FIFO unit contains two 16bit data and 32 bit space is full, it is impossible to choose justified mode.<br>1'b0: Right justified<br>1'b1: Left justified |
| 30 | RW | 0x1 | path3_en<br>Path 3 enable<br>1'b1: Enable<br>1'b0: Disable |
| 29 | RW | 0x1 | path2_en<br>Path 2 enable<br>1'b1: Enable<br>1'b0: Disable |
| 28 | RW | 0x1 | path1_en<br>Path 1 enable<br>1'b1: Enable<br>1'b0: Disable |
| 27 | RW | 0x1 | path0_en<br>Path 0 enable<br>1'b1: Enable<br>1'b0: Disable |
| 26 | RW | 0x0 | hwt_en<br>Halfword word transform<br>Only valid when VDW select 16bit data.<br>1'b0: 32 bit data valid to AHB/APB bus. Low 16 bit for left channel and high 16 bit for right channel.<br>1'b1: Low 16bit data valid to AHB/APB bus, high 16 bit data invalid |
| 25 | RW | 0x0 | filter_gate_en<br>Filter gate enable<br>If some filters not work, the filter and its corresponding memory clock will be gated if filter_gate_en is 1'b1, otherwise the clock will be still active. |
| 24 | RW | 0x0 | sig_scale_mode<br>Signal scale mode select<br>1'b0: CIC outputs the normal latitude.<br>1'b1: Scale the CIC outputs to half of the normal latitude and scale 2 times after hpf-filter. |
| 23:16 | RW | 0x00 | int_div_20x_con<br>Integer divider for PDM filter operation.<br>This divider is used to generate internal logic operation clock from PDM input clock(mclk).<br>Int_div_20x_con=(mclk/(frequency of internal logic operation clock))-1. Int_div_20x_con can be any value from 0 to 255. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 15:8 | RW | 0x03 | int_div_con<br>Integer divider<br>This divider is used to generate sample clock from PDM input clock(mclk).<br>Int_div_con=(mclk/(frequency of sample clock))-1. Int_div_con can be any value from 0 to 255.<br>Can be written only when SYSCONFIG[2] is 0. |
| 7:5 | RW | 0x3 | sample_rate_sel<br>Selects which kind of sample rate.<br>3'b000: 12kHz/11.024kHz/8kHz<br>3'b001: 24kHz/22.05kHz/16kHz<br>3'b010: 32kHz<br>3'b011: 48kHz/44.1kHz<br>3'b100: 96kHz/88.2kHz/64kHz<br>3'b101~3'b111: 192kHz/176.4kHz/128kHz |
| 4:0 | RW | 0x17 | data_vld_width<br>Can be written only when SYSCONFIG[2] is 0.<br>Valid Data width<br>0~14: Reserved<br>15: 16bit<br>16: 17bit<br>17: 18bit<br>18: 19bit<br>.....<br>n: (n+1)bit<br>.....<br>23: 24bit |

**PDM_CTRL1**

Address: Operational Base + offset (0x0008)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RW | 0x0bb8 | frac_div_numerator<br>Fraction divider numerator<br>Can be written only when SYSCONFIG[2] is 0. |
| 15:0 | RW | 0xea60 | frac_div_denomonator<br>Fraction divider denominator<br>Can be written only when SYSCONFIG[2] is 0. |

**PDM_CLK_CTRL**

Address: Operational Base + offset (0x000c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:16 | RO | 0x0000 | reserved |
| 15:14 | RW | 0x3 | rx_path_select3<br>RX Path Select<br>2'b00: Path3 data from PDM data0<br>2'b01: Path3 data from PDM data1<br>2'b10: Path3 data from PDM data2<br>2'b11: Path3 data from PDM data3 |
| 13:12 | RW | 0x2 | rx_path_select2<br>RX Path Select<br>2'b00: Path2 data from PDM data0<br>2'b01: Path2 data from PDM data1<br>2'b10: Path2 data from PDM data2<br>2'b11: Path2 data from PDM data3 |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 11:10 | RW | 0x1 | rx_path_select1<br>RX Path Select<br>2'b00: Path1 data from PDM data0<br>2'b01: Path1 data from PDM data1<br>2'b10: Path1 data from PDM data2<br>2'b11: Path1 data from PDM data3 |
| 9:8 | RW | 0x0 | rx_path_select0<br>RX Path Select<br>2'b00: Path0 data from PDM data0<br>2'b01: Path0 data from PDM data1<br>2'b10: Path0 data from PDM data2<br>2'b11: Path0 data from PDM data3 |
| 7:6 | RO | 0x0 | reserved |
| 5 | RW | 0x0 | pdm_clk_en<br>PDM clk enable, working at PDM mode.<br>Can be written only when SYSCONFIG[2] is 0.<br>1'b0: PDM clk disable<br>1'b1: PDM clk enable |
| 4 | RW | 0x0 | div_type_sel<br>Divider type select signal<br>Can be written only when SYSCONFIG[2] is 0.<br>1'b0: Fraction divider<br>1'b1: Integer divider |
| 3 | RW | 0x0 | lr_ch_ex<br>Left and right channel data exchange<br>1'b0: Not inverted<br>1'b1: Inverted |
| 2 | RW | 0x0 | fir_com_bps<br>Fir compensate filter bypass<br>1'b0: Not bypass<br>1'b1: Bypass |
| 1:0 | RW | 0x0 | cic_ds_ratio<br>CIC filter decimation ratio<br>2'b00: 16 times decimation<br>2'b01: 8 times decimation<br>2'b10: 4 times decimation<br>other: 8 times decimation |

**PDM_HPF_CTRL**

Address: Operational Base + offset (0x0010)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3 | RW | 0x0 | hpfle<br>High-pass filter enable for left channel<br>1'b0: High pass filter for right channel is disabled.<br>1'b1: High pass filter for right channel is enabled. |
| 2 | RW | 0x0 | hpfre<br>High-pass filter enable for right channel<br>1'b0: High pass filter for right channel is disabled.<br>1'b1: High pass filter for right channel is enabled. |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 1:0 | RW | 0x0 | hpf_cf<br>High-pass filter configure<br>2'b00: 3.79Hz<br>2'b01: 60Hz<br>2'b10: 243Hz<br>2'b11: 493Hz |

**PDM_FIFO_CTRL**

Address: Operational Base + offset (0x0014)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:15 | RO | 0x00000 | reserved |
| 14:8 | RW | 0x00 | rft<br>Receive FIFO threshold<br>When the number of receive FIFO entries is more than or equal to this threshold plus 1, the receive FIFO threshold interrupt is triggered. |
| 7:0 | RO | 0x00 | rfl<br>Receive FIFO level<br>Contains the number of valid data entries in the receive FIFO. |

**PDM_DMA_CTRL**

Address: Operational Base + offset (0x0018)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:9 | RO | 0x000000 | reserved |
| 8 | RW | 0x0 | rde<br>Receive DMA enable<br>1'b0: Receive DMA disabled<br>1'b1: Receive DMA enabled |
| 7 | RO | 0x0 | reserved |
| 6:0 | RW | 0x1f | rdl<br>Receive data level<br>This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1. |

**PDM_INT_EN**

Address: Operational Base + offset (0x001c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | rxoie<br>RX overflow interrupt enable<br>1'b0: Disable<br>1'b1: Enable |
| 0 | RW | 0x0 | rxftie<br>RX full threshold interrupt enable<br>1'b0: Disable<br>1'b1: Enable |

**PDM_INT_CLR**

Address: Operational Base + offset (0x0020)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RW | 0x0 | rxoic<br>RX overflow interrupt clear (high active and auto cleared). |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**PDM_INT_ST**

Address: Operational Base + offset (0x0024)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:2 | RO | 0x00000000 | reserved |
| 1 | RO | 0x0 | rxoi<br>RX overflow interrupt<br>1'b0: Inactive<br>1'b1: Active |
| 0 | RO | 0x0 | rxfi<br>RX full interrupt<br>1'b0: Inactive<br>1'b1: Active |

**PDM_RXFIFO_DATA_REG**

Address: Operational Base + offset (0x0030)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | rxdr<br>Receive FIFO shadow register<br>When the register is read, data in the receive FIFO is accessed. |

**PDM_DATA0R_REG**

Address: Operational Base + offset (0x0034)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | data0r<br>Data of the path 0 right channel |

**PDM_DATA0L_REG**

Address: Operational Base + offset (0x0038)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | data0l<br>Data of the path 0 left channel |

**PDM_DATA1R_REG**

Address: Operational Base + offset (0x003c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | data1r<br>Data of the path 1 right channel |

**PDM_DATA1L_REG**

Address: Operational Base + offset (0x0040)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | data1l<br>Data of the path 1 left channel |

**PDM_DATA2R_REG**

Address: Operational Base + offset (0x0044)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | data2r<br>Data of the path 2 right channel |

**PDM_DATA2L_REG**

Address: Operational Base + offset (0x0048)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | data2l<br>Data of the path 2 left channel |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

**PDM_DATA3R_REG**

Address: Operational Base + offset (0x004c)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | data3r<br>Data of the path 3 right channel |

**PDM_DATA3L_REG**

Address: Operational Base + offset (0x0050)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | data3l<br>Data of the path 3 left channel |

**PDM_DATA_VALID**

Address: Operational Base + offset (0x0054)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:4 | RO | 0x0000000 | reserved |
| 3 | WO | 0x0 | path0_vld<br>1'b0: DATA0R_REG, DATA0L_REG value is invalid.<br>1'b1: DATA0R_REG, DATA0L_REG value is valid. |
| 2 | WO | 0x0 | path1_vld<br>1'b0: DATA1R_REG, DATA1L_REG value is invalid.<br>1'b1: DATA1R_REG, DATA1L_REG value is valid. |
| 1 | WO | 0x0 | path2_vld<br>1'b0: DATA2R_REG, DATA2L_REG value is invalid.<br>1'b1: DATA2R_REG, DATA2L_REG value is valid. |
| 0 | WO | 0x0 | path3_vld<br>1'b0: DATA3R_REG, DATA3L_REG value is invalid.<br>1'b1: DATA3R_REG, DATA3L_REG value is valid. |

**PDM_VERSION**

Address: Operational Base + offset (0x0058)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RW | 0x59313031 | version<br>PDM version |

**PDM_INCR_RXDR**

Address: Operational Base + offset (0x0400)

| Bit | Attr | Reset Value | Description |
|---|---|---|---|
| 31:0 | RO | 0x00000000 | receive_fifo_data<br>FIFO data can be read from these registers. This register is used when the access address is increment. |

## 39.5 Interface Description

There are two groups of IO interfaces embedded in the chip for each PDM. Following tables show the group 0 and group 1 of PDM0 IO interface respectively.

Table 39-2 Group 0 PDM0 IO Interface Description

| Module Pin | Direction | Pin Name | IOMUX Setting |
|---|---|---|---|
| o_pdm_clk0 | O | PDM0_CLK0_M0/I2C4_SDA_M4/PWM15_IR_M2/GPIO1_C6_d | BUS_IOC_GPIO1C_IOMUX_SEL_H[11:8]=4'h3 |
| o_pdm_clk1 | O | PDM0_CLK1_M0/I2C2_SDA_M3/PWM11_IR_M2/SPI4_CS1_M0/GPIO1_C4_d | BUS_IOC_GPIO1C_IOMUX_SEL_H[3:0]=4'h3 |
| i_pdm_data0 | I | PDM0_SDI0_M0/SPI1_CS1_M2/GPIO1_D5_d | BUS_IOC_GPIO1D_IOMUX_SEL_H[7:4]=4'h3 |
| i_pdm_data1 | I | I2S0_SDO2/I2S0_SDI3/PDM0_SDI1_M0/I2C7_SDA_M0/UART6_RX_M2/SPI1_MOSI_M2/GPIO1_D1_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[7:4]=4'h3 |

*Copyright 2022 © Rockchip Electronics Co., Ltd.*

| | | | |
|---|---|---|---|
| i_pdm_data2 | I | I2S0_SDO3/I2S0_SDI2/PDM0_SDI2_M0/I2C1_SCL_M4/UART4_TX_M0/PWM0_M1/SPI1_CLK_M2/GPIO1_D2_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[11:8]=4'h3 |
| i_pdm_data3 | I | I2S0_SDI1/PDM0_SDI3_M0/I2C1_SDA_M4/UART4_RX_M0/PWM1_M1/SPI1_CS0_M2/GPIO1_D3_d | BUS_IOC_GPIO1D_IOMUX_SEL_L[15:12]=4'h3 |

Table 39-3 Group 1 PDM0 IO Interface Description

| Module Pin | Direction | Pin Name | IOMUX Setting |
|---|---|---|---|
| o_pdm_clk0 | O | PDM0_CLK0_M1/PWM1_M0/I2C2_SDA_M0/CAN0_RX_M0/SPI0_MOSI_M0/PCIE30X1_0_CLKREQN_M0/GPIO0_C0_d | PMU2_IOC_GPIO0C_IOMUX_SEL_L[3:0]=4'h2 |
| o_pdm_clk1 | O | PDM0_CLK1_M1/PWM2_M0/UART0_RX_M0/I2C4_SDA_M2/DP0_HPDIN_M1/PCIE30X1_0_WAKEN_M0/GPIO0_C4_d | PMU2_IOC_GPIO0C_IOMUX_SEL_H[3:0]=4'h2 |
| i_pdm_data0 | I | I2S1_SDI2_M1/PDM0_SDI0_M1/I2C6_SDA_M0/UART1_RTSN_M2/PWM6_M0/SPI0_MISO_M0/PCIE30X4_WAKEN_M0/GPIO0_C7_d | PMU2_IOC_GPIO0C_IOMUX_SEL_H[15:12]=4'h2 |
| i_pdm_data1 | I | I2S1_SDI3_M1/PDM0_SDI1_M1/I2C6_SCL_M0/UART1_CTSN_M2/PWM7_IR_M0/SPI3_MISO_M2/PCIE30X4_PERSTN_M0/GPIO0_D0_d | PMU2_IOC_GPIO0D_IOMUX_SEL_L[3:0]=4'h2 |
| i_pdm_data2 | I | I2S1_SDO2_M1/PDM0_SDI2_M1/PWM3_IR_M0/I2C1_SCL_M2/CAN2_RX_M1/HDMI_TX0_SDA_M1/SPI3_CS0_M2/PCIE30X2_PERSTN_M0/SATA_CPDET/GPIO0_D4_u | PMU2_IOC_GPIO0D_IOMUX_SEL_H[3:0]=4'h2 |
| i_pdm_data3 | I | PMIC_SLEEP6/PDM0_SDI3_M1/GPIO0_D6_d | PMU2_IOC_GPIO0D_IOMUX_SEL_H[11:8]=4'h2 |

*Notes: I=input, O=output, I/O=input/output, bidirectional*

Following tables show the group 0 and group 1 of PDM1 IO interface respectively.

Table 39-4 Group 0 PDM1 IO Interface Description

| Module Pin | Direction | Pin Name | IOMUX Setting |
|---|---|---|---|
| o_pdm_clk0 | O | SDMMC_CLK/PDM1_CLK0_M0/TEST_CLKOUT_M0/MCU_JTAG_TMS_M0/CAN0_RX_M1/UART5_TX_M0/GPIO4_D5_d | BUS_IOC_GPIO4D_IOMUX_SEL_H[7:4]=4'h2 |
| o_pdm_clk1 | O | SDMMC_CMD/PDM1_CLK1_M0/MCU_JTAG_TCK_M0/CAN0_TX_M1/UART5_RX_M0/PWM7_IR_M1/GPIO4_D4_u | BUS_IOC_GPIO4D_IOMUX_SEL_H[3:0]=4'h2 |
| i_pdm_data0 | I | SDMMC_D3/PDM1_SDI0_M0/JTAG_TMS_M0/I2C8_SDA_M0/UART5_RTSN_M0/PWM10_M1/GPIO4_D3_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[15:12]=4'h2 |
| i_pdm_data1 | I | SDMMC_D2/PDM1_SDI1_M0/JTAG_TCK_M0/I2C8_SCL_M0/UART5_CTSN_M0/GPIO4_D2_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[11:8]=4'h2 |
| i_pdm_data2 | I | SDMMC_D1/PDM1_SDI2_M0/JTAG_TMS_M1/I2C3_SDA_M4/UART2_RX_M1/PWM9_M1/GPIO4_D1_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[7:4]=4'h2 |
| i_pdm_data3 | I | SDMMC_D0/PDM1_SDI3_M0/JTAG_TCK_M1/I2C3_SCL_M4/UART2_TX_M1/PWM8_M1/GPIO4_D0_u | BUS_IOC_GPIO4D_IOMUX_SEL_L[3:0]=4'h2 |

Table 39-5 Group 1 PDM1 IO Interface Description

| Module Pin | Direction | Pin Name | IOMUX Setting |
|---|---|---|---|
| o_pdm_clk0 | O | PDM1_CLK0_M1/PCIE30X1_0_PERSTN_M2/UART7_RX_M2/SPI0_CS0_M2/GPIO1_B4_u | BUS_IOC_GPIO1B_IOMUX_SEL_H[3:0]=4'h2 |
| o_pdm_clk1 | O | PDM1_CLK1_M1/PCIE30X1_0_WAKEN_M2/SATA0_ACT_LED_M1/UART4_TX_M2/SPI0_CLK_M2/GPIO1_B3_d | BUS_IOC_GPIO1B_IOMUX_SEL_L[15:12]=4'h2 |
| i_pdm_data0 | I | PDM1_SDI0_M1/PCIE30X1_1_PERSTN_M2/PWM3_IR_M3/SPI2_CS0_M0/GPIO1_A7_u | BUS_IOC_GPIO1A_IOMUX_SEL_H[15:12]=4'h2 |
| i_pdm_data1 | I | PDM1_SDI1_M1/PCIE30X4_CLKREQN_M3/SPI2_CS1_M0/GPIO1_B0_u | BUS_IOC_GPIO1B_IOMUX_SEL_L[3:0]=4'h2 |

Copyright 2022 © Rockchip Electronics Co., Ltd.

| | | | |
|---|---|---|---|
| i_pdm_data2 | I | PDM1_SDI2_M1/PCIE30X4_WAKEN_M3/SPI0_MISO_M2/GPIO1_B1_d | BUS_IOC_GPIO1B_IOMUX_SEL_L[7:4]=4'h2 |
| i_pdm_data3 | I | PDM1_SDI3_M1/PCIE30X4_PERSTN_M3/UART4_RX_M2/SPI0_MOSI_M2/GPIO1_B2_d | BUS_IOC_GPIO1B_IOMUX_SEL_L[11:8]=4'h2 |

*Notes: I=input, O=output, I/O=input/output, bidirectional*

## 39.6 Application Notes

PDM usage flow is shown as following figure.

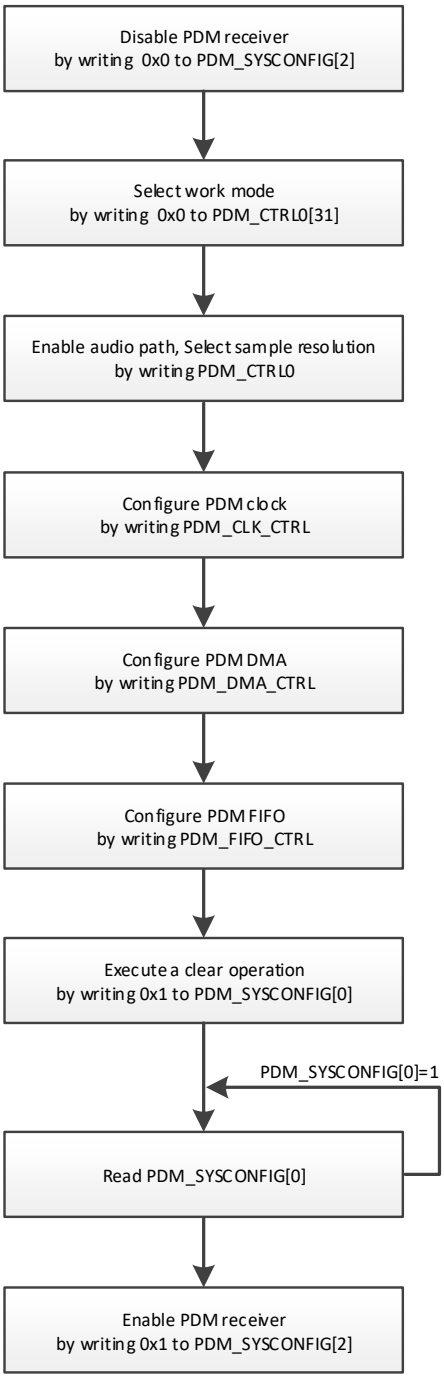



Fig. 39-6 PDM Operation Flow

Copyright 2022 © Rockchip Electronics Co., Ltd.